TQMxE39S
User's Manual

TQMxE39S UM 0104
2021-04-20

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	2018-02-16	FP		Initial release
0101	2019-01-15	WM	3.4.3.3	Type of supported SPI Boot Flash corrected
0102	2019-08-27	US	5.3, 6 8.3, 8.4, 8.5, 8.6	EAPI and BIOS chapters added Added
0103	2020-08-25	PF	Table 3	Values added and updated
0104	2021-04-20	PF	Table 10	Pins S157 and S158 added

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Through our website www.tq-group.com you could also get registered, to have access to restricted information and automatic update services.

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For service / RMA, please contact our service team by email (service@tq-group.com) or your dedicated sales team at TQ.

1.6 Tips on Safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and Typographic Conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.8 Handling and ESD Tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMxE39S and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of Signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.

The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.10 Further Applicable Documents / Presumed Knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used.
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

Implementation information for the carrier board design is provided in the SMARC Design Guide (2) maintained by the SGET (Standardization Group for Embedded Technologies). This Carrier Design Guide includes a very good guideline to design SMARC carrier board.

It includes detailed information with schematics and detailed layout guidelines.

Please refer to the official SGET documentation for additional information (1).

2. INTRODUCTION

The TQ module TQMxE39S is based on the latest generation of Intel® Atom™, Pentium® and Celeron® CPUs (code name "Apollo Lake"). It achieves a new level of computing performance, security and media processing performance in a very compact form factor to empower real-time computing, industrial automation, digital surveillance, aviation, medical, retail and more.

The TQMxE39S corresponds to the internationally established SGET standard SMARC (V2.0). 6 USB ports – including 2 USB 3.0 – and up to 4 PCIe lanes natively supported by the CPUs enable high bandwidth communication with peripherals and additional interfaces on the carrier board. With the latest Intel® graphics processor integrated, the TQMxE39S delivers 4K high resolution graphics output, immersive 3D processing and also greatly increased video encode and playback performance.

Time coordinated computing capabilities enable time synchronized processes within IoT networks and industrial control applications. On-board eMMC up to 64 Gbyte and the option for LVDS or native eDP enable flexibility and reduce overall BOM cost.

The integrated TQMx86 board controller enables high flexibility through "flexiCFG" and supports thermal management, watchdog, 16550 compatible UARTs, I²C controllers, and GPIO handling. Combined with options like conformal coating and optimized cooling solutions the TQMxE39S perfectly fits for mobile, low power, low profile and battery driven applications in multiple vertical markets like industrial automation, medical devices, transportation and others.

2.1 Functional Overview

The following key functions are implemented on the TQMxE39S:

CPU:

- Intel® Atom™ E3900 (“Apollo Lake-I“)
- Intel® Pentium® N4200 (“Apollo Lake“)
- Intel® Celeron® N3350 (“Apollo Lake“)

Memory:

- LPDDR4: 2 Gbyte, 4 Gbyte, 8 Gbyte
- eMMC 5.0 on-board flash up to 64 Gbyte
- EEPROM: 32 Kbit (24LC32)

Graphics:

- 1 × Digital Display Interface (DDI) (DP 1.2a, DVI, HDMI 1.4b)
- 1 × HDMI Interface (DVI, HDMI 1.4b)
- 1 × Embedded Digital Display Interface (eDDI) or LVDS interface (eDP 1.3 or LVDS)

Peripheral interfaces:

- 1 × Gigabit Ethernet (Intel® i210), external IEEE1588 sync optional
- 1 × SATA 3.0 (up to 6 Gb/s), eSATA capable
- 4 × PCIe 2.0 (up to 5 Gb/s) (4th lane optional, if no Ethernet)
- 2 × Camera interface MIPI CSI (2 and 4 lane)
- 4 × USB 2.0, 2 x USB 3.0 (1 x Host / 1 x Host/Client)
- 1 × Intel® HD audio (I) or I²S
- 1 × I²C (General Purpose; master/slave capable)
- 1 × SMBus
- 1 × SPI (for external uEFI BIOS flash)
- 4 × Serial port (Rx/Tx, legacy compatible)
- 1 × SD card interface
- 12 GPIO signals (multiplexed with fan / camera control and HD audio Reset)

Others:

- TQMx86 board controller with Watchdog and TQ-flexiCFG
- Hardware monitor

Power supply:

- Voltage: 4.75 V to 5.25 V
  3 V Battery for RTC

Environment:

- Standard Temperature: 0 °C to +60 °C
- Extended Temperature: –40 °C to +85 °C

Form factor / dimensions:

- SMARC short form factor; 82 mm × 50 mm

2.2 SMARC Specification Compliance

The TQMxE39S is compliant to the SMARC Hardware Specification (Version 2.0).

2.3 TQMxE39S Variants

The TQMxE39S is available in several standard configurations:

Table 2: TQMxE39S Module Variants

Module	CPU			SDRAM	eMMC	TDP	Graphics	Temp. Range
	Core	Clock	Cache					
TQMxE39S-AA	Intel Atom x7-E3950	4 × 1.6 / 2.0 GHz	2 MB	8 GB LPDDR4	32 GB	12 W	LVDS	–40 °C to +85 °C
TQMxE39S-AB	Intel Atom x5-E3940	4 × 1.6 / 1.8 GHz	2 MB	8 GB LPDDR4	32 GB	9.5 W	eDP	–40 °C to +85 °C
TQMxE39S-AC	Intel Atom x5-E3930	2 × 1.3 / 1.8 GHz	2 MB	4 GB LPDDR4	8 GB	6.5 W	LVDS	–40 °C to +85 °C
TQMxE39S-AD	Intel Celeron N3350	2 × 1.1 / 2.4 GHz	2 MB	4 GB LPDDR4	8 GB	6 W	LVDS	0 °C to +60 °C
TQMxE39S-AE	Intel Pentium N4200	4 × 1.1 / 2.5 GHz	2 MB	8 GB LPDDR4	32 GB	6 W	eDP	0 °C to +60 °C
TQMxE39S-AF	Intel Atom x5-E3940	4 × 1.6 / 1.8 GHz	2 MB	8 GB LPDDR4	32 GB	9.5 W	LVDS	–40 °C to +85 °C
TQMxE39S-AG	Intel Atom x7-E3950	4 × 1.6 / 2.0 GHz	2 MB	8 GB LPDDR4	32 GB	12 W	eDP	–40 °C to +85 °C

Please visit www.tq-group.com/TQMxE39S for a complete list of standard variants.
Other configurations are available on request.

Standard configuration features are:

- eDP or LVDS
- CPU version
- Memory configuration
- Temperature range

Optional hardware and software configuration features:

- Conformal coating can be offered as custom specific add-on
- Custom specific BIOS configuration

2.4 Accessories

TQMxE39S-HSP-E, TQMxE39S-HSP-N: Heat spreader for TQMxE39S according to the SMARC specification
Evaluation platform MB-SMARC-1:

- Mainboard for SMARC modules
- 170 mm × 170 mm
- Interfaces: DP, HDMI, eDP/LVDS, 2 × GbE, 1 × USB Type C, 1 x USB 3.0, 1 x USB 2.0, audio, Micro SD card, 4 x M.2 socket (Key E, B, B, M), 4 × RS232, 2 × CSI

3. FUNCTION

3.1 TQMxE39S Block Diagram

The following illustration shows the block diagram of the TQMxE39S:

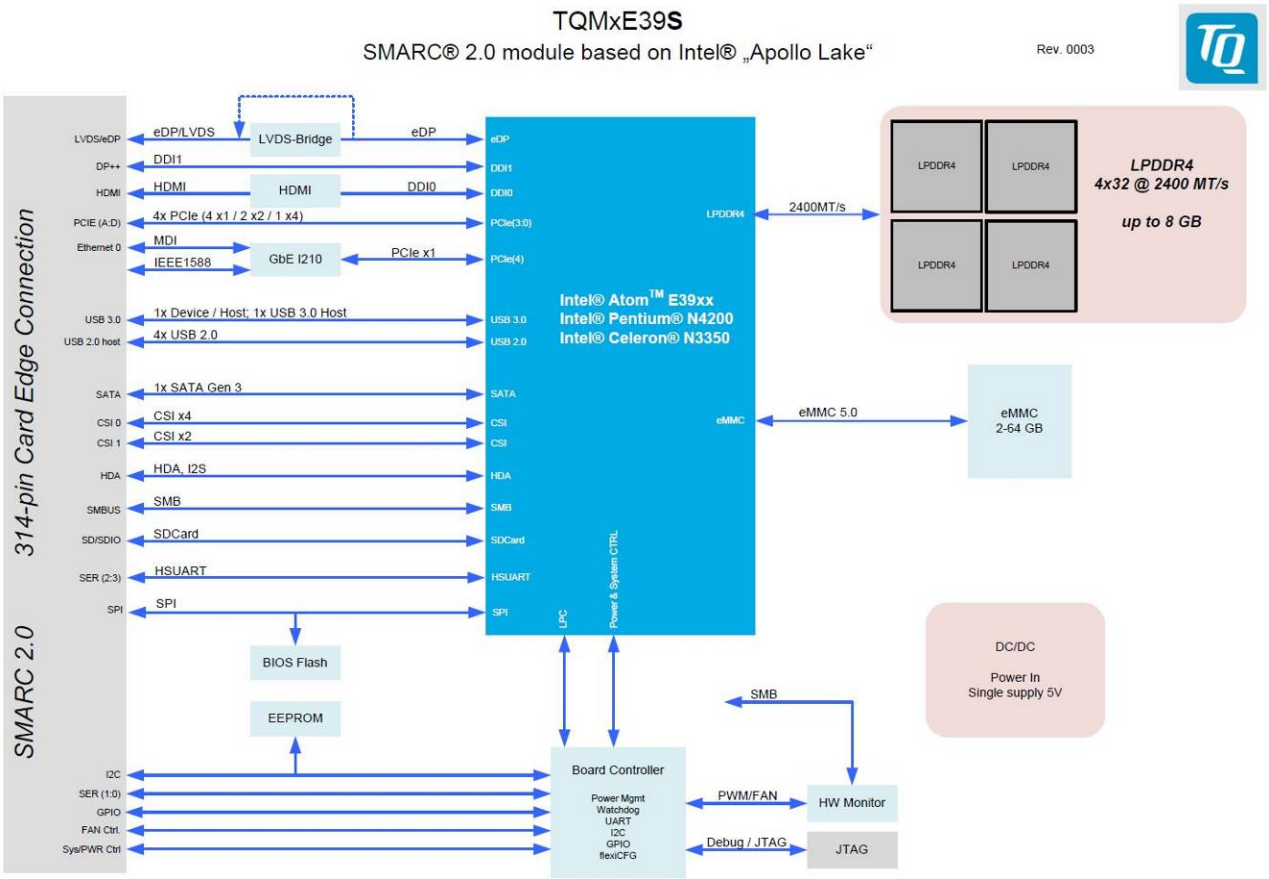

Figure 1: Block Diagram TQMxE39S

3.2 Electrical Characteristics

3.2.1 Supply Voltage

The TQMxE39S supports an input voltage from 4.75 V to 5.25 V.

The following supply voltages are specified at the SMARC connector:

- Main Power Rail: 4.75 V to 5.25 V max input ripple: ±100 mV
- VCC_RTC: 2.0 V to 3.3 V max input ripple: ±20 mV

The input voltages shall rise from 10 % of nominal to 90 % of nominal within 0.1 to 20 msec (0.1 msec ≤ Rise Time ≤ 20 msec).

There must be a smooth and continuous ramp of each DC output voltage from 10 % to 90 % of its final set point within the regulation band.

3.2.2 Power Consumption

The values below show voltage and power consumption details for the TQMxE39S.
The values were measured using the TQMxE39S and the MB-SMARC-1 carrier board.
The measurement was done with two power supplies, one for the TQMxE39S and one for the MB-SMARC-1 carrier board.
The power consumption of each TQMxE39S was measured running Windows® 10, 64 bit and a four chip LPDDR4 configuration (4 × 2 Gbyte). All measurements were done at a temperature of +25 °C and an input voltage of +5.0 V.
The power consumption of the TQMxE39S depends on the application, the mode of operation and the operating system.
The power consumption was measured under the following conditions:

- **Suspend mode:**
  The system is in S5/S4 state, Ethernet port is disconnected.
- **Windows 10, 64 bit, idle:**
  Desktop idles, Ethernet port is disconnected.
- **Windows 10, 64 bit, maximum load:**
  These values show the maximum worst case power consumption, achieved by using the Intel® stress test tool to apply maximum load to the cores only, and cores plus graphics engine, Ethernet port is connected (1000 Mbps Speed)
- **Windows 10, 64 bit, Suspend Mode:**
  The system is in S5/S4 state, Ethernet port is disconnected.

The following table shows the power consumption with different CPU configurations.

Table 3: TQMxE39S Power Consumption

Module	Mode		
	Suspend (OS shut down)	Win10, 64 bit idle	Win10, 64 bit max. load
E3950 with 8 Gbyte LPDDR4	0.33 W	1.7 W	16 W
E3940 with 8 Gbyte LPDDR4	0.33 W	1.7 W	11.5 W
E3930 with 8 Gbyte LPDDR4	0.33 W	1.7 W	8 W
N4200[1] with 8 Gbyte LPDDR4	0.33 W	1.7 W	13 W
N3350[1] with 8 Gbyte LPDDR4	0.4 W	1.7 W	13.2 W

Note: Power requirement	
	The power supplies on the carrier board for the TQMxE39S must be designed with enough reserve. The carrier board should provide at least twice the maximum workload power of the TQMxE39S. The TQMxE39S supports several low-power states. The power supply of the carrier board has to be stable even with no load.

1: Turbo Mode enabled.

3.2.2.1 Real Time Clock Power Consumption

The RTC (VCC_RTC) current consumption is shown below.
The values were measured at +25 °C under battery operating conditions.

Table 4: RTC Current Consumption

Integrated RTC	Voltage	Current
Intel® Atom™ E3900, Intel® Pentium® N4200, Intel® Celeron® N3350	3.0 V	3 µA

The current consumption of the RTC in the Intel® Atom™ E3900, Intel® Pentium® N4200, and Intel® Celeron® N3350 is specified in the Product Family Datasheet with 6 µA in average, but the values measured on several modules were lower.

3.3 Environmental Conditions

- Operating Temperature Standard: 0 °C to +60 °C
- Operating Temperature Extended: –40 °C to +85 °C
- Storage Temperature: –40 °C to +85 °C
- Relative humidity (operating / storage): 10 % to 90 % (non-condensing)

Attention: Maximum operating temperature	
	Do not operate the TQMxE39S without heat spreader or without heat sink! The heat spreader is not a sufficient heat sink!

3.4 System Components

3.4.1 CPUs

The TQMxE39S supports the Intel® Atom™ E3900, Intel® Pentium® N4200, and Intel® Celeron® N3350 CPUs.
The following list shows some key features of these CPUs:

- Quad and dual CPU cores
- Intel® 64 Architecture
- Intel® Virtualization Technology (VT-x)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Enhanced Intel® SpeedStep® technology
- 2 Mbyte Cache
- Intel® HD Graphics
- Triple independent displays

Table 5: Intel® Atom™ E3900, Intel® Pentium® N4200, and Intel® Celeron® N3350

Mode	N3350	N4200	x5-E3930	x5-E3940	x7-E3950
CPU Cores	2	4	2	4	4
Cache	2 Mbyte	2 Mbyte	2 Mbyte	2 Mbyte	2 Mbyte
CPU frequency HFM / Turbo	1.1 / 2.4 GHz	1.1 / 2.5 GHz	1.3 / 1.8 GHz	1.6 / 1.8 GHz	1.6 / 2.0 GHz
Temperature $T_{junction}$	0 °C to +105 °C	0 °C to +105 °C	–40 °C to +110 °C	–40 °C to +110 °C	–40 °C to +110 °C
Memory Speed	2400 MT/s	2400 MT/s	2133 MT/s	2133 MT/s	2400 MT/s
Max Memory	8 Gbyte	8 Gbyte	8 Gbyte	8 Gbyte	8 Gbyte
Max Memory Channels	4 x 32	4 x 32	4 x 32	4 x 32	4 x 32
Intel® HD Graphics Gen 9	500	505	500	500	505
GFX: No. of Execution Units	12	18	12	12	18
GFX: Base / Burst	200 / 650 MHz	200 / 750 MHz	400 / 550 MHz	400 / 600 MHz	500 / 650 MHz
Thermal Design Power (TDP)	6 W	6 W	6.5 W	9.5 W	12 W

3.4.2 Graphics

The Intel® Atom™ E3900, Intel® Pentium® N4200, and Intel® Celeron® N3350 CPUs includes an integrated Intel® HD (Gen 9) graphics accelerator. It provides excellent 2D/3D graphics performance with dual simultaneous display support.

The following list shows some key features of the Intel® Atom™ E3900, Intel® Pentium® N4200, and Intel® Celeron® N3350 CPUs:

- Graphics Technology (Gen 09 LP) with 12 Execution Units (HD Graphics 500) or 18 Execution Units (HD Graphics 505)
- Hardware accelerated video decoding/encoding for H.264, MPEG2, MVC, VC-1, WMV9, H.265/HEVC, VP9, JPEG/MJPAG
- Direct3D* 12, DirectX* 12 support
- OpenGL* 4.3, OpenCL* 1.2 support

The TQMxE39S supports one Digital Display Interface (DDI) one HDMI interface and one eDP or LVDS interface at the SMARC connector.

Table 6: Maximum Resolution in Dual Display Configuration

Display	Maximum Display Resolution
LVDS	1920 × 1200 @ 60 Hz (dual channel)
eDP	3840 × 2160 @ 60 Hz
DP	4096 × 2160 @ 60 Hz
HDMI	3840 × 2160 @ 30 Hz

3.4.3 Memory

3.4.3.1 LPDDR4 SDRAM

The TQMxE39S supports a memory-down configuration running at up to 2400 MT/s.
The maximum memory size is 8 Gbyte. The available memory configuration can be 2 Gbyte, 4 Gbyte or 8 Gbyte.

3.4.3.2 eMMC

The TQMxE39S supports up to 64 Gbyte on-board eMMC 5.0 flash (compatible with rev. 5.0).

3.4.3.3 SPI Boot Flash

The TQMxE39S provides a 128 Mbit SPI boot flash. It includes the Intel® Trusted Execution Engine and the uEFI BIOS.
An external SPI boot flash can be used instead of the on-board SPI boot flash.
The uEFI BIOS supports the following 1.8 V SPI flash devices on the carrier board:
Winbond W25Q128FW / GigaDevice GD25LQ128D
Ensure that the QE (Quad Enable) bit is 0. Otherwise the SPI boot flash won't work.

3.4.3.4 EEPROM

On the TQMxE39S there can be placed a 32 Kbit serial EEPROM on the I2C_GP bus. This feature is optional.

3.4.4 Real Time Clock

The TQMxE39S includes a standard RTC (Motorola MC146818B) integrated in the Intel® Atom™ E3900, Intel® Pentium® N4200 and Intel® Celeron® N3350 CPU.

3.4.5 Hardware Monitor

The TQMxE39S includes an integrated Hardware Monitor to monitor the on-board temperature, board voltages and manage a fan (GPIO5 / PWM_OUT and GPIO6 / TACHIN).

3.4.6 TQ flexible I/O configuration (TQ-flexiCFG)

The module includes a flexible I/O configuration feature, the TQ-flexiCFG.
Using the TQ-flexiCFG feature, several I/O interfaces and functions can be configured via a programmable FPGA.
Special embedded features and configuration options can be added to the TQMxE39S to reduce the carrier board design effort.
Here are some examples of the flexible I/O configuration:

- GPIO interrupt configuration
- Interrupt configuration via LPC Serial IRQ
- Serial Port handshake signals via GPIOs
- Integrate additional I/O functions, e.g. additional Serial, I^2C, PWM controller or special power management configurations

Please contact support@tq-group.com for further information about the TQ-flexiCFG.

3.5 Interfaces

3.5.1 PCI Express

The TQMxE39S with Intel® Atom™ E3900, Intel® Pentium® N4200, and Intel® Celeron® N3350 CPU supports a very flexible PCI Express configuration with up 4 PCI Express Gen 2 ports.
With a customized BIOS the PCI Express lanes can be configured as follows:

Table 7: PCI Express Configuration Options

SMARC Port 0 – 3	On-board Ethernet i210	Configuration
4 × 1 ports (maximum 3 ports enabled)	enabled	Configuration in the BIOS
4 × 1 ports	disabled	Configuration in the BIOS
2 × 2 ports	enabled	Configuration via custom BIOS
1 × 4 port	enabled	Configuration via custom BIOS

3.5.2 Gigabit Ethernet

The TQMxE39S provides the Intel® i210IT Ethernet controller with 10/100/1000 Mbps speed and IEEE1588 support.

3.5.3 Serial ATA

The TQMxE39S supports one SATA Gen 3.0 interface which supports up to 6 Gb/s.
The integrated SATA host controller supports AHCI mode, the SATA controller no longer supports legacy IDE mode using I/O space.

3.5.4 Digital Display Interface

The TQMxE39S supports three Digital Display Interfaces: DisplayPort, HDMI and Embedded DisplayPort (eDP)
The module either supports eDP or LVDS (assembly option).
The TQMxE39S supports the following maximum display resolutions:

- DisplayPort 1.2a: Up to 4096 × 2160 @ 60 Hz
- Embedded DisplayPort 1.3: Up to 3840 × 2160 @ 60 Hz
- HDMI 1.4b: Up to 3840 × 2160 @ 30 Hz
- DVI: Up to 3840 × 2160 @ 30 Hz (HDMI without Audio)

Please contact support@tq-group.com for further information about the display configuration.

3.5.5 LVDS Interface

The TQMxE39S supports an LVDS interface which is provided through an on-board eDP to LVDS bridge.
The eDP to LVDS bridge supports single or dual LVDS signalling with colour depths of 18 bits per pixel or 24 bits per pixel up to 112 MHz and a resolution up to 1920 × 1200 @ 60 Hz in dual LVDS mode. The LVDS data packing can be configured either in VESA or JEIDA format.
The eDP to LVDS bridge can emulate EDID ROM behaviour avoiding specific changes in system video BIOS, to support panels without EDID ROM.
Please contact support@tq-group.com for further information about the LVDS configuration.

3.5.6 USB 2.0 Interfaces

The TQMxE39S supports six USB 2.0 ports at the SMARC connector.

3.5.7 USB 3.0 Interfaces

The TQMxE39S supports two USB 3.0 ports at the SMARC connector.

Note: USB Port Mapping	
	USB 2.0 port 0 must be paired with USB 3.0 SuperSpeed port 0. USB 2.0 port 1 must be paired with USB 3.0 SuperSpeed port 1.

3.5.8 SD Card Interface

The TQMxE39S provides an SD card interface for 4-bit SD/MMC cards at the SMARC connector.

3.5.9 General Purpose Input/Output

The TQMxE39S provides twelve GPIO signals at the SMARC connector.
The GPIO signals are shared with camera control, fan Control and HD Audio Reset signals. They can be configured by software.
The GPIO signals are integrated in the TQ-flexiCFG block and can be configured flexible.
Therefore the signals can also be used for several special functionality (see 3.4.6).
Please contact support@tq-group.com for further information about the GPIO configuration and their alternate uses.

3.5.10 High Definition Audio Interface

The TQMxE39S provides a High Definition Audio (I) and an I^2 interface, which support Audio codecs at the SMARC connector. The audio codec on the carrier board should be supported by the BIOS of the TQMxE39S.
Please contact support@tq-group.com for further information.

3.5.11 MIPI CSI Camera Interface

The TQMxE39S supports two camera interfaces. 2-lane or 4-lane MIPI CSI cameras can be connected.

3.5.12 I^2C Bus

The TQMxE39S supports a general purpose I^2C bus via a dedicated LPC to I^2C controller, integrated in the TQ-flexiCFG block.
The I^2C host controller supports a clock frequency of up to 400 kHz and can be configured independently.

3.5.13 SMBus / Power Management I^2C Bus

The TQMxE39S provides an I^2C based SMBus interface. This bus is also called Power Management I^2C Bus.

3.5.14 Serial Peripheral Interface

The TQMxE39S provides an SPI interface. The SPI interface can only be used for SPI boot Flash devices.

3.5.15 Serial Ports

The TQMxE39S offers up to four UARTs (Universal Asynchronous Receiver and Transmitter). The register set of SER0 and SER1 is based on the industry standard 16550 UART. The UART operates with standard serial port drivers without requiring a custom driver to be installed. The 16 byte transmit and receive FIFOs reduce CPU overhead and minimize the risk of buffer overflow and data loss.

SER2 and SER3 are connected to the HSUART (High Speed UART) of the Intel® Atom™ E3900, Intel® Pentium® N4200, or Intel® Celeron® N3350 CPU.

TQ recommends preferring the usage of SER0 and SER1. There might be some problems with serial console when using the Intel® HSUARTs.

3.5.16 Watchdog Timer

The TQMxE39S supports a freely programmable two-stage Watchdog timer, integrated in the TQ-flexiCFG block.

There are four operation modes available for the Watchdog timer:

- Dual-stage mode
- Interrupt mode
- Reset mode
- Timer mode

The timeout of the Watchdog timer ranges from 125 msec to 1 h.

The SMARC Specification does not support external hardware triggering of the Watchdog.

An external Watchdog Trigger can be configured to GPIO pins at the SMARC connector with the TQ-flexiCFG feature.

3.6 Connectors

3.6.1 SMARC Connector

A 314 pin 0.5 mm pitch card edge connector is realized on the TQMxE39S PCB. On the carrier board a connector mechanical compatible to MXM3 graphic cards is used to contact the module. The stacking height is defined by the connector used on the carrier (e.g. 1.5 mm, 2.7 mm, 5 mm, and 8 mm are available).

3.6.2 TQM Debug Card

The TQM debug card is designed to provide access to several processor and chipset control signals. The uEFI BIOS Power-On Self-Test (POST) codes can be displayed through four hexadecimal display panels on the TQM debug card.

When the module is turned on, the hexadecimal display should show the uEFI BIOS POST codes. If the module does not boot, the uEFI BIOS POST has detected a fatal fault and stopped. The number showing in the hexadecimal display on the TQM debug card is the number of the test in which uEFI BIOS boot failed.

The debug card can be connected with an adaptor PCB in combination with the MB-SMARC-1.

Figure 2: TQM Debug Card

3.6.3 Debug Module LED

The TQMxE39S includes a dual colour LED providing boot and BIOS information.
The following table shows some LED boot messages.

Table 8: LED Boot Messages

Red LED	Green LED	Remark
ON	OFF	Power supply error
ON	ON	S4/S5 state
BLINKING	BLINKING	S3 state
OFF	BLINKING	uEFI BIOS is booting
OFF	ON	uEFI BIOS boot is finished

3.7 SMARC Connector Pinout

This section describes the TQMxE39S SMARC connector pin assignment, which is compliant with the SMARC hardware specification Version 2.0.

3.7.1 Signal Assignment Abbreviations

Table 9 lists the abbreviations used in Table 10.

Table 9: Abbreviations used

Abbreviation	Description
GND	Ground
PWR	Power
I	Input
I PU	Input with pull-up resistor
I PD	Input with pull-down resistor
O	Output
OD	Open drain output
IO	Bi-directional

Note: Unused signals on the carrier board	
	If the input signals at the SMARC connector are not used, these signals can be left open on the carrier board, since these signals have a termination on the TQMxE39S.

3.7.2 SMARC Connector Pin Assignment

Table 10: SMARC Connector Pin Assignment

Pin	Signal	Description	Type	Level	Remark
P1	SMB_ALERT_1V8#	SM Bus Alert# (interrupt) signal	I PU	1.8 V	
P2	GND	Ground	GND		
P3	CSI1_CK+	CSI differential clock input	I	LVDS D-PHY	
P4	CSI1_CK–	CSI differential clock input	I	LVDS D-PHY	
P5	GBE1_SDP	IEEE 1588 Trigger Signal	IO	3.3 V	N/A
P6	GBE0_SDP	IEEE 1588 Trigger Signal	IO	3.3 V	
P7	CSI1_RX0+	CSI differential data input	I	LVDS D-PHY	
P8	CSI1_RX0–	CSI differential data input	I	LVDS D-PHY	
P9	GND	Ground	GND		
P10	CSI1_RX1+	CSI differential data input	I	LVDS D-PHY	
P11	CSI1_RX1–	CSI differential data input	I	LVDS D-PHY	
P12	GND	Ground	GND		
P13	CSI1_RX2+	CSI differential data input	I	LVDS D-PHY	
P14	CSI1_RX2–	CSI differential data input	I	LVDS D-PHY	
P15	GND	Ground	GND		
P16	CSI1_RX3+	CSI differential data input	I	LVDS D-PHY	
P17	CSI1_RX3–	CSI differential data input	I	LVDS D-PHY	
P18	GND	Ground	GND		
P19	GBE0_MDI3–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P20	GBE0_MDI3+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P21	GBE0_LINK100#	Link Speed Indication LED for 100 Mbps	OD	3.3 V tolerant	
P22	GBE0_LINK1000#	Link Speed Indication LED for 1000 Mbps	OD	3.3 V tolerant	
P23	GBE0_MDI2–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P24	GBE0_MDI2+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P25	GBE0_LINK_ACT#	Link / Activity Indication LED	OD	3.3 V tolerant	
P26	GBE0_MDI1–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P27	GBE0_MDI1+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P28	GBE0_CTREF	Center-Tap reference voltage for Carrier Ethernet magnetics	PWR		
P29	GBE0_MDI0–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P30	GBE0_MDI0+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	
P31	SPI0_CS1#	SPI0 Master Chip Select 1 output	O	1.8 V	
P32	GND	Ground	GND		
P33	SDIO_WP	SD Card: Write Protect	I	3.3 V	
P34	SDIO_CMD	SD Card: Command line	IO	3.3 V	
P35	SDIO_CD#	SD Card: Card Detect	I	3.3 V	
P36	SDIO_CK	SD Card: Clock	O	3.3 V	
P37	SDIO_PWR_EN	SD Card: Power enable	O (PU)	3.3 V	PU to 3.3 V
P38	GND	Ground	GND		
P39	SDIO_D0	SD Card: data path	IO	3.3 V	
P40	SDIO_D1	SD Card: data path	IO	3.3 V	
P41	SDIO_D2	SD Card: data path	IO	3.3 V	
P42	SDIO_D3	SD Card: data path	IO	3.3 V	
P43	SPI0_CS0#	SPI0 Master Chip Select 0 output	O	1.8 V	
P44	SPI0_CK	SPI0 Master Clock output	O	1.8 V	
P45	SPI0_DIN	SPI0 Master Data input (CPU input, SPI device output)	I	1.8 V	
P46	SPI0_DO	SPI0 Master Data output (CPU output, SPI device input)	O	1.8 V	
P47	GND	Ground	GND		
P48	SATA_TX+	Differential SATA transmit data Pair	O	SATA	
P49	SATA_TX–	Differential SATA transmit data Pair	O	SATA	
P50	GND	Ground	GND		
P51	SATA_RX+	Differential SATA receive data Pair	I	SATA	
P52	SATA_RX–	Differential SATA receive data Pair	I	SATA	

3.7.2 SMARC Connector Pin Assignment (continued)

Table 10: SMARC Connector Pin Assignment (continued)

Pin	Signal	Description	Type	Level	Remark
P53	GND	Ground	GND		
P54	ESPI_CS0#	LPSS SPI: Slave select	O	1.8 V	
P55	ESPI_CS1#	LPSS SPI: Slave select	O	1.8 V	
P56	ESPI_CK	LPSS SPI: Clock signal	O	1.8 V	
P57	ESPI_IO_1	LPSS SPI: RXD (MISO)	I or IO	1.8 V	
P58	ESPI_IO_0	LPSS SPI: TXD (MOSI)	O or IO	1.8 V	
P59	GND	Ground	GND		
P60	USB0+	USB differential pair	IO	USB	
P61	USB0–	USB differential pair	IO	USB	
P62	USB0_EN_OC#	USB over-current input / enable output (both OD)	IO PU	3.3 V	OD input only (2)
P63	USB0_VBUS_DET	Host power detection (when port is used as device)	I PD	5 V	N/A
P64	USB0_OTG_ID	USB OTG ID input, active high (high ⇨ device)	I PU	3.3 V	N/A
P65	USB1+	USB differential pair	IO	USB	
P66	USB1–	USB differential pair	IO	USB	
P67	USB1_EN_OC#	USB over-current input / enable output (both OD)	IO PU	3.3 V	OD input only (2)
P68	GND	Ground	GND		
P69	USB2+	USB differential pair	IO	USB	
P70	USB2–	USB differential pair	IO	USB	
P71	USB2_EN_OC#	USB over-current input / enable output (both OD)	IO PU	3.3 V	OD input only (2)
P72	RSVD	Reserved			
P73	RSVD	Reserved			
P74	USB3_EN_OC#	USB over-current input / enable output (both OD)	IO PU	3.3 V	OD input only (2)
P75	PCIE_A_RST#	PCIe Port reset output	O	3.3 V	(2)
P76	USB4_EN_OC#	USB over-current input / enable output (both OD)	IO PU	3.3 V	OD input only (2)
P77	RSVD	Reserved			
P78	RSVD	Reserved			
P79	GND	Ground	GND		
P80	PCIE_C_REFCK+	Differential PCIe Link reference clock output	O	PCIe	
P81	PCIE_C_REFCK–	Differential PCIe Link reference clock output	O	PCIe	
P82	GND	Ground	GND		
P83	PCIE_A_REFCK+	Differential PCIe Link reference clock output	O	PCIe	
P84	PCIE_A_REFCK–	Differential PCIe Link reference clock output	O	PCIe	
P85	GND	Ground	GND		
P86	PCIE_A_RX+	Differential PCIe Link receive data pair	I	PCIe	
P87	PCIE_A_RX–	Differential PCIe Link receive data pair	I	PCIe	
P88	GND	Ground	GND		
P89	PCIE_A_TX+	Differential PCIe Link transmit data pair	O	PCIe	
P90	PCIE_A_TX–	Differential PCIe Link transmit data pair	O	PCIe	
P91	GND	Ground	GND		
P92	HDMI_D2+ / DP1_LANE0+	TMDS / HDMI data differential pair / DP data pair	O	TDMS / DP	HDMI only
P93	HDMI_D2– / DP1_LANE0–	TMDS / HDMI data differential pair / DP data pair	O	TDMS / DP	HDMI only
P94	GND	Ground	GND		
P95	HDMI_D1+ / DP1_LANE1+	TMDS / HDMI data differential pair / DP data pair	O	TDMS / DP	HDMI only
P96	HDMI_D1– / DP1_LANE1–	TMDS / HDMI data differential pair / DP data pair	O	TDMS / DP	HDMI only
P97	GND	Ground	GND		
P98	HDMI_D0+ / DP1_LANE2+	TMDS / HDMI data differential pair / DP data pair	O	TDMS / DP	HDMI only
P99	HDMI_D0– / DP1_LANE2–	TMDS / HDMI data differential pair / DP data pair	O	TDMS / DP	HDMI only
P100	GND	Ground	GND		
P101	HDMI_CK+ / DP1_LANE3+	HDMI differential clock output pair / DP data pair	O	TDMS / DP	HDMI only
P102	HDMI_CK– / DP1_LANE3–	HDMI differential clock output pair / DP data pair	O	TDMS / DP	HDMI only
P103	GND	Ground	GND		
P104	HDMI_HPD / DP1_HPD	HDMI / DP Hot Plug Detect input	I PD	1.8 V	HDMI only PD

2: Configurable through TQ-flexiCFG.

3.7.2 SMARC Connector Pin Assignment (continued)

Table 10: SMARC Connector Pin Assignment (continued)

Pin	Signal	Description	Type	Level	Remark
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI I²C clock / DP AUX Channel	O / IO	1.8 V / DP	HDMI only; PU
P106	HDMI_CTRL_DAT / DP1_AUX–	HDMI I²C data / DP AUX Channel	IO	1.8 V / DP	HDMI only; PU
P107	DP1_AUX_SEL	DP AUX select (to select between DP and HDMI)	I	1.8 V	N/A
P108	GPIO0 / CAM0_PWR#	GPIO / Camera power enable (active low output)	IO PU/O	1.8 V	(3)
P109	GPIO1 / CAM1_PWR#	GPIO / Camera power enable (active low output)	IO PU/O	1.8 V	(3)
P110	GPIO2 / CAM0_RST#	GPIO / Camera reset (active low output)	IO PU/O	1.8 V	(3)
P111	GPIO3 / CAM1_RST#	GPIO / Camera reset (active low output)	IO PU/O	1.8 V	(3)
P112	GPIO4 / HDA_RST#	GPIO / HD audio reset (active low output)	IO PU/O	1.8 V	Preconfigured to HDA_RST# (3)
P113	GPIO5 / PWM_OUT	GPIO / PWM out for fan speed control	IO PU/O	1.8 V	Preconfigured to PWM_OUT (3)
P114	GPIO6 / TACHIN	GPIO / Tachometer input for fan speed measurement	IO PU/O	1.8 V	Preconfigured to TACHIN (3)
P115	GPIO7	GPIO	IO PU	1.8 V	(3)
P116	GPIO8	GPIO	IO PU	1.8 V	(3)
P117	GPIO9	GPIO	IO PU	1.8 V	(3)
P118	GPIO10	GPIO	IO PU	1.8 V	(3)
P119	GPIO11	GPIO	IO PU	1.8 V	(3)
P120	GND	Ground	GND		
P121	I2C_PM_CK	Power management I²C bus: SMBus	IO PU	1.8 V	
P122	I2C_PM_DAT	Power management I²C bus: SMBus	IO PU	1.8 V	
P123	BOOT_SEL0#	Boot source select	I	1.8 V	N/A
P124	BOOT_SEL1#	Boot source select	I	1.8 V	N/A
P125	BOOT_SEL2#	Boot source select (tie to GND to boot from carrier SPI)	I PU	1.8 V	(3)
P126	RESET_OUT#	General purpose reset output to carrier board	O	1.8 V	(3)
P127	RESET_IN#	Reset input from Carrier board	I PU	1.8 V	(3)
P128	POWER_BTN#	Power-button input from Carrier board	I PU	1.8 V	(3)
P129	SER0_TX	Serial port data out	O	1.8 V	(3)
P130	SER0_RX	Serial port data in	I	1.8 V	(3)
P131	SER0_RTS#	Serial port handshake: Request to Send	O	1.8 V	(3)
P132	SER0_CTS#	Serial port handshake: Clear to Send	I	1.8 V	(3)
P133	GND	Ground	GND		
P134	SER1_TX	Serial port data out	O	1.8 V	(3)
P135	SER1_RX	Serial port data in	I	1.8 V	(3)
P136	SER2_TX	Serial port data out	O	1.8 V	
P137	SER2_RX	Serial port data in	I	1.8 V	
P138	SER2_RTS#	Serial port handshake: Request to Send	O	1.8 V	
P139	SER2_CTS#	Serial port handshake: Clear to Send	I	1.8 V	
P140	SER3_TX	Serial port data out	O	1.8 V	
P141	SER3_RX	Serial port data in	I	1.8 V	
P142	GND	Ground	GND		
P143	CAN0_TX	CAN Transmit output	O	1.8 V	N/A
P144	CAN0_RX	CAN Receive input	I	1.8 V	N/A
P145	CAN1_TX	CAN Transmit output	O	1.8 V	N/A
P146	CAN1_RX	CAN Receive input	I	1.8 V	N/A
P147	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P148	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P149	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P150	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P151	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P152	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P153	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P154	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P155	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	
P156	VDD_IN	Module power input voltage	PWR	4.75 to 5.25 V	

3: Configurable through TQ-flexiCFG.

3.7.2 SMARC Connector Pin Assignment (continued)

Table 10: SMARC Connector Pin Assignment (continued)

Pin	Signal	Description	Type	Level	Remark
S1	CSI1_TX+ / I2C_CAM1_CK	Camera configurations differential data / Camera I²C	O/IO PU	TDMS / 1.8 V	I²C only
S2	CSI1_TX– / I2C_CAM1_DAT	Camera configurations differential data / Camera I²C	O/IO PU	TDMS / 1.8 V	I²C only
S3	GND	Ground	GND		
S4	RSVD	Reserved			(4)
S5	CSI0_TX+ / I2C_CAM0_CK	Camera configurations differential data / Camera I²C	O/IO PU	TDMS / 1.8 V	I²C only
S6	CAM_MCK	Master clock output for CSI camera support	O	1.8 V	
S7	CSI0_TX– / I2C_CAM0_DAT	Camera configurations differential data / Camera I²C	O/IO PU	TDMS / 1.8 V	I²C only
S8	CSI0_CK+	CSI differential clock input	I	LVDS D-PHY	
S9	CSI0_CK–	CSI differential clock input	I	LVDS D-PHY	
S10	GND	Ground	GND		
S11	CSI0_RX0+	CSI differential data input	I	LVDS D-PHY	
S12	CSI0_RX0–	CSI differential data input	I	LVDS D-PHY	
S13	GND	Ground	GND		
S14	CSI0_RX1+	CSI differential data input	I	LVDS D-PHY	
S15	CSI0_RX1–	CSI differential data input	I	LVDS D-PHY	
S16	GND	Ground	GND		
S17	GBE1_MDI0+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S18	GBE1_MDI0–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S19	GBE1_LINK100#	Link Speed Indication LED for 100 Mbps	OD	3.3 V tolerant	N/A
S20	GBE1_MDI1+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S21	GBE1_MDI1–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S22	GBE1_LINK1000#	Link Speed Indication LED for 1000 Mbps	OD	3.3 V tolerant	N/A
S23	GBE1_MDI2+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S24	GBE1_MDI2–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S25	GND	Ground	GND		
S26	GBE1_MDI3+	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S27	GBE1_MDI3–	Gigabit Ethernet Controller: Media Dependent Interface	IO	GBE MDI	N/A
S28	GBE1_CTREF	Center-Tap reference voltage for Carrier Ethernet magnetics	PWR		N/A
S29	PCIE_D_TX+	Differential PCIe Link transmit data pair	O	PCIe	
S30	PCIE_D_TX–	Differential PCIe Link transmit data pair	O	PCIe	
S31	GBE1_LINK_ACT#	Link / Activity Indication LED	OD	3.3 V tolerant	N/A
S32	PCIE_D_RX+	Differential PCIe Link receive data pair	I	PCIe	
S33	PCIE_D_RX–	Differential PCIe Link receive data pair	I	PCIe	
S34	GND	Ground	GND		
S35	USB4+	USB differential pair	IO	USB	
S36	USB4–	USB differential pair	IO	USB	
S37	USB3_VBUS_DET	Host power detection (when port is used as device)	I PD	5 V	
S38	AUDIO_MCK	I²S: Master clock output to Audio codecs	O	1.8 V	
S39	I2S0_LRCK	I²S: Left& Right audio synchronization clock	IO	1.8 V	
S40	I2S0_SDOUT	I²S: Digital audio Output	O	1.8 V	
S41	I2S0_SDIN	I²S: Digital audio Input	I	1.8 V	
S42	I2S0_CK	I²S: Digital audio clock	IO	1.8 V	
S43	ESPI_ALERT0#	Input from eSPI slave to request service from master	I	1.8 V	N/A
S44	ESPI_ALERT1#	Input from eSPI slave to request service from master	I	1.8 V	N/A
S45	RSVD	Reserved			(4)
S46	RSVD	Reserved			
S47	GND	Ground	GND		
S48	I2C_GP_CK	General Purpose I²C bus	IO PU	1.8 V	
S49	I2C_GP_DAT	General Purpose I²C bus	IO PU	1.8 V	
S50	HDA_SYNC / I2S2_LRCK	HDA: sync / I²S: Left& Right audio synchronization clock	IO	1.8 V	
S51	HDA_SDO / I2S2_SDOUT	HDA: data out / / I²S: Digital audio Output	O	1.8 V	
S52	HDA_SDI / I2S2_SDIN	HDA: data in / I²S: Digital audio Input	I	1.8 V	

4: Configurable through TQ-flexiCFG.

3.7.2 SMARC Connector Pin Assignment (continued)

Table 10: SMARC Connector Pin Assignment (continued)

Pin	Signal	Description	Type	Level	Remark
S53	HDA_CK / I2S2_CK	HDA: clock / I²S: Digital audio clock	IO	1.8 V	
S54	SATA_ACT#	Active low SATA activity indicator (16 mA max)	OD	3.3 V	(5)
S55	USB5_EN_OC#	USB over-current input / enable output (both OD)	IO PU	3.3 V	OD input only (5)
S56	ESPI_IO_2	ESPI Master Data Input / Outputs	IO	1.8 V	N/A
S57	ESPI_IO_3	ESPI Master Data Input / Outputs	IO	1.8 V	N/A
S58	ESPI_RESET#	ESPI Reset	O	1.8 V	
S59	USB5+	USB differential pair	IO	USB	
S60	USB5–	USB differential pair	IO	USB	
S61	GND	Ground	GND		
S62	USB3_SSTX+	Differential USB SuperSpeed transmit data pair	O	USB SS	
S63	USB3_SSTX–	Differential USB SuperSpeed transmit data pair	O	USB SS	
S64	GND	Ground	GND		
S65	USB3_SSRX+	Differential USB SuperSpeed receive data pair	I	USB SS	
S66	USB3_SSRX–	Differential USB SuperSpeed receive data pair	I	USB SS	
S67	GND	Ground	GND		
S68	USB3+	USB differential pair	IO	USB	
S69	USB3–	USB differential pair	IO	USB	
S70	GND	Ground	GND		
S71	USB2_SSTX+	Differential USB SuperSpeed transmit data pair	O	USB SS	
S72	USB2_SSTX–	Differential USB SuperSpeed transmit data pair	O	USB SS	
S73	GND	Ground	GND		
S74	USB2_SSRX+	Differential USB SuperSpeed receive data pair	I	USB SS	
S75	USB2_SSRX–	Differential USB SuperSpeed receive data pair	I	USB SS	
S76	PCIE_B_RST#	PCIe Port reset output	O	3.3 V	
S77	PCIE_C_RST#	PCIe Port reset output	O	3.3 V	
S78	PCIE_C_RX+	Differential PCIe Link receive data pair	I	PCIe	
S79	PCIE_C_RX–	Differential PCIe Link receive data pair	I	PCIe	
S80	GND	Ground	GND		
S81	PCIE_C_TX+	Differential PCIe Link transmit data pair	O	PCIe	
S82	PCIE_C_TX–	Differential PCIe Link transmit data pair	O	PCIe	
S83	GND	Ground	GND		
S84	PCIE_B_REFCK+	Differential PCIe Link reference clock output	O	PCIe	
S85	PCIE_B_REFCK–	Differential PCIe Link reference clock output	O	PCIe	
S86	GND	Ground	GND		
S87	PCIE_B_RX+	Differential PCIe Link receive data pair	I	PCIe	
S88	PCIE_B_RX–	Differential PCIe Link receive data pair	I	PCIe	
S89	GND	Ground	GND		
S90	PCIE_B_TX+	Differential PCIe Link transmit data pair	O	PCIe	
S91	PCIE_B_TX–	Differential PCIe Link transmit data pair	O	PCIe	
S92	GND	Ground	GND		
S93	DP0_LANE0+	DP++ data differential pair	O	DP++	
S94	DP0_LANE0–	DP++ data differential pair	O	DP++	
S95	DP0_AUX_SEL	DP AUX select (to select between DP and HDMI)	I PD	1.8 V	PD
S96	DP0_LANE1+	DP++ data differential pair	O	DP++	
S97	DP0_LANE1–	DP++ data differential pair	O	DP++	
S98	DP0_HPD	DP++ Hot Plug Detect input	I PD	1.8 V	PD
S99	DP0_LANE2+	DP++ data differential pair	O	DP++	
S100	DP0_LANE2–	DP++ data differential pair	O	DP++	
S101	GND	Ground	GND		
S102	DP0_LANE3+	DP++ data differential pair	O	DP++	
S103	DP0_LANE3–	DP++ data differential pair	O	DP++	
S104	USB3_OTG_ID	USB OTG ID input, active high (high ⇨ device)	I PU	3.3 V	

5: Configurable through TQ-flexiCFG.

3.7.2 SMARC Connector Pin Assignment (continued)

Table 10: SMARC Connector Pin Assignment (continued)

Pin	Signal	Description	Type	Level	Remark
S105	DP0_AUX+	DP++ AUX Channel (could also be used as 3.3 V I²C for HDMI)	IO	DP++ /3.3 V	PU at high AUX_SEL
S106	DP0_AUX–	DP++ AUX Channel (could also be used as 3.3 V I²C for HDMI)	IO	DP++ /3.3 V	PU at high AUX_SEL
S107	LCD1_BKLT_EN	LCD Backlight enable: high enables panel backlight	O	1.8 V	N/A
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS LCD differential clock pair / eDP AUX Channel	O/IO	LVDS/DP	LVDS only
S109	LVDS1_CK– / eDP1_AUX– / DSI1_CLK–	LVDS LCD differential clock pair / eDP AUX Channel	O/IO	LVDS/DP	LVDS only
S110	GND	Ground	GND		
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S112	LVDS1_0– / eDP1_TX0– / DSI1_D0–	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S113	eDP1_HPD	eDP Hot Plug Detect	I PD	1.8 V	N/A
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S115	LVDS1_1– / eDP1_TX1– / DSI1_D1–	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S116	LCD1_VDD_EN	Enable signal for panel power	O	1.8 V	N/A
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S118	LVDS1_2– / eDP1_TX2– / DSI1_D2–	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S119	GND	Ground	GND		
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S121	LVDS1_3– / eDP1_TX3– / DSI1_D3–	LVDS / eDP data differential pair /	O	LVDS/DP	LVDS only
S122	LCD1_BKLT_PWM	Display Backlight brightness control output (PWM)	O	1.8 V	N/A
S123	RSVD	Reserved			
S124	GND	Ground	GND		
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS / eDP data differential pair /	O	LVDS/DP	
S126	LVDS0_0– / eDP0_TX0– / DSI0_D0–	LVDS / eDP data differential pair /	O	LVDS/DP	
S127	LCD0_BKLT_EN	LCD Backlight enable: high enables panel backlight	O	1.8 V	
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS / eDP data differential pair /	O	LVDS/DP	
S129	LVDS0_1– / eDP0_TX1– / DSI0_D1–	LVDS / eDP data differential pair /	O	LVDS/DP	
S130	GND	Ground	GND		
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS / eDP data differential pair /	O	LVDS/DP	
S132	LVDS0_2– / eDP0_TX2– / DSI0_D2–	LVDS / eDP data differential pair /	O	LVDS/DP	
S133	LCD0_VDD_EN	Enable signal for panel power	O	1.8 V	
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS LCD differential clock pair / eDP AUX Channel	O/IO	LVDS/DP	
S135	LVDS0_CK– / eDP0_AUX– / DSI0_CLK–	LVDS LCD differential clock pair / eDP AUX Channel	O/IO	LVDS/DP	
S136	GND	Ground	GND		
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS / eDP data differential pair /	O	LVDS/DP	
S138	LVDS0_3– / eDP0_TX3– / DSI0_D3–	LVDS / eDP data differential pair /	O	LVDS/DP	
S139	I2C_LCD_CK	I²C bus to read display EDID EEPROMs (for LVDS displays)	IO PU	1.8 V	
S140	I2C_LCD_DAT	I²C bus to read display EDID EEPROMs (for LVDS displays)	IO PU	1.8 V	
S141	LCD0_BKLT_PWM	Display Backlight brightness control output (PWM)	O	1.8 V	
S142	RSVD	Reserved			
S143	GND	Ground	GND		
S144	eDP0_HPD	eDP Hot Plug Detect	I PD	1.8 V	
S145	WDT_TIME_OUT#	Watch-Dog-Timer Output	O	1.8 V	(6)
S146	PCIE_WAKE#	PCIe wake up interrupt to host	I PU	3.3 V	(6)
S147	VDD_RTC	Real-time clock circuit-power input	PWR	2 V to 3.3 V	
S148	LID#	Lid open/close indication to module (low indicates closed lid)	I PU	1.8 V	(6)
S149	SLEEP#	Sleep indicator from carrier board	I PU	1.8 V	(6)
S150	VIN_PWR_BAD#	Power bad indication from Carrier board	I PU	VDD_IN	
S151	CHARGING#	Held low by carrier during battery charging	I PU	1.8 V	(6)
S152	CHARGER_PRSNT#	Held low by carrier if DC input for battery charger is present	I PU	1.8 V	(6)
S153	CARRIER_STBY#	Driven low by module during standby power state. (SUS_S3#)	O	1.8 V	(6)
S154	CARRIER_PWR_ON	Signal to carrier to turn on determined power supplies (SUS_S5#)	O	1.8 V	(6)
S155	FORCE_RECOV#	Force recovery input: pull low to load BIOS defaults	I PU	1.8 V	(6)
S156	BATLOW#	Battery low indication to module	I PU	1.8 V	
S157	TEST#	Reserved for module-specific test functions	I	1.8 V	DNC
S158	GND	Ground	GND		

6: Configurable through TQ-flexiCFG.

4. MECHANICS

4.1 TQMxE39S Dimensions

The dimensions of the TQMxE39S are 82 mm × 50 mm.
The following illustration shows the Three View Drawing of the TQMxE39S.

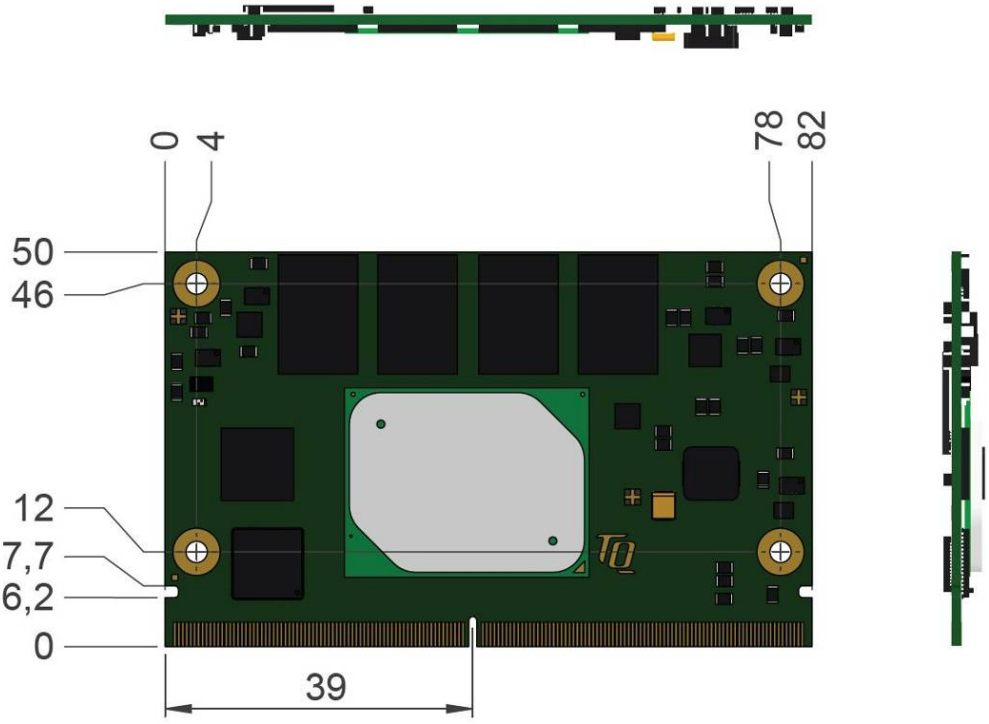

Figure 3: Three View Drawing TQMxE39S

The following illustration shows the bottom view of the TQMxE39S.

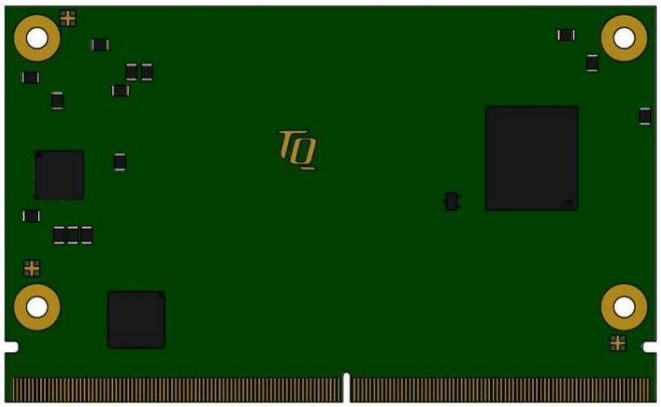

Figure 4: Bottom View Drawing TQMxE39S

4.2 Heat Spreader Dimensions

The TQMxE39S supports two different heat spreader versions.
Both versions are compliant to the SMARC specification with 6 mm height.

Heat spreader for the Intel® Pentium® N4200, and Intel® Celeron® N3350 CPU

- **TQMxE39S-HSP-N**

Heat spreader for the Intel® Atom™ E3900 CPU

- **TQMxE39S-HSP-E**

The following illustration shows the standard heat spreader (TQMxE39S-HSP) for the TQMxE39S.

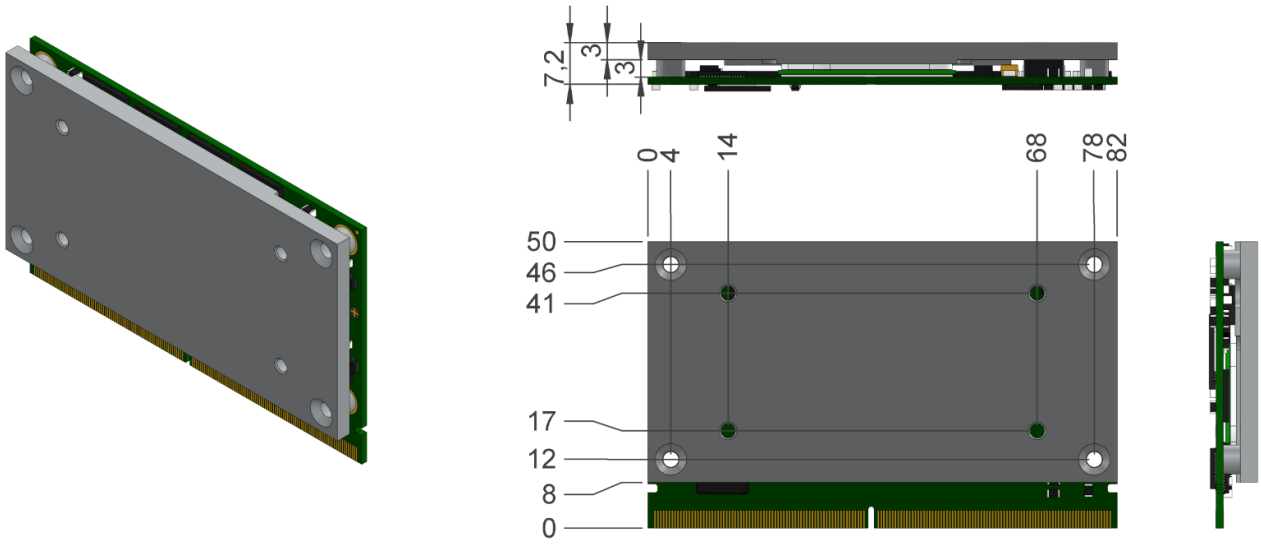

Figure 5: Standard Heat Spreader TQMxE39S-HSP

Attention: Heat Spreader	
	The packages of the Intel® Pentium® N4200 and the Intel® Celeron® N3350 CPU have a different height than the package of the Intel® Atom™ E3900 CPU! The Intel® Atom™ E3900 CPU family includes an integrated heat spreader, the Intel® Pentium® N4200 and the Intel® Celeron® N3350 CPUs have no integrated heat spreaders. Both CPU packages require different heat spreader versions. It is not permitted to use the TQMxE39S-HSP-**E** heat spreader on the Intel® Pentium® **N**4200 or the Intel® Celeron® **N**3350 CPU. It is also not permitted to use the TQMxE39S-HSP-**N** heat spreader on the Intel® Atom™ **E**3900 CPU. To mount the wrong heat spreader will damage the TQMxE39S.

If a special cooling solution has to be implemented an extensive thermal design analysis and verification has to be performed. TQ-Systems GmbH offers thermal analysis and simulation as a service.

Please contact support@tq-group.com for more details about 2D/3D Step models.

4.3 Mechanical and Thermal Considerations

The TQMxE39S is designed to operate in a wide range of thermal environments.

An important factor for each system integration is the thermal design. The heat spreader acts as a thermal coupling device to the TQMxE39S. The heat spreader is thermally coupled to the CPU: It provides optimal heat transfer from the TQMxE39S to the heat spreader. The heat spreader itself is not an appropriate heat sink.

System designers can implement different passive and active cooling versions through the thermal connection to the heat spreader.

Attention: Thermal Considerations	
	Do not operate the TQMxE39S without heat spreader or without heat sink! The heat spreader is not a sufficient heat sink!

If a special cooling solution has to be implemented, an extensive thermal design analysis and verification has to be performed.

TQ-Systems GmbH offers thermal analysis and simulation as a service.

Please contact support@tq-group.com for more information about the thermal configuration.

4.4 Protection Against External Effects

The TQMxE39S itself is not protected against dust, external impact and contact (IP00).

Adequate protection has to be guaranteed by the surrounding system and carrier board.

To support applications in harsh environment, conformal coating can be offered as custom specific add-on.

Please contact support@tq-group.com for further details.

5. SOFTWARE

5.1 System Resources

5.1.1 I²C Bus

The TQMxE39S provides a general purpose I²C port via a dedicated LPC to I²C controller in the TQ-flexiCFG block.
The following table shows the I²C address mapping for the SMARC I²C port.

Table 11: I²C Address Mapping on GP I²C Port

8-bit Address	Function	Remark
0xA0	TQMxE39S EEPROM	–
0xAE	Carrier Board EEPROM	Embedded EEPROM configuration not supported

5.1.2 SMBus

The TQMxE39S provides a System Management Bus (SMBus).
The following table shows the I²C address mapping for the SMARC SMBus port.

Table 12: I²C Address Mapping on SMBus Port

8-bit Address	Function	Remark
0x58	Hardware Monitor	–

5.1.3 Memory Map

The TQMxE39S supports the standard PC system memory and I/O memory map.
Please contact support@tq-group.com for further information about the memory map.

5.1.4 IRQ Map

The TQMxE39S supports the standard PC Interrupt routing.
The integrated legacy devices (COM1, COM2) can be configured via the BIOS to IRQ3 and IRQ4.
Please contact support@tq-group.com for further information about the Interrupt configuration.

5.2 Operating Systems

5.2.1 Supported Operating Systems

The TQMxE39S supports various Operating Systems:

- Microsoft® Windows® 10
- Linux (i.e. Ubuntu 16.10 or later)

Other Operating Systems are supported on request.

Please contact support@tq-group.com for further information about supported Operating Systems.

5.2.2 Driver Download

The TQMxE39S is well supported by the Standard Operating Systems, which already include most of the required drivers. The use of the latest Intel® drivers to optimize performance and the full feature set of the TQMxE39S is recommended.

Drivers for Graphics can be downloaded at this Intel® page:
https://downloadcenter.Intel.com/download/26228/Intel-Graphics-Driver-for-Windows-10-and-Windows-7-8-1-15-40-?v=t

Drivers for Chipset Components in the Device Manager can be downloaded at this Intel® page:
https://downloadcenter.Intel.com/download/20775/Intel-Chipset-Device-Software-INF-Update-Utility

The Intel® Driver Update Utility is a tool that analyses the system drivers on your computer. The utility reports if any new drivers are available, and provides the download files for the driver updates so you can install them quickly and easily.
https://downloadcenter.Intel.com/download/24345/Intel-Driver-Update-Utility

Drivers for the Intel® Gigabit Ethernet controller can be downloaded at this Intel® page:
https://downloadcenter.intel.com/download/18713/Intel-Network-Adapter-Driver-for-Windows-7-?v=t

The White Paper “Windows Driver Installation Instructions“ provides information how to install the Windows driver.

Please contact support@tq-group.com for further driver download assistance.

5.3 TQ-Systems Embedded Application Programming Interface (EAPI)

The TQ-Systems Embedded Application Programming Interface (EAPI) is a driver package to access and control hardware resources on all TQ-Systems COM Express™ modules.
The TQ-Systems EAPI is compatible with the PICMG® specification.

5.4 Software Tools

Please contact support@tq-group.com for further information about available software tools.

6. BIOS

The TQMxE39S uses a 64 bit uEFI BIOS with a legacy Compatibility Support Module (CSM).
This additional functionality permits to load a traditional OS or a traditional OpROM.
To access the InsydeH2O BIOS Front Page, the button <ESC> has to be pressed after System Power-Up during POST phase.
If the button is successfully pressed, you will get to the BIOS front page, which shows the main menu items.
For Help Dialog please press <F1>.

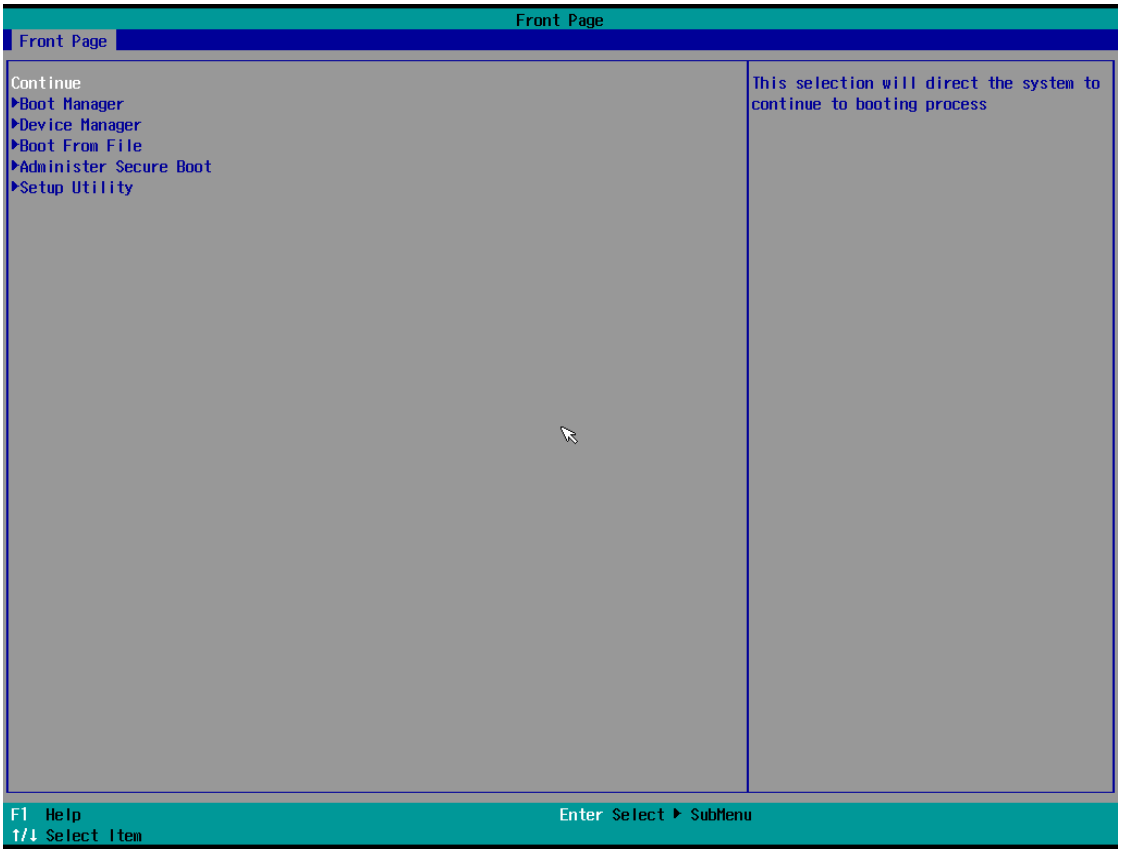

Figure 6: InsydeH2O BIOS Front Page

6.1 Continue Boot Process

Continue boot process the same way if <ESC> was not be pressed.

6.2 Boot Manager

Choose between possible Boot Options. If system is in UEFI Boot Mode one Boot Option will be “Internal EFI Shell“.
You can go back to “Boot Manager“ by entering command “exit“ and press <ENTER>.

6.3 Device Manager

6.3.1 SioTqmx86

Menu Item	Option	Description
Power State S5	Normal / Low Power	Configure Power State S5. Normal: Wakeup over LAN (WOL), timer, external Wake and Power Button possible.
Serial Port X	Enabled / Disabled / Auto	Disabled: No configuration Enabled: User Configuration Auto: EFI/OS chooses configuration
Base I/O Address	2E8 / 2F8 / 3E8 / 3F8	Configure Base I/O Address of corresponding Serial Port X.
Interrupt	IRQ3 / IRQ4 / IRQ5 / IRQ6 / IRQ7	Configure Interrupt of corresponding Serial Port X.
LVDS Configuration	Enabled / Disabled	Enable or Disable the configuration of eDP-to-LVDS bridge.
LVDS Colour depth and data packing format	VESA 24 bpp / JEIDA 24 bpp / VESA and JEIDA 18 bpp	Configure the LVDS Colour depth in eDP-to-LVDS bridge.
LVDS dual/single mode	Single LVDS bus mode / Dual LVDS bus mode	Configure LVDS Single/dual bus mode.
LVDS EDID information	EDID Emulation off – read from DDC EDID Emulation on – read from internal Flash	Configure if the EDID information should be read from DDC or internal flash of eDP-to-LVDS bridge.
LVDS Resolution	1024 × 768 @ 60 Hz NXP Generic / 800 × 480 @ 60 Hz NXP Generic / 480 × 272 @ 60 Hz NXP Generic / 1600 × 900 @ 60 Hz Samsung LTM200 KT / 1920 × 1080 @ 60 Hz Samsung LTM230 HT / 1366 × 768 @ 60 Hz NXP Generic / 320 × 240 @ 60 Hz NXP Generic	Configure the Resolution of eDP-to-LVDS bridge. Note: This option is only visible if 'LVDS EDID information' is set on 'EDID Emulation on – read from internal Flash.

6.4 Boot From File

Boot from a specific mass storage device where a boot file is stored.

6.5 Administer Secure Boot

Enable and configure Secure Boot mode. This option can be also used to integrate PK, KEK, DB and DBx.

Note: Secure Boot	
	This option should only be used by advanced users.

6.6 Setup Utility

A basic setup of the board can be done by Insyde Software Corp. "Insyde Setup Utility" stored inside an on-board SPI flash.
To get access to InsydeH2O Setup Utility the button <ESC> has to be pressed after System Power Up during POST phase.
If the button successfully pressed can be seen by sentence "ESC is pressed. Go to boot options" shown below the boot logo.
On the splash screen that will appear, select "Setup Utility". The left frame of each menu page show the option, which can be configured whereas the right frame shows the corresponding help.

Key:

↑ / ↓	Navigate between setup items.
← / →	Navigate between setup screens (Main, Advanced, Security, Power, Boot and Exit).
<F1>	Show general help screen (Key Legend).
<F5> / <F6>	In the Main screens this buttons allow to change between different languages. Otherwise it allows to change the value of highlighted menu item.
<ENTER>	Press to display or change setup option listed for a certain menu or to display setup sub-screens.
<F9>	Press to load the setup default configuration of the board which cannot be changed by the user. This option has to be confirmed and saved by <F10> afterwards. Leaving the InsydeH2O Setup Utility will discard the changes.
<F10>	Press to save any changes made and exit setup utility by executing a restart.
<ESC>	Press to leave the current screen or sub-screen and discard all changes.

6.6.1 Main

The Main screen shows details regarding the BIOS version, processor type, bus speed, memory configuration and further information. There are three options which can be configured.

Menu Item	Option	Description
Language	English / Francis / Korean / Chinese	Configures the language of the InsydeH2O Setup Utility
System Time	HH:MM:SS	Use to change the system time to the 24-hour format
System Date	MM:DD:YYYY	Use to change the system date

6.6.2 Advanced

Use the right cursor to get from the main menu item to the advanced menu item.

Menu Item	Option	Description
Boot Configuration	See submenu	Configures settings for Boot Phase
Uncore Configuration	See submenu	Configure Graphical settings
South Cluster Configuration	See submenu	Configure parameter for Audio, PCI Express, SATA, SCC, USB and others
Security Configuration	See submenu	Configure TPM parameters
System Component	See submenu	Configure System Components parameters
Debug Configuration	See submenu	Configure Debug parameters
RTD3 settings	See submenu	Configure RTD3 parameters
ACPI Table/Features Control	See submenu	Configure ACPI parameters
SIO Hardware Monitor Nuvoton NCT7802Y	See submenu	Configure parameters of Super-IO chip NCT7802y
Console Redirection	See submenu	Configure parameters of Console Redirection
H2OUve Configuration	See submenu	Configure parameters of Insyde Tool H2OUve

6.6.2.1 Boot Configuration

Setup Utility ⇨ Advanced ⇨ Boot Configuration

Menu Item	Option	Description
OS Selection	Windows / Android / Linux	Choose the preferred Operating System
Numlock	On / Off	Allows to choose whether NumLock Key at system boot must be turned On or Off
Real Time Option	RT Disabled / RT Enabled. Agent IDI1 / RT Enabled. Agent Disabled	Select Real-Time Enable and IDI Agent Real-Time Traffic Mask Bits.

6.6.2.2 Uncore Configuration

Setup Utility ⇨ Advanced ⇨ Uncore Configuration

Menu Item	Option	Description
Logo & SCU Resolution	Auto / 640 x 480 / 800 x 600 / 1024 x 768	Select which solution should be used for Boot Logo and Setup Utility screen.
Rotate Screen	Disabled / 90 degrees clockwise / 270 degrees clockwise	Allows to rotate screen with 90 or 270 degrees clockwise.
VBT Hook Configuration	See submenu	Set VBT Hook Configuration parameters.
GOP Driver	Enabled / Disabled	Allows to disable or enable the driver for Graphical Output Protocol (GOP).
GOP Brightness Level	20 / 40 / 60 / 80 / 100 / 120 / 140 / 160 / 180 / 200 / 220 / 240 / 255	Select which GOP (Graphical Output Protocol) brightness level.
Integrated Graphics Device	Enabled / Disabled	Allows to enable or disable Integrated Graphics Device (IGD). If Primary Display is set on IGD enable this option.
Primary Display	Auto / IGD / PCIe	Select which of IGD or PCI Graphics device should be Primary Display.
RC6(Render Standby)	Enabled / Disabled	Allows to enable or disable Intel's Render Standby technology where the standby voltage is adjusted very low. RC6 should be enabled when Max Package C-State is set on S0ix.
GTT Size	2 MB / 4 MB / 8 MB	Select the Size of the Graphical Translation Table (GTT).
Aperture Size	256 MB	Just 256MB is adjustable because of an Intel Graphics driver issue (IPS case #00215535).
DVMT Pre-Allocated	64M / 96M / 128M / 160M / 192M / 224M / 256M / 288M / 320M / 352M / 384M / 416M / 448M / 480M / 512M	Select DVMT5.0 (Dynamic Video Memory Technology) Pre-Allocated (fixed) Graphics Memory size used by the Internal Graphic Device.
DVMT Total Gfx Mem	128M / 256M / MAX	Select the DVMT5.0 (Dynamic Video Memory Technology) Total Graphics Memory size used by the Internal Graphics Device.
Cd Clock Frequency	144 MHz / 288 MHz / 384 MHz / 576 MHz / 624 MHz	Select the highest Cd Clock frequency supported by the platform.
GT PM Support	Enabled / Disabled	Enable/Disable GT PM Support.
PAVP Enable	Enabled / Disabled	Enable/Disable PAVP.

6.6.2.2 Uncore Configuration (continued)

Setup Utility ⇨ Advanced ⇨ Uncore Configuration ⇨ VBT Hook Configuration

Menu Item	Option	Description
LFP 1 Configuration	eDP / No Device	Allows to enable the Local Flat Panel (LFP) as embedded Display Port (eDP)
EFP 1 Configuration	HDMI/DVI / DisplayPort with HDMI/DVI Compatible / No Device	Configure or disable the External Flat Panel 1 (EFP1).
EFP 2 Configuration	HDMI/DVI / DisplayPort with HDMI/DVI Compatible / No Device	Configure or disable the External Flat Panel 2 (EFP2).

6.6.2.3 South Cluster Configuration

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration

Menu Item	Option	Description
HD-Audio Configuration	See submenu	Set HD-Audio Configuration parameters
LPSS Configuration	See submenu	Set LPSS Configuration
PCI Express Configuration	See submenu	Set PCI Express Configuration parameters
SATA Drives	See submenu	Set SATA Drives parameters
SCC Configuration	See submenu	Set SCC (South Cluster Configuration) Configuration parameters
USB Configuration	See submenu	Set USB Configuration parameters
Miscellaneous Configuration	See submenu	Set Miscellaneous Configuration parameters

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ HD-Audio Configuration

Menu Item	Option	Description
HD-Audio Support	Enabled / Disabled	Allows to enable or disable HD-Audio Support
HD-Audio DSP	Enabled / Disabled	Allows to enable or disable HD-Audio DSP

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ LPSS Configuration

Menu Item	Option	Description
LPSS HSUART #1 Support (D24:F0, Ser2)	Disabled / PCI Mode	Enable/Disable LPSS HSUART #1 Support.
LPSS HSUART #3 Support (D24:F2, Ser3)	Disabled / PCI Mode	Enable/Disable LPSS HSUART #2 Support.

6.6.2.3 South Cluster Configuration (continued)

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ PCI Express Configuration

Menu Item	Option	Description
PCI Express Root Port 1 (Local i210 Controller)	See submenu	Configure PCI Express Root Port parameters respectively.
PCI Express Root Port 3 (COME Port 0)	See submenu	
PCI Express Root Port 4 (COME Port 1)	See submenu	
PCI Express Root Port 5 (COME Port 2)	See submenu	
PCI Express Root Port 6 (COME Port 3)	See submenu	

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ PCI Express Configuration ⇨ PCI Express Root Port X

Note: All PCI Express Root Port Configuration submenus are identical. Thus, they just will be listed once

Menu Item	Option	Description
PCI Express Root Port X	Enabled / Disabled / Auto	Enable or disable single PCI Express Root Port X. Set them to Auto means to disable unused root port automatically for the most optimum power savings. PCI Express Root Port 1 is internally connected to Intel® Gigabit Ethernet Controller I210. Disabling this port will result in disabling Ethernet interface.
ASPM	Disabled / Los / L1 / LOsL1 / Auto	This manages PCI Express LOs power states, for Operating Systems able to handle Active State Power Management (ASPM).
PCIe Speed	Auto / Gen1 / Gen2	Select the PCIe Speed.
Extra Bus Reserved	0-7	Configure Extra Bus Reserved for bridges behind this Root Bridge. Numbers from 0 to 7 are configurable.
Reserved Memory	1-20 MB	Configure Reserved Memory and Prefetchable Memory Range for this Root Bridge. Range from 1 to 20MB are configurable.
Reserved I/O	4-20K	Configure Reserved I/O Range for this Root Bridge. Range from 4 to 20 are configurable.
PCIe Selectable De-emphasis	Enabled / Disabled	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b = -3.5dB 0b = -6 dB

6.6.2.3 South Cluster Configuration (continued)

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ SATA Drives

Menu Item	Option	Description
SATA Mode Selection	AHCI	Determines how SATA controller operates. Just AHCI for standard SATA functionalities are selectable.
SATA Interface Speed	Gen1 / Gen2 / Gen3	Select SATA Interface Speed.
Aggressive LPM Support	Enabled / Disabled	Enable or disable PCH to aggressively enter Link power state.

Note: All SATA Port Configurations are identical and, thus, they just will be listed once.

Menu Item	Option	Description
SATA Port X	Enabled / Disabled	Enable or disable respective SATA Port X.
SATA Port X Hot Plug Capability	Enabled / Disabled	Enable or disable respective SATA Port X Hot Plug Capability.
Spin Up Device	Enabled / Disabled	Enable or disable SATA device as Spin Up Device. If enabled for any of ports Staggered Spin Up sill be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA Device Type	Hard Disk Drive / Solid State Drive	Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.
DITO Configuration	Enabled / Disabled	Enable or disable the possibility to configure DITO Value or DM Value.
DITO Value	0 - 1023	Set the Device Sleep Idle Timeout (DITO). This specifies the amount of the time (with approximately 1ms granularity) that the HBA shall wait before driving the Device Sleep (DEVSLP) signal. Only configurable if DITO configuration is enabled.
DM Value	0 - 15	0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1ms to 16368ms. (DITO_actual = DITO*(DM+1)). Only configurable if DITO configuration is enabled.

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ SCC Configuration

Menu Item	Option	Description
SCC SD Card Support (D27:F0)	Enabled / Disabled	Enable or disable the SCC SD Card Support.
SCC eMMC Support (D28:F0)	Enabled / Disabled	Enable or disable the SCC eMMC Support.
eMMC Max Speed	HS400 / HS200 / DDR50	Select the maximum Speed allowed of the eMMC.

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ USB Configuration

Menu Item	Option	Description
USB BIOS Support	Enabled / Disabled	Enable or disable the support of USB Keyboard / mouse / storage under UEFI and Legacy environment.
USB Per-Port Control	Enabled / Disabled	Allows to Enable or disable every single USB Port.
USB Port #X	Enabled / Disabled	Enable or disable USB Port #X. Only visible if USB Per-Port Control is enabled.
USB Host/Client Configuration	Host / Client	Configure logical USB Port 0 to Host or Client. Note: This is a static configuration and there is no automatic change between host and client.

6.6.2.3 South Cluster Configuration (continued)

Setup Utility ⇨ Advanced ⇨ South Cluster Configuration ⇨ Miscellaneous Configuration

Menu Item	Option	Description
High Precision Timer	Enabled / Disabled	Enable or disable the High Precision Event Timer.
State After G3	S0 State / S5 State / Last State	Specify which state to go to when power is reapplied after a power failure (G3 state). S0 State: System will boot directly as soon as power applied. S5 State: System keeps in power-off state until power button is pressed.
DCI enable (HDCIEN)	Enabled / Disabled	When DCI is Enabled, it is taken ass user consent to enable the DCI which allows debug over the USB3 interface. When Disabled, the host control is not enabling DCI feature.
Hide Unused LPSS devices	Enabled / Disabled	Enable/Disable hide Unused LPSS ACPI devices.

6.6.2.4 Security Configuration

Setup Utility ⇨ Advanced ⇨ Security Configuration

Menu Item	Option	Description
Target TPM device	dTPM / fTPM	Select the TPM device as a discrete TPM (dTPM) or firmware TPM (fTPM).

6.6.2.5 System Component

Setup Utility ⇨ Advanced ⇨ System Component

Menu Item	Option	Description
OS Reset Select	Warm Reset / Cold Reset	Select the reset type In FACP table.

6.6.2.6 Debug Configuration

Setup Utility ⇨ Advanced ⇨ Debug Configuration

Menu Item	Option	Description
TXE Prepare For Update	Enabled / Disabled	Send Prepare For Update Command in next boot, please send this command before update IAFW BIOS or TXE data region: Note: NVMs data is unavailable in next boot.

6.6.2.7 RTD3 Settings

Setup Utility ⇨ Advanced ⇨ RTD3 settings

Menu Item	Option	Description
RTD3 Support	Enabled / Disabled	Enable or disable Runtime Device Power State D3 (RTD3) support.

6.6.2.8 ACPI Table / Features Control

Setup Utility ⇨ Advanced ⇨ ACPI Table / Features Control

Menu Item	Option	Description
FACP – RTC S4 Wakeup	Enabled / Disabled	Enable or disable S4 Wakeup from RTC. Value only for ACPI.
APIC – IO APIC Mode	Enabled / Disabled	This item is valid only for Win2k and WinXP. Also, a fresh install of the OS must occur when APIC Mode is desired. Test the IO ACPI by setting item to Enable. The APIC Table will then be pointed to by the RSDT, the Local APIC will be initialized, and the proper enable bits will be set in ICH4M.
Smart Battery Support	Enabled / Disabled	Enable or disable Smart Battery Support. Note: Due to the SMBus driver i2c_i801 the SMBus is not working under Linux if Smart Battery is enabled. To get Smart Battery and the SMBus work simultaneously under Linux the i2c_i801 driver has to be adapted. Windows is not affected of this issue.

6.6.2.9 SIO Hardware Monitor Nuvoton NCT7802Y

Setup Utility ⇨ Advanced ⇨ SIO Hardware Monitor Nuvoton NCT7802Y

Menu Item	Option	Description
Hardware Monitor	See submenu	Set Hardware Monitor parameters.
Fan PWM Frequency	Low (32 Hz) / High (25 kHz)	Select PWM Frequency for the FAN.
Enable Fan Scaling	[ ] / [X]	Enabling Fan Scaling unhides a menu to define trip points to configure the Fan Speed / Temperature curve. The default is shown in the diagram below.

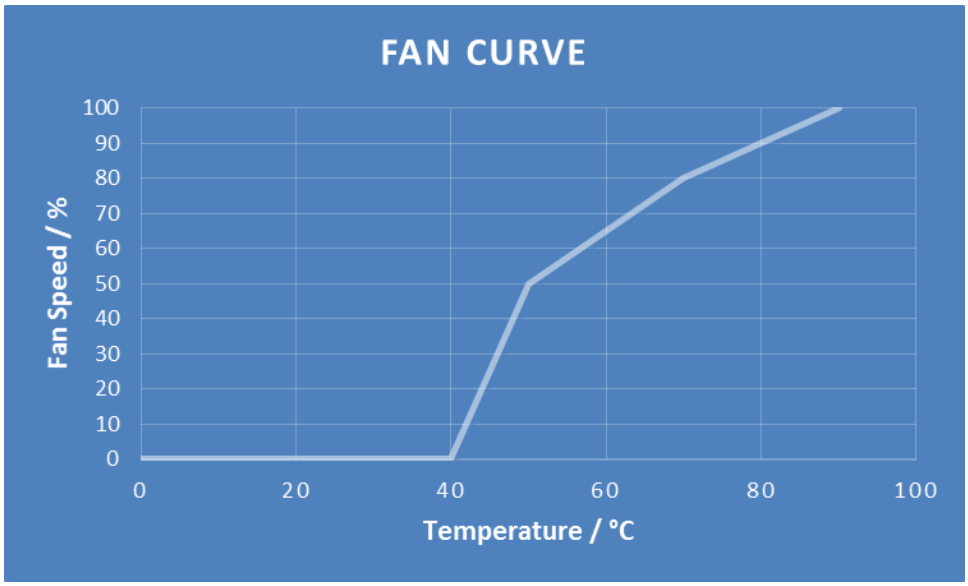

Figure 7: Fan Curve

6.6.2.10 Console Redirection

Setup Utility ⇨ Advanced ⇨ Console Redirection

Menu Item	Option	Description
Console Serial Redirect	Enabled / Disabled	Enable or disable the Console Redirection. This options unhide CR parameters when enabled.

If enabled:

Menu Item	Option	Description
Terminal Type	VT_100 / VT_100+ / VT_UTF8 / PC_ANSI	Select the Console Redirection terminal type.
Baud Rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	Select the Console Redirection Baud Rate.
Data Bits	7 Bits / 8 Bits	Select the Console Redirection Data Bits.
Parity	None / Even / Odd	Select the Console Redirection Parity Bits.
Stop Bits	1 Bit / 2 Bits	Select the Console Redirection Stop Bits.
Flow Control	None / RTS/CTS / XON/XOFF	Select the Console Redirection Flow Control type.
Information Wait Time	0 Second / 2 Second / 5 Second / 10 Second / 30 Second	Select the Console Redirection Port information display time.
C.R. After Post	Yes / No	Console Redirection continue works after POST time.
Text Mode Resolution	AUTO / Force 80x25 / Force 80x24 (DEL FIRST ROW) / Force 80x24 (DEL LAST ROW)	Console Redirection Text Mode Resolution. Auto: Follow VGA text mode Force 80x25: Don't care about VGA and force text mode to be 80x25 Force 80x24 (DEL FIRST ROW): Don't care about VGA and force text mode to be 80x24 and Del first row Force 80x24 (DEL LAST ROW): Don't care about VGA and force text mode to be 80x24 and Del last row
AutoRefresh	Enabled / Disabled	When feature enable, screen will be auto refresh once after detect remote terminal was connected.
COM_A	See submenu	Set parameters of serial Port COMA.
COM_B	See submenu	Set parameters of serial Port COMB.
HSUART-2 (Ser3)	See submenu	Set parameters of High-Speed-UART-2.
PCI_HS_UART (Ser2)	See submenu	Set parameters of PCI-High-Speed-UART.

Note: All COM / HSUART submenu are identical and, thus, they just will be listed once.

Menu Item	Option	Description
PortEnable	Enabled / Disabled	Enable or disable corresponding port.
UseGlobalSetting	Enabled / Disabled	If enabled use settings defined in superordinate CR menu. Disabling this option unhides corresponding settings.
Terminal Type	VT_100 / VT_100+ / VT_UTF8 / PC_ANSI	Select the Console Redirection terminal type.
Baud Rate	115200 / 57600 / 38400 / 19200 / 9600 / 4800 / 2400 / 1200	Select the Console Redirection Baud Rate.
Data Bits	7 Bits / 8 Bits	Select the Console Redirection Data Bits.
Parity	None / Even / Odd	Select the Console Redirection Parity Bits.
Stop Bits	1 Bit / 2 Bits	Select the Console Redirection Stop Bits.
Flow Control	None / RTS/CTS / XON/XOFF	Select the Console Redirection Flow Control type.

6.6.2.11 H2OUVE Configuration

Setup Utility ⇨ Advanced ⇨ H2OUVE Configuration

Menu Item	Option	Description
H2OUVE Support	Enabled / Disabled	Enable or disable support for Insyde Tool H2OUVE (UEFI Variable Editor). This tool is used to change i.e. default values of a BIOS image.

6.6.3 Security

Menu Item	Option	Description
TPM Availability	Available / Hidden	Unhide or hide TPM parameters. When Hidden, don't exposes TPM to 0.
TPM Operation	No Operation / Disable and Deactivate / Enable and Activate	Enable or disable the TPM Function. Note: This option will automatically return to No-operation in next boot.
Clear TPM	[X] / [ ]	Removes all TPM context associated with a specific owner.
Set Supervisor Password	123456	Install or change the BIOS password. The length of password must be greater than one and smaller or equal ten characters.

6.6.4 Power

Menu Item	Option	Description
CPU Configuration	See submenu	
Wake on PME	Disabled / Enabled by OS / Force Enabled	Determines the action taken when the system power is off and a PCI Power Management Enable (PME) wake up event occurs.

6.6.4.1 CPU Configuration

Setup Utility ⇨ Power ⇨ CPU Configuration

Menu Item	Option	Description
Bi-directional PROCHOT#	Enabled / Disabled	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.
VTX-2	Enabled / Disabled	Enable or disable the VTX-2 mode support.
VT-d	Enabled / Disabled	Enable or disable VT-d capability. It is recommended to disable IPU when enabling this option. Note: IPU is already disabled and hidden in this BIOS.
TM1	Enabled / Disabled	Enable or disable TM1.
DTS	Enabled / Disabled	Enable or disable Digital Thermal Sensor (DTS).
Active Processor Cores	Enabled / Disabled	Enable this option to disable core in each processor package.
Core 1	Enabled / Disabled	Enable or disable Core 1. This option is hidden when Active Processor Cores is disabled.
Core 2	Enabled / Disabled	Enable or disable Core 2. This option is hidden when Active Processor Cores is disabled.
Core 3	Enabled / Disabled	Enable or disable Core 3. This option is hidden when Active Processor Cores is disabled.
Monitor Mwait	Enabled / Disabled / Auto	Enable or disable Monitor Mwait. If Auto is selected, Monitor Mwait will be disabled for Linux/Yocto OS with B1 silicon. For the rest Monitor Mwait will be enabled.
CPU Power Management	See submenu	

Setup Utility ⇨ Power ⇨ CPU Configuration ⇨ CPU Power Management

Menu Item	Option	Description
Intel® SpeedStep™	Enabled / Disabled	Allows more than two frequency ranges to be supported.
Boot performance mode	Max Performance / Max Battery	Select the performance state that the BIOS will set before OS handoff.
Intel® Turbo Boost Technology	Enabled / Disabled	Enable to automatically allow processor cores to run faster than the base operating frequency if it's operating below power, current and temperature specification limits. Hidden if Intel® SpeedStep™ is disabled.
Power Limit 1 Enable	Enabled / Disabled	Enable or Disable Power Limit 1.
Power Limit 1 Clamp Mode	Enabled / Disabled	Enable or Disable Power Limit 1 Clamp Mode.
Power Limit 1 Power	Auto / 6 – 25	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.
Power Limit 1 Time Window	Auto / 6 -128	Power Limit 1 Time Window Value in Seconds. Auto will program Power Limit 1 Time Window based on silicon default support value.
C-States	Enabled / Disabled	Enable or disable C-States. This option hide corresponding C-States options.
Enhanced C-states	Enabled / Disabled	Enable or disable C1E (Auto halt, low frequency, low voltage). When enabled, CPU will switch to minimum speed when all cores enter C-State. Hidden if C-States is disabled.
Max Package C State	S0ix default / PC2 / C0	This option controls the Max Package C-State that the processor will support. Hidden if C-States is disabled.
Max Core C State	Fused value / Core C10 / Core C9 / Core C8 / Core C7 / Core C6 / Core C1 / Unlimited	This option controls the Max Core C-State that cores will support. Hidden if C-States is disabled.
C-State Auto Demotion	Disabled / C1	Configure C-State Auto Demotion. Hidden if C-States is disabled.
C-State Un-demotion	Disabled / C1	Configure C-State Un-demotion. Hidden if C-States is disabled.

6.6.5 Boot

Menu Item	Option	Description
Boot Type	Dual Boot Type / Legacy Boot Type / UEFI Boot Type	Select boot type to Dual type, Legacy type or UEFI type. Note: Operating systems installed in UEFI only will boot in UEFI or Dual boot type, not in Legacy. Also the other way around when an OS is installed in Legacy it will not boot in UEFI type.
Quick Boot	Enabled / Disabled	Allow InsydeH2O to skip certain tests while booting. This will decrease the time needed to boot the system.
Quite Boot	Enabled / Disabled	Enable or disable booting in Text mode. No textual outputs are given while booting if this option is disabled.
Network Stack	Enabled / Disabled	Enable or disable Network stack Support: Windows 8 BitLocker Unlock UEFI IPv4/IPv6 PXE Legacy PXE OPROM Note: This option will grey-out the PXE Boot capability option.
PXE Boot capability	Disabled / UEFI: IPv4 / UEFI: IPv6 / UEFI: IPv4/IPv6	Disabled: Support Network Stack UEFI PXE: IPv4/IPv6 Legacy: Legacy PXE OPROM only
Power up In Standby Support	Enabled / Disabled	Enable or disable the Power Up in Standby Support (PUIS). The PUIS feature allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.
Add Boot Options	First / Last / Auto	Position in Boot Order for Shell, Network and Removables.
ACPI Selection	Acpi1.0B / Acpi3.0 / Acpi4.0 / Acpi5.0 / Acpi6.0 / Acpi6.1	Select booting to which ACPI version.
USB Boot	Enabled / Disabled	Enable or disable booting to USB boot device.
UEFI OS Fast Boot	Enabled / Disabled	If enabled the system firmware does not initialize keyboard and check for firmware menu key. Note: If enabled it is not possible to change to BIOS menu by pressing <F10> when booting Windows.
USB Hot Key Support	Enabled / Disabled	Enable or disable to support USB hot key while booting. This will decrease the time needed to boot the system, however, it is not possible to get into BIOS menu by pressing <ESC> while booting. The change into BIOS has to be done over OS.
Timeout	0 – 10	The number of seconds that the firmware will wait before booting the original default boot selection.
Automatic Failover	Enabled / Disabled	Enable: If boot to default device fail, it will directly try to boot next device. Disable: If boot to default device fail, it will pop warning message then go into firmware UI.
EFI / Legacy	Submenu depends on bootable devices	Option to adapt boot order. Selection depends on boot devices connected. Note: Add Boot Options has to be configured as First or Last. The order can be changed by pressing <F5> or <F6>.

6.6.6 Exit

Menu Item	Option	Description
Exit Saving Changes		Save changes and reboot system afterwards. <F10> can be used for this operation.
Save Change Without Exit		Save changes without reboot system.
Exit Discarding Changes		Exit InsydeH2O Setup Utility without saving any changes. <ESC> can be used for this operation.
Load Optimal Defaults		Load optimal default values for all setup items. <F9> can be used for this operation.
Load Custom Defaults		Load custom default values for all setup items.
Save Custom Defaults		Save custom defaults for all setup items.
Discard Changes		Discard all changes without exiting InsydeH2O Setup Utility.

6.7 BIOS Update

The uEFI BIOS update instruction serves to guarantee a proper way to update the uEFI BIOS on the TQMxE39S.
Please read the entire instructions before beginning the BIOS update.
By disregarding the information you can destroy the uEFI BIOS on the TQMxE39S.
This document will guide the customer to update the uEFI BIOS on the TQMxE39S by using the Insyde Flash Firmware Tools.
Please contact support@tq-group.com for more information to the latest uEFI BIOS version for the TQMxE39S.

Note: Installation procedures and screen shots	
	Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

6.7.1 Step 1: Preparing USB Stick

A USB stick with FAT32 format can be used. Copy the following files to the USB stick.
(See: https://www.tq-group.com/de/support/downloads/tq-embedded/software-treiber/x86-architektur/)

- H2OFFT-Sx64.efi (Flash Firmware Tool from Insyde for update via UEFI Shell)
- InsydeH2OFF_x86_WIN folder (Flash Firmware Tool from Insyde for update via Windows 32-bit system)
- InsydeH2OFF_x86_WINx64 folder (Flash Firmware Tool from Insyde for update via Windows 64-bit system)
- BIOS.bin file e.g. xx.bin

6.7.2 Step 2a: Updating uEFI BIOS via EFI Shell

Plug the USB stick into the board you want to update the uEFI BIOS, and turn on the board. The board will boot and go to the internal EFI shell. Note: If a boot device is plugged change to “Boot Manager“ over Front Page and select “Internal EFI Shell“.

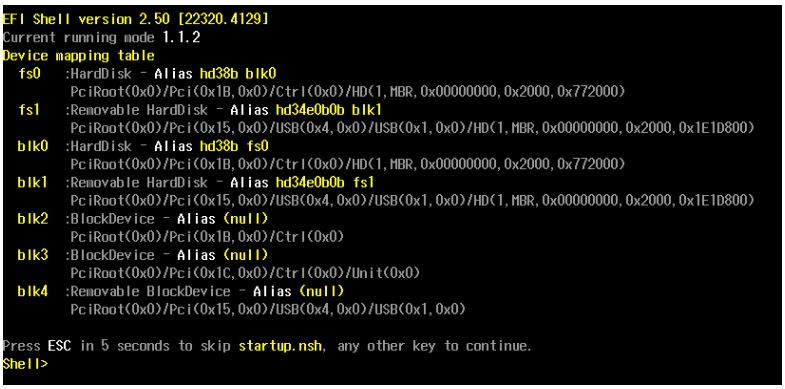

Figure 8: EFI Shell

Please see device mapping table on the screen and select the removable hard disk file system “fsX“ (X = 0, 1, 2, …).
Move operating directory to USB drive with e.g. “`fs0:`“
Then, enter into the BIOS folder (e.g. “`cd tqmxe39s`“) to execute the Insyde BIOS update tool:

```
H2OFFT-Sx64.efi <BIOS file> -ALL -RA
```

If the argument “`-RA`“ is set the SMBIOS data will not be overwritten and the UUID included in SMBIOS data will be preserved. However, this argument is not necessary.

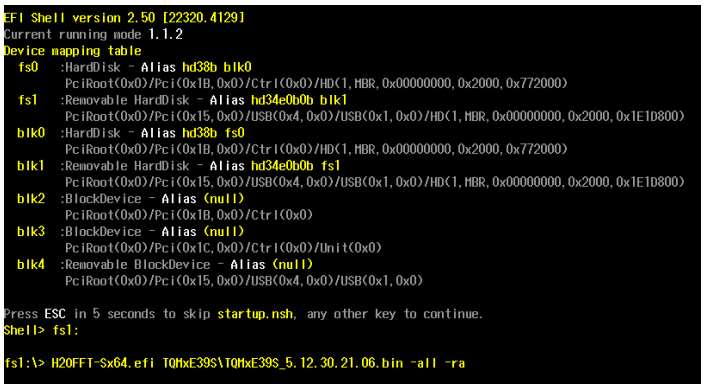

Figure 9: EFI Shell uEFI BIOS Update

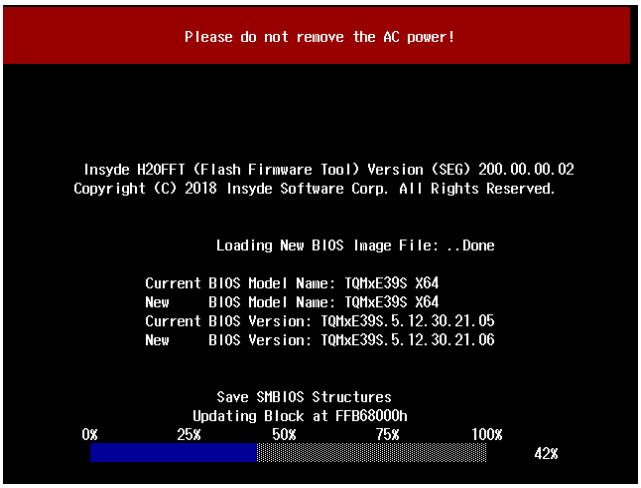

Figure 10: Screen during BIOS Update

6.7.3 Step 2b: Updating uEFI BIOS via Windows Operating System

Boot the Windows operating system (64-bit) and plug the USB stick into the board you want to update the uEFI BIOS.
Start the Command prompt (CMD), important the Command Prompt must be started in the administrator mode.

Select the BIOS update folder with the Insyde Windows 64-bit update tool and execute the Insyde BIOS update tool.

```
H2OFFT-Wx64.exe <BIOS file>.bin -all -ra
```

For the <BIOS file> argument, please specify the .bin file with the full path (e. g.: D:\TQMxXXXX_X.xx.xx.xx.xx.bin).

If the argument "-RA" is set the SMBIOS data will not be overwritten and the UUID included in SMBIOS data will be preserved. However, this argument is not necessary.

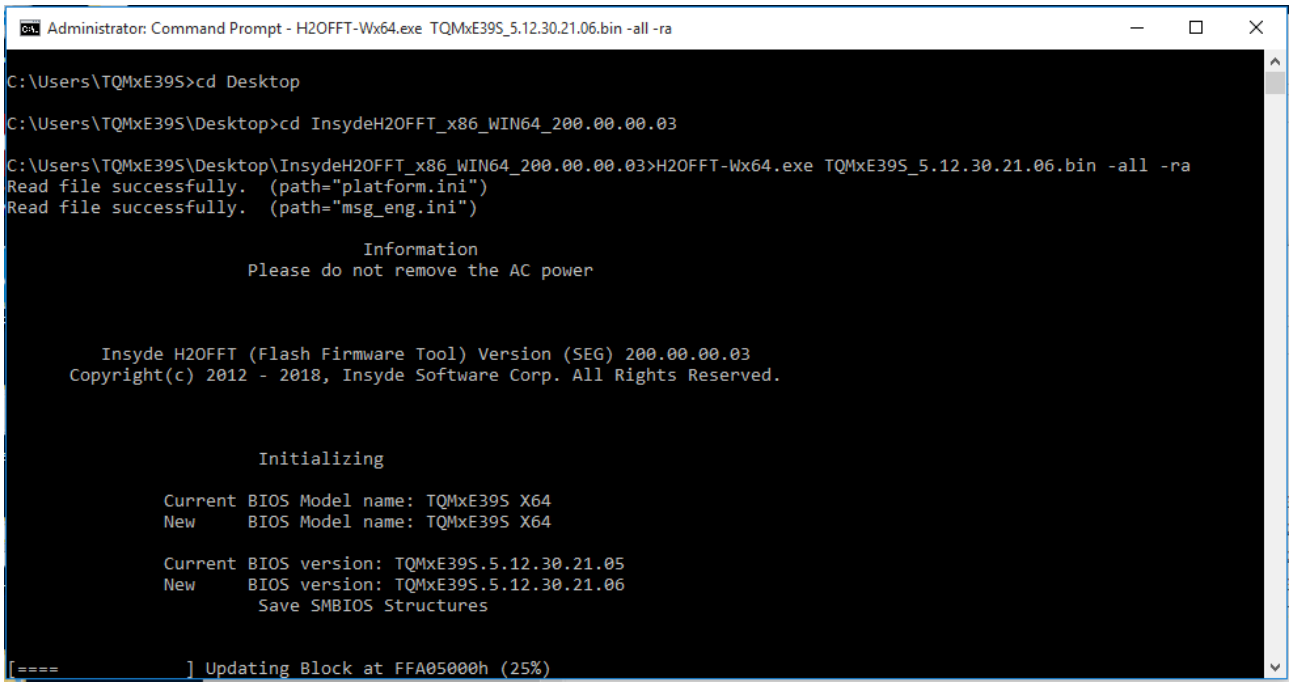

Figure 11: Windows 10 64-bit BIOS update

Start the BIOS update with the Insyde Windows 64-bit update tool.
Note: The start of updating BIOS could need longer time (up to 2 – 3 minutes). Means, the initializing information of current and new BIOS will be shown immediately whereas the "Updating Block at …" need longer time.

6.7.4 Step 3: BIOS update check on the TQMxE39S Module

After the uEFI BIOS update the new uEFI BIOS configures the complete TQMxE39S hardware and this results in some reboots and the first boot time takes longer (up to 1 – 2 minutes).

The TQMxE39S includes a dual colour Debug LED providing boot and uEFI BIOS information.

If the green LED is blinking the uEFI BIOS is booting. If the green LED is lit the uEFI BIOS boot is finished.

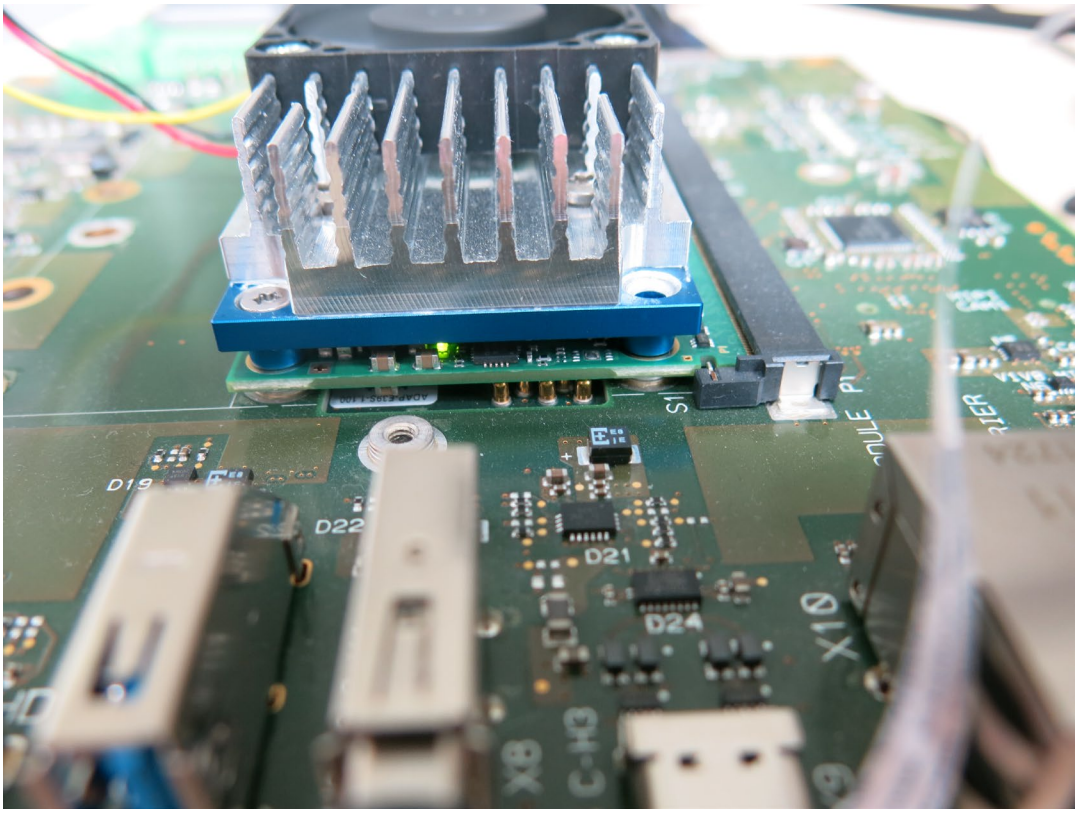

Figure 12: TQMxE39S Debug LED

After the uEFI BIOS has been flashed completely, please check whether the uEFI BIOS has been flashed successfully. The BIOS Main menu includes the board and hardware information and it shows the installed BIOS version.

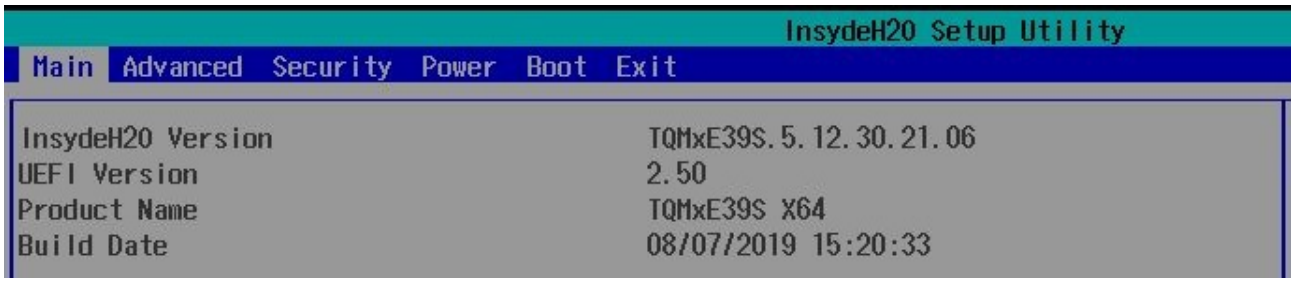

Figure 13: EFI BIOS Main Menu

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMxE39S was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were done on the TQMxE39S.

7.3 Shock & Vibration

The TQMxE39S is designed to be insensitive to shock and vibration and impact.
The design avoids additional connectors like SO-DIMM sockets to support applications also in harsh environments.

7.4 Operational Safety and Personal Security

Due to the occurring voltages (≤20 V DC), tests with respect to the operational and personal safety haven't been carried out.

7.5 Reliability and Service Life

The MTBF according to MIL-HDBK-217F N2 is 435,070 hours, Ground Benign, at +40 °C.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The TQMxE39S is manufactured RoHS compliant.

- All used components and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

8.2 WEEE®

WEEE® regulations do not apply since the TQMxE39S cannot operate on its own.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMxE39S must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMxE39S enable compliance with EuP requirements for the TQMxE39S.

8.5 Battery

No batteries are assembled on the TQMxE39S.

8.6 Packaging

The TQMxE39S is delivered in reusable packaging.

8.7 Other Entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMxE39S, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and Definitions

The following acronyms and abbreviations are used in this document:

Table 13: Acronyms

Acronym	Meaning
AHCI	Advanced Host Controller Interface
ATA	Advanced Technology Attachment
BIOS	Basic Input/Output System
BOM	Bill Of Material
CAN	Controller Area Network
CPU	Central Processing Unit
CSM	Compatibility Support Module
DDI	Digital Display Interface
DDR3L	Double Data Rate 3 Low Voltage
DMA	Direct Memory Access
DP	Display Port
DVI	Digital Visual Interface
EAPI	Embedded Application Programming Interface
eDDI	embedded Digital Display Interface
EDID	Extended Display Identification Data
eDP	embedded Display Port
EEPROM	Electrically Erasable Programmable Read-only Memory
EFI	Extensible Firmware Interface
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multi-Media Card
eSATA	external Serial ATA
ESD	Electro-Static Discharge
FAE	Field Application Engineer
FPGA	Field Programmable Gate-Array
FR-4	Flame Retardant 4
FTPM	Firmware Trusted Platform Module
GbE	Gigabit Ethernet
GFX	Graphics
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPMI	General Purpose Media Interface
GPO	General Purpose Output
GPT	General Purpose Timer
HD	High Definition
HDMI	High Definition Multimedia Interface
HEVC	High Efficiency Video Coding
HFM	High Frequency Mode
HPD	Hot Plug Detection
I	High Definition Audio
I/O	Input Output
I^2C	Inter-Integrated Circuit
IDE	Integrated Device Electronics
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IoT	Internet of Things
IP	Ingress Protection
IRQ	Interrupt Request
JEIDA	Japan Electronic Industries Development Association
JPEG	Joint Photographic Experts Group
JTAG®	Joint Test Action Group
LED	Light Emitting Diode
LP	Low Power or Low Profile

9.1 Acronyms and Definitions (continued)

Table 13: Acronyms (continued)

Acronym	Meaning
LPC	Low Pin-Count
LVDS	Low Voltage Differential Signal
MISO	Master In Slave Out
MMC	Multimedia Card
MOSI	Master Out Slave In
mPCIe	Mini PCIe
MPEG	Moving Picture Experts Group
mSATA	Mini SATA
MTBF	Mean operating Time Between Failures
N/A	Not Applicable
OD	Open Drain
OpROM	Option ROM
OS	Operating System
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	PCI Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PICMG®	PCI Industrial Computer Manufacturers Group
PU	Pull-Up
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RMA	Return Merchandise Authorization
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RSVD	Reserved
RTC	Real-Time Clock
SATA	Serial ATA
SCU	System Configuration Utility
SD card	Secure Digital Card
SD/MMC	Secure Digital Multimedia Card
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SGET	Standardization Group for Embedded Technologies
SIMD	Single Instruction Multiple Data
SMARC	Smart Mobility ARChitecture
SMBus	System Management Bus
SO-DIMM	Small Outline Dual In-Line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SSD	Solid-State Drive
TBD	To Be Determined
TDM	Time-Division Multiplexing
TDP	Thermal Design Power
TPM	Trusted Platform Module
TPM_PP	Trusted Platform Module Physical Presence
UART	Universal Asynchronous Receiver and Transmitter
uEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
VC1	Video Coding (standard) 1
VESA	Video Electronics Standards Association
VP9	Video Playback 9
WDT	Watchdog Timer
WEEE®	Waste Electrical and Electronic Equipment

9.2 References

Table 14: Further Applicable Documents and Links

No.	Name	Rev., Date	Company
(1)	SMARC (Smart Mobility ARChitecture) Hardware Specification	Version 2.0, June 2, 2016	SGET
(2)	SMARC (Smart Mobility ARChitecture) Design Guide	Rev. 2.0, March 23, 2017	SGET

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Technology in Quality