TQMLS102xA
User's Manual

TQMLS102xA UM 0105
29.11.2019

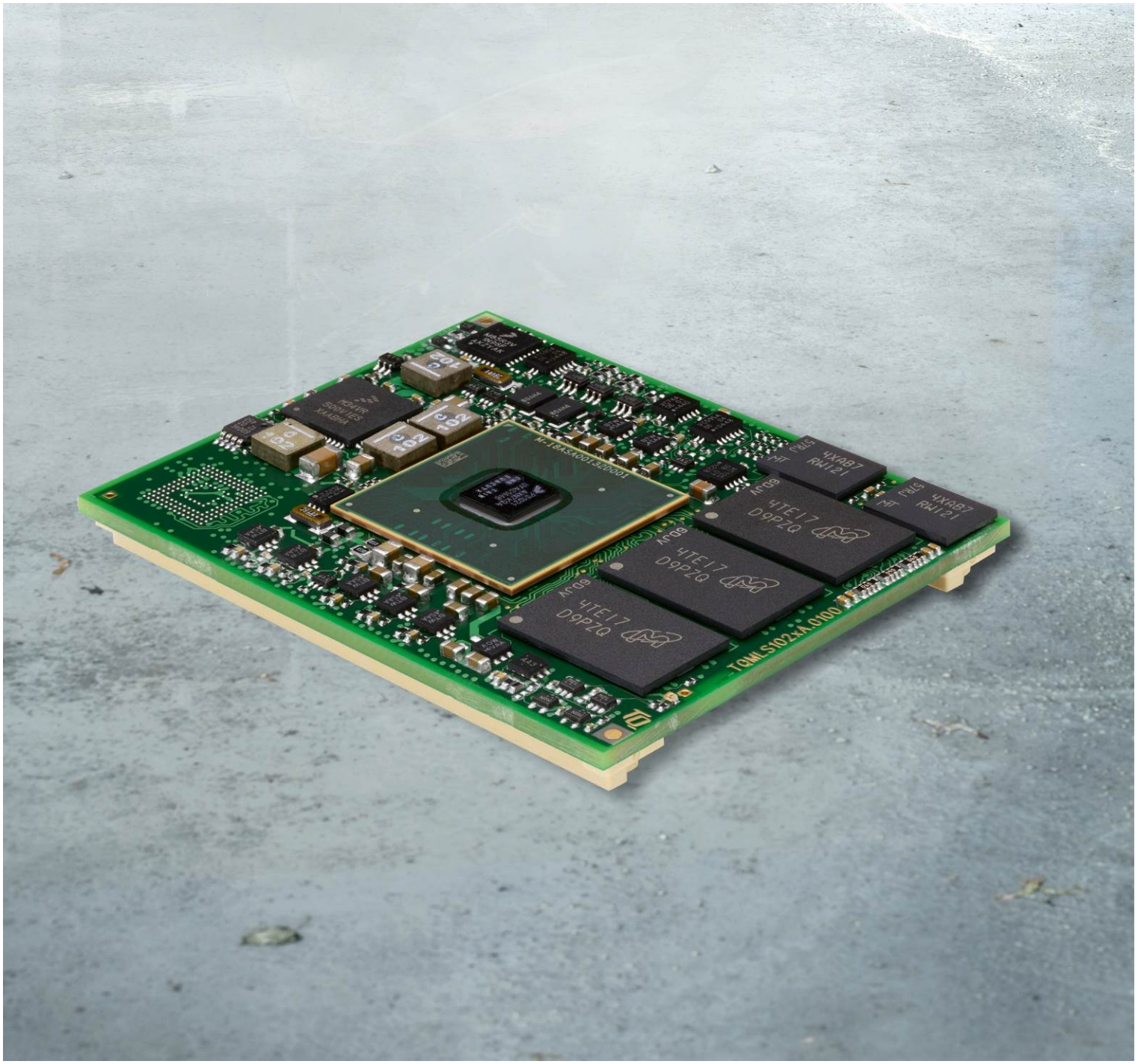

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	18.07.2016	Petz		First issue
0101	24.08.2016	Petz	All Illustration 6 Table 6 Table 7, Table 8, Table 9	Typo Text in illustration translated Address (hex) added Pull-Ups and Pull-Downs added and corrected
0102	21.10.2018	Petz	All Table 4 4.1.3 4.4.1, 4.4.3 1.3, 4.2.2, 4.4.2, 4.5, 4.7, 5.6, Illustration 7, Illustration 9, Illustration 13, Table 8 Illustration 14 Table 6, Table 7, Table 13, 4.6, 4.9.2 Table 10 Table 11 Illustration 16, Illustration 17, 8, Table 20	Referrer to connector on MBLS102xA added, signal name “PORESET#” corrected “RESET_REQ#” corrected to “RESET_REQ_OUT#”, 2.2 kΩ corrected to 47 kΩ Information regarding “coupling” added Warning added Reworked and updated Corrected Added X1-86: “Function” added Direction of EC1_GTX_CLK corrected “Function” of X2-25 and X2-27 corrected Updated
0103	06.12.2018	Petz	All 4.4.2, Illustration 9 Table 6 Table 8	Revision dependent PD at “BOOT_CFG0” added Revision dependent PD at “WC#” added Updated and clarified Updated and wrong I^2C address corrected
0104	08.08.2019	Petz	All All Illustration 1 4.1.3 Table 13	Non-functional corrections, clarifications OVDD and O1VDD voltages defined Updated Cfg_eng_use0 is pulled “high” corrected Superfluous “TQMLS102xA” removed
0105	29.11.2019	Petz	1.9, 9.2 Table 4 4.9.3	Link to Yocto documentation added, links updated Clarified Chapters 4.9.3 to 4.9.5 merged

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMLS102xA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLS102xA circuit diagram
- MBLS102xA User's Manual
- LS102xA Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMLS102xA

2. BRIEF DESCRIPTION

This User's Manual describes the TQMLS102xA, and refers to some software settings.
A certain TQMLS102xA derivative does not necessarily provide all features described in this User's Manual.
This User's Manual does also not replace the NXP LS102xA Reference Manuals.
The TQMLS102xA is a universal Minimodule based on the NXP Layerscape CPU LS1020A / LS1021A / LS1022A.
The Layerscape CPU is a Dual Cortex A7 with QorIQ technology.
The TQMLS102xA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
A suitable CPU derivative (LS1020A, LS1021A, and LS1022A) can be selected for each requirement.

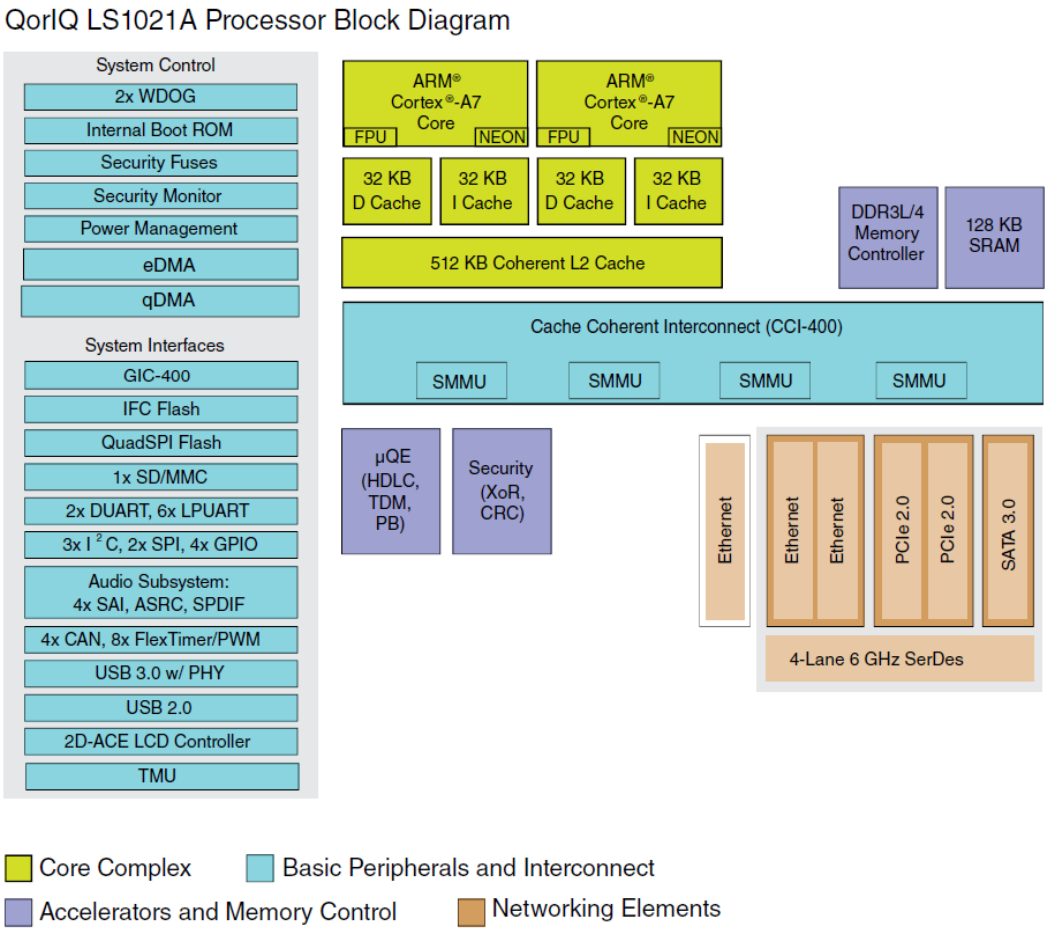


Illustration 1: Block diagram LS1021A (simplified)
(Source: NXP)

All essential LS102xA pins are routed to the TQMLS102xA connectors.
There are therefore no restrictions for customers using the TQMLS102xA with respect to an integrated customised design.
Furthermore all components required for the LS102xA to function like DDR3L SDRAM, eMMC, power supply and power management are integrated on the TQMLS102xA.
The main TQMLS102xA characteristics are:

- CPU derivatives LS1020A, LS1021A, LS1022A
- DDR3L SDRAM with ECC
- eMMC and NOR flash
- Single supply voltage 3.3 V
- On-board RTC / EEPROM / temperature sensor
- Extended power management
- Simple boot source selection

The MBLS102xA is used as a carrier board for the TQMLS102xA.

3. OVERVIEW

3.1 Block diagram

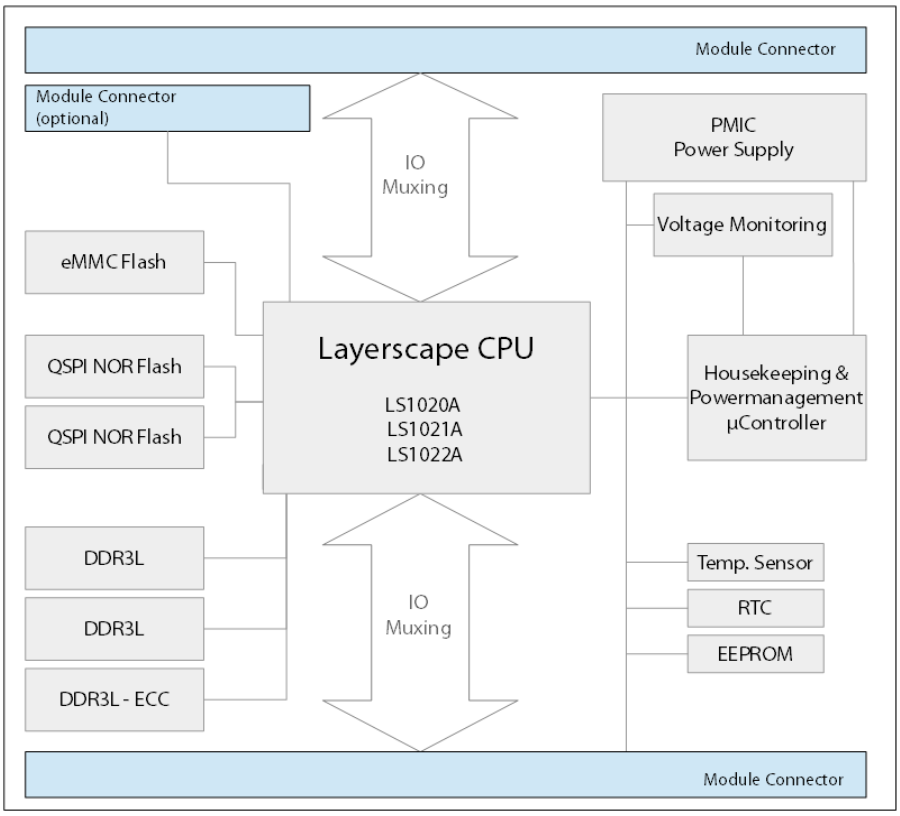


Illustration 2: Block diagram TQMLS102xA (simplified)

3.2 System components

The TQMLS102xA provides the following key functions and characteristics:

- Layerscape CPUs LS1020A / LS1021A / LS1022A
- Oscillators for LS102xA and DDR3L
- Reset structure and power-sequencing
- Power supply by PMIC
- Supervision of all voltages
- Housekeeping / Power management µController (PMC)
- Temperature sensor
- RTC
- EEPROM
- DDR3L SDRAM with ECC
- QSPI NOR flash
- eMMC
- Three connectors (280 pins)

All essential LS102xA pins are routed to the TQMLS102xA connectors.
There are therefore no restrictions for customers using the TQMLS102xA with respect to an integrated customised design.
All TQMLS102xA versions are fully pin-compatible and therefore interchangeable.
The functionality of the different TQMLS102xA is mainly determined by the features provided by the respective LS102xA.

4. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMLS102xA, and the BSP provided by TQ-Systems GmbH. See also chapter 6.

4.1 LS102xA

4.1.1 Reset Configuration Word RCW

The Reset Configuration Word RCW can be taken from the QorIQ LS1021A Reference Manual (1).

4.1.2 RCW source selection

The LS102xA permits to store the RCW in the eSDHC, QSPI and several parallel flashes, see QorIQ LS1021A Reference Manual (1).
On the TQMLS102xA the RCW source is selected and time-controlled actively driven by the Power Management Controller PMC MKL04Z16 (3). No external pin strapping is required.

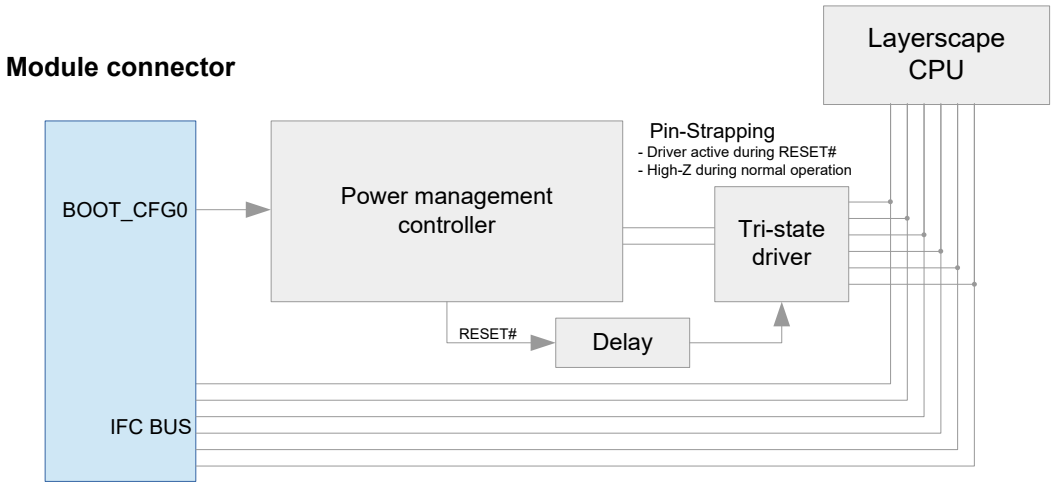


Illustration 3: Block diagram RCW source selection

The signal BOOT_CFG0 selects the boot source.

Table 2: RCW source selection

BOOT_CFG0	RCW Source	Pin strapping RCW[0:8]
Low	eSDHC	0 0100 0000b
High	QSPI	0 0100 0100b

- A 10 kΩ PD is assembled on TQMLS102xA ≤ Rev. 0202 at BOOT_CFG0
- A 100 kΩ PD is assembled on TQMLS102xA ≥ Rev. 0203 at BOOT_CFG0

After the TQMLS102xA is powered-up, the Power Management Controller applies the pin strapping.
The RESET# signal switches the drivers to high-impedance with a delay of +3 SYSCLOCKs, and thus removes the pin strapping from the bus.

4.1.3 Clock supply

The clock supply on the TQMLS102xA corresponds to the structure „Multiple Reference clocking“, described in the QorIQ LS1021A Reference Manual (1).

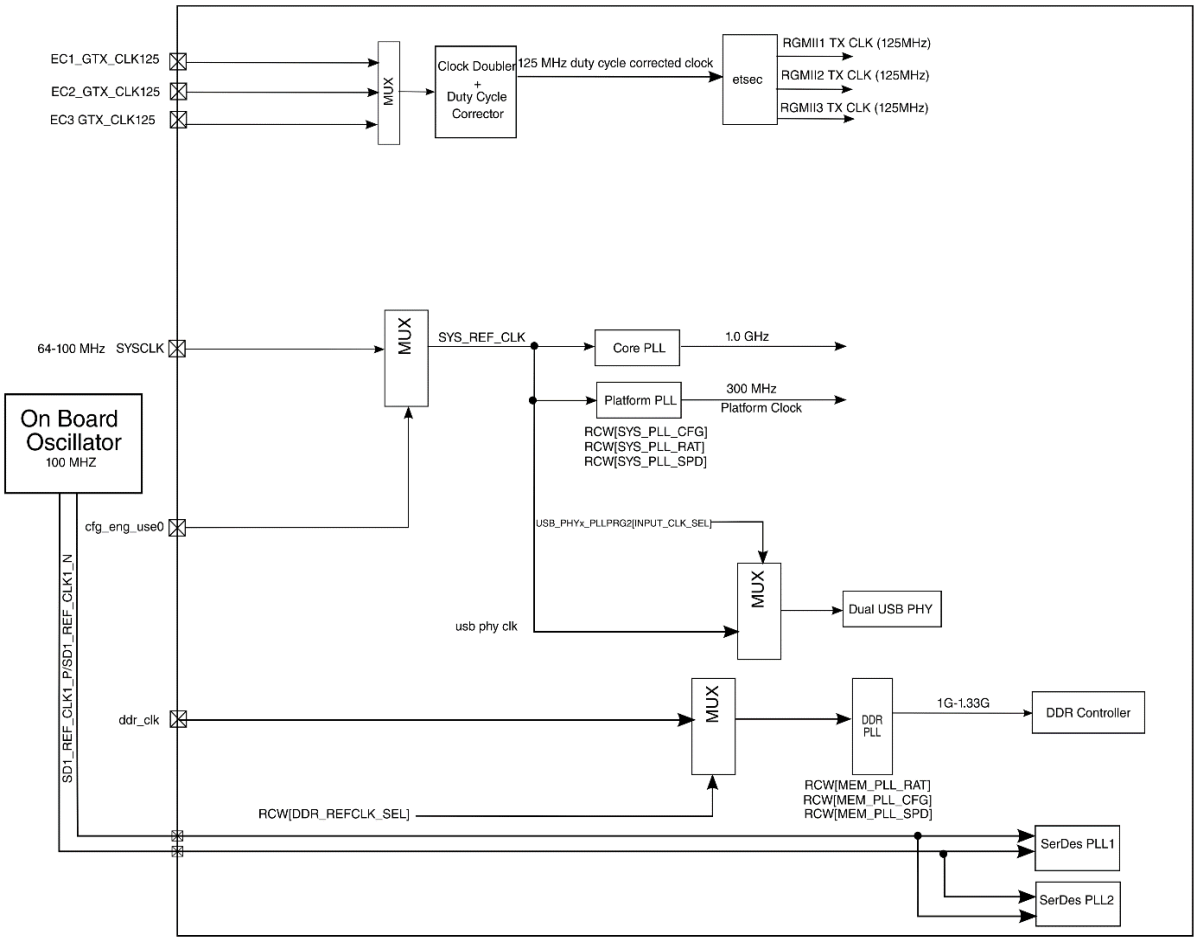


Illustration 4: Block diagram clock generation
(Source: NXP)

- Cfg_eng_use0 is pulled “high” by the pin strapping. Thus configured to Single-Ended SYSCLK.
- SYSCLK = 100 MHz
- DDRCLK provides two options:
  - Same clock as SYSCLK (default)
  - 66.666 MHz clock independent from SYSCLK (placement option)
- ECx_GTX_CLK125 is not generated on the TQMLS102xA, but has to be generated externally.
- Differential SERDES clocks are not generated on the TQMLS102xA, but have to be generated externally.

The SERDES reference clock inputs SD_REF_CLK_P/N are DC-coupled on the TQMLS102xA. The signals are directly routed from the LS102xA to the TQMLS102xA connectors. Coupling capacitors have to be placed on the carrier board.

4.1.4 Power Modes

- LPM20 (Sleep Mode)
- LPM35 (Deep Sleep Mode)

Deep Sleep is an especially efficient energy saving mode (LPM35), a variation of the LPM20, were Core supply parts are switched off. The transition to Deep Sleep is a complicated multistage process. It is partly controlled by software, and partly by an LS102xA internal State Machine, which also has to be configured by software. (Up to now this feature is not tested.)

4.1.5 JTAG

The JTAG interface is routed to the connectors. The signals TDI, TCK, TMS, and TRST# have 10 kΩ pull-ups to OVDD (1.8 V).

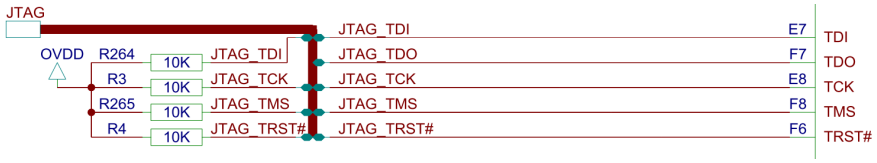


Illustration 5: Block diagram JTAG interface

The signal JTAG_TRST# is connected with PORESET# by resistors.

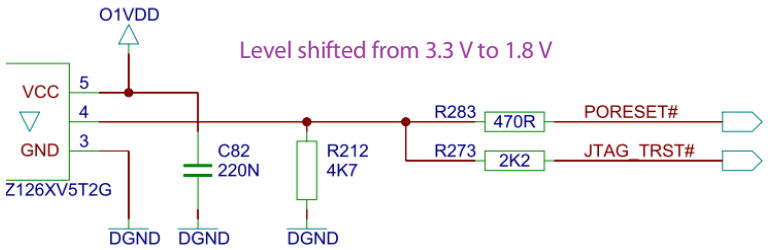


Illustration 6: Wiring of JTAG_TRST# and PORESET#

JTAG_TRST# is pulled low simultaneously with PORESET#, but it can also be pulled low by an external debugger, while PORESET# remains unchanged.

4.2 Power supply

4.2.1 Input voltage

The TQMLS102xA requires a 3.3 V supply with a maximum tolerance ±3 %. The peak power consumption is approx. 3.6 W.
A continuous power consumption (measured during tftp download) is around 2.6 W.
It is recommended to design the power supply for a worst case power consumption of 5 W.
The values given in the following table are estimated and assume an average load.

Table 3: Power consumption

Component	Estimated power consumption
LS102xA	1.5 W
DDR3L SDRAM	1.0 W
NOR flash	0.2 W
Other	0.5 W
Total	**3.2 W**

4.2.2 Power-up sequencing

The TQMLS102xA complies with the sequencing specification defined by NXP.
It must be ensured, that external components also comply with the sequencing specification.
External voltages have to be applied immediately or ideally after the TQMLS102xA is supplied with power.
The power management controller provides the signal PMC_PWR_STATUS at the TQMLS102xA connector, which can be used to activate external voltages. The signal is switched “High” (3.3 V), when all voltages on the TQMLS102xA are stable.
The maximum load at pin PMC_PWR_STATUS (X1-86) is 5 mA. Further information regarding power-up can be taken from (7).

4.3 Reset Structure

The following illustration shows the TQMLS102xA reset structure.

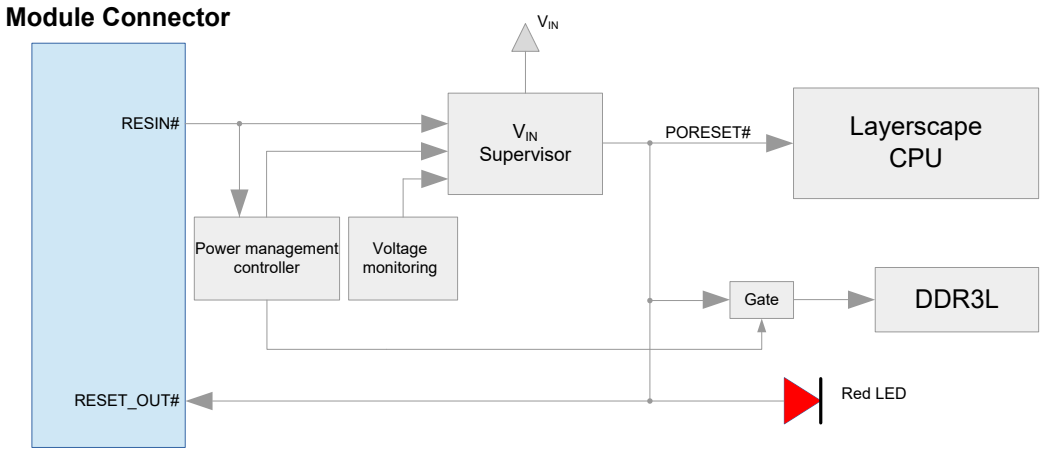


Illustration 7: Block diagram reset structure

A red LED indicates the reset status of the TQMLS102xA. The LED lights up during boot-up, when the Reset Configuration is read or when e.g. a TQMLS102xA-internal voltage is outside its defined range.

- RESIN# keeps the TQMLS102xA in RESET#
- Further RESET# sources are:
  - VIN Power Fail
  - PMC Power Management Controller
  - Voltage Supervisor ADM1069 [1]

Table 4: RESET options

Wiring at RESIN#	Reset function
Open Drain	Self-reset possible Logic Low at RESIN# triggers RESET
Open, or Pull-up ≥47 kΩ to VCC3V3	Self-reset possible RESET_REQ_OUT# can trigger RESIN# on TQMLS102xA
Pull-up <10 kΩ to VCC3V3	**No** self-reset possible RESET_REQ_OUT# cannot trigger RESIN# on TQMLS102xA
Push/Pull driver	**No** self-reset, but external RESET possible Logic High at RESIN# overrides RESET_REQ_OUT# on TQMLS102xA

1: The Supervisor is an assembly option.

4.4 Memory

4.4.1 SPI NOR Flash

Up to two QSPI NOR flash devices can be assembled on the TQMLS102xA.
The following illustration shows how the QSPI NOR flash devices are connected on the TQMLS102xA.

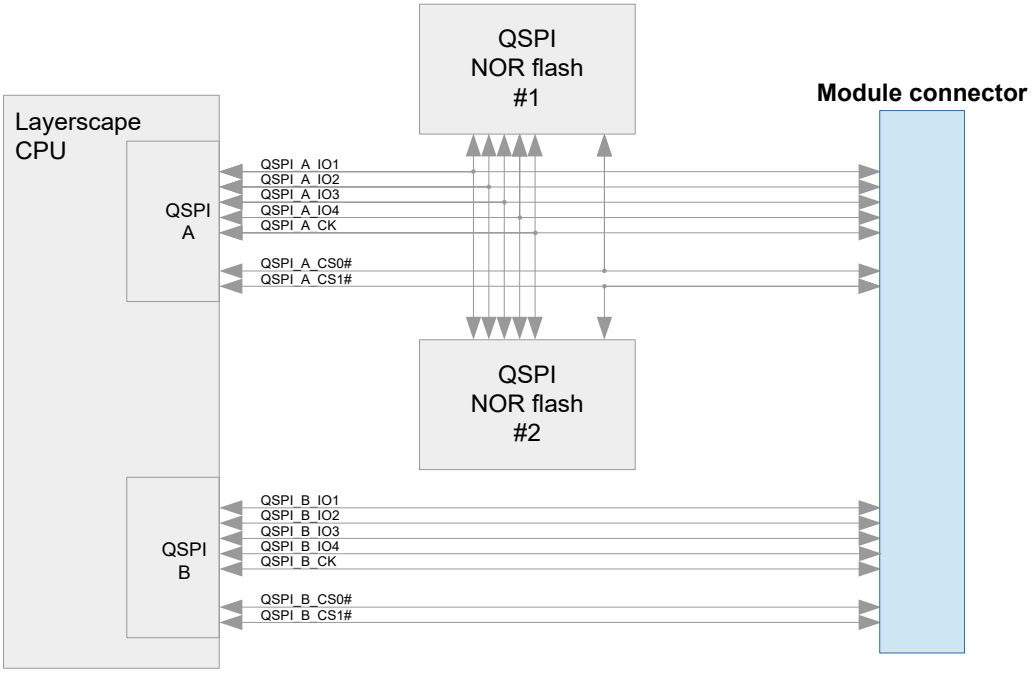


Illustration 8: Block diagram SPI NOR flash interface

- NOR flash #1 is the boot device; QSPI_A_CS0# is used as chip select.
- All QSPI signals are routed to the TQMLS102xA connectors; see multiplexing options.

Table 5: SPI NOR flash

Manufacturer	Size	Remark
Micron	256 Mbit	Size of each NOR flash, #1 and #2
Micron	512 Mbit	Size of each NOR flash, #1 and #2
Micron	1024 Mbit	Size of each NOR flash, #1 and #2
Micron	2048 Mbit	Size of each NOR flash, #1 and #2

Attention: Destruction or malfunction	
	Depending on whether NOR flash is assembled on the TQMLS102xA, the QSPI_A signals routed to the connectors cannot be used externally. Please note that QSPI_A_CS0# and QSPI_A_CS1# are not available for external circuitry if both NOR flashes are assembled on the TQMLS102xA.

4.4.2 EEPROM

An M24C64 series EEPROM is assembled on the TQMLS102xA. It provides the following key features:

- 64 Kbit
- 3.3 V supply
- Max 400 kHz I²C bus clock

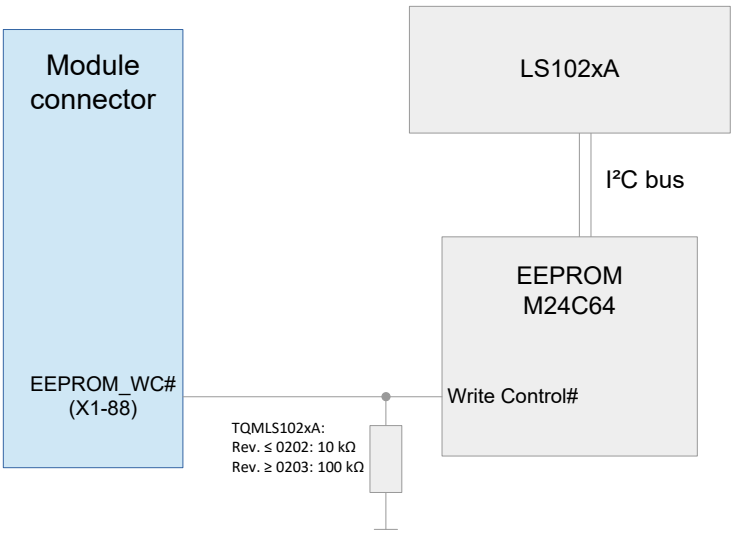


Illustration 9: Block diagram EEPROM interface

Write protection can be controlled by:

- External control with signal EEPROM_WC#: low ⇨ write enable
- 10 kΩ PD on TQMLS102xA ≤ Rev. 0202
- 100 kΩ PD on TQMLS102xA ≥ Rev. 0203

The EEPROM I²C address can be altered by assembly option to avoid address conflicts with I²C devices on the carrier board.

Table 6: EEPROM I²C addresses

Address	Remark
0x50 / 101 0000b	Default address on TQMLS102xA ≤ Rev. 0202
0x54 / 101 0100b	Default address on TQMLS102xA ≥ Rev. 0203
0x52 / 101 0010b	Alternative addresses on TQMLS102xA ≥ Rev. 0203 (assembly option)
0x56 / 101 0110b	

In the EEPROM, TQMLS102xA-specific data is stored. It is, however, not essential for the correct operation of the TQMLS102xA. The user can delete or alter the data.

In the following table, the parameters stored in the EEPROM are shown.

Table 7: EEPROM, TQMLS102xA-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	–	–	$32_{(10)}$	–	(Reserved)
0x20	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
0x30	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x40	Variable	Variable	$64_{(10)}$	ASCII	Order code
0x80	–	–	$8064_{(10)}$	–	(Unused)

4.4.3 eMMC

The SDHC interface is routed to the TQMLS102xA connectors; see multiplexing options.
Micron series MTFC2GMDEA eMMC is assembled on the TQMLS102xA.
Expansion stages with 2 Gbyte, 4 Gbyte, 8 Gbyte or 16 Gbyte are possible.

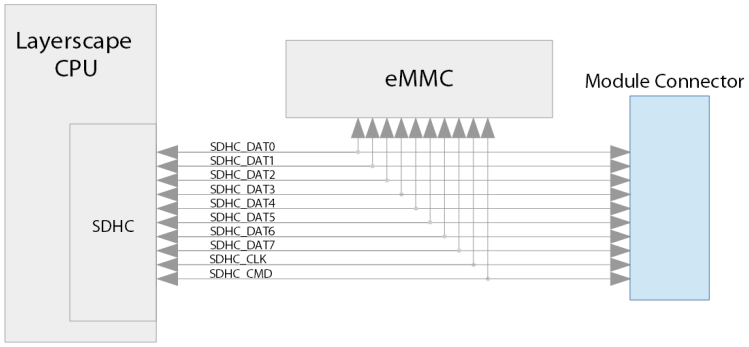


Illustration 10: Block diagram eMMC interface

Attention: Destruction or malfunction	
	The Layerscape CPUs LS102xA provide only one SDHC controller. Therefore no external SD card can be connected when eMMC is assembled on the TQMLS102xA.

4.5 Temperature sensor

The temperature sensor SA56004EDP is assembled on the TQMLS102xA. The sensor measures its own housing temperature (ambient temperature) as well as a remote temperature. This remote temperature is the die temperature of the LS102xA.

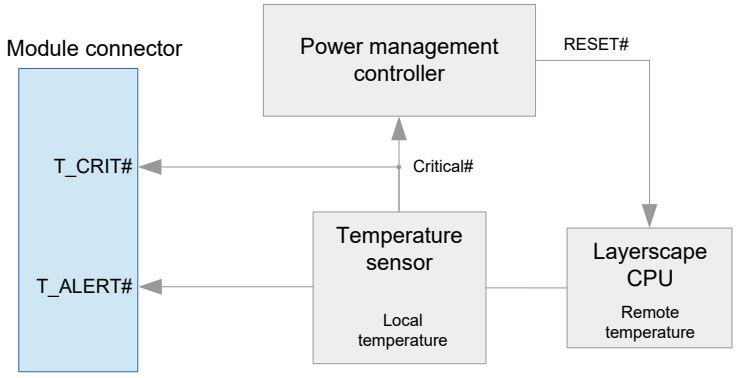


Illustration 11: Block diagram temperature sensor

- Accuracy remote: ±1 °C; accuracy local: ±2 °C
- Signal T_ALERT# provides a warning at a programmed trigger level. It is directly routed to the TQMLS102xA connector. Since the signal has an Open Drain output, an external pull-up is required.
- Signal T_CRIT# is also routed to the TQMLS102xA connector and signals the second programmed trigger level, which corresponds to the critical temperature.
  This signal is also read by the PMC, and triggers a system RESET# if the threshold is exceeded.
- The sensor is configured to T_CRIT_LOCAL = +95 °C and T_CRIT_REMOTE = +105 °C by the PMC during power-up. These values can be overwritten.

4.6 USB 3.0

The USB 3.0 interface of the LS102xA is directly routed to the TQMLS102xA connectors.

The Tx+ / Tx– AC coupling capacitors have to be assembled on the carrier board, as close as possible to the TQMLS102xA.

If the Tx+ / Tx– lines of the "Device" (Rx+ / Rx– lines on Host side) do not provide AC coupling capacitors, these capacitors have to be assembled on the carrier board, as close as possible to the USB connector.

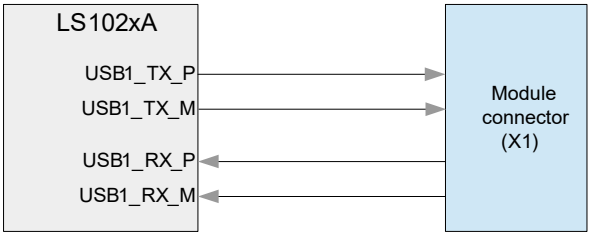


Illustration 12: Block diagram USB 3.0 interface

4.7 RTC

An RTC type PCF85063 is available as an assembly option. It is supplied with 3.3 V.

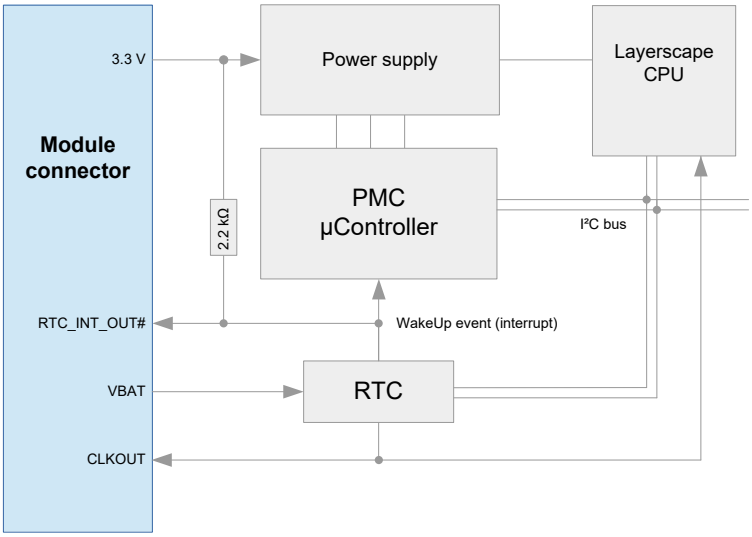


Illustration 13: Block diagram RTC interface

CLKOUT of the RTC is routed to X1-69 and fed back to GPIO1_14 of the LS102xA, RTC_INT_OUT# is routed to X1-71 and pulled-up to 3.3 V with 2.2 kΩ on the TQMLS102xA. When Advanced Power Modes are used, the TQMLS102xA can be put in Stop Mode, and wake up timer controlled via the RTC interrupt RTC_INT_OUT#.

The RTC is clocked with a 32.768 kHz crystal with an accuracy of ±20 ppm at +25 °C. This corresponds to a maximum deviation of 1.7 seconds per day. The accuracy at +85 °C is ±30 ppm. This corresponds to a maximum deviation of 2.6 seconds per day.

The RTC is supplied by VBAT. A GoldCap® or a battery is required. The following figure shows the wiring on the TQMLS102xA:

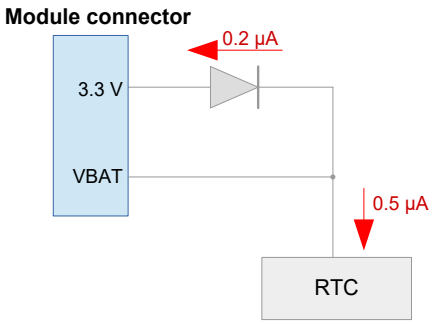


Illustration 14: Block diagram RTC buffering interface

4.8 I²C Bus

The I²C devices on the TQMLS102xA are connected to the I2C_1 bus, since the I2C_1 bus is multiplexing-independent.

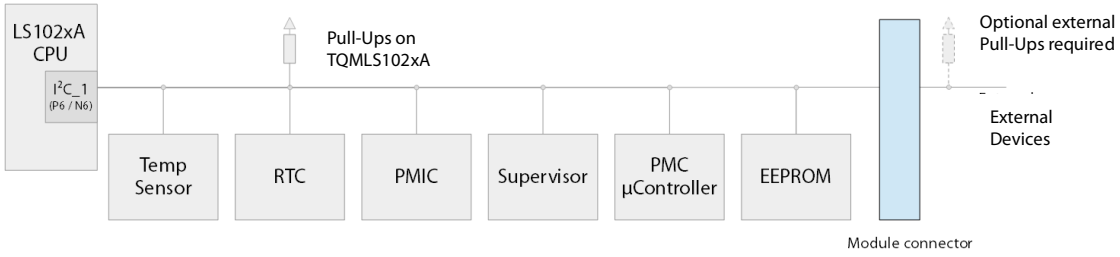


Illustration 15: Block diagram I²C bus 1

The I²C bus signals are pulled-up with 2.2 kΩ on the TQMLS102xA. More devices can be connected to the bus but then additional external pull-ups are necessary on account of the relatively high capacitive load.

Table 8: I²C addresses

Function	Device	7 bit address	8 bit address	Remark
RTC	PCF85063	0x51 / 101 0001b	0xA2 / 1010 0010b	–
Temperature sensor	SA56004EDP	0x4C / 100 1100b	0x98 / 1001 1000b	–
EEPROM	M24C64	Rev. ≤ 0202: 0x50 / 101 0000b Rev. ≥ 0203: 0x54 / 101 0100b	Rev. ≤ 0202: 0xA0 / 1010 0000b Rev. ≥ 0203: 0xA8 / 1010 1000b	See Table 6
Supervisor [2]	ADM1069	0x4F / 100 1111b	0x9E / 1001 1110b	–
PMIC	34VR500	0x04 / 000 0100b	0x08 / 0000 1000b	–
PMC	MKL04Z16	0x11 / 001 0001b	0x22 / 0010 0010b	–

Except for the PMC, the addresses are fixed and cannot be altered.

4.9 TQMLS102xA interface

4.9.1 Pin multiplexing

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The pin assignment listed in
Table 10 to Table 12 refer to the corresponding BSP provided by TQ-Systems GmbH in combination with the MBLS102xA.

Attention: Destruction or malfunction	
	Depending on the configuration many LS102xA pins can provide several different functions. Please take note of the information in the QorIQ LS1021A Reference Manual (1), concerning the pin configuration before integration or start-up of your carrier board / Starterkit.

NXP provides an Excel Sheet, which shows the Multiplexing and simplifies interface selection and configuration.

2: The Supervisor is an assembly option.

4.9.2 Pull-Ups / Pull-Downs

The following table shows all pull-ups and pull-downs assembled on the TQMLS102xA.

Table 9: Pull-ups / Pull-downs

Signal	Pin	Value	Voltage	Remark
ASLEEP	X1-83	4.7 kΩ	1.8 V	
BOOT_CFG0	X1-70	10 kΩ PD on TQMLS102xA ≤ Rev. 0202 100 kΩ PD on TQMLS102xA ≥ Rev. 0203	GND	
EC1_TX_EN	X2-75	1 kΩ	GND	
EC2_TX_EN	X2-43	1 kΩ	GND	
EC3_TX_EN	X2-59	1 kΩ	GND	
EEPROM_WC#	X1-88	10 kΩ PD on TQMLS102xA ≤ Rev. 0202 100 kΩ PD on TQMLS102xA ≥ Rev. 0203	GND	
EVT0#	X3-3	10 kΩ	1.8 V	
EVT1#	X3-5	10 kΩ	1.8 V	
EVT2#	X1-75	10 kΩ	1.8 V	
EVT3#	X1-77	10 kΩ	1.8 V	
EVT4#	X1-79	10 kΩ	1.8 V	
EVT9#	X1-81	10 kΩ	1.8 V	
GPIO1_14	X1-90	4.7 kΩ	GND	
HRESET#	X1-58	1 kΩ	1.8 V	
I2C1_SCL	X1-36	2.2 kΩ	3.3 V	
I2C1_SDA	X1-34	2.2 kΩ	3.3 V	
IRQ0	X1-85	4.7 kΩ	1.8 V	
IRQ1	X1-87	4.7 kΩ	1.8 V	
IRQ2	X2-80	4.7 kΩ	2.5 V or 3.3 V	L1VDD
IRQ3	X2-29	4.7 kΩ	2.5 V or 3.3 V	LVDD
IRQ4	X1-63	4.7 kΩ	3.3 V	
IRQ5	X1-65	4.7 kΩ	3.3 V	
JTAG_TCK	X1-78	10 kΩ	1.8 V	
JTAG_TDI	X1-82	10 kΩ	1.8 V	
JTAG_TMS	X1-76	10 kΩ	1.8 V	
JTAG_TRST#	X1-84	10 kΩ	1.8 V	
PROG_MTR	X3-7	330 Ω	GND	
QSPI_A_CS0	X1-115	4.7 kΩ	3.3 V or GND	See [3]
QSPI_A_CS1	X1-117	4.7 kΩ	3.3 V or GND	See [3]
QSPI_A_IO2	X1-107	10 kΩ	3.3 V	
QSPI_A_IO3	X1-109	10 kΩ	3.3 V	
RESET_OUT#	X1-62	1 kΩ	3.3 V	
RESET_REQ_OUT#	X1-60	2.2 kΩ	3.3 V	
RESIN#	X1-23	12 kΩ	3.3 V	
RTC_CLK_OUT	X1-69	4.7 kΩ	In series to X1.90	GPIO1_14
RTC_INT_OUT#	X1-71	2.2 kΩ	3.3 V	
SDHC_CMD	X2-10	10 kΩ	3.3 V	
TA_BB_RTC	X3-9	10 kΩ	GND	
TA_BB_TMP_DETECT#	X3-4	1 kΩ	GND	
TA_PROG_SFP	X3-6	330 Ω	GND	
TA_TMP_DETECT#	X3-8	1 kΩ	GND	
TEMP_CRIT_OUT#	X1-66	10 kΩ	3.3 V	
TEST_SEL#	X1-55	1 kΩ	1.8 V	

3: TQMLS1020A: PU at QSPI_A_CS0, PU at QSPI_A_CS1.
TQMLS1021A: PD at QSPI_A_CS0, PU at QSPI_A_CS1.
TQMLS1022A: PU at QSPI_A_CS0, PD at QSPI_A_CS1.

4.9.3 Pinout connectors X1, X2, X3

Table 10: Pinout connector X1 (X36 on MBLS102xA)

LS102xA	I/O	Function	Group	Pin name	Pin		Pin name	Group	Function	I/O	LS102xA
–	I		Power	VCC3V3IF	1	2	VCC3V3IF	Power		I	–
–	I		Power	VCC3V3IF	3	4	VCC3V3IF	Power		I	–
–	I		Power	VCC3V3IF	5	6	VCC3V3IF	Power		I	–
–	I		Power	VCC3V3IF	7	8	VCC3V3IF	Power		I	–
–	I		Power	L1VDD_IN	9	10	VBAT	Power		I	–
–	O		Power	L1VDD_OUT	11	12	DGND				
–	O		Power	LVDD_OUT	13	14	USB1_D_P	USB		I/O	D3
–	I		Power	LVDD_IN	15	16	USB1_D_M	USB		I/O	C3
				DGND	17	18	DGND				
–	O		Power	O1VDD (1.8 V)	19	20	USB1_RX_P	USB		I	B4
				DGND	21	22	USB1_RX_M	USB		I	A4
–	I		SYSTEM	RESIN#	23	24	DGND				
–	I		SYSTEM	POWER_STBY	25	26	USB1_TX_P	USB		O	B2
–	I		SYSTEM	POWER_EN	27	28	USB1_TX_M	USB		O	A2
				DGND	29	30	DGND				
–	O	For factory test only	TEST	SYSCLK_EXT	31	32	CLK_OE	TEST	For factory test only	I	–
				DGND	33	34	I2C1_SDA	I2C	2.2 kΩ PU to 3.3 V [4]	I/O	P6
–	O	For factory test only	TEST	DDRCLK_EXT	35	36	I2C1_SCL	I2C	2.2 kΩ PU to 3.3 V [4]	O	N6
				DGND	37	38	DGND				
N4	I	2D_ACE_VSYNC	UART	UART3_SIN	39	40	I2C2_SDA	I2C	SDHC_WP	I/O	L1
N3	O	2D_ACE_HSYNC	UART	UART3_SOUT	41	42	I2C2_SCL	I2C	SDHC_CD#	O	K1
N1	O		UART	UART1_SOUT	43	44	DGND				
M1	I	10 kΩ PU to 3.3 V [5]	UART	UART1_SIN	45	46	GPIO4_19	GPIO	2D_ACE_D10	I/O	K5
				DGND	47	48	DGND				
L5	I	2D_ACE_D11	GPIO	GPIO4_20	49	50	GPIO4_12	GPIO	2D_ACE_D03	I/O	J5
				DGND	51	52	GPIO4_11	GPIO	2D_ACE_D02	I/O	J4
H5	O	2D_ACE_D04	GPIO	GPIO4_13	53	54	GPIO4_10	GPIO	2D_ACE_D01	I/O	J3
F3	I	1 kΩ PU to O1VDD (1.8 V)	TEST	TEST_SEL#	55	56	GPIO4_09	GPIO	2D_ACE_D00	I/O	H3
E3	I		USB	USB1_ID	57	58	HRESET#	SYSTEM	1 kΩ PU to O1VDD (1.8 V)	I	E5
C1	I		USB	USB1_VBUS	59	60	RESET_REQ_OUT#	SYSTEM	2.2 kΩ PU to 3.3 V	O	–
				DGND	61	62	RESET_OUT#	SYSTEM		O	–
L2	I	GPIO_INT1#, 4.7 kΩ PU to 3.3 V [6]	IRQ	IRQ4	63	64	DGND				
M2	I	GPIO_INT2#, 4.7 kΩ PU to 3.3 V [6]	IRQ	IRQ5	65	66	TEMP_CRIT_OUT#	SYSTEM	10 kΩ PU to 3.3 V	O	–
				DGND	67	68	TEMP_ALERT#	SYSTEM	Open Drain	O	–
–	O		RTC	RTC_CLK_OUT	69	70	BOOT_CFG0	SYSTEM	10 kΩ or 100 kΩ PD [7]	I	–
–	O	2.2 kΩ PU to 3.3 V / VBAT	RTC	RTC_INT_OUT#	71	72	DGND				
D5	I/O	10 kΩ PU to O1VDD (1.8 V)	SYSTEM	EVT1# (TQMLS102xA Rev. 01xx)	73	74	EVT0# (TQMLS102xA Rev. 01xx)	SYSTEM	10 kΩ PU to O1VDD (1.8 V)	I/O	C5
–	I/O		PMC SWD	SWD_DIO (TQMLS102xA Rev. 02xx)			SWD_CLK (TQMLS102xA Rev. 02xx)	PMC SWD		I	–
A6	I/O	10 kΩ PU to O1VDD (1.8 V)	SYSTEM	EVT2#	75	76	JTAG_TMS	JTAG	10 kΩ PU to OVDD (1.8 V)	I	F8
B6	I/O	10 kΩ PU to O1VDD (1.8 V)	SYSTEM	EVT3#	77	78	JTAG_TCK	JTAG	10 kΩ PU to OVDD (1.8 V)	I	E8
C7	I/O	10 kΩ PU to O1VDD (1.8 V)	SYSTEM	EVT4#	79	80	JTAG_TDO	JTAG		O	F7
D7	I/O	10 kΩ PU to O1VDD (1.8 V)	SYSTEM	EVT9#	81	82	JTAG_TDI	JTAG	10 kΩ PU to OVDD (1.8 V)	I	E7
E6	O	4.7 kΩ PU to O1VDD (1.8 V)	SYSTEM	ASLEEP	83	84	JTAG_TRST#	JTAG	10 kΩ PU to OVDD (1.8 V)	I	F6
G6	I	4.7 kΩ PU to O1VDD (1.8 V)	IRQ	IRQ0	85	86	PMC_PWR_STATUS	SYSTEM	Power Good	O	–
G8	I	4.7 kΩ PU to OVDD (1.8 V)	IRQ	IRQ1	87	88	EEPROM_WC#	SYSTEM	10 kΩ PD	I	–
				DGND	89	90	GPIO1_14 / RTC	SYSTEM		I/O	E10
D15	I/O		IFC	QSPI_B_IO0	91	92	DGND				
E13	I/O		IFC	QSPI_B_IO1	93	94	QSPI_B_CS0	IFC		O	D9
C15	I/O		IFC	QSPI_B_IO2	95	96	QSPI_B_CS1	IFC		O	C10
F18	I/O		IFC	QSPI_B_IO3	97	98	QSPI_B_DQS	IFC	4.7 kΩ PU to 3.3 V [5]	I/O	D13
D10	O		IFC	QSPI_B_CK	99	100	DGND				
				DGND	101	102	SPI1_CS0#	IFC		O	D17
C11	I/O		IFC	QSPI_A_IO0	103	104	SPI1_SCK	IFC		O	C18
D11	I/O		IFC	QSPI_A_IO1	105	106	SPI1_CS5 / RCW_SRC4	IFC	RCW config during POR	I/O	A14
C12	I/O	10 kΩ PU to 3.3 V	IFC	QSPI_A_IO2	107	108	SPI1_SIN	IFC		I	F15
D12	I/O	10 kΩ PU to 3.3 V	IFC	QSPI_A_IO3	109	110	SPI1_SOUT / RCW_SRC5	IFC	RCW config during POR	I/O	B15
C9	O		IFC	QSPI_A_CK	111	112	SPI1_CS1 / RCW_SRC0	IFC	RCW config during POR	I/O	B12
				DGND	113	114	SPI1_CS2 / RCW_SRC1	IFC	RCW config during POR	I/O	A12
C8	O	4.7 kΩ PU or PD [8]	IFC	QSPI_A_CS0	115	116	SPI1_CS3 / RCW_SRC2	IFC	RCW config during POR	I/O	A13
D8	O	4.7 kΩ PU or PD [8]	IFC	QSPI_A_CS1	117	118	SPI1_CS4 / RCW_SRC3	IFC	RCW config during POR	I/O	B14
C13	I/O	4.7 kΩ PU to 3.3 V [5]	IFC	QSPI_A_DQS	119	120	DGND				

4: 4.7 kΩ PU to 3.3 V on MBLS102xA.
5: On MBLS102xA.
6: 10 kΩ PU to 3.3 V on MBLS102xA.
7: 10 kΩ on TQMLS102xA Rev. ≤ 0202; 100 kΩ on TQMLS102xA Rev. ≥ 0203.
8: TQMLS1020A: PU at QSPI_A_CS0, PU at QSPI_A_CS1.
TQMLS1021A: PD at QSPI_A_CS0, PU at QSPI_A_CS1.
TQMLS1022A: PU at QSPI_A_CS0, PD at QSPI_A_CS1.

4.9.3 Pinout connectors X1, X2, X3 (continued)

Table 11: Pinout connector X2 (X7 on MBLS102xA)

LS102xA	I/O	Function	Group	Pin name	Pin		Pin name	Group	Function	I/O	LS102xA
				DGND	1	2	SDHC_DAT4	SDHC		I/O	H2
D1	O		SDHC	SDHC_CLK	3	4	SDHC_DAT5	SDHC		I/O	H1
				DGND	5	6	SDHC_DAT6	SDHC	USB1_DRVVBUS	I/O	J2
E1	I/O		SDHC	SDHC_DAT0	7	8	SDHC_DAT7	SDHC	USB1_PWRFAULT	I/O	J1
F2	I/O		SDHC	SDHC_DAT1	9	10	SDHC_CMD	SDHC		I/O	E2
F1	I/O		SDHC	SDHC_DAT2	11	12	DGND				
G1	I/O		SDHC	SDHC_DAT3	13	14	GPIO4_22	GPIO	2D_ACE_CLK_OUT	I/O	N5
				DGND	15	16	DGND				
M5	I/O	2D_ACE_DE	GPIO	GPIO4_21	17	18	GPIO4_18	GPIO	2D_ACE_D09	I/O	K4
				DGND	19	20	GPIO4_14	GPIO	2D_ACE_D05	I/O	K3
M3	I/O	2D_ACE_D07	GPIO	GPIO4_16	21	22	GPIO4_15	GPIO	2D_ACE_D06	I/O	L3
M4	I/O	2D_ACE_D08	GPIO	GPIO4_17	23	24	UART2_SIN	UART	LPUART1_SIN	I	P2
P5	I	LPUART1_CTS#	UART	UART4_SIN	25	26	UART2_SOUT	UART	LPUART1_SOUT	O	P1
P3	O	LPUART1_RTS#	UART	UART4_SOUT	27	28	DGND				
R5	I	TOUCH_GPIO_INT#, 4.7 kΩ PU to LVDD	IRQ	IRQ3	29	30	USB2_D0	USB		I/O	U2
				DGND	31	32	USB2_D1	USB		I/O	U1
U3	I		USB	USB2_CLK	33	34	USB2_D2	USB		I/O	T1
T3	I/O		USB	USB2_D4	35	36	USB2_D3	USB		I/O	R2
T4	I/O		USB	USB2_D5	37	38	USB2_NXT	USB		I	V1
R3	I/O		USB	USB2_D6	39	40	USB2_DIR	USB		I	R1
R4	I/O		USB	USB2_D7	41	42	DGND				
T5	O	1 kΩ PD	USB	USB2_STP	43	44	EC3_RXD0	EC3		I	AA1
U5	I	10 kΩ PD [9]	USB	USB2_PWRFAULT	45	46	EC3_RXD1	EC3		I	Y2
				DGND	47	48	EC3_RXD2	EC3		I	Y1
V5	O		EC3	EC3_GTX_CLK	49	50	EC3_RXD3	EC3		I	W1
W4	O		EC3	EC3_TXD0	51	52	EC3_RX_DV	EC3		I	AA2
W3	O		EC3	EC3_TXD1	53	54	EC3_RX_CLK	EC3		I	V2
V4	O		EC3	EC3_TXD2	55	56	DGND				
V3	O		EC3	EC3_TXD3	57	58	MDIO	MDIO	1 kΩ PU to L1VDD_IN [9]	I/O	AB3
Y3	O	1 kΩ PD	EC3	EC3_TX_EN	59	60	MDC	MDIO	1 kΩ PU to L1VDD_IN [9]	O	AB2
				DGND	61	62	DGND				
Y4	I		EC3	EC3_GTX_CLK125	63	64	EC1_RX_CLK	EC1		I	AC3
				DGND	65	66	EC1_RX_DV	EC1		I	AC6
AA6	O		EC1	EC1_TXD0	67	68	EC1_RXD0	EC1		I	AB6
Y6	O		EC1	EC1_TXD1	69	70	EC1_RXD1	EC1		I	AC5
AA5	O		EC1	EC1_TXD2	71	72	EC1_RXD2	EC1		I	AC4
W5	O		EC1	EC1_TXD3	73	74	EC1_RXD3	EC1		I	AB4
W6	O	1 kΩ PD	EC1	EC1_TX_EN	75	76	DGND				
AA4	I		EC1	EC1_GTX_CLK125	77	78	EC1_GTX_CLK	EC1		O	Y7
				DGND	79	80	IRQ2	IRQ	4.7 kΩ PU to L1VDD	I	W7
W10	O	LANE_A_TX_P	SERDES	SD_TX0_P	81	82	DGND				
				DGND	83	84	SD_REF_CLK1_P	SERDES	SD_REF_CLK1_P	I	AC8
Y10	O	LANE_A_TX_N	SERDES	SD_TX0_N	85	86	DGND				
				DGND	87	88	SD_REF_CLK1_N	SERDES	SD_REF_CLK1_N	I	AB8
W11	O	SATA_TX_P	SERDES	SD_TX1_P	89	90	DGND				
				DGND	91	92	SD_RX0_P	SERDES	LANE_A_RX_P	I	AC10
Y11	O	SATA_TX_N	SERDES	SD_TX1_N	93	94	DGND				
				DGND	95	96	SD_RX0_N	SERDES	LANE_A_RX_N	I	AB10
W13	O	LANE_C_TX_P	SERDES	SD_TX2_P	97	98	DGND				
				DGND	99	100	SD_RX1_P	SERDES	SATA_RX_P	I	AC11
Y13	O	LANE_C_TX_N	SERDES	SD_TX2_N	101	102	DGND				
				DGND	103	104	SD_RX1_N	SERDES	SATA_RX_N	I	AB11
W14	O	LANE_D_TX_P	SERDES	SD_TX3_P	105	106	DGND				
				DGND	107	108	SD_RX2_P	SERDES	LANE_C_RX_P	I	AC13
Y14	O	LANE_D_TX_N	SERDES	SD_TX3_N	109	110	DGND				
				DGND	111	112	SD_RX2_N	SERDES	LANE_C_RX_N	I	AB13
AC16	I	SD_REF_CLK2_P	SERDES	SD_REF_CLK2_P	113	114	DGND				
				DGND	115	116	SD_RX3_P	SERDES	LANE_D_RX_P	I	AC14
AB16	I	SD_REF_CLK2_N	SERDES	SD_REF_CLK2_N	117	118	DGND				
				DGND	119	120	SD_RX3_N	SERDES	LANE_D_RX_N	I	AB14

9: On MBLS102xA.

4.9.3 Pinout connectors X1, X2, X3 (continued)

Table 12: Pinout connector X3 (X22 on MBLS102xA)

LS102xA	I/O	Function	Group	Pin name	Pin		Pin name	Group	Function	I/O	LS102xA
				DGND	1	2	DGND				
–	I		PMC SWD	SWD_CLK (TQMLS102xA Rev. 01xx)	3	4	TA_BB_TMP_DETECT#	TRUST	1 kΩ PD	I	U6
C5	I/O	10 kΩ PU to O1VDD (1.8 V)	SYSTEM	EVT0# (TQMLS102xA Rev. 02xx)							
–	I/O		PMC SWD	SWD_DIO (TQMLS102xA Rev. 01xx)	5	6	TA_PROG_SFP	FUSE PRG	330 Ω PD	I	F11
D5	I/O	10 kΩ PU to O1VDD (1.8 V)	SYSTEM	EVT1# (TQMLS102xA Rev. 02xx)							
F10	I	330 Ω PD	FUSE PRG	PROG_MTR	7	8	TA_TMP_DETECT#	TRUST	1 kΩ PD	I	F9
R6	I	10 kΩ PD	TRUST	TA_BB_RTC	9	10	DGND				
				DGND	11	12	IFC_AD00	IFC		I/O	A7
B8	I/O		IFC	IFC_AD01	13	14	IFC_AD02	IFC		I/O	A8
B9	I/O		IFC	IFC_AD03	15	16	IFC_AD04	IFC		I/O	A9
A10	I/O		IFC	IFC_AD05	17	18	IFC_AD06	IFC		I/O	B11
A11	I/O		IFC	IFC_AD07	19	20	IFC_WE0#	IFC		O	F14
				DGND	21	22	IFC_BTCL	IFC		O	E14
C14	O		IFC	IFC_NDDDR_CLK	23	24	DGND				
A15	I/O	RCW config during POR	IFC	IFC_AD14 / RCW_SRC6	25	26	IFC_TE / RCW_IFC_TE	IFC	RCW config during POR	O	D14
A16	I/O	RCW config during POR	IFC	IFC_AD15 / RCW_SRC7	27	28	IFC_AVD	IFC		O	C16
–	–		-	NC	29	30	IFC_NDDQS	IFC		I/O	D16
C17	O	4.7 kΩ PU to 3.3 V [10]	IFC	IFC_CS0#	31	32	DGND				
F16	I	4.7 kΩ PU to 3.3 V [10]	IFC	IFC_RB0#	33	34	IFC_OE#	IFC		O	E16
				DGND	35	36	IFC_CLE / RCW_SRC8	IFC	RCW config during POR	O	E17
A17	O		IFC	IFC_CLK0	37	38	DGND				
E18	O		IFC	IFC_WP0#	39	40	IFC_CLK1	IFC		O	B17

10: On MBLS102xA.

4.10 Assembly

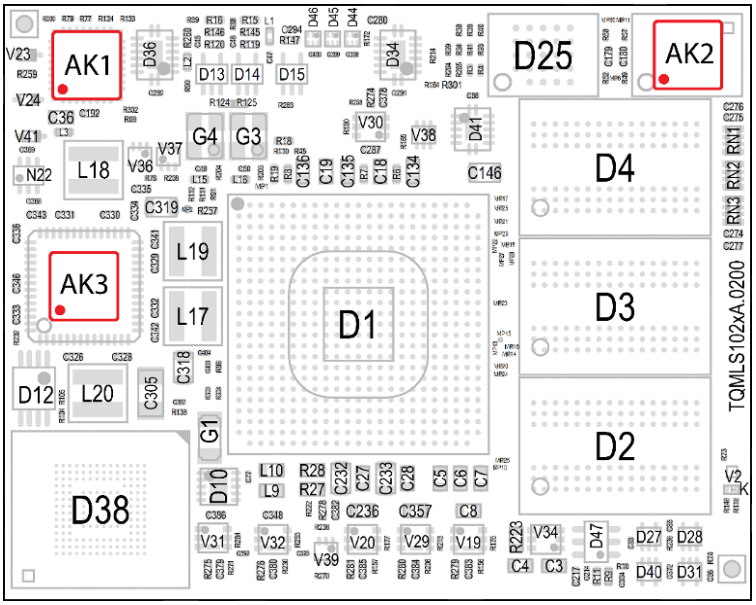


Illustration 16: TQMLS102xA assembly, top

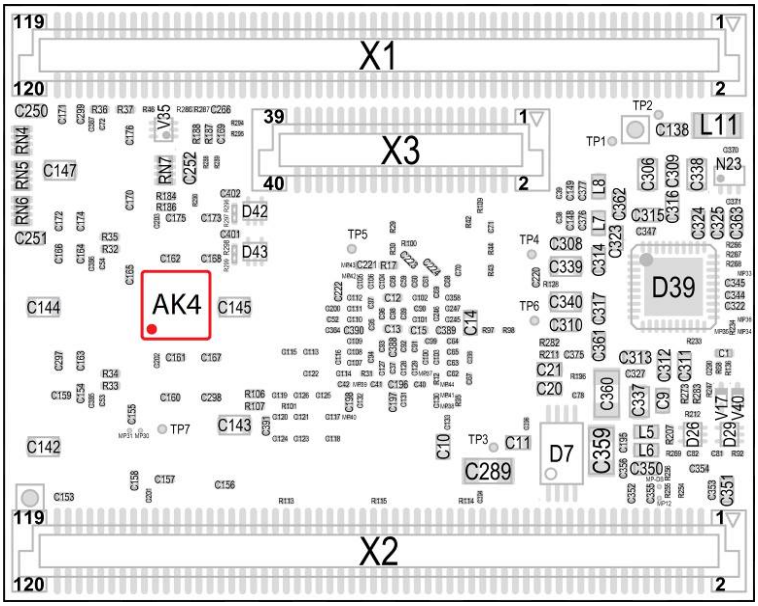


Illustration 17: TQMLS102xA assembly, bottom

The labels on the TQMLS102xA show the following information:

Table 13: Labels on TQMLS102xA

Label	Text
AK1	Serial number
AK2	MAC address
AK3	TQMLS102xA version and revision
AK4	Tests performed

5. MECHANICS

5.1 Dimensions

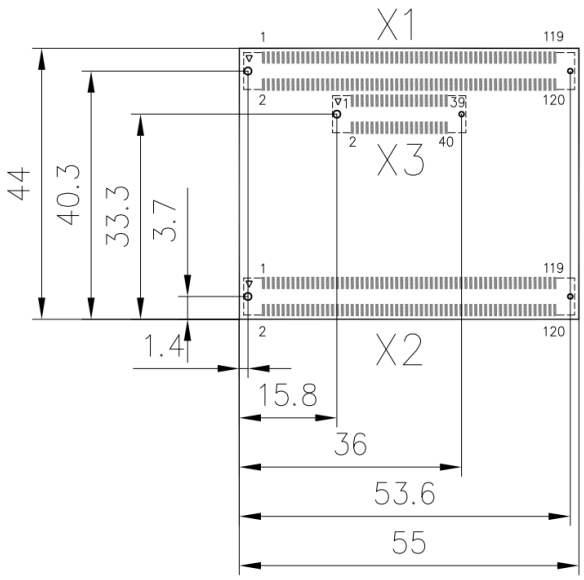


Illustration 18: TQMLS102xA dimensions, top view **through** TQMLS102xA

5.2 TQMLS102xA images

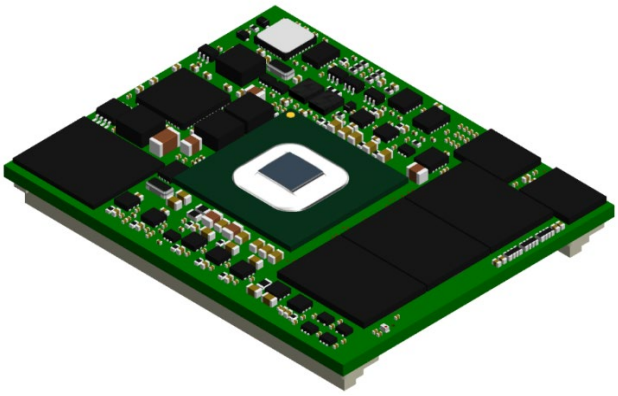


Illustration 19: TQMLS102xA, 3D, top view

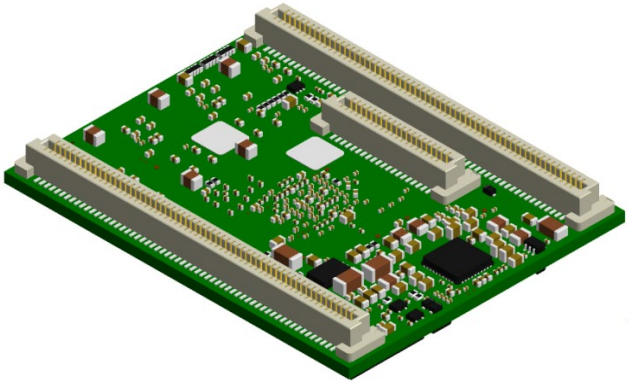


Illustration 20: TQMLS102xA, 3D, bottom view

5.3 Connectors

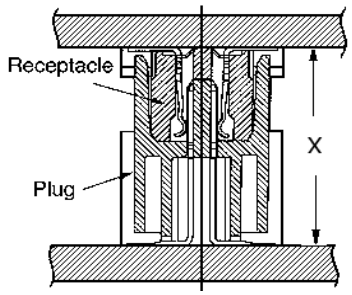
The TQMLS102xA is connected to the carrier board with 280 pins on three connectors.
The following table shows details of the connectors used.

Table 14: TQMLS102xA connectors

Manufacturer	Part number	Remark
TE connectivity	40-pin: 5177985-1 120-pin: 5177985-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMLS102xA is held in the mating connectors with a retention force of approximately 28 N.
To avoid damaging the TQMLS102xA connectors as well as the carrier board connectors while removing the TQMLS102xA the use of an extraction tool is strongly recommended. See chapter 5.8 for further information.
The following table shows suitable carrier board mating connectors.

Table 15: Carrier board mating connectors

Manufacturer	Part number	Remark	Stack height (X)	
TE connectivity	40-pin: 5177986-1 120-pin: 5177986-5	On MBLS102xA	5 mm	
	40-pin: 1-5177986-1 120-pin: 1-5177986-5	–	6 mm	
	40-pin: 2-5177986-1 120-pin: 2-5177986-5	–	7 mm	
	40-pin: 3-5177986-1 120-pin: 3-5177986-5	–	8 mm	

5.4 Adaptation to the environment

The TQMLS102xA overall dimensions (length × width) are 55 × 44 mm².
The LS102xA CPU on the TQMLS102xA has a maximum height of approximately 8.6 mm above the MBLS102xA.
A STEP model of the TQMLS102xA can be provided on request. Please contact TQ-Support.

5.5 Protection against external effects

As an embedded module, the TQMLS102xA is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.6 Thermal management

To cool the TQMLS102xA, a theoretical maximum of approximately 4 W have to be dissipated.
The power dissipation originates primarily in the LS102xA and the DDR3L SDRAM.
The power dissipation also depends on the software used and can vary according to the application.

Attention: Destruction or malfunction, TQMLS102xA heat dissipation	
	The TQMLS102xA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LS102xA must be taken into consideration when connecting the heat sink, see (4). The LS102xA is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMLS102xA and thus malfunction, deterioration or destruction.

5.7 Structural requirements

The TQMLS102xA is held in the mating connectors by the retention force of the pins (a total of 280). For high requirements with respect to vibration and shock firmness an additional retainer has to be provided in the final product to hold the TQMLS102xA in its position. As no heavy and big components are used, no further requirements are given.

5.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMLS102xA may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

Attention: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMLS102xA for the extraction tool MOZI8XXL.

5.9 Shock and Vibration

Table 16: Shock resistance

Parameter	Details
Shocks	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	18 ms
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 17: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 – 9 Hz, 9 – 200 Hz, 200 – 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X-Y-Z axis
Number of frequency cycles	20 frequency cycles
Amplitude	2 Hz … 9 Hz: 3.5 ms^{-2} 9 Hz … 200 Hz: 10 ms^{-2} 200 Hz … 500 Hz: 15 ms^{-2}

The values shown are based on the guidelines of standard DIN ETS 300019 (Environmental tests for telecommunications equipment).

6. SOFTWARE

The TQMLS102xA is delivered with a preinstalled boot loader and a BSP provided by TQ-Systems GmbH, which is configured for the Starterkit MBLS102xA.
The boot loader provides TQMLS102xA-specific as well as board-specific settings, e.g.:

- LS102xA configuration
- PMIC configuration
- DDR3L SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

More information can be found in the Support Wiki for the TQMLS102xA.

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMLS102xA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
The following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board.
- A sufficient number of blocking capacitors in all supply voltages.
- Fast or permanently clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and / or shielding. Take note of not only the frequency, but also the signal rise times.
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly).

Since the TQMLS102xA is plugged on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMLS102xA.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering / Zener diode(s)
- Fast signals: Integrated protective devices (e.g., suppressor diode arrays)

7.3 Operational safety and personal security

Due to the occurring voltages (≤3.3 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly. In general, a reliable operation is given when following conditions are met:

Table 18: Climate and operational conditions

Parameter	Range	Remark
Environment temperature	–40 °C to +85 °C	–
Storage temperature	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the CPUs' thermal characteristics is to be taken from the NXP QorIQ LS1021A Reference Manual (1).

Attention: Destruction or malfunction, TQMLS102xA heat dissipation	
	The TQMLS102xA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LS102xA must be taken into consideration when connecting the heat sink, see (4). The LS102xA is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMLS102xA and thus malfunction, deterioration or destruction.

7.5 Reliability and service life

No detailed MTBF calculation has been done for the TQMLS102xA.

The TQMLS102xA is designed to be insensitive to shock and vibration.

High quality industrial grade connectors are assembled on the TQMLS102xA.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The TQMLS102xA is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMLS102xA was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Eco-design Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMLS102xA must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the TQMLS102xA enable compliance with EuP requirements for the TQMLS102xA.

8.5 Battery

No batteries are assembled on the TQMLS102xA.

8.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMLS102xA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMLS102xA is delivered in reusable packaging.

8.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 19: Acronyms

Acronym	Meaning
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIN	German industry standard (Deutsche Industrienorm)
EC	European Community
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	European standard (Europäische Norm)
ESD	Electrostatic Discharge
eSDHC	enhanced Secure Digital High Capacity
ETS	European Telecommunications Standards
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
I/O	Input/ Output
I^2C	Inter-Integrated Circuit
IFC	Integrated Flash-Controller
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LPM	Low Power Mode
MOZI	Modulzieher (Module extractor)
MTBF	Mean operating Time Between Failures
NC	Not Connected
NOR	Not-Or
PC	Personal Computer
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PMC	Power Management Controller
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
QSPI	Quad Serial Peripheral Interface
RC	Resistor-Capacitor
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SD card	Secure Digital Card
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer/Deserializer
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment

9.2 References

Table 20: Further applicable documents

No.:	Name	Rev., Date	Company
(1)	QorIQ LS1021A Reference Manual	Rev. D, 09/2014	NXP
(2)	PMIC 34VR500	Rev. 3.0, 1/2015	NXP
(3)	PMC MKL04Z16	Rev. 3.1, Nov. 2012	NXP
(4)	AN4871, Application Note Assembly Handling for Lidless FCBGA Packages	Rev. 0, 02/2014	NXP
(5)	MBLS102xA User's Manual	– current –	TQ-Systems
(6)	TQMLS102xA Support-Wiki	– current –	TQ-Systems
(7)	TQMLS102xA Design Checklist	– current –	TQ-Systems

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