TQMLS1028A
User's Manual

TQMLS1028A UM 0101
28.11.2020

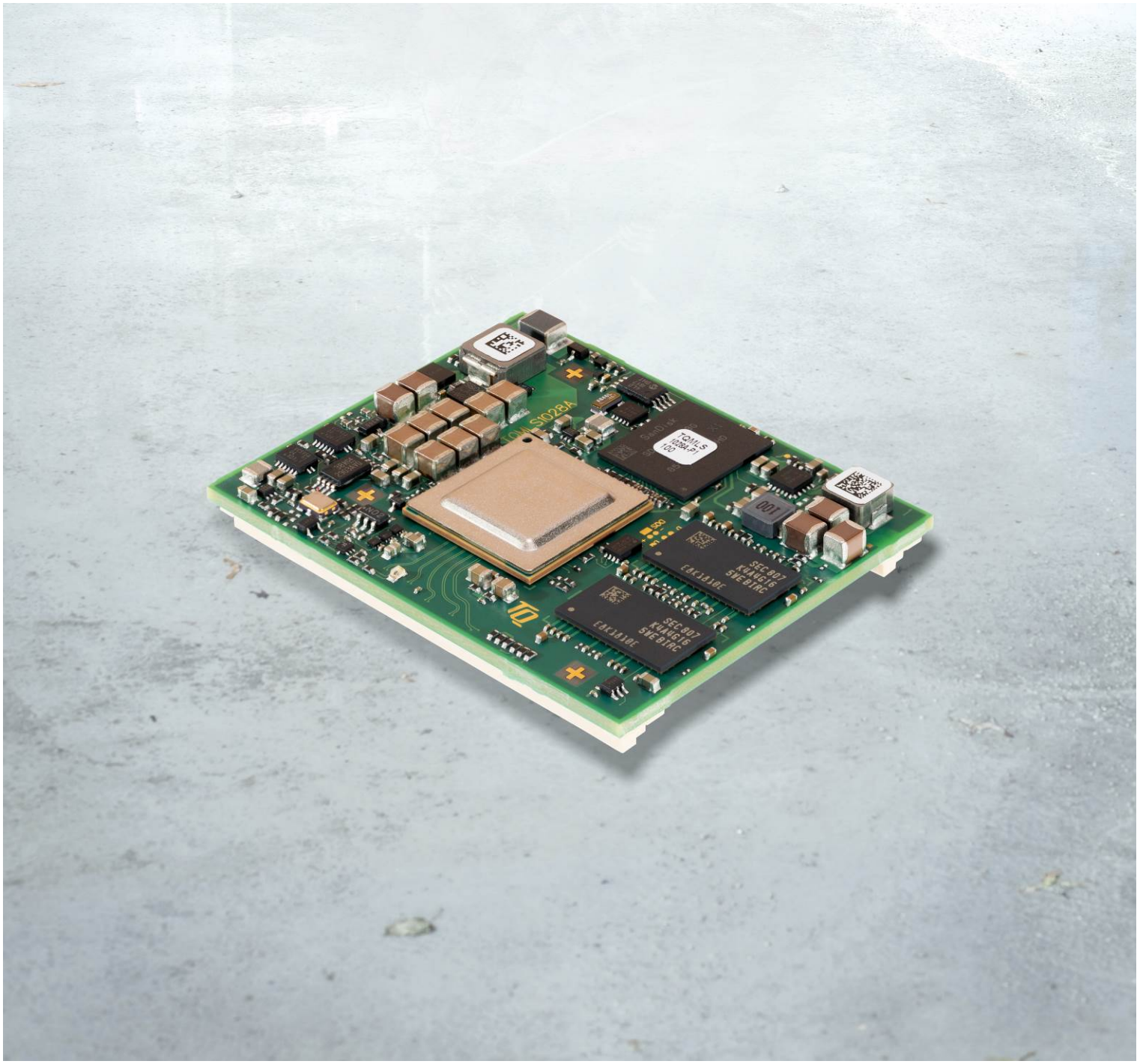

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TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	24.06.2020	Petz		First edition
0101	28.11.2020	Petz	All Table 3 4.2.3 4.3.3 4.15.1, Figure 12 Table 13 5.3, Figure 18 and 19	Non-functional changes Remarks added Explanation added Description of RCW clarified Added Signals “Secure Element” added 3D views removed

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMLS1028A and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.

The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLS1028A circuit diagram
- MBLS1028A User's Manual
- LS1028A Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMLS1028A

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMLS1028A revision 02xx, and refers to some software settings.
Differences to TQMLS1028A revision 01xx are noted, when applicable.
A certain TQMLS1028A derivative does not necessarily provide all features described in this User's Manual.
This User's Manual does also not replace the NXP CPU Reference Manuals.
The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMLS1028A, and the BSP provided by TQ-Systems GmbH. See also chapter 6.
The TQMLS1028A is a universal Minimodule based on the NXP Layerscape CPUs LS1028A / LS1018A / LS1027A / LS1017A.
These Layerscape CPUs feature a Single, or a Dual Cortex®-A72 core, with QorIQ technology.
The TQMLS1028A extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
A suitable CPU derivative (LS1028A / LS1018A / LS1027A / LS1017A) can be selected for each requirement.
All essential CPU pins are routed to the TQMLS1028A connectors.
There are therefore no restrictions for customers using the TQMLS1028A with respect to an integrated customised design.
Furthermore all components required for the correct CPU operation, like DDR4 SDRAM, eMMC, power supply and power management are integrated on the TQMLS1028A. The main TQMLS1028A characteristics are:

- CPU derivatives LS1028A / LS1018A / LS1027A / LS1017A
- DDR4 SDRAM, ECC as an assembly option
- eMMC NAND Flash
- QSPI NOR Flash
- Single supply voltage 5 V
- RTC / EEPROM / temperature sensor

The MBLS1028A also serves as carrier board and reference platform for the TQMLS1028A.

3. OVERVIEW

3.1 Block diagram

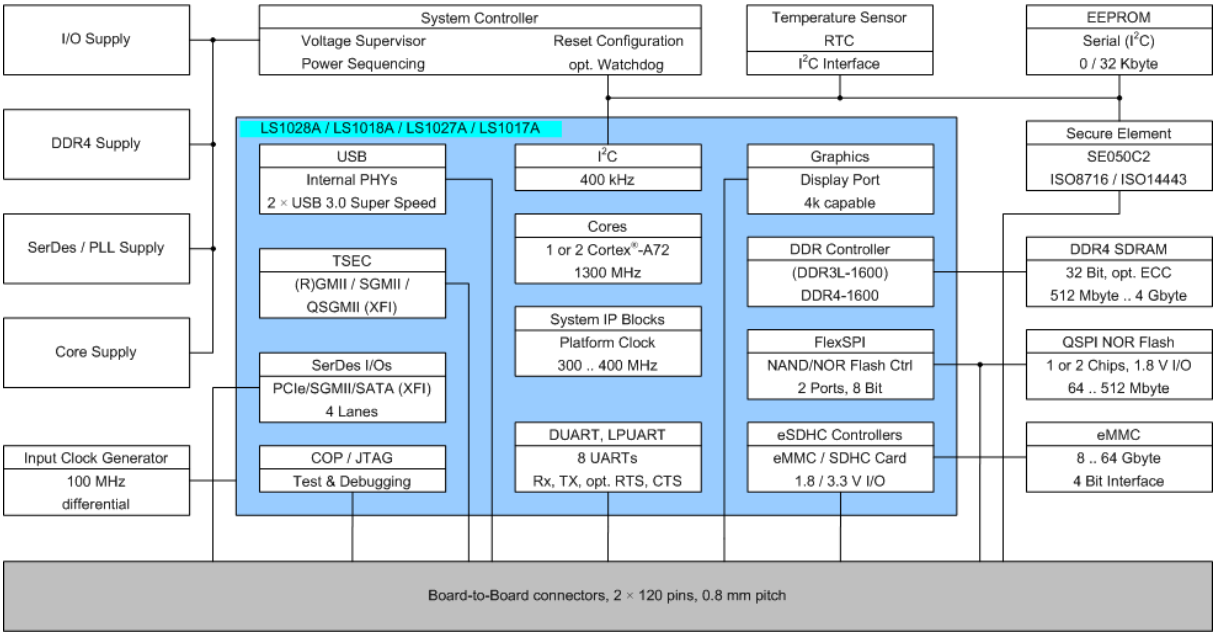


Figure 1: Block diagram TQMLS1028A (simplified)

3.2 System components

The TQMLS1028A provides the following key functions and characteristics:

- Layerscape CPU LS1028A or pin compatible, see 4.1
- DDR4 SDRAM with ECC (ECC is an assembly option)
- QSPI NOR Flash (assembly option)
- eMMC NAND Flash
- Oscillators
- Reset structure, Supervisor and Power Management
- System Controller for Reset-Configuration and Power Management
- Voltage regulators for all voltages used on the TQMLS1028A
- Voltage supervision
- Temperature sensors
- Secure Element SE050 (assembly option)
- RTC
- EEPROM
- Boar-to-Board connectors

All essential CPU pins are routed to the TQMLS1028A connectors. There are therefore no restrictions for customers using the TQMLS1028A with respect to an integrated customised design. The functionality of the different TQMLS1028A is mainly determined by the features provided by the respective CPU derivative.

4. ELECTRONICS

4.1 LS1028A

4.1.1 LS1028A variants, block diagrams

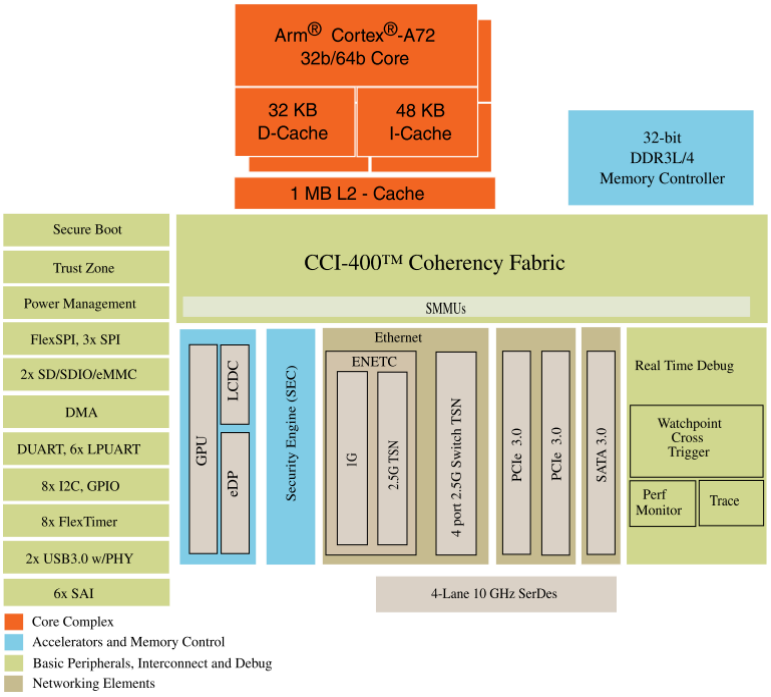


Figure 2: Block diagram LS1028A
(Source: NXP)

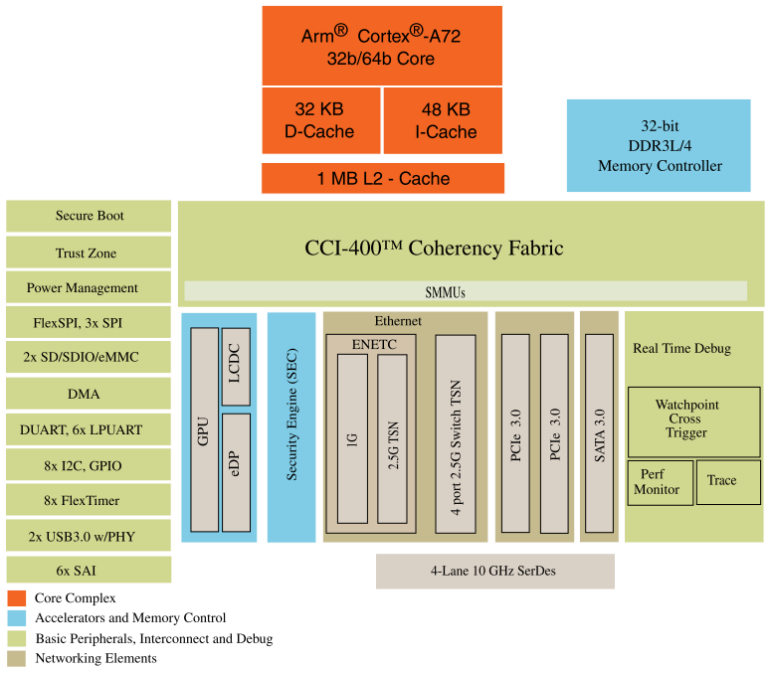


Figure 3: Block diagram LS1018A
(Source: NXP)

4.1.1 LS1028A variants, block diagrams (continued)

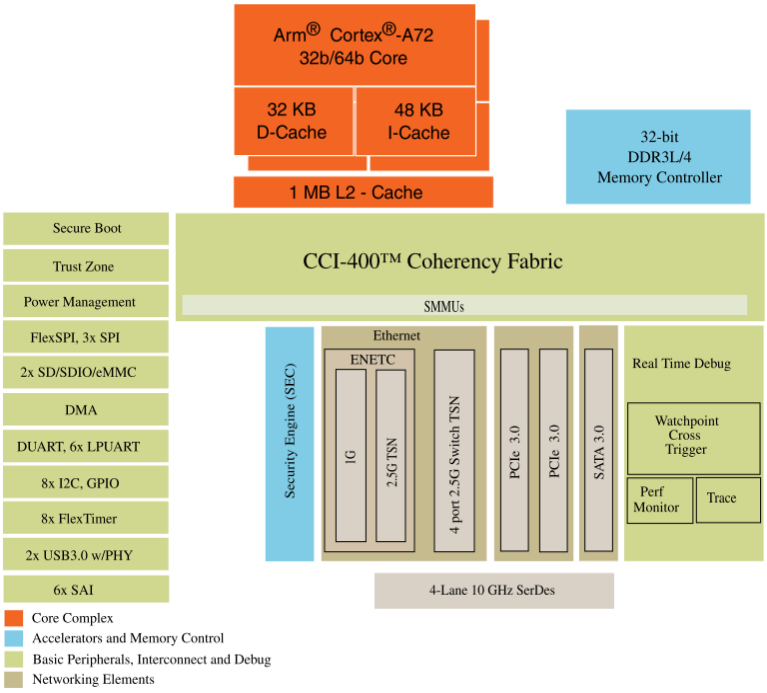


Figure 4: Block diagram LS1027A
(Source: NXP)

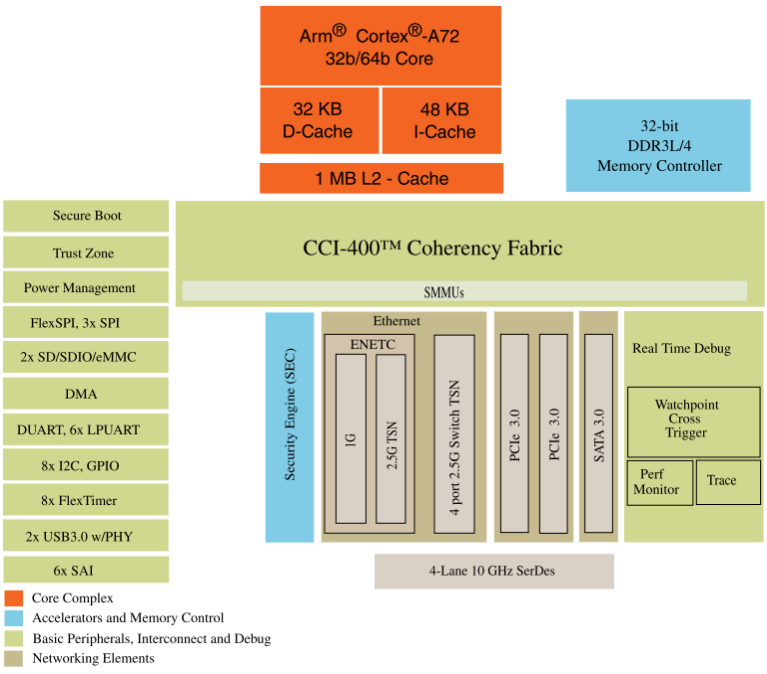


Figure 5: Block diagram LS1017A
(Source: NXP)

4.1.2 LS1028A variants, details

The following table shows the features provided by the different variants.
Fields with a red background indicate differences; fields with a green background indicate compatibility.

Table 2: LS1028A variants

Feature	LS1028A	LS1027A	LS1018A	LS1017A
ARM® core	2 × Cortex®-A72	2 × Cortex®-A72	1 × Cortex®-A72	1 × Cortex®-A72
SDRAM	32-bit, DDR4 + ECC	32-bit, DDR4 + ECC	32-bit, DDR4 + ECC	32-bit, DDR4 + ECC
GPU	1 × GC7000UltraLite	–	1 × GC7000UltraLite	–
Ethernet	4 × 2.5 G/1 G switched Eth (TSN enabled) 1 × 2.5 G/1 G Eth (TSN enabled) 1 × 1 G Eth	4 × 2.5 G/1 G switched Eth (TSN enabled) 1 × 2.5 G/1 G Eth (TSN enabled) 1 × 1 G Eth	4 × 2.5 G/1 G switched Eth (TSN enabled) 1 × 2.5 G/1 G Eth (TSN enabled) 1 × 1 G Eth	4 × 2.5 G/1 G switched Eth (TSN enabled) 1 × 2.5 G/1 G Eth (TSN enabled) 1 × 1 G Eth
PCIe	2 × Gen 3.0 Controllers (RC or RP)	2 × Gen 3.0 Controllers (RC or RP)	2 × Gen 3.0 Controllers (RC or RP)	2 × Gen 3.0 Controllers (RC or RP)
USB	2 × USB 3.0 with PHY (Host or Device)	2 × USB 3.0 with PHY (Host or Device)	2 × USB 3.0 with PHY (Host or Device)	2 × USB 3.0 with PHY (Host or Device)

4.2 Reset Logic and Supervisor

The reset logic contains the following functions:

- Voltage monitoring on the TQMLS1028A
- External reset input
- PGOOD output for power-up of circuits on the carrier board, e.g., PHYs
- Reset LED (Function: PORESET# low: LED lights up)

Table 3: TQMLS1028A Reset- and Status signals

Signal	TQMLS1028A	Dir.	Level	Remark
PORESET#	X2-93	O	1.8 V	PORESET# also triggers RESET_OUT# (TQMLS1028A revision 01xx) or RESET_REQ_OUT# (TQMLS1028A revision 02xx)
HRESET#	X2-95	I/O	1.8 V	–
TRST#	X2-100	I/O_{OC}	1.8 V	–
PGOOD	X1-14	O	3.3 V	Enable signal for supplies and drivers on carrier board
RESIN#	X1-17	I	3.3 V	–
RESET_REQ#	X2-97	O	1.8 V	TQMLS1028A revision 01xx
RESET_REQ_OUT#		O	3.3 V	TQMLS1028A revision 02xx

4.2.1 JTAG-Reset TRST#

TRST# is coupled to PORESET#, as shown in the following Figure. See also NXP QorIQ LS1028A Design Checklist (5).

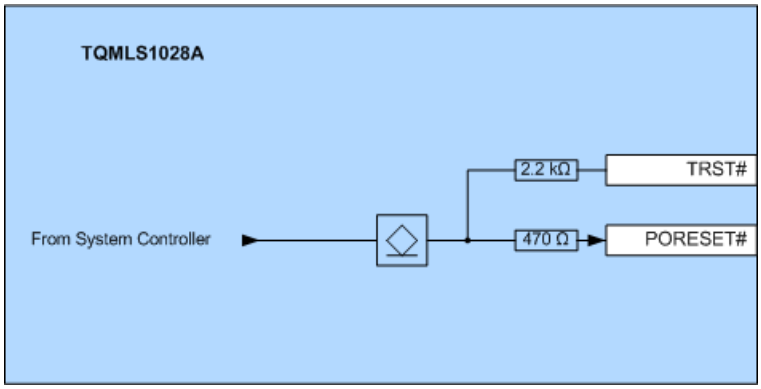


Figure 6: Block diagram TRST#

4.2.2 Self-Reset on TQMLS1028A revision 01xx

The following block diagram shows the RESET_REQ# / RESIN# wiring of the TQMLS1028A revision 01xx.

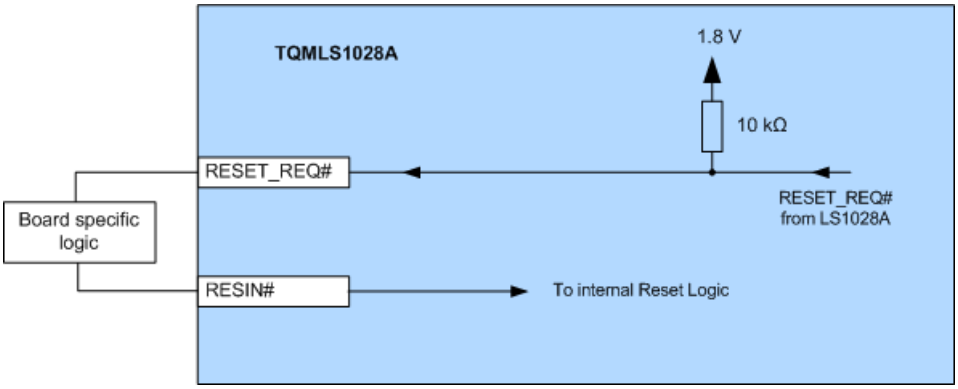


Figure 7: Block diagram RESET_REQ# / RESIN# TQMLS1028A revision 01xx

4.2.3 Self-Reset on TQMLS1028A revision 02xx

The LS1028A can initiate or request a hardware reset via software.
The output HRESET_REQ# is driven internally by the CPU and can be set by software by writing to RSTCR register (bit 30).
By default, RESET_REQ# is fed back via 10 kΩ to RESIN# on the TQMLS1028A. No feedback on the carrier board is required. This leads to a self reset when RESET_REQ# is set.
Depending on the design of the feedback on the carrier board, it can "overwrite" the TQMLS1028A internal feedback and thus, if RESET_REQ# is active, can optionally

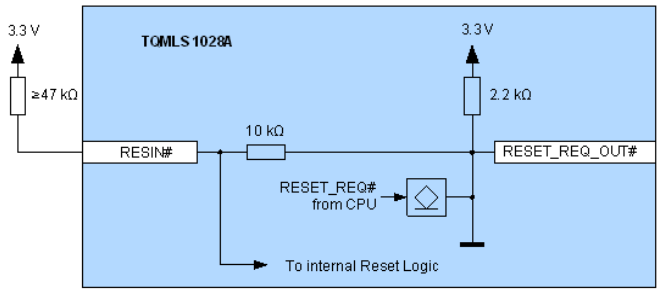
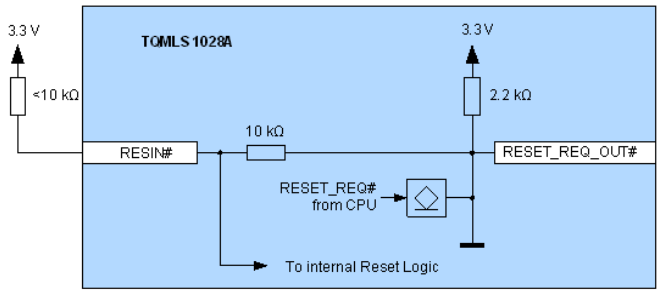
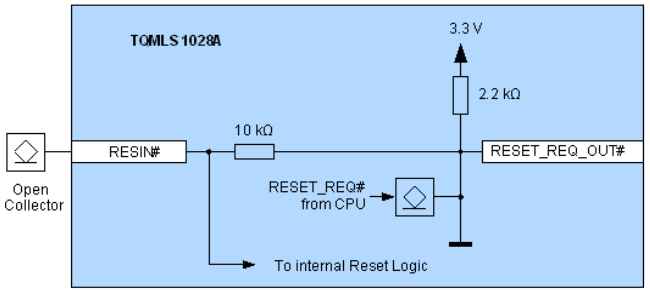
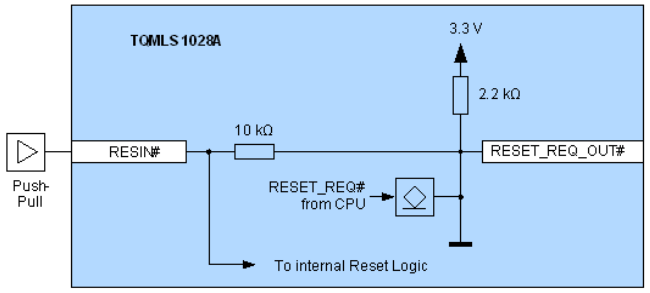
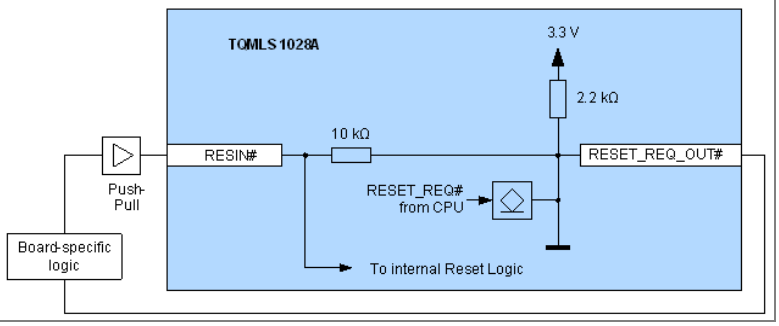
- trigger a reset
- not trigger a reset
- trigger further actions on the base board in addition to the reset

RESET_REQ# is indirectly routed as signal RESET_REQ_OUT# to the connector (see Table 4).
"Devices" that can trigger a RESET_REQ# see TQMLS1028A Reference Manual (3), section 4.8.3.

4.2.3 Self-Reset on TQMLS1028A revision 02xx (continued)

The following wirings show different possibilities to connect RESIN#.

Table 4: RESIN# connection

Self-Reset performed when RESET_REQ# asserted by CPU.	
No Self-Reset performed when RESET_REQ# asserted by CPU.	
Self-Reset performed when RESET_REQ# asserted by CPU, external reset signal connected to RESIN#.	
No Self-Reset performed when RESET_REQ# asserted by CPU, external reset signal connected to RESIN#.	
Self-Reset via external reset signal using additional logic.	

4.3 LS1028A Configuration

4.3.1 RCW Source

The RCW source of the TQMLS1028A is determined by the level of the analogue 3.3 V signal RCW_SRC_SEL.
The RCW source selection is managed by the system controller. A 10 kΩ Pull-Up to 3.3 V is assembled on the TQMLS1028A.

Table 5: Signal RCW_SRC_SEL

RCW_SRC_SEL (3.3 V)	Reset Configuration Source	PD on carrier board
3.3 V (80 % to 100 %)	SD card, on carrier board	None (open)
2.33 V (60 % to 80 %)	eMMC, on TQMLS1028A	24 kΩ PD
1.65 V (40 % to 60 %)	SPI NOR flash, on TQMLS1028A	10 kΩ PD
1.05 V (20 % to 40 %)	Hard Coded RCW, on TQMLS1028A	4.3 kΩ PD
0 V (0 % to 20 %)	I²C EEPROM on TQMLS1028A, address 0x50 / 101 0000b	0 Ω PD

4.3.2 Configuration signals

The LS1028A CPU is configured via pins as well as via registers.

Table 6: Reset Configuration Signals

Reset cfg. name	Functional signal name	Default	On TQMLS1028A	Variable [1]
cfg_rcw_src[0:3]	ASLEEP, CLK_OUT, UART1_SOUT, UART2_SOUT	1111	Several	Yes
cfg_svr_src[0:1]	XSPI1_A_CS0_B, XSPI1_A_CS1_B	11	11	No
cfg_dram_type	EMI1_MDC	1	0 = DDR4	No
cfg_eng_use0	XSPI1_A_SCK	1	1	No
cfg_gpinput[0:3]	SDHC1_DAT[0:3], I/O voltage 1.8 or 3.3 V	1111	Not driven, internal PUs	–
cfg_gpinput[4:7]	XSPI1_B_DATA[0:3]	1111	Not driven, internal PUs	–

The following table shows the coding of the field cfg_rcw_src:

Table 7: Reset Configuration Source

cfg_rcw_src[3:0]	RCW source
0xxx	Hard-coded RCW (TBD)
1000	SDHC1 (SD card)
1001	SDHC2 (eMMC)
1010	I2C1 extended addressing [2]
1011	(Reserved)
1100	XSPI1A NAND 2 KB pages
1101	XSPI1A NAND 4 KB pages
1110	(Reserved)
1111	XSPI1A NOR

Green Standard configuration
Yellow Configuration for development and debugging

1: Yes ⇨ via shift register; No ⇨ fixed value.
2: Device address 0x50 / 101 0000b = Configuration EEPROM.

4.3.3 Reset Configuration Word

The RCW structure (Reset Configuration Word) can be found in the NXP LS1028A Reference Manual (3).
The Reset Configuration Word (RCW) is transferred to the LS1028A as memory structure.
It has the same format as the Pre-Boot Loader (PBL). It has a start identifier and a CRC.
The Reset Configuration Word contains 1024 bits (128 bytes user data (memory image))

+ 4 bytes preamble
+ 4 bytes address
+ 8 bytes end command incl. CRC
= 144 bytes

NXP offers a free tool (registration required) "QorIQ Configuration and Validation Suite 4.2" with which the RCW can be created.

Note: Adaption of RCW	
	The RCW must be adapted to the actual application. This applies, for example, to SerDes configuration and I/O multiplexing. For the MBLS1028A there are three RCWs according to the selected boot source: - rcw_1300_emmc.bin - rcw_1300_sd.bin - rcw_1300_spi_nor.bin

4.3.4 Settings via Pre-Boot-Loader PBL

In addition to the Reset Configuration Word, the PBL offers a further possibility to configure the LS1028A without any additional software. The PBL uses the same data structure as the RCW or extends it. For details see (3), Table 19.

4.3.5 Error handling during RCW loading

If an error occurs while loading the RCW or the PBL, the LS1028A proceeds as follows, see (3), Table 12:
Halt the Reset Sequence on RCW Error Detection.
If the Service Processor reports an error during its process of loading the RCW data, the following occurs:

- The device reset sequence is halted, remaining in this state.
- An error code is reported by the SP in RCW_COMPLETION[ERR_CODE].
- A request for a reset of the SoC is captured in RSTRQSR1[SP_RR], which generates a reset request if not masked by RSTRQMR1[SP_MSK].

This state can only be exited with a PORESET_B or Hard Reset.

4.4 System Controller

The TQMLS1028A uses a system controller for housekeeping and initialization functions. This system controller also performs power sequencing and voltage monitoring.
The functions are in detail:

- Correctly timed output of the reset configuration signal cfg_rcw_src[0:3]
- - Input for cfg_rcw_src selection, analogue level to encode five states (see Table 7):
  1. SD card
  2. eMMC
  3. NOR Flash
  4. Hard-coded
  5. I²C

- Power Sequencing: Control of power-up sequence of all module-internal supply voltages
- Voltage supervision: Monitoring of all supply voltages (assembly option)

4.5 System Clock

The system clock is permanently set to 100 MHz. Spread spectrum clocking is not possible.

4.6 SDRAM

1, 2, 4 or 8 GB of DDR4-1600 SDRAM can be assembled on the TQMLS1028A.

4.7 Flash

Assembled on TQMLS1028A:

- QSPI NOR Flash
- eMMC NAND Flash, Configuration as SLC is possible (higher reliability, half capacity)
  Please contact TQ-Support for more details.

External storage device:

- SD card (on MBLS1028A)

4.7.1 QSPI NOR Flash

The TQMLS1028A supports three different configurations, see following Figure.

1. Quad SPI on Pos. 1 or Pos. 1 and 2, Data on DAT[3:0], separate chip selects, common clock
2. Octal SPI on pos. 1 or pos. 1 and 2, Data on DAT[7:0], separate chip selects, common clock
3. Twin-Quad SPI on pos. 1, Data on DAT[3:0] and DAT[7:4], separate chip selects, common clock

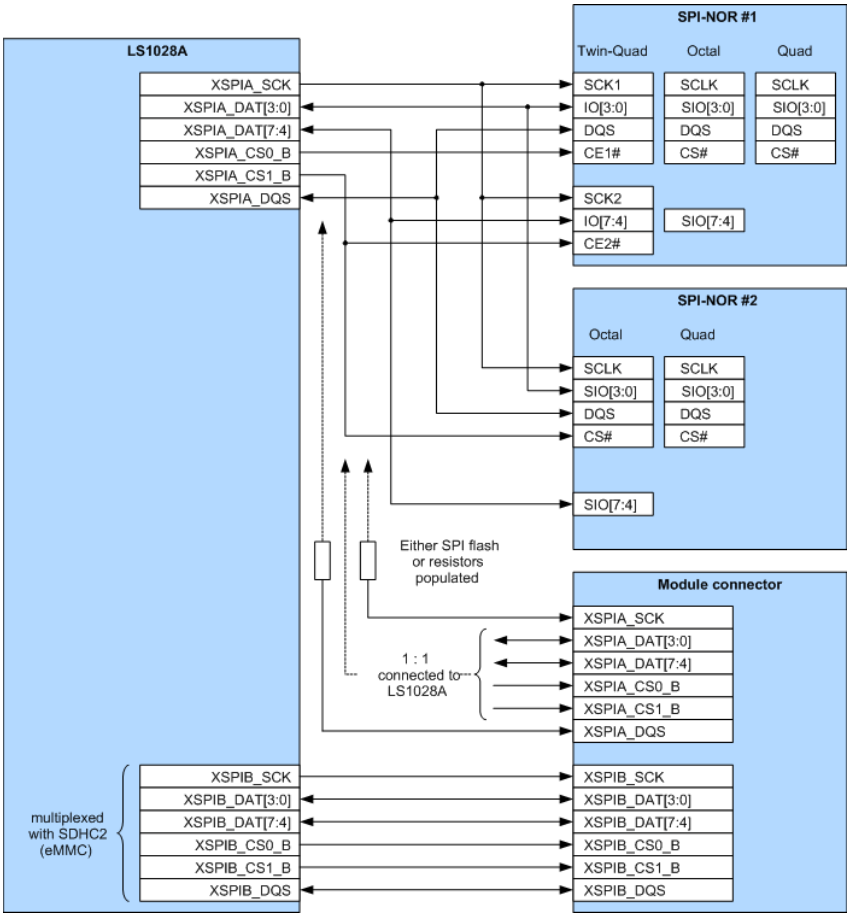


Figure 8: Block diagram QSPI interface

4.7.2 eMMC / SD card

The LS1028A provides two SDHCs; one is for SD cards (with switchable I/O voltage) and the other is for the internal eMMC (fixed I/O voltage). When populated, the TQMLS1028A internal eMMC is connected to SDHC2. The maximum transfer rate corresponds to the HS400 mode (eMMC from 5.0). In case the eMMC is not populated, an external eMMC can be connected.

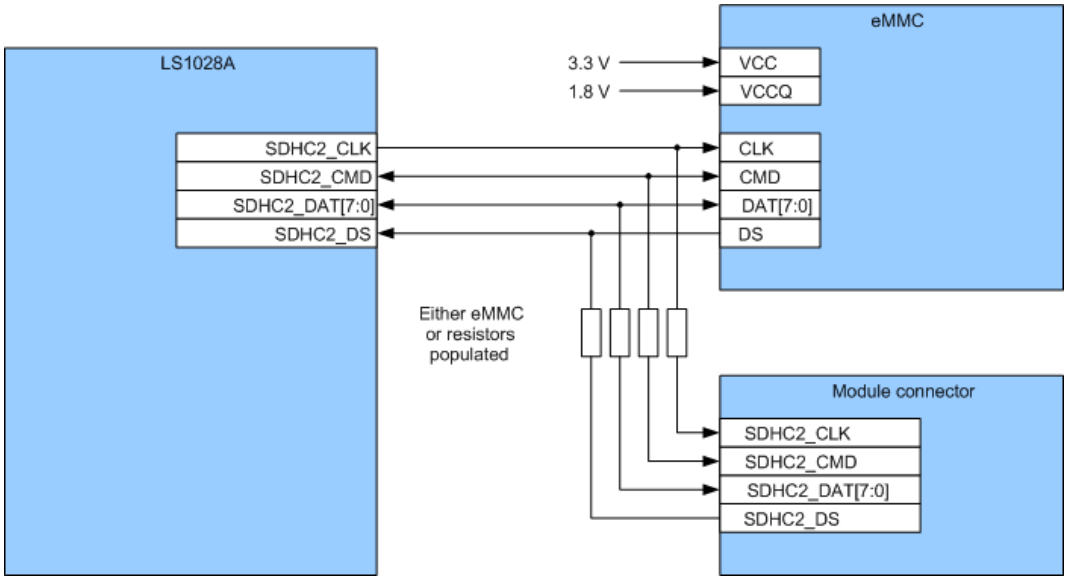


Figure 9: Block diagram eMMC interface

4.8 EEPROM

4.8.1 Data EEPROM 24LC256T

The EEPROM is empty on delivery.

- 256 Kbit or not assembled
- 3 decoded address lines
- Connected to I²C controller 1 of the LS1028A
- 400 kHz I²C clock
- Device address is `0x57 / 101 0111b`

4.8.2 Configuration EEPROM SE97B

The temperature sensor SE97BTP also contains a 2 Kbit (256 × 8 Bit) EEPROM. The EEPROM is divided into two parts.
The lower 128 bytes (address 00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. The upper 128 bytes (address 80h to FFh) are not write protected and can be used for general purpose data storage.

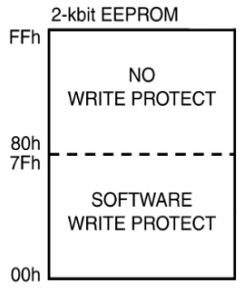


Figure 10: Memory Map SE97BTP EEPROM

The EEPROM can be accessed with the following two I²C addresses.

- EEPROM (Normal Mode): `0x50 / 101 0000b`
- EEPROM (Protected Mode): `0x30 / 011 0000b`

The configuration EEPROM contains a standard reset configuration at delivery.
The following table lists the parameters stored in the configuration EEPROM.

Table 8: EEPROM, TQMLS1028A-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	–	$32_{(10)}$	$32_{(10)}$	Binary	(Not used)
0x20	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
0x30	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x40	Variable	Variable	$64_{(10)}$	ASCII	Order code

The configuration EEPROM is only one of several options for storing the reset configuration.
By means of the standard reset configuration in the EEPROM, a correctly configured system can always be achieved by simply changing the Reset Configuration Source.
If the Reset Configuration Source is selected accordingly, 4 + 4 + 64 + 8 bytes = 80 bytes are required for the reset configuration. It can also be used for the Pre-Boot Loader PBL.

4.9 RTC

The RTC PCF85063ATL is supported by U-Boot and Linux kernel.
The RTC is powered via V_{IN}, battery buffering is possible (battery on carrier board, see Figure 11).
The alarm output INTA# is routed to the module connectors. A wake-up is possible via the system controller.
The RTC is connected to the I²C controller 1, device address is `0x51 / 101 0001b`.
The accuracy of the RTC is primarily determined by the characteristics of the quartz used. The type FC-135 used on the TQMLS1028A has a standard frequency tolerance of ±20 ppm at +25 °C. (Parabolic coefficient: max. -0.04×10^{-6} / °C²)
This results in an accuracy of approximately 2.6 seconds / day = 16 minutes / year.

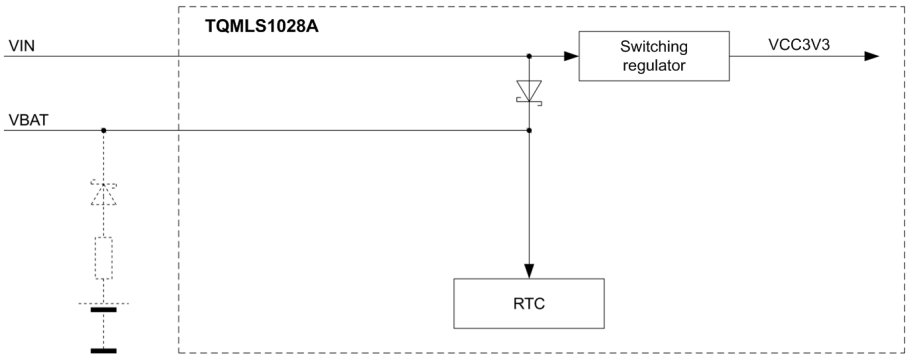


Figure 11: Block diagram RTC buffering

4.10 Temperature monitoring

Due to the high power dissipation, temperature monitoring is absolutely necessary in order to comply with the specified operating conditions and thus ensure reliable operation of the TQMLS1028A. The temperature critical components are:

- LS1028A
- DDR4 SDRAM

The following measuring points exist:

- LS1028A temperature:
  Measured via diode integrated in LS1028A, read out via external channel of SA56004
- DDR4 SDRAM:
  Measured by temperature sensor SE97B
- 3.3 V switching regulator:
  SA56004 (internal channel) to measure the 3.3 V switching regulator temperature

The open-drain Alarm Outputs (open drain) are connected and have a Pull-Up to signal TEMP_OS#.
Control via I²C controller I2C1 of the LS1028A, device addresses see Table 11.
Further details can be found in the SA56004EDP data sheet (6).
An additional temperature sensor is integrated in the configuration EEPROM, see 4.8.2.

4.11 TQMLS1028A Supply

The TQMLS1028A requires a single supply of 5 V ±10 % (4.5 V to 5.5 V).

4.12 Power consumption TQMLS1028A

The power consumption of the TQMLS1028A strongly depends on the application, the mode of operation and the operating system. For this reason the given values have to be seen as approximate values.

Current peaks of 3.5 A may occur. The carrier board power supply should be designed for a TDP of 13.5 W.

The following table shows power consumption parameters of the TQMLS1028A measured at +25 °C.

Table 9: TQMLS1028A power consumption

Mode of operation	Current @ 5 V	Power @ 5 V	Remark
RESET	0.46 A	2.3 W	Reset button on MBLS1028A pressed
U-Boot idle	1.012 A	5.06 W	–
Linux idle	1.02 A	5.1 W	–
Linux 100 % load	1.21 A	6.05 W	Stress test [3]

4.13 Power consumption RTC

Table 10: RTC power consumption

Mode of operation	Min.	Typ.	Max.
V_{BAT}, I²C RTC PCF85063A active	1.8 V	3 V	4.5 V
I_{BAT}, I²C RTC PCF85063A active	–	18 µA	50 µA
V_{BAT}, I²C RTC PCF85063A inactive	0.9 V	3 V	4.5 V
I_{BAT}, I²C RTC PCF85063A inactive	–	220 nA	600 nA

4.14 Voltage monitoring

The permitted voltage ranges are given by the data sheet of the respective component and, if applicable, the voltage monitoring tolerance. Voltage monitoring is an assembly option.

4.15 Interfaces to other systems and devices

4.15.1 Secure Element SE050

A Secure Element SE050 is available as assembly option.

All six signals of ISO_14443 (NFC Antenna) and ISO_7816 (Sensor Interface) provided by the SE050 are available.

The ISO_14443 and ISO_7816 signals of the SE050 are multiplexed with the SPI bus and JTAG signal TBSCAN_EN#, see Table 13.

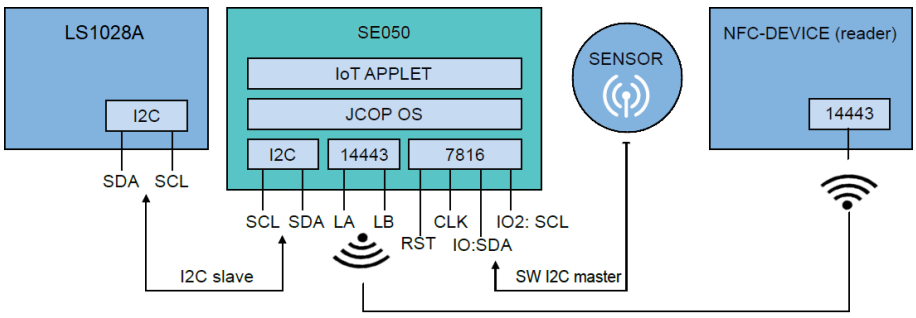


Figure 12: Block diagram SE050
(Source: NXP)

➢ The I2C address of the Secure Element is `0x48 / 100 1000b`.

3: stressapptest -M 512 -m 8 -C 8 -W -s 54000 --printsec 5

4.15.2 I²C bus

All six I²C buses of the LS1028A (I2C1 to I2C6) are routed to the TQMLS1028A connectors and not terminated.
The I2C1 bus is level shifted to 3.3 V and terminated with 4.7 kΩ Pull-Ups to 3.3 V on the TQMLS1028A.
The I²C devices on the TQMLS1028A are connected to the level-shifted I2C1 bus. More devices can be connected to the bus, but additional external Pull-Ups may be necessary on account of the relatively high capacitive load.

Table 11: I2C1 device addresses

Device	Function	7-bit address	Remark
24LC256	EEPROM	0x57 / 101 0111b	For general usage
MKL04Z16	System Controller	0x11 / 001 0001b	Should not be altered
PCF85063A	RTC	0x51 / 101 0001b	–
SA560004EDP	Temperature sensor	0x4C / 100 1100b	–
SE97BTP	Temperature sensor	0x18 / 001 1000b	Temperature
	EEPROM	0x50 / 101 0000b	Normal Mode
	EEPROM	0x30 / 011 0000b	Protected Mode
SE050C2	Secure Element	0x48 / 100 1000b	Only on TQMLS1028A revision 02xx

4.15.3 UART

Two UART interfaces are configured in the BSP provided by TQ-Systems and directly routed to the TQMLS1028A connectors.
More UARTs are available with an adapted pin multiplexing.

4.15.4 JTAG®

The MBLS1082A provides a 20-pin header with standard JTAG® signals.
Alternatively the LS1028A can be addressed via OpenSDA.

4.16 TQMLS1028A interfaces

4.16.1 Pin multiplexing

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The pin assignment in Table 12 and Table 13 refers to the BSP provided by TQ-Systems in combination with the MBLS1028A.

Attention: Destruction or malfunction	
	Depending on the configuration many LS1028A pins can provide several different functions. Please take note of the information concerning the configuration of these pins in (1), before integration or start-up of your carrier board / Starterkit.

4.16.2 Pinout TQMLS1028A connectors

Table 12: Pinout connector X1

Level	Group	Signal	Pin		Signal	Group	Level
5 V	Power	VINF	1	2	VINF	Power	5 V
5 V	Power	VINF	3	4	VINF	Power	5 V
5 V	Power	VINF	5	6	VINF	Power	5 V
5 V	Power	VINF	7	8	VINF	Power	5 V
5 V	Power	VINF	9	10	VINF	Power	5 V
5 V	Power	VINF	11	12	VINF	Power	5 V
3.0 V	Power	VBAT	13	14	PGOOD	System	3.3 V
0 V	Power	DGND	15	16	DGND	Power	0 V
3.3 V	System	RESIN#	17	18	PROG_MTR	Factory Test	–
3.3 V	System	RCW_SRC_SEL	19	20	FA_VL	Factory Test	–
3.3 V	System	IIC1_SCL_3V3	21	22	TA_PROG_SFP	Factory Test	–
3.3 V	System	IIC1_SDA_3V3	23	24	TA_BB_VDD	Power	3.3 V
5 V_{OC}	System	RTC_INT_OUT#	25	26	EVDD	Power	1.8 / 3.3 V
VBAT	System	RTC_CLKOUT	27	28	DGND	Power	0 V
0 V	Power	DGND	29	30	USB1_D_P	USB	–
0 V	Power	DGND	31	32	USB1_D_M	USB	–
–	USB	USB2_RX_P	33	34	DGND	Power	0 V
–	USB	USB2_RX_M	35	36	DGND	Power	0 V
0 V	Power	DGND	37	38	USB1_RX_P	USB	–
0 V	Power	DGND	39	40	USB1_RX_M	USB	–
–	USB	USB2_TX_P	41	42	DGND	Power	0 V
–	USB	USB2_TX_M	43	44	DGND	Power	0 V
0 V	Power	DGND	45	46	USB1_TX_P	USB	–
0 V	Power	DGND	47	48	USB1_TX_M	USB	–
–	USB	USB2_D_P	49	50	DGND	Power	0 V
–	USB	USB2_D_M	51	52	DGND	Power	0 V
0 V	Power	DGND	53	54	USB1_VBUS	USB	–
–	USB	USB2_VBUS	55	56	USB1_ID	USB	–
–	USB	USB2_ID	57	58	USB_PWRFAULT	USB	1.8 V
1.8 V	USB	USB_DRVVBUS	59	60	VCC1V8	Factory Test	1.8 V
2.5 V	Factory Test	VCC2V5	61	62	DGND	Power	0 V
0 V	Power	DGND	63	64	XSPI1_A_DATA1	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA0	65	66	XSPI1_A_DATA3	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA2	67	68	XSPI1_A_DATA5	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA4	69	70	XSPI1_A_DATA7	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA6	71	72	XSPI1_A_CS0#	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_CS1#	73	74	XSPI1_A_DQS	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_SCK	75	76	DGND	Power	0 V
0 V	Power	DGND	77	78	SDHC2_CLK	SDHC	1.8 V
1.8 V	SDHC	SDHC2_CMD	79	80	DGND	Power	0 V
1.8 V	SDHC	SDHC2_DS	81	82	SDHC2_DAT0	SDHC	1.8 V
1.8 V	SDHC	SDHC2_DAT4	83	84	SDHC2_DAT1	SDHC	1.8 V
0 V	Power	DGND	85	86	SDHC2_DAT2	SDHC	1.8 V
1.8 V	SDHC	SDHC2_DAT5	87	88	SDHC2_DAT3	SDHC	1.8 V
1.8 V	SDHC	SDHC2_DAT6	89	90	DGND	Power	0 V
1.8 V	SDHC	SDHC2_DAT7	91	92	VCC1V2	Factory Test	1.8 V
0 V	Power	DGND	93	94	DP_HPD	DP	1.8 V
–	DP	DP_REFCLK_P	95	96	DGND	Power	0 V
–	DP	DP_REFCLK_N	97	98	DGND	Power	0 V
0 V	Power	DGND	99	100	DP_LANE0_P	DP	–
0 V	Power	DGND	101	102	DP_LANE0_N	DP	–
–	DP	DP_LANE1_P	103	104	DGND	Power	0 V
–	DP	DP_LANE1_N	105	106	DGND	Power	0 V
0 V	Power	DGND	107	108	DP_LANE2_P	DP	–
0 V	Power	DGND	109	110	DP_LANE2_N	DP	–
–	DP	DP_LANE3_P	111	112	DGND	Power	0 V
–	DP	DP_LANE3_N	113	114	DGND	Power	0 V
0 V	Power	DGND	115	116	DP_AUX_P	DP	–
0 V	Power	DGND	117	118	DP_AUX_N	DP	–
0.6 V	Factory Test	VTT	119	120	DGND	Power	0 V

4.16.2 Pinout TQMLS1028A connectors (continued)

Table 13: Pinout connector X2

Level	Group	Signal	Pin		Signal	Group	Level
3.3 V	System	SWD_IO	1	2	TEMP_ALERT#	System	3.3 V_{OC}
3.3 V	System	SWD_CLK/PWM_VREF	3	4	TEMP_CRIT_MOD#	System	3.3 V
0 V	Power	DGND	5	6	VCC3V3S	Factory Test	3.3 V
1.8 V	SDHC	SDHC1_VSEL	7	8	DGND	Power	0 V
1.8 / 3.3 V	SDHC	SDHC1_CLK	9	10	CLK_OUT	Debug	1.8 V
1.8 / 3.3 V	SDHC	SDHC1_CMD	11	12	ASLEEP	Debug	1.8 V
0 V	Power	DGND	13	14	TA_TMP_DETECT#	Trust	1.8 V
1.8 / 3.3 V	SDHC	SDHC1_DAT0	15	16	TA_BB_TMP_DETECT#	Trust	3.3 V
1.8 / 3.3 V	SDHC	SDHC1_DAT1	17	18	DGND	Power	0 V
1.8 / 3.3 V	SDHC	SDHC1_DAT2	19	20	IIC1_SCL	I2C	1.8 V
1.8 / 3.3 V	SDHC	SDHC1_DAT3	21	22	IIC1_SDA	I2C	1.8 V
0 V	Power	DGND	23	24	IIC2_SCL	I2C	1.8 V
1.8 V	UART	UART1_SIN	25	26	IIC2_SDA	I2C	1.8 V
1.8 V	UART	UART1_SOUT	27	28	IIC3_SCL	I2C	1.8 V
1.8 V	UART	UART2_SIN	29	30	IIC3_SDA	I2C	1.8 V
1.8 V	UART	UART2_SOUT	31	32	IIC4_SCL	I2C	1.8 V
0 V	Power	DGND	33	34	IIC4_SDA	I2C	1.8 V
1 V	Factory Test	VDD_1	35	36	IIC5_SCL	I2C	1.8 V
3.3 V	Factory Test	VDD	37	38	IIC5_SDA	I2C	1.8 V
1.35 V	Factory Test	VCC1V35	39	40	IIC6_SCL	I2C	1.8 V
0 V	Power	DGND	41	42	IIC6_SDA	I2C	1.8 V
–	SerDes	SD1_REF_CLK1_P	43	44	DGND	Power	0 V
–	SerDes	SD1_REF_CLK1_N	45	46	DGND	Power	0 V
0 V	Power	DGND	47	48	SD1_RX0_P	SerDes	–
0 V	Power	DGND	49	50	SD1_RX0_N	SerDes	–
–	SerDes	SD1_TX0_P	51	52	DGND	Power	0 V
–	SerDes	SD1_TX0_N	53	54	DGND	Power	0 V
0 V	Power	DGND	55	56	SD1_RX1_P	SerDes	–
0 V	Power	DGND	57	58	SD1_RX1_N	SerDes	–
–	SerDes	SD1_TX1_P	59	60	DGND	Power	0 V
–	SerDes	SD1_TX1_N	61	62	DGND	Power	0 V
0 V	Power	DGND	63	64	SD1_RX2_P	SerDes	–
0 V	Power	DGND	65	66	SD1_RX2_N	SerDes	–
–	SerDes	SD1_TX2_P	67	68	DGND	Power	0 V
–	SerDes	SD1_TX2_N	69	70	DGND	Power	0 V
0 V	Power	DGND	71	72	SD1_RX3_P	SerDes	–
0 V	Power	DGND	73	74	SD1_RX3_N	SerDes	–
–	SerDes	SD1_TX3_P	75	76	DGND	Power	0 V
–	SerDes	SD1_TX3_N	77	78	DGND	Power	0 V
0 V	Power	DGND	79	80	SD1_REF_CLK2_P	SerDes	–
0 V	Power	DGND	81	82	SD1_REF_CLK2_N	SerDes	–
1.8 V	SPI / Secure Element	SPI3_SCK / SE050: ISO7816_CLK	83	84	DGND	Power	0 V
1.8 V	SPI / Secure Element	SPI3_PCS0 / SE050: ISO7816_RST#	85	86	SCAN_MODE# / SE050: ISO14443_LA	Factory Test / Secure Element	1.8 V
1.8 V	SPI / Secure Element	SPI3_SIN / SE050: ISO7816_IO2	87	88	TEST_SEL#	Factory Test	1.8 V
1.8 V	SPI / Secure Element	SPI3_SOUT / SE050: ISO7816_IO1	89	90	TBSCAN_EN# / SE050: ISO14443_LB	JTAG / Secure Element	1.8 V
0 V	Power	DGND	91	92	TDI	JTAG	1.8 V
1.8 V	System	PORESET#	93	94	TDO	JTAG	1.8 V
1.8 V	System	HRESET#	95	96	TCK	JTAG	1.8 V
1.8 V	System	RESET_REQ# [4]	97	98	TMS	JTAG	1.8 V
3.3 V	System	RESET_REQ_OUT# [5]					
0 V	Power	DGND	99	100	TRST#	JTAG	1.8 V
1.8 V	Ethernet	EC1_RX_DV	101	102	DGND	Power	0 V
1.8 V	Ethernet	EC1_RXD0	103	104	EC1_TXD0	Ethernet	1.8 V
1.8 V	Ethernet	EC1_RXD1	105	106	EC1_TXD1	Ethernet	1.8 V
1.8 V	Ethernet	EC1_RXD2	107	108	EC1_TXD2	Ethernet	1.8 V
1.8 V	Ethernet	EC1_RXD3	109	110	EC1_TXD3	Ethernet	1.8 V
1.8 V	Ethernet	EC1_RX_CLK	111	112	EC1_TX_EN	Ethernet	1.8 V
0 V	Power	DGND	113	114	DGND	Power	0 V
1.8 V	Ethernet	EC1_GTX_CLK	115	116	EMI1_MDC	Ethernet	1.8 V
1.8 V	Ethernet	EC1_GTX_CLK125	117	118	EMI1_MDIO	Ethernet	1.8 V
0 V	Power	DGND	119	120	DGND	Power	0 V

4: Default on TQMLS1028A revision 01xx.
5: Default on TQMLS1028A revision 02xx. Backward compatibility with revision 01xx is possible by assembly option.

5. MECHANICS

5.1 Assembly

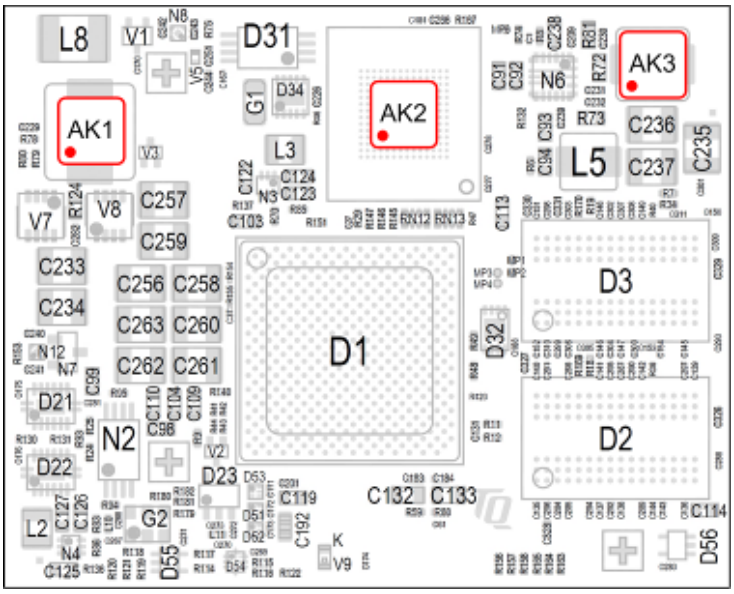


Figure 13: TQMLS1028A assembly revision 01xx, top

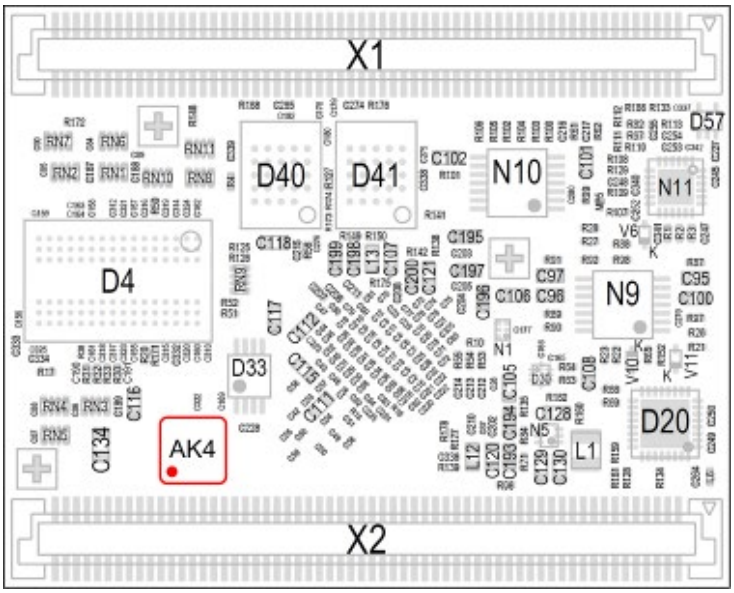


Figure 14: TQMLS1028A assembly revision 01xx, bottom

The labels on the TQMLS1028A revision 01xx show the following information:

Table 14: Labels on TQMLS1028A revision 01xx

Label	Content
AK1	2D serial number
AK2	TQMLS1028A version and revision
AK3	2D MAC address
AK4	Tests performed

5.1 Assembly (continued)

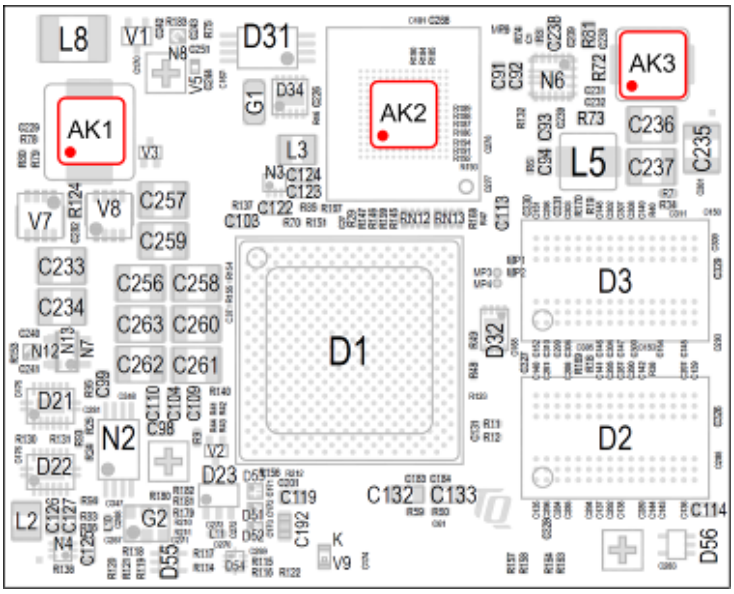


Figure 15: TQMLS1028A assembly revision 02xx, top

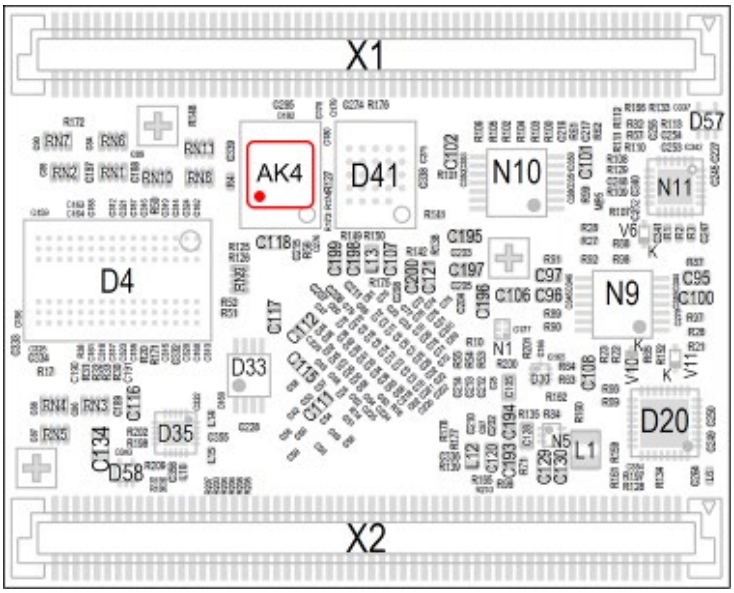


Figure 16: TQMLS1028A assembly revision 02xx, bottom

The labels on the TQMLS1028A revision 02xx show the following information:

Table 15: Labels on TQMLS1028A revision 02xx

Label	Content
AK1	2D serial number
AK2	TQMLS1028A version and revision
AK3	2D MAC address
AK4	Tests performed

5.2 Dimensions

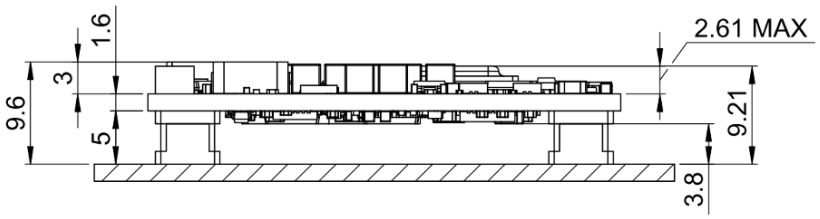


Figure 17: TQMLS1028A dimensions, side view

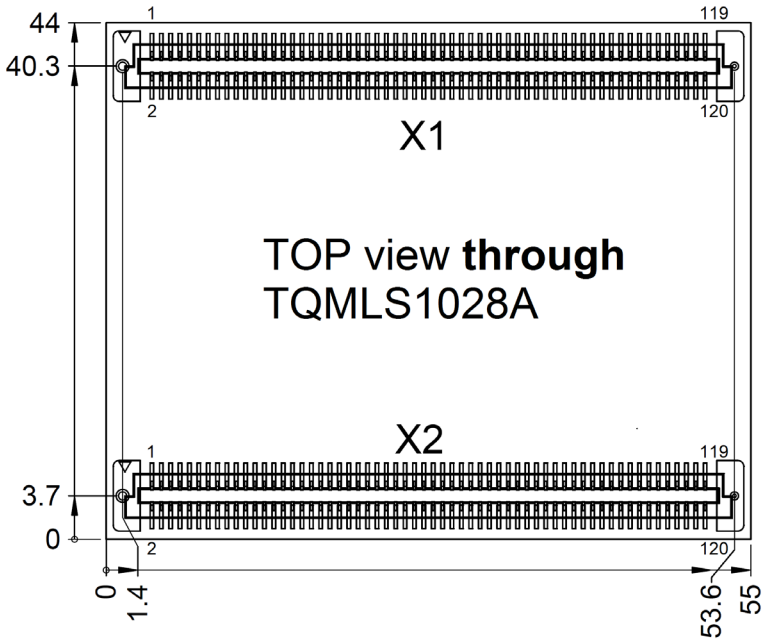


Figure 18: TQMLS1028A dimensions, top view **through** TQMLS1028A

3D models are available in SolidWorks, STEP and 3D PDF formats. Please contact TQ-Support for more details.

5.3 Connectors

The TQMLS1028A is connected to the carrier board with 240 pins on two connectors.

The following table shows details of the connector assembled on the TQMLS1028A.

Table 16: Connector assembled on TQMLS1028A

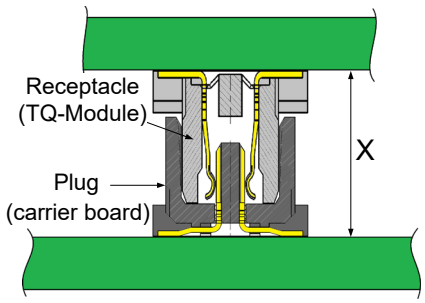
Manufacturer	Part number	Remark
TE connectivity	5177985-5	• 120-pin, 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMLS1028A is held in the mating connectors with a retention force of approximately 24 N.
To avoid damaging the TQMLS1028A connectors as well as the carrier board connectors while removing the TQMLS1028A the use of the extraction tool MOZI8XX is strongly recommended. See chapter 5.8 for further information.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMLS1028A for the extraction tool MOZI8XX.

The following table shows some suitable mating connectors for the carrier board.

Table 17: Carrier board mating connectors

Manufacturer	Pin count / part number	Remark	Stack height (X)	
TE connectivity	120-pin: 5177986-5	On MBLS1028A	5 mm	
	120-pin: 1-5177986-5	–	6 mm	
	120-pin: 2-5177986-5	–	7 mm	
	120-pin: 3-5177986-5	–	8 mm	

5.4 Adaptation to the environment

The TQMLS1028A overall dimensions (length × width) are 55 × 44 mm².
The LS1028A CPU has a maximum height of approximately 9.2 mm above the carrier board, the TQMLS1028A has a maximum height of approximately 9.6 mm above the carrier board.
The TQMLS1028A weighs approximately 16 grams.

5.5 Protection against external effects

As an embedded module, the TQMLS1028A is not protected against dust, external impact and contact (IP00). Adequate protection has to be guaranteed by the surrounding system.

5.6 Thermal management

To cool the TQMLS1028A, approximately 6 Watt must be dissipated, see Table 9 for typical power consumption.
The power dissipation originates primarily in the LS1028A, the DDR4 SDRAM and the buck regulators.
The power dissipation also depends on the software used and can vary according to the application.

Attention: Destruction or malfunction, TQMLS1028A heat dissipation	
	The TQMLS1028A belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LS1028A must be taken into consideration when connecting the heat sink. The LS1028A is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMLS1028A and thus malfunction, deterioration or destruction.

For the TQMLS1028A, TQ-Systems offers a suitable heat spreader (MBLS1028A-HSP) and a suitable heat sink (MBLS1028A-KK). Both can be purchased separately for larger quantities. Please contact your local sales representative.

5.7 Structural requirements

The TQMLS1028A is held in its mating connectors by the 240 pins with a retention force of approximately 24 N.

5.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMLS1028A may only be extracted from the carrier board by using the extraction tool MOZI8XX that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMLS1028A for the extraction tool MOZI8XX.

6. SOFTWARE

The TQMLS1028A is delivered with a preinstalled boot loader and a BSP provided by TQ-Systems, which is configured for the combination of TQMLS1028A and MBLS1028A.
The boot loader provides TQMLS1028A-specific as well as board-specific settings, e.g.:

- LS1028A configuration
- PMIC configuration
- DDR4 SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

More information can be found in the Support Wiki for the TQMLS1028A.

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMLS1028A was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

The following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board.
- A sufficient number of blocking capacitors in all supply voltages.
- Fast or permanently clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and / or shielding besides,
  take note of not only the frequency, but also the signal rise times.
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly).

Since the TQMLS1028A is plugged on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMLS1028A.

The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMLS1028A.

In general, a reliable operation is given when following conditions are met:

Table 18: Climate and operational conditions

Parameter	Range	Remark
Ambient temperature	–40 °C to +85 °C	–
Storage temperature	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the CPUs' thermal characteristics is to be taken from the NXP Reference Manuals (1).

7.5 Reliability and service life

No detailed MTBF calculation was performed for the TQMLS1028A.

The TQMLS1028A is designed to be insensitive to vibration and impact.

High quality industrial grade connectors are assembled on the TQMLS1028A.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The TQMLS1028A is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMLS1028A was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMLS1028A must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMLS1028A enable compliance with EuP requirements for the TQMLS1028A.

8.5 Battery

No batteries are assembled on the TQMLS1028A.

8.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMLS1028A, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMLS1028A is minimised by suitable measures. The TQMLS1028A is delivered in reusable packaging.

8.7 Other entries

The energy consumption of the TQMLS1028A is minimised by suitable measures.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 19: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DDR4	Double Data Rate 4
DNC	Do Not Connect
DP	Display Port
DTR	Double Transfer Rate
EC	European Community
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multi-Media Card
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPU	Graphics Processing Unit
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LED	Light Emitting Diode
MAC	Media Access Control
MOZI	Module extractor (Modulzieher)
MTBF	Mean (operating) Time Between Failures
NAND	Not-And
NOR	Not-Or
O	Output
OC	Open Collector

9.1 Acronyms and definitions (continued)

Table 19: Acronyms (continued)

Acronym	Meaning
PBL	Pre-Boot Loader
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (device)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
RWP	Reversible Write Protected
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SLC	Single Level Cell (memory technology)
SoC	System on Chip
SPI	Serial Peripheral Interface
STEP	Standard for the Exchange of Product (model data)
STR	Single Transfer Rate
SVHC	Substances of Very High Concern
TBD	To Be Determined
TDP	Thermal Design Power
TSN	Time-Sensitive Networking
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
XSPI	Expanded Serial Peripheral Interface

9.2 References

Table 20: Further applicable documents

No.:	Name	Rev., Date	Company
(1)	LS1028A / LS1018A Data Sheet	Rev. C, 06/2018	NXP
(2)	LS1027A / LS1017A Data Sheet	Rev. C, 06/2018	NXP
(3)	LS1028A Reference Manual	Rev. B, 12/2018	NXP
(4)	QorIQ Power Management	Rev. 0, 12/2014	NXP
(5)	QorIQ LS1028A Design Checklist	Rev. 0, 12/2019	NXP
(6)	SA56004X Data Sheet	Rev. 7, 25 February 2013	NXP
(7)	MBLS1028A User's Manual	– current –	TQ-Systems
(8)	TQMLS1028A Support-Wiki	– current –	TQ-Systems

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