TQMLS1012AL
User's Manual

TQMLS1012AL UM 0104
31.01.2020

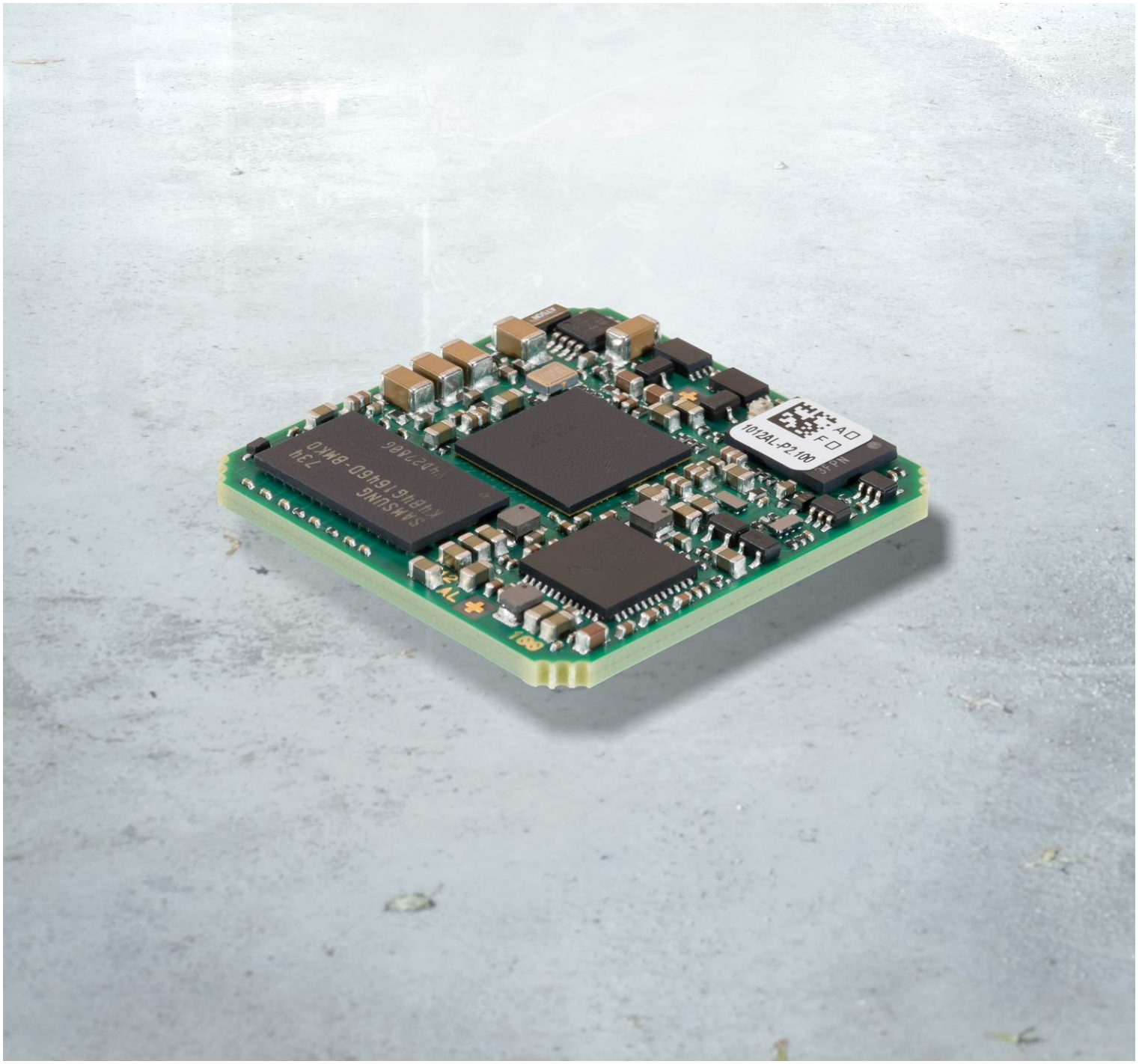

TABLE OF CONTENTS

1. ABOUT THIS MANUAL 1
1.1 Copyright and license expenses 1
1.2 Registered trademarks 1
1.3 Disclaimer 1
1.4 Imprint 1
1.5 Tips on safety 2
1.6 Symbols and typographic conventions 2
1.7 Handling and ESD tips 2
1.8 Naming of signals 3
1.9 Further applicable documents / presumed knowledge 3
2. BRIEF DESCRIPTION 4
2.1 LS1012A block diagram 4
2.2 Key functions and characteristics 5
3. ELECTRONICS 6
3.1 Interfaces to other systems and devices 6
3.1.1 Pin multiplexing 6
3.1.2 LGA pad-out 6
3.1.2.1 TQMLS1012AL pinout 7
3.1.2.2 TQMLS1012AL signals 8
3.2 System components 10
3.2.1 LS1012A CPU 10
3.2.1.1 LS1012A derivatives 10
3.2.1.2 LS1012A errata 10
3.2.1.3 Boot modes 10
3.2.1.4 Boot configuration 11
3.2.1.5 Security Fuse Processor 11
3.2.1.6 Pin multiplexing 11
3.2.1.7 LS1012A errata 11
3.2.2 Memory 12
3.2.2.1 DDR3L SDRAM 12
3.2.2.2 QSPI NOR flash 12
3.2.2.3 24LC64T, EEPROM 13
3.2.2.4 SE97BTB, EEPROM with temperature sensor 13
3.2.3 RTC 14
3.2.4 Reset 15
3.2.5 Interfaces 16
3.2.5.1 TQMLS1012AL-internal interfaces 16
3.2.5.2 EMI 16
3.2.5.3 GPIO 16
3.2.5.4 I^2C 17
3.2.5.5 JTAG 17
3.2.5.6 PCIe 18
3.2.5.7 RGMII 18
3.2.5.8 SATA 19
3.2.5.9 eSDHC 19
3.2.5.10 SerDes 20
3.2.5.11 SGMII 21
3.2.5.12 TAMPER 21
3.2.5.13 UART 21
3.2.5.14 USB 22
3.2.6 Power supply 23
3.2.6.1 Power consumption 23
3.2.6.2 Input protection 23
3.2.6.3 Voltage monitoring 23
3.2.6.4 PMIC 24

TABLE OF CONTENTS (continued)

4. SOFTWARE 25
5. MECHANICS 26
5.1 TQMLS1012AL pads 26
5.2 TQMLS1012AL dimensions 26
5.3 TQMLS1012AL component placement 28
5.4 Adaptation to the environment 29
5.5 Protection against external effects 29
5.6 Thermal management 29
5.7 Structural requirements 29
6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS 30
6.1 EMC 30
6.2 ESD 30
6.3 Operational safety and personal security 30
6.4 Climate and operational conditions 30
6.5 Reliability and service life 30
7. ENVIRONMENT PROTECTION 31
7.1 RoHS 31
7.2 WEEE® 31
7.3 REACH® 31
7.4 EuP 31
7.5 Battery 31
7.6 Packaging 31
7.7 Other entries 31
8. APPENDIX 32
8.1 Acronyms and definitions 32
8.2 References 34

TABLE DIRECTORY

Table 1: Terms and conventions 2
Table 2: TQMLS1012AL pinout, top view **through** TQMLS1012AL 7
Table 3: TQMLS1012AL signals 8
Table 4: LS1012A derivatives 10
Table 5: Boot Mode Select 10
Table 6: JTAG adapters 10
Table 7: General boot settings 11
Table 8: DDR3L SDRAM 12
Table 9: QSPI NOR flash 12
Table 10: 24LC64T EEPROM 13
Table 11: TQMLS1012AL specific data in the EEPROM 13
Table 12: SE97BTP EEPROM 13
Table 13: Reset signals 15
Table 14: TQMLS1012AL-internal interfaces 16
Table 15: Pinout EMI1 16
Table 16: Pinout GPIO 16
Table 17: Pinout I^2C 17
Table 18: Address assignment I2C1 bus 17
Table 19: Pinout JTAG 17
Table 20: Pinout PCIe 18
Table 21: Pinout RGMII 18
Table 22: Pinout SATA 19
Table 23: Pinout SDHC1 19
Table 24: SerDes standard multiplexing 20
Table 25: Pinout SerDes reference clock 20
Table 26: Pinout SGMII 21
Table 27: Pinout TAMPER 21
Table 28: Pinout UART1 21
Table 29: Pinout USB 22
Table 30: TQMLS1012AL voltage rails 23
Table 31: Power consumption 23
Table 32: Power-Management signals 24
Table 33: TQMLS1012AL heights 26
Table 34: Labels on TQMLS1012AL 28
Table 35: Climate and operational conditions 30
Table 36: Acronyms 32
Table 37: Further applicable documents 34

ILLUSTRATION DIRECTORY

Illustration 1: Block diagram LS1012A 4
Illustration 2: Block diagram TQMLS1012AL (simplified) 6
Illustration 3: TQMLS1012AL DDR3L SDRAM interface 12
Illustration 4: Block diagram RTC 14
Illustration 5: Block diagram Reset 15
Illustration 6: Block diagram PMIC interface 24
Illustration 7: TQMLS1012AL dimensions, side view 26
Illustration 8: TQMLS1012AL dimensions, top view 27
Illustration 9: TQMLS1012AL dimensions, recommended PCB land pattern, top view through TQMLS1012AL 27
Illustration 10: TQMLS1012AL component placement, top view 28
Illustration 11: TQMLS1012AL contact numbering scheme, **bottom** view 28

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	25.07.2018	Petz		First issue
0101	30.10.2018	Petz	All Table 36	Block diagrams updated “Package temperature” replaced with “Case temperature”
0102	24.04.2019	Petz	All Illustration 2 Table 10 Illustration 4 Table 14 Table 16	VDD Power Groups specified Updated Moved from 3.2.2.4 to 3.2.2.3 Removed Pull-Up value at EMI1_MDIO corrected Remarks extended
0103	20.09.2019	Petz	All 1.9 4.7 (8)	Hyperlinks updated, typo and formatting Link to PTXdist removed, Link to Yocto added Updated Added
0104	31.01.2020	Petz	All 2 Table 3 3.2.1.3 Table 6 Illustration 5, Table 13 Table 15 Table 17 3.2.5.9.1, 3.2.6 Table 20, Table 22, Table 23 Table 25, Table 26 Table 30, Table 32, Table 33 Table 37	Typo, expression, formatting Supported hardware changed from 01xx to 02xx Footnote 2 added Reworked Added Updated PU for signal EMI1_MDIO corrected I2C1_1V8 signal assignment at TQMLS1012AL corrected Completely reworked Remarks added / updated LS1012A ball assignment corrected, Remarks added Reworked, Remarks clarified, column TQMLS1012AL added Revisions and dates updated

1. ABOUT THIS MANUAL

1.1 Copyright and license expenses

This User's Manual may not be copied, reproduced, translated, changed or distributed, completely or partially in electronic, machine readable, or in any other form without the written consent of TQ-Systems GmbH.

The drivers and utilities for the components used as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Bootloader-licence expenses are paid by TQ-Systems GmbH and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be calculated / declared separately.

1.2 Registered trademarks

TQ-Systems GmbH aims to adhere to copyrights of all graphics and texts used in all publications, and strives to use original or license-free graphics and texts.

All brand names and trademarks mentioned in this User's Manual, including those protected by a third party, unless specified otherwise in writing, are subjected to the specifications of the current copyright laws and the proprietary laws of the present registered proprietor without any limitation. One should conclude that brand and trademarks are rightly protected by a third party.

1.3 Disclaimer

TQ-Systems GmbH does not guarantee that the information in this User's Manual is up-to-date, correct, complete or of good quality. Nor does TQ-Systems GmbH assume guarantee for further usage of the information. Liability claims against TQ-Systems GmbH, referring to material or non-material related damages caused, due to usage or non-usage of the information given in this User's Manual, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of TQ-Systems GmbH.

TQ-Systems GmbH explicitly reserves the rights to change or add to the contents of this User's Manual or parts of it without special notification.

Important Notice:

Before using the Starterkit MBLS1012AL or parts of the schematics of the MBLS1012AL, you must evaluate it and determine if it is suitable for your intended application. You assume all risks and liability associated with such use. TQ-Systems GmbH makes no other warranties including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose. Except where prohibited by law, TQ-Systems GmbH will not be liable for any indirect, special, incidental or consequential loss or damage arising from the usage of the Starterkit MBLS1012AL or schematics used, regardless of the legal theory asserted.

1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMLS1012AL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLS1012AL circuit diagram
- MBLS1012AL User's Manual
- QorIQ LS1012A Data Sheet
- QorIQ LS1012A Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqmls1012al

2. BRIEF DESCRIPTION

This User's Manual describes the TQMLS1012AL hardware revision 02xx and refers to some software settings.
A certain TQMLS1012AL derivative does not necessarily provide all features described in this User's Manual.
This User's Manual does also not replace the LS1012A Reference Manual (2).
The TQMLS1012AL is a universal Minimodule based on the NXP QorIQ Layerscape CPU LS1012A.

2.1 LS1012A block diagram

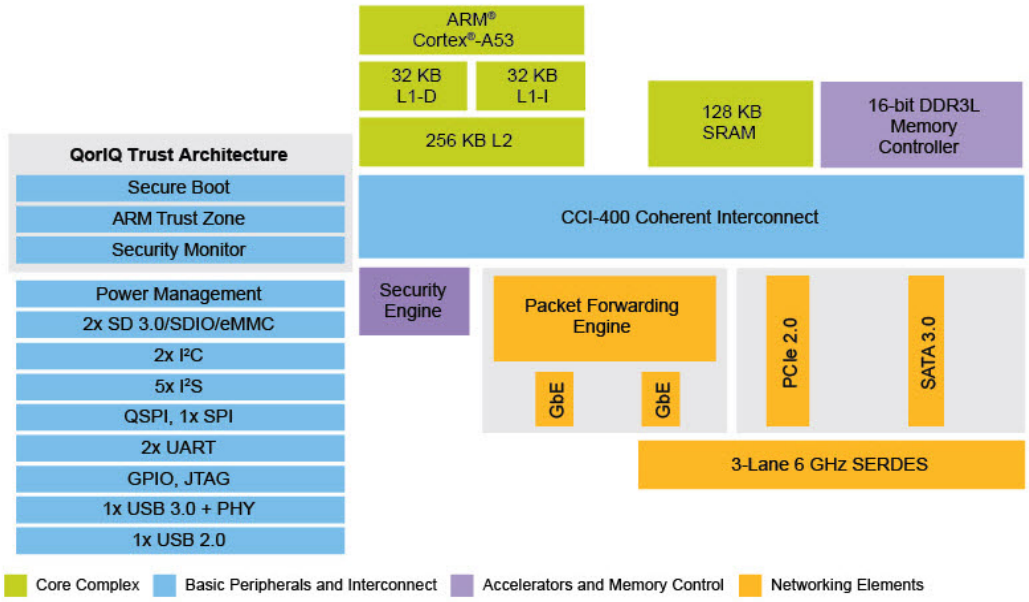

Illustration 1: Block diagram LS1012A
(Source: NXP)

The TQMLS1012AL extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
All essential LS1012A pins are routed to the TQMLS1012AL pads. There are therefore no restrictions for customers using the TQMLS1012AL with respect to an integrated customised design. All essential components like LS1012A, DDR3L SDRAM, eMMC, and power management are already integrated on the TQMLS1012AL.
The main features of the TQMLS1012AL are:

- NXP LS1012A CPU (64-bit, ARM® v8 Cortex®-A53)
- Up to 1 Gbyte DDR3L SDRAM, 16 bit
- Up to 256 Mbyte QSPI NOR flash
- SD card interface (for SD card or eMMC NAND flash)
- 64 kbit EEPROM (assembly option)
- Manufacturer EEPROM (128 byte for protection mode, 128 byte for normal usage)
- RTC (assembly option)
- Temperature sensor
- NXP Power Management Integrated Circuit VR5100
- All essential LS1012A pins are routed to the TQMLS1012AL pads
- Extended temperature range
- Single supply voltage 3.3 V

2.2 Key functions and characteristics

The following components are assembled or available as an assembly option on the TQMLS1012AL:

- QorIQ Layerscape LS1012A CPU
- DDR3L SDRAM
- QSPI NOR flash
- EEPROM
- Manufacturer EEPROM with temperature sensor
- RTC
- Supervisor
- PMIC

The following interfaces are available at the TQMLS1012AL LGA pads in the standard configuration selected by TQ:

- 1 × SerDes with 3 lanes
  - PCIe
  - SATA 3.0
  - SGMII
- 1 × eSDHC 4 Bit mode, with SD card or eMMC support
- 1 × USB 3.0
- 1 × EMI
- 1 × RGMII
- 1 × JTAG
- 1 × UART
- 1 × I^2C (with 1.8 V and 3.3 V)
- 6 × GPIO
- 1 × Tamper

By adapting the pin configuration, further LS1012A interfaces are also available as an alternative to the mentioned factory configuration. These are amongst others:

- 2 × Frequency Timer Module
- 16 × GPIO
- 1 × UART
- 1 × I^2C
- 1 × SAI
- 1 × SPI
- 1 × USB 2.0

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMLS1012AL, and the BSP provided by TQ-Systems GmbH, see also chapter 4.

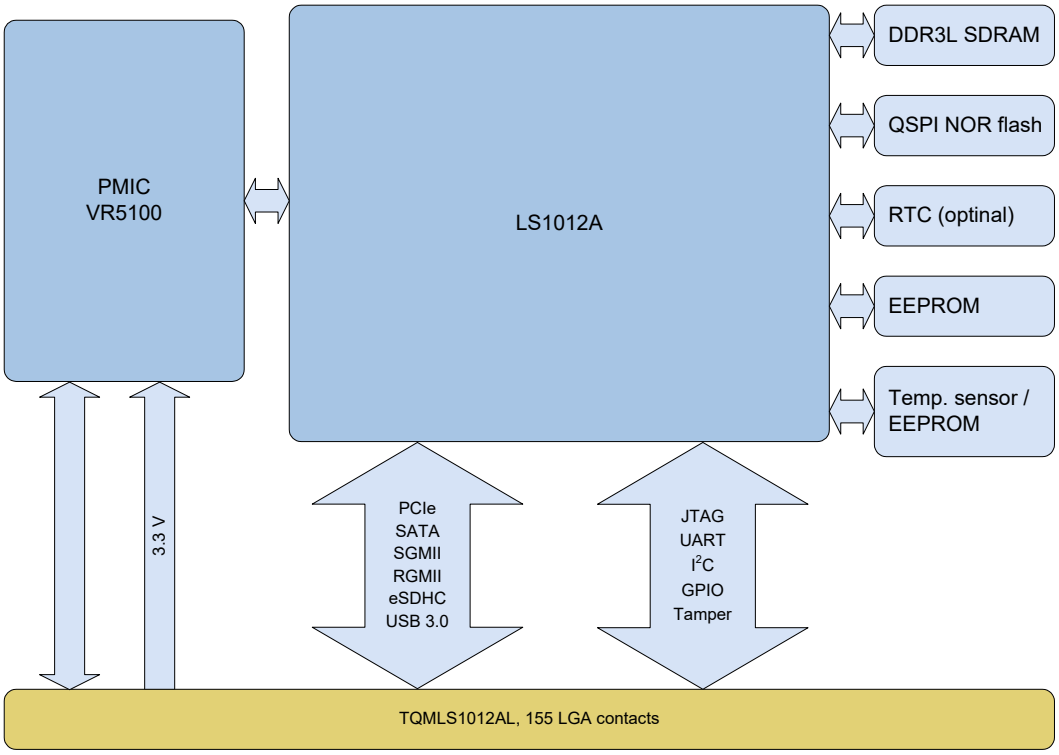

Illustration 2: Block diagram TQMLS1012AL (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

When using the LS1012A signals, the multiple pin configurations by different LS1012A-internal function units must be taken note of. The pin assignment shown in Table 2 refers to the corresponding standard BSP provided by TQ-Systems GmbH in combination with the Starterkit MBLS1012AL.

NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool).

The electrical and pin characteristics are to be taken from the LS1012A Data Sheet (1), and Reference Manual (2) as well as the PMIC Data Sheet (3).

3.1.2 LGA pad-out

Attention: LS1012A pin multiplexing	
	Depending on the configuration, many LS1012A pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the LS1012A Reference Manual (2), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMLS1012AL.

The TQMLS1012AL features 155 LGA pads.

The following table shows the pad-out as **top view through the TQMLS1012AL** with LS1012A2 or LS1012A3 CPU.

Please take note of the different LS1012A1 pad-out!

3.1.2.1 TQMLS1012AL pinout

Table 2: TQMLS1012AL pinout, top view **through** TQMLS1012AL

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14		USB_ VBUS	GND	SDHC1_ DAT3	SDHC1_ CLK	SDHC1_ DAT1	V_ 3V3_ IN	V_ 3V3_ IN	V_ 3V3_ IN	GND	GND	V_ SNVS	GND		14
13	USB1_ D+	USB1_ DRVVBUS	SDHC1_ DAT2	SDHC1_ CMD	GND	SDHC1_ DAT0	V_ SD	GND	PMIC_ INT#	GND	GND	V_ LICELL	GPIO1_ 24	GPIO1_ 25	13
12	USB1_ D–	GND	USB1_ ID	GND	SDHC1_ CD#	SDHC1_ WP	GND	SDHC1_ VSEL	PMIC_ EN	GND	GND	DNC	GND	GPIO1_ 26	12
11	GND	USB1_ TX+	GND	QSPI_ CS0#	GND	QSPI_ DATA0	GND	I2C1_ 1V8_ SDA	I2C1_ 1V8_ SCL	GND	GND	GND	GPIO1_ 27	GPIO1_ 28	11
10	USB1_ RX+	USB1_ TX–	GND	GND							GND	GPIO1_ 29	GND	V_ LDO4_ 2V5	10
9	USB1_ RX–	GND	USB1_ PWR FAULT	QSPI_ SCK							TA_ TMP_ DETECT	GND	GND	GND	9
8	GND	RGMII_ TXD3	RGMII_ TXD2	GND							V_ 1V35	V_ LDO3_ 3V3	V_ 1V8	V_ 1V8	8
7	RGMII_ TX_ CLK	RGMII_ TXD1	GND	V_ 1V8_ PRG							GND	RESET_ REQ# / RCW_ SRC	RESET#	V_ LDO2_ 1V55	7
6	RGMII_ TX_ EN	RGMII_ TXD0	RGMII_ RXD0	GND							DRAM_ DQS0+	GND	DRAM_ DQ1	I2C1_ 3V3_ SDA	6
5	RGMII_ RX_ CLK	RGMII_ RXD1	RGMII_ RXD2	UART1_ SIN							DRAM_ DQS0–	RTC_ SQW / INT#	DRAM_ CK+	I2C1_ 3V3_ SCL	5
4	GND	RGMII_ RXD3	RGMII_ RX_ DV	GND	CLK_ 25M	GND	V_ 0V9	TEMP_ EVENT#	GND	V_ DRAM_ REF	GND	PMIC_ POR#	DRAM_ CK–	GND	4
3	EMI1_ MDC	EMI1_ MDIO	GND	UART1_ SOUT	JTAG_ TDI	JTAG_ TCK	GND	TJTAG_ EN	TBSCAN_ EN#	GND	DRAM_ A0	V_ BAT_ RTC	GND	SATA_ RX+	3
2	GND		SGMII_ TX–	SGMII_ TX+	GND	JTAG_ TDO	JTAG_ TMS	JTAG_ TRST#	GND	PCIE_ RX+	PCIE_ RX–	GND	SATA_ TX–	SATA_ RX–	2
1		SGMII_ RX–	SGMII_ RX+	GND	SD_ REF_ CLK–	SD_ REF_ CLK+	GND	GND	PCIE_ TX+	PCIE_ TX–	GND	GND	SATA_ TX+		1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

3.1.2.2 TQMLS1012AL signals

Details about the electrical characteristics of all pins are to be taken from the LS1012A Data Sheet (1), and Reference Manual (2).

Table 3: TQMLS1012AL signals

Signal	Group	Dir.	Level	LS1012A	TQMLS1012AL	Remark
CLK_25M	CLK	–	1.8 V	22	E4	Do not connect, for reference only
DRAM_A0	DRAM	–	1.35 V	103	L3	Do not connect, for reference only
DRAM_CK+	DRAM	–	1.35 V	–	N5	Do not connect, for reference only
DRAM_CK–	DRAM	–	1.35 V	–	N4	Do not connect, for reference only
DRAM_DQ1	DRAM	–	1.35 V	50	N6	Do not connect, for reference only
DRAM_DQS0+	DRAM	–	1.35 V	111	L6	Do not connect, for reference only
DRAM_DQS0–	DRAM	–	1.35 V	48	L5	Do not connect, for reference only
EMI1_MDC	EMI	O	1.8 V	15	A3	–
EMI1_MDIO	EMI	I/O	1.8 V	82	B3	–
GPIO1_24	GPIO	I/O	1.8 V	65	N13	–
GPIO1_25	GPIO	I/O	1.8 V	126	P13	–
GPIO1_26	GPIO	I/O	1.8 V	64	P12	–
GPIO1_27	GPIO	I/O	1.8 V	125	N11	–
GPIO1_28	GPIO	I/O	1.8 V	63	P11	–
GPIO1_29	GPIO	I/O	1.8 V	127	M10	–
I2C1_1V8_SCL	I2C	I/O	1.8 V	121	J11	–
I2C1_1V8_SDA	I2C	I/O	1.8 V	58	H11	–
I2C1_3V3_SCL	I2C	I/O	3.3 V	–	P5	–
I2C1_3V3_SDA	I2C	I/O	3.3 V	–	P6	–
JTAG_TCK	JTAG	O	1.8 V	18	F3	–
JTAG_TDI	JTAG	I	1.8 V	19	E3	–
JTAG_TDO	JTAG	O	1.8 V	20	F2	–
JTAG_TMS	JTAG	I	1.8 V	84	G2	–
JTAG_TRST#	JTAG	I	1.8 V	85	H2	–
TBSCAN_EN#	JTAG	I	1.8 V	86	J3	–
TJTAG_EN	JTAG	I	1.8 V	21	H3	–
PCIE_RX+	PCIE	I	[1]	92	K2	–
PCIE_RX–	PCIE	I	[1]	27	L2	–
PCIE_TX+	PCIE	O	[1]	91	J1	–
PCIE_TX–	PCIE	O	[1]	26	K1	–
PMIC_EN	PMIC	I	3.0 V	–	J12	–
PMIC_INT#	PMIC	O	1.8 V	–	J13	–
PMIC_POR#	PMIC	–	3.3 V	–	M4	Do not connect, for reference only
V_0V9	Power	–	0.9 V	171	G4	Do not connect, for reference only
V_1V35	Power	–	1.35 V	165	L8	Do not connect, for reference only
V_1V8	Power	O	1.8 V	0	N8	–
V_1V8	Power	O	1.8 V	0	P8	–
V_1V8_PRG	Power	–	1.8 V	134	D7	Do not connect, for reference only
V_3V3_IN	Power	I	3.3 V	–	G14	–
V_3V3_IN	Power	I	3.3 V	–	H14	–
V_3V3_IN	Power	I	3.3 V	–	J14	–
V_BAT_RTC	Power	I	2.7 ~ 2.97 V	–	M3	–
V_DRAM_REF	Power	–	0.675 V	52	K4	Do not connect, for reference only
V_LDO2_1V55	Power	O	1.55 V	–	P7	–
V_LDO3_3V3	Power	O	3.3 V	–	M8	–
V_LDO4_2V5	Power	O	2.5 V	–	P10	–
V_LICELL	Power	I	3.3 V [2]	–	M13	–
V_SD	Power	I	1.8 V / 3.3 V	159	G13	–
V_SNVS	Power	–	3 V	–	M14	Do not connect, for reference only
QSPI_CS0#	QSPI	–	1.8 V	124	D11	Do not connect, for reference only
QSPI_DATA0	QSPI	–	1.8 V	123	F11	Do not connect, for reference only
QSPI_SCK	QSPI	–	1.8 V	–	D9	Do not connect, for reference only
RESET#	RESET	I/O	1.8 V	59	N7	–
RESET_REQ#/RCW_SRC	RESET	O	1.8 V	17	M7	–

1: See PCI Express Base Specification, Revision 3.0.
2: Minimum operating voltage is 2.8 V with a valid LICELL voltage (1.8 V to 3.3 V).
Minimum operating voltage is 3.1 V when no voltage is applied at the LICELL pin.
If operation down to 2.8 V is required for systems without a coin cell, connect the LICELL pin to any system voltage between 1.8 V and 3.3 V.

3.1.2.2 TQMLS1012AL signals (continued)

Table 3: TQMLS1012AL signals (continued)

Signal	Group	Dir.	Level	LS1012A	TQMLS1012AL	Remark
RGMII_RX_CLK	RGMII	I	1.8 V	12	A5	–
RGMII_RX_DV	RGMII	I	1.8 V	81	C4	–
RGMII_RXD0	RGMII	I	1.8 V	14	C6	–
RGMII_RXD1	RGMII	I	1.8 V	80	B5	–
RGMII_RXD2	RGMII	I	1.8 V	13	C5	–
RGMII_RXD3	RGMII	I	1.8 V	79	B4	–
RGMII_TX_CLK	RGMII	O	1.8 V	78	A7	–
RGMII_TX_EN	RGMII	O	1.8 V	11	A6	–
RGMII_TXD0	RGMII	O	1.8 V	77	B6	–
RGMII_TXD1	RGMII	O	1.8 V	10	B7	–
RGMII_TXD2	RGMII	O	1.8 V	76	C8	–
RGMII_TXD3	RGMII	O	1.8 V	9	B8	–
RTC_SQW/INT#	RTC	O	3.3 V	–	M5	–
SATA_RX+	SATA	I	[3]	94	P3	–
SATA_RX–	SATA	I	[3]	29	P2	–
SATA_TX+	SATA	O	[3]	93	N1	–
SATA_TX–	SATA	O	[3]	28	N2	–
SDHC1_CD#	SDHC	I	1.8 V	8	E12	–
SDHC1_CLK	SDHC	O	1.8 V / 3.3 V	–	E14	–
SDHC1_CMD	SDHC	I/O	1.8 V / 3.3 V	5	D13	–
SDHC1_DAT0	SDHC	I/O	1.8 V / 3.3 V	72	F13	–
SDHC1_DAT1	SDHC	I/O	1.8 V / 3.3 V	6	F14	–
SDHC1_DAT2	SDHC	I/O	1.8 V / 3.3 V	73	C13	–
SDHC1_DAT3	SDHC	I/O	1.8 V / 3.3 V	7	D14	–
SDHC1_VSEL	SDHC	O	1.8 V	75	H12	–
SDHC1_WP	SDHC	I	1.8 V / 3.3 V	74	F12	–
SD_REF_CLK+	SERDES	I	–	207	F1	–
SD_REF_CLK–	SERDES	I	–	206	E1	–
SGMII_RX+	SGMII	I	[4]	89	C1	–
SGMII_RX–	SGMII	I	[4]	24	B1	–
SGMII_TX+	SGMII	O	[4]	90	D2	–
SGMII_TX–	SGMII	O	[4]	25	C2	–
TA_TMP_DETECT	TAMPER	I	1.8 V	120	L9	–
TEMP_EVENT#	TEMP	O	3.3 V	–	H4	–
UART1_SIN	UART	I	1.8 V	16	D5	–
UART1_SOUT	UART	O	1.8 V	83	D3	–
USB_VBUS	USB	P	5 V	4	B14	–
USB1_D+	USB	I/O	[5]	130	A13	–
USB1_D–	USB	I/O	[5]	68	A12	–
USB1_DRVVBUS	USB	O	1.8 V	67	B13	–
USB1_ID	USB	I	1.8 V	129	C12	–
USB1_PWRFAULT	USB	I	1.8 V	–	C9	–
USB1_RX+	USB	I	[5]	70	A10	–
USB1_RX–	USB	I	[5]	3	A9	–
USB1_TX+	USB	O	[5]	69	B11	–
USB1_TX–	USB	O	[5]	2	B10	–
DNC	DNC / RFU	–	–	–	M12	Do not connect
(NA)	(NA)	–	–	–	B2	Pin 1 indicator

TQMLS1012AL	Signal	Group
A02, A04, A08, A11, B09, B12, C03, C07, C10, C11, C14, D01, D04, D06, D08, D10, D12, E02, E11, E13, F04, G01, G03, G11, G12, H01, H13, J02, J04, K03, K11, K12, K13, K14, L01, L04, L07, L10, L11, L12, L13, L14, M01, M02, M06, M09, M11, N03, N09, N10, N12, N14, P04, P09	GND	Power
A01, A14, E05, E06, E07, E08, E09, E10, F05, F06, F07, F08, F09, F10, G05, G06, G07, G08, G09, G10, H05, H06, H07, H08, H09, H10, J05, J06, J07, J08, J09, J10, K05, K06, K07, K08, K09, K10, P01, P14	(NA)	(NA)

3: See Serial ATA 3.0 Specification.
4: See Serial-GMII Specification, Rev. 1.8.
5: See USB Specification Rev. 3.0.

3.2 System components

3.2.1 LS1012A CPU

3.2.1.1 LS1012A derivatives

Depending on the TQMLS1012AL variant, one of the following LS1012A derivatives is assembled.

Table 4: LS1012A derivatives

Part number	Characteristics	LS1012A clock	T_J temperature range	Die Rev.
LS1012AXE7EKB	With SEC Encryption	600 MHz	–40 °C to +105 °C	2
LS1012AXE7HKB	With SEC Encryption	800 MHz	–40 °C to +105 °C	2
LS1012AXE7KKB	With SEC Encryption	1000 MHz	–40 °C to +105 °C	2
LS1012AXN7EKB	No SEC Encryption	600 MHz	–40 °C to +105 °C	2
LS1012AXN7HKB	No SEC Encryption	800 MHz	–40 °C to +105 °C	2
LS1012AXN7KKB	No SEC Encryption	1000 MHz	–40 °C to +105 °C	2

3.2.1.2 LS1012A errata

Attention: LS1012A malfunction	
	Please take note of the current LS1012A errata “LS1012ACE”.

3.2.1.3 Boot modes

The boot behaviour of the LS1012A is defined by a 512-bit long Reset Configuration Word (RCW). This is loaded from the connected QSPI Flash to the TQMLS1012AL during normal operation. The LS1012A supports only this one boot source.

In case the RCW in the QSPI flash is missing or damaged, a fall-back level for a suitable boot configuration exists. For this purpose, a fixed standard configuration of the RCW (hard-coded RCW) is loaded, which provides the minimum required values for the LS1012A to operate.

By wiring the signal CLK_OUT, the value for cfg_rcw_src determines one of two possible RCW sources. The value is read in during power-on reset and can be read out in register PORSR1[RCW_SRC], see (2), chapter 4.4.4.1.

Table 5: Boot Mode Select

cfg_rcw_src	RCW source
0	Hard-coded in CPU
1 (default)	QuadSPI (QSPI)

NXP provides the "Code Warrior Development Studio for QorIQ LS series" and the "CodeWarrior TAP" programmer for development and to program the LS1012A processor.

A Ronetix debugger is also a good choice to program the TQMLS1012AL.

The following table shows suitable JTAG adapters.

Table 6: JTAG adapters

Manufacturer	Part number	Details
Lauterbach	JTAG-ARMV8-A/R, LA-3743	Debugger for Cortex-A/R (ARMv8 32/64-bit)
NXP	CWH-CTP-BASE-HE, 935328292598	CodeWarrior TAP
Ronetix	PEEDI, PD-CORTEX-GDB	Flash-Programmer & High Speed JTAG Emulator
	FLASH PROGRAMMER, PGM-CORTEX	Flash-Programmer

3.2.1.4 Boot configuration

The reset configuration signals are multiplexed with other signals. The function is described in Table 5 and Table 7.

Table 7: General boot settings

LS1012A				TQMLS1012AL
Signal (pin)	POR function	Description	Conf.	Wiring
RESET_REQ# (17)	cfg_rcw_src	RCW source selection, see chapter 3.2.1.3.	1	TQMLS1012AL pad M7. Must be pulled to 1.8 V by PU on carrier board during Reset phase (RCW from QSPI).
UART1_SOUT (83)	cfg_eng_use	Crystal transconductance value. Not used, since oscillator is used.	1	TQMLS1012AL pad D3, used for UART. May not be pulled to GND, internal PU.
QSPI_A_DATA0 (123)	cfg_eng_use2	Crystal transconductance value. Not used, since oscillator is used.	1	Internal use on TQMLS1012AL.
QSPI_A_DATA1 (61)	cfg_func_backup	Selection of clock source.	0	Internal use on TQMLS1012AL.
QSPI_A_CS0 (124)	cfg_sysclk_sel	Selection of clock source.	0	Internal use on TQMLS1012AL.

3.2.1.5 Security Fuse Processor

Some LS1012A derivatives provide a Security Engine, the so-called Trust Architecture. To use the Trust Architecture, Security Fuses must be burnt by software. For this purpose, a separate voltage is required, which is provided by LDO1 of the PMIC. This voltage should only be switched on to burn the Fuses. The constraints described in (1), chapters 3.2 and 7 must be observed.

Attention: Security Fuses	
	Over its lifetime, the LS1012A is only specified for six burning processes of its Security Fuses!

3.2.1.6 Pin multiplexing

Depending on the configuration, pin multiplexing allows various pins to be used for different purposes.
This document describes the configuration of the TQMLS1012AL for use on the MBLS1012AL.

Attention: Pin multiplexing	
	Many LS1012A pins can be used in several different configurations. Please observe the wiring instructions for these pins in the LS1012A Reference Manual before integrating / operating your carrier board / Starterkit. Improper programming can lead to malfunctions, premature aging or destruction of the TQMLS1012AL.

3.2.1.7 LS1012A errata

Attention: LS1012A errata	
	Please take note of the current LS1012A errata “LS1012ACE”.

3.2.2 Memory

The following memory is assembled on the TQMLS1012AL:

- 256 Mbyte DDR3L SDRAM with 16 bit interface
- 64 Mbyte QSPI NOR flash
- 64 kbit EEPROM
- 256 bytes Manufacturer EEPROM (128 byte for protection mode, 128 byte for normal usage)

3.2.2.1 DDR3L SDRAM

The TQMLS1012AL features a 16 bit DDR3L SDRAM interface. The default SDRAM size is 256 Mbyte, max SDRAM size is 1 Gbyte.
The LS1012A does not support ECC. One DDR3L SDRAM chip is assembled on the TQMLS1012AL.
The following block diagram shows the DDR3L SDRAM interface.

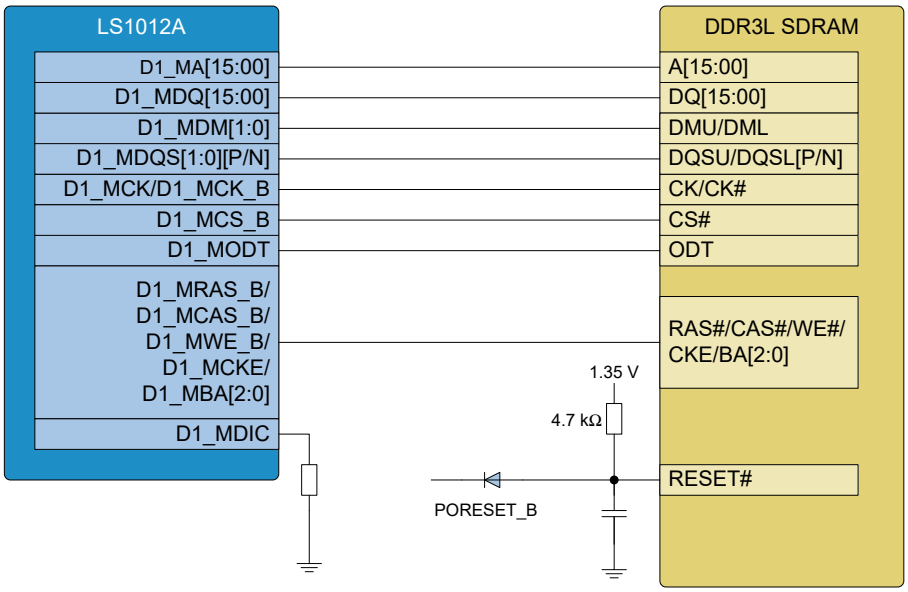

Illustration 3: TQMLS1012AL DDR3L SDRAM interface

The following SDRAMs are supported:

Table 8: DDR3L SDRAM

Manufacturer	Part number	Size	Temperature range
Samsung	K4B2G1646F-BMK0	2 Gbit (256 Mbyte)	–40 °C to +95 °C
Samsung	K4B4G1646E-BMMA000	4 Gbit (512 Mbyte)	–40 °C to +95 °C
Micron	MT41K512M16HA-125 IT:A	8 Gbit (1 Gbyte)	–40 °C to +95 °C

3.2.2.2 QSPI NOR flash

The TQMLS1012AL features a QSPI NOR flash interface. The default NOR flash size is 64 Mbyte, max. NOR flash size is 256 Mbyte.
The memory can be reset by software. The following QSPI NOR flash is supported.

Table 9: QSPI NOR flash

Manufacturer	Part number	Size	Temperature range
Micron	MT25QU512ABB8E12-0SIT	512 Mbit (64 Mbyte)	–40 °C to +85 °C

3.2.2.3 24LC64T, EEPROM

An EEPROM type 24LC64T, controlled by the I2C1 bus, is assembled. Write-Protection (WP) is not supported.
The EEPROM has I²C address `0x50 / 101 0000b`. The following table shows details of the EEPROM.

Table 10: 24LC64T EEPROM

Manufacturer	Part number	Size	Temperature range
Microchip	24LC64T-I/MC	64 Kbit	–40 °C to +85 °C

In the EEPROM, TQMLS1012AL-specific data is stored. It is, however, not essential for the correct operation of the TQMLS1012AL. The user can delete or alter the data. In the following table, the parameters stored in the EEPROM are shown.

Table 11: TQMLS1012AL specific data in the EEPROM

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	Variable	Variable	$32_{(10)}$	Binary	Hard Reset Configuration Word (HRCW), (optional)
0x20	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
0x30	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x40	Variable	Variable	$64_{(10)}$	ASCII	Order code
0x80	–	–	$8{,}064_{(10)}$	–	(Unused)

3.2.2.4 SE97BTB, EEPROM with temperature sensor

The SE97BTB contains a 2 kbit (256 × 8 Bit) EEPROM and a temperature sensor, controlled by the I2C1 bus.

- The SE97BTP has the following I²C addresses:
  - EEPROM (normal): `0x51 / 101 0001b`
  - EEPROM (Protection mode): `0x31 / 011 0001b`
  - Temperature sensor: `0x19 / 001 1001b`

EEPROM:

The following table shows details of the EEPROM.

Table 12: SE97BTP EEPROM

Manufacturer	Part number	Size	Temperature range
NXP	SE97BTP	2 × 128 bytes	–45 °C to +85 °C

The EEPROM is divided into two parts. The lower 128 bytes (00h to 7Fh) can be set to Permanent Write Protected (PWP) mode or Reversible Write Protected (RWP) mode by software. The upper 128 bytes (80h to FFh) cannot be write-protected and can be used for general data storage.

Temperature sensor:

The temperature sensor in the SE97BTP determines the TQMLS1012AL temperature and is located near the LS1012A.
The accuracy of the temperature sensor is as follows:

- Max. ±1 °C between +75 °C and +95 °C
- Max. ±2 °C between +40 °C and +125 °C
- Max. ±3 °C between –40 °C and +125 °C

The EVENT# pin is routed to TQMLS1012AL pad H4 and can be connected via an interruptible I/O expander or a free GPIO of the LS1012A if required. In this case, a suitable pull-up must be provided on the carrier board.

3.2.3 RTC

The LS1012A does not contain an RTC and therefore cannot provide a low-power mode with LS1012A-internal RTC operation.
Therefore, an optional discrete RTC DS1339U-33+ is assembled on the TQMLS1012AL.
If the TQMLS1012AL input voltage (VIN) is not present, the RTC can be powered by a coin cell.
If the TQMLS1012AL input voltage is present, the RTC automatically switches to this voltage source.
The backup supply of the RTC with a current consumption < 1 µA, achieves an operating time of approx. 10 years.
An RTC-internal circuit protects against accidental feedback into the coin cell.
The RTC offers the possibility to charge accumulators or GoldCaps®. This can be achieved via a circuit on the carrier board.
Pin SQW/INT# is routed to TQMLS1012AL pad M5 and thus available on the carrier board.
The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The FC-135R used on the TQMLS1012AL has a standard frequency tolerance of ±20 ppm at +25 °C, and an ageing tolerance of max. ±3 ppm per year.

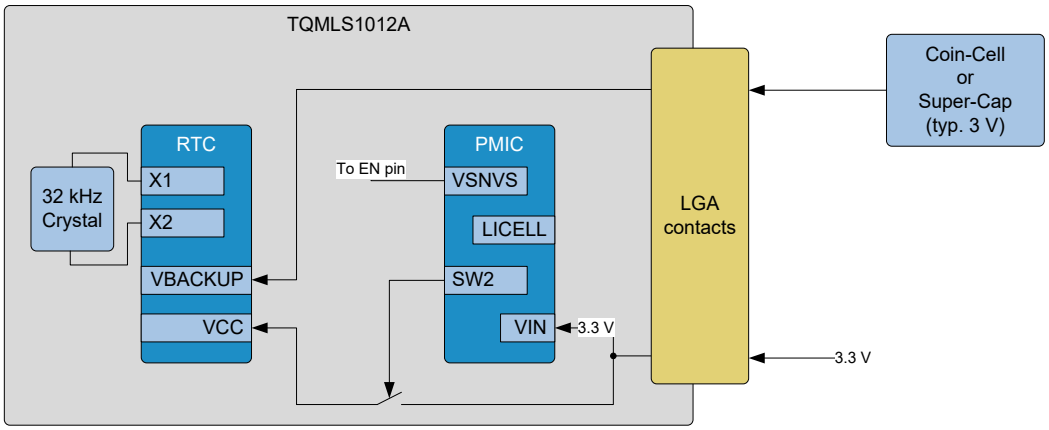

Illustration 4: Block diagram RTC

- The RTC has I²C address `0x68 / 110 1000b`

3.2.4 Reset

Reset inputs or outputs are available at the TQMLS1012AL contacts.
A red LED on the TQMLS1012AL indicates the RESET# condition.
The following block diagram shows the wiring of the reset signals.

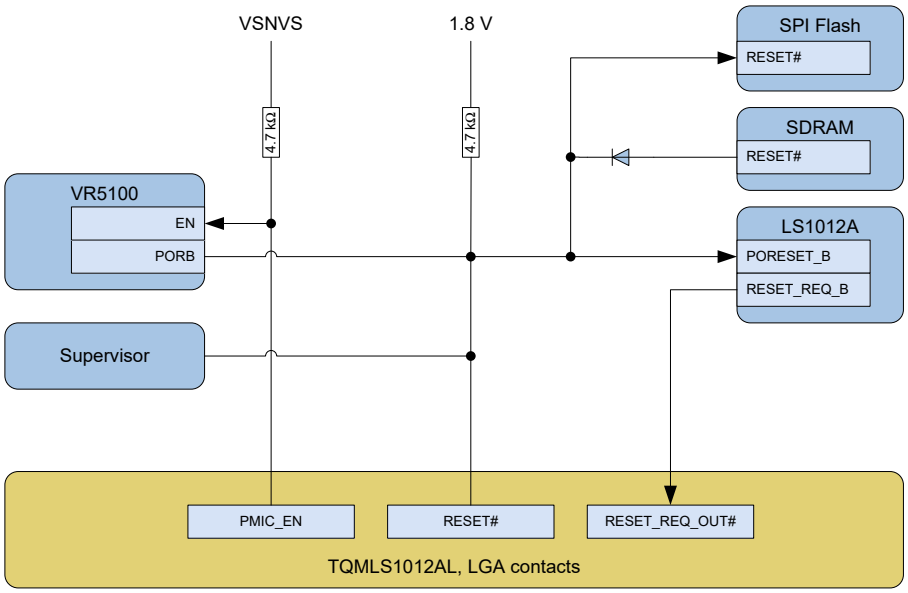

Illustration 5: Block diagram Reset

The following table describes the reset signals available at the TQMLS1012AL LGA pads:

Table 13: Reset signals

Signal	Dir.	LS1012A	TQMLS1012AL	Remark
PMIC_EN	I	–	J12	• PMIC enable input • Enables a cold-reset of the TQMLS1012AL • Pull Low to switch-off the PMIC • Leave floating for normal operation • 4.7 kΩ PU to VSNVS (3 V) on TQMLS1012AL • PMIC must not be switched off if I/O pins on carrier board are still powered.
RESET#	I	59	N7	• Reset input of TQMLS1012AL • Low-active signal • Open Drain • 4.7 kΩ PU to 1.8 V on TQMLS1012AL
RESET_REQ_OUT#	O	17	M7	• Reset output of LS1012A • Low-active signal, Push/Pull (1.8 V) • Connected to reset on carrier board, see (5), chapter 5.17.

3.2.5 Interfaces

3.2.5.1 TQMLS1012AL-internal interfaces

The following interfaces are exclusively used on the TQMLS1012AL.

Table 14: TQMLS1012AL-internal interfaces

Interface	Qty.	Chapter	Remark
DDR	1	3.2.2.1	DDR3L, 16 bit
QSPI	1	3.2.2.2	NOR flash

3.2.5.2 EMI

Ethernet PHYs can be configured at the EMI interface.

Table 15: Pinout EMI1

Signal	Dir.	LS1012A	TQMLS1012AL	Remark
EMI1_MDC	O	15	A3	4.7 kΩ PU to 1.8 V on TQMLS1012AL. Must not be pulled to GND during POR.
EMI1_MDIO	I/O	82	B3	Requires 4.7 kΩ PU to 1.8 V on carrier board.

The signals only support 1.8 V level. If a PHY requires a higher voltage, a level shifter must be used on the carrier board.
The signals must be connected accordingly on the carrier board.

3.2.5.3 GPIO

The LS1012A features up to 28 GPIO signals. These are multiplexed with other functions of the LS1012A. Therefore, only a relatively small number of GPIOs is available in the standard multiplexing. These are listed in Table 16.

Table 16: Pinout GPIO

Signal	LS1012A	TQMLS1012AL	Remark
GPIO1_24	65	N13	–
GPIO1_25	126	P13	–
GPIO1_26	64	P12	–
GPIO1_27	125	N11	–
GPIO1_28	63	P11	–
GPIO1_29	127	M10	4.7 kΩ PU to 1.8 V on TQMLS1012AL; Output Only! Must not be pulled to GND during POR.

To provide more GPIO signals, it is recommended to use GPIO expanders for non-critical signals (LEDs, buttons, and switches for time-uncritical systems) on the carrier board.

3.2.5.4 I²C

The LS1012A features two I²C interfaces, I2C1 and I2C2. Only I2C1 is used on the TQMLS1012AL.
According to NXP, the pins for I2C2 can be multiplexed after the boot process, so the QSPI must be operated in 2-bit mode.
The I2C2 pins are multiplexed to QSPI. Table 17 shows the signals used.

Table 17: Pinout I²C

Signal	LS1012A	TQMLS1012AL	Remark
I2C1_1V8_SCL	121	J11	4.7 kΩ PU to 1.8 V on TQMLS1012AL
I2C1_1V8_SDA	58	H11	4.7 kΩ PU to 1.8 V on TQMLS1012AL
I2C1_3V3_SCL	–	P5	4.7 kΩ PU to 3.3 V on TQMLS1012AL
I2C1_3V3_SDA	–	P6	4.7 kΩ PU to 3.3 V on TQMLS1012AL

The LS1012A supports the I²C 2.0 standard, except HS (high speed) mode.
The interface can operate at up to 100 kbps (standard mode), or up to 400 kbps (fast mode).
The I²C bus operates at 1.8 V. The 1.8 V I²C bus is used on the TQMLS1012AL and routed to the TQMLS1012AL pads.
The I2C1 bus signals are pulled-up to 1.8 V with 4.7 kΩ on the TQMLS1012AL.
A level shifter is present on the TQMLS1012AL to connect 3.3 V devices to the I²C bus.
The 3.3 V I²C interface is routed to the TQMLS1012AL pads. Ensure that no address conflicts occur.
The following table shows the I²C devices connected to the I2C1 bus on the TQMLS1012AL.

Table 18: Address assignment I2C1 bus

Device	Function	7-bit address
M24C64	EEPROM	0x50 / 101 0000b
VR5100	PMIC	0x08 / 000 1000b
DS1339U-33 (optional)	RTC	0x68 / 110 1000b
SE97BTP	Manufacturer EEPROM, Normal Mode	0x51 / 101 0001b
	Manufacturer EEPROM, Protection Mode	0x31 / 011 0001b
	Temperature sensor	0x19 / 001 1001b

If more devices have to be connected to the I²C bus on the carrier board, the maximum capacitive bus load in accordance with the I²C standard must be observed. If necessary, additional pull-ups have to be provided at the buses on the carrier board.

3.2.5.5 JTAG

The LS1012A features a JTAG interface, which is routed to the TQMLS1012AL pads. An appropriate hardware adapter is required to access this interface. The JTAG interface can also be configured for boundary scan. With a Pull-Up at the LS1012A signal TBSCAN_EN_B, the JTAG mode can be set. In the standard multiplexing, the JTAG functionality is available as described in Table 19. The required wiring must be provided on the carrier board.

Table 19: Pinout JTAG

Signal	Dir.	LS1012A	TQMLS1012AL	Remark
JTAG_TDI	I	19	E3	Always-on internal PU
JTAG_TDO	O	20	F2	–
JTAG_TCK	O	18	F3	4.7 kΩ PU to 1.8 V
JTAG_TMS	I	84	G2	Always-on internal PU
JTAG_TRST#	I	85	H2	Always-on internal PU
TJTAG_EN	I	21	H3	4.7 kΩ PU to 1.8 V
TBSCAN_EN#	I	86	J3	4.7 kΩ PU to 1.8 V

3.2.5.6 PCIe

The LS1012A features a PCIe Gen2 interface with one lane (x1) at the SerDes interface.
In the standard multiplexing, Lane B of the SerDes interface is used, see also chapter 3.2.5.10.
The interface is compatible with PCI Express Base Specification, Revision 3.0 and supports transfer rates of 2.5 Gb/s and 5 Gb/s.
The differential signals are routed length-aligned with a differential impedance of 100 Ω.

Table 20: Pinout PCIe

Signal	Dir.	LS1012A	TQMLS1012AL	Remark
PCIE_RX+	I	92	K2	Tie to GND if not used
PCIE_RX–	I	27	L2	Tie to GND if not used
PCIE_TX+	O	91	J1	Leave floating if not used
PCIE_TX–	O	26	K1	Leave floating if not used

The signals must be terminated on the carrier board according to the PCIe specification.

3.2.5.7 RGMII

The LS1012A features an RGMII interface via the Packet Forwarding Engine (PFE). In standard multiplexing, MAC 2 is assigned to the RGMII interface. The interface supports transfer rates of 10/100 and 1000 Mbps, as well as full- and half-duplex connections.
The signals are routed length-aligned with an impedance of 50 Ω to GND.
On the carrier board, they must be connected according to RGMII specifications.

Table 21: Pinout RGMII

Signal	Dir.	LS1012A	TQMLS1012AL	Remark
RGMII_RX_CLK	I	12	A5	–
RGMII_RX_DV	I	81	C4	–
RGMII_RXD0	I	14	C6	–
RGMII_RXD1	I	80	B5	–
RGMII_RXD2	I	13	C5	–
RGMII_RXD3	I	79	B4	–
RGMII_TX_CLK	O	78	A7	–
RGMII_TX_EN	O	11	A6	Requires PD on carrier board
RGMII_TXD0	O	77	B6	–
RGMII_TXD1	O	10	B7	–
RGMII_TXD2	O	76	C8	–
RGMII_TXD3	O	9	B8	–

3.2.5.8 SATA

The LS1012A features a SATA 3.0 AHCI interface at the SerDes interface. Transfer rates of 1.5 Gb/s, 3 Gb/s, and 6 Gb/s are possible.
In the standard multiplexing, Lane D of the SerDes interface is used, see also chapter 3.2.5.10.
The differential signals are routed length-aligned with a differential impedance of 100 Ω.

Table 22: Pinout SATA

Signal	Power-Group	Dir.	LS1012A	TQMLS1012AL	Remark
SATA_RX+	(0.9 V)	I	94	P3	Tie to GND if not used
SATA_RX–	(0.9 V)	I	29	P2	Tie to GND if not used
SATA_TX+	(1.35 V)	O	93	N1	Leave floating if not used
SATA_TX–	(1.35 V)	O	28	N2	Leave floating if not used

3.2.5.9 eSDHC

eSDHC is available in two instances (eSDHC1 and eSDHC2), whereby the use of eSDHC2 is not provided by default.
Instead, the signals are configured as GPIO. The signals are length-aligned with an impedance of 50 Ω to GND.
eSDHC1 offers the possibility to switch the signal level. Thus the UHS-I protocol can be used.
In addition, an eMMC memory module can be connected to this interface. In this case, only 1.8 V levels are used.

3.2.5.9.1 eSDHC1

SD card

The processor supports SD cards up to UHS-I in SDR104 mode at 125 MHz. The eSDHC1 interface is powered by a separate switching regulator. By default, communication starts at 3.3 V and is switched to 1.8 V if required. No voltage switching is required on the mainboard.

eMMC

Instead of an SD card, an eMMC memory can be connected on the carrier board. In this case, SDHC1_CD# and SDHC1_WP are not actively used. A proper termination must be ensured in any case.

Table 23: Pinout SDHC1

Signal	Dir.	LS1012A	TQMLS1012AL	Remark
SDHC1_CD#	I	8	E12	4.7 kΩ PU to 1.8 V on TQMLS1012AL. Must be disconnected during reset with tristate buffer, when used on the carrier board.
SDHC1_CLK	O	71	E14	Must not be pulled to GND during POR. PU to V_SD on TQMLS1012AL.
SDHC1_CMD	I/O	5	D13	–
SDHC1_DAT0	I/O	72	F13	Provide 10 kΩ PU to 1.8 V on carrier board.
SDHC1_DAT1	I/O	6	F14	Provide 10 kΩ PU to 1.8 V on carrier board.
SDHC1_DAT2	I/O	73	C13	Provide 10 kΩ PU to 1.8 V on carrier board.
SDHC1_DAT3	I/O	7	D14	Provide 10 kΩ PU to 1.8 V on carrier board.
SDHC1_VSEL	O	75	H12	Provide 470 kΩ PU to 1.8 V on carrier board.
SDHC1_WP	I	74	F12	–

3.2.5.9.2 eSDHC2

The eSDHC2 interface is not used in standard multiplexing. The pins are routed to the TQMLS1012AL pads as GPIO.
The eMMC functionality can be used on the carrier board taking into account the required pull-ups.

3.2.5.10 SerDes

The LS1012A features a SerDes interface. This offers the following functionalities on three lanes (A, B, D):

- PCIe
- SATA
- SGMII

The standard multiplexing is defined as in Table 24:

Table 24: SerDes standard multiplexing

Lane	Function	Signal	LS1012A	TQMLS1012AL
A	SGMII	SGMII_RX+	89	C1
		SGMII_RX–	24	B1
		SGMII_TX+	90	D2
		SGMII_TX–	25	C2
B	PCIe	PCIE_RX+	92	K2
		PCIE_RX–	27	L2
		PCIE_TX+	91	J1
		PCIE_TX–	26	K1
C	(N/A)	–	–	–
D	SATA	SATA_RX+	94	P3
		SATA_RX–	29	P2
		SATA_TX+	93	N1
		SATA_TX–	28	N2

In this configuration, the MACs provided by the Packet Forwarding Engine (PFE) are available as follows:

- SGMII on SerDes Lane A: MAC1
- RGMII: MAC2

The individual functionalities of the SerDes unit are described in chapters 3.2.5.6, 3.2.5.7, and 3.2.5.8.
An external reference clock can be used for the SerDes unit. This is required, for example, for a Common Clocked Architecture for PCIe. A differential 100 or 125 MHz clock can be fed at the SD1_REF_CLK1 pins for this purpose.
This clock is processed by internal PLLs and distributed to the individual SerDes lanes.
For PCIe, a spread spectrum clock can also be fed in, but only if no other SerDes lanes use this clock.
An external reference clock is provided, since many PCIe cards are designed for only one common clock.

Table 25: Pinout SerDes reference clock

Signal	Power-Group	Dir.	LS1012A	TQMLS1012AL	Remark
SD_REF_CLK+	(0.9 V)	I	207	F1	On-Chip termination and AC-coupling in LS1012A
SD_REF_CLK–	(0.9 V)	I	206	E1	On-Chip termination and AC-coupling in LS1012A

3.2.5.11 SGMII

The LS1012A features an SGMII interface at the SerDes interface.
In the standard multiplexing, Lane A of the SerDes interface is used, see also chapter 3.2.5.10.
The interface offers data rates of 10 Mbps, 100 Mbps, 1000 Mbps and 2500 Mbps in full- and half-duplex.
In this configuration, MAC1 of the LS1012A is used for this interface.
The differential signals are length-aligned with a differential impedance of 100 Ω.

Table 26: Pinout SGMII

Signal	Dir.	LS1012A	TQMLS1012AL	Remark
SGMII_RX+	I	89	C1	Tie to GND if not used
SGMII_RX–	I	24	B1	Tie to GND if not used
SGMII_TX+	O	90	D2	Leave floating if not used
SGMII_TX–	O	25	C2	Leave floating if not used

The signals must be terminated on the carrier board according to the SGMII specifications.
The connected PHYs are supplied locally with a clock signal. The synchronisation with the CPU is done by means of clock recovery from the data signal.
The PHYs connected are supplied locally. The LS1012A is synchronized with the clock recovered from the data signal.

3.2.5.12 TAMPER

Tamper sensors can be connected to the tamper pin of the LS1012A. This function can be used, to delete secret keys or to prevent the execution of certain program routines when the system is physically accessed. The Tamper functionality of this pin has to be enabled by burning a fuse (ITS). By default this fuse is not burnt and the pin acts as a general-purpose input.
The pin is closely linked to the security unit of the LS1012A. The exact function is documented in (4).

Table 27: Pinout TAMPER

Signal	Power-Group	LS1012A	TQMLS1012AL	Remark
TAMPER_DETECT#	(1.8 V)	120	L9	See (5), chapter 5.16.

3.2.5.13 UART

The LS1012A features two UART interfaces, UART1 and UART2. In the standard configuration, UART2 is assigned to the JTAG signals. Unlike UART2, UART1 only provides signals RxD / TxD.
UART1 is intended as debug interface and can be implemented as an RS-232 interface on the carrier board, if required.

Table 28: Pinout UART1

Signal	Power-Group	Dir.	LS1012A	TQMLS1012AL	Remark
UART1_SIN	(1.8 V)	I	16	D5	–
UART1_SOUT	(1.8 V)	O	83	D3	Boot Strap Pin, see 3.2.1.4. Must not be pulled to GND.

3.2.5.14 USB

The LS1012A features a USB 3.0 interface with integrated PHY at the USB1 interface. This supports Super-Speed (5 Gbit/s), High-Speed (480 Mbit/s), Full-Speed (12 Mbit/s), and Low-Speed (1.5 Mbit/s). It offers Host, Device, and OTG 2.0 functions. Depending on the operating mode, not all speeds are available. For the exact assignment see (2), chapter 32.1.1.
The following table shows the pinout.

Table 29: Pinout USB

Signal	Dir.	LS1012A	TQMLS1012AL
USB1_D+	I/O	130	A13
USB1_D–	I/O	68	A12
USB1_RX+	I	70	A10
USB1_RX–	I	3	A9
USB1_TX+	O	69	B11
USB1_TX–	O	2	B10
USB1_DRVVBUS	O	67	B13
USB_VBUS	P	4	B14
USB1_PWRFAULT	I	128	C9
USB1_ID	I	129	C12

The differential impedance for USB signals is nominally 90 Ω. However, the driver outputs of the LS1012A only provide an output impedance of 100 Ω. For this reason, the TQMLS1012AL USB signals are routed with a differential impedance of 100 Ω. This must be taken into account when designing the carrier board.

3.2.6 Power supply

The NXP PMIC VR5100, which is tailored for the LS1 CPUs, is used to complement the LS1012A on the TQMLS1012AL.
The input voltage of the TQMLS1012AL is 3.3 V ±5 %. This corresponds to an input voltage range of 3.135 V to 3.465 V.
All LS1012A I/O voltages are less than 3.3 V. Thus voltage converters for I²C, SPI and UART may be required on the carrier board.
LDOs 2, 3, and 4 on the TQMLS1012AL are not used. The corresponding voltages are routed to the TQMLS1012AL pads and can be used to supply peripherals. Table 30 shows the voltage rails provided.

Table 30: TQMLS1012AL voltage rails

Rail	Voltage	TQMLS1012AL	Input / Output	Max. load	Remark
V_0V9	0.9 V	G4	O	0 A	Do not connect, for reference only
V_1V35	1.35 V	L8	O	0 A	Do not connect, for reference only
V_1V8	1.8 V	N8, P8	O	1 A	–
V_1V8_PRG	1.8 V	D7	O	0 A	Do not connect, for reference only
V_3V3_IN	3.3 V ±5 %	G14, H14, J14	I	–1.183 A	Max. load, input voltage
V_DRAM_REF	0.675 V	K4	O	0 A	Do not connect, for reference only
V_LDO2_1V55	1.55 V	P7	O	0.25 A	Add 4.7 µF on carrier board
V_LDO3_3V3	3.3 V	M8	O	0.1 A	Add 2.2 µF on carrier board
V_LDO4_2V5	2.5 V	P10	O	0.35 A	Add 2.2 µF on carrier board
V_SD	3.3 V / 1.8 V	G13	O	0 A	Do not connect, for reference only
V_SNVS	3 V	M14	O	0 A	Do not connect, for reference only
V_BAT_RTC	3 V	M3	I	< –1µ A	V_{BAT} input
V_LICELL	3 V	M13	I	0 A	V_{BAT} input for PMIC, do not use!

3.2.6.1 Power consumption

The power consumption of the TQMLS1012AL strongly depends on the LS1012A load and the interfaces used.
Typical power consumption values are given in Table 31.

Table 31: Power consumption

Parameter	I	P	Remark
Maximum power consumption, V_{IN} = 3.3 V	1.183 A	3.9 W	Theoretical maximum (Worst Case)
Power consumption, Reset	0.112 A	0.37 W	RESET# = low
Power consumption, U-Boot-Prompt	0.395 A	1.3 W	–
Power consumption, Linux-Prompt	0.39 A	1.29 W	–
Power consumption, Linux, 100 % load	0.56 A	1.85 W	–

3.2.6.2 Input protection

The TQMLS1012AL is designed for embedded operation in a larger system (carrier board). For this reason, no special input-voltage protective-circuitry is provided on the TQMLS1012AL. The external circuitry of the TQMLS1012AL must be designed in such a way that both the board's and the TQMLS1012AL's electronics are adequately protected against incorrect circuitry, ESD events, etc.

3.2.6.3 Voltage monitoring

The 3.3 V input voltage of the TQMLS1012AL is monitored by a Reset circuitry.
The Reset circuitry creates a 200 msec reset-pulse at a threshold voltage between 2.87 and 2.99 V, typically 2.93 V.

Attention: Voltage monitoring	
	The voltage monitoring does not detect an exceedance of the maximum permissible input voltage. An excessively high input voltage can lead to malfunctions, premature aging or destruction of the TQMLS1012AL.

3.2.6.4 PMIC

The properties and functions of the individual pins and signals can be found in the Data Sheets or Reference Manuals of PMIC and LS1012A. The PMIC is connected to the I2C1_1V8V bus of the LS1012A.

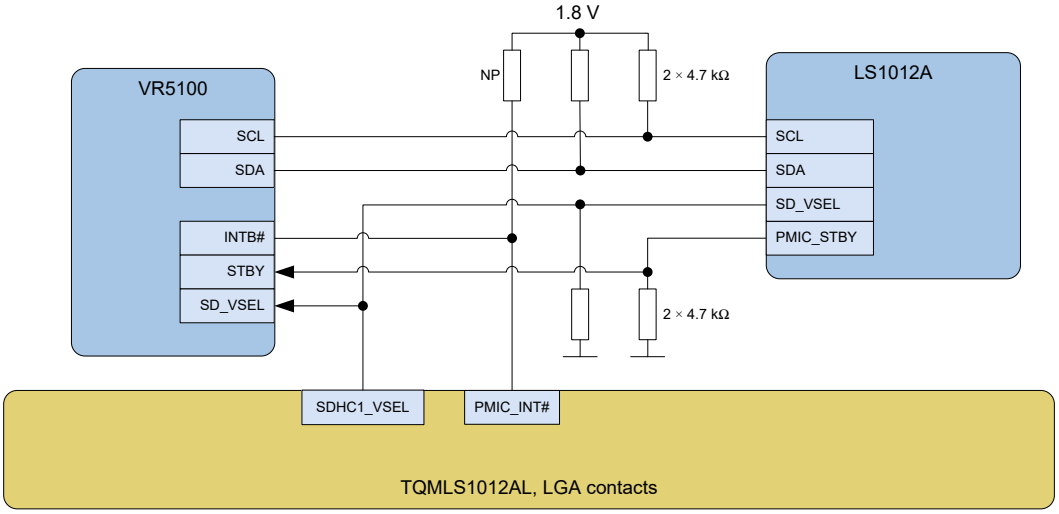

Illustration 6: Block diagram PMIC interface

The following PMIC and power management signals are available on TQMLS1012AL pads, see also chapter 3.2.4.

Table 32: Power-Management signals

Signal	TQMLS1012AL	Remark
PMIC_INT#	J13	Open drain, Low-active PMIC output. Can signal errors. Function can be changed via I²C. Wiring of this signal is optional.
PMIC_STBY	–	PMIC standby pin can be used to toggle between Standby and ON mode. Polarity can be programmed via I²C. Pin is configured as USB1_PWRFAULT by default. Usage as standby signal through assembly option.
SDHC1_VSEL	H12	See chapter 3.2.5.9.1

- The PMIC has I²C address `0x08 / 000 1000b`

Attention: PMIC programming	
	Wrong PMIC programming can lead to the LS1012A or peripherals operating outside its specifications. This can lead to malfunctions, premature aging or destruction of the TQMLS1012AL.

4. SOFTWARE

The TQMLS1012AL is delivered with a preinstalled boot loader U-Boot, which is tailored for the MBLS1012AL.
The BSP provided by TQ-Systems GmbH is configured for the combination of TQMLS1012AL and MBLS1012AL.
The boot loader U-Boot features TQMLS1012AL-specific as well as board-specific settings, e.g.:

- CPU configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

If another bootloader is used, these data must be adapted. Details can be requested from TQ-Support.
More information can be found in the Support Wiki for the TQMLS1012AL.

5. MECHANICS

5.1 TQMLS1012AL pads

The pad assignment shown in Table 2 refers to the corresponding BSP provided by TQ-Systems GmbH.
For information regarding I/O pads in Table 2, refer to the LS1012A pins.

5.2 TQMLS1012AL dimensions

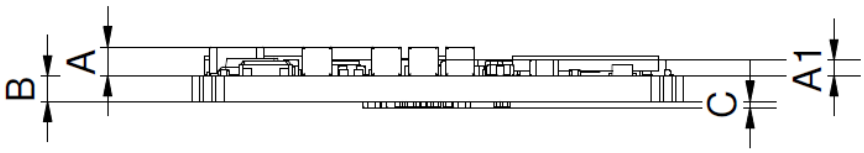

Illustration 7: TQMLS1012AL dimensions, side view

Table 33: TQMLS1012AL heights

Dim.	Value [mm]		Remark
A	1.67 ±0.03		Highest component on TQMLS1012AL, top side.
A1	0.81 ±0.13		Height LS1012A CPU on TQMLS1012AL.
B	1.65 ±0.16		PCB thickness without solder resist.
C	Max. 0.4		Highest component on TQMLS1012AL, bottom side.
E [6]	2.56 ±0.21		LS1012A CPU above carrier board, TQMLS1012AL soldered on carrier board (not shown).
E1 [6]	3.42 ±0.17		Highest component above carrier board, TQMLS1012AL soldered on carrier board (not shown).
X	0.125	+0.075 –0.025	TQMLS1012AL ball height (not shown).

6: Statistical tolerance chain with Gaussian distribution (99.7 % coverage).

5.2 TQMLS1012AL dimensions (continued)

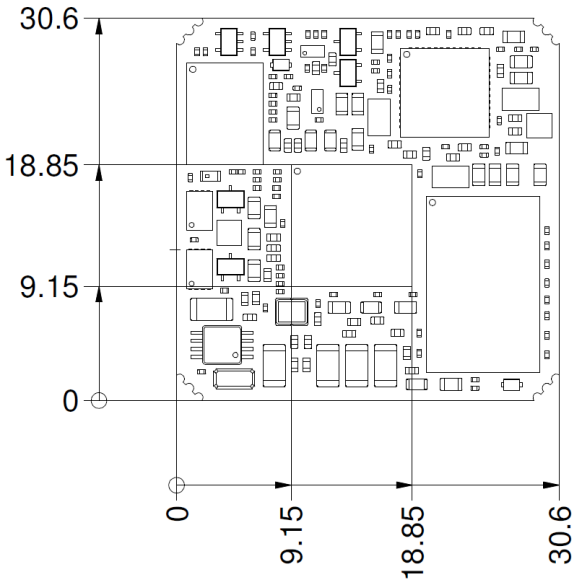

Illustration 8: TQMLS1012AL dimensions, top view

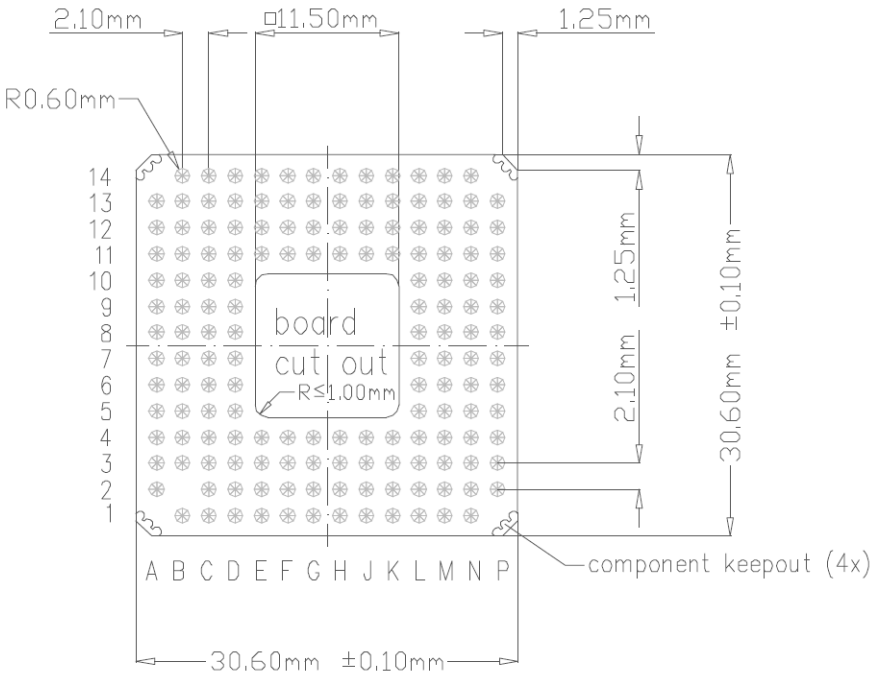

Illustration 9: TQMLS1012AL dimensions, recommended PCB land pattern, top view through TQMLS1012AL

5.3 TQMLS1012AL component placement

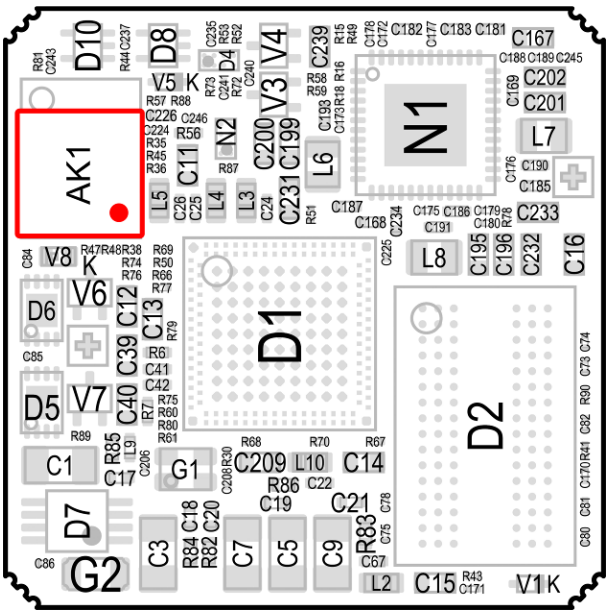

Illustration 10: TQMLS1012AL component placement, top view

The label on the TQMLS1012AL shows the following information:

Table 34: Labels on TQMLS1012AL

Label	Text
AK1	TQMLS1012AL serial number, tests performed, version and revision

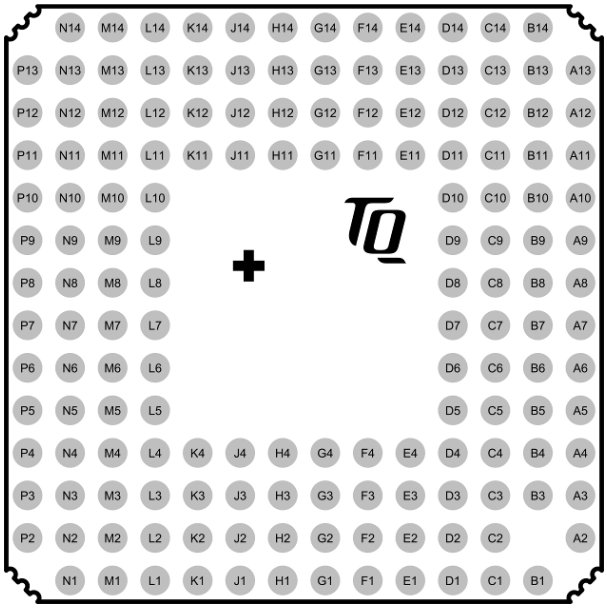

Illustration 11: TQMLS1012AL contact numbering scheme, **bottom** view

5.4 Adaptation to the environment

The TQMLS1012AL has overall dimensions (length × width × height) of 30.6 × 30.6 mm × 3.3 mm³.
The TQMLS1012AL has a maximum height above the carrier board of approximately 3.3 mm.
The TQMLS1012AL weighs approximately 6 grams ±1 gram.

5.5 Protection against external effects

As an embedded module, the TQMLS1012AL is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.6 Thermal management

To cool the TQMLS1012AL, a theoretical peak maximum of approximately 3.9 W have to be dissipated, see Table 31.
The power dissipation originates primarily in the LS1012A, the DDR3L SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.

Attention: Thermal management	
	The LS1012A belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LS1012A must be taken into consideration when connecting the heat sink, see (5). The LS1012A is not the highest component on the TQMLS1012AL. Inadequate cooling connections can lead to overheating of the TQMLS1012AL and thus malfunction, deterioration or destruction.

It is recommended to monitor critical temperatures and to react appropriately by suitable software routines.
The LS1012A has an integrated temperature sensor, which monitors the die temperature. An additional temperature sensor is assembled on the TQMLS1012AL. A further temperature sensor can be placed on the carrier board.
The power dissipation of the PMIC can lead to a severe heating of the component. The PMIC has an internal temperature sensor, which generates four different interrupts. These are set at +110 °C, +120 °C, +125 °C, and +130 °C by default. These interrupts can be used to trigger suitable software measures to reduce power consumption. The PMIC automatically switches off at +140 °C.

5.7 Structural requirements

The TQMLS1012AL has to be soldered on the carrier board. Please contact TQ-Support for soldering instructions (8).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMLS1012AL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

Since the TQMLS1012AL operates on an application-specific carrier board, EMC or ESD tests have to be performed with these.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMLS1012AL.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering, perhaps Zener diode(s)
- Fast signals: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 35: Climate and operational conditions

Parameter	Range	Remark
T_J temperature LS1012A	–40 °C to +105 °C	–
T_J temperature PMIC	–40 °C to +125 °C	–
Environmental temperature PMIC	–40 °C to +105 °C	–
Case temperature DDR3L SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Storage temperature TQMLS1012AL	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information about the CPUs' thermal characteristics is to be taken from NXP documents (1).

6.5 Reliability and service life

At a constant error rate, the calculated theoretical MTBF for the TQMLS1012AL is approx. 1,345,790 hours at +40 °C ambient temperature. The TQMLS1012AL is designed to be insensitive to shock and vibration. Detailed information concerning the CPUs' service life under different operational conditions is to be taken from the NXP Application Note (5).

NXP guarantees a 15 year availability of the LS1012A.

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMLS1012AL is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMLS1012AL was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMLS1012AL always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMLS1012AL on account of available Standby or Sleep-Modes of the components on the TQMLS1012AL.

7.5 Battery

No batteries are assembled on the TQMLS1012AL.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. The energy consumption of this subassembly is minimised by suitable measures.

7.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 36: Acronyms

Acronym	Meaning
AHCI	Advanced Host Controller Interface
ARM®	Advanced RISC Machine
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CPU	Central Processing Unit
DDR3L	Double Data Rate 3 Low voltage
DNC	Do Not Connect
DRAM	Dynamic Random Access Memory
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
eSDHC	enhanced Secure Digital High Capacity
EuP	Energy using Products
FR-4	Flame Retardant 4
FS	Full Speed (USB: 12 Mbit/s)
GPIO	General-Purpose Input/Output
HRCW	Hard Reset Configuration Word
HS	High Speed (USB: 480 Mbit/s)
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LDO	Low Drop-Out
LED	Light Emitting Diode
LGA	Land Grid Array
LS	Low Speed (USB: 1.5 Mbit/s)
MAC	Media Access Control
MTBF	Mean operating Time Between Failures
N/A	Not Applicable
NOR	Not-Or
OTG	On-The-Go

8.1 Acronyms and definitions (continued)

Table 36: Acronyms (continued)

Acronym	Meaning
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PFE	Packet Forwarding Engine
PHY	Physical (layer of the OSI model)
PLL	Phase-Locked Loop
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PU	Pull-Up
PWP	Permanent Write Protected
PWR	Power
QSPI	Quad Serial Peripheral Interface
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGMII	Reduced Gigabit Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
RWP	Reversible Write Protected
SAI	Serial Audio Interface
SATA	Serial ATA
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media-Independent Interface
SPI	Serial Peripheral Interface
SS	SuperSpeed (USB: 5 Gbit/s)
TBD	To Be Determined
UART	Universal Asynchronous Receiver / Transmitter
UHS	Ultra High Speed
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 37: Further applicable documents

No.	Name	Rev., Date	Company
(1)	QorIQ LS1012A Data Sheet	Rev. 2, 01/2019	NXP
(2)	QorIQ LS1012A Reference Manual	Rev. 2, 02/2019	NXP
(3)	VR5100 Data Sheet	Rev. 4.0, 02/2017	NXP
(4)	QorIQ LS1012A Security (SEC) Reference Manual	Rev. 1, 07/2017	NXP
(5)	QorIQ LS1012A Design Checklist AN5192	Rev. 2, 05/2019	NXP
(6)	MBLS1012AL User's Manual	– current –	TQ-Systems
(7)	Support-Wiki for the TQMLS1012AL	– current –	TQ-Systems
(8)	Processing instructions for TQMLS1012AL	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

Technology in Quality