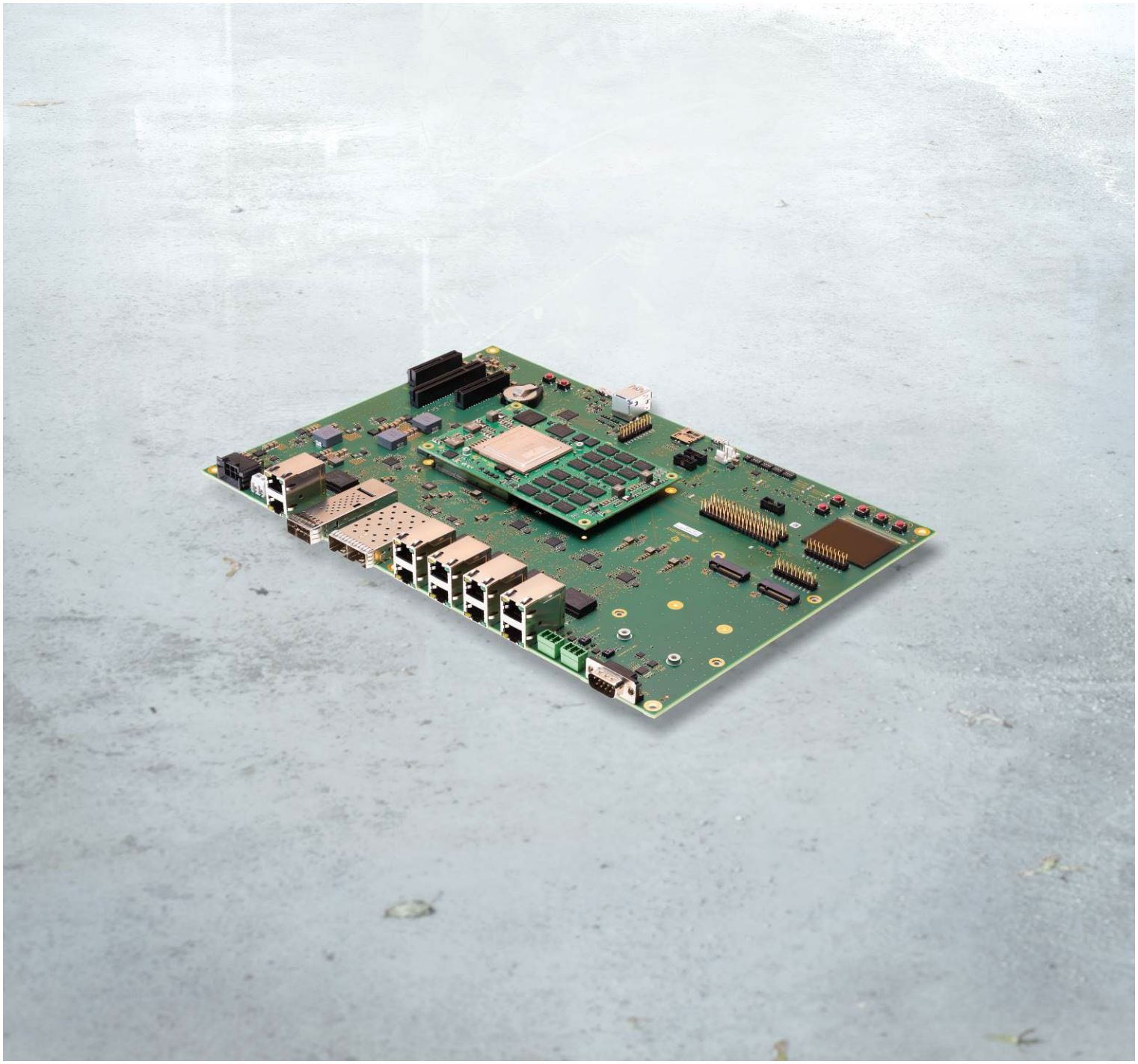
MBLX2160A
User's Manual

MBLX2160A UM 0101
28.02.2022



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	17.09.2021	Petz		First edition
0101	28.2.2022	Kreuzer	Figure 5, 8, 13, 26 Figure 27	Translated Changed

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBLX2160A and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLX2160A circuit diagram
- TQMLX2160A User's Manual
- LX2160A Data Sheet
- LX2160A Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMLX2160A

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBLX2160A revisions 01xx and 02xx.
The MBLX2160A is designed as a carrier board for the TQMLX2160A.
All TQMLX2160A interfaces, which can be used, are available on the MBLX2160A, thus the features of the LX2160A can be evaluated and software development for a TQMLX2160A-based project can be started directly.
The MBLX2160A supports TQMLX2160A modules with an LX2108A, LX2120A or LX2160A CPU.

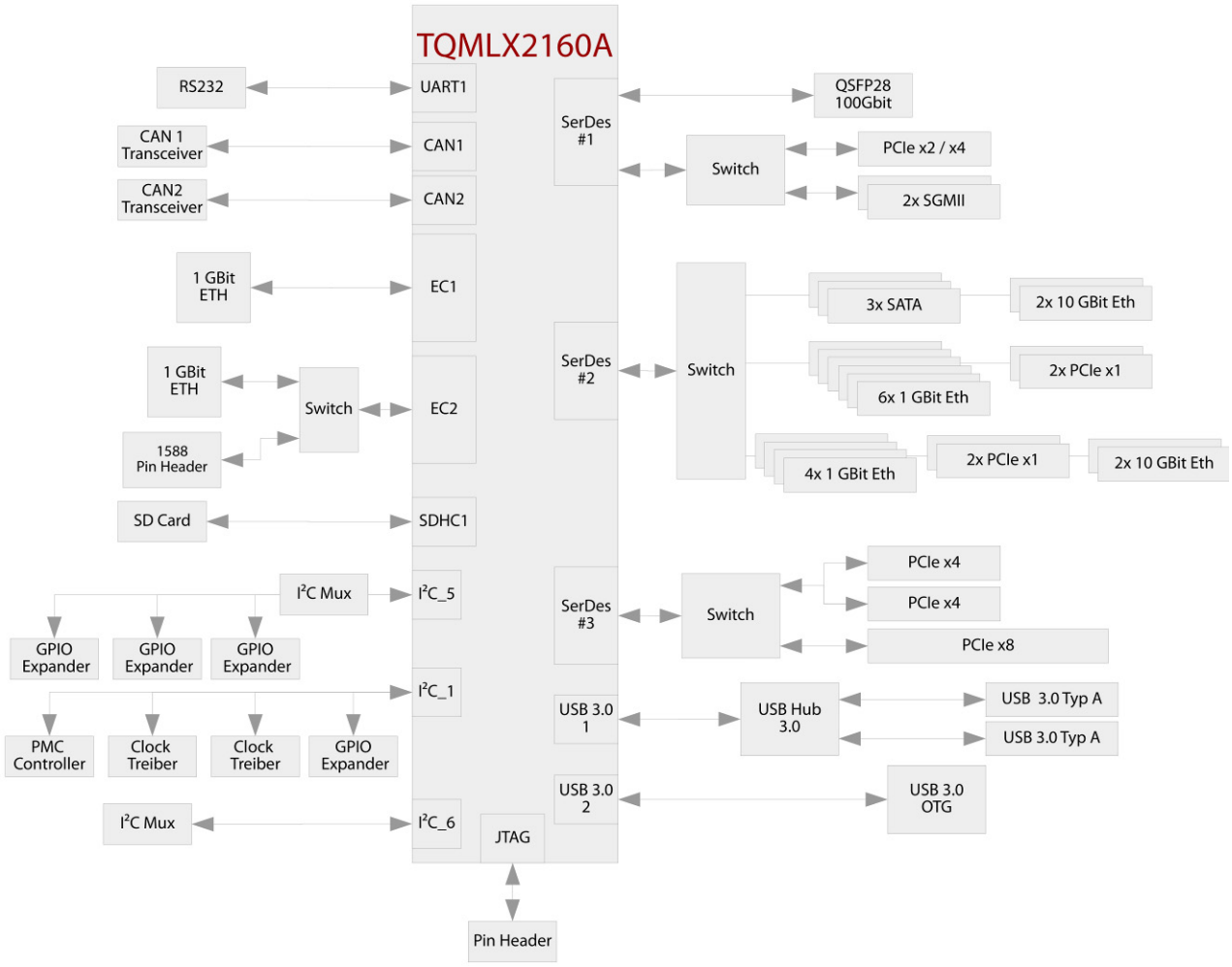


Figure 1: Block diagram MBLX2160A

3. ELECTRONICS

The boot behaviour of the TQMLX2160A can be customised. The required boot-mode configuration can be set with DIP switches on the MBLX2160A, see chapter 3.1.3.

3.1 TQMLX2160A

The TQMLX2160A with its LX2160A CPU is the central system component. It provides DDR4 SDRAM, eMMC, NOR flash and an EEPROM. All TQMLX2160A internal voltages are derived from the 5 V supply voltage. Further information can be found in the TQMLX2160A User's Manual. The available signals are routed to the MBLX2160A via three connectors. On the MBLX2160A the interfaces provided by the TQMLX2160A are routed to industry standard connectors. Furthermore the MBLX2160A provides all power supplies and configurations required for the operation of the TQMLX2160A. The MBLX2160A supports TQMLX2160A modules with an LX2108A, LX2120A or LX2160A CPU.

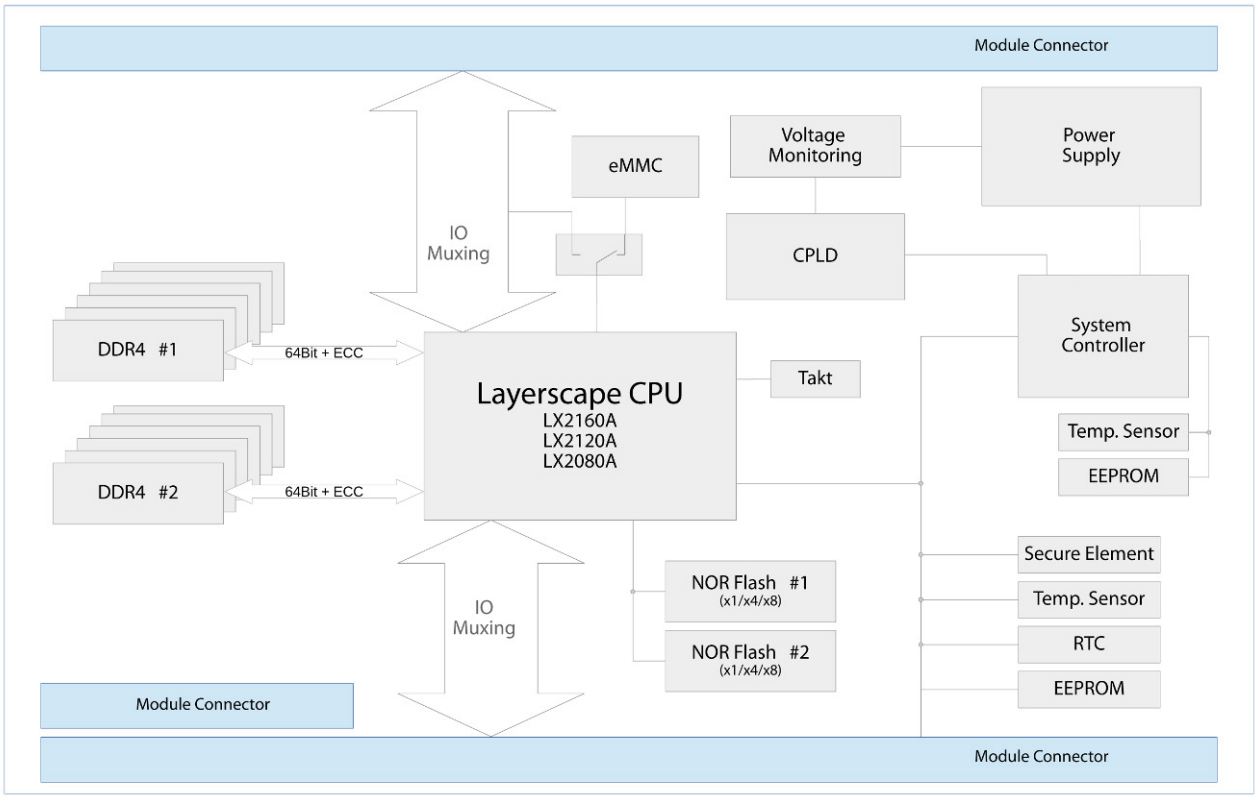


Figure 2: Block diagram TQMLX2160A

The following functionalities and interfaces are provided by the MBLX2160A:

- 1 × QSFP28 slot for 100 Gbit Ethernet module
- 2 × SFP+ slots for 10 Gbit Ethernet modules
- 6 × 1 Gbit Ethernet
- 3 × SATA
- 3 × PCIe / 2 × mPCIe
- 2 × CAN
- SD card
- 2 × USB 3.0 / 1 × USB OTG
- Power supply and voltage supervision
- Multiplexing configuration by DIP switches
- OLED display for additional information

3.1.1 TQMLX2160A mating connectors

The TQMLX2160A is held in the mating connectors on the MBLX2160A by 560 pins on three connectors. The standard board-to-board distance is 8 mm, but a reduced distance of 5 mm is possible.

Table 2: TQMLX2160A mating connectors

Manufacturer	Part number	Type	Remark
EPT	401-55401-51	• 120 pin, 0.5 mm pitch • Data transfer rate 10+ Gbit/s	Assembled on MBLX2160A
	401-55103-51	• 220 pin, 0.5 mm pitch • Data transfer rate 16+ Gbit/s	
	402-51401-51	• 120 pin, 0.5 mm pitch • Data transfer rate 10+ Gbit/s	Assembled on TQMLX2160A
	402-51101-51	• 220 pin, 0.5 mm pitch • Data transfer rate 16+ Gbit/s	

To avoid damaging the connectors of the MBLX2160A or the TQMLX2160A while removing the TQMLX2160A, the use of the extraction tool MOZILX2160A is strongly recommended.

Note: 16 Gbit+ specification	
	It is strongly recommended to use 220-pin connectors on carrier boards that comply with the 16 Gbit+ specification. For the 120-pin connectors the 10 Gbit+ specification is sufficient.

3.1.2 TQMLX2160A pinout

All available TQMLX2160A signals are routed to three connectors on the MBLX2160A.
More detailed information is to be taken from the TQMLX2160A User's Manual (4).
The direction of the signals in the following tables are seen from the TQMLX2160A's perspective.

Note: Available interfaces	
	Depending on the TQMLX2160A derivative not all interfaces are available. Refer to the TQMLX2160A User's Manual and the TQMLX2160A pinout table to see which interfaces are available. When using the processor signals, it is essential to pay attention to the multiple pin assignment by different CPU functions (multiplexing). The pin assignments shown in the following tables refer to the MBLX2160A.

3.1.2 TQMLX2160A pinout (continued)

Table 3: Connector X1, MBLX2160A

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
I	5 V	Power	V_{IN}	A1	B1	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A2	B2	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A3	B3	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A4	B4	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A5	B5	V_{IN}	Power	5 V	I
–	0 V	Ground	DGND	A6	B6	DGND	Ground	0 V	–
I	5 V	Power	V_{IN}	A7	B7	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A8	B8	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A9	B9	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A10	B10	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A11	B11	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A12	B12	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A13	B13	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A14	B14	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A15	B15	V_{IN}	Power	5 V	I
–	0 V	Ground	DGND	A16	B16	DGND	Ground	0 V	–
I	5 V	Power	V_{IN}	A17	B17	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A18	B18	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A19	B19	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A20	B20	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A21	B21	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A22	B22	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A23	B23	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A24	B24	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A25	B25	V_{IN}	Power	5 V	I
–	0 V	Ground	DGND	A26	B26	DGND	Ground	0 V	–
I	5 V	Power	V_{IN}	A27	B27	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A28	B28	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A29	B29	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A30	B30	V_{IN}	Power	5 V	I
I	5 V	Power	V_{IN}	A31	B31	V_{IN}	Power	5 V	I
–	0 V	Ground	DGND	A32	B32	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A33	B33	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A34	B34	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A35	B35	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A36	B36	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A37	B37	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A38	B38	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A39	B39	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A40	B40	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A42	B42	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A43	B43	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A45	B45	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A46	B46	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A47	B47	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A48	B48	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A49	B49	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A50	B50	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–
O	1.8 V	Power	1V8_OUT	A52	B52	1V8_OUT	Power	1.8 V	O
O	1.8 V	Power	1V8_OUT	A53	B53	1V8_OUT	Power	1.8 V	O
–	0 V	Ground	DGND	A54	B54	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A55	B55	DGND	Ground	0 V	–
O	3.3 V	Power	3V3_OUT	A56	B56	3V3_OUT	Power	3.3 V	O
O	3.3 V	Power	3V3_OUT	A57	B57	3V3_OUT	Power	3.3 V	O
I	3.3 V	Power	TA_BB_VDD_IN	A58	B58	(NC)	DNC	–	–
I	1.8 V	Power	TA_PROG_SFP_IN	A59	B59	(NC)	DNC	–	–
–	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	–

3.1.2 TQMLX2160A pinout (continued)

Table 4: Connector X2, MBLX2160A

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	–
O	3.3 V	Reset	LX_CPU_RESET_OUT#	A2	B2	TQMLX_RST_IN#	Reset	3.3 V	I
O	3.3 V	Reset	RESET_REQ_OUT	A3	B3	SYSC_MON_UART_RX	SYSC	3.3 V	I
O	3.3 V	Reset	HRESET_OUT#	A4	B4	SYSC_MON_UART_TX	SYSC	3.3 V	O
–	0 V	Ground	DGND	A5	B5	DGND	Ground	0 V	–
I/O	1.8 V	I2C	I2C1_CPU_SCL	A6	B6	SYSC_UART_MUX_RX	SYSC	3.3 V	I
I/O	1.8 V	I2C	I2C2_CPU_SDA	A7	B7	SYSC_UART_MUX_TX	SYSC	3.3 V	O
–	0 V	Ground	DGND	A8	B8	DGND	Ground	0 V	–
I	3.3 V	JTAG_CPLD	JTAG_CPLD_TCK	A9	B9	I2C5_CPU_SCL	I2C	1.8 V	I/O
I	3.3 V	JTAG_CPLD	JTAG_CPLD_TMS	A10	B10	I2C5_CPU_SDA	I2C	1.8 V	I/O
–	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	–
O	3.3 V	JTAG_CPLD	JTAG_CPLD_TDO	A12	B12	UART1_SOUT	UART	1.8 V	I/O
I	3.3 V	JTAG_CPLD	JTAG_CPLD_TDI	A13	B13	UART1_SIN	UART	1.8 V	I/O
–	0 V	Ground	DGND	A14	B14	UART2_SOUT	UART	1.8 V	I/O
I	3.3 V	SYSC	SYSC_SWCLK	A15	B15	UART2_SIN	UART	1.8 V	I/O
I/O	3.3 V	SYSC	SYSC_SWDIO	A16	B16	UART3_SOUT	UART	1.8 V	I/O
–	0 V	Ground	DGND	A17	B17	UART3_SIN	UART	1.8 V	I/O
–	0 V	Ground	DGND	A18	B18	UART4_SOUT	UART	1.8 V	I/O
I/O	1.8 V	SDHC1	SDHC1_CD#	A19	B19	UART4_SIN	UART	1.8 V	I/O
I/O	1.8 V	SDHC1	SDHC1_WP	A20	B20	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	–
I/O	EVDD	SDHC1	SDHC1_CLK	A22	B22	SDHC1_DATA0	SDHC1	EVDD	I/O
–	0 V	Ground	DGND	A23	B23	SDHC1_DATA1	SDHC1	EVDD	I/O
I/O	1.8 V	SDHC1	SDHC1_DS	A24	B24	SDHC1_DATA2	SDHC1	EVDD	I/O
–	0 V	Ground	DGND	A25	B25	SDHC1_DATA3	SDHC1	EVDD	I/O
I/O	EVDD	SDHC1	SDHC1_CMD	A26	B26	SDHC1_DATA4	SDHC1	1.8 V	I/O
–	0 V	Ground	DGND	A27	B27	SDHC1_DATA5	SDHC1	1.8 V	I/O
I	3.3 V	CONFIG	eMMC_SEL0	A28	B28	SDHC1_DATA6	SDHC1	1.8 V	I/O
I	3.3 V	CONFIG	eMMC_SEL1	A29	B29	SDHC1_DATA7	SDHC1	1.8 V	I/O
–	0 V	Ground	DGND	A30	B30	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	–
I	3.3 V	CONFIG	BOOT_SRC0	A32	B32	DGND	Ground	0 V	–
I	3.3 V	CONFIG	BOOT_SRC1	A33	B33	DGND	Ground	0 V	–
I	3.3 V	CONFIG	BOOT_SRC2	A34	B34	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A35	B35	TA_BB_TMP_DETECT#	TRUST	TA_BB_VDD	I
I	3.3 V	CONFIG	NOR_SWAP#	A36	B36	TA_TMP_DETECT#	TRUST	1.8 V	I
–	0 V	Ground	DGND	A37	B37	TQMLX_WAKE	CONFIG	3.3 V	I
I	1.8 V	CONFIG	EVDD_SEL	A38	B38	TQMLX_SLEEP#	CONFIG	3.3 V	I
O	3.3 V	SYSC	SYSC_I2C2_SCL	A39	B39	EXT_POWER_FAIL_IN#	CONFIG	3.3 V	I
I/O	3.3 V	SYSC	SYSC_I2C2_SDA	A40	B40	TQMLX_PGOOD	CONFIG	3.3 V	O
–	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A42	B42	DGND	Ground	0 V	–
O	–	USB1	USB1_TX_P	A43	B43	DGND	Ground	0 V	–
O	–	USB1	USB1_TX_N	A44	B44	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A45	B45	USB1_ID	USB1	3.3 V	I/O
I	–	USB1	USB1_RX_P	A46	B46	DGND	Ground	0 V	–
I	–	USB1	USB1_RX_N	A47	B47	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A48	B48	USB1_PWRFAULT	USB1	1.8 V	I/O
I/O	–	USB1	USB1_DP	A49	B49	USB1_DRVBUS	USB1	1.8 V	I/O
I/O	–	USB1	USB1_DN	A50	B50	USB1_VBUS	USB1	5 V	I
–	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–
O	–	USB2	USB2_TX_P	A52	B52	DGND	Ground	0 V	–
O	–	USB2	USB2_TX_N	A53	B53	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A54	B54	USB2_ID	USB2	3.3 V	IO
I	–	USB2	USB2_RX_P	A55	B55	DGND	Ground	0 V	–

3.1.2 TQMLX2160A pinout (continued)

Table 4: Connector X2, MBLX2160A (continued)

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
I	–	USB2	USB2_RX_N	A56	B56	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A57	B57	USB2_PWRFAULT	USB2	1.8 V	I/O
I/O	–	USB2	USB2_DP	A58	B58	USB2_DRVBUS	USB2	1.8 V	I/O
I/O	–	USB2	USB2_DN	A59	B59	USB2_VBUS	USB2	5 V	I
–	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A61	B61	DGND	Ground	0 V	–
I	–	SERDES3	SD3_PLLF_REFCLK_P	A62	B62	SD3_PLLS_REFCLK_P	SERDES3	–	I
I	–	SERDES3	SD3_PLLF_REFCLK_N	A63	B63	SD3_PLLS_REFCLK_N	SERDES3	–	I
–	0 V	Ground	DGND	A64	B64	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX0_P	A65	B65	SD3_RX0_P	SERDES3	–	I
O	–	SERDES3	SD3_TX0_N	A66	B66	SD3_RX0_N	SERDES3	–	I
–	0 V	Ground	DGND	A67	B67	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX1_P	A68	B68	SD3_RX1_P	SERDES3	–	I
O	–	SERDES3	SD3_TX1_N	A69	B69	SD3_RX1_N	SERDES3	–	I
–	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A71	B71	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX2_P	A72	B72	SD3_RX2_P	SERDES3	–	I
O	–	SERDES3	SD3_TX2_N	A73	B73	SD3_RX2_N	SERDES3	–	I
–	0 V	Ground	DGND	A74	B74	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX3_P	A75	B75	SD3_RX3_P	SERDES3	–	I
O	–	SERDES3	SD3_TX3_N	A76	B76	SD3_RX3_N	SERDES3	–	I
–	0 V	Ground	DGND	A77	B77	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX4_P	A78	B78	SD3_RX4_P	SERDES3	–	I
O	–	SERDES3	SD3_TX4_N	A79	B79	SD3_RX4_N	SERDES3	–	I
–	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A81	B81	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX5_P	A82	B82	SD3_RX5_P	SERDES3	–	I
O	–	SERDES3	SD3_TX5_N	A83	B83	SD3_RX5_N	SERDES3	–	I
–	0 V	Ground	DGND	A84	B84	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX6_P	A85	B85	SD3_RX6_P	SERDES3	–	I
O	–	SERDES3	SD3_TX6_N	A86	B86	SD3_RX6_N	SERDES3	–	I
–	0 V	Ground	DGND	A87	B87	DGND	Ground	0 V	–
O	–	SERDES3	SD3_TX7_P	A88	B88	SD3_RX7_P	SERDES3	–	I
O	–	SERDES3	SD3_TX7_N	A89	B89	SD3_RX7_N	SERDES3	–	I
–	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A91	B91	DGND	Ground	0 V	–
I/O	1.8 V	SDHC2	SDHC2_MOD_CLK	A92	B92	SDHC2_DATA0	SDHC2	1.8 V	I/O
–	0 V	Ground	DGND	A93	B93	SDHC2_DATA1	SDHC2	1.8 V	I/O
I/O	1.8 V	SDHC2	SDHC2_MOD_DS	A94	B94	SDHC2_DATA2	SDHC2	1.8 V	I/O
–	0 V	Ground	DGND	A95	B95	SDHC2_DATA3	SDHC2	1.8 V	I/O
I/O	1.8 V	SDHC2	SDHC2_MOD_CMD	A96	B96	SDHC2_DATA4	SDHC2	1.8 V	I/O
–	0 V	Ground	DGND	A97	B97	SDHC2_DATA5	SDHC2	1.8 V	I/O
–	0 V	Ground	DGND	A98	B98	SDHC2_DATA6	SDHC2	1.8 V	I/O
–	0 V	Ground	DGND	A99	B99	SDHC2_DATA7	SDHC2	1.8 V	I/O
–	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	–
I	3.3 V	CONFIG	LX_CONFIG_RFU1	A101	B101	DGND	Ground	0 V	–
I	3.3 V	CONFIG	LX_CONFIG_RFU2	A102	B102	TB_SCAN_EN#	TEST	1.8 V	I
I	3.3 V	CONFIG	LX_CONFIG_RFU3	A103	B103	DGND	Ground	0 V	–
I	3.3 V	CONFIG	LX_CONFIG_RFU4	A104	B104	JTAG_LX_HRESET	JTAG_CPU	1.8 V	I
I	3.3 V	CONFIG	LX_CONFIG_RFU5	A105	B105	JTAG_LX_TDI	JTAG_CPU	1.8 V	I
–	0 V	Ground	DGND	A106	B106	JTAG_LX_TDO	JTAG_CPU	1.8 V	O
I/O	1.8 V	I2C	I2C6_CPU_SCL	A107	B107	JTAG_LX_TMS	JTAG_CPU	1.8 V	I
I/O	1.8 V	I2C	I2C5_CPU_SDA	A108	B108	JTAG_LX_TRST#	JTAG_CPU	1.8 V	I
O	1.8 V	JTAG_CPU	JTAG_LX_VREF	A109	B109	JTAG_LX_TCK	JTAG_CPU	1.8 V	I
–	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	–

3.1.2 TQMLX2160A pinout (continued)

Table 5: Connector X3, MBLX2160A

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	–
I/O	1.8 V	EC1	EC1_TX_EN	A2	B2	EC1_RX_CLK	EC1	1.8 V	I/O
–	0 V	Ground	DGND	A3	B3	DGND	Ground	0 V	–
I/O	1.8 V	EC1	EC1_TXD0	A4	B4	EC1_RXD0	EC1	1.8 V	I/O
I/O	1.8 V	EC1	EC1_TXD1	A5	B5	EC1_RXD1	EC1	1.8 V	I/O
I/O	1.8 V	EC1	EC1_TXD2	A6	B6	EC1_RXD2	EC1	1.8 V	I/O
I/O	1.8 V	EC1	EC1_TXD3	A7	B7	EC1_RXD3	EC1	1.8 V	I/O
–	0 V	Ground	DGND	A8	B8	EC1_RX_DV	EC1	1.8 V	I/O
I/O	1.8 V	EC1	EC1_GTX_CLK	A9	B9	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A10	B10	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	–
I/O	1.8 V	EC2	EC2_TX_EN	A12	B12	EC2_RX_CLK	EC2	1.8 V	I/O
–	0 V	Ground	DGND	A13	B13	DGND	Ground	0 V	–
I/O	1.8 V	EC2	EC2_TXD0	A14	B14	EC2_RXD0	EC2	1.8 V	I/O
I/O	1.8 V	EC2	EC2_TXD1	A15	B15	EC2_RXD1	EC2	1.8 V	I/O
I/O	1.8 V	EC2	EC2_TXD2	A16	B16	EC2_RXD2	EC2	1.8 V	I/O
I/O	1.8 V	EC2	EC2_TXD3	A17	B17	EC2_RXD3	EC2	1.8 V	I/O
–	0 V	Ground	DGND	A18	B18	EC2_RX_DV	EC2	1.8 V	I/O
I/O	1.8 V	EC2	EC2_GTX_CLK	A19	B19	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A20	B20	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	–
O	1.8 V	EMI	EMI1_MDC	A22	B22	EC_GTX_CLK125_IN_P	EC1	–	I
I/O	1.8 V	EMI	EMI1_MDIO	A23	B23	EC_GTX_CLK125_IN_N	EC1	–	I
–	0 V	Ground	DGND	A24	B24	DGND	Ground	0 V	–
O	1.8 V	EMI	EMI2_MDC	A25	B25	CLK_OUT	CLKOUT	1.8 V	I/O
I/O	1.8 V	EMI	EMI2_MDIO	A26	B26	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A27	B27	CAN1_TX	CAN	1.8 V	I/O
I/O	1.8 V	EVT	EVT0#	A28	B28	CAN1_RX	CAN	1.8 V	I/O
I/O	1.8 V	EVT	EVT1#	A29	B29	CAN2_TX	CAN	1.8 V	I/O
I/O	1.8 V	EVT	EVT2#	A30	B30	CAN2_RX	CAN	1.8 V	I/O
–	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	–
I/O	1.8 V	EVT	EVT3#	A32	B32	EVT4#	EVT	1.8 V	I/O
–	0 V	Ground	DGND	A33	B33	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A34	B34	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A35	B35	DGND	Ground	0 V	–
I	–	SERDES1	SD1_PLLF_REFCLK_P	A36	B36	SD1_PLLS_REFCLK_P	SERDES1	–	I
I	–	SERDES1	SD1_PLLF_REFCLK_N	A37	B37	SD1_PLLS_REFCLK_N	SERDES1	–	I
–	0 V	Ground	DGND	A38	B38	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX0_P	A39	B39	SD1_TX0_P	SERDES1	–	O
I	–	SERDES1	SD1_RX0_N	A40	B40	SD1_TX0_N	SERDES1	–	O
–	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX1_P	A42	B42	SD1_TX1_P	SERDES1	–	O
I	–	SERDES1	SD1_RX1_N	A43	B43	SD1_TX1_N	SERDES1	–	O
–	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX2_P	A45	B45	SD1_TX2_P	SERDES1	–	O
I	–	SERDES1	SD1_RX2_N	A46	B46	SD1_TX2_N	SERDES1	–	O
–	0 V	Ground	DGND	A47	B47	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX3_P	A48	B48	SD1_TX3_P	SERDES1	–	O
I	–	SERDES1	SD1_RX3_N	A49	B49	SD1_TX3_N	SERDES1	–	O
–	0 V	Ground	DGND	A50	B50	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX4_P	A52	B52	SD1_TX4_P	SERDES1	–	O
I	–	SERDES1	SD1_RX4_N	A53	B53	SD1_TX4_N	SERDES1	–	O
–	0 V	Ground	DGND	A54	B54	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX5_P	A55	B55	SD1_TX5_P	SERDES1	–	O

3.1.2 TQMLX2160A pinout (continued)

Table 5: Connector X3, MBLX2160A (continued)

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
I	–	SERDES1	SD1_RX5_N	A56	B56	SD1_TX5_N	SERDES1	–	O
–	0 V	Ground	DGND	A57	B57	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX6_P	A58	B58	SD1_TX6_P	SERDES1	–	O
I	–	SERDES1	SD1_RX6_N	A59	B59	SD1_TX6_N	SERDES1	–	O
–	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	–
I	–	SERDES1	SD1_RX7_P	A61	B61	SD1_TX7_P	SERDES1	–	O
I	–	SERDES1	SD1_RX7_N	A62	B62	SD1_TX7_N	SERDES1	–	O
–	0 V	Ground	DGND	A63	B63	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A64	B64	DGND	Ground	0 V	–
I	–	SERDES2	SD2_PLLF_REFCLK_P	A65	B65	SD2_PLLS_REFCLK_P	SERDES2	–	I
I	–	SERDES2	SD2_PLLF_REFCLK_N	A66	B66	SD2_PLLS_REFCLK_N	SERDES2	–	I
–	0 V	Ground	DGND	A67	B67	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX0_P	A68	B68	SD2_TX0_P	SERDES2	–	O
I	–	SERDES2	SD2_RX0_N	A69	B69	SD2_TX0_N	SERDES2	–	O
–	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX1_P	A71	B71	SD2_TX1_P	SERDES2	–	O
I	–	SERDES2	SD2_RX1_N	A72	B72	SD2_TX1_N	SERDES2	–	O
–	0 V	Ground	DGND	A73	B73	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A74	B74	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX2_P	A75	B75	SD2_TX2_P	SERDES2	–	O
I	–	SERDES2	SD2_RX2_N	A76	B76	SD2_TX2_N	SERDES2	–	O
–	0 V	Ground	DGND	A77	B77	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX3_P	A78	B78	SD2_TX3_P	SERDES2	–	O
I	–	SERDES2	SD2_RX3_N	A79	B79	SD2_TX3_N	SERDES2	–	O
–	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX4_P	A81	B81	SD2_TX4_P	SERDES2	–	O
I	–	SERDES2	SD2_RX4_N	A82	B82	SD2_TX4_N	SERDES2	–	O
–	0 V	Ground	DGND	A83	B83	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A84	B84	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX5_P	A85	B85	SD2_TX5_P	SERDES2	–	O
I	–	SERDES2	SD2_RX5_N	A86	B86	SD2_TX5_N	SERDES2	–	O
–	0 V	Ground	DGND	A87	B87	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX6_P	A88	B88	SD2_TX6_P	SERDES2	–	O
I	–	SERDES2	SD2_RX6_N	A89	B89	SD2_TX6_N	SERDES2	–	O
–	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	–
I	–	SERDES2	SD2_RX7_P	A91	B91	SD2_TX7_P	SERDES2	–	O
I	–	SERDES2	SD2_RX7_N	A92	B92	SD2_TX7_N	SERDES2	–	O
–	0 V	Ground	DGND	A93	B93	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A94	B94	DGND	Ground	0 V	–
I/O	1.8 V	GPIO	GPIO3_DATA08	A95	B95	VBAT_RTC	RTC	3.3 V	I
I/O	1.8 V	GPIO	GPIO3_DATA09	A96	B96	RTC_INT_OUT#	RTC	3.3 V	O
I/O	1.8 V	GPIO	GPIO3_DATA10	A97	B97	RTC_CLKOUT	RTC	3.3 V	O
I/O	3.3 V	I2C	I2C1_MOD_SDA	A98	B98	EEPROM_WP	EEPROM	3.3 V	I
O	3.3 V	I2C	I2C1_MOD_SCL	A99	B99	EVENT_TEMPSENSOR	TEMP	3.3 V	O
–	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A101	B101	IRQ0	IRQ	1.8 V	I/O
–	0 V	Ground	DGND	A102	B102	IRQ1	IRQ	1.8 V	I/O
I/O	–	SECURE	SE14443_LA	A103	B103	IRQ2	IRQ	1.8 V	I/O
I/O	–	SECURE	SE14443_LB	A104	B104	IRQ3	IRQ	1.8 V	I/O
–	0 V	Ground	DGND	A105	B105	IRQ4	IRQ	1.8 V	I/O
I/O	3.3 V	SECURE	SE_7816_IO1	A106	B106	IRQ5	IRQ	1.8 V	I/O
I/O	3.3 V	SECURE	SE_7816_IO2	A107	B107	IRQ6	IRQ	1.8 V	I/O
O	3.3 V	SECURE	SE_7816_CLK	A108	B108	IRQ7	IRQ	1.8 V	I/O
I	3.3 V	SECURE	SE_7816_RST#	A109	B109	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	–

3.1.3 Boot source

The boot source of the MBLX2160A is selected with signals BOOT_SRC[2:0] via DIP switch S1. Pull-ups to 3.3 V are populated on the TQMLX2160A.

Table 6: Boot source selection, DIP switch S1

BOOT_SRC2 (S1-3)	BOOT_SRC1 (S1-2)	BOOT_SRC0 (S1-1)	Boot source
1	1	1	NOR flash
1	1	0	SD card
1	0	1	eMMC
1	0	0	I^2C
0	1	1	XSPI – NAND 2 KB
0	1	0	XSPI – NAND 4 KB
0	0	1	Hard Coded Option
0	0	0	TBD

Graphical illustration of the DIP switch positions for the three most common boot sources:

The boot source is shown on the status display in the "Settings" ⇨ "DIP S1" menu.

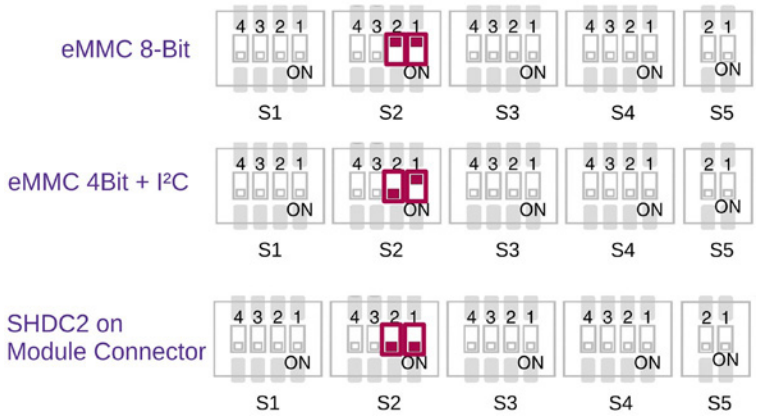
3.1.4 eMMC configuration

The TQMLX2160A allows a variable configuration of the SDHC2 interface via the control signals eMMC_SEL[1:0].
These signals are pulled-up to 3.3 V on the TQMLX2160A by default.
The eMMC_SEL[1:0] configuration cannot be changed during runtime.

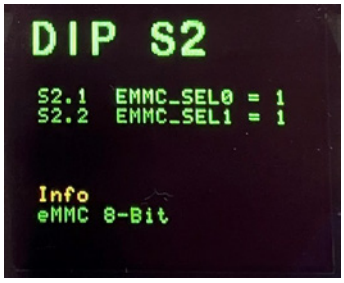
Table 7: eMMC configuration

eMMC_SEL1 (X2-A29)	eMMC_SEL0 (X2-A28)	Configuration
0	0	SDHC2 at TQMLX2160A connectors
0	1	eMMC on TQMLX2160A connected with 4 bit data + 2 × I²C
1	0	(Undefined)
1	1	eMMC on TQMLX2160A connected with 8 bit data (default)

Graphical illustration of the DIP switch positions for the three defined SDHC2 configurations:



The current setting is shown on the status display in the "Settings" ⇨ "DIP S2" menu.



3.1.5 NOR flash swap

The TQMLX2160A allows an easy toggle of the two XSPI NOR Flash devices. Only the chip select of both devices are swapped, so that from the view of the CPU no differences appear. This is controlled by the signal NOR_SWAP#. The signal has a pullup to 3.3V on the TQMLX2160A. Alternatively a software configuration via I²C slave register is provided.

Table 8: NOR flash swap configuration

NOR_SWAP# (X2-A36)	I²C slave register	NOR flash multiplexing
Low	–	X mapping
High	–	1:1 mapping
Low	1:1 mapping set	1:1 mapping
High	1:1 mapping set	1:1 mapping
Low	X mapping set	X mapping
High	X mapping set	X mapping

The current setting of the NOR_SWAP# pins is shown on the status display in the "Settings" ⇨ "DIP S1" menu.

3.2 Power supply and PMC

The MBLX2160A has to be supplied with 24 V ±10 % (21.6 V to 26.4 V) at the 6-pin connector X40 or the 2-pin connector X4.

The maximum power consumption of the MBLX2160A can be approximately 180 W to 220 W without additional PCIe cards.

An STM µController STM32L471VET6 serves as Power Management Controller (PMC) for controlling and monitoring the power supplies on the MBLX2160A. The PMC starts up as soon as the MBLX2160A is supplied with power. In the further course the following points are monitored and controlled by the PMC:

- Power-up sequencing
- Voltage monitoring
- Reset control of the TQMLX2160A
- OLED display control with display of real-time data / settings

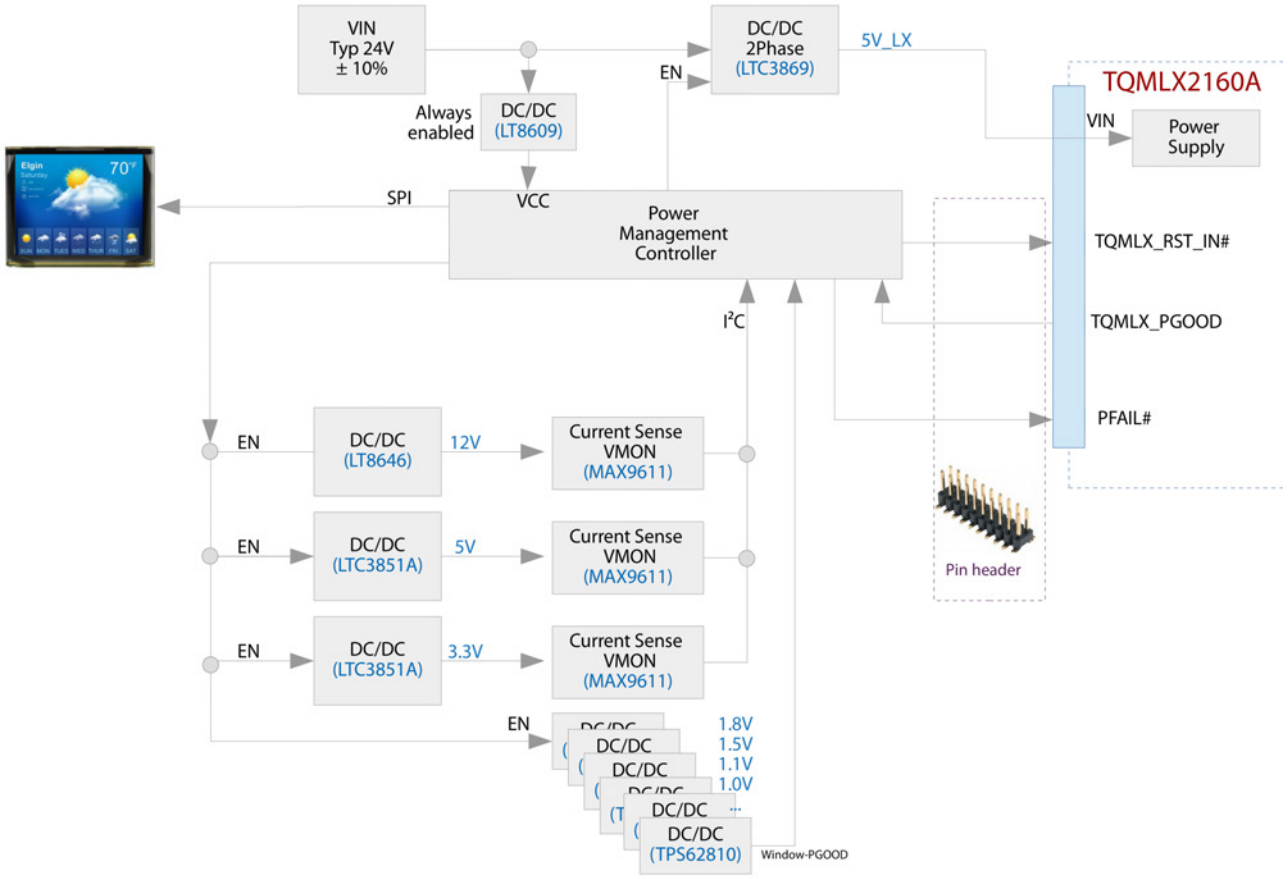


Figure 3: Block diagram power supply

On the MBLX2160A there is a two-part supply:

- The Standby Power Supply (VIN_FILT_STANDBY) is permanently activated for Power Management Controller / Display / Wake Up
- The Switched Power Supply (VIN_FILT_MAIN) ist the main power supply of the MBLX2160A. It must be activated first and is switched off in standby mode.

The standard pinout of the 24 V power supply was adopted on the MBLX2160A:

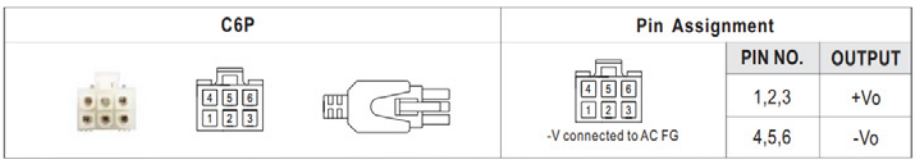


Figure 4: Pinout 24 V Supply
(source: Mean Well)

Alternatively, as usual on TQ mainboards, a connector with screw terminals is available on the MBLX2160A. The polarity is labeled in copper on the mainboard.

3.2.1 Protective circuitry

The protection circuit features the following characteristics:

- Overcurrent protection by fuse 10 A, slow blow
- Overvoltage protection diode
- Reverse polarity protection
- Filter

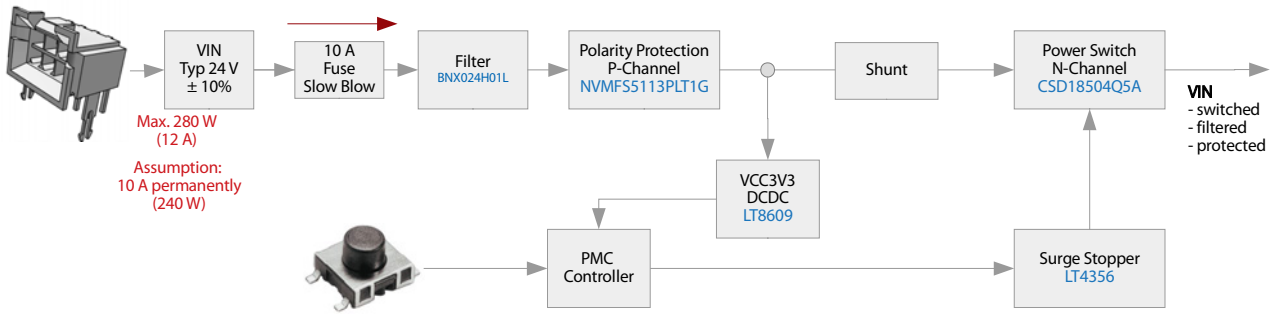


Figure 5: Block diagram protective circuit

3.2.2 MBLX2160A power-up sequencing

The power-up sequencing of the MBLX2160A is controlled by the PMC.
The status of signals TQMLX_PGOOD and MBLX_PGOOD is also indicated by green LEDs.

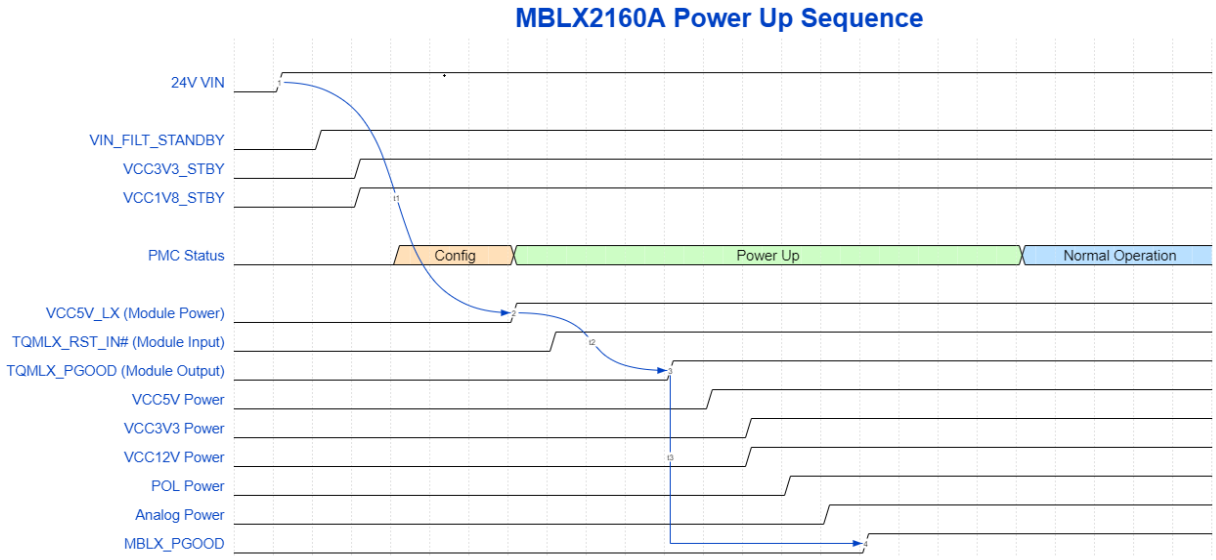


Figure 6: MBLX2160A Power-up sequencing

Typical sequence times are:

t1: 600 … 900 ms
t2: 300 … 500 ms
t3: 60 … 220 ms

3.2.3 Battery

In case of power failure or power down a lithium battery type CR2032 on the MBLX2160A supplies the RTC on the TQMLX2160A via pin VBAT_RTC (X3-B95), which can be supplied with 2.1 V to 3.7 V, typical 3.0 V.

VBAT_RTC is also routed to X31-16 on the MBLX2160A. This pin can be used as a measuring point or, if the Coin Cell is removed, as a feed point.

3.3 Clock generation

SYSCLK and DDRCLK are generated on the TQMLX2160A. Therefore the following clocks must be applied externally:

- SerDes clocks
- ECx Ethernet clocks

The clocks depend on the chosen SerDes protocol, see following table:

Table 9: Valid SerDes RCW Encodings and Reference Clocks

SerDes protocol (given lane)	Valid Reference Clock Frequency	Valid setting as determined by SRDS_PRTCL_S*n*	Valid setting as determined by SRDS_PLL_REF_CLK_SEL_S*n*	Valid setting as determined by SRDS_DIV_*_S*n*
High Speed Serial Interfaces				
PCI Express (2.5 Gbps) (doesn't negotiate upwards)	100 MHz	Any PCIe	0: 100 MHz	11: 2.5 Gbps
	125 MHz		1: 125 MHz	
PCI Express (5 Gbps) (can negotiate up to 5 Gbps)	100 MHz	Any PCIe	0: 100 MHz	10: 5 Gbps
	125 MHz		1: 125 MHz	
PCI Express (8 Gbps) (can negotiate up to 8 Gbps)	100 MHz	Any PCIe	0: 100 MHz	01: 8 Gbps
	125 MHz		1: 125 MHz	
PCI Express (16 Gbps) (can negotiate up to 16 Gbps)	100 MHz	Any PCIe	0: 100 MHz	00: 16 Gbps
	125 MHz		1: 125 MHz	
SATA (1.5, 3 or 6 Gbps)	100 MHz	Any SATA	0: 100 MHz	Don't care
	125 MHz		1: 125 MHz	
Networking interfaces				
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps	0: 100 MHz	Don't care
	125 MHz		1: 125 MHz	
USXGMII/XFI, 40 GE (each lane: 10.3125 Gbaud)	156.25 MHz	USXGMII/XFI, 40 GE @ 10.3125 Gbaud	0: 156.25 MHz	Don't care
	161.1328125 MHz		1: 161.1328125 MHz	
25 GE, 50 GE, 100 GE (each lane: 25.78125 Gbaud)	161.1328125 MHz	25 GE, 50 GE, 100 GE @ 25.78125 Gbaud	0: 161.1328125 MHz	Don't care

The MBLX2160A is designed for the configuration 0b00:

- For 1.25, 2.5, 3, 5, 6, 8 or 16 GHz protocols: 100 MHz
- For 3.125 or 6.25 GHz protocols: 125 MHz
- For 10.3125 GHz protocols: 156.25 MHz
- For 25.78125 GHz protocols: 161.1328125 MHz

The following SerDes clocks are used:

- PCIe 100 MHz (for requirements according to Gen 3)
- SGMII 100 MHz
- SATA 100 MHz
- XFI 156.25 MHz
- CAUI-4 161.1328125 MHz
- RGMII ECx_GTX_CLK125 125 MHz

3.3 Clock generation (continued)

Two programmable clock drivers are provided on the MBLX2160A for the clock structure.

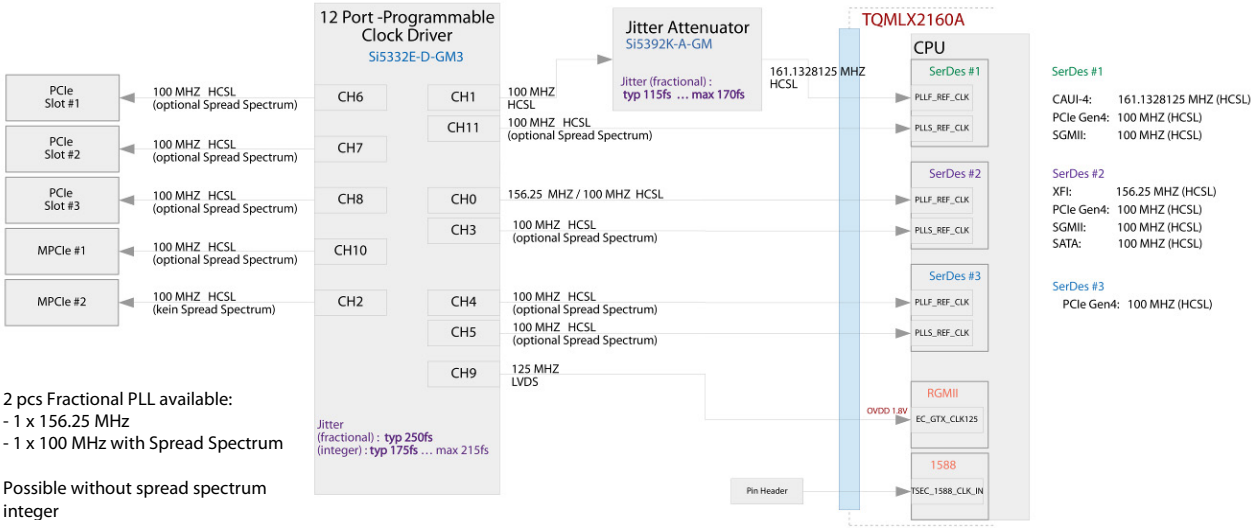


Figure 7: Clock distribution on the MBLX2160A

Both clock drivers are connected to the LX2160A via I2C1.
A reference clock of 125 MHz is required for the RGMII Ethernet interfaces on EC1 and EC2.
On the TQMLX2160A the clock signal is differentially routed to an LVDS receiver.

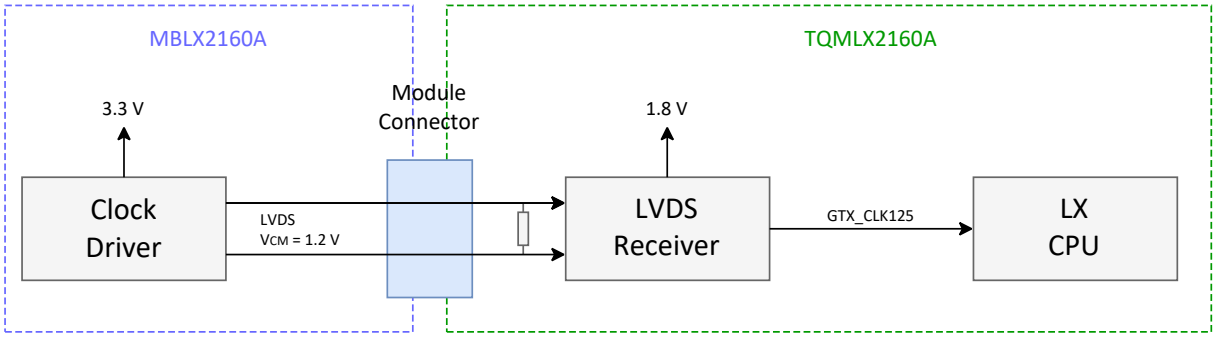


Figure 8: LVDS receiver

LVDS is terminated with 100 Ω on the TQMLX2160A.

3.4 I2C devices

The TQMLX2160A provides up to six I²C buses, of which I2C1, I2C5 and I2C6 are used on the MBLX2160A.
The following block diagram shows the I²C bus structure:

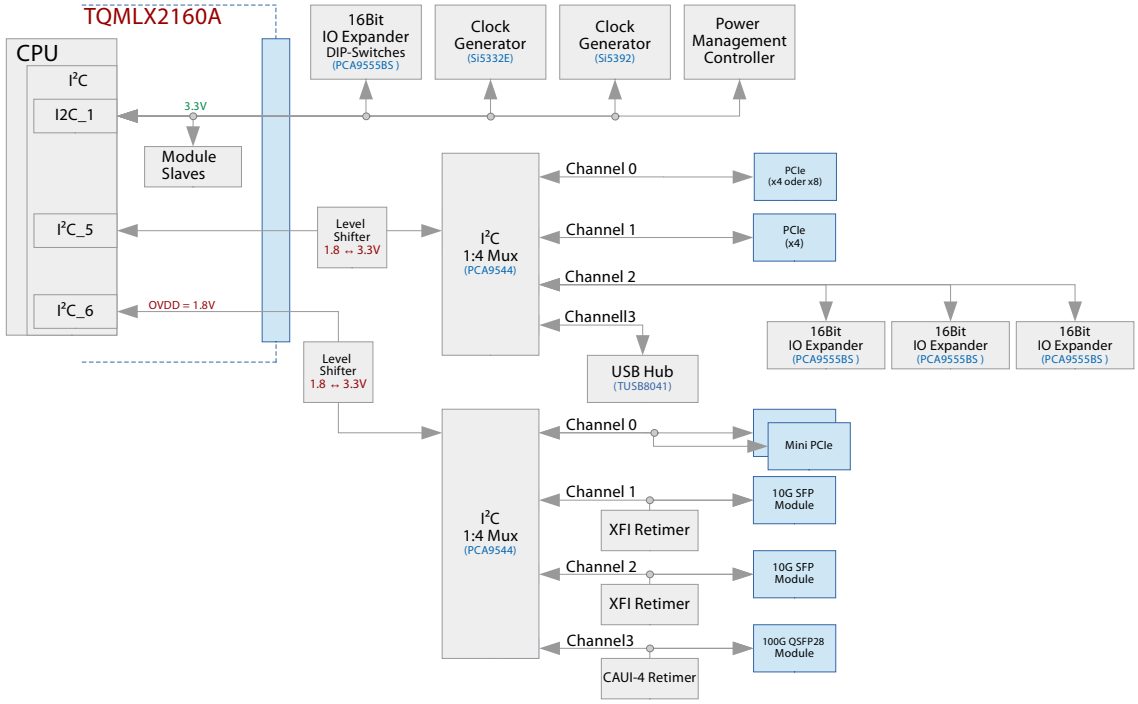


Figure 9: Block diagram I²C buses

On the TQMLX2160A further I²C devices are used, therefore the already assigned I²C addresses were taken into account.

Table 10: I²C devices, address mapping, MBLX2160A

I²C bus	Device	Function	7-bit address	8-bit address	Remark
I2C1	STM32L471VET6	PMC	0x04	0x08	D77
	PCA9555S	GPIO Expander	0x20	0x40	D20
	SI5392K-A-GM	Clock Generator	0x68	0xD0	D8
	SI5332F-D-GM3	Clock Generator	0x6A	0xD4	D7
I2C5	PCA9555S	GPIO Expander	0x20	0x40	D20
	PCA9555S	GPIO Expander	0x21	0x42	D21
	PCA9555S	GPIO Expander	0x22	0x44	D22
	TUSB8041I	USB Hub	0x44	0x88	D26
	PCA9544ABS	I2C Multiplexer	0x70	0xE0	D4
	PCIe slot	PCIe 1	–	–	Connectors X35, X37
	PCIe slot	PCIe 2	–	–	Connector X36
I2C6	DS110DF111SQ	XFI1 Retimer	0x19	0x32	D1
	QSFP slot	XFI1 QSFP module			Connector X8
	DS110DF111SQ	XFI2 Retimer	0x1B	0x36	D2
	QSFP slot	XFI2 QSFP module			Connector X9
	DS250DF410ABM	CAUI4 Retimer 1	0x20	0x40	D24
	DS250DF410ABM	CAUI4 Retimer 2	0x21	0x42	D25
	PCA9544ABS	I2C Multiplexer	0x70	0xE0	D3
	mPICe slot	mPCIe	–	–	Connectors X16, X17
	QSFP28 slot	QSFP28 module	–	–	Connector X29

3.5 SerDes

3.5.1 SerDes Multiplexing options

The LX2160A provides three SerDes blocks with eight lanes each.
No AC coupling capacitors are assembled on the TQMLX2160A. These have to be populated on the carrier board.
The following tables show the SerDes multiplexing options.

Table 11: SerDes Block 1 multiplexing options

	Front Side Left SERDES1 (×8)							
	0	1	2	3	4	5	6	7
	H	G	F	E	D	C	B	A
1	PCIe.1 ×4				PCIe.2 ×4			
2	SGMII.3	SGMII.4	SGMII.5	SGMII.6	PCIe.2 ×4			
3	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 ×4			
4	SGMII.3	SGMII.4	SGMII.5	SGMII.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10
5	PCIe.1 ×4				USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
6	USXGMII / XFI.3	USXGMII / XFI.4	SGMII.3	SGMII.3	SGMII.7	SGMII.8	SGMII.9	SGMII.10
7	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10
8	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
9	PCIe.1 ×1	SGMII.4	SGMII.5	SGMII.6	PCIe.2 ×1	SGMII.8	SGMII.9	SGMII.10
10	PCIe.2 ×1 (gen 1,2)	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 ×1 (gen 1,2)	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
11	PCIe.1 ×2		SGMII.5	SGMII.6	PCIe.2 ×2		SGMII.9	SGMII.10
12	PCIe.1 ×4				PCIe.2 ×2		SGMII.9	SGMII.10
13	100GE.1				100GE.2			
14	100GE.1				PCIe.2 ×4			
15	50GE.1		50GE.2		PCIe.2 ×4			
16	50GE.1		25GE.5	25GE.6	PCIe.2 ×4			
17	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 ×4			
18	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
19	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	40GE.2			
20	40GE.1				40GE.2			
21	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 ×2		25GE.9	25GE.10
22	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 ×2		USXGMII / XFI.9	USXGMII / XFI.10

Table 12: SerDes Block 2 multiplexing options

	Front Side Right SERDES2 (×8)							
	0	1	2	3	4	5	6	7
	A	B	C	D	E	F	G	H
1	PCIe.3 ×2 (gen 1,2)		SATA.1	SATA.2	PCIe.4 ×4 (gen 1,2)			
2	PCIe.3 ×8							
3	PCIe.3 ×4				PCIe.4 ×4			
4	PCIe.3 ×4 (gen 1,2)				PCIe.4 ×2 (gen 1,2)		SATA.1	SATA.2
5	PCIe.3 ×4				SATA.3	SATA.4	SATA.1	SATA.2
6	PCIe.3 ×4 (gen 1,2)				SGMII.15	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14
7	PCIe.3 ×1 (gen 1,2)	SGMII.12	SGMII.17	SGMII.18	PCIe.4 ×1 (gen 1,2)	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14
8	X	X	SATA.1	SATA.2	SATA.3	SATA.4	USXGMII / XFI.13	USXGMII / XFI.14
9	SGMII.11	SGMII.12	SGMII.17	SGMII.18	SGMII.15	SGMII.16	SGMII.13	SGMII.14
10	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.2 ×4			
11	PCIe.3 ×1	SGMII.12	SGMII.17	SGMII.18	PCIe.4 ×1	SGMII.16	SGMII.13	SGMII.14
12	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.4 ×2 (gen 1,2)		SATA.1	SATA.2
13	PCIe.3 ×4				PCIe.4 ×2		SGMII.13	SGMII.14
14	PCIe.3 ×2		SGMII.17	SGMII.18	PCIe.4 ×2		SGMII.13	SGMII.14

Table 13: SerDes Block 3 multiplexing options

	Back Side SERDES3 (×8)							
	0	1	2	3	4	5	6	7
	A	B	C	D	E	F	G	H
1	PCIe.5 ×8							
2	PCIe.5 ×4				PCIe.6 ×4			

3.5.2 SerDes #1

The following multiplexing options are used on the MBLX2160A:

- Multiplexing 14 (1 × 100 Gbit Eth + 1 × PCIe ×4)
- Multiplexing 12 (1 × PCIe ×2 + 2 × SGMII Gbit Eth)

Lanes 0–3 cannot be used with multiplexing 12, since the CAUI-4 interface is used exclusively for the 100 Gbit Ethernet.

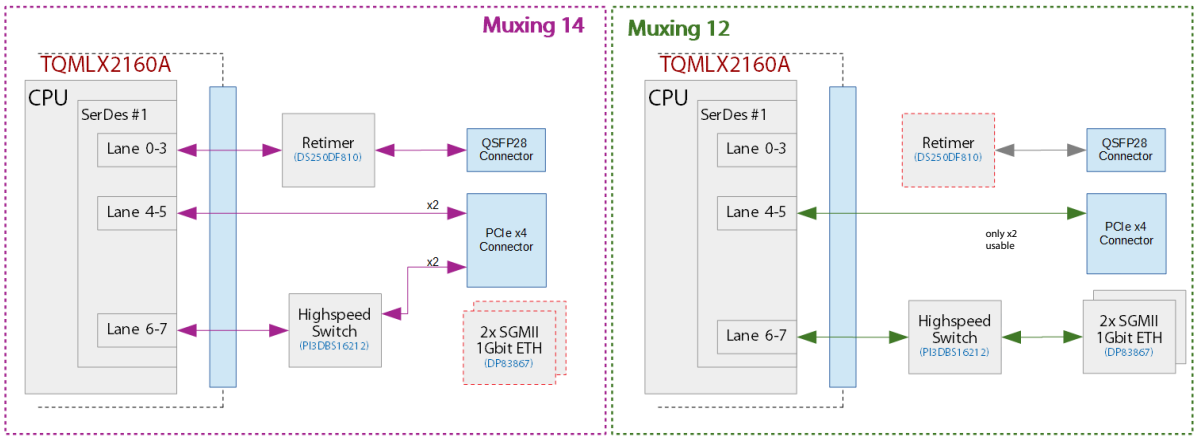


Figure 10: SerDes #1 multiplexing options

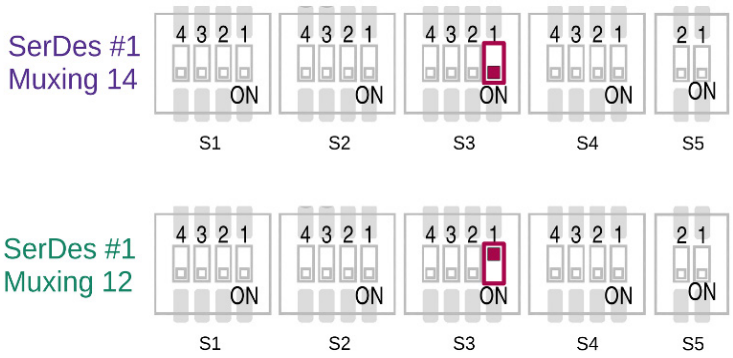


Figure 11: DIP switch setting for SerDes #1

The current setting can be shown in the status display under "Settings" -> "Serdes 1", e.g.:

Figure 12: Information about Serdes 1 can be displayed with the Status Display.

3.5.3 SerDes #2

The following multiplexing options are used on the MBLX2160A:

- Multiplexing 7 (2 × PCIe ×1 + 4 × 1 Gbit Ethernet + 2 × 10 Gbit Ethernet)
- Multiplexing 8 (3 × SATA + 2 × 10 Gbit Ethernet)
- Multiplexing 11 (2 × PCIe ×1 + 6 × 1 Gbit Ethernet)

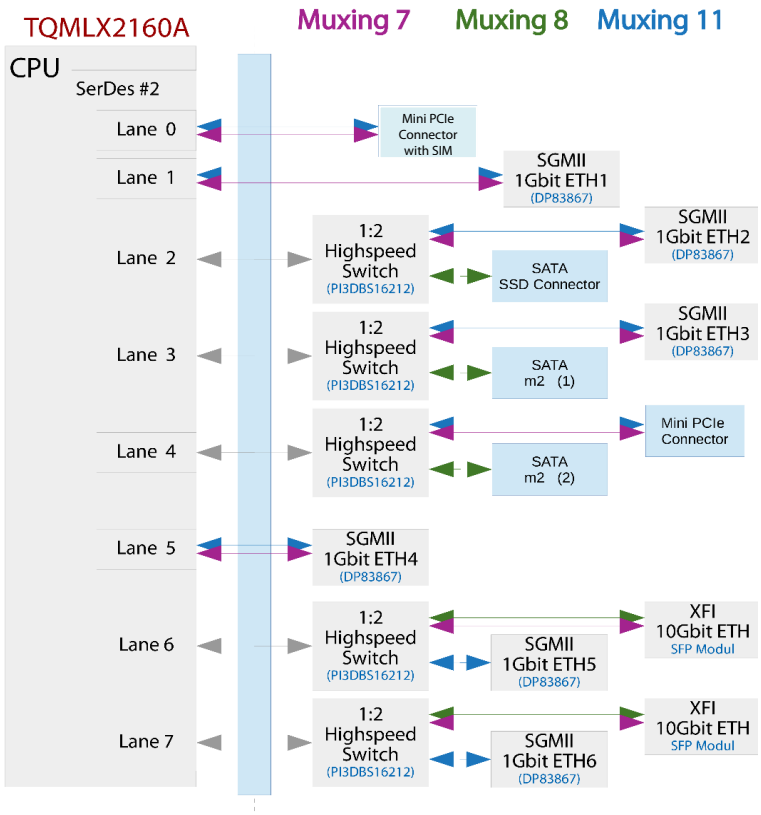


Figure 13: SerDes #2 multiplexing options

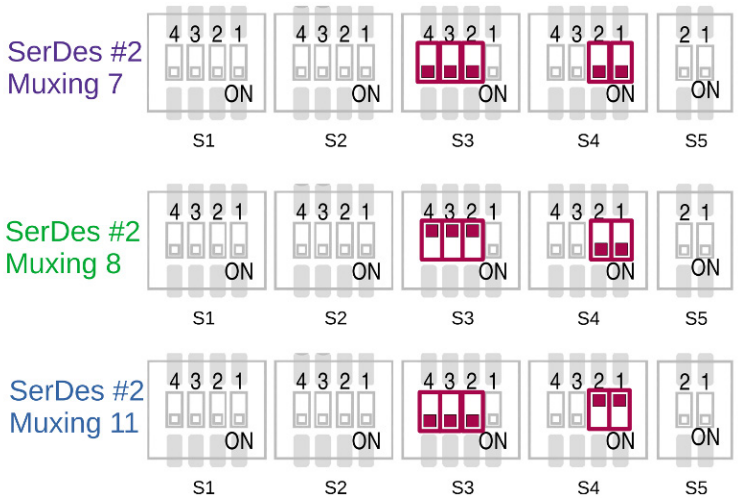


Figure 14: DIP switch setting for SerDes #2

3.5.4 SerDes #3

The following multiplexing options are possible on the MBLX2160A:

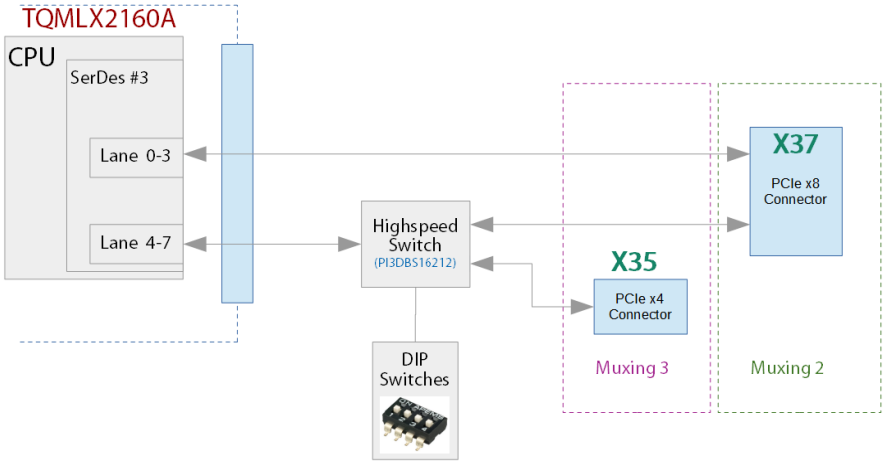


Figure 15: SerDes #3 multiplexing options

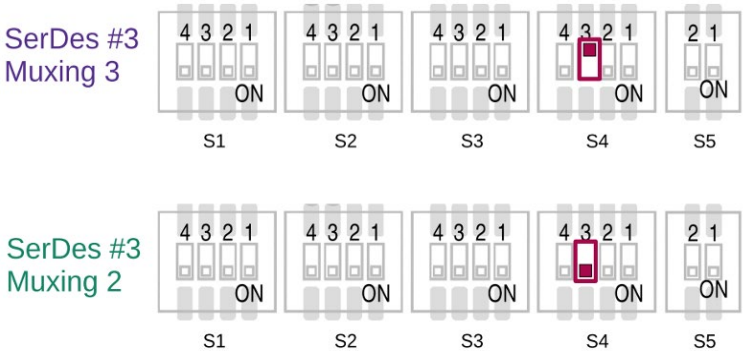


Figure 16: DIP switch setting for SerDes #3

3.6 QSFP28 100 Gbit Ethernet

For the 100 Gbit Ethernet the SerDes #1 interface (multiplexing 14) with CAUI-4 interface is used on the MBLX2160A. Only optical media are still suitable for transmission. Similar to the implementation for the XFI 10 Gbit Ethernet with SFP modules, there are modules for 100 Gbit Ethernet, according to the QSFP28 standard.

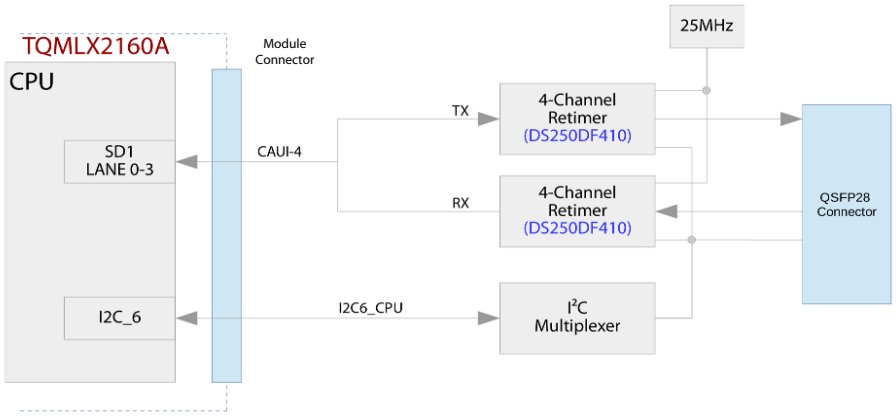


Figure 17: QSFP28 interface

I2C configuration via I2C_6:

- Retimer D25 address 0x42
- Retimer D24 address 0x40

The retimers must be configured at startup. (Is taken over by U-Boot)

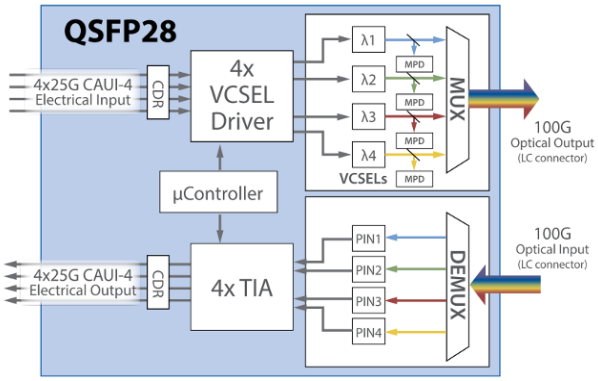


Figure 18: Block diagram QSFP28 module

Figure 19: QSFP28 module

The pinout of the QSFP28 connector is standardized:

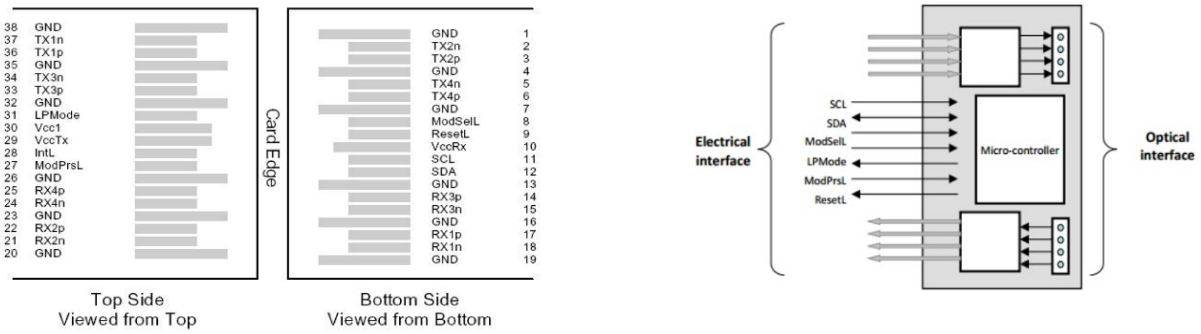


Figure 20: Pinout QSFP28

Clock supply of the retimers via 25 MHz oscillator

I²C configuration via I2C_6 and multiplexer

- Retimer D25 address 0x42
- Retimer D24 address 0x40

The retimers must be configured at start-up. (Taken over by the U-Boot)

3.7 SFP+ 10 Gbit Ethernet

Two SFP+ slots are available on the MBLX2160A. These are intended for 10 Gbit Ethernet. According to the multiplexing of SerDes block #2 (see 3.8.3) the slots with the XFI interface can only be used with muxing 7 + 8.

Both SFP+ slots on the MBLX2160A are designed identically and feature a retimer between module and SFP+ slot. A two-piece QSFP+ connector system is used.

- XFI 1
  - Reference D1
  - SFP+ Connector X8
  - Configurable via I2C_XFI_1 / Slave address 0x33
  - SD2 Lane 6
  - Reference clock via REF_CLK_XFI_1 (G13)
  - IO control signals controllable via GPIO port expander

- XFI 2
  - Reference D2
  - SFP+ Connector X9
  - Configurable via I2C_XFI_2 / Slave address 0x37
  - SD2 Lane 7
  - Reference clock via REF_CLK_XFI_2 (G14)
  - IO control signals controllable via GPIO port expander

3.8 RGMII / SGMII Ethernet

Ten individual 1-Gbit Ethernet interfaces are available on the MBLX2160A. However, not all of them can be used at the same time, but depending on the SerDes multiplexing, see chapter 3.5.

ETH9 and ETH10 are connected to the LX2160A via RGMII. ETH10 offers the option of using IEEE 1588 control signals instead of the RGMII interface. For this purpose, a switch is installed.

The two bidirectional switches are switched together via a DIP switch, see chapter 3.10.4. The signals are available collectively at pin header X32.

The following illustration shows the ETH sockets as well as the dependence on multiplexing. The designations ETH1...ETH10 correspond to the signal naming in the circuit diagram of the MBLX2160A.

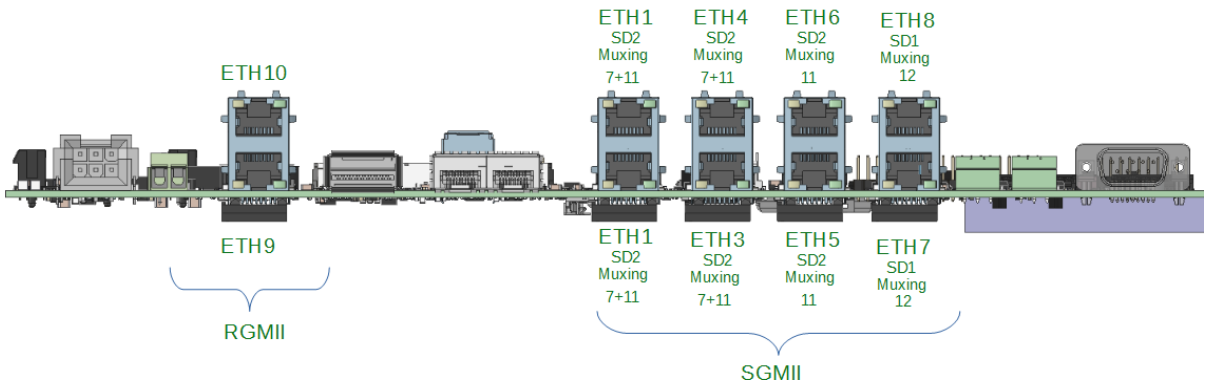


Figure 21: Ethernet sockets ETH1 to ETH10

In principle, all Ethernet interfaces have an identical structure.

- Ethernet TI DP83867 PHY (connection via SGMII or RGMII)
- Stacked ETH sockets with two LEDs each (green / orange)
- 10/100/1000 magnetics 749020010A
- Individual reset signal, can be controlled via GPIO port expander
- Individual 25 MHz reference source with quartz

The LED control can be set individually:

- Green LED: Connected to port LED_0, Low Active control
- Orange LED: Connected to Port LED_1, Low Active control

The PHYs have the following addresses on the MDIO bus:

Table 14: MDIO addresses

MDIO bus	Ethernet	PHY – Ref ID	Socket	Address
EMI_1	ETH1	D27	X10-A	0001
	ETH2	D29	X10-B	0010
	ETH3	D31	X11-A	0011
	ETH4	D32	X11-B	0100
	ETH5	D28	X12-A	0101
	ETH6	D34	X12-B	0110
EMI_2	ETH7	D35	X13-A	0001
	ETH8	D33	X13-B	0010
	ETH9	D30	X14-A	0011
	ETH10	D36	X14-B	0100

ETH9 and ETH10 are connected to the CPU via RGMII. At ETH10 there is the option to use the IEEE 1588 control signals instead of the RGMII interface. For this reason switches were installed. The two bidirectional switches are switched together via a DIP switch (see 3.10.4).

The signals are available collected at pin header X32:

Table 15: Pinout 20-pin header, X32

Signal	Pin		Signal
EC2_1588_TRIGIN2	1	2	SE_14443_LA
EC2_1588_PULSEO1	3	4	SE_14443_LB
EC2_1588_CLK_IN	5	6	DGND
EC2_1588_PULSEO2	7	8	SE_7816_IO1
EC2_1588_CLK_OUT	9	10	SE_7816_IO2
EC2_1588_ALARMO1	11	12	SE_7816_CLK
EC2_1588_ALARMO2	13	14	SE_7816_RST#
EC2_1588_TRIGIN1	15	16	DGND
DGND	17	18	TB_SCAN_EN#
DGND	19	20	DGND

3.9 Communication interfaces

All unspecified signals have a single-ended impedance of nominal 50 Ω ± 10 %.
Depending on the interface, other impedances are also used on the MBLX2160A.

Table 16: MBLX2160A interface impedances

Interface	Impedance TQMLX2160A	Recommendation for carrier board
USB 3.0	90 Ω, differential	85 Ω ±15 %, differential
SerDes 1	100 Ω, differential	100 Ω ±10 %, differential
SerDes 2	100 Ω, differential	100 Ω ±10 %, differential
SerDes 3	90 Ω, differential	90 Ω ±15 %, differential

The layout guidelines of the respective standards are to be taken note of for the mainboard design.

FR-4 is used as PCB material for the MBLX2160A. Therefore the track lengths of the SerDes signals and the estimated insertion losses have to be taken into consideration. The insertion losses are estimated as follows:

- PCIe Gen 3 (4 GHz): 0.75 dB/Inch
- XFI (5.17 GHz): 0.85 dB/Inch
- CAUI (12.9 GHz): 2 dB/Inch

3.9.1 PCIe

There are 3 PCIe slots assembled on the MBLX2160A.

- 2 × PCIe ×4 (X35 and X36)
- 1 × PCIe ×8 (X37)

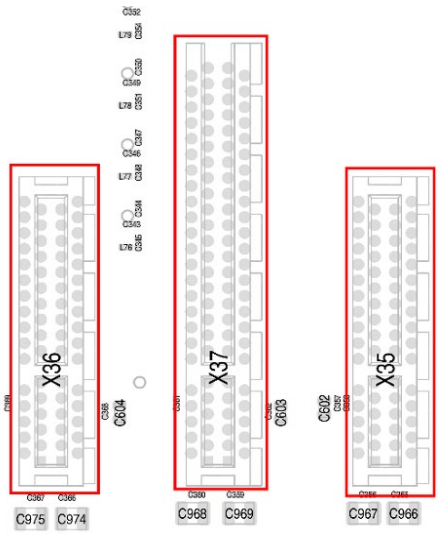


Figure 22: PCIe slots arrangement

These three interfaces depend on the multiplexing and are not available without restrictions.
As described in chapter 3.5.1 the following options are possible:

- **PCIe ×4, X35:**
  - o ×4 via SerDes #3 with muxing 3

- **PCIe ×4, X36:**
  - o ×4 via SerDes #1 with muxing 14
  - o ×2 via SerDes #1 with muxing 12

- **PCIe ×8, X37:**
  - o ×8 via SerDes #3 with muxing 2
  - o ×4 via SerDes #3 with muxing 3

3.9.2 Mini PCIe

The MBLX2160A provides two Mini PCIe slots, each with one PCIe lane (×1) for full-size cards (50.95 mm × 30 mm).

- mPCIe ×1, X16 plus SIM card holder
- mPCIe ×1, X17

Any standard compliant Mini PCIe card can be used.
As described in chapter 3.5.1, these are available at SerDes #2 with muxing 7 and 11.

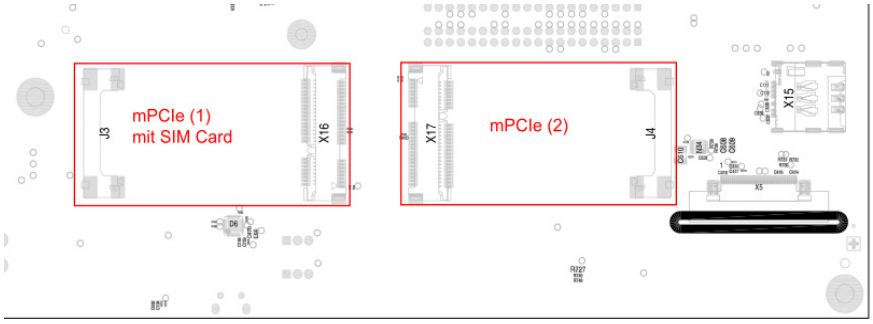


Figure 23: Position of mPCIe slots and SIM card holder

3.9.3 SD card

The SD card socket on the MBLX2160A is connected via a 4-bit data interface to the SDHC1 controller of the TQMLX2160A.
The SD card is supplied with 3.3V. This voltage is generated by the module and is toggled at each reset. Card Detect is supported.
The I/O voltage can be dynamically switched from 3.3V to 1.8V at runtime via SDHC1_DATA4. High-speed mode is supported.

Table 17: Pinout SD card, X44

Pin	Signal	Remark
1	SDHC1_DATA2_R	10 kΩ PU to 3.3 V + ESD protection
2	SDHC1_DATA3_R	10 kΩ PU to 3.3 V + ESD protection
3	SDHC1_CMD_R	10 kΩ PU to 3.3 V + ESD protection
4	VCC3V3	VCC3V3_LX_OUT
5	SDHC1_CLK	ESD protection
6	DGND	–
7	SDHC1_DATA0_R	10 kΩ PU to 3.3 V + ESD protection
8	SDHC1_DATA1_R	10 kΩ PU to 3.3 V + ESD protection
SW1	SDHC1_CD#	10 kΩ PU to 1.8 V + ESD protection
SW2	DGND	–
M1 … M4	SHIELD	Shield

Note: LX2160A Erratum A-011552	
	Due to CPU Erratum A-011552 a SD Card level converter must be added to the SDHC interface. The adapter board MBLX2160A-SDMOD is part of the shipment of the MBLX2160A and contains the level converter and the SD card connector.

3.9.4 SATA

The following SATA options are possible on the MBLX2160A:

- 2 × SATA M.2
- 1 × SATA for 2.5" SSD

As described in chapter 3.5.1, SATA is available at SerDes #2 with muxing 8.
The M.2 slots with B-Key on the MBLX2160A support M.2 sizes 2242 and 2280. The default mounting is for type 2280.
The third SATA interface on X18 is designed for a standard 2.5" SSD. The pinout and the connectors are standard compliant.
The implementation on the MBLX2160A is as shown in the following illustration:

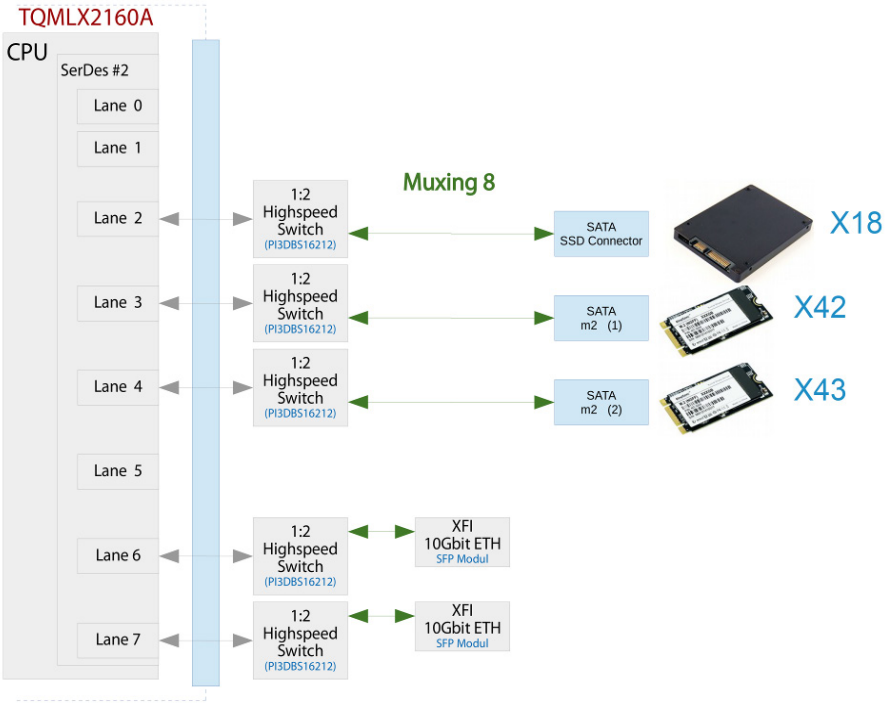


Figure 24: SATA interfaces on the MBLX2160A

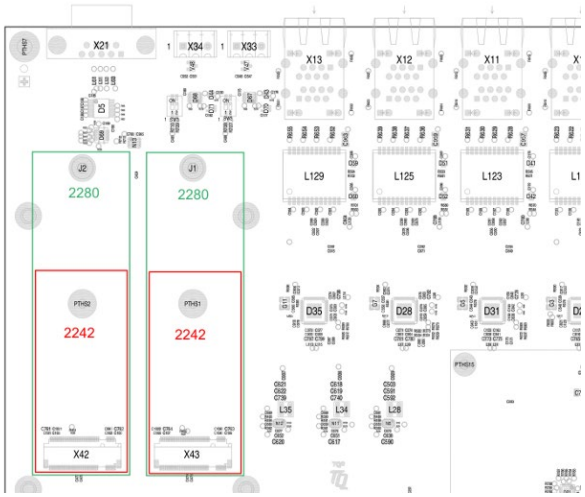


Figure 25: Position of SATA ports

3.9.5 USB 3.0

The TQMLX2160A provides two USB 3.0 controller with integrated PHYs.

Both controllers support:

- SuperSpeed (5 Gbps)
- Hi-Speed (480 Mbps)
- Full- and Low Speed

A 4-port USB 3.0 hub is used on the board, which is connected to USB1. Two USB 3.0 ports are available via Type-A sockets. USB2 is used as OTG interface. A Micro USB 3.0 TYPE B socket is available. In order to use the interface as Host/Device, a suitable adapter comes with the MBLX2160A in the Starterkit-Set STKLX2160A.

Each USB port has its own switched and overcurrent protected VBUS power supply.

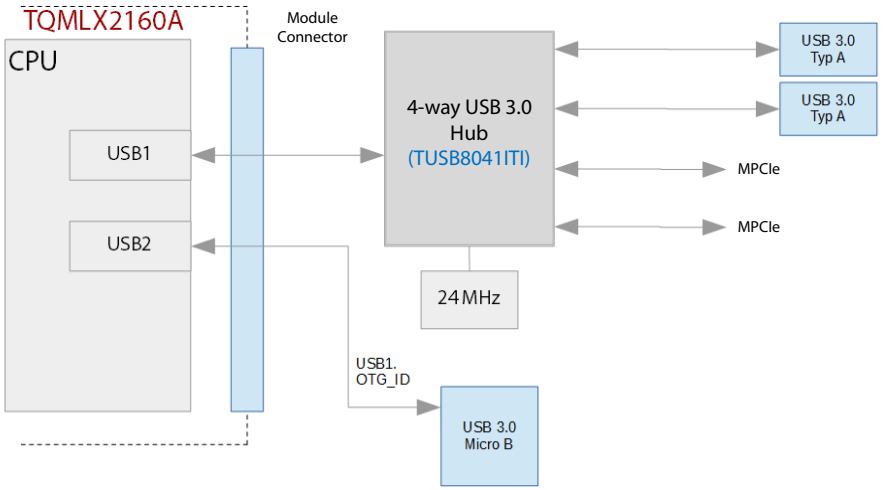


Figure 26: Block diagram USB

The following figure shows the OTG detection for the USB3.0 Micro B connector.

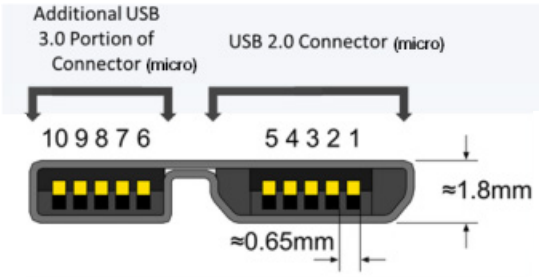


Figure 27: Pinout USB 3.0 Micro connector (source Amphenol ICC)

Table 18: Pinout USB 3.0 Micro B OTG connector

Pin	Pin name	Remark
1	VBUS	+5 V
2	USB D–	USB 2.0 differential pair
3	USB D+	USB 2.0 differential pair
4	OTG ID	USB OTG ID for identifying lines
5	GND	Ground
6	USB3 SSTX–	USB 3.0 signal transmission line
7	USB3 SSTX+	USB 3.0 signal transmission line
8	GND	Ground
9	USB3 SSRX–	USB 3.0 signal receiving line
10	USB3 SSRX+	USB 3.0 signal receiving line

3.9.6 CAN

The LX2160A provides two internal CAN controllers, which support both the 2.0B standard and the CAN-FD protocol.
The interfaces are not galvanically isolated.

The muxing offers the following options:

- CAN1 or I2C_3 or GPIO
- CAN2 or I2C_4 or GPIO

The I/O reference voltage is 1.8 V. The I/O signals of the transceivers are fed through a level shifter 1.8V ⇔ 3.3V. A 120 Ω split termination is provided; this can be switched off via a DIP switch. The CAN signals are ESD protected.
CAN1 and CAN2 can be individually terminated by DIP switch, so that either the CAN interfaces or the muxing options I2C3 and I2C4 can be used. These are routed to a pin header.

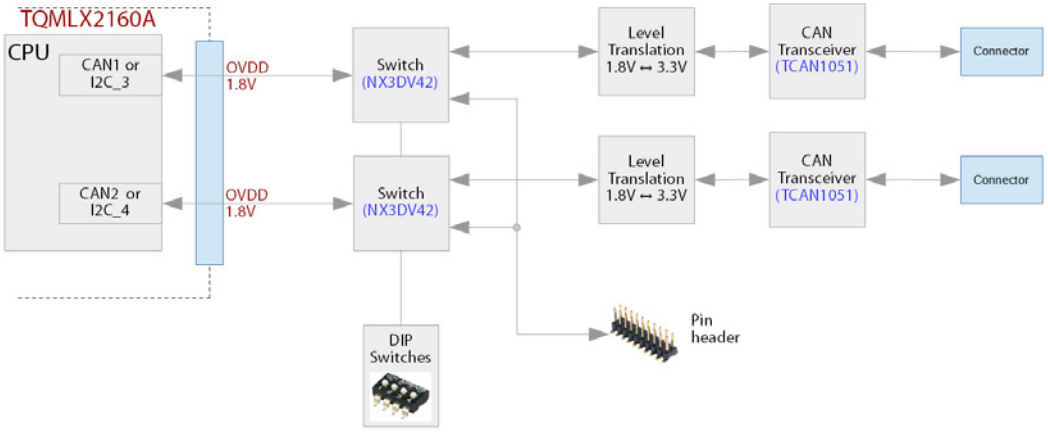


Figure 28: Block diagram CAN

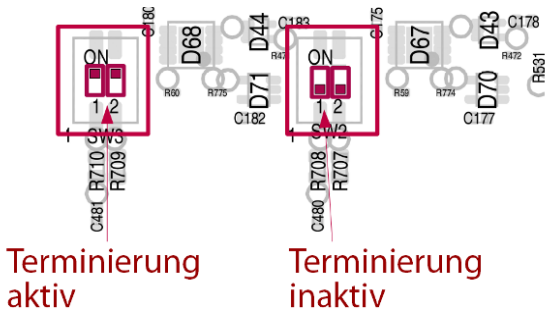


Figure 29: CAN termination DIP switches

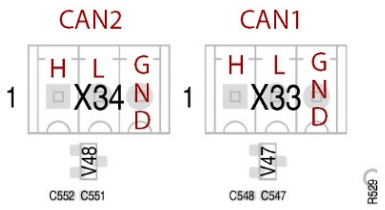


Figure 30: CAN connector pinout

3.9.7 UART

The LX2160A provides four UART interfaces with Rx/Tx signals, or two UART interfaces when the handshake signals are used.

On the MBLX2160A, one UART is connected as RS-232 to a D-Sub-9 connector, which serves as the primary console. The data rate for the console outputs is 115200 baud.

The RS-232 SP3232EEY transceiver signals are routed through a 1.8V ⇔ 3.3V level shifter.

The UART signals UART2, UART3 and UART4, or the handshake signals, are routed directly to a pin header. The handshake lines are routed to the RS-232 D-Sub-9 connector via 0 Ω resistors. Additionally, all UART signals are routed to pin header X27.

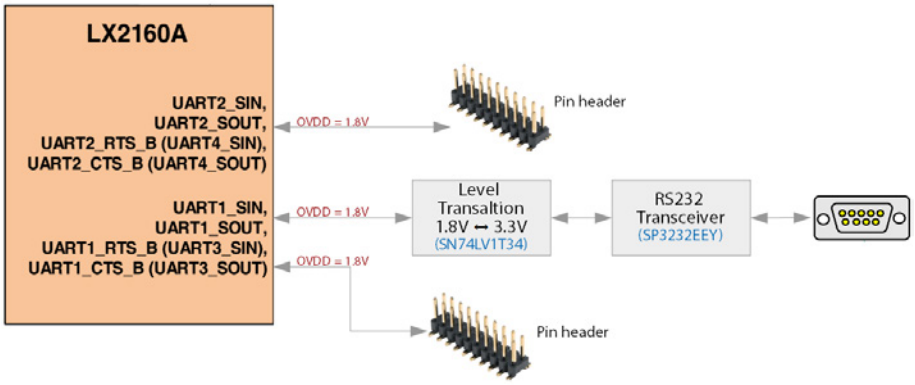


Figure 31: Block diagram UART with RS-232

3.9.8 GPIO port expanders

Four GPIO expanders are provided on the MBLX2160A. Three are accessible via I²C bus I2C_5_MUX_CH2, the fourth via I2C_1.

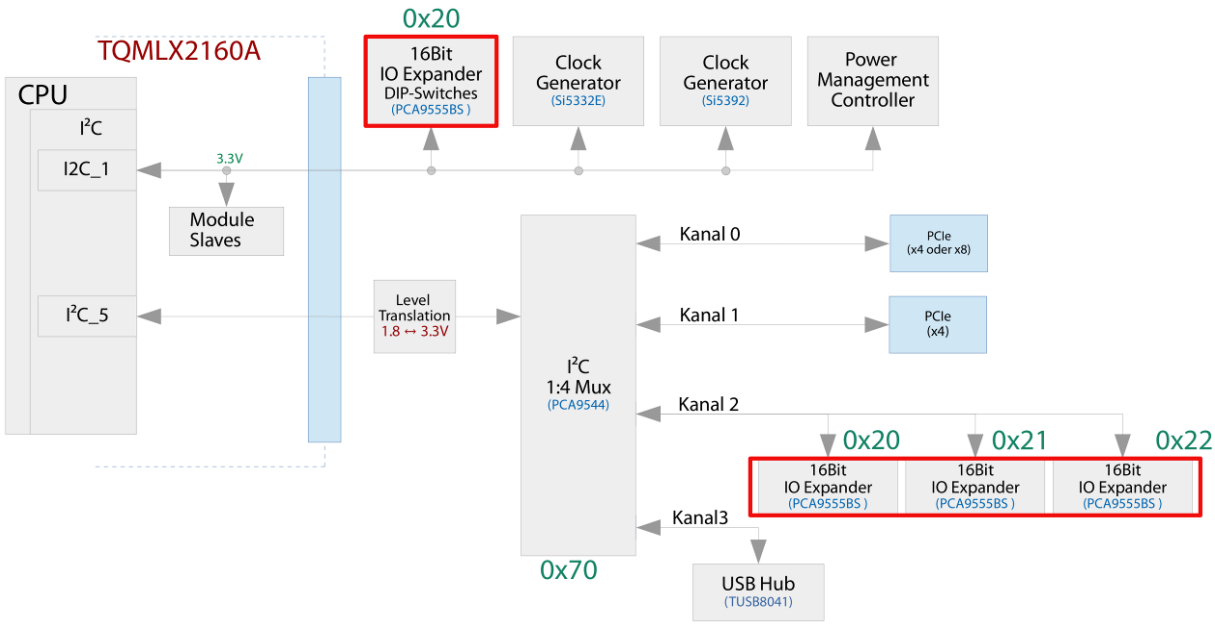


Figure 32: Block diagram GPIO expander at the I2C buses

3.9.9 GPIO (continued)

Table 19: GPIO port expander signals

Reference	7-bit address	Port	Signal	Function block
D20	0x20	IO0_0	QSFP_MODSEL	100G - QSFP module
		IO0_1	QSFP_RESET#	
		IO0_2	QSFP_PODPRS#	
		IO0_3	QSFP_INT#	
		IO0_4	QSFP_LPMODE	
		IO0_5	IRQ_RETIMER_1#	
		IO0_6	IRQ_RETIMER_2#	
		IO0_7	MPCIE_1_WAKE#	mPCIe #1
		IO1_0	MPCIE_1_DISABLE#	
		IO1_1	MPCIE_1_RESET#	
		IO1_2	MPCIE_2_WAKE#	mPCIe #2
		IO1_3	MPCIE_2_DISABLE#	
		IO1_4	MPCIE_2_RESET#	
		IO1_5	EN_SILENT_CAN1	CAN
		IO1_6	EN_SILENT_CAN2	
		IO1_7	SIM_CARD_DETECT	mPCIe #1
D21	0x21	IO0_0	RESET_USB_HUB#	USB HUB
		IO0_1	RESET_ETH1	Ethernet
		IO0_2	RESET_ETH2	
		IO0_3	RESET_ETH3	
		IO0_4	RESET_ETH4	
		IO0_5	RESET_ETH5	
		IO0_6	RESET_ETH6	
		IO0_7	RESET_ETH7	
		IO1_0	RESET_ETH8	
		IO1_1	RESET_ETH9	
		IO1_2	RESET_ETH10	
		IO1_3	CAN1_SEL	CAN
		IO1_4	CAN2_SEL	
		IO1_5	RST_M2_SATA_1	SATA
		IO1_6	RST_M2_SATA_2	
		IO1_7	EN_USER_LED_2	USER_LED
D22	0x22	IO0_0	XFI1_TX_FAULT	XFI1
		IO0_1	XFI1_TX_DIS	
		IO0_2	XFI1_MOD_DETECT	
		IO0_3	XFI1_RX_LOSS	
		IO0_4	XFI2_TX_FAULT	
		IO0_5	XFI2_TX_DIS	XFI2
		IO0_6	XFI2_MOD_DETECT	
		IO0_7	XFI2_RX_LOSS	
		IO1_0	XFI1_RET_LOSS	
		IO1_1	XFI2_RET_LOSS	
		IO1_2	PCIE_1_PERST#	PCIe
		IO1_3	PCIE_2_PERST#	
		IO1_4	PCIE_WAKE#	
		IO1_5	X8_PRSNT1#	
		IO1_6	X4_1_PRSTN1#	
		IO1_7	X4_2_PRSNT1#	
D23	0x20	IO0_0	NOR_SWAP#	See chapter 3.10.4
		IO0_1	BOOT_SRC2	
		IO0_2	BOOT_SRC1	
		IO0_3	BOOT_SRC0	
		IO0_4	EMMC_SEL1	
		IO0_5	EMMC_SEL0	
		IO0_6	SD2_4_MUX_SEL	
		IO0_7	SD2_3_MUX_SEL	
		IO1_0	SD2_2_MUX_SEL	
		IO1_1	SD1_MUX_SEL	
		IO1_2	ENABLE_FAN	
		IO1_3	SD3_MUX_SEL	
		IO1_4	SD2_7_MUX_SEL	
		IO1_5	SD2_6_MUX_SEL	
		IO1_6	–	
		IO1_7	EC2_SEL	

3.9.9 Headers

On the MBLX2160A four pin headers are installed, whose signals are grouped as shown below:

- Supply voltages: X31
- CPU signals after muxing: X27, X28
- Module debug signals: X30

Table 20: Pinout 40-pin header, X27

Signal	Pin		Signal
UART1_SOUT	1	2	SDHC2_DATA0
UART1_SIN	3	4	SDHC2_DATA1
UART2_SOUT	5	6	SDHC2_DATA2
UART2_SIN	7	8	SDHC2_DATA3
DGND	9	10	SDHC2_DATA4
UART3_SOUT	11	12	SDHC2_DATA5
UART3_SIN	13	14	SDHC2_DATA6
UART4_SOUT	15	16	SDHC2_DATA7
UART4_SIN	17	18	SDHC2_CMD
DGND	19	20	SDHC2_DS
CAN2_TX_MUX	21	22	SDHC2_CLK
CAN2_RX_MUX	23	24	SDHC1_CD#
CAN1_TX_MUX	25	26	SDHC1_WP
CAN1_RX_MUX	27	28	SDHC1_DS
DGND	29	30	DGND
RTC_CLKOUT	31	32	SDHC1_DATA4
(NC)	33	34	SDHC1_DATA5
TA_TMP_DETECT#	35	36	SDHC1_DATA6
TA_BB_TMP_DETECT	37	38	SDHC1_DATA7
DGND	39	40	DGND

Table 21: Pinout 40-pin header, X28

Signal	Pin		Signal
GPIO3_DATA08	1	2	IRQ_0
GPIO3_DATA09	3	4	IRQ_1
GPIO3_DATA10	5	6	IRQ_2
EVT0#	7	8	IRQ_3
DGND	9	10	DGND
EVT1#	11	12	IRQ_4
EVT2#	13	14	IRQ_5
EVT3#	15	16	IRQ_6
EVT4#	17	18	IRQ_7
DGND	19	20	DGND
EVENT_TEMPSENSOR#	21	22	INT_PORTEXPANDER#
EEPROM_WP	23	24	INT_I2C_MUX#
RTC_INT_OUT	25	26	I2C1_CPU_SCL
CLK_OUT	27	28	I2C1_CPU_SDA
DGND	29	30	DGND
HRESET_OUT#	31	32	LX_CONFIG_RFU2
LX_CPU_RESET_REQ_OUT#	33	34	LX_CONFIG_RFU3
LX_CPU_RESET_OUT#	35	36	LX_CONFIG_RFU4
TQMLX_RST_IN#	37	38	LX_CONFIG_RFU5
DGND	39	40	DGND

3.9.10 Headers (continued)

Table 22: Pinout 20-pin header, X30

Signal	Pin		Signal
SYSC_I2C_SCL	1	2	VCC3V3_STBY
SYSC_I2C_SDA	3	4	JTAG_CPLD_TCK
PMC_I2C_SCL	5	6	JTAG_CPLD_TMS
PMC_I2C_SDA	7	8	JTAG_CPLD_TDI
RESET_BUTTON	9	10	JTAG_CPLD_TDO
ON_OFF_BUTTON	11	12	TQMLX_MON_UART_RXD
EXT_POWER_FAIL_IN#	13	14	TQMLX_MON_UART_TXD
MBLX_PGOOD	15	16	TQMLX_SLEEP#
TQMLX_PGOOD	17	18	TQMLX_WAKE
DGND	19	20	DGND

Table 23: Pinout 20-pin header, X31

Signal	Pin		Signal
VCC12V	1	2	VCC12V
VCC12V	3	4	VCC12V
VCC5V	5	6	VCC5V
VCC5V	7	8	VCC5V
VCC3V3	9	10	VCC3V3
VCC3V3	11	12	VCC3V3
OVDD_LX_OUT	13	14	VCC3V3_LX_OUT
TQ_BB_VDD_IN	15	16	VBAT_RTC
TQ_PROG_SFP_IN	17	18	DGND
DGND	19	20	DGND

3.10 User interfaces

3.10.1 OLED display

On the MBLX2160A an OLED display is installed. The interface is adapted to the Newhaven Display NHD-1.69-160128G. Detailed information about the display is provided by Newhaven:
https://www.newhavendisplay.com/nhd169160128g-p-9642.html

Figure 33: OLED display NHD-1.69-160128G

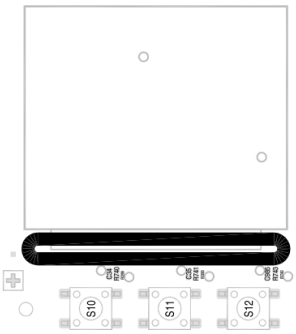


Figure 34: Push buttons S10 to S12

With the keys S10 to S12 below the display you can navigate through the menu structure.
The display is controlled by the PMC via SPI.

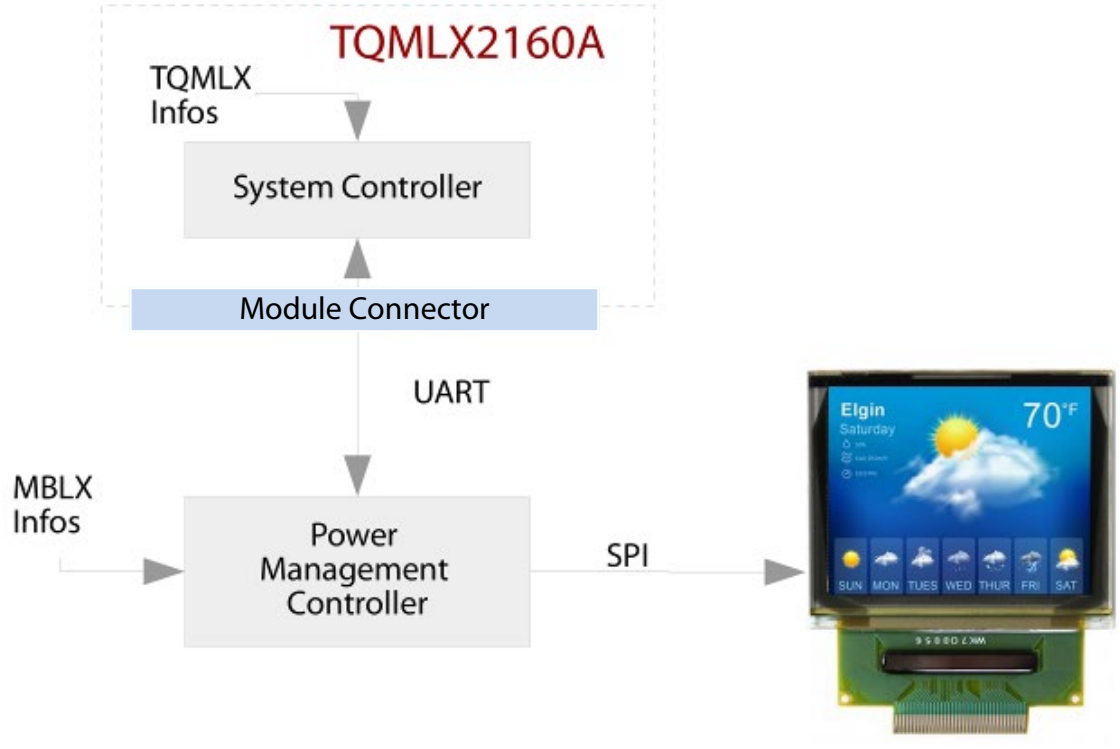
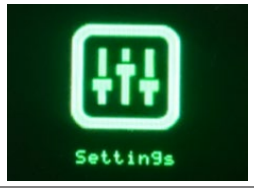
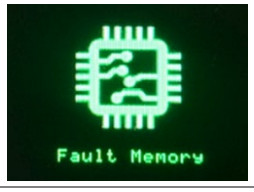


Figure 35: OLED display interface

Data can be displayed in real time, such as

- Power consumption
- Temperatures
- Error messages

3.10.1 OLED display (continued)

	**System UP** If the system was successfully started, "System Up" is displayed. Press ⊖ to access the menu.
	**Home** From here you can navigate through the menu with ⊖ and ⊖. ⊖ opens the respective submenu.
	**Power** - Power consumption - Current consumptions
	**Temperatures** Readings of the temperature sensors
	**Settings** Shows the DIP switch settings.
	**Fault Memory** List of the fault memory entries of the TQMLX2160A.
	**Timer** (TBD)
	**System** System information
 	Pressing ON/OFF for a longer time puts the system into shutdown mode.

3.10.2 GP LEDs and GP buttons

Two GP_LEDs and two GP_BUTTONs are provided on the MBLX2160A. They are controlled as follows:

- GP_LED **V41**: GPIO3_DATA08
- GP_LED **V42**: GP_LED_2 via Port Expander D21
- GP_BUTTON **S8**: GPIO3_DATA09 or IRQ6
- GP_BUTTON **S9**: GPIO3_DATA10 or IRQ7

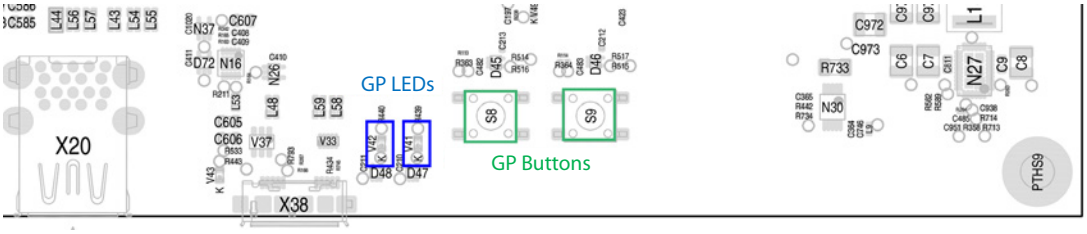


Figure 36: GP LEDs and GP buttons, position

3.10.3 Status LEDs

Seven Status LEDs are provided on the MBLX2160A. For a better overview they are grouped:

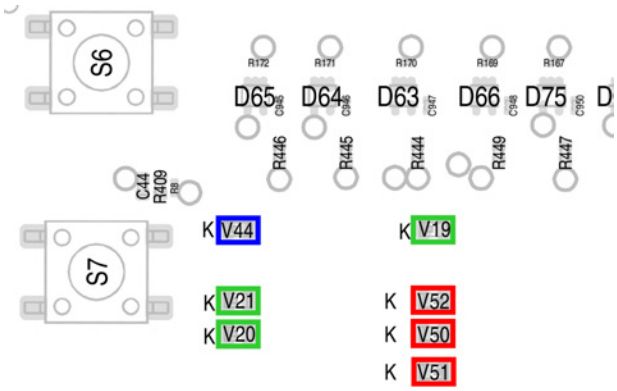


Figure 37: Status LEDs, position

Table 24: Status LEDs

Reference	Colour	Signal	Description
V44	Blue	VIN_FILT_STANDBY	Signals the presence of a supply voltage
V19	Green	LED_PMC_ALIVE	Operational readiness of the Power Management Controller
V20	Green	TQMLX_PGOOD	PGOOD Signal coming from TQMLX2160A
V21	Green	MBLX_PGOOD	PGOOD Status of the MBLX2160A
V50	Red	TQMLX_RST_IN#	Reset signal to TQMLX2160A
V51	Red	EVENT_TEMPSENSOR#	Interrupt signal from temperature sensor on the TQMLX2160A
V52	Red	MBLX_FAILURE	Error status on the MBLX2160A

3.10.4 DIP switches

The MBLX2160A can be configured with DIP switches S1 ~ S5.
The switch positions can be read out by the I²C Port Expander D23 (connected to I2C1_CPU).
The DIP switches switch to GND, which results in the following logic levels:

- DIP switch ON: Logic Low
- DIP switch OFF: Logic High

Table 25: Function DIP switch, S1 ~ S5

DIP	Switch	Signal	Function
S1	1~2	BOOT_SRC0	Boot source selection, see 3.1.3
	3~4	BOOT_SRC1	
	5~6	BOOT_SRC2	
	7~8	NOR_SWAP#	NOR Flash Swap Option, see 3.1.5
S2	1~2	EMMC_SEL0	EMMC configuration, see 3.1.4
	3~4	EMMC_SEL1	
	5~6	EVDD_SEL	
	7~8	LX_CONIG_RFU1	RFU
S3	1~2	SD1_MUX_SEL	SD1 Muxing options, see 3.5.2
	3~4	SD2_2_MUX_SEL	SD2 Muxing options, see 3.5.3
	5~6	SD2_3_MUX_SEL	
	7~8	SD2_4_MUX_SEL	
S4	1~2	SD2_6_MUX_SEL	
	3~4	SD2_7_MUX_SEL	
	5~6	SD3_MUX_SEL	SD3 Muxing options, see 3.5.4
	7~8	ENABLE_FAN	Enables / disables the FAN Switch, see 3.11
S5	1~2	EC2_SEL	EC2 1588 Muxing, see 3.8
	3~4	–	–

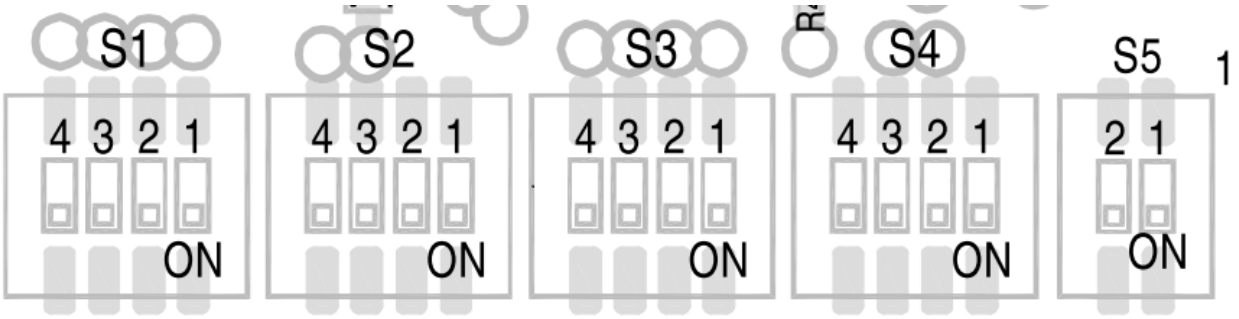


Figure 38: DIP switches S1 to S5

3.10.5 JTAG

Separate debug / programming interfaces are provided for the System Controller on the TQMLX2160A and the PMC on the MBLX2160A. Reprogramming these components is normally neither useful nor necessary, as this can impair system stability. Programming should only be carried out for good reason after consultation with TQ-Systems.

The JTAG® interface of the LX2160A can be used. It is routed to connector X26:

Table 26: Connector X26

Signal	Pin	Pin	Signal
JTAG_LX_VREF	1	2	JTAG_LX_TMS
DGND	3	4	JTAG_LX_TCK
DGND	5	6	JTAG_LX_TDO
NC	7	8	JTAG_LX_TDI
DGND	9	10	JTAG_LX_HRESET ↔ JTAG_LX_TRST#

The following NXP Code Warrior TAP adapter can be used: CWH-CTP-CTX10-YE

Figure 39: NXP Code Warrior TAP adapter (source NXP)

For the PMC on the MBLX2160A and the System Controller on the TQMLX2160A a UART-USB interface for console outputs is available. The USB debug interface is self-powered and has two ports.

3.11 Fan

For proper operation, the TQMLX2160A must be cooled. Two connectors for fans are provided. No speed or voltage control is provided. Only 12 V can be switched. The fans can be activated / deactivated collectively by DIP switch S4-4.

Table 27: Pinout FAN connectors, X22, X23

Pin	Description
1	GND
2	12 V, switched
3	(NC)

4. SOFTWARE

No software is required for the MBLX2160A.
Suitable software is only required on the TQMLX2160A and is not a part of this User's Manual.
More information can be found in the Support Wiki for the TQMLX2160A.

5. MECHANICS

5.1 TQMLX2160A and MBLX2160A dimensions

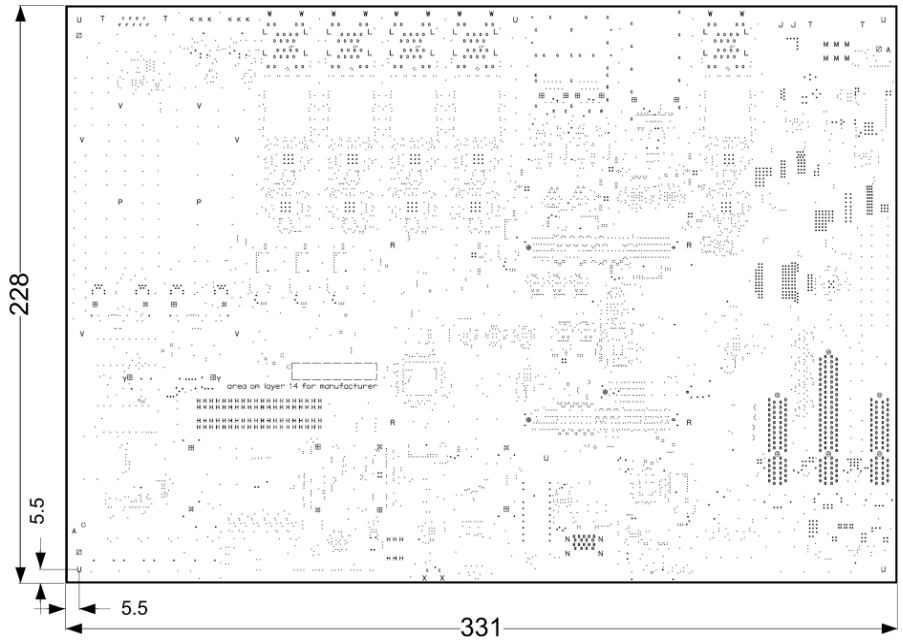


Figure 40: MBLX2160A dimensions (± 0,1 mm)

5.2 Notes of treatment

The TQMLX2160A is held in its mating connectors with a considerable retention force.

To avoid damage caused by mechanical stress, the TQMLX2160A may only be extracted from the MBLX2160A by using the extraction tool MOZILX2160A that can be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBLX2160A for the extraction tool MOZILX2160A.

5.3 Thermal management

The TQMLX2160A on the MBLX2160A has a maximum peak power consumption of approximately 60 W.

Further power consumption occurs mainly at externally connected devices.

Attention: Destruction or malfunction, TQMLX2160A heat dissipation	
	The TQMLX2160A belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LX2160A must be taken into consideration when connecting the heat sink. The LX2160A is the highest component on the TQMLX2160A. Inadequate cooling connections can lead to overheating of the TQMLX2160A and thus malfunction, deterioration or destruction.

5.4 Assembly

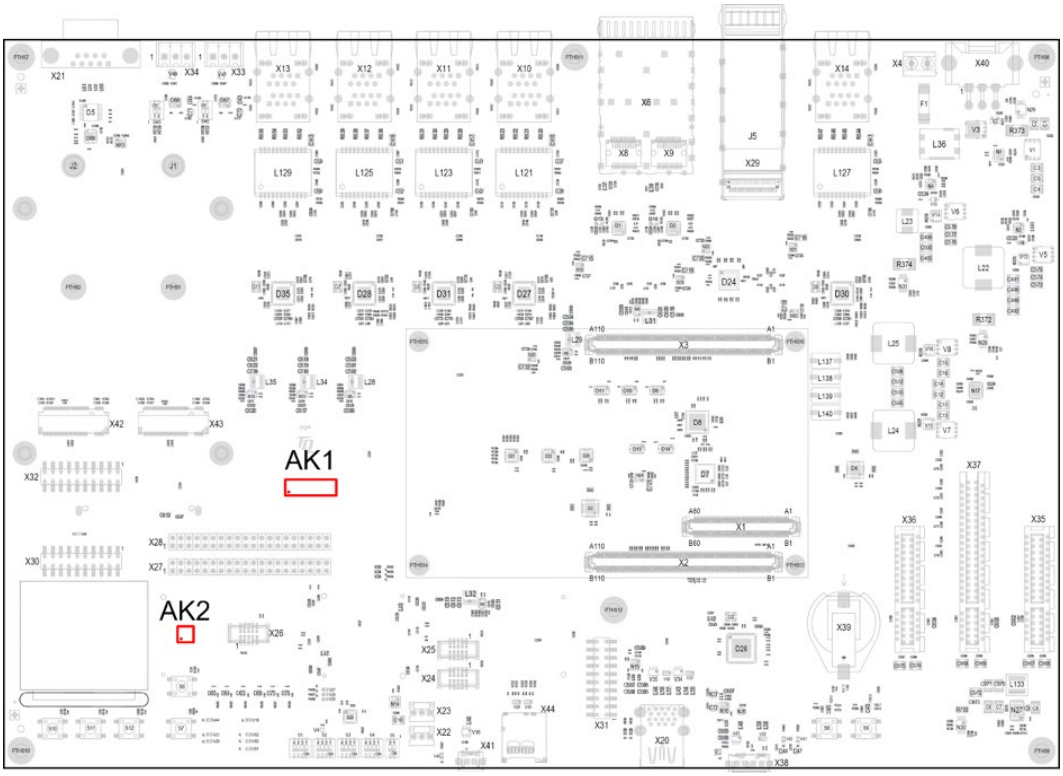


Figure 41: MBLX2160A labels

The labels on the MBLX2160A revision 01xx show the following information:

Table 28: Labels on MBLX2160A

Label	Content
AK1	MBLX2160A version and revision, tests performed
AK2	Serial number

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The MBLX2160A was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

A good protection against electrostatic discharge must be installed directly at the inputs of a system. On the MBLX2160A common measures have been provided. The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤24 V DC.

7. CLIMATE AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 29: Climatic and operational conditions MBLX2160A

Parameter	Range	Remark
Ambient temperature	-10 °C to +60 °C	With Lithium battery
Ambient temperature	-40 °C to +85 °C	Without Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: Destruction or malfunction, TQMLX2160A heat dissipation	
	The TQMLX2160A belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LX2160A must be taken into consideration when connecting the heat sink. The LX2160A is the highest component on the TQMLX2160A. Inadequate cooling connections can lead to overheating of the TQMLX2160A and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBLX2160A. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBLX2160A.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBLX2160A is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBLX2160A was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBLX2160A must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBLX2160A enable compliance with EuP requirements for the MBLX2160A.

8.5 Packaging

The MBLX2160A is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

Due to technical reasons a battery is necessary for the MBLX2160A. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (chapter 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 gram.
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 gram.
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBLX2160A, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBLX2160A is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 30: Acronyms

Acronym	Meaning
BGA	Ball Grid Array
BIOS	Basic Input/Output System
CAN	Controller Area Network
CAUI	100 Gigabit Attachment Unit Interface
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DC	Direct Current
DIP	Dual In-line Package
DNC	Do Not Connect
EEPROM	Electrically erasable programmable read-only memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LED	Light Emitting Diode
LP_DDR4	Double Data Rate 4
LVDS	Low-Voltage Differential Signaling
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures
NAND	Not-And (flash memory)
NC	Not Connected
NOR	Not-Or
OLED	Organic Light-Emitting Diode
OTG	On-the-Go
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMC	Power Management Controller
PU	Pull-Up

9.1 Acronyms and definitions (continued)

Table 29: Acronyms (continued)

Acronym	Meaning
QSFP	Quad Small Form-Factor Pluggable
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RFU	Reserved for Future Use
RGMII	Reduced Gigabit Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SerDes	Serializer/Deserializer
SFP	Small Form-factor Pluggable
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SSD	Solid-State Disk
SVHC	Substances of Very High Concern
TAP	Telelocator Alphanumeric Protocol
TBD	To be Determined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDOG	Watch-Dog
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write Protect
XFI	10 Gigabit Small Form-factor Interface
XSPI	Expanded Serial Peripheral Interface

9.2 References

Table 31: Further applicable documents

No.	Name	Rev., Date	Company
(1)	LX2160A Reference Manual	(TBD)	NXP
(2)	LX2160A Data Sheet	(TBD)	NXP
(3)	LX2160A Fact Sheet	Rev. 0, 05. Oct. 2017	NXP
(4)	TQMLX2160A User's Manual	– current –	TQ-Systems
(5)	TQMLX2160A Support Wiki	– current –	TQ-Systems

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