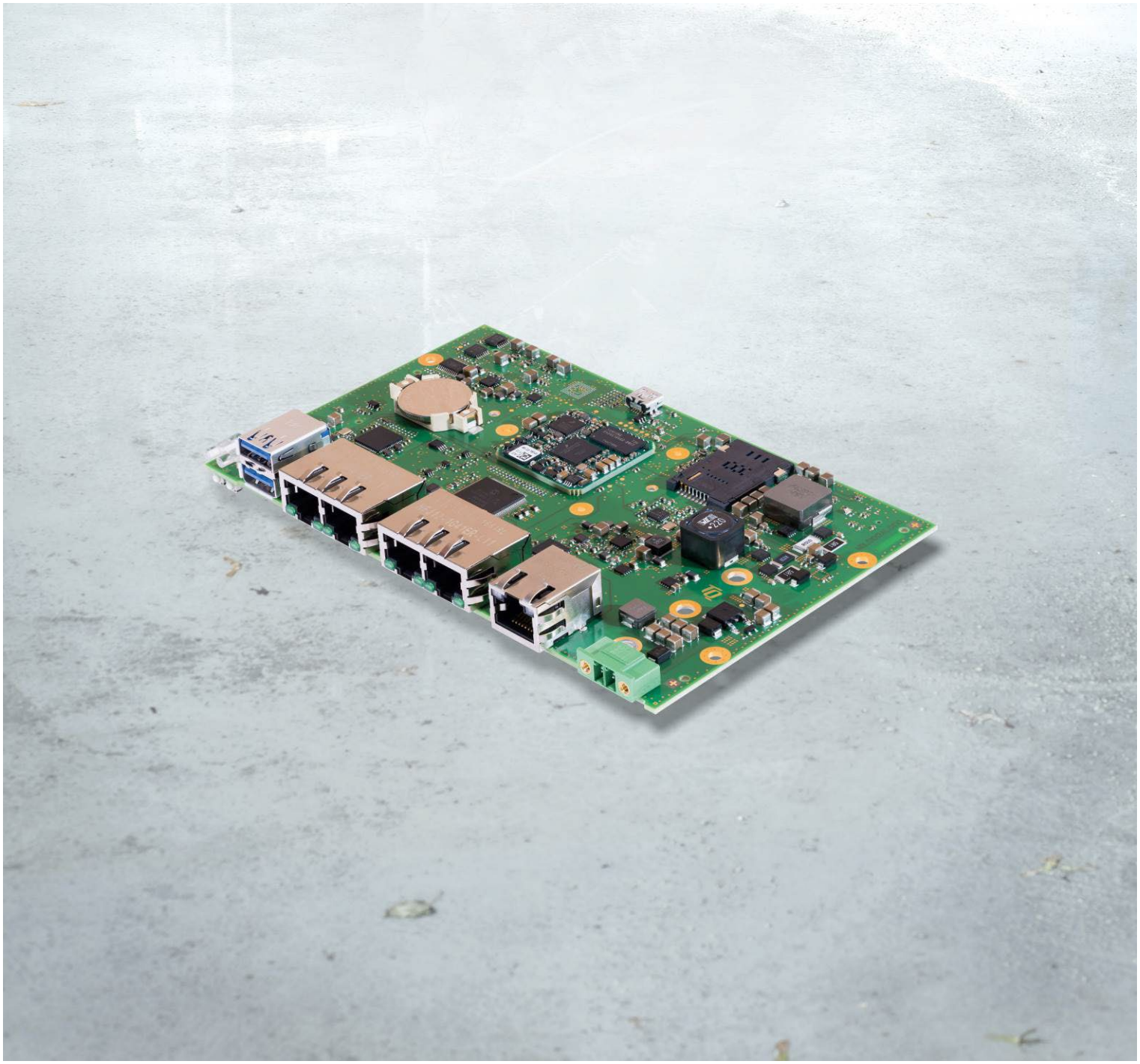
MBLS1012AL
User's Manual

MBLS1012AL UM 0100
07.03.2022



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Rev.	Date	Name	Pos.	Modification
0100	07.03.2022	Kreuzer		First issue

1. ABOUT THIS MANUAL

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBLS1012AL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLS1012AL circuit diagram
- TQMLS1012AL User's Manual
- LS1012A Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: support.tq-group.com/en/layerscape/tqmls1012al/mbls1012al

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBLS1012AL from revision 0200.

The MBLS1012AL is designed as a carrier board for the TQMLS1012AL.

All TQMLS1012AL interfaces, which can be used, are available on the MBLS1012AL, thus the features of the CPU LS1012A can be evaluated and software development for a TQMLS1012AL-based project can be started directly.

2.1 System architecture and functionality

2.1.1 Block diagram MBLS1012AL

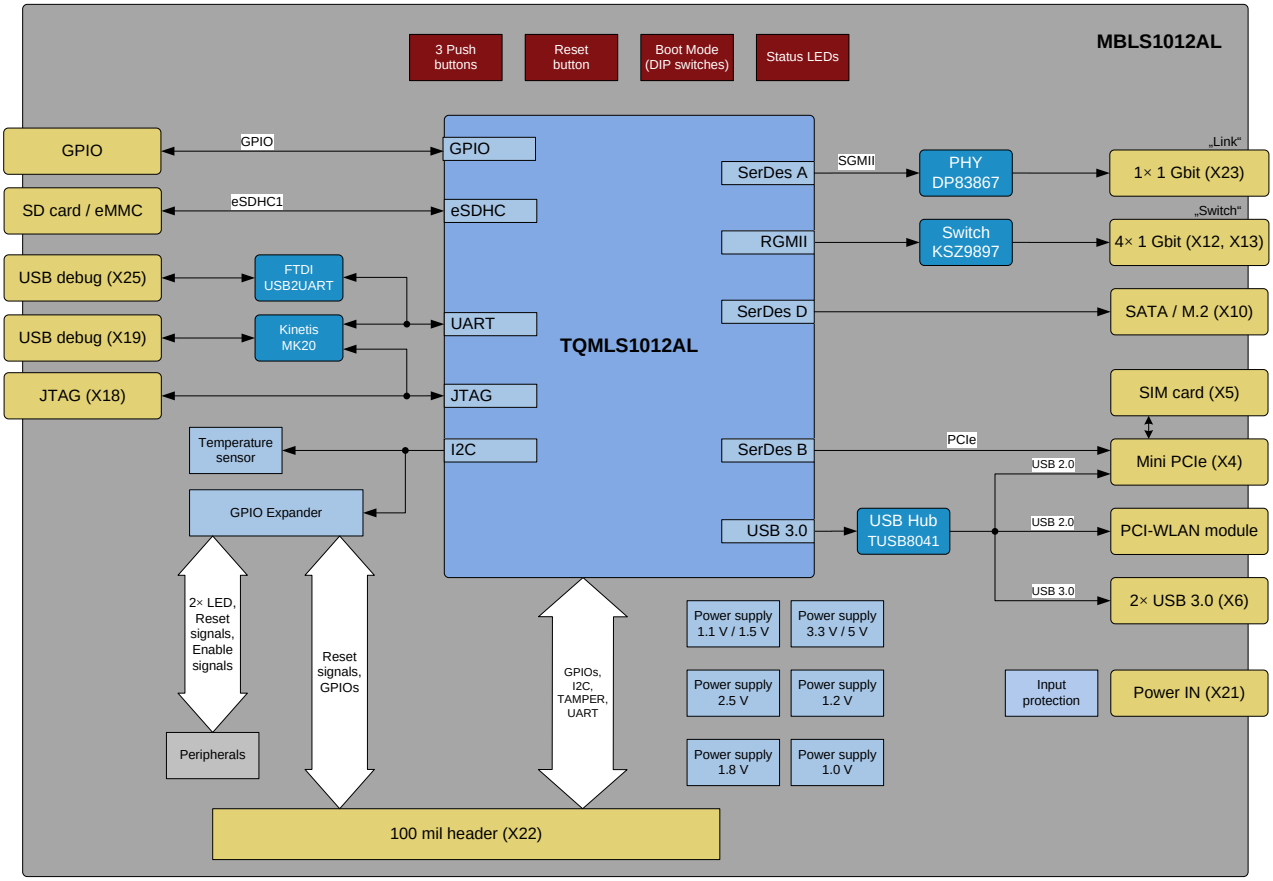

Figure 1: Block diagram MBLS1012AL

2.1.2 Functionality and interfaces

Core of the system is the soldered processor module TQMLS1012AL with an ARM Cortex A53 based NXP LS1012A CPU.
In addition to the standard communication interfaces such as USB, Ethernet, etc., more TQMLS1012AL signals are routed to a 100 mil pin header on the MBLS1012AL.

The MBLS1012AL provides the following interfaces and functions:

Table 2: Overview interfaces

Interface	Qty.	LS1012A interface	Remark
Ethernet 1000 Mbit	1	SGMII (SerDes Lane A, MAC1)	Gigabit PHY DP83867
Ethernet 1000 Mbit	4	RGMII (MAC2)	5-fold Gigabit switch KSZ9897
SATA	1	SATA (SerDes Lane D)	Supply and insert nut for M.2 SSD
Mini PCIe	1	PCIe (SerDes Lane B) USB 2.0 from TUSB8041	With external SIM card slot
USB 3.0	4	USB 3.0 from TUSB8041	Hub TUSB8041: • 1x stacked USB Type A (USB 3.0) • 1x WLAN module (USB 2.0) • 1x Mini PCIe (USB 2.0)
WLAN	1	USB 2.0 from TUSB8041	As Mini PCIe socket
eMMC [1]	1	eSDHC1	On-board 4-bit JEDEC 4.5 5.0 eMMC compatible Optional instead SD card
SD card	1	eSDHC1	Optional instead eMMC
GPIO (native, 1.8 V)	4	GPIO1	GPIO1_25 and GPIO1_26 with Pull-Up and Pull-Down at DIP switch
GPIO (Port Expander, 3.3 V)	3	–	Provided via GPIO Expander, control via I2C_3V3
Debug	1	UART	3.3 V UART, switchable between FTDI USB2UART/pin header and OpenSDA [2] (USB) by DIP switch
JTAG	1	JTAG	10-pin header and over OpenSDA via USB
I^2C	1	I2C1_3V3	On pin header

Table 3: Overview Diagnostic and User Interfaces

Interface	Qty.	Device	Remark
Status LEDs	6	Green LED	• 24 V • 5 V • 3.3 V • 3.3 V PCIe • 3.3 V WLAN • 2.5 V
	3	Green LED	Mini PCIe, WLAN, SATA (M.2)
	1	Green LED	GPIO LED at Port Expander
	1	Green LED	GPIO LED at Port Expander with light guide
	1	Red LED	Reset LED with light guide
Temperature sensor	1	–	Digital I^2C temperature sensor
Reset button	1	Push button	CPU / MBLS1012AL Reset
User push button	3	Push button	GPIO push button at Port Expander
Boot Mode configuration	1	DIP switch	See chapter 3.1.1.1
JTAG	1	10-pin, 100 mil header	–

1: eMMC functionality prepared. Currently not supported.
2: OpenSDA function is currently not supported.

3. ELECTRONICS

The TQ-Minimodule TQMLS1012AL with its LS1012A CPU is the central system component. It provides DDR3L SDRAM, eMMC, NOR flash and EEPROM memory. All voltages required by the TQMLS1012AL are derived from the supply voltage of 3.3 V.

The available signals are routed to two connectors on the MBLS1012AL. More detailed information is to be taken from the TQMLS1012AL User's Manual. The boot behaviour of the TQMLS1012AL can be customised.

The required Boot mode configuration can be set with DIP switches, see section 3.1.1.1.

3.1 MBLS1012AL functional groups

3.1.1 TQMLS1012AL

The TQ-Minimodule TQMLS1012AL with the LS1012A CPU is the central system component. It provides DDR3L SDRAM, NOR flash and an EEPROM. All TQMLS1012AL internal voltages are derived from the 3.3 V supply voltage. Further information can be found in the TQMLS1012AL User's Manual.

The boot behaviour of the TQMLS1012AL can be modified. The configuration is defined by DIP switches on the MBLS1012AL, see chapter 3.1.1.1. The available signals of the TQMLS1012AL are routed to solder pads on the MBLS1012AL. The signal assignment can be found in the TQMLS1012AL User's Manual.

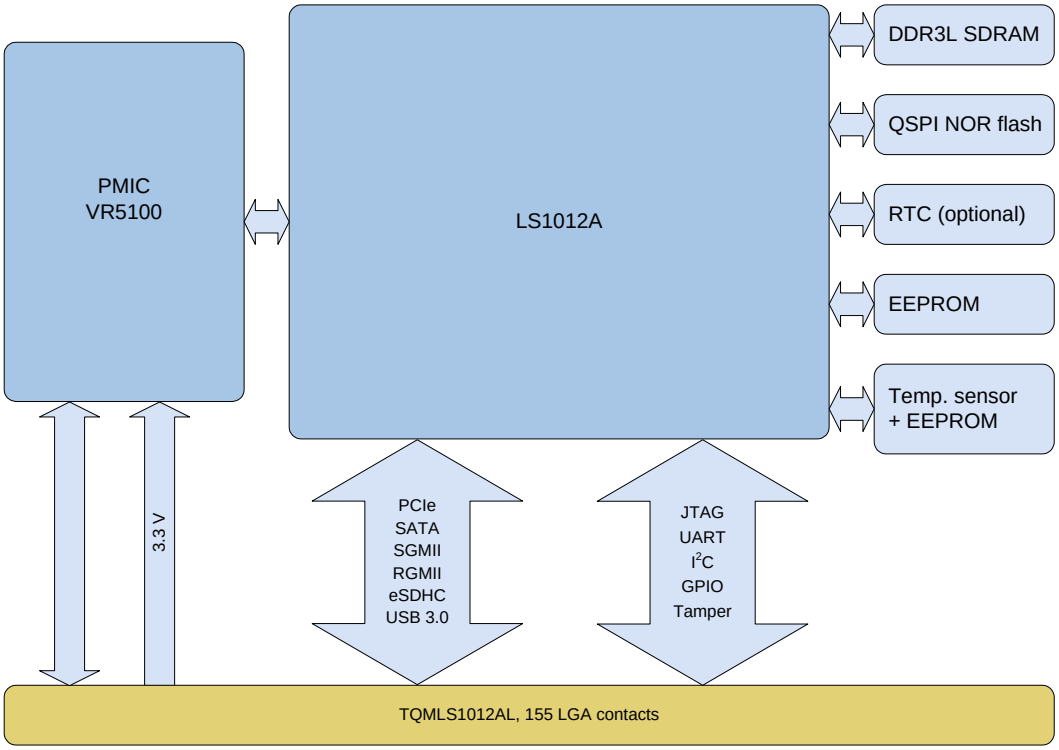

Figure 2: Block diagram TQMLS1012AL

3.1.1.1 Boot Mode configuration

The boot behaviour of the LS1012A is determined by a 512-bit Reset Configuration Word (RCW). During normal operation this is loaded from the connected QSPI flash memory on the TQMLS1012AL. The processor only supports this one boot source.

In case the RCW on the QSPI flash is missing or damaged, a fall-back mode exists to load a suitable boot configuration. For this purpose a fixed standard configuration of the RCW (Hard-Coded RCW) is loaded, which provides the minimum necessary values for the CPU to operate. This is activated via a boot strap resistor at RESET_REQ#.

By connecting the RESET_REQ# / RCW_SRC signal to DIP switch (S1) (see also chapter 3.4.1), the value assigned to cfg_rcw_src determines one of the two possible RCW sources. See also LS1012A Data Sheet (1) chapters 4.2.1.1, 4.4.1, 4.4.4, and 4.4.5.
The value is read in during Power-On-Reset and can be read out in CPU register PORSR1[RCW_SRC]. For this purpose there is a Pull-Down resistor at the RESET_REQ# signal to select the Hard-Coded RCW during the boot process (see following table).

Table 4: Boot Mode-Select values for cfg_rcw_src

cfg_rcw_src value	Selection on MBLS1012AL	RCW source
0	Slot 1 at DIP switch (S1) to ON	Hard-coded in CPU
1 (Default)	Slot 1 at DIP switch (S1) to OFF	QuadSPI (QSPI)

Table 35 lists suitable debuggers/programmers to write RCW and bootloader to the QSPI flash.

Attention: Missing RCW in QSPI flash	
	If no RCW is detected in the QSPI flash, the CPU automatically triggers a reset. See section 3.1.6. Table 35 shows a selection of debuggers / programmers for writing the RCW and / or the bootloader to the QSPI flash.

3.1.2 I²C devices

The TQMLS1012AL provides an I²C bus on the MBLS1012AL. This I²C bus is implemented with a 1.8 V and a 3.3 V branch. The 3.3 V branch is routed to a 100 mil pin header and terminated with 4.7 kΩ Pull-Ups on the MBLS1012AL.
Table 5 lists all I²C addresses used.

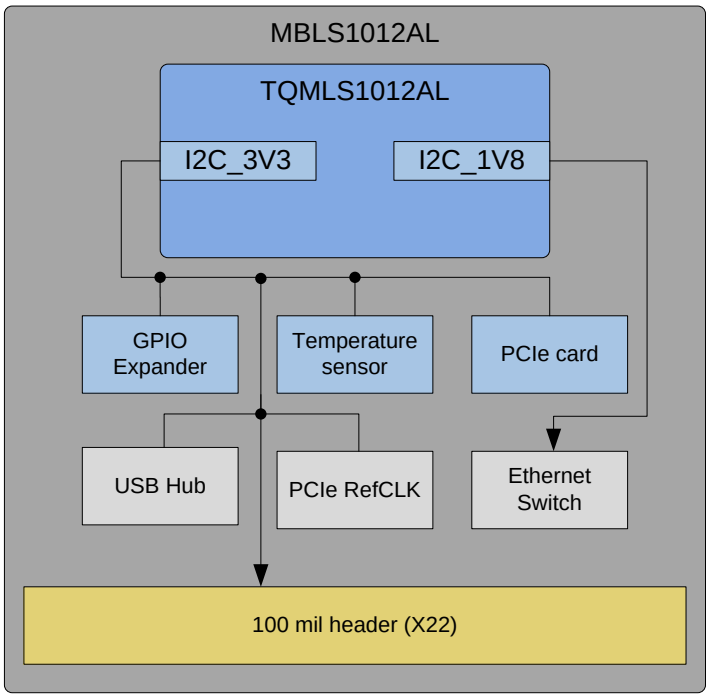

Figure 3: Block diagram I²C bus

The following table shows the I²C address mapping on TQMLS1012AL and MBLS1012AL.

Table 5: I²C devices, address mapping on TQMLS1012AL and MBLS1012AL

Location	Device	Function	7-bit address	Remark
MBLS1012AL	KSZ9897R	Ethernet Switch	0x5F / 101 1111b	Optional, not connected
	TUSB8041	USB Hub	0x44 / 100 0100b	Optional, not connected
	LM75ADP	Temperature sensor	0x48 / 100 1000b	–
	9FGV0241	PCIe RefClk	0x69 / 110 1001b	Optional, not connected
	–	PCIe card	–	Defined by PCIe card
	–	WLAN card	–	Defined by WLAN card
	PCA9555PW	GPIO expander	0x20 / 010 0000b	Device D13, 3.3 V
	PCA9538ABS	GPIO expander	0x70 / 111 0000b	Device D24, 1.8 V
TQMLS1012AL	DS1339U-33	RTC	0x68 / 110 1000b	–
	SE97B	Temperature sensor	0x19 / 001 1001b	Access to temperature registers
		EEPROM	0x51 / 101 0001b	R/W access in Normal Mode
		EEPROM	0x31 / 011 0001b	R/W access in Protected Mode
	24LC64T	EEPROM	0x50 / 101 0000b	–
	VR5100	PMIC	0x08 / 000 1000b	Should not be altered

3.1.3 Temperature sensor

The MBLS1012AL provides a temperature sensor LM75A, which monitors the environmental temperature.

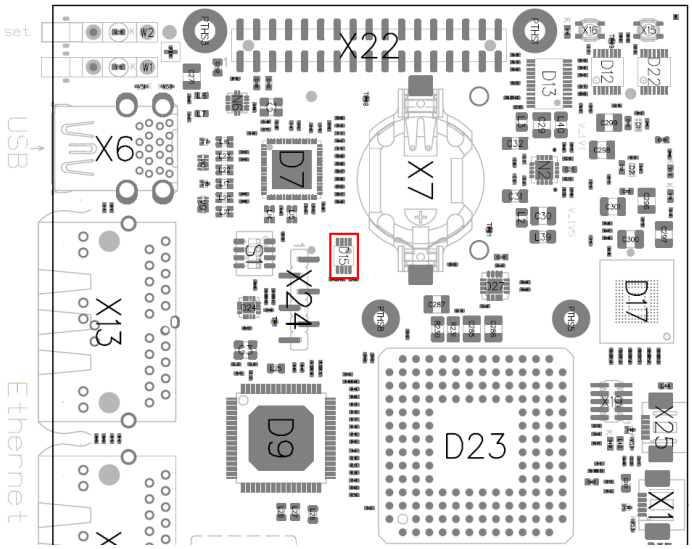

Figure 4: Position of temperature sensor LM75A

Table 6: Electrical characteristics LM75A

Manufacturer	Resolution	Accuracy	Range	Error
NXP	0.125 °C	11 bit	–25 °C to +100 °C –55 °C to +125 °C	±2 °C ±3 °C

➢ The temperature sensor on the MBLS1012AL has I²C address `0x48 / 100 1000b`.

3.1.4 RTC backup supply

In case of power failure a lithium battery on the MBLS1012AL supplies the RTC on the TQMLS1012AL.

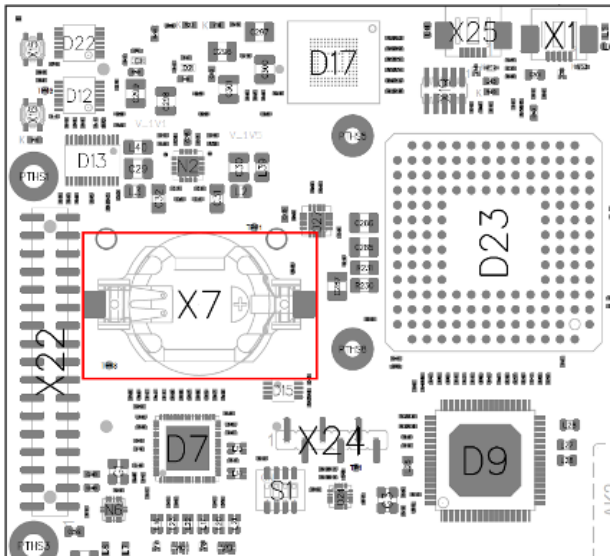

Figure 5: Position of backup battery X7

For the RTC on the MBLS1012AL the following applies:

Table 7: Electrical characteristics backup battery

Parameter	Remark
Coin Cell voltage	2.1 V to 3.7 V, typical 3.0 V
Coin Cell type	CR2032
Current consumption RTC	Depends on RTC option used

3.1.5 GPIO port expander

Due to the low number of native GPIOs provided by the LS1012A CPU, two GPIO expanders with 16 and 8 IOs are provided on the MBLS1012AL. The respective interrupt pin of the GPIO expander is connected to a GPIO pin of the LS1012A CPU:

- 16-port expander PCA9555PW: GPIO1_24
- 8-port Expander PCA9538ABS: GPIO1_27

The port expanders are configured via I²C. The address of the port expanders can be altered by resistor assembly.
The assembly options are documented in the circuit diagram.
When changing the address, care must be taken to avoid address conflicts with existing I²C devices.
In the initial state, after power-up, all ports are set as input and the connected component is thus deactivated.
For the properties of the externally available GPIOs see section 3.4.2.
The following table shows the functions of the pins of the port expander.

Table 8: Function of Port Expanders

Port	Signal	Dir.	Default	Remark
16-port Expander PCA9555PW, D13, I²C address 0x20 / 010 0000b				
IO0_0	WLAN_DISABLE#	O	High	X3, pin 20 (WLAN)
IO0_1	VCC_PCIE_EN_3V3	O	Low	Enable-Signal for 3.3 V, PCIe
IO0_2	GPIO_3V3_3	I/O	–	GPIO on header X22, pin 28
IO0_3	VCC_WLAN_EN_3V3	O	Low	Enable-Signal for 3.3 V, WLAN
IO0_4	IOXP_PCIE_RST#	O	Low	Selective Reset, PCIe
IO0_5	IOXP_WLAN_RST#	O	Low	Selective Reset, WLAN
IO0_6	IOXP_USB_RST#	O	Low	Selective Reset, USB
IO0_7	IOXP_ETH_SW_RST#	O	Low	Selective Reset, Ethernet Switch
IO1_0	IOXP_ETH_LNK_RST#	O	Low	Selective Reset, Ethernet Link
IO1_1	GPIO_3V3_1	I/O	–	GPIO on header X22, pin 24
IO1_2	GPIO_3V3_2	I/O	–	GPIO on header X22, pin 26
IO1_3	PCIE_DIS#	O	High	X4, pin 20 (Mini PCIe)
IO1_4	PCIE_WAKE#	I	High	X4, pin 1 (Mini PCIe)
IO1_5	–	I	High	Input from push button S2 on front panel
IO1_6	–	O	High	LED V15 green, with light guide to front panel
IO1_7	–	O	High	LED V16 green
8-port Expander, PCA9538ABS, D24, I²C address 0x70 / 111 0000b				
IO_0	PCIE_CLK_PD#	O	High	Disable for PCIe Clock
IO_1	PMIC_INT#	I	High	Input from PMIC Interrupt, also routed to X22, pin 22
IO_2	ETH_SW_INT#	I	High	Input from Ethernet Switch Interrupt
IO_3	ETH_LINK_PWRDWN#	O	Low	Power-Down output for Ethernet Link
IO_4	–	I	High	Input from push button X15
IO_5	–	I	High	Input from push button X16
IO_6	VCC_WLAN_EN_1V5	O	Low	Enable-Signal for 1.5 V, WLAN
IO_7	VCC_PCIE_EN_1V5	O	Low	Enable-Signal for 1.5 V, PCIe

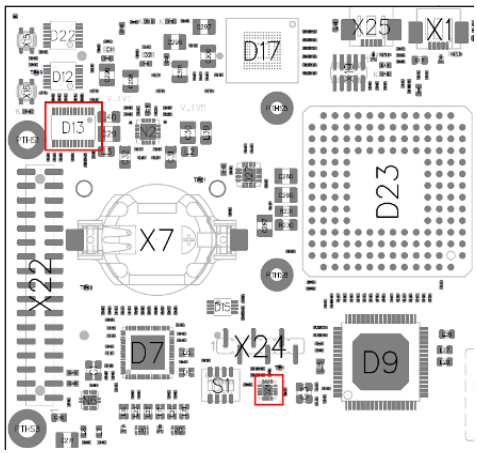

Figure 6: Position of Port Expanders

3.1.6 Reset structure

The RESET# signal of the TQMLS1012AL is available via signals RESET_1V8# and RESET_3V3# on the MBLS1012AL. Signal RESET_3V3# on the MBLS1012AL is generated from RESET_1V8#.

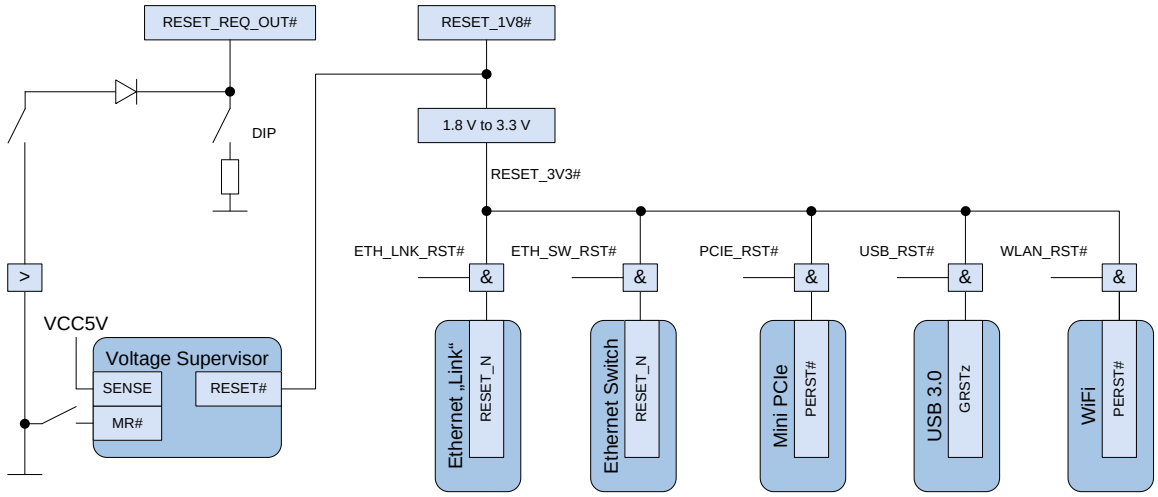

Figure 7: Reset structure

Attention: Signal RESET_1V8#	
	Signal RESET_3V3# is designed as reset triggering signal. Signal RESET_1V8# must be used to reset the system.

The global reset is also used by the voltage monitoring. The Supervisor TPS3808G01DBV is used for this purpose. It monitors the 5 V input voltage and includes the manual reset button. The under-voltage threshold is set to 4.455 V, the delay until the reset signal is enabled again is set to 300 ms. On the MBLS1012AL a red LED indicates a reset, see Table 33.

In addition to the signals described above, the MBLS1012AL offers further options for a complete or partial reset of the TQMLS1012AL. All important interfaces are connected to the reset signal via AND gates in such a way that, in addition to the global reset, they can be reset individually via a GPIO signal of the IO expander. In addition, the power supplies of the WLAN and PCIe cards can be switched separately. The following table shows the signals used.

3.1.6 Reset structure (continued)

Table 9: Reset signals

Signal	Source	Default	Remark
RESET_1V8#	TQMLS1012AL	High	Activated by the TQMLS1012AL during power sequencing. Is activated approximately 140 to 460 ms after the TQMLS1012AL supply is switched on.
RESET_3V3#	MBLS1012AL	High	Is generated on the MBLS1012AL from signal RESET_1V8#
PCIE_RST#	I/O-Expander	Low	–
WLAN_RST#	I/O-Expander	Low	–
VCC_WLAN_EN_1V5	I/O-Expander	Low	Switches the 1.5 V power supply of the WLAN card
VCC_WLAN_EN_3V3	I/O-Expander	Low	Switches the 3.3 V power supply of the WLAN card
VCC_PCIE_EN_1V5	I/O-Expander	Low	Switches the 1.5 V power supply of the PCIe card
VCC_PCIE_EN_3V3	I/O-Expander	Low	Switches the 3.3 V power supply of the PCIe card
USB_RST#	I/O-Expander	Low	–
ETH_SW_RST#	I/O-Expander	Low	–
ETH_LNK_RST#	I/O-Expander	Low	–

The RESET_REQ# signal enables the CPU to trigger a reset itself via software or in the event of an error (watchdog, security violation, etc.).

The signals RESET_REQ# and RESET_1V8# are connected via DIP switch S1, slot 2. This enables to separate the connection between the two signals. Thus an endless boot loop can be prevented in case of a missing RCW.

This is necessary to install a new RCW, see also section 3.1.1.1.

A diode is placed between RESET_REQ# and DIP switch. This prevents RCW_SRC from being pulled Low during the reset phase, thus loading the hard-coded RCW (see section 3.1.1.1).

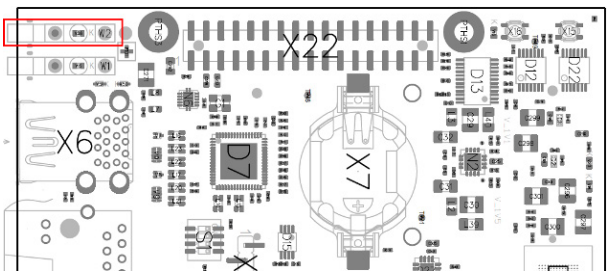

Figure 8: Position of Reset LED

3.2 Power supply

The MBLS1012AL has to be supplied with 16 V to 28 V at X21. The typical supply voltage is 24 V. All voltages required on the MBLS1012AL are derived from the supply voltage. The MBLS1012AL has a maximum peak power consumption of approx. 51 W at the 24 V supply. This corresponds to a typical maximum peak current consumption of 2.1 A. The power supply used must be dimensioned accordingly. In most applications, however, the power consumption will be significantly lower. The largest part of the possible power consumption results from the standard-compliant supply of the USB, PCIe and SATA (M.2) interfaces, as well as from the power available at the pin header.

3.3 V (1.5 A), 5 V (0.75 A) and 24 V (maximum current not defined) are available on pin header X22. The current drawn must be added to the input current. It has to be ensured that the permissible limit values of the input circuit are not exceeded.

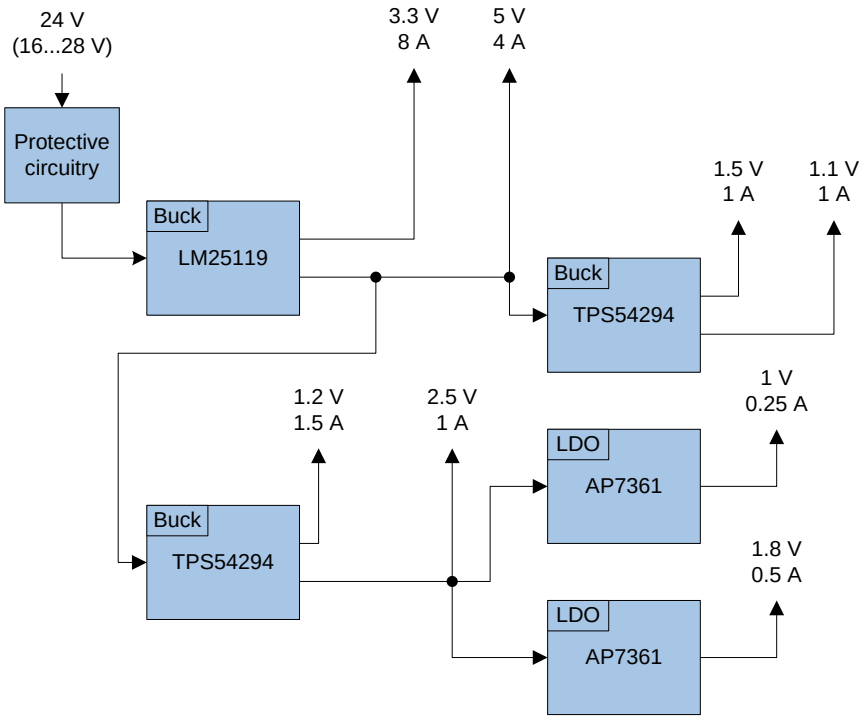

Figure 9: Block diagram power supply

3.2.1 Protective circuit

The 24 V supply of the MBLS1012AL supplies the 3.3 V / 5 V regulators.
The protection circuit (see Figure 10) features the following characteristics:

- Overcurrent protection by fuse 4 A, slow blow
- Overvoltage protection diode
- PI filter
- Reverse polarity protection by MOSFET
- Capacitors for voltage smoothing

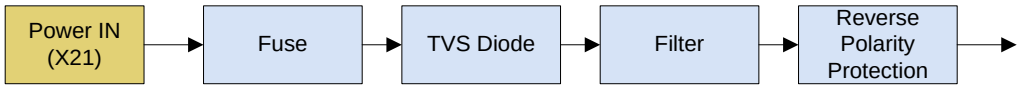

Figure 10: Block diagram protective circuit

The protective circuit has the following electrical characteristics:

Table 10: Parameter protective circuit

Parameter	Min.	Typ.	Max.	Unit
Overcurrent limitation by fuse (slow blow)	–	4	–	A
Overvoltage limitation	28.9	–	42.1	V

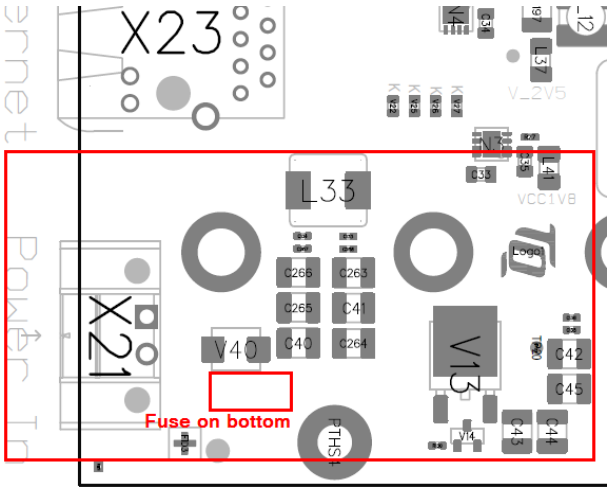

Figure 11: Positon of protective circuit

3.2.2 Voltage regulators

The following table show the electrical parameters of the voltage regulators.

Table 11: Electrical parameters of voltage regulators

Voltage	Parameter	Min.	Typ.	Max.	Unit	Remark
24 V	Input voltage	16	24	28	V	–
	Max. input current	–	–	3.2	A	–
	Idle current	–	0.19	–	A	U-Boot / Linux Idle @24 V
5 V	Output voltage	4.918	4.98	5.124	V	Over input voltage and full load range
	Max. current			4	A	
3.3 V	Output voltage	3.281	3.31	3.392	V	Over input voltage and full load range
	Max. current	–	–	8	A	
2.5 V	Output voltage	2.44	2.48	2.55	V	Over full load range
	Max. current			1	A	
1.2 V	Output voltage	1.18	1.22	1.23	V	Over input voltage and full load range
	Max. current	–	–	1.5	A	
1.5 V	Output voltage	1.46	1.49	1.52	V	Over full load range
	Max. Current			1	A	
1.1 V	Output voltage	1.08	1.08	1.11	V	Over input voltage and full load range
	Max. Current	–	–	1	A	
1.8 V	Output voltage	1.827	1.88	1.895	V	Over full load range
	Max. Current			0.5	A	
1.0 V	Output voltage	1.02	1.04	1.044	V	Over input voltage and full load range
	Max. Current	–	–	0.25	A	

The following table shows the voltage drop under full load:

Table 12: Electrical parameters of PCIe and WLAN voltages

Voltage	Min.	Typ.	Max.	Unit	Remark
V_1V5_PCIE	–	3	–	mV	IOUT = 0.375 A
V_3V3_PCIE	–	9	–	mV	IOUT = 1.1 A
V_1V5_WLAN	–	3	–	mV	IOUT = 0.375 A
V_3V3_WLAN	–	9	–	mV	IOUT = 1.1 A

3.3 Data interfaces

3.3.1 Debug UART

A debug interface is available via UART1. This UART is provided as a virtual COM port via USB. In addition, the UART can also be accessed at the 6-pin pin header X24.
UART1 is optionally available on the DAPLink / OpenSDA interface [3] (see 3.4.8).
The input signal for the TQMLS1012AL can be switched between OpenSDA and USB/pin header with a DIP switch.
The output level is adapted to 3.3 V using a level converter.

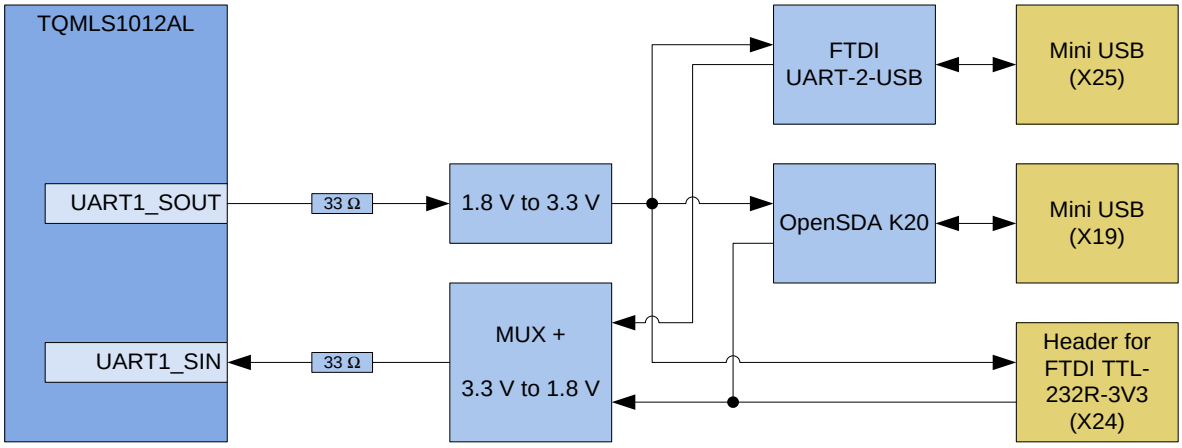

Figure 12: Block diagram Debug UART1

Table 13: DIP switch setting for UART source

DIP switch	OFF	ON
S1, slot 3	Debug UART on OpenSDA	Debug UART on USB / header X24

3.3.2 eMMC

An eMMC can be used instead of the SD card.

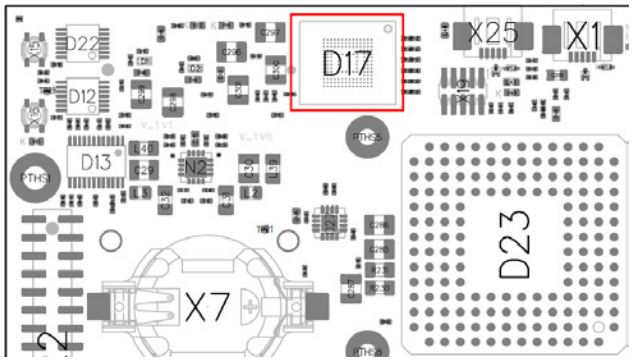

Figure 13: Position of eMMC

3: The DAPLink / OpenSDA interface is currently not supported.

3.3.3 Gigabit Ethernet (Link)

When using the MBLS1012AL e.g. as router or switch, the single port can be used as LINK interface e.g. to a modem.
The single Ethernet port is provided via the PHY DP83867 at the SGMII interface (SerDes Lane A).
The PHY has boot straps to start with configurable default values. Some boot straps can be customized with assembly options.
Further information is available in the latest circuit diagram of the MBLS1012AL.
The following table shows the pin assignment of the Ethernet connector.

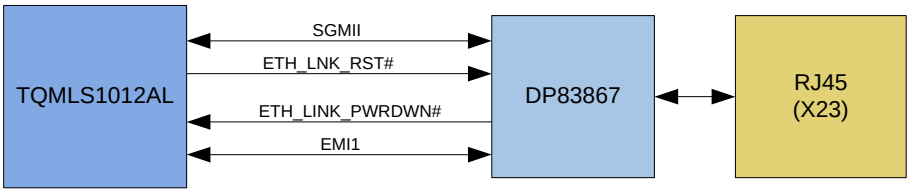

Figure 14: Block diagram Ethernet Link

Table 14: Pinout RJ45 connector X23 for "Link"

Pin	Name	Target pin / Net	Remark
1	GND	GND	–
2	TD1+	TD_P_A	–
3	TD1–	TD_M_A	–
4	TD2+	TD_P_B	–
5	TD2–	TD_M_B	–
6	TD3+	TD_P_C	–
7	TD3–	TD_M_C	–
8	TD4+	TD_P_D	–
9	TD4–	TD_M_D	–
10	GND	GND	–
11	GREEN_ANODE	V_2V5	82 Ω in series
12	GREEN_KATODE	LED_0 (DP83867)	Switched with transistor
13	YELLOW_ANODE	V_2V5	82 Ω in series
14	YELLOW_KATODE	LED_2 (DP83867)	Switched with transistor

The possible data throughput is influenced by the system load and the software platform used.
With the MBLS1012AL and the BSP provided ty TQ-Systems, the following transfer rates can be achieved.

Table 15: Characteristics Gigabit Ethernet X23 (Link)

Parameter	Min.	Typ.	Max.	Unit
Upstream	–	–	940	Mbit/s
Downstream	–	–	840	Mbit/s

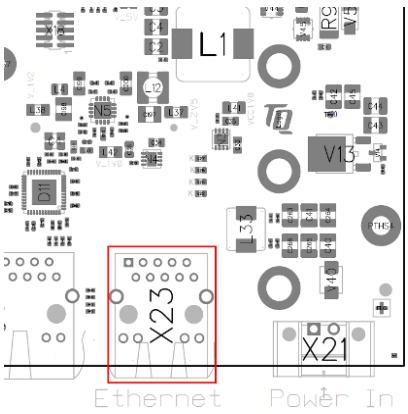

Figure 15: Position of Gigabit Ethernet X23 (Link)

3.3.4 Gigabit Ethernet (Switch ports)

Four Ethernet interfaces (1000Base-T) are available via Microchip's KSZ9897 gigabit switch, which is connected via RGMII.

The switch is managed via I²C. In contrast to MIIM (EMI), this enables full control of the device. The EMI1 bus can be connected via assembly option. The switch has boot straps to start with configurable default values. Some boot straps can be configured with assembly options. Further information is available in the latest circuit diagram of the MBLS1012AL.

The following table shows the pin assignment of the Ethernet connectors:

Table 16: Pinout RJ45 connector X12, X13 for "Switch"

Switch pin	Pin name	RJ45 pin	Remark
Ports 4-1 Gigabit Ethernet Pins			
1, 12, 24, 34	TXRX[4:1]P_A	TD0+[4:1]	–
2, 13, 25, 35	TXRX[4:1]M_A	TD0–[4:1]	–
4, 15, 26, 37	TXRX[4:1]P_B	TD1+[4:1]	–
5, 16, 27, 38	TXRX[4:1]M_B	TD1–[4:1]	–
6, 17, 28, 39	TXRX[4:1]P_C	TD2+[4:1]	–
7, 18, 29, 40	TXRX[4:1]M_C	TD2–[4:1]	–
8, 20, 31, 42	TXRX[4:1]P_D	TD3+[4:1]	–
9, 21, 32, 43	TXRX[4:1]M_D	TD3–[4:1]	–
85, 88, 91, 105	LED[4:1]_0	LED1_K[4:1]	–
86, 89, 92, 106	LED[4:1]_1	LED2_K[4:1]	–
–	–	LED1_A[4:1]	V_2V5, 100 Ω in series
–	–	LED2_A[4:1]	V_2V5, 100 Ω in series

Table 17: Ethernet Switch, Port Link Status information

LED1	LED2	Status
OFF	OFF	Link off
OFF	ON	1000 Mbps Link / No Activity
OFF	Blinking	1000 Mbps Link / Activity
ON	OFF	100 Mbps Link / No Activity
Blinking	OFF	100 Mbps Link / Activity
ON	ON	10 Mbps Link / No Activity
Blinking	Blinking	10 Mbps Link / Activity

The possible data throughput is influenced by the system load and the software platform used.

With the MBLS1012AL and the BSP provided by TQ-Systems, the following transfer rates can be achieved.

Table 18: Characteristics Gigabit Ethernet (Link)

Parameter	Min.	Typ.	Max.	Unit
Upstream	–	–	1,000	Mbit/s
Downstream	–	–	1,000	Mbit/s

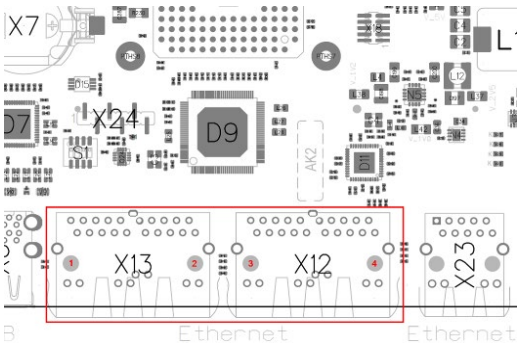

Figure 16: Position of Gigabit Ethernet X12, X13 (Switch)

3.3.5 Mini PCIe

The LS1012A provides a PCIe Gen2 interface with one lane (×1) via the SerDes interface. In default pin multiplexing, this Lane occupies Lane B of the SerDes interface. It is compatible to the PCI Express Base Specification, Revision 3.0 and supports transfer rates of 2.5 GT/s as well as 5 GT/s.

In addition to the PCIe Lane, a USB host (from the USB hub) and an I²C interface are connected to the Mini PCIe interface. The power supply is implemented with 3.3 V and 1.5 V and must be activated separately on the port expander via VCC_PCIE_EN_1V5 and VCC_PCIE_EN_3V3.

When using the I²C functionality, it has to be ensured that the I²C address used by the plug-in card is not already used by a peripheral on the MBLS1012AL, see also Table 5.

The reference clock is provided by PCIe clock generator 9FGV0241. The clock generator can optionally be connected to the I²C bus with 0 Ω resistors. Individual outputs can be switched off and the slew rate and amplitude can be changed via the I²C bus. The I²C address is `0x69 / 110 1001b`, see also Table 5.

The control signals PCIE_WAKE# and PCIE_DIS# can be switched via the port expander.

There is only one LED, which can be connected to one of the pins 42, 44 or 46. By default LED_WWAN# is connected.

The design accepts full-size and half-size Mini PCI Express cards. The retainer for full-size Mini PCI Express cards is populated.

The interface is connected with all signals provided by the standard (e.g. USB, I²C, and PCIe).

Any standard compliant Mini PCIe card can be used [4].

A micro SIM card holder is also provided to use a GSM card. SIM cards that require 5 V supply/signal level are not supported.

The voltages provided for the Mini PCIe card must not exceed the currents specified in Table 21.

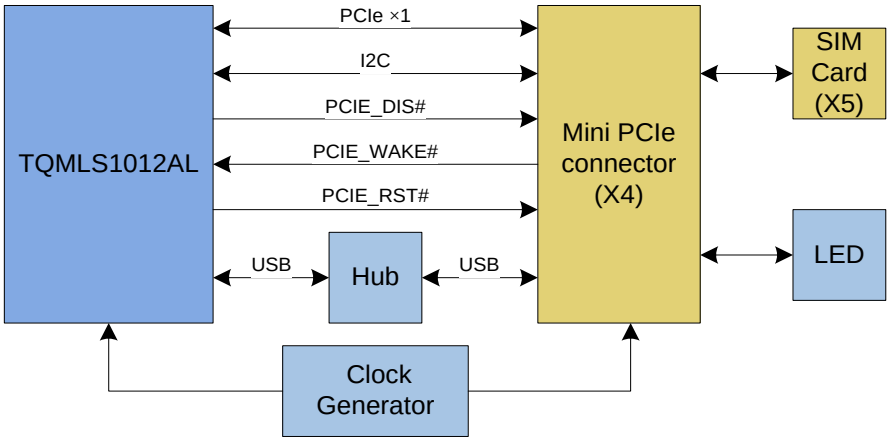

Figure 17: Block diagram Mini PCIe

4: When required drivers are available.

3.3.5 Mini PCIe (continued)

Table 19: Pinout Mini PCIe X4

Target pin / Net	Pin name	Pin		Pin name	Target pin / Net
PCIE_WAKE#	WAKE#	1	2	+3.3Vaux	V_3V3_PCIE
NC	COEX1	3	4	GND	GND
NC	COEX1	5	6	+1.5V	V_1V5_PCIE
NC	CLKREQ#	7	8	UIM_PWR	UIM_PWR
GND	GND	9	10	UIM_DATA	UIM_DATA
PCIE_REFCLK_N	REFCLK–	11	12	UIM_CLK	UIM_CLK
PCIE_REFCLK_P	REFCLK+	13	14	UIM_RESET	UIM_RESET
GND	GND	15	16	UIM_SPU	UIM_SPU
Key notch					
NC	UIM_IC_DM	17	18	GND	GND
NC	UIM_IC_DP	19	20	W_DISABLE1#	PCIE_DIS#
GND	GND	21	22	PERST#	RESET_OUT#
PCIE_RX– (TP31)	PERn0	23	24	+3.3Vaux	V_3V3_PCIE
PCIE_RX+ (TP30)	PERp0	25	26	GND	GND
GND	GND	27	28	+1.5V	V_1V5_PCIE
GND	GND	29	30	SMB_CLK	I2C_3V3_SCL
PCIE_TX– (TP33)	PETn0	31	32	SMB_DATA	I2C_3V3_SDA
PCIE_TX+ (TP32)	PETp0	33	34	GND	GND
GND	GND	35	36	USB_D–	USB_H3.D_M
GND	GND	37	38	USB_D+	USB_H3.D_P
V_3V3_PCIE	+3.3Vaux	39	40	GND	GND
V_3V3_PCIE	+3.3Vaux	41	42	LED_WWAN#	LED V28
GND	GND	43	44	LED_WLAN#	LED V28 (optional)
NC	Reserved	45	46	LED_WPAN#	LED V28 (optional)
NC	Reserved	47	48	+1.5V	V_1V5_PCIE
NC	Reserved	49	50	GND	GND
Pin 20, 0 Ω (NP)	W_DISABLE2#	51	52	+3.3V	V_3V3_PCIE

Table 20: Pinout SIM Card Connector X5

Pin	Signal
C1	UIM_PWR
C2	UIM_RST
C3	UIM_CLK
C4	(NA)
C5	DGND
C6	UIM_VPP
C7	UIM_DATA
SW1, SW2	NC

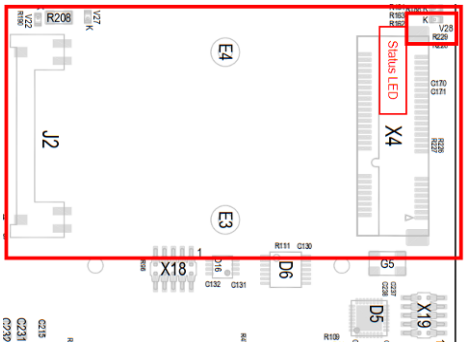

Figure 18: Position of Mini PCIe socket X4

Table 21: Maximum permitted currents Mini PCIe X4

Voltage	Nominal value	I_{max}
V_3V3_PCIE	3.3 V	1.1 A
V_1V5_PCIE	1.5 V	0.375 A

3.3.6 SATA

For mass storage, an SSD interface in M.2 form factor is provided. The LS1012A CPU provides a SATA 3.0 AHCI interface via the SerDes interface. Transfer rates of 1.5 Gb/s (Gen I), 3 Gb/s (Gen II), and 6 Gb/s (Gen III) are possible.

The M.2 standard defines different codings for the connector; an M.2 slot with B coding is used on the MBLS1012AL. M.2 modules are available in different form factors. The MBLS1012AL supports the common form factors 2242, 2260 and 2280. The insert nut for the 2280 form factor (J3) is installed as standard.

The SATA interface (SerDes Lane D) of the LS1012A and a 3.3 V power supply are used. The power budget of the MBLS1012AL is 2.5 A for a SATA SSD, in accordance with the M.2 specification.

The Device Activity Signal (DAS/DSS#; X10, pin 10) and the Device Sleep Signal (SATA_DEVSLP#; X10, pin 38) are implemented, in accordance with the M.2 specification.

SATA_DEVSLP# is connected to X22 pin 27 and must be wired accordingly if the functionality is required.

DAS/DSS# is directly connected to LED V17.

Table 22: SATA transfer rates

Value	Min.	Typ.	Max.	Unit
Net transmission rate, SATA Rev 1	–	–	1.2	Gbit/s
Net transmission rate, SATA Rev 2	–	–	2.4	Gbit/s
Net transmission rate, SATA Rev 3	–	–	4.8	Gbit/s

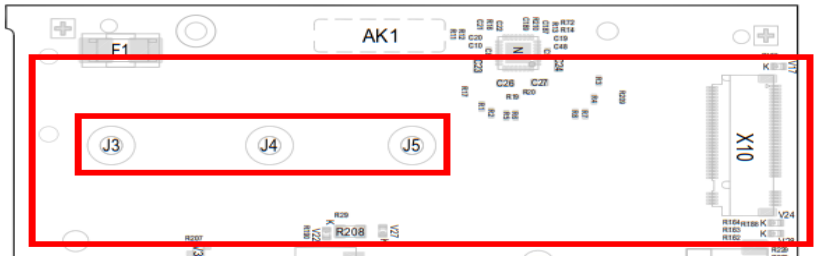

Figure 19: Position of SATA (M.2) connector X10

3.3.7 SD card

A microSD card is used as non-volatile program memory. Standard, high and extended capacity card types are supported. Alternatively, an eMMC memory can be assembled.

In the reset phase, the LS1012A CPU requires a High signal (1.8 V) at signal SDHC1_CD#. For this reason, the signal is separated by a tristate buffer during reset (see also (3), Table 5 and Figure 15). The Pull-Up is located on the TQMLS1012AL, all data signals are protected against ESD.

Default Speed, High-Speed Mode and the SD UHS-1 Speed Mode SDR104 with max. 104 MB/s are supported.

UHS-1 speed modes SDR12, SDR25, SDR50 and DDR50 are theoretically supported, but have not been verified.

The SDHC1 interface on the TQMLS1012AL is supplied by a separate PMIC switching regulator, whose output voltage can be set by the LS1012A CPU to 1.8 V or 3.3 V, depending on the transfer mode. The conversion is usually done by the corresponding driver and does not have to be done explicitly.

The signal SDHC1_WP is not used and is terminated accordingly.

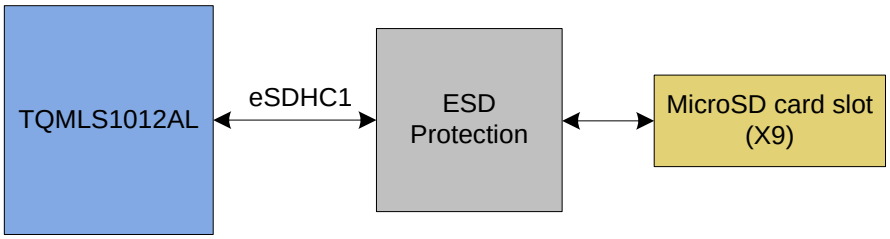

Figure 20: Block diagram SD card

Table 23: Pinout microSD card X9

Pin	Pin name	Target pin / Net	Remark
1	DAT2	SDHC1_DAT2 (TP43)	10 kΩ Pull-Up
2	DAT3	SDHC1_DAT3 (TP44)	10 kΩ Pull-Up
3	CMD	SDHC1_CMD (TP40)	10 kΩ Pull-Up
4	VDD	V_3V3	–
5	CLK	SDHC1_CLK (TP39)	–
6	GND	GND	–
7	DAT0	SDHC1_DAT0 (TP41)	10 kΩ Pull-Up
8	DAT1	SDHC1_DAT1 (TP42)	10 kΩ Pull-Up
M1…4	SHIELD	GND	–

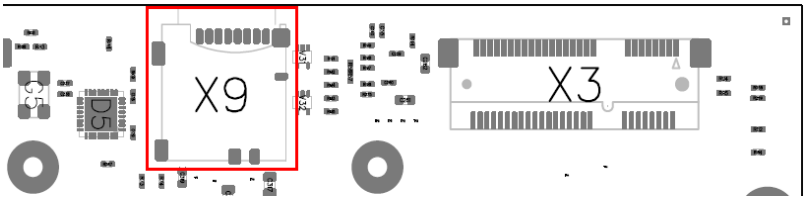

Figure 21: Position of microSD card socket X9

3.3.8 USB

The TI USB 3.0 Hub TUSB8041 connected to the USB 3.0 OTG port of the TQMLS1012AL provides four USB HOST ports.

Two ports are routed as USB 3.0 interfaces to a stacked connector (X6), the other two ports are routed as USB 2.0 interfaces to the two Mini PCIe connectors. The I²C interface of the TUSB8041 can be connected via optional 0 Ω bridges to access its registers.

The I²C address is `0x44 / 100 0100b`, see also Table 5.

A power distribution switch provides the 5 V supply for the USB connectors. The components used monitor the current and can switch off the bus voltage in the event of overload and/or overheating.

Table 24 shows the wiring of the unused USB pins of the LS1012A CPU.

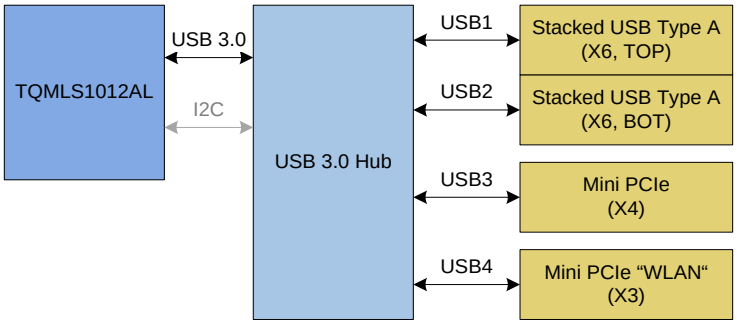

Figure 22: Block diagram USB

Table 24: Unused LS1012A USB pins

Pin	Name	Target pin / Net	Remark
TP62	USB_VBUS	VCC5V5	0 Ω series resistor
TP54	USB1_PWRFAULT	GND	1 kΩ Pull-Down

The USB host port of the TQMLS1012AL provides a theoretical data rate of 5 Gbit/s (gross). This is divided among the connected ports. Depending on the software and hardware used, the effective read and write rates of the ports may vary.

Table 25: Characteristics USB Host

Parameter	Min.	Typ.	Max.	Unit	Remark
Voltage	4.75	5	5.25	V	Preliminary values
Current	0.89	1.02	1.143	A	Per channel, preliminary values

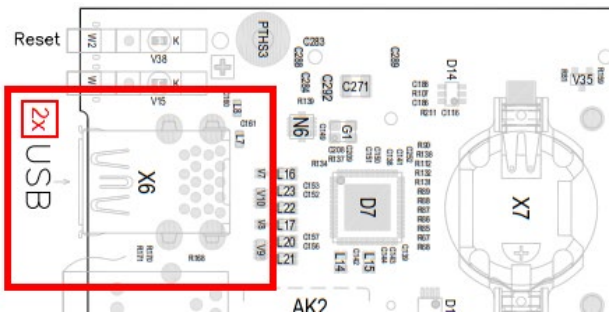

Figure 23: Position of USB 3.0 stacked socket X6

3.3.9 WLAN

A USB host and an I²C interface are provided to access WLAN networks via an additional Mini PCIe slot (full-size).

Half-size and full-size cards are supported. Half-size cards can be extended to full-size with card extenders.

The power supply is implemented with 3.3 V and 1.5 V and must be activated separately on the port expander with VCC_WLAN_EN_1V5 and VCC_WLAN_EN_3V3.

The voltages provided for the WLAN card may be loaded with the maximum currents specified in Table 27.

The Mini PCIe slot is not connected to the PCIe bus of the TQMLS1012AL. Communication with the host has to take place via USB or I²C. If I²C is used, it has to be ensured that the I²C address used by the Mini PCIe card is not already used by a participant on the MBLS1012AL or in the PCIe slot, see also Table 5. LED_WLAN_WL# is connected by default.

Table 26: Pinout WLAN module /Mini PCIe (USB) X3

Target pin / Net	Pin name	Pin		Pin name	Target pin / Net
NC	WAKE#	1	2	+3.3Vaux	V_3V3_WLAN
NC	COEX1	3	4	GND	GND
NC	COEX1	5	6	+1.5V	V_1V5_WLAN
NC	CLKREQ#	7	8	UIM_PWR	NC
GND	GND	9	10	UIM_DATA	NC
NC	REFCLK–	11	12	UIM_CLK	NC
NC	REFCLK+	13	14	UIM_RESET	NC
GND	GND	15	16	UIM_SPU	NC
Key notch					
NC	UIM_IC_DM	17	18	GND	GND
NC	UIM_IC_DP	19	20	W_DISABLE1#	WLAN_DISABLE#, 4.7 kΩ Pull-Up
GND	GND	21	22	PERST#	WLAN_RST#
NC	PERn0	23	24	+3.3Vaux	V_3V3_WLAN
NC	PERp0	25	26	GND	GND
GND	GND	27	28	+1.5V	V_1V5_WLAN
GND	GND	29	30	SMB_CLK	I2C_3V3_SCL
NC	PETn0	31	32	SMB_DATA	I2C_3V3_SDA
NC	PETp0	33	34	GND	GND
GND	GND	35	36	USB_D–	USB_DN4_D–
GND	GND	37	38	USB_D+	USB_DN4_D+
V_3V3_WLAN	+3.3Vaux	39	40	GND	GND
V_3V3_WLAN	+3.3Vaux	41	42	LED_WWAN#	LED V18 (optional)
GND	GND	43	44	LED_WLAN#	LED V18
NC	Reserved	45	46	LED_WPAN#	LED V18 (optional)
NC	Reserved	47	48	+1.5V	V_1V5_WLAN
NC	Reserved	49	50	GND	GND
NC	W_DISABLE2#	51	52	+3.3Vaux	V_3V3_WLAN

Table 27: Maximum permitted current consumption WLAN

Voltage	Nominal value	I_{max}
V_3V3_WLAN	3.3 V	1.1 A
V_1V5_WLAN	1.5 V	0.375 A

Figure 24: Position of WLAN X3

3.4 Diagnostic and user interfaces

3.4.1 DIP switch S1

A 4-fold DIP switch is used to set boot configurations and select hardware settings.
The functions of the individual switches are described in the following table:

Table 28: DIP switch S1, functions

Slot	ON	OFF	Remark
1	Hard Coded RCW switched on	Hard Coded RCW switched off	In case the RCW cannot be read in the flash.
2	RESET_REQ# and RESET# connected	RESET_REQ# and RESET# separated	To prevent a boot loop in case of a boot error.
3	Debug UART on USB/header	Debug UART on OpenSDA	TX is not switched and can be received at both ends.
4	CPU JTAG switched off	CPU JTAG switched on	–

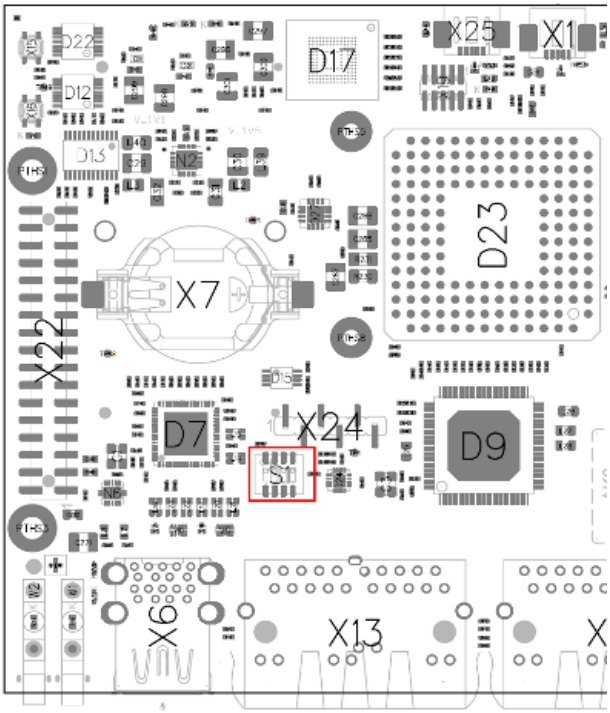

Figure 25: Position of DIP switch S1

3.4.2 GPIOs

GPIO pins from two different sources are available on the MBLS1012AL.

Native GPIOs

The TQMLS1012AL provides six GPIO signals on the MBLS1012AL. Four of these can be accessed at Header X22, see also 3.1.5.
All GPIO signals configured as input are interrupt capable.

Table 29: Electrical characteristics of 1.8 V GPIOs

Wert	Min.	Typ.	Max.	Unit	Remark
Voltage level	–	1.8	–	V	–
Output impedance	30	45	60	Ω	Preliminary values, see (1), table 5
Switchable load High	–0.5	–	–	mA	See (1), table 33
Switchable load Low	0.5	–	–	mA	See (1), table 33

Attention: GPIO1_29	
	GPIO1_29 can only be configured as an output. This pin must not be pulled Low during the reset cycle! See also (1), table 1 (GPIO1_29) note 5, and (2), chapter 20.1.

Port Expander GPIO:

Two GPIO port expanders are used (see also section 3.1.5), of which three pins are available on Header 22, see also 3.4.3.

GPIO pins which are implemented via a port expander are usually not suitable for time-critical I/O operations due to their indirect connection to the CPU. In addition, it should be noted that these pins are only available with a delay at boot time, since the I^2C driver must first be loaded for the configuration.

The nominal signal level of the GPIO signals GPIO_3V3_[3:1] is 3.3 V. However, the pins are 5 Volt tolerant and can be operated with an external signal level up to a maximum of 5.5 V.

At the pins GPIO_3V3_[3:1], a current of max. 25 mA can be switched.

For more detailed information, refer to the data sheet of the port expander.

Table 30: GPIO assignment

Header X22	Target pin / Net	Signal level	Remark
25	GPIO1_29	1.8 V	See above attention note
23	GPIO1_28	1.8 V	–
–	GPIO1_27	1.8 V	Interrupt input, 8-fold GPIO expander
21	GPIO1_26	1.8 V	–
19	GPIO1_25	1.8 V	–
–	GPIO1_24	1.8 V	Interrupt input, 16-fold GPIO expander
16	GPIO_3V3_1	3.3 V	5 V tolerant
18	GPIO_3V3_2	3.3 V	5 V tolerant
20	GPIO_3V3_3	3.3 V	5 V tolerant

3.4.3 Header X22

The MBLS1012AL provides a 34-pin, 100 mil header. On this header all unused signals and those which should be easy to reach are provided. In addition to the signals, 24 V, 5 V, 3.3 V and 1.8 V are available on the header.

Table 31: Pinout header X22

Pin	Pin name	Remark
1	GND	–
2	V_24V	Note the Attention Hint below
3	V_5V	0.75 A maximum
4	GND	–
5	GND	–
6	V_3V3	1.5 A maximum
7	I2C_3V3_SDA	3.3 V
8	V_1V8_PMIC_OUT	1 A maximum
9	I2C_3V3_SCL	3.3 V
10	GND	–
11	V_3V3	–
12	GND	–
13	SDHC1_CD#	1.8 V / Option eMMC: GPIO1_21
14	GND	–
15	SDHC1_WP	1.8 V
16	GPIO_3V3_1	3.3 V / Port Expander
17	TA_TMP_DETECT#	1.8 V / 10 kΩ Pull-Up
18	GPIO_3V3_2	3.3 V / Port Expander
19	GPIO1_25	1.8 V
20	GPIO_3V3_3	3.3 V / Port Expander
21	GPIO1_26	1.8 V
22	PMIC_INT#	1.8 V
23	GPIO1_28	1.8 V
24	PMIC_EN	1.8 V
25	GPIO1_29	1.8 V
26	TEMP_EVENT#	1.8 V
27	SATA_DEVSLP#	3.3 V
28	QSPI_DATA2	1.8 V / alternative: I2C2_SCL
29	RESET_1V8#	1.8 V
30	QSPI_DATA3	1.8 V / alternative: I2C2_SDA
31	RESET_3V3#	3.3 V
32	GND	–
33	RTC_SQW/INT#	3.3 V
34	GND	–

3.4.3 Header X22 (continued)

Attention: Power drawn from V_24V, and V_1V8_PMIC_OUT	
	The current drawn from V_24V (pin 2) is added to the current consumption of MBLS1012AL and TQMLS1012AL. Any additional power required at the voltage input of the MBLS1012AL has to be taken into account. The maximum current load of the fuse has to be observed. The power taken from V_1V8_PMIC_OUT (pin 8) is added to the power consumption at V_3V3_IN (balls G14, H4, J14) of the TQMLS1012AL. If power is taken from V_1V8_PMIC_OUT and there are doubts about the existing utilization of the V_3V3 power budget, the external current consumption at V_3V3 (e.g. at X22 pins 2 and 11) must be restricted accordingly. V_1V8_PMIC_OUT supplies critical components on the TQMLS1012AL. If this voltage rail is used to supply external components, it has to be ensured that the function of the TQMLS1012AL is not impaired. This can be achieved by filtering V_1V8_PMIC_OUT on the carrier board using a suitable circuit.

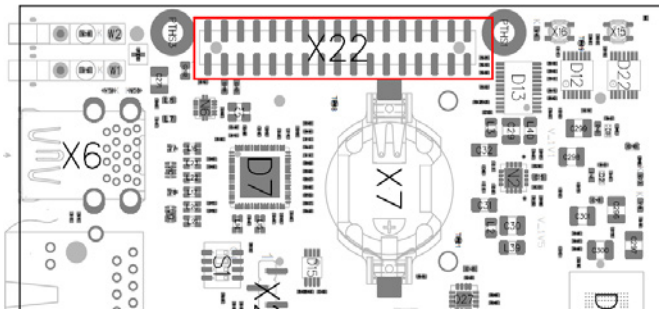

Figure 26: Position of header X22

Table 32: X22, type of header

Manufacturer / part number	Description
Fischer Elektronik / SL 22 124 60 G	Header, 100 mil pitch, 2 × 17 pins

3.4.4 LEDs

The MBLS1012AL provides 13 diagnosis and Status LEDs (plus the LEDs at the Ethernet ports) to indicate the system condition. The following table shows the function of all LEDs.

Table 33: Status LEDs

Interface	LED	Colour	Function
Mini PCIe	V28	Green	Mini PCIe WWAN, can be changed to WLAN or WPAN by assembly option
WLAN	V18	Green	Mini PCIe WLAN, can be changed to WWAN or WPAN by assembly option
GPIO	V15	Green	LED on 16 Port Expander Port IO1_0 (lit when pin is “Low”). With light guide to front panel
	V16	Green	LED on Port Expander Port IO1_1 (lit when pin is “Low”)
Power	V27	Green	Status 24 V (lights up when supply 24 V is active)
	V26	Green	Status 5 V (lights up when supply 5 V is active)
	V25	Green	Status 3.3 V (lights up when supply 3.3 V is active)
	V22	Green	Status 2.5 V (lights up when supply 2.5 V is active)
	V24	Green	Status 3.3 V Mini PCIe (lights up when supply 3.3 V for Mini PCIe is active)
	V23	Green	Status 3.3 V WLAN (lights up when power supply 3.3 V for Mini PCIe is active)
OpenSDA	V21	Green	Indicator LED for OpenSDA Interface
Reset	V38	Red	Reset LED (lights up when TQMLS1012AL is in reset). With light guide to front panel
SATA (M.2)	V17	Green	SATA Device Activity
Ethernet	–	–	See 3.3.3 and 3.3.4

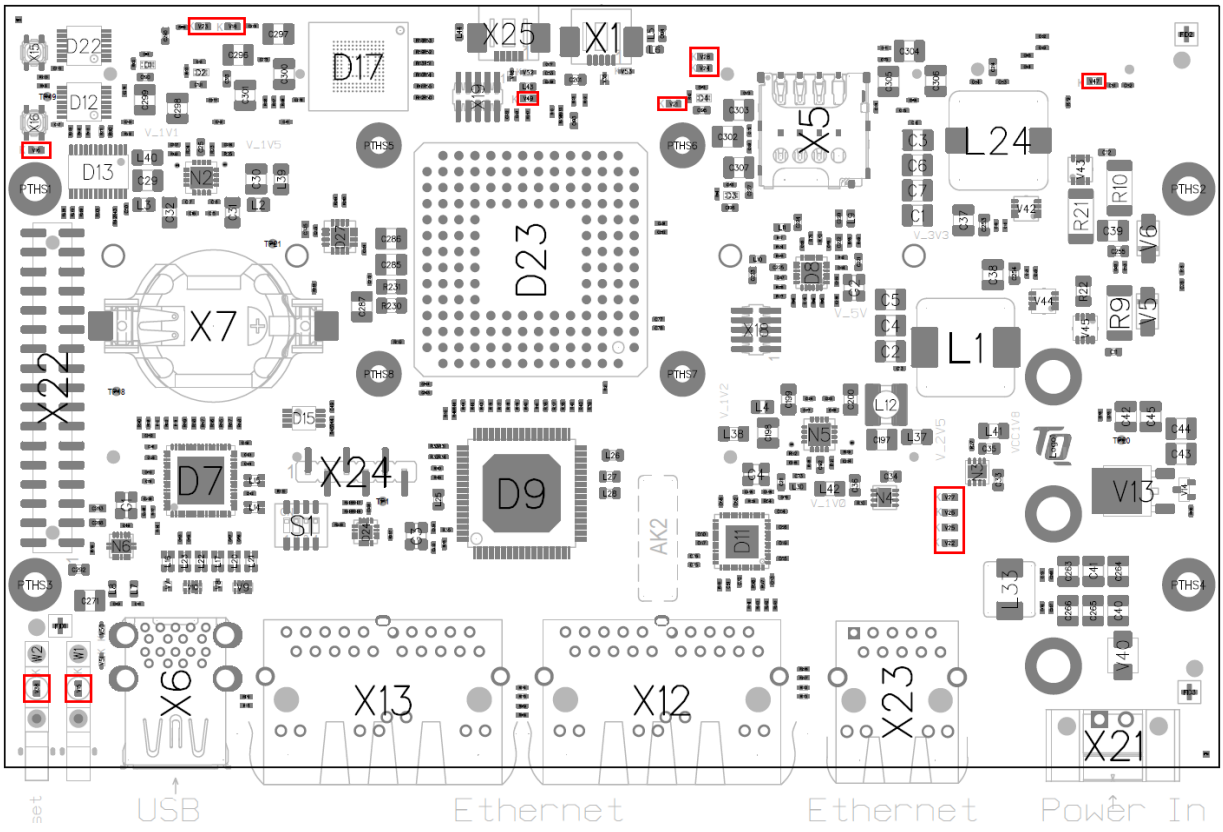

Figure 27: Position of Status LEDs

3.4.5 Push buttons

For tests during the development phase, the MBLS1012AL provides three push buttons connected to the port expanders. By using the interrupt signals at GPIO1_24 and GPIO1_27 interrupts can be triggered with the push buttons.
The signals between the push button and the port expander have 10 kΩ Pull-Up resistors.

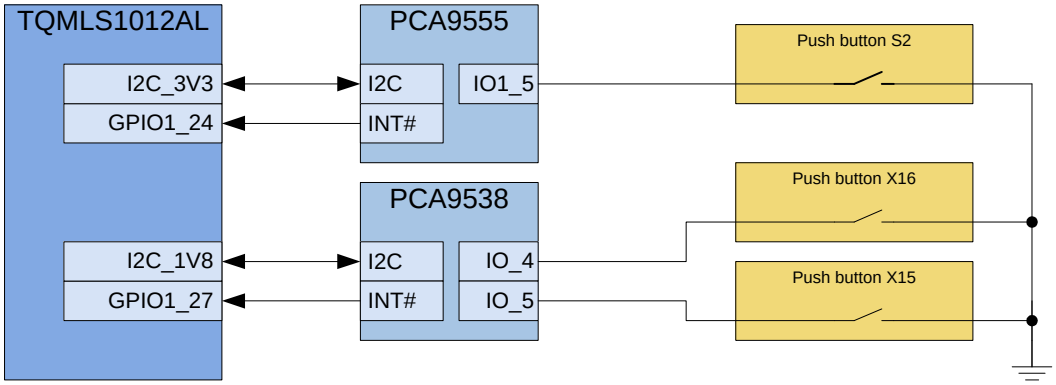

Figure 28: Block diagram push buttons

Table 34: Push buttons

Push button	Function
S2	PCA9555PW pin 18, GPIO1_5
X15	PCA9538ABS pin 8, GPIO_5
X16	PCA9538ABS pin 7, GPIO_4

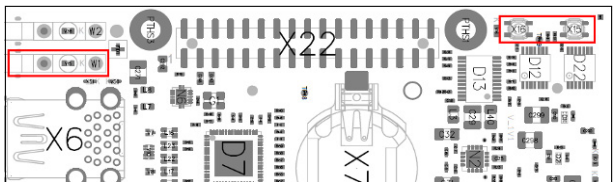

Figure 29: Position of push buttons

3.4.6 Reset Push button

For information on reset and reset button, see section 3.1.6.

3.4.7 JTAG

The JTAG port of the TQMLS1012AL is routed to a standard ARM 10-pin JTAG connector.

The OpenSDA microcontroller JTAG interface is also routed to a 10-pin connector with standard ARM assignment.

For the OpenSDA circuit see section 3.4.8.

NXP provides the "Code Warrior Development Studio for QorIQ LS series" and the "CodeWarrior TAP" programmer for development and to program the LS1012A processor.

The JTAG test reset pin (TP18, JTAG_TRST#) must be pulled to ground simultaneously with PORESET# during normal operation. This is achieved by means of a 0 Ohm jumper on the mainboard. If a boundary scan is to be performed, this jumper must be removed and the two signals controlled accordingly.

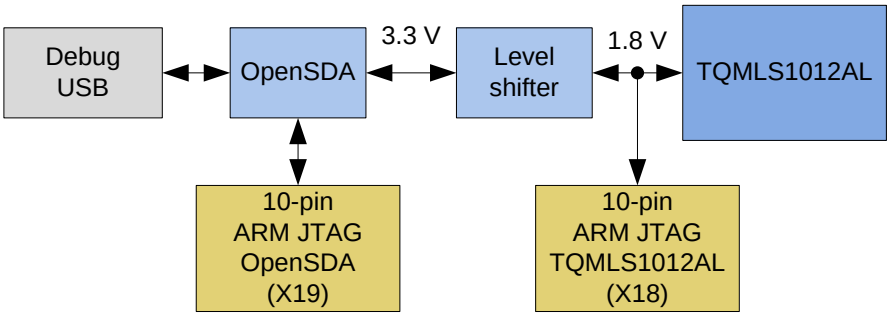

Figure 30: Block diagram JTAG

The following table shows suitable JTAG adapters.

Table 35: JTAG adapters

Manufacturer	Part number	Details
Lauterbach	JTAG-ARMV8-A/R, LA-3743	Debugger for Cortex-A/R (ARMv8 32/64-bit)
	CONV-ARM20/MIPI34, LA-3770	ARM Converter ARM-20 to MIPI-10/20/34
NXP	CWH-CTP-BASE-HE, 935328292598	CodeWarrior TAP
	CWH-CTP-CTX10-YE, 935327448598	ARM Mini 10-Pin JTAG
Ronetix	PEEDI, PD-CORTEX-GDB	Flash-Programmer & High Speed JTAG Emulator
	FLASH PROGRAMMER, PGM-CORTEX	Flash-Programmer
	ADAPTER_CORTEX10	Adapter PEEDI to CORTEX-10

3.4.7 JTAG (continued)

The JTAG interface is not protected against ESD.
The following table shows the pin assignment of the JTAG connector.

Table 36: Pinout JTAG header X18

Pin	Pin name	Target pin / Net
1	VTref / VCC	V_1V8
2	JTAG_CPU_TMS	JTAG_TMS (TP17)
3	GND	GND
4	JTAG_CPU_TCK	JTAG_TCK (TP16)
5	GND	GND
6	JTAG_CPU_TDO	JTAG_TDO (TP15)
7	KEY	NC
8	JTAG_CPU_TDI	JTAG_TDI (TP14)
9	GND_DETECT_1V8	GND_DETECT_3V3
10	JTAG_CPU_RESET#	RESET_IN#

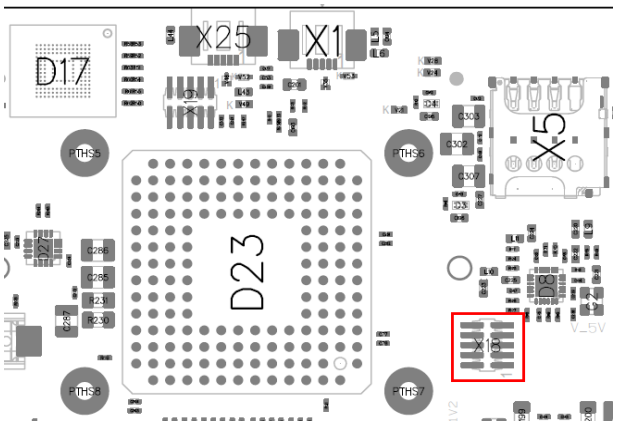

Figure 31: Position of JTAG header X18

3.4.8 DAPLink / OpenSDA

A circuit for a DAPLink/OpenSDA programmer is prepared on the MBLS1012AL. Currently this circuit is not supported.

4. SOFTWARE

No software is required for the MBLS1012AL.
Suitable software is only required on the TQMLS1012AL and is not a part of this specification.
More information can be found in the Support Wiki for the TQMLS1012AL.

5. MECHANICS

5.1 TQMLS1012AL and MBLS1012AL dimensions

The MBLS1012AL has overall dimensions (length × width) of 160 mm × 100 mm.
The MBLS1012AL has a maximum height of approximately 29 mm.
The MBLS1012AL has four mounting holes with a diameter of 2.7 mm and three 2.2 mm heat sink mounting holes.
The MBLS1012AL weighs approximately 147 grams including TQMLS1012AL.

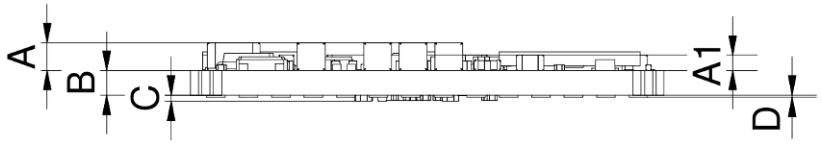

Figure 32: TQMLS1012AL, dimensions, height profile

Table 37: TQMSL1012AL dimensions

Parameter	Description	Nominal [mm]	Tolerance [mm]
A	Component height top side	1.7	Max.
A1	Component height CPU	0.81	±0.13
B	Thickness of PCB	1.65	±0.16
C	Component height bottom side	0.4	Max.
D	Height LGA balls	0.125	+0.075 −0.025

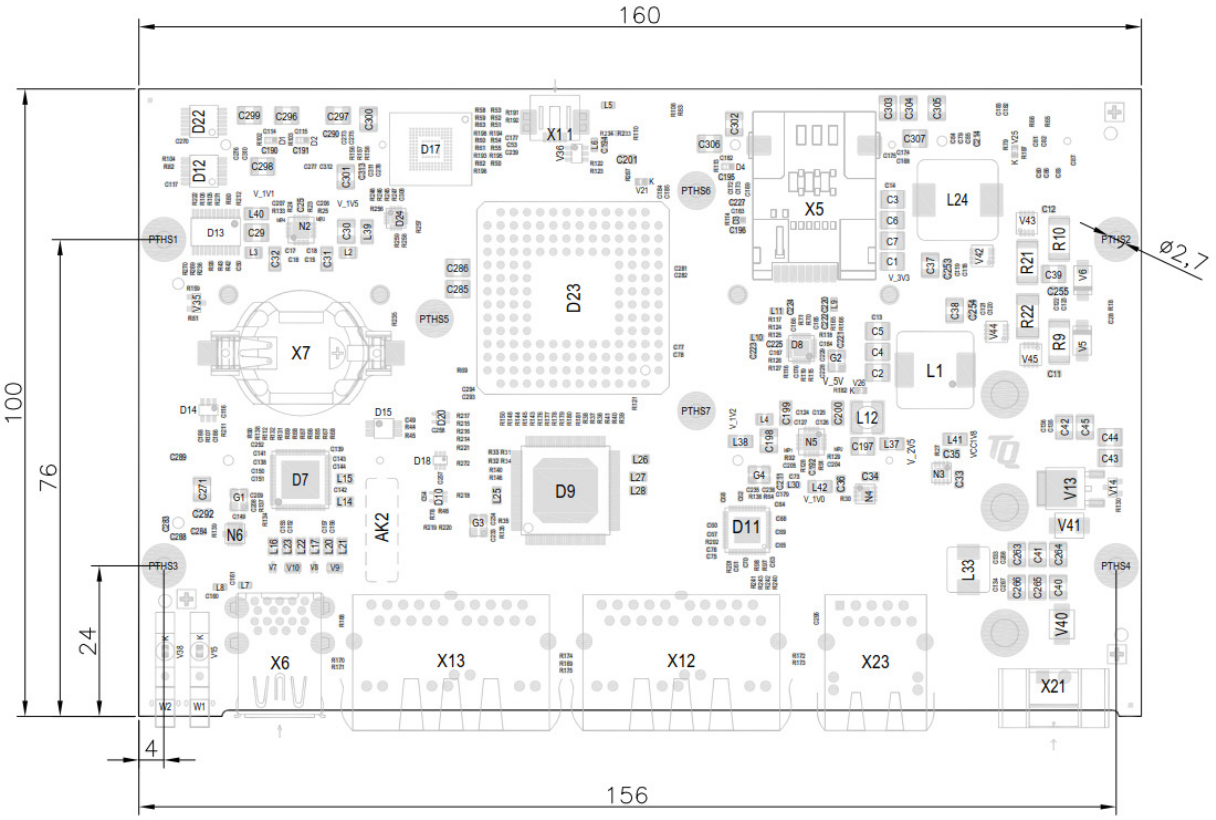

Figure 33: MBLS1012AL, dimensions

5.2 Housing

The form factor and the mounting holes of the MBLS1012AL are designed for installation in a standard EURO housing.

5.3 Thermal management

The MBLS1012AL has a maximum peak power consumption of approx. 51 W at the 24 V supply. This corresponds to a typical maximum peak current consumption of 2.1 A. In most applications, however, the power consumption will be significantly lower. Depending on the application, the value must be assessed individually.

A maximum of approx. 3.9 W must be dissipated from the TQMLS1012AL. This value also represents a theoretical maximum and depends strongly on the application and the individual load. Required measures must be evaluated accordingly for the intended application.

Three holes are provided on the MBLS1012AL to mount a heat sink. The heat sink should be fastened to the MBLS1012AL with M2 screws and spacers as well as a thermal gap pad. More information is to be taken from the TQMLS1012AL User's Manual.

Attention: TQMLS1012AL heat dissipation	
	The LS1012A CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMLS1012AL must be taken into consideration when connecting the heat sink. The TQMLS1012AL is not the highest component. Inadequate cooling connections can lead to overheating of the MBLS1012AL and thus malfunction, deterioration or destruction.

5.4 Assembly

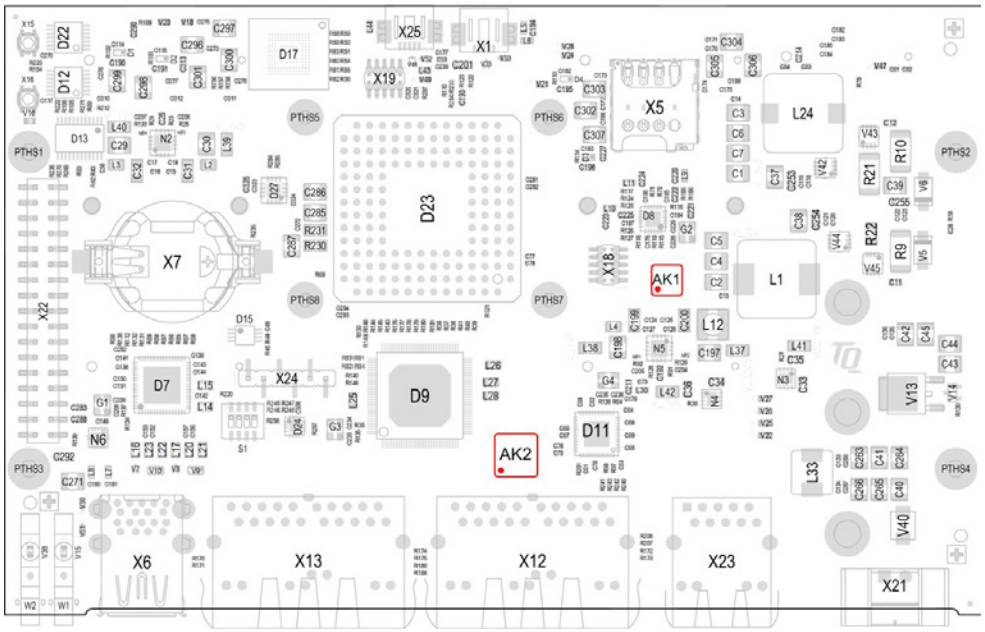

Figure 34: MBLS1012AL, component placement top

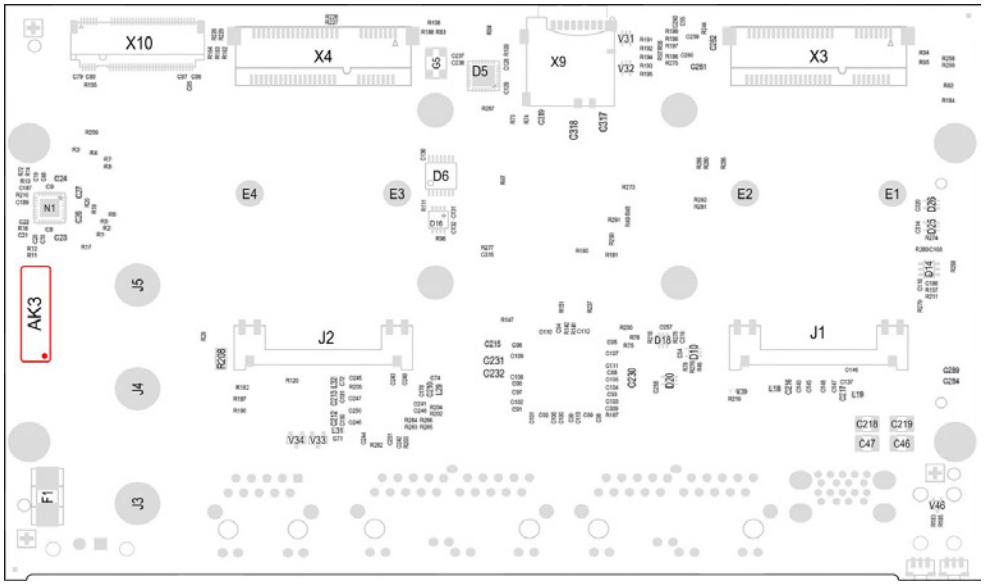

Figure 35: MBLS1012AL, component placement bottom

The labels on the MBLS1012AL revision 02xx show the following information:

Table 38: Labels on MBLS1012AL revision 02xx

Label	Content
AK1	Serial number
AK2	First MAC address plus three additional reserved consecutive MAC addresses
AK3	MBLS1012AL version and revision, tests performed

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBLS1012AL is a development platform, no EMC tests have been performed.

6.2 ESD

ESD protection is provided on most interfaces of the MBLS1012AL.
The circuit diagram shows which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 39: Climatic and operational conditions MBLS1012AL

Parameter	Range	Remark
Permitted environmental temperature	0 °C to +60 °C	With Lithium battery
Permitted environmental temperature	0 °C to +70 °C	Without Lithium battery
Permitted storage temperature	–10 °C to +60 °C	With Lithium battery
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMLS1012AL heat dissipation	
	The LS1012A CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMLS1012AL must be taken into consideration when connecting the heat sink. The TQMLS1012AL is not the highest component. Inadequate cooling connections can lead to overheating of the TQMLS1012AL and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBLS1012AL. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBLS1012AL.
The MBLS1012AL is designed to be insensitive to vibration and impact.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBLS1012AL is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBLS1012AL was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000.
The MBLS1012AL must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the MBLS1012AL enable compliance with EuP requirements for the MBLS1012AL.

8.5 Packaging

The MBLS1012AL is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

Due to technical reasons a battery is necessary for the MBLS1012AL. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBLS1012AL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBLS1012AL is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 40: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
CAN	Controller Area Network
CEC	Consumer Electronics Control
CPI	CEC Programming Interface (Silicon Image)
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIP	Dual In-line Package
EDID	Extended Display Identification Data
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
ESD	Electrostatic Discharge
EuP	Energy using Products
FFC	Flat Flex Cable
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communications (Groupe Spécial Mobile)
HDMI	High Definition Multimedia Interface
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IFC	Integrated Flash-Controller
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LDO	Low Drop-Out
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signalling
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF	Mean operating Time Between Failures
NA	Not Available
NC	Not Connected
O	Output
OpenSDA	Serial and Debug Adapter (NXP)
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (layer of the OSI model)
PMC	Power Management Controller
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface

9.1 Acronyms and definitions (continued)

Table 40: Acronyms (continued)

Acronym	Meaning
RCW	Reset Configuration Word
REACH	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232, RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SAI	Serial Audio Interface
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SD/MMC	Secure Digital Multimedia Card
SDHC	Secure Digital High Capacity
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SMBUS	System Management Bus
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
SWD	Serial Wire Debug
TDM	Time-Division Multiplexing
THT	Through-Hole Technology
TPI	Transmitter Programming Interface (Silicon Image)
UART	Universal Asynchronous Receiver/Transmitter
UCC	Unified Communications Controller
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
VHDL	VHSIC Hardware Description Language
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 41: Further applicable documents

No.	Name	Rev., Date	Company
(1)	QorIQ® LS1012A Data Sheet	Rev. 2.0, 01/2019	NXP
(2)	QorIQ® LS1012A Reference Manual	Rev. 2, 02/2019	NXP
(3)	QorIQ® LS1012A Design Checklist, AN5192	Rev. 2, 05/2019	NXP
(4)	User's Manual TQMLS1012AL	– current –	TQ-Systems

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Info@TQ-Group | TQ-Group

Technology in Quality