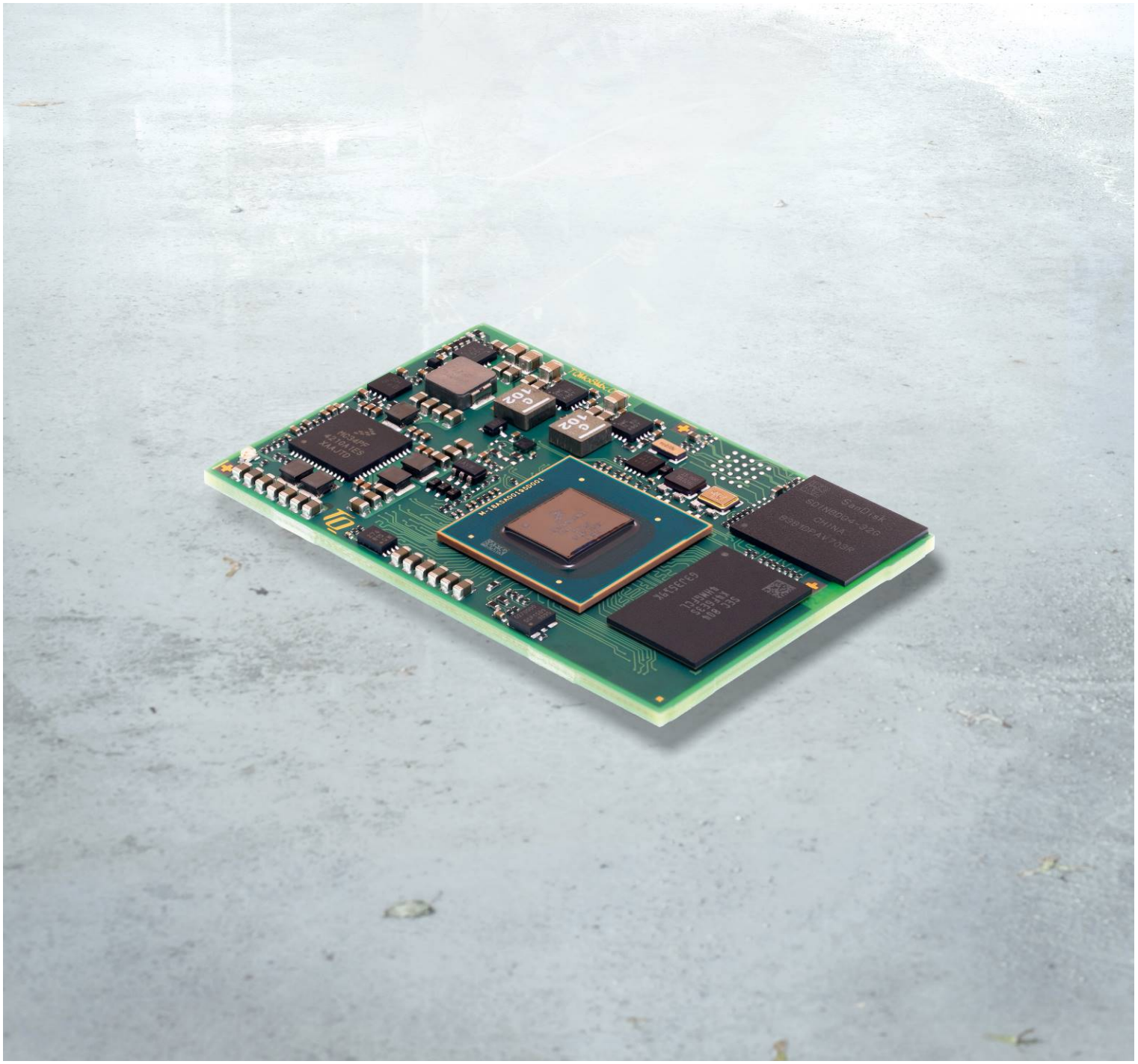
TQMa8Mx
User's Manual

TQMa8Mx UM 0100
11.07.2020



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	11.07.2020	Petz		Initial release

1. ABOUT THIS MANUAL

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa8Mx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8Mx circuit diagram
- MBa8Mx User's Manual
- i.MX 8M Data Sheet
- i.MX 8M Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8Mx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa8Mx Rev. 02xx, in combination with the MBa8Mx and refers to some software settings. The MBa8Mx serves as an evaluation board for the TQMa8Mx.

A certain TQMa8Mx version does not necessarily provide all features described in this User's Manual.

This User's Manual does also not replace the NXP i.MX 8M Reference Manual (2).

The CPU derivatives i.MX 8MD (Dual), i.MX 8MQ (Quad), and i.MX 8MQL (Quad Light) feature ARM® Cortex™ A53 cores, and one ARM® Cortex™-M4 co-processor. In addition, the CPUs also provide a GPU as well as a VPU, which features a VP9 decoder. The integrated display controller can control two independent 4Kp60, and supports HDR10.

The TQMa8Mx is a universal Minimodule based on these NXP ARM® Cortex™ A53 i.MX 8M CPUs, see also Table 6.

An i.MX 8M Cortex™ A53 core typically operates at 1.3 GHz.

The TQMa8Mx extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX 8M derivative (i.MX 8MD, i.MX 8MQ or i.MX 8MQL) can be selected for each requirement.

All essential CPU signals are routed to the connectors. There are therefore no restrictions for customers using the TQMa8Mx with respect to an integrated customised design. All essential components like CPU, LPDDR4 SDRAM, eMMC, RTC, EEPROM, power supply, and power management are already integrated on the TQMa8Mx.

The main features of the TQMa8Mx are:

- NXP i.MX 8M CPU with up to 4 × ARM® Cortex™ A53 and 1 × ARM® Cortex™ M4F cores
- CPU derivatives: i.MX 8MD, i.MX 8MQ, i.MX 8MQL
- Up to 4 Gbyte LPDDR4 SDRAM, optional additional ECC
- Up to 64 Gbyte eMMC NAND flash
- Up to 256 Mbyte QSPI NOR flash (optional)
- 64 kbit EEPROM
- EEPROM + temperature sensor
- On-board RTC
- NXP Power Management Integrated Circuit PF4210
- All essential I.MX 8M signals are routed to the TQMa8Mx connectors
- Extended temperature range
- Boot Mode selection on TQMa8Mx
- 5 V single supply voltage

2.1 Block diagram i.MX 8M

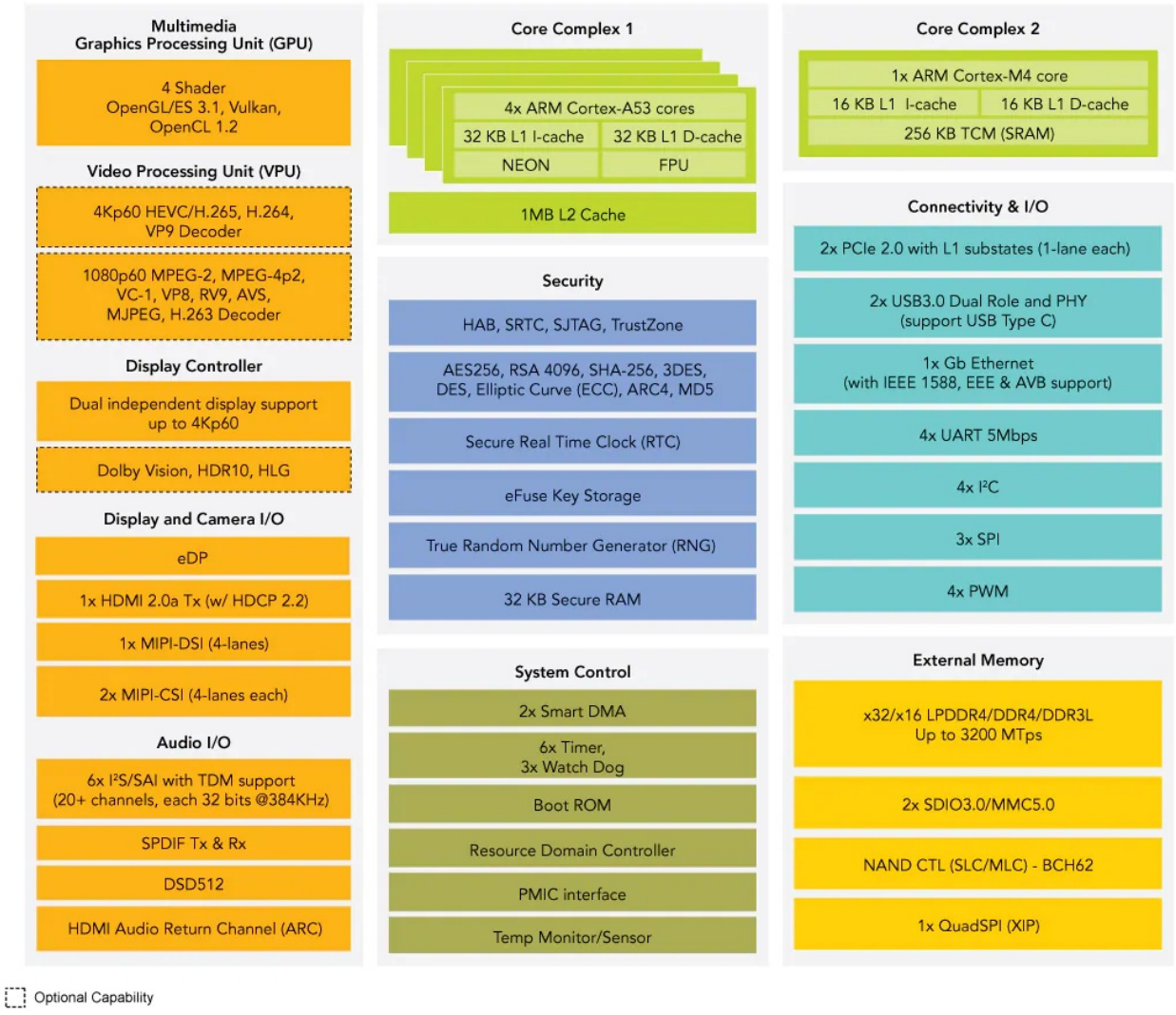


Figure 1: Block diagram i.MX 8M CPU family
(Source: NXP)

2.2 Key functions and characteristics

The following components are implemented on the TQMa8Mx:

- NXP CPU i.MX 8MD (Dual) / i.MX 8MQ (Quad) / i.MX 8MQL (QuadLite)
- LPDDR4 SDRAM
- eMMC NAND flash
- QSPI NOR flash
- EEPROM
- EEPROM + Temperature sensor
- RTC
- Reset structure
- Power supply with Power Sequencing (single 5 V supply)
- Voltage monitoring
- Boot configuration
- Three connectors (2 × 120 pins, 1 × 100 pins)

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa8Mx, and the BSP provided by TQ-Systems, see also chapter 5.

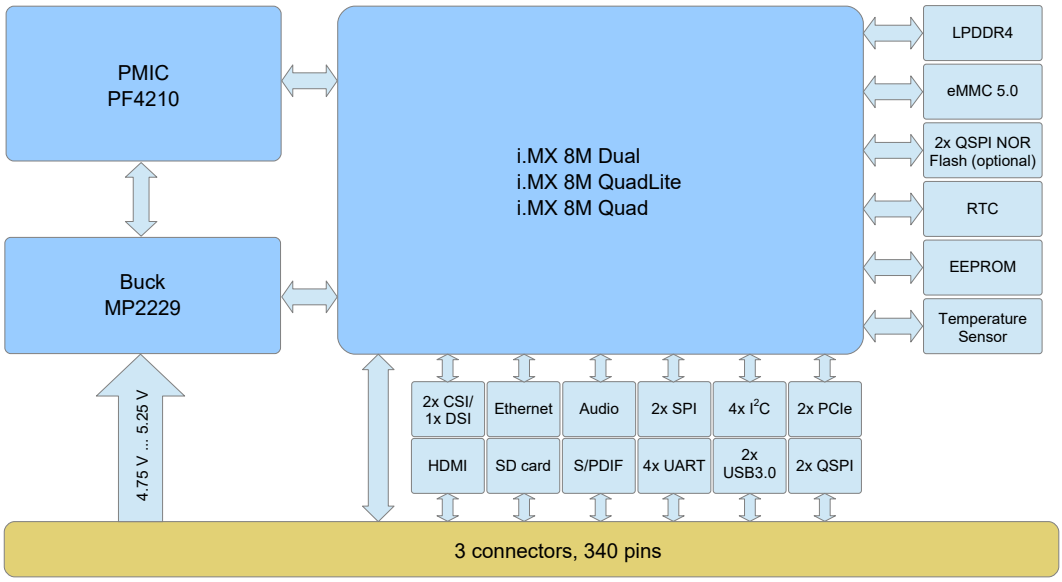


Figure 2: Block diagram TQMa8Mx

3.1 TQMa8Mx internal interfaces

The following interfaces are not routed to the TQMa8Mx connectors and are used exclusively on the TQMa8Mx:

Table 2: TQMa8Mx internal interfaces

Interface	Chapter	Remark
DDR SDRAM	3.3.3	LPDDR4, 32 bit
USDHC1	3.3.4	eMMC, 8 bit
QSPIA & QSPIB	3.3.5	Conditionally available, more information can be found in chapter 3.4.9.

3.2 Interfaces to other systems and devices

3.2.1 i.MX 8M pin multiplexing

When using the I.MX 8M signals, the multiple pin configurations by different I.MX 8M-internal function units must be taken note of. NXP provides a tool showing the multiplexing and simplifies the selection and configuration (NXP Pin Mux Tool).

The pin assignment listed in Table 3, Table 4, and Table 5 refers to the corresponding BSP provided by TQ-Systems in combination with the MBa8Mx.

The electrical and pin characteristics are to be taken from the i.MX 8M Data Sheet (1), the i.MX 8M Reference Manual (2), and the PMIC Data Sheet (7).

Attention: Destruction or malfunction, i.MX 8M pin multiplexing, TQMa8Mx reserved pins	
	Depending on the configuration, many i.MX 8M balls can provide several different functions. Please take note of the information in the i.MX 8M Reference Manual (2), and the i.MX 8M Errata (3) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa8Mx. The meanings given in the following tables must be observed: RFU: Reserved pins without function. To support future TQMa8Mx versions, these pins must not be connected. DNC: These pins must never be wired and must be left open.

3.2.2 Pinout connectors X1, X2, X3

Table 3: Pinout connector X1

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	5 V	Supply	VCC5V_IN	1	2	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	3	4	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	5	6	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	7	8	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	9	10	VCC5V_IN	Supply	5 V	P	–
–	P	5 V	Supply	VCC5V_IN	11	12	VCC5V_IN	Supply	5 V	P	–
–	P	0 V	Ground	DGND	13	14	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	15	16	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	17	18	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	19	20	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	21	22	I2C4_SDA	I2C	3.3 V	I/O	F9
E9	I/O	3.3 V	I2C	I2C3_SDA	23	24	I2C4_SCL	I2C	3.3 V	O	F8
G8	O	3.3 V	I2C	I2C3_SCL	25	26	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	27	28	UART2_TXD	UART	1.8 V / 3.3 V [1]	O	D6
A7	O	1.8 V / 3.3 V [1]	UART	UART1_TXD	29	30	UART2_RXD	UART	1.8 V / 3.3 V [1]	I	B6
C7	I	1.8 V / 3.3 V [1]	UART	UART1_RXD	31	32	UART4_TXD	UART	1.8 V / 3.3 V [1]	O	D7
B7	O	1.8 V / 3.3 V [1]	UART	UART3_TXD	33	34	UART4_RXD	UART	1.8 V / 3.3 V [1]	I	C6
A6	I	1.8 V / 3.3 V [1]	UART	UART3_RXD	35	36	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	37	38	CSI2_CLK_N	CSI	1.8 V	O	A19
–	P	0 V	Ground	DGND	39	40	CSI2_CLK_P	CSI	1.8 V	O	B19
A22	O	1.8 V	CSI	CSI1_CLK_N	41	42	DGND	Ground	0 V	P	–
B22	O	1.8 V	CSI	CSI1_CLK_P	43	44	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	45	46	CSI2_D3_N	CSI	1.8 V	I	C19
–	P	0 V	Ground	DGND	47	48	CSI2_D3_P	CSI	1.8 V	I	D19
C21	I	1.8 V	CSI	CSI1_D3_N	49	50	DGND	Ground	0 V	P	–
D21	I	1.8 V	CSI	CSI1_D3_P	51	52	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	53	54	CSI2_D2_N	CSI	1.8 V	I	A21
–	P	0 V	Ground	DGND	55	56	CSI2_D2_P	CSI	1.8 V	I	B21
B24	I	1.8 V	CSI	CSI1_D2_N	57	58	DGND	Ground	0 V	P	–
C23	I	1.8 V	CSI	CSI1_D2_P	59	60	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	61	62	CSI2_D1_N	CSI	1.8 V	I	A20
–	P	0 V	Ground	DGND	63	64	CSI2_D1_P	CSI	1.8 V	I	B20
C22	I	1.8 V	CSI	CSI1_D1_N	65	66	DGND	Ground	0 V	P	–
D22	I	1.8 V	CSI	CSI1_D1_P	67	68	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	69	70	CSI2_D0_N	CSI	1.8 V	I	C20
–	P	0 V	Ground	DGND	71	72	CSI2_D0_P	CSI	1.8 V	I	D20
A23	I	1.8 V	CSI	CSI1_D0_N	73	74	DGND	Ground	0 V	P	–
B23	I	1.8 V	CSI	CSI1_D0_P	75	76	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	77	78	QSPI_B_DQS	QSPI_B [2]	1.8 V	I	K19
M20	I	1.8 V	QSPI_A [2]	QSPI_A_DQS	79	80	QSPI_B_SS1#	QSPI_B	1.8 V	O	H20
G21	O	1.8 V	QSPI_A	QSPI_A_SS1#	81	82	QSPI_B_SS0#	QSPI_B [2]	1.8 V	O	F21
H19	O	1.8 V	QSPI_A [2]	QSPI_A_SS0#	83	84	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	85	86	QSPI_B_DATA3	QSPI_B [2]	1.8 V	I/O	M19
J21	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA3	87	88	QSPI_B_DATA2	QSPI_B [2]	1.8 V	I/O	L19
H22	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA2	89	90	QSPI_B_DATA1	QSPI_B [2]	1.8 V	I/O	J22
J20	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA1	91	92	QSPI_B_DATA0	QSPI_B [2]	1.8 V	I/O	L20
G20	I/O	1.8 V	QSPI_A [2]	QSPI_A_DATA0	93	94	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	95	96	QSPI_B_SCLK	QSPI_B [2]	1.8 V	O	H21
G19	O	1.8 V	QSPI_A [2]	QSPI_A_SCLK	97	98	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	99	100	ENET_MDC	ENET	1.8 V	O	N20
N19	I/O	1.8 V	ENET	ENET_MDIO	101	102	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	103	104	ENET_TXC	ENET	1.8 V	O	T19
T20	I	1.8 V	ENET	ENET_RXC	105	106	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	107	108	DGND	Ground	0 V	P	–
T21	I	1.8 V	ENET	ENET_RX_CTL	109	110	ENET_TX_CTL	ENET	1.8 V	O	P19
U19	I	1.8 V	ENET	ENET_RD0	111	112	ENET_TD0	ENET	1.8 V	O	R20
U21	I	1.8 V	ENET	ENET_RD1	113	114	ENET_TD1	ENET	1.8 V	O	R21
U20	I	1.8 V	ENET	ENET_RD2	115	116	ENET_TD2	ENET	1.8 V	O	R19
V19	I	1.8 V	ENET	ENET_RD3	117	118	ENET_TD3	ENET	1.8 V	O	P20
–	P	0 V	Ground	DGND	119	120	DGND	Ground	0 V	P	–

1: Voltage can be set via NVCC_UART, pin X2-10.
2: Depending on the TQMa8Mx variant, one or both QSPI_A / QSPI_B interfaces are used by populated NOR flash.

3.2.2 Pinout connectors X1, X2, X3 (continued)

Table 4: Pinout connector X2

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	3.3 V	Supply	VCC3V3	1	2	DGND	Ground	0 V	P	–
F5	P	1.8 V / 3.3 V	Supply	NVCC_ECSPI	3	4	V_LICELL	Supply	3 V	P	–
–	P	0 V	Ground	DGND	5	6	NVCC_1V8	Supply	1.8 V	P	–
F6	O	3.3 V	SPDIF	SPDIF_TX	7	8	NVCC_SD2	Supply	1.8 V / 3.3 V	P	N23
G6	I	3.3 V	SPDIF	SPDIF_RX	9	10	NVCC_UART	Supply	1.8 V / 3.3 V	P	D8
E6	I	3.3 V	SPDIF	SPDIF_EXT_CLK	11	12	DGND	Ground	0 V	P	–
W6	I	3.3 V	Config	BOOT_MODE0	13	14	SYS_RST#	Config	3.3 V	I	–
V6	I	3.3 V	Config	BOOT_MODE1	15	16	ONOFF	Config	3.3 V	I	W21
K20	I/O	1.8 V	GPIO	GPIO3_IO16	17	18	DGND	Ground	0 V	P	–
E8	I/O	3.3 V	I2C	I2C1_SDA	19	20	GPIO3_IO17	GPIO	1.8 V	I/O	K22
E7	O	3.3 V	I2C	I2C1_SCL	21	22	GPIO3_IO18	GPIO	1.8 V	I/O	K21
–	P	0 V	Ground	DGND	23	24	I2C2_SCL	I2C	3.3 V	O	G7
A3	O	3.3 V	SAI	SAI1_MCLK	25	26	I2C2_SDA	I2C	3.3 V	I/O	F7
C1	O	3.3 V	SAI	SAI1_TXD7	27	28	DGND	Ground	0 V	P	–
B3	O	3.3 V	SAI	SAI1_TXD6	29	30	ECSPI1_SCLK	ECSPI	1.8 V / 3.3 V	O	D5
C2	O	3.3 V	SAI	SAI1_TXD5	31	32	ECSPI1_MISO	ECSPI	1.8 V / 3.3 V	I	B4
–	P	0 V	Ground	DGND	33	34	ECSPI1_MOSI	ECSPI	1.8 V / 3.3 V	O	A4
D2	O	3.3 V	SAI	SAI1_TXD4	35	36	ECSPI1_SS0	ECSPI	1.8 V / 3.3 V	O	D4
D1	O	3.3 V	SAI	SAI1_TXD3	37	38	DGND	Ground	0 V	P	–
B2	O	3.3 V	SAI	SAI1_TXD2	39	40	ECSPI2_SCLK	ECSPI	1.8 V / 3.3 V	O	C5
E2	O	3.3 V	SAI	SAI1_TXD1	41	42	ECSPI2_MISO	ECSPI	1.8 V / 3.3 V	I	B5
–	P	0 V	Ground	DGND	43	44	ECSPI2_MOSI	ECSPI	1.8 V / 3.3 V	O	E5
F2	O	3.3 V	SAI	SAI1_TXD0	45	46	ECSPI2_SS0	ECSPI	1.8 V / 3.3 V	O	A5
H1	O	3.3 V	SAI	SAI1_TXFS	47	48	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	49	50	SAI3_MCLK	SAI	3.3 V	O	D3
E1	O	3.3 V	SAI	SAI1_TXC	51	52	SAI3_RXD	SAI	3.3 V	I	F3
G1	I	3.3 V	SAI	SAI1_RXD7	53	54	SAI3_RXFS	SAI	3.3 V	I	G4
G2	I	3.3 V	SAI	SAI1_RXD6	55	56	SAI3_RXC	SAI	3.3 V	I	F4
F1	I	3.3 V	SAI	SAI1_RXD5	57	58	SAI3_TXD	SAI	3.3 V	O	C3
–	P	0 V	Ground	DGND	59	60	SAI3_TXFS	SAI	3.3 V	O	G3
J1	I	3.3 V	SAI	SAI1_RXD4	61	62	SAI3_TXC	SAI	3.3 V	O	C4
J2	I	3.3 V	SAI	SAI1_RXD3	63	64	DGND	Ground	0 V	P	–
H2	I	3.3 V	SAI	SAI1_RXD2	65	66	SAI2_MCLK	SAI	3.3 V	O	H5
L2	I	3.3 V	SAI	SAI1_RXD1	67	68	SAI2_RXD0	SAI	3.3 V	I	H6
K2	I	3.3 V	SAI	SAI1_RXD0	69	70	SAI2_RXFS	SAI	3.3 V	I	J4
L1	I	3.3 V	SAI	SAI1_RXFS	71	72	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	73	74	SAI2_RXC	SAI	3.3 V	I	H3
K1	O	3.3 V	SAI	SAI1_RXC	75	76	SAI2_TXD0	SAI	3.3 V	O	G5
M5	I	3.3 V	SAI	SAI5_RXD0	77	78	SAI2_TXFS	SAI	3.3 V	O	H4
L4	I	3.3 V	SAI	SAI5_RXD1	79	80	SAI2_TXC	SAI	3.3 V	O	J5
M4	I	3.3 V	SAI	SAI5_RXD2	81	82	DGND	Ground	0 V	P	–
K5	I	3.3 V	SAI	SAI5_RXD3	83	84	SAI5_RXC	SAI	3.3 V	O	L5
–	I	0 V	Ground	DGND	85	86	SAI5_RXFS	SAI	3.3 V	I	N4
W2	I	1.8 V	HDMI	HDMI_HPD	87	88	SAI5_MCLK	SAI	3.3 V	O	K4
W3	I/O	1.8 V	HDMI	HDMI_CEC	89	90	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	91	92	HDMI_TX0_P	HDMI	1.8 V	O	T1
–	P	0 V	Ground	DGND	93	94	HDMI_TX0_N	HDMI	1.8 V	O	T2
U2	O	1.8 V	HDMI	HDMI_TX1_P	95	96	DGND	Ground	0 V	P	–
U1	O	1.8 V	HDMI	HDMI_TX1_N	97	98	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	99	100	HDMI_TX2_P	HDMI	1.8 V	O	N2
–	P	0 V	Ground	DGND	101	102	HDMI_TX2_N	HDMI	1.8 V	O	N1
M1	O	1.8 V	HDMI	HDMI_TX3_P	103	104	DGND	Ground	0 V	P	–
M2	O	1.8 V	HDMI	HDMI_TX3_N	105	106	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	107	108	HDMI_AUXP	HDMI	1.8 V	I	V1
–	P	0 V	Ground	DGND	109	110	HDMI_AUXN	HDMI	1.8 V	I	V2
R3	O	1.8 V	HDMI	HDMI_DDC_SCL	111	112	DGND	Ground	0 V	P	–
P3	I/O	1.8 V	HDMI	HDMI_DDC_SDA	113	114	JTAG_TDI	JTAG	3.3 V	I	W5
V5	I	3.3 V	JTAG	JTAG_TMS	115	116	JTAG_TDO	JTAG	3.3 V	O	U5
T5	I	3.3 V	JTAG	JTAG_TCK	117	118	JTAG_TRST#	JTAG	3.3 V	I	U6
–	P	0 V	Ground	DGND	119	120	JTAG_MOD	JTAG	3.3 V	I	U7

3.2.2 Pinout connectors X1, X2, X3 (continued)

Table 5: Pinout connector X3

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
P7	I/O	3.3 V	GPIO	GPIO1_IO05	1	2	GPIO1_IO07	DNC [3]	3.3 V	I/O	N6
N5	I/O	3.3 V	DNC [3]	GPIO1_IO06	3	4	GPIO1_IO08	GPIO	3.3 V	I/O	N7
L7	O	3.3 V	USB	USB1_OTG_PWR	5	6	GPIO1_IO09	GPIO	3.3 V	I/O	M6
K6	I	3.3 V	USB	USB1_OTG_OC	7	8	USB2_OTG_PWR	USB	3.3 V	O	K7
M7	I	3.3 V	USB	USB1_OTG_ID	9	10	USB2_OTG_OC	USB	3.3 V	I	J6
–	P	0 V	Ground	DGND	11	12	USB2_OTG_ID	USB	3.3 V	I	L6
A12	I	3.3 V	USB	USB1_RX_P	13	14	DGND	Ground	0 V	P	–
B12	I	3.3 V	USB	USB1_RX_N	15	16	DGND	Ground	0 V	P	–
D14	I	3.3 V	USB	USB1_VBUS	17	18	USB2_VBUS	USB	3.3 V	I	D9
C14	I	3.3 V	USB	USB1_ID	19	20	USB2_ID	USB	3.3 V	I	C9
–	P	0 V	Ground	DGND	21	22	USB2_RX_P	USB	3.3 V	I	A8
–	P	0 V	Ground	DGND	23	24	USB2_RX_N	USB	3.3 V	I	B8
A13	O	3.3 V	USB	USB1_TX_P	25	26	DGND	Ground	0 V	P	–
B13	O	3.3 V	USB	USB1_TX_N	27	28	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	29	30	USB2_TX_P	USB	3.3 V	O	A9
–	P	0 V	Ground	DGND	31	32	USB2_TX_N	USB	3.3 V	O	B9
A14	I/O	3.3 V	USB	USB1_DP	33	34	DGND	Ground	0 V	P	–
B14	I/O	3.3 V	USB	USB1_DN	35	36	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	37	38	USB2_DP	USB	3.3 V	I/O	A10
–	P	0 V	Ground	DGND	39	40	USB2_DN	USB	3.3 V	I/O	B10
C16	O	1.8 V	DSI	DSI_CLK_N	41	42	DGND	Ground	0 V	P	–
D16	O	1.8 V	DSI	DSI_CLK_P	43	44	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	45	46	DSI_D3_N	DSI	1.8 V	O	A15
–	P	0 V	Ground	DGND	47	48	DSI_D3_P	DSI	1.8 V	O	B15
A16	O	1.8 V	DSI	DSI_D1_N	49	50	DGND	Ground	0 V	P	–
B16	O	1.8 V	DSI	DSI_D1_P	51	52	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	53	54	DSI_D2_N	DSI	1.8 V	O	A18
–	P	0 V	Ground	DGND	55	56	DSI_D2_P	DSI	1.8 V	O	B18
A17	O	1.8 V	DSI	DSI_D0_N	57	58	DGND	Ground	0 V	P	–
B17	O	1.8 V	DSI	DSI_D0_P	59	60	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	61	62	PCIE1_TX_N	PCIE	3.3 V	O	J24
–	P	0 V	Ground	DGND	63	64	PCIE1_TX_P	PCIE	3.3 V	O	J25
E24	O	3.3 V	PCIE	PCIE2_TX_N	65	66	DGND	Ground	0 V	P	–
E25	O	3.3 V	PCIE	PCIE2_TX_P	67	68	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	69	70	PCIE1_RX_N	PCIE	3.3 V	I	H24
–	P	0 V	Ground	DGND	71	72	PCIE1_RX_P	PCIE	3.3 V	I	H25
D24	I	3.3 V	PCIE	PCIE2_RX_N	73	74	DGND	Ground	0 V	P	–
D25	I	3.3 V	PCIE	PCIE2_RX_P	75	76	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	77	78	PCIE1_REF_CLK_N	PCIE	3.3 V	I	K24
–	P	0 V	Ground	DGND	79	80	PCIE1_REF_CLK_P	PCIE	3.3 V	I	K25
F24	I	3.3 V	PCIE	PCIE2_REF_CLK_N	81	82	DGND	Ground	0 V	P	–
F25	I	3.3 V	PCIE	PCIE2_REF_CLK_P	83	84	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	85	86	GPIO1_IO01 [4]	DNC	3.3 V	I/O	T7
P4	I/O	3.3 V	DNC	TEMP_INT# [5]	87	88	GPIO1_IO00 [6]	DNC	3.3 V	I/O	T6
R4	I/O	3.3 V	DNC	WDOG1# [7]	89	90	SD2_VSELECT	uSDHC2	3.3 V	O	P5
N22	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA0	91	92	SD2_WP	uSDHC2	1.8 V / 3.3 V	I	M21
N21	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA1	93	94	SD2_CD#	uSDHC2	1.8 V / 3.3 V	I	L21
P22	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA2	95	96	SD2_RST#	uSDHC2	1.8 V / 3.3 V	O	R22
P21	I/O	1.8 V / 3.3 V	uSDHC2	SD2_DATA3	97	98	SD2_CMD	uSDHC2	1.8 V / 3.3 V	I/O	M22
–	P	0 V	Ground	DGND	99	100	SD2_CLK	uSDHC2	1.8 V / 3.3 V	O	L22

Attention: Destruction or malfunction, DNC / GPIOs [3]		
	GPIO1_IO00:03 GPIO1_IO06:07	It is not recommended to use these six GPIOs as this will lead to limitations on the TQMa8Mx. GPIO1_IO06:07 can however be provided on request.. Please contact TQ-Support for details.

3: GPIOs can be made available as on request. Please contact TQ-Support.
4: GPIO1_IO01, can be used as CLK2_N.
5: TEMP_INT# (GPIO1_IO03), can be used as CLK1_N.
6: GPIO1_IO00, can be used as CLK2_P.
7: WDOG1# (GPIO1_IO02), can be used as CLK1_P.

3.3 System components

3.3.1 i.MX 8M CPU

3.3.1.1 i.MX 8M derivatives

Depending on the TQMa8Mx version, one of the following i.MX 8M derivatives is assembled.
Red fields indicate a difference, green fields indicate 100 % compatibility of the resource.

Table 6: i.MX 8M derivatives

Feature	i.MX 8MQ	i.MX 8MD	i.MX 8MQL
Core Complex 1			
Number of cores	4× A53 ARM®v8-A architecture	2× A53 ARM®v8-A architecture	4× A53 ARM®v8-A architecture
Architecture width	64-bit	64-bit	64-bit
Max. clock (MHz)	1300 (–25 °C to +85 °C) 1500 (0 °C to +85 °C)	1300 (–25 °C to +85 °C) 1500 (0 °C to +85 °C)	1300 (–25 °C to +85 °C) 1500 (0 °C to +85 °C)
Memory			
L1 cache	32 kB I/D	32 kB I/D	32 kB I/D
L2 cache	Shared 1 MB	Shared 1 MB	Shared 1 MB
Memory type	1× LPDDR4, up to 3200 MT/s	1× LPDDR4, up to 3200 MT/s	1× LPDDR4, up to 3200 MT/s
Max. size	4 Gbyte	4 Gbyte	4 Gbyte
Core Complex 2			
Number of cores	1× ARM® Cortex-M4F	1× ARM® Cortex-M4F	1× ARM® Cortex-M4F
Architecture width	64-bit	64-bit	64-bit
Max. clock (MHz)	266	266	266
Memory			
L1 cache	16 kB I/D	16 kB I/D	16 kB I/D
Memory type	SRAM (On-Chip) with ECC	SRAM (On-Chip) with ECC	SRAM (On-Chip) with ECC
Max. size	256 kB TCM	256 kB TCM	256 kB TCM
Graphics			
GPU	GC7000Lite OpenGL/ES 3.1, OpenGL 3.0, Vulkan, OpenCL 1.2	GC7000Lite OpenGL/ES 3.1, OpenGL 3.0, Vulkan, OpenCL 1.2	GC7000Lite OpenGL/ES 3.1, OpenGL 3.0, Vulkan, OpenCL 1.2
VPU	4Kp60 with High Dynamic Range (h.265, VP9), 4Kp30 (h.264), 1080p60 (MPEG2, MPEG4p2, VC-1, VP8, RV9, AVS/AVS+, h.263, DivX), MJPEG - 8×8	4Kp60 with High Dynamic Range (h.265, VP9), 4Kp30 (h.264), 1080p60 (MPEG2, MPEG4p2, VC-1, VP8, RV9, AVS/AVS+, h.263, DivX), MJPEG - 8×8	No VPU

3.3.1.1 i.MX 8M derivatives (continued)

Table 6: i.MX 8M derivatives (continued)

Feature	i.MX 8MQ	i.MX 8MD	i.MX 8MQL
I/O			
Ethernet controllers	1× RGMII	1× RGMII	1× RGMII
PCI Express controllers	1× Gen 2.0 Dual Mode controller; 5 Gbit/s Root complex or end point supported ×1, ×2, ×4, ×8, ×16 link widths 1 ×2 lanes or 2 ×1 lane	1× Gen 2.0 Dual Mode controller; 5 Gbit/s Root complex or end point supported ×1, ×2, ×4, ×8, ×16 link widths 1 ×2 lanes or 2 ×1 lane	1× Gen 2.0 Dual Mode controller; 5 Gbit/s Root complex or end point supported ×1, ×2, ×4, ×8, ×16 link widths 1 ×2 lanes or 2 ×1 lane
HDMI	1× HDMI 2.0a with HDR Up to 4096 × 2160@60Hz	1× HDMI 2.0a with HDR Up to 4096 × 2160@60Hz	1× HDMI 2.0a Up to 4096 × 2160@60Hz
MIPI-DSI	1× MIPI-DSI standard v1.1 Up to 4-lanes 1.5 Gbit/s	1× MIPI-DSI standard v1.1 Up to 4-lanes 1.5 Gbit/s	1× MIPI-DSI standard v1.1 Up to 4-lanes 1.5 Gbit/s
MIPI-CSI	2× MIPI-CSI2 standard Up to 4-lanes 1.5 Gbit/s standard	2× MIPI-CSI2 standard Up to 4-lanes 1.5 Gbit/s standard	2× MIPI-CSI2 standard Up to 4-lanes 1.5 Gbit/s standard
USB	2× USB 3.0 controllers; 5 Gbit/s	2× USB 3.0 controllers; 5 Gbit/s	2× USB 3.0 controllers; 5 Gbit/s
SAI	5× SAI supporting I2S, AC97, TDM and codec/DSP interfaces 1× SAI 16 Tx and 16 Rx channels 1× SAI 8 Tx and 8 Rx channels 3× SAI 2 Tx and 2 Rx channels	5× SAI supporting I2S, AC97, TDM and codec/DSP interfaces 1× SAI 16 Tx and 16 Rx channels 1× SAI 8 Tx and 8 Rx channels 3× SAI 2 Tx and 2 Rx channels	5× SAI supporting I2S, AC97, TDM and codec/DSP interfaces 1× SAI 16 Tx and 16 Rx channels 1× SAI 8 Tx and 8 Rx channels 3× SAI 2 Tx and 2 Rx channels
Other peripherals	2× uSDHC; 2× QSPI; 3× SPI; 4× I^{2}C; 4× UART; 1× S/PDIF	2× uSDHC; 2× QSPI; 3× SPI; 4× I^{2}C; 4× UART; 1× S/PDIF	2× uSDHC; 2× QSPI; 3× SPI; 4× I^{2}C; 4× UART; 1× S/PDIF
Package			
Package	17 mm × 17 mm, 0.65 mm grid, 621 pin FCBGA Unlidded	17 mm × 17 mm, 0.65 mm grid, 621 pin FCBGA Unlidded	17 mm × 17 mm, 0.65 mm grid, 621 pin FCBGA Unlidded

Attention: Destruction or malfunction, i.MX 8M errata	
⚠	Please take note of the current i.MX 8M errata (3).

3.3.1.2 TMU

The i.MX 8M has a Thermal Management Unit to protect the DIE temperature. The temperature values are regularly read out and used by the reference BSP as the current value for thermal management. This allows the i.MX 8M to be protected at high temperatures by thermal throttling and thermal shutdown. The TMU is specified in the temperature range 0 °C to +85 °C ±5 °C.

For operation outside these DIE temperatures, additional project-specific precautions must be taken, for example

- Use a heat spreader with heat sink or, if necessary, a fan.
- In addition to the TMU, the temperature sensor on the TQMa8Mx can also be used.

3.3.1.3 Boot Mode

The Boot Mode configuration of the i.MX 8M is selected via boot strapping pins when the reset is released.
At this time the correct levels must be applied to the corresponding I.MX 8M pins to ensure the desired configuration.
The Boot Mode and, if required, the Boot Device must be selected.
For the series, the internal eFuses can be burned, which then select the boot device.
More information about boot interfaces and its configuration is to be taken from the i.MX 8M Data Sheet (1) and the i.MX 8M Reference Manual (2). Alternatively, an image can be loaded into the internal RAM via serial downloader.
The Boot Mode is selected via BOOT_MODE[1:0] (4-pin DIP switch on the MBa8Mx).
Both the boot device and its configuration, as well as some I.MX 8M settings must be set via several Boot Mode registers.
For this the i.MX 8M offers two possibilities:

- Burning and reading internal eFuses
- Reading-in of different GPIO pins

The exact behaviour depends on the value of the register BT_FUSE_SEL.
The following table shows the behaviour of the value of BT_FUSE_SEL depending on the selected Boot Mode.

Table 7: Boot mode selection

BOOT_MODE[1:0]	Boot source	Boot source	Usage
00 (default)	Boot from eFuses	0 = Boot using Serial Downloader (Default) 1 = Boot Mode Configuration is taken from eFuses	Series
01	Serial Downloader	Boot using Serial Downloader (USB1)	Development/Testing
10	Internal Boot	0 = Boot Mode Configuration is taken from GPIOs (Default) 1 = Boot Mode Configuration is taken from eFuses	Development
11	(Reserved)	(n/a)	(n/a)

Note: Field software updates	
	When designing a carrier board, it is recommended to have a redundant update concept for field software updates.

3.3.1.4 Boot devices

The Boot Device Selection is done either via the Boot Configuration Pins (during development) or via the eFuses (in series).
The boot configuration pins are multiplexed on the SAI1 interface. Alternatively, an image can be loaded into the internal RAM using the Serial Downloader.
The Boot Device can be selected according to the Boot Mode selection in the following table.
With some eFuses, general settings are made independently of the Boot Device.

Table 8: General boot configuration

eFuse [8]	i.MX 8M signal	i.MX 8M ball	TQMa8Mx	Setting	Default	TQMa8Mx
BOOT_CFG[15]	SAI1_TXD7	C1	X2-27	Infinite Loop (for Debug): 0 = Disabled 1 = Enabled	0	0

8: Signals BOOT_CFG[15:0] have internal 95 kΩ Pull-Downs.

3.3.1.4 Boot devices (continued)

Table 9: Boot device eMMC at USDHC1

eFuse [9]	i.MX 8M signal	i.MX 8M ball	TQMa8Mx	Setting	Default	TQMa8Mx
BOOT_CFG[14]	SAI1_TXD6	B3	X2-29	Boot Device: 010 = MMC/eMMC	000	010
BOOT_CFG[13]	SAI1_TXD5	C2	X2-31			
BOOT_CFG[12]	SAI1_TXD4	D2	X2-35			
BOOT_CFG[11]	SAI1_TXD3	D1	X2-37	Port: 00 = eSDHC1 01 = eSDHC2	00	00
BOOT_CFG[10]	SAI1_TXD2	B2	X2-39			
BOOT_CFG[7]	SAI1_RXD7	G1	X2-53	Fast Boot: 0 = Regular 1 = Fast Boot	0	0
BOOT_CFG[6]	SAI1_RXD6	G2	X2-55	Bus Width: 000 = 1 bit 001 = 4 bit 010 = 8 bit 101 = 4-bit DDR (MMC 4.4) 110 = 8-bit DDR (MMC 4.4)	000	000
BOOT_CFG[5]	SAI1_RXD5	F1	X2-57			
BOOT_CFG[4]	SAI1_RXD4	J1	X2-61			
BOOT_CFG[3]	SAI1_RXD3	J2	X2-63	Speed: 00 = Normal Speed 01 = High Speed	00	00
BOOT_CFG[2]	SAI1_RXD2	H2	X2-65			
BOOT_CFG[1]	SAI1_RXD1	L2	X2-67	USDHC1 I/O Voltage: 0 = 3.3 V 1 = 1.8 V	0	1
BOOT_CFG[0]	SAI1_RXD0	K2	X2-69	USDHC2 I/O Voltage: 0 = 3.3 V 1 = 1.8 V	0	0

9: Signals BOOT_CFG[15:0] have an internal 95 kΩ Pull-Down.

3.3.1.4 Boot devices (continued)

Table 10: Boot device SD card at USDHC1

eFuse [10]	i.MX 8M signal	i.MX 8M ball	TQMa8Mx	Setting	Default	TQMa8Mx
BOOT_CFG[14]	SAI1_TXD6	B3	X2-29	Boot Device: 001 = SD / eSD	000	001
BOOT_CFG[13]	SAI1_TXD5	C2	X2-31			
BOOT_CFG[12]	SAI1_TXD4	D2	X2-35			
BOOT_CFG[11]	SAI1_TXD3	D1	X2-37	Port: 00 = eSDHC1 01 = eSDHC2	01	01
BOOT_CFG[10]	SAI1_TXD2	B2	X2-39			
BOOT_CFG[7]	SAI1_RXD7	G1	X2-53	SD Power Cycle: 0 = Disabled 1 = Enabled	0	0
BOOT_CFG[6]	SAI1_RXD6	G2	X2-55	SD Loopback Clock Source: 0 = Through SD pad 1 = Direct	0	0
BOOT_CFG[5]	SAI1_RXD5	F1	X2-57	Fast Boot: 0 = Regular 1 = Fast Boot	0	0
BOOT_CFG[4]	SAI1_RXD4	J1	X2-61	Bus Width: 0 = 1 bit 1 = 4 bit	0	1
BOOT_CFG[3]	SAI1_RXD3	J2	X2-63	Speed: 000 = Normal / SDR12 001 = High / SDR25 010 = SDR50 011 = SDR104 101 = Reserved for DDR50	000	001
BOOT_CFG[2]	SAI1_RXD2	H2	X2-65			
BOOT_CFG[1]	SAI1_RXD1	L2	X2-67			

10: Signals BOOT_CFG[15:0] have an internal 95 kΩ Pull-Down.

3.3.2 Memory

3.3.3 LPDDR4 SDRAM

The LPDDR4 is connected via two 16-bit wide data buses and 6-bit wide command/address lines.
The memory is designed for a maximum speed of 3200 MT/s (= 1600 MHz DDR clock).
A maximum of 4 Gbyte LPDDR4 SDRAM is supported.

3.3.4 eMMC

The I.MX 8M provides two uSDHC controllers. The eMMC is connected with 8 bit to uSDHC1 and supports MMC standard v5.0.
A maximum of 64 Gbyte eMMC is supported. The uSDHC1 interface is not routed to the TQMa8Mx connectors.
The following eMMC modes are supported at the i.MX 8M port USDHC1:

Table 11: USDHC1 eMMC modes

eMMC mode	1 bit	4 bit	8 bit	Fast Boot	Remark
Normal Speed	Yes	Yes	Yes	No [11]	Not tested
High Speed	Yes	Yes	Yes	No [11]	–
HS200	(n/a) [12]	Yes	Yes	No [11]	–
HS400	(n/a) [12]	(n/a) [12]	Yes	No [11]	Default in TQ-BSP

3.3.5 QSPI NOR flash

Up to two QSPI storage devices, QSPI_A and QSPI_B, are supported on the TQMa8Mx.
More detailed information can be found in the app note TN-28-05.

- All QSPI signal lines are available at the TQMa8Mx connector
- Variants of TQMa8Mx:
  - No NOR assembled on TQMa8Mx: QSPI_A and QSPI_B available at TQMa8Mx connectors
  - Single-Die NOR assembled on TQMa8Mx: QSPI_B available at TQMa8Mx connectors

Attention: Malfunction or destruction, QSPI interface	
	The QSPI interface may only be used as memory interface. Other SPI devices have to be connected at the eCSPI interfaces.

3.3.6 EEPROM

A 64 kbit serial EEPROM, controlled by the I2C1 bus, is assembled. Write-Protect (WP#) is not supported.
To store data “read-only”, the EEPROM with temperature sensor must be used, see 3.3.7.
The following table shows details of the EEPROM:

Table 12: EEPROM

Manufacturer	Device	Size	Temperature range
Microchip	24LC64T-I/MC MCH	64 Kbit	–45 °C to +85 °C

➢ The EEPROM has I²C address `0x57 / 101 0111b`

11: Not supported by software.
12: Not specified by JEDEC.

3.3.7 EEPROM with temperature sensor

A serial EEPROM including temperature sensor, controlled by the I2C1 bus, is assembled on the TQMa8Mx.
The lower 128 bytes (addresses 00h to 7Fh) can be set to Permanent Write Protected (PWP) mode or Reversible Write Protected (RWP) mode by software. The upper 128 bytes (addresses 80h to FFh) cannot be write-protected and can be used for general data storage. The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa8Mx.
The following table shows details of the Manufacturer EEPROM:

Table 13: Manufacturer EEPROM

Manufacturer	Device	Size	Temperature range
NXP	SE97BTP	2 × 128 bytes	–45 °C to +125 °C

- The device has the following I²C addresses:
  - EEPROM (Normal Mode): `0x53 / 101 0011b`
  - EEPROM (Protected Mode): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

The following figure shows the interface of the temperature sensor to the i.MX 8M.

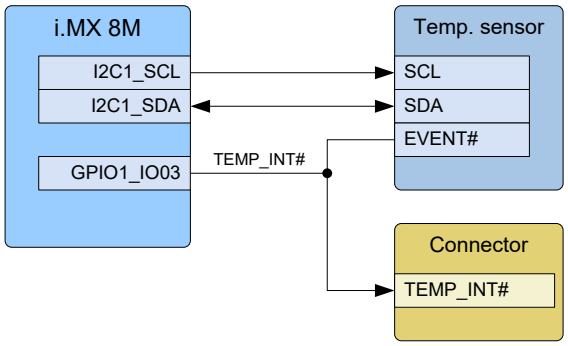


Figure 3: Block diagram temperature sensor interface

The EEPROM with temperature sensor (D3) is assembled on the bottom side of the TQMa8Mx, see Figure 9.
Signal TEMP_INT# is connected to GPIO1_IO03 of the I.MX 8M and also routed to connector X3-87. Signal TEMP_INT# provides an interrupt warning for a programmed switching threshold. The threshold is configured by the I.MX 8M.
During Reset signal TEMP_INT# is pulled to DGND via the i.MX 8M-internal 90 kΩ Pull-Down.
The following table shows details of the temperature sensor:

Table 14: Temperature sensor SE97BTP

Manufacturer	Device	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±1 °C Max. ±2 °C Max. ±3 °C	+75 °C to +95 °C +40 °C to +125 °C –40 °C to +125 °C

3.3.8 RTC

The TQMa8Mx provides a discrete RTC PCF85063A. The accuracy of the RTC is essentially determined by the characteristics of the quartz used. The RTC on the TQMa8Mx is clocked by a 32.768 kHz crystal with a tolerance of ±20 ppm (+25 °C). This equals to a deviation of 1.7 s/day or ±30 ppm (+85 °C) = 2.6 s/day. The RTC is connected to the I2C1 bus.
Interrupt Signal RTC_INT# is connected to GPIO1_IO01 of the I.MX 8M.
Supply via V_LICELL possible for buffered RTC (GoldCap or battery required).

- The RTC has I²C address `0x51 / 101 0001b`

3.3.9 I²C devices

I2C1 is used for the I²C devices on the TQMa8Mx. The I2C1 bus has 4.7 kΩ Pull-Ups on the TQMa8Mx.
The following I²C devices are connected to the I2C1 bus on the TQMa8Mx:

Table 15: TQMa8Mx I²C addresses

Device	Function	Hex / 7-bit address	Remark
MCPF4210	PMIC	0x08 / 000 1000b	Should not be altered
M24LC64	EEPROM	0x57 / 101 0111b	For general usage
SE97BTP	Temperature sensor	0x1B / 001 1011b	Access to temperature registers
	EEPROM	0x53 / 101 0011b	R/W access in Normal Mode
	EEPROM	0x33 / 011 0011b	R/W access in Protected Mode
PCF85063A	RTC	0x51 / 101 0001b	Assembly option

If more I²C devices are connected to the I2C1 bus on the carrier board, the maximum capacitive bus load according to the I²C standard must be observed. If necessary, additional Pull-Ups have to be provided on the carrier board.

3.3.10 Reset

A reset can be performed from an external source via SYS_RST#, which is routed to TQMa8Mx connector X2-14.
Signal GPIO1_IO02 (WDOG#) can also be used as reset. A green LED signals the RESET# condition (POR#).
After an external reset is carried out on the TQMa8Mx, the power sequencing starts.
After the power sequencing has been completed, the i.MX 8M starts.

The following block diagram shows the Reset signal wiring:

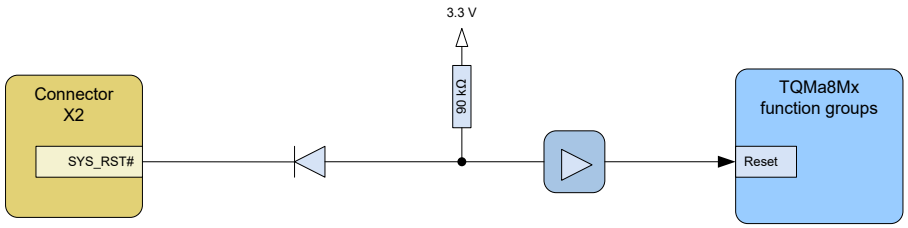


Figure 4: Block diagram Reset

The following table shows the Reset signals:

Table 16: Reset signals

Signal	TQMa8Mx	Dir.	Power domain	Remark
SYS_RST#	X2-14	I	3.3 V	Supervisor Reset input • To activate: Pull to DGND • To deactivate: Pull to 3.3 V
VCC3V3	X2-1	O	3.3 V	Indicates, that TQMa8Mx boot-up is completed. Serves as reset signal for carrier board components.
NVCC_1V8	X2-6	O	1.8 V	

3.4 TQMa8Mx interfaces

The TQMa8Mx has interfaces with primary functions. These can be used simultaneously regardless of their configuration.
If a secondary function is used, some primary functions are omitted. The three interfaces listed in the following table are not routed to the TQMa8Mx connectors and are exclusively used on the TQMa8Mx:

Table 17: TQMa8Mx internal interfaces

Interface	Chapter	Remark
SDRAM	3.3.3	LPDDR4, 32 bit
USDHC1	3.3.4	eMMC, 8 bit
QSPIA & QSPIB	3.3.5	Availability depends on placement options

3.4.1 ECSPI

The i.MX 8M provides three ECSPI interfaces. ECSPI1 and ECSPI2 are available as primary interfaces at the TQMa8Mx connectors. The following table shows the signals used by the ECSPI interfaces:

Table 18: ECSPI signals

Signal name	TQMa8Mx	Dir.	Power domain
ECSPI1_SCLK	X2-30	O	NVCC_ECSPI (1.8V / 3.3 V)
ECSPI1_MOSI	X2-34	O	
ECSPI1_MISO	X2-32	I	
ECSPI1_SS0	X2-36	O	
ECSPI2_SCLK	X2-40	O	
ECSPI2_MOSI	X2-44	O	
ECSPI2_MISO	X2-42	I	
ECSPI2_SS0	X2-46	O	

3.4.2 ENET

The i.MX 8M provides a 10/100/1000 MAC core that supports MII, RMII and RGMII. The RGMII signals are available as primary function on the TQMa8Mx connectors. The following table shows the signals used by the ENET interface:

Table 19: ENET1 signals

Signal name	TQMa8Mx	Dir.	Power domain
ENET_MDC	X1-100	O	NVCC_1V8
ENET_MDIO	X1-100	I/O	
ENET_TXC	X1-104	O	
ENET_TD3	X1-118	O	
ENET_TD2	X1-116	O	
ENET_TD1	X1-114	O	
ENET_TD0	X1-112	O	
ENET_TX_CTL	X1-110	O	
ENET_RXC	X1-105	I	
ENET_RD3	X1-117	I	
ENET_RD2	X1-115	I	
ENET_RD1	X1-113	I	
ENET_RD0	X1-111	I	
ENET_RX_CTL	X1-109	I	

3.4.3 GPIO

Most i.MX 8M pins can be multiplexed as GPIO. All these GPIOs can trigger an interrupt. Details can be found in the NXP Reference Manual (2). Several pins are pre-configured as GPIO on the TQMa8Mx connectors. The following table shows the available GPIOs:

Table 20: GPIO signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
GPIO1_IO00 [13]	X3-88	O	VCC3V3	TQMa8Mx internal signal Alternative: CLK2_P
GPIO1_IO01 [13]	X3-86	O		TQMa8Mx internal signal Alternative: CLK2_N
GPIO1_IO02 [13]	X3-89	O		Default: WDOG1# Alternative: CLK1_P
GPIO1_IO03 [13]	X3-87	O		Default: TEMP_INT# Alternative: CLK1_N
GPIO1_IO05	X3-1	I/O		–
GPIO1_IO06 [13, 14]	X3-3	O		TQMa8Mx internal signal Alternative: GPIO
GPIO1_IO07 [13, 14]	X3-2	O		TQMa8Mx internal signal Alternative: GPIO
GPIO1_IO08	X3-4	I/O		–
GPIO1_IO09	X3-6	I/O		–
GPIO3_IO16	X2-17	I/O	NVCC_1V8	–
GPIO3_IO17	X2-20	I/O		–
GPIO3_IO18	X2-22	I/O		–

3.4.4 HDMI

The i.MX 8M provides an HDMI interface that is routed to the TQMa8Mx connectors.
The following table shows the signals used by the HDMI interface:

Table 21: HDMI signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
HDMI_AUXP	X2-108	I	VDD_PHY_1V8	–
HDMI_AUXN	X2-110	I		–
HDMI_CEC	X2-89	I/O		–
HDMI_HPD	X2-87	I		–
HDMI_DDC_SCL	X2-111	O		22 Ω serial termination on TQMa8Mx
HDMI_DDC_SDA	X2-113	I/O		22 Ω serial termination on TQMa8Mx
HDMI_TX3_P	X2-103	O		–
HDMI_TX3_N	X2-105	O		–
HDMI_TX2_P	X2-100	O		–
HDMI_TX2_N	X2-102	O		–
HDMI_TX1_P	X2-95	O		–
HDMI_TX1_N	X2-97	O		–
HDMI_TX0_P	X2-92	O		–
HDMI_TX0_N	X2-94	O		–

3.4.5 I²C busses

The i.MX 8M provides four I²C busses, which are all available at the TQMa8Mx connectors as primary functions. Details about the I²C devices connected to I2C1 bus on the TQMa8Mx can be found in chapter 3.3.9. The following table shows the signals used by the I²C busses:

Table 22: I²C signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
I2C1_SCL	X2-21	O	VCC3V3	4.7 kΩ Pull-Up to 3.3 V on TQMa8Mx
I2C1_SDA	X2-19	I/O		4.7 kΩ Pull-Up to 3.3 V on TQMa8Mx
I2C2_SCL	X2-24	O		–
I2C2_SDA	X2-26	I/O		–
I2C3_SCL	X1-25	O		–
I2C3_SDA	X1-23	I/O		–
I2C4_SCL	X1-24	O		–
I2C4_SDA	X1-22	I/O		–

13: Do not connect. Please contact TQ-Support.
14: Can be made available on request. Please contact TQ-Support.

3.4.6 MIPI CSI

The i.MX 8M provides two MIPI Camera Serial Interfaces (CSI), which are routed to the TQMa8Mx connectors.
The following table shows the signals used by the MIPI-CSI interface:

Table 23: MIPI CSI signals

Signal name	TQMa8Mx	Power domain
CSI1_CLK_P	X1-43	VDD_PHY_1V8
CSI1_CLK_N	X1-41	
CSI1_D3_P	X1-51	
CSI1_D3_N	X1-49	
CSI1_D2_P	X1-59	
CSI1_D2_N	X1-57	
CSI1_D1_P	X1-67	
CSI1_D1_N	X1-65	
CSI1_D0_P	X1-75	
CSI1_D0_N	X1-73	
CSI2_CLK_P	X1-40	
CSI2_CLK_N	X1-38	
CSI2_D3_P	X1-48	
CSI2_D3_N	X1-46	
CSI2_D2_P	X1-56	
CSI2_D2_N	X1-54	
CSI2_D1_P	X1-64	
CSI2_D1_N	X1-62	
CSI2_D0_P	X1-72	
CSI2_D0_N	X1-70	

3.4.7 MIPI DSI

The i.MX 8M provides a MIPI_DSI interface, which is routed to the TQMa8Mx connectors.
The following table shows the signals used by the MIPI-DSI interface:

Table 24: MIPI DSI signals

Signal name	TQMa8Mx	Power domain
DSI_CLK_P	X3-43	VDD_PHY_1V8
DSI_CLK_N	X3-41	
DSI_D3_P	X3-48	
DSI_D3_N	X3-46	
DSI_D2_P	X3-56	
DSI_D2_N	X3-54	
DSI_D1_P	X3-51	
DSI_D1_N	X3-49	
DSI_D0_P	X3-59	
DSI_D0_N	X3-57	

3.4.8 PCIe

The i.MX 8M offers two Gen-2 PCIe interfaces, which are routed to the TQMa8Mx connectors.
The following table shows the signals used by the PCIe interface:

Table 25: PCIe signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
PCIE1_REF_CLK_P	X3-80	I	VDD_PHY_3V3	–
PCIE1_REF_CLK_N	X3-78	I		–
PCIE1_TX_P	X3-64	O		100 nF in series
PCIE1_TX_N	X3-62	O		100 nF in series
PCIE1_RX_P	X3-72	I		–
PCIE1_RX_N	X3-70	I		–
PCIE2_REF_CLK_P	X3-83	I		–
PCIE2_REF_CLK_N	X3-81	I		–
PCIE2_TX_P	X3-67	O		100 nF in series
PCIE2_TX_N	X3-65	O		100 nF in series
PCIE2_RX_P	X3-75	I		–
PCIE2_RX_N	X3-73	I		–

3.4.9 QSPI

The i.MX 8M provides two Quad-SPI interfaces, which are used for the optional NOR flash on the TQMa8Mx.
To provide memory on the carrier board, the interfaces are available at the TQMa8Mx connectors.
The following table shows the signals used by the QSPI interfaces:

Table 26: QSPI signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
QSPI_A_SCLK	X1-97	O	NVCC_1V8	22 Ω serial termination on TQMa8Mx
QSPI_A_DQS	X1-79	I/O		–
QSPI_A_SS1#	X1-81	O		–
QSPI_A_SS0#	X1-83	O		–
QSPI_A_DATA3	X1-87	I/O		–
QSPI_A_DATA2	X1-89	I/O		–
QSPI_A_DATA1	X1-91	I/O		–
QSPI_A_DATA0	X1-93	I/O		–
QSPI_B_SCLK	X1-96	O		22 Ω serial termination on TQMa8Mx
QSPI_B_DQS	X1-78	I/O		–
QSPI_B_SS1#	X1-80	O		–
QSPI_B_SS0#	X1-82	O		–
QSPI_B_DATA3	X1-86	I/O		–
QSPI_B_DATA2	X1-88	I/O		–
QSPI_B_DATA1	X1-90	I/O		–
QSPI_B_DATA0	X1-92	I/O		–

Attention: Malfunction or destruction, QSPI NOR flash	
	For TQMa8Mx variants with populated QSPI NOR flash, the QSPI interface should not be connected on the carrier board in order to prevent malfunctions caused by reflections at high transmission rates. The QSPI interface may only be used as a memory interface. Other SPI devices must be connected to the eCSPI interfaces.

3.4.10 SAI

Of the five SAI interfaces, SAI1, SAI2, SAI3 and SAI5 are available at the TQMa8Mx connectors to connect audio codecs via e.g. I²S. The following table shows the signals used by the SAI interface:

Table 27: SAI signals

Signal name	TQMa8Mx	Dir. [15]	Power domain
SAI1_MCLK	X2-25	O	VCC3V3
SAI1_RXC	X2-75	I	
SAI1_TXC	X2-51	O	
SAI1_RXFS	X2-71	I	
SAI1_TXFS	X2-47	O	
SAI1_RXD7	X2-53	I	
SAI1_RXD6	X2-55	I	
SAI1_RXD5	X2-57	I	
SAI1_RXD4	X2-61	I	
SAI1_RXD3	X2-63	I	
SAI1_RXD2	X2-65	I	
SAI1_RXD1	X2-67	I	
SAI1_RXD0	X2-69	I	
SAI1_TXD7	X2-27	O	
SAI1_TXD6	X2-29	O	
SAI1_TXD5	X2-31	O	
SAI1_TXD4	X2-35	O	
SAI1_TXD3	X2-37	O	
SAI1_TXD2	X2-39	O	
SAI1_TXD1	X2-41	O	
SAI1_TXD0	X2-45	O	
SAI2_MCLK	X2-66	O	
SAI2_RXC	X2-74	I	
SAI2_TXC	X2-80	O	
SAI2_RXFS	X2-70	I	
SAI2_TXFS	X2-78	O	
SAI2_RXD0	X2-68	I	
SAI2_TXD0	X2-76	O	
SAI3_MCLK	X2-50	O	
SAI3_RXC	X2-56	I	
SAI3_TXC	X2-62	O	
SAI3_RXFS	X2-54	I	
SAI3_TXFS	X2-60	O	
SAI3_RXD	X2-52	I	
SAI3_TXD	X2-58	O	
SAI5_MCLK	X2-88	O	
SAI5_RXC	X2-84	I	
SAI5_RXFS	X2-86	I	
SAI5_RXD3	X2-83	I	
SAI5_RXD2	X2-81	I	
SAI5_RXD1	X2-79	I	
SAI5_RXD0	X2-77	I	

15: Depending on the codec mode configured, the information given here may differ.

3.4.11 SJC/JTAG

The i.MX 8M supports two JTAG modes. Pin JTAG_MOD defines the mode.
The following table shows the available modes as well as the mode set on the TQMa8Mx:

Table 28: JTAG modes

JTAG_MOD	Name	Remark
0 (default)	Daisy Chain All	For Software debugging
1	SJC only	IEEE 1149.1 (JTAG) interface

The following table shows the signals used for the JTAG interface:

Table 29: SJC/JTAG signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
JTAG_TCK	X2-117	I	NVCC_JTAG (3.3 V)	i.MX 8M-internal 27 kΩ Pull-Up
JTAG_TMS	X2-115	I		i.MX 8M-internal 27 kΩ Pull-Up
JTAG_TDI	X2-114	I		i.MX 8M-internal 27 kΩ Pull-Up
JTAG_TDO	X2-116	O		i.MX 8M-internal 27 kΩ Pull-Up
JTAG_TRST#	X2-118	I		i.MX 8M-internal 27 kΩ Pull-Up
JTAG_MOD	X2-120	I		i.MX 8M-internal 90 kΩ Pull-Down 10 kΩ Pull-Down on TQMa8Mx

3.4.12 S/PDIF

The i.MX 8M provides two S/PDIF interfaces. SPDIF1 is routed to the TQMa8Mx connectors.
The following table shows the signals used by the S/PDIF interface:

Table 30: S/PDIF signals

Signal name	TQMa8Mx	Dir.	Power domain
SPDIF_TX	X2-7	O	VCC3V3
SPDIF_RX	X2-9	I	
SPDIF_EXT_CLK	X2-11	I	

3.4.13 UART

The i.MX 8M provides four UART interfaces, which are all available as primary function on the TQMa8Mx connectors. Handshake signals are not available.
The following table shows the UART interface signals used:

Table 31: UART signals

Signal name	TQMa8Mx	Dir.	Power domain
UART1_RX	X1-31	I	NVCC_UART (1.8V / 3.3V)
UART1_TX	X1-29	O	
UART2_RX	X1-30	I	
UART2_TX	X1-28	O	
UART3_RX	X1-35	I	
UART3_TX	X1-33	O	
UART4_RX	X1-34	I	
UART4_TX	X1-32	O	

3.4.14 USB

The i.MX 8M provides two USB 3.0 / 2.0 controllers with integrated PHY. Both controllers are OTG interfaces and are routed to the TQMa8Mx connectors.
The following table shows the signals used by the USB1 interface:

Table 32: USB1 signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
USB1_DP	X3-33	I/O	VDD_PHY_3V3	–
USB1_DN	X3-35	I/O		–
USB1_ID	X3-19	I		–
USB1_TX_P	X3-25	O		100 nF in series
USB1_TX_N	X3-27	O		100 nF in series
USB1_RX_P	X3-13	I		–
USB1_RX_N	X3-15	I		–
USB1_VBUS	X3-17	I	–	Supply with 5 V on carrier board
USB1_OTG_ID	X3-9	I	VCC3V3	GPIO1_IO10
USB1_OTG_OC	X3-7	I		GPIO1_IO13
USB1_OTG_PWR	X3-5	O		GPIO1_IO12

The following table shows the signals used by the USB2 interface:

Table 33: USB2 signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
USB2_DP	X3-38	I/O	VDD_PHY_3V3	–
USB2_DN	X3-40	I/O		–
USB2_ID	X3-20	I		–
USB2_TX_P	X3-30	O		100 nF in series
USB2_TX_N	X3-32	O		100 nF in series
USB2_RX_P	X3-22	I		–
USB2_RX_N	X3-24	I		–
USB2_VBUS	X3-18	I	–	Supply with 5 V on carrier board
USB2_OTG_ID	X3-12	I	VCC3V3	GPIO1_IO11
USB2_OTG_OC	X3-10	I		GPIO1_IO15
USB2_OTG_PWR	X3-8	O		GPIO1_IO14

3.4.15 USDHC

The USDHC2 port of the i.MX 8M is routed to the TQMa8Mx connectors. MMC, SD or SDIO cards can be connected.
The following table shows the signals used by the USDHC2 interface:

Table 34: USDHC2 signals

Signal name	TQMa8Mx	Dir.	Power domain	Remark
SD2_DATA3	X3-97	I/O	NVCC_SD2 (1.8 V / 3.3 V)	–
SD2_DATA2	X3-95	I/O		–
SD2_DATA1	X3-93	I/O		–
SD2_DATA0	X3-91	I/O		–
SD2_CLK	X3-100	O		22 Ω serial termination on TQMa8Mx
SD2_CMD	X3-98	I/O		–
SD2_CD#	X3-94	I		–
SD2_WP	X3-92	I		–
SD2_RST#	X3-96	O		–
SD2_VSELECT	X3-90	O	NVCC_GPIO1 (3.3V)	3.3 V

Attention: Malfunction or destruction, SDHC2 supply voltage

The interface supports transfer rates up to UHS-I mode (SDR104) with 208 MHz or 104 MB/s.
To use these, the I/O voltage of the USDHC interface must be changed from 3.3 V to 1.8 V.
The USDHC interface can only be used with a low I/O voltage. During card detection, the signal SDHC2_VSELECT, which is available as an output on the connector, is used for this purpose.
The I/O voltage must be switched by software.
It is not permitted to switch the I/O voltage by applying a voltage to TQMa8Mx pin SDHC2_VSELECT.

Note: Interface reset

In case of a power cycle or reset, it must be ensured that the respective interface (e.g. SD card) is also reset. The signal SDHC2_RESET_B, for example, can be used for this purpose.

3.4.16 WDOG

The i.MX 8M provides three watchdog timers, of which WDOG1# is routed to TQMa8Mx connector X3-89.
The following table shows the signal used by the watchdog timer:

Table 35: WDOG signal

Signal name	**TQMa8Mx** pin	Direction	Power domain	Remark
WDOG1#	X3-89	O	VCC3V3	GPIO1_IO02, see also chapter 3.3.10

3.5 Power

3.5.1 Power supply

The TQMa8Mx only requires a single power supply of 5 V ±5 %.
The TQMa8Mx provides the voltages NVCC_SD2, NVCC_ECSPI, and NVCC_UART, at the TQMa8Mx connectors.
These voltages can be fed back to the TQMa8Mx on the carrier board according to customer requirements.
The voltages generated on the TQMa8Mx may only be used for the TQMa8Mx itself.
A further load by circuitry on a carrier board is not permitted and can lead to errors in supply and monitoring.

Attention: Malfunction or destruction, overvoltage	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. A too high input voltage can lead to malfunctions, premature aging or destruction of the TQMa8Mx. To avoid cross-supply and errors during the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the sequence is indicated by a high level of signals VCC3V3 and NVCC_1V8.

3.5.2 TQMa8Mx Power supply inputs

In addition to VCC5V, the following voltage inputs are available at the TQMa8Mx connectors:

Table 36: TQMa8Mx Power supply inputs

Voltage	TQMa8Mx	V_{in}	Usage
NVCC_ECSPI	X2-3	1.8 V ±5 % 3.3 V ±5 %	i.MX 8M supply for I/O block NVCC_ECSPI. Connect to NVCC_1V8 (X2-6) or VCC3V3 (X2-1) on the carrier board.
NVCC_SD2	X2-8	1.8 V ±5 % 3.3 V ±5 %	i.MX 8M supply for I/O block NVCC_SD2. Connect to NVCC_1V8 (X2-6) or VCC3V3 (X2-1) on the carrier board.
NVCC_UART	X2-10	1.8 V ±5 % 3.3 V ±5 %	i.MX 8M supply for I/O block NVCC_UART. Connect to NVCC_1V8 (X2-6) or VCC3V3 (X2-1) on the carrier board.
V_LICELL	X2-4	(See Data Sheet (7))	Supply or backup voltage for RTC

3.5.3 TQMa8Mx Power supply outputs

In addition to the TQMa8Mx supply input, some internal voltages are available at TQMa8Mx connectors.
The following table shows these voltages and their usage:

Table 37: TQMa8Mx Power supply outputs

Voltage	TQMa8Mx	Source	Usage
VCC3V3	X2-1	VCC3V3	Supply for other TQMa8Mx supply inputs. Supply for BOOT_CFG and BOOT_MODE pins.
NVCC_1V8	X2-6	SW4Lx	Supply for other TQMa8Mx supply inputs.

Attention: Malfunction or destruction, voltage outputs	
	VCC3V3 and NVCC_1V8 are outputs. These TQMa8Mx pins must not be supplied with voltage under any circumstances.

3.5.4 TQMa8Mx power-up sequencing

The power-up sequencing is carried out and monitored independently by the TQMa8Mx.
During power-up the POR# is held low. The power-up sequence is controlled by DC/DC converters, LDOs and the PMIC.
There are timing requirements regarding the power-up of voltages on the carrier board.
Voltages VCC3V3 and NVCC_1V8 serve as indicators to start the supply of other carrier board circuitry.

3.5.5 Power consumption

The power consumption of the TQMa8Mx strongly depends on the application, the mode of operation and the operating system. For this reason the given values have to be seen as approximate values.
The following table shows power supply and power consumption parameters of the TQMa8Mx:

Table 38: TQMa8Mx power consumption @ 5 V

Mode of operation	TQMa8MD	TQMa8MQ	TQMa8MQL	Remark
Theoretical calculated peak	8 W	8 W	8 W	–
U-Boot prompt, idle	2.73 W	2.465 W	2.795 W	–
Linux prompt, idle	2.635 W	2.175 W	2.68 W	–
Linux, 100 % CPU load	3.885 W	3.870 W	4.68 W	8MD: stressapptest -s 60 -M 512 -m 4 -C 4 -i 4 8MQ: stressapptest -s 60 -M 512 -m 4 -C 4 -i 4 8MQL: stressapptest -s 60 -M 1024 -m 4 -C 4 -i 4
Off-Mode	0.29 W	0.155 W	0.3 W	SYS_RST# = LOW

3.5.6 Power modes

The i.MX 8M automatically performs power saving without requiring user involvement. The i.MX 8M in combination with the PMIC supports various standby modes. Further information can be found in Data Sheets (1), (2), and in Application Note (6).

4. MECHANICS

4.1 Connectors

The TQMa8Mx is connected to the carrier board with 340 pins on three connectors.
The following table shows details of the connectors used:

Table 39: TQMa8Mx connectors

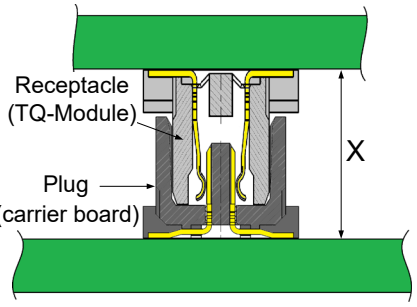
Manufacturer	Pin count part number	Remark
TE connectivity	100-pin: 5177985-4 120-pin: 5177985-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMa8Mx is held in the mating connectors with a retention force of approximately 34 N.
To avoid damaging the connectors of the TQMa8Mx as well as the connectors on the carrier board while removing the TQMa8Mx the use of the extraction tool MOZIa8M is strongly recommended. See chapter 4.9 for further information.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa8Mx for the extraction tool MOZIa8M.

The following table shows some suitable mating connectors for the carrier board:

Table 40: Carrier board mating connectors

Manufacturer	Pin count part number	Remark	Stack height (X)	
TE connectivity	100-pin: 5177986-4 120-pin: 5177986-5	On MBa8Mx	5 mm	
	100-pin: 1-5177986-4 120-pin: 1-5177986-5	–	6 mm	
	100-pin: 2-5177986-4 120-pin: 2-5177986-5	–	7 mm	
	100-pin: 3-5177986-4 120-pin: 3-5177986-5	–	8 mm	

The pins assignment listed in Table 3, Table 4, and Table 5 refer to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in Table 3, Table 4, and Table 5 refer to the i.MX 8M Data Sheet (1).

4.2 Dimensions

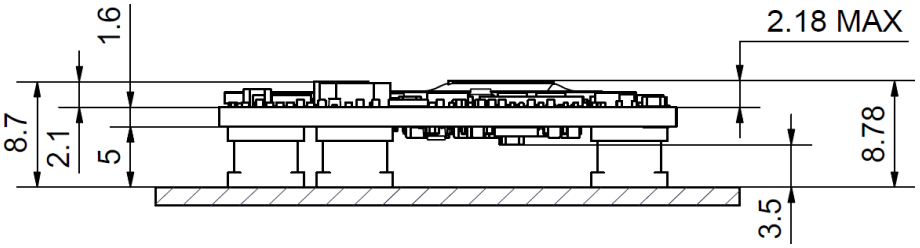


Figure 5: TQMa8Mx dimensions, side view

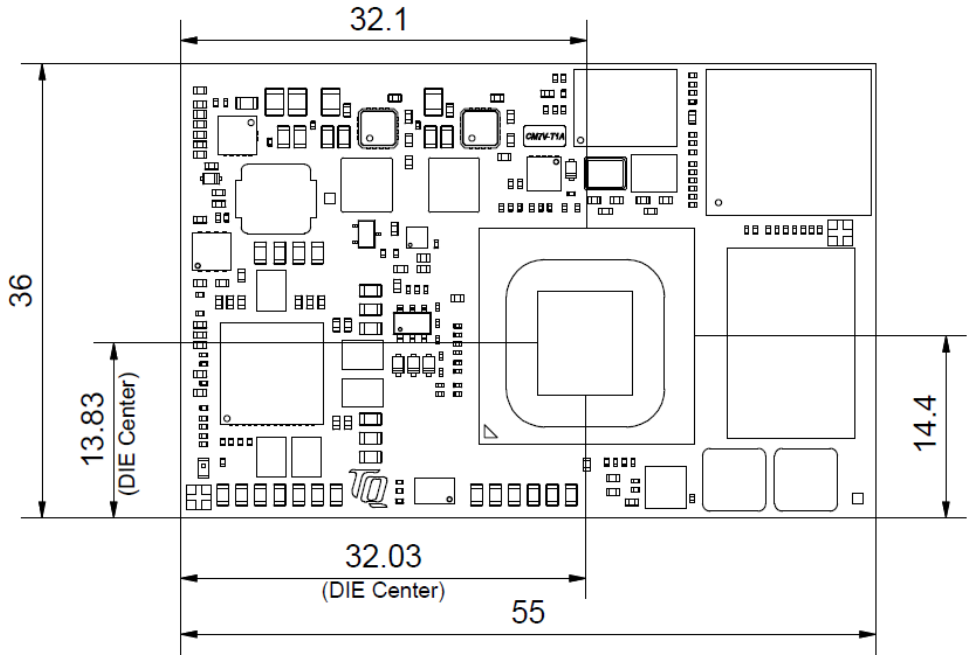


Figure 6: TQMa8Mx CPU position, top view

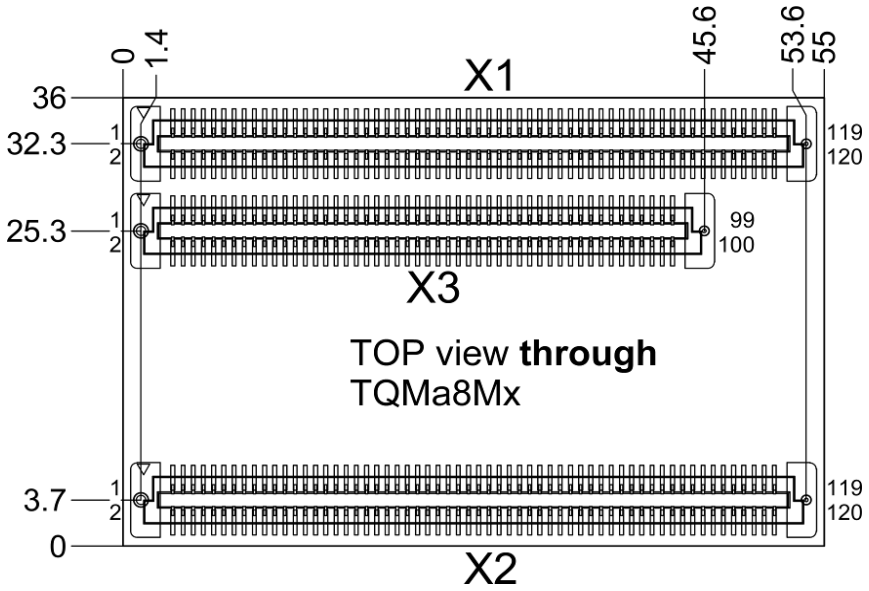


Figure 7: TQMa8Mx dimensions, top view **through** TQMa8Mx

4.3 Component placement

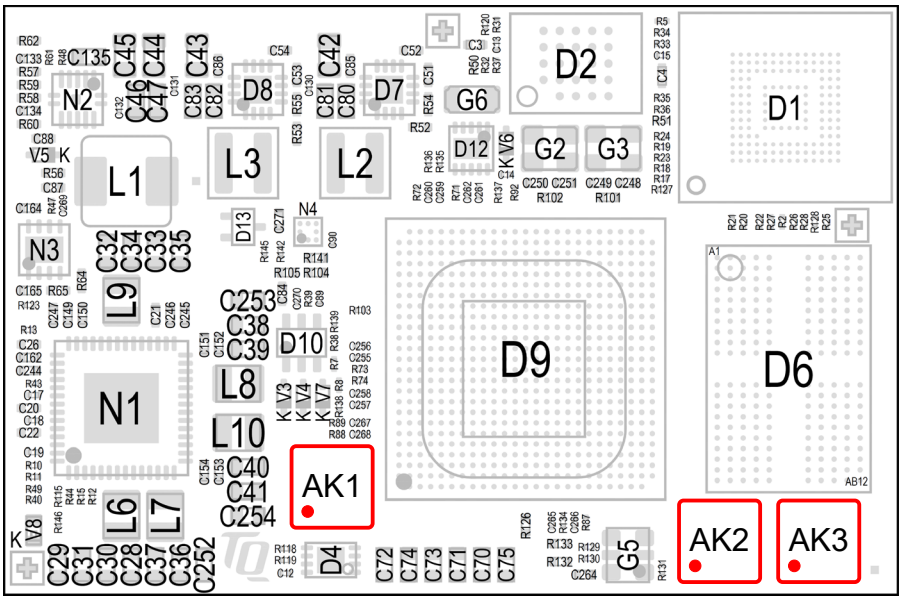


Figure 8: TQMa8Mx, component placement top

The labels on the TQMa8Mx show the following information:

Table 41: Labels on TQMa8Mx

Label	Text
AK1	TQMa8Mx version, revision
AK2	Tests performed
AK3	MAC address (= serial number)

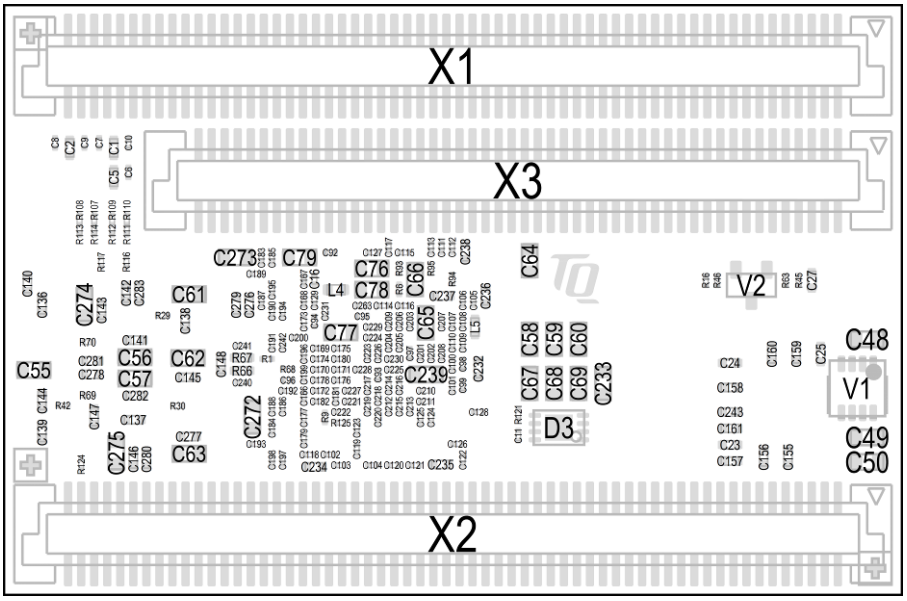


Figure 9: TQMa8Mx, component placement bottom

4.4 3D views

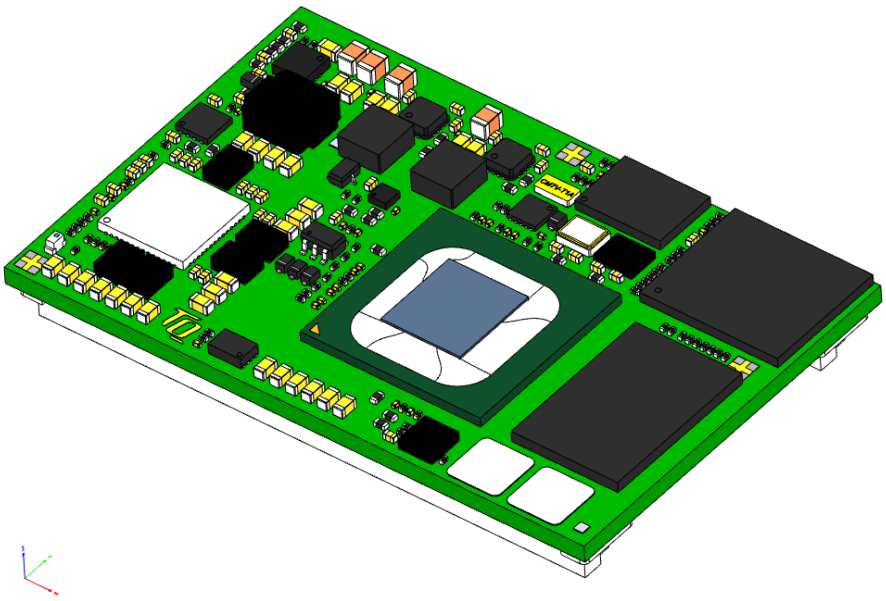


Figure 10: TQMa8Mx, 3D view top

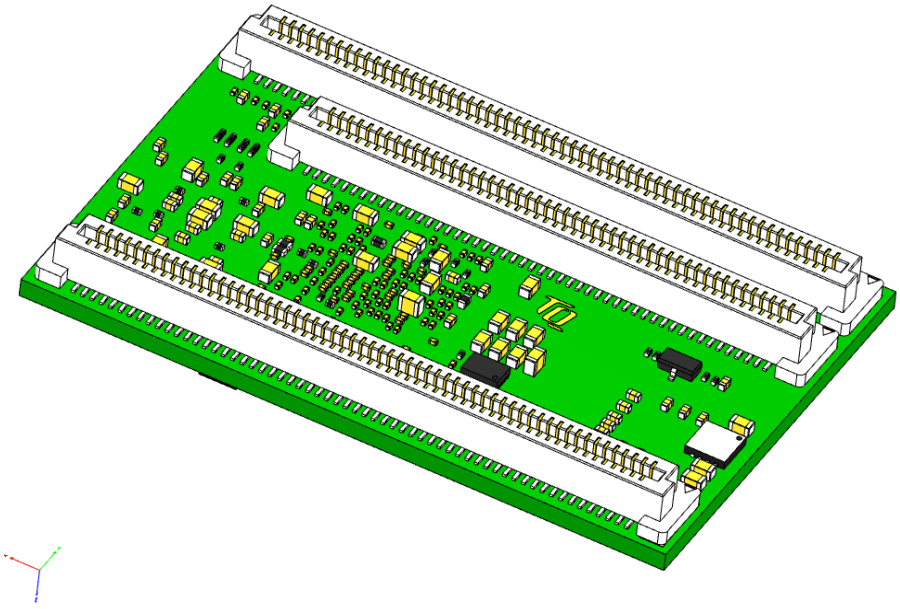


Figure 11: TQMa8Mx, 3D view bottom

3D STEP models are available on request. Please contact TQ-Support.

4.5 Adaptation to the environment

The TQMa8Mx has overall dimensions (length × width × height) of 55 × 36 × 8 mm³.
The TQMa8Mx has a maximum height above the carrier board of approximately 8.78 mm.
The TQMa8Mx weighs approximately 15 grams.

4.6 Protection against external effects

As an embedded module, the TQMa8Mx is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.7 Thermal management

To cool the TQMa8Mx, a calculated theoretical maximum of approximately 8 W has to be dissipated, see Table 38.
The cooling solution must be able to dissipate this peak power; it will never occur permanently in normal operation.
The power dissipation originates primarily in the i.MX 8M, the LPDDR4 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See i.MX 8M Data Sheet (1) for further information.

Attention: Destruction or malfunction, TQMa8Mx heat dissipation	
	The TQMa8Mx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M must be taken into consideration when connecting the heat sink. The i.MX 8M is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Mx and thus malfunction, deterioration or destruction.

4.8 Structural requirements

The TQMa8Mx is held in the mating connectors by the retention force of the pins (340). For high requirements with respect to vibration and shock firmness, an additional retainer has to be provided in the final product to keep the TQMa8Mx in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

4.9 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa8Mx may only be extracted from the carrier board by using the extraction tool MOZIa8M that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa8Mx for the extraction tool MOZIa8M.

5. SOFTWARE

The TQMa8Mx is shipped with a preinstalled boot loader U-Boot and a BSP provided by TQ-Systems, which is tailored for the MBa8Mx. The boot loader U-Boot provides TQMa8Mx-specific as well as board-specific settings, e.g.:

- i.MX 8M configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.
More information can be found in the Support Wiki for the TQMa8Mx.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa8Mx was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Stable ground conditions (sufficient ground planes) on the carrier board.
- A sufficient number of block capacitors at all supply voltages
- Keep fast or constantly clocked lines short; avoid interference with other signals by means of distance and/or shielding; pay attention not only to the frequency but also to the signal rise times.
- Filtering of all signals which are connected externally (also "slow" and DC voltage signals can emit HF indirectly).
- For critical applications, an EMC shielding hood should be used.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the TQMa8Mx.

The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Shock and vibration

Table 42: Shock resistance

Parameter	Details
Shocks	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 ms
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 43: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 – 9 Hz, 9 – 200 Hz, 200 – 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Amplitude	2 Hz … 9 Hz: 3.5 ms^{-2} 9 Hz … 200 Hz: 10 ms^{-2} 200 Hz … 500 Hz: 15 ms^{-2}

6.5 Climate and operational conditions

The operating temperature range for the TQMa8Mx strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.
In general, reliable operation is ensured if the following conditions are met:

Table 44: Climate and operational conditions –25 °C to +85 °C

Parameter	Range	Remark
Ambient temperature	–25 °C to +85 °C	–
T_j i.MX 8M	–40 °C to +105 °C	Junction temperature
T_j PMIC	–40 °C to +125 °C	Junction temperature
Case temperature LPDDR4	–40 °C to +95 °C	–
Case temperature other ICs	–25 °C to +85 °C	–
Storage temperature TQMa8Mx	–25 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 45: Climate and operational conditions –40 °C to +85 °C

Parameter	Range	Remark
Ambient temperature	–40 °C to +85 °C	–
T_j i.MX 8M	–40 °C to +105 °C	Junction temperature
T_j PMIC	–40 °C to +125 °C	Junction temperature
Case temperature LPDDR4	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Storage temperature TQMa8Mx	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

For consumer applications, a version specified for a temperature range of 0 °C to +95 °C can be provided on request.
Detailed information concerning the thermal characteristics of the i.MX 8M is to be taken from the NXP documents (1), and (2).

Attention: Destruction or malfunction, TQMa8Mx heat dissipation	
	The TQMa8Mx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M must be taken into consideration when connecting the heat sink. The i.MX 8M is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Mx and thus malfunction, deterioration or destruction.

6.6 Reliability and service life

The theoretical MTBF at a constant error rate for the TQMa8MQL is approximately 944,787 h @ +40 °C ambient temperature.
The theoretical MTBF at a constant error rate for the TQMa8MQ is approximately 929,450 h @ +40 °C ambient temperature.
The TQMa8Mx is designed to be insensitive to shock and vibration.
High quality industrial grade connectors are assembled on the TQMa8Mx.

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa8Mx is manufactured RoHS compliant. All components and assemblies are RoHS compliant. The soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa8Mx was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa8Mx must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa8Mx enable compliance with EuP requirements for the TQMa8Mx.

7.5 Battery

No batteries are assembled on the TQMa8Mx.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa8Mx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa8Mx is delivered in reusable packaging.

7.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 46: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
AVS	Audio Video coding Standard
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR	Double Data Rate
DIN	Deutsche Industrienorm
DIP	Dual In-line Package
DivX	Digital Video Express
DNC	Do Not Connect
DSI	Display Serial Interface
DSP	Digital Signal Processor
ECC	Error Checking and Correction
eCSPI	enhanced Capability Serial Peripheral Interface
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card
EN	European Norm
ENET	Ethernet
ESD	Electro-Static Discharge
eSD	embedded Secure Digital
eSDHC	embedded Secure Digital High Capacity
EuP	Energy using Products
FCBGA	Flip-Chip Ball Grid Array
FR-4	Flame Retardant 4
GbE	Gigabit Ethernet
GPIO	General Purpose Input/Output
GPU	Graphics Processor Unit
HDMI	High Definition Multimedia Interface
HDR	High Data Rate
I	Input
I/D	Instruction / Data
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IC	Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JEDEC	Joint Electronic Device Engineering Council
JPEG	Joint Photographic Experts Group
JTAG®	Joint Test Action Group
LDO	Low Drop-Out regulator
LED	Light Emitting Diode
LPDDR4	Low Power DDR4 SDRAM
LVDS	Low Voltage Differential Signal
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MII	Media Independent Interface
MIPI	Mobile Industry Processor Interface
MJPEG	Motion JPEG
MMC	Multimedia Card

8.1 Acronyms and definitions (continued)

Table 46: Acronyms (continued)

Acronym	Meaning
MOZI	Module extractor (Modulzieher)
MPEG	Moving Picture Experts Group
MT/s	Mega transfers per second
MTBF	Mean operating Time Between Failures
n/a	not available
NAND	Not-And
NOR	Not-Or
O	Output
OpenGL/ES	Open Graphics Library for Embedded Systems
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
S/PDIF	Sony-Philips Digital Interface Format
SAI	Serial Audio Interface
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDIO	Secure Digital Input/Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SJC	Secure JTAG Controller
SMP	Serial Management Protocol
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
STEP	Standard for Exchange of Products
SVHC	Substances of Very High Concern
TBD	To Be Determined
TCM	Tightly Coupled Memory
TDM	Time-Division Multiplexing
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UM	User's Manual
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
VC-1	Video Codec Standard
VP8	Video Progressive (compression format) 8
VPU	Video Processing Unit
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 47: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Data Sheet for Industrial Products Document: IMX8MDQLQIEC	Rev. 1.1, 07/2019	NXP
(2)	i.MX 8M Dual / 8M QuadLite / 8M Quad Applications Processors Reference Manual Document: IMX8MDQLQRM	Rev. 1, 04/2019	NXP
(3)	Mask Set Errata for Mask 2N14W Document: IMX8MDQLQ_2N14W	Rev. 0, 10/2018	NXP
(4)	i.MX 8M Quad Power Consumption Measurement Document: AN12118	Rev. 2, 08/2018	NXP
(5)	i.MX 8M Dual / 8M QuadLite / 8M Quad Product Lifetime Usage Document: AN12147	Rev. 0, 02/2018	NXP
(6)	PF4210 – 14-channel Power Management Integrated Circuit (PMIC) for audio/video applications Document: PF4210 Rev 1.0	Rev. 1.0, 02/2018	NXP
(7)	PCF85063A – Tiny Real-Time Clock/calendar with alarm function Document: PCF85063A	Rev. 7, 01/2018	NXP
(8)	MBa8Mx User's Manual	– current –	TQ-Systems
(9)	TQMa8Mx Support-Wiki	– current –	TQ-Systems

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