TQMa65xx
Preliminary User's Manual

TQMa65xx UM 0001
07.02.2021

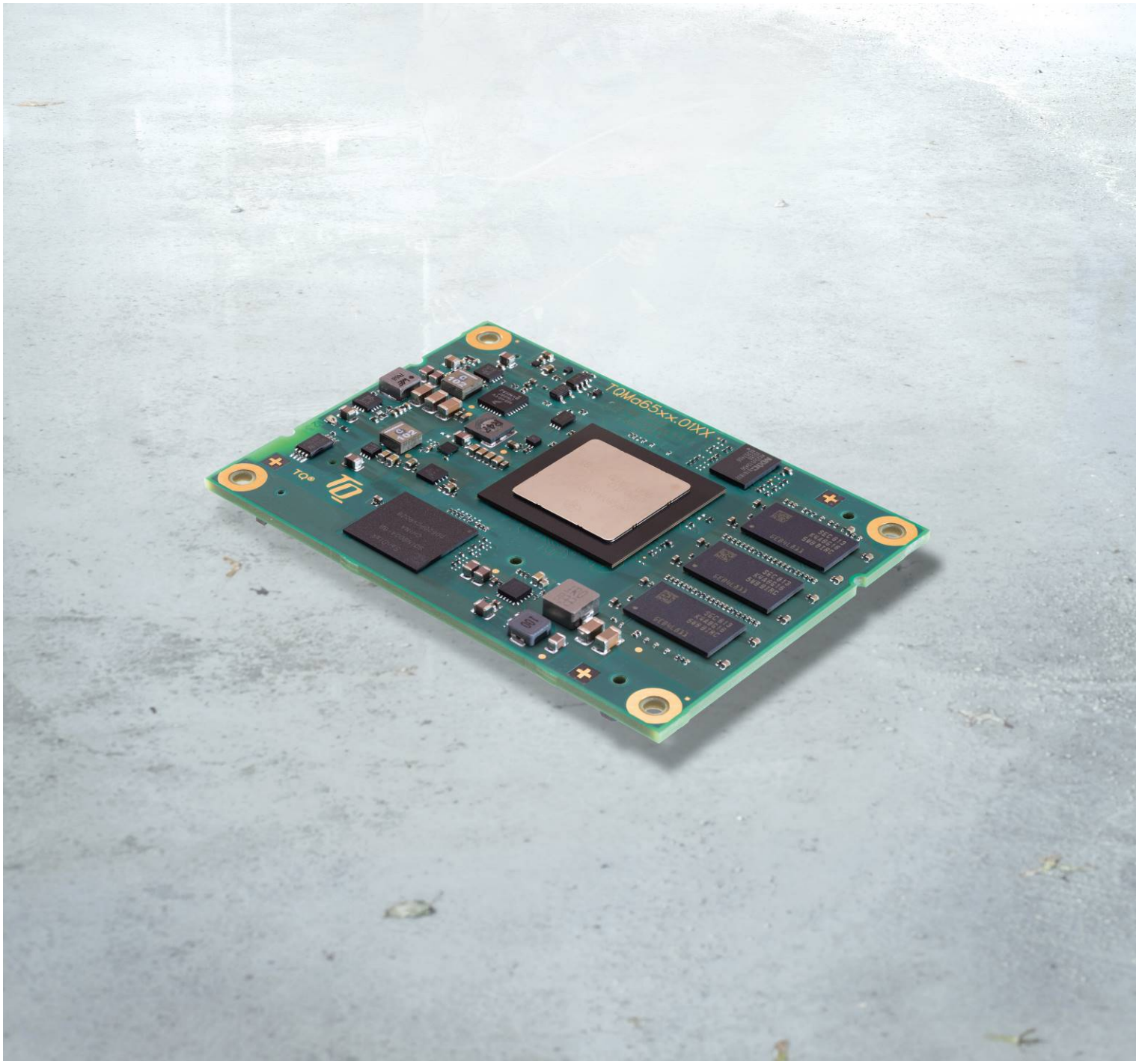

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ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	07.02.2021	Petz		Initial release

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa65xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa65xx circuit diagram
- MBa65xx User's Manual
- AM65xx Data Sheet
- AM65xx Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa65xx

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of the TQMa65xx Rev. 01xx, in combination with the MBa65xx and refers to some software settings. The MBa65xx serves as an evaluation board for the TQMa65xx.

A certain TQMa65xx version does not necessarily provide all features described in this Preliminary User's Manual.

This Preliminary User's Manual does also not replace the TI AM65xx Reference Manual (2).

The CPU derivatives feature ARM® Cortex-A53 cores, and two ARM® Cortex-R5F coprocessors. The CPUs also provide a 3D GPU.

The TQMa65xx is a universal Minimodule based on these TI ARM® Cortex-A53 AM65xx CPUs, see also (1), (2).

An AM65xx Cortex-A53 core typically operates at 1.1 GHz.

The TQMa65xx extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

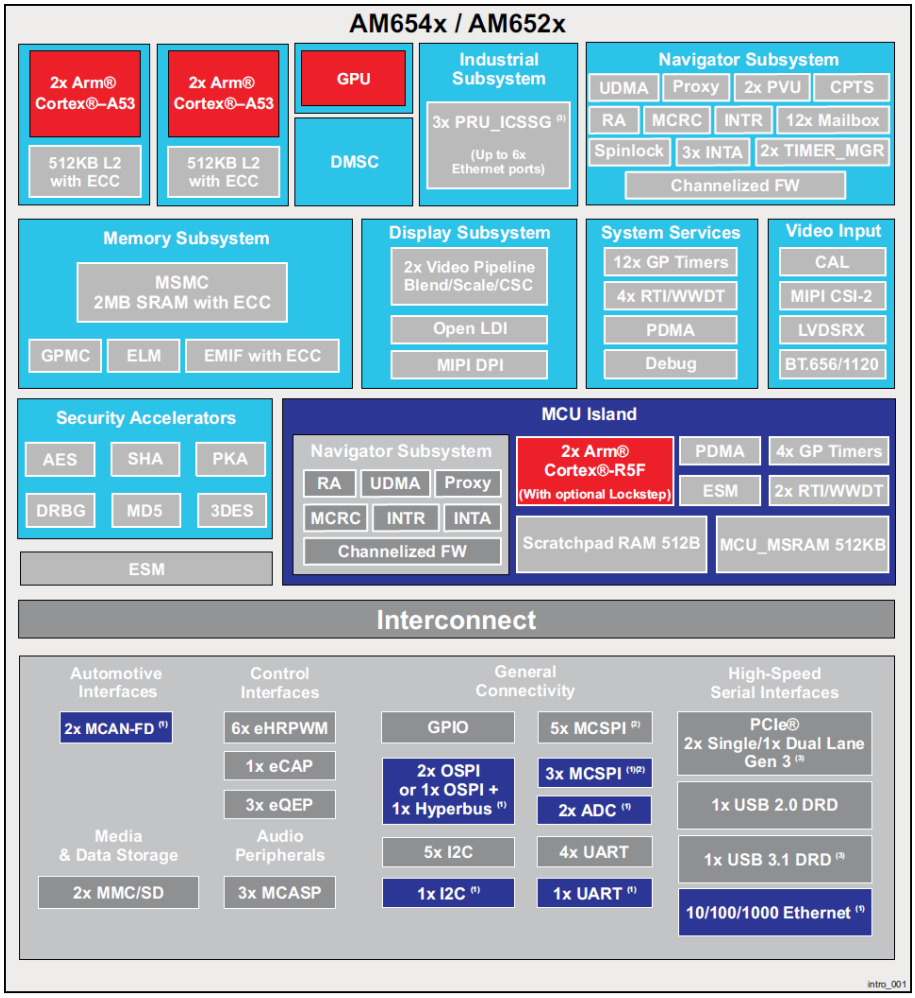
A suitable AM65xx derivative (AM6526, AM6527, AM6528, AM6546, or AM6548) can be selected for each requirement.

All essential CPU signals are routed to the connectors. There are therefore no restrictions for customers using the TQMa65xx with respect to an integrated customised design. All essential components like CPU, DDR4 SDRAM, eMMC, RTC, EEPROM, power supply, and power management are already integrated on the TQMa65xx.

The main features of the TQMa65xx are:

- TI AM65xx CPU with up to 4 × ARM® Cortex-A53 and 2 × ARM® Cortex-R5F cores
- CPU derivatives: AM6526, AM6527, AM6528, AM6546, or AM6548
- Up to 4 Gbyte DDR4 SDRAM, optional additional ECC
- Up to 64 Gbyte eMMC NAND flash
- Up to 512 Mbyte OSPI NOR flash (optional)
- 64 Kbit EEPROM
- EEPROM + temperature sensor
- On-board RTC
- Secure Element (optional)
- All essential AM65XX signals are routed to the TQMa65xx connectors
- Extended temperature range
- 5 V single supply voltage

2.1 Block diagram AM65xx



(1) This interface is located on the MCU Island but is available for the full system to access.
(2) One port is internally connected only; not connected to any pins.
(3) SGMII, USB3.1 and PCIe share a total of two SerDes lanes.

Figure 1: Block diagram AM65xx CPU family
(Source: Texas Instruments)

2.2 Key functions and characteristics

The following components are implemented on the TQMa65xx:

- AM6526, AM6527, AM6528, AM6546, or AM6548
- DDR4 SDRAM
- eMMC NAND flash
- OSPI NOR flash
- EEPROM
- EEPROM + Temperature sensor
- RTC
- Reset structure
- Power supply with Power Sequencing (single 5 V supply)
- Voltage monitoring
- Boot configuration
- Three connectors (2 × 220 pins, 1 × 120 pins)

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa65xx, and the BSP provided by TQ-Systems, see also chapter 5.

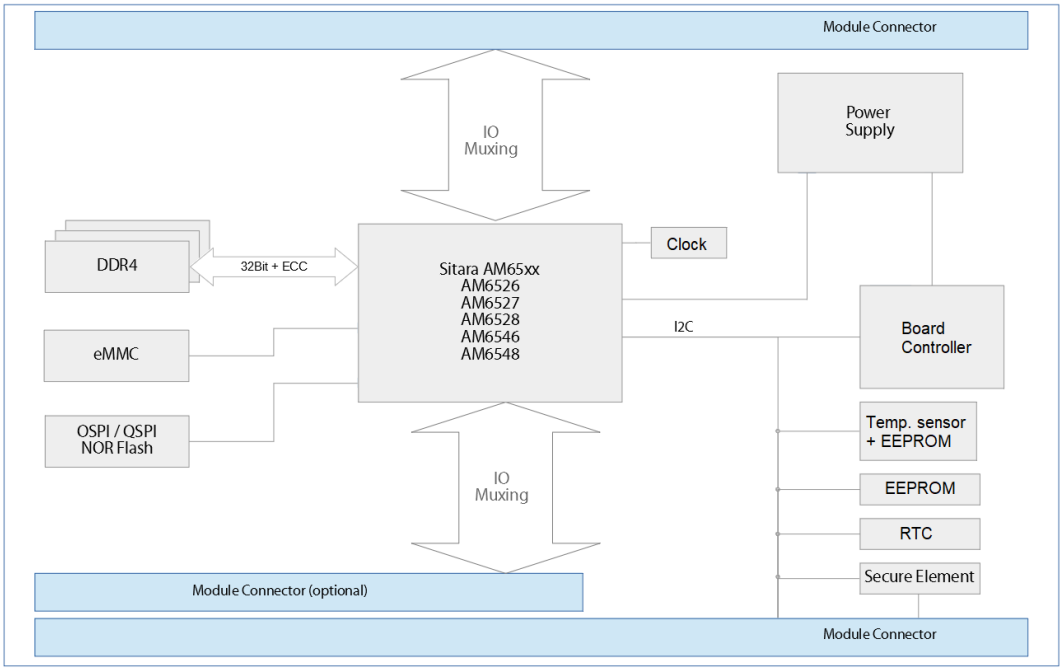


Figure 2: Block diagram TQMa65xx

3.1 Interfaces to other systems and devices

3.1.1 AM65xx pin multiplexing

When using the AM65XX signals, the multiple pin configurations by different AM65xx-internal function units must be taken note of. TI provides a tool showing the multiplexing and simplifies the selection and configuration (TI Pin Mux Tool).

The pin assignment listed in Table 2 to Table 4 refers to the corresponding BSP provided by TQ-Systems in combination with the MBa65xx.

The electrical and pin characteristics are to be taken from the AM65xx Data Sheet (1), and the AM65xx Reference Manual (2).

Attention: Destruction or malfunction, AM65xx pin multiplexing, TQMa65xx reserved pins	
	Depending on the configuration, many AM65xx balls can provide several different functions. Please take note of the information in the AM65xx Reference Manual (2), and the AM65xx Errata (3) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa65xx. Pins marked with “NC” must never be connected and have to be left open.

3.1.2 Pinout TQMa65xx

Table 2: Pinout TQMa65xx connector X1

AM65xx	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	AM65x
–	P	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	P	–
–	P	5 V	Power	VIN	A2	B2	VIN	Power	5 V	P	–
–	P	5 V	Power	VIN	A3	B3	VIN	Power	5 V	P	–
–	P	5 V	Power	VIN	A4	B4	VIN	Power	5 V	P	–
–	P	5 V	Power	VIN	A5	B5	VIN	Power	5 V	P	–
–	P	5 V	Power	VIN	A6	B6	VIN	Power	5 V	P	–
–	P	5 V	Power	VIN	A7	B7	VIN	Power	5 V	P	–
–	P	5 V	Power	VIN	A8	B8	VIN	Power	5 V	P	–
–	P	5 V	Power	VIN	A9	B9	VIN	Power	5 V	P	–
–	P	0 V	Ground	DGND	A10	B10	VIN	Power	5 V	P	–
–	P	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A12	B12	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A13	B13	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A14	B14	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A15	B15	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A16	B16	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A17	B17	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A18	B18	VDD_SD	Power	3.3 V	P	–
–	P	0 V	Ground	DGND	A19	B19	V_BAT	Power	3.3 V	P	–
–	P	1.8 V	Power	VCC1V8L1	A20	B20	VCC3V3S	Power	1.8 / 3.3 V	P	–
–	P	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	P	–
–	P	1.8 V	Power	VCC1V8	A22	B22	VCC3V3	Power	3.3 V	P	–
–	P	1.8 V	Power	VCC1V8	A23	B23	VCC3V3	Power	3.3 V	P	–
–	P	0 V	Ground	DGND	A24	B24	DGND	Ground	0 V	P	–
–	I	3.3 V	JTAG	nSRST_JTAG#	A25	B25	IO1_RES	Factory Test	3.3 V	I/O	–
–	I	1.8 V	SYSTEM	POR#_MB	A26	B26	IO2_RES	Factory Test	3.3 V	I/O	–
C19	O	1.8 / 3.3 V	SYSTEM	POR#_OUT	A27	B27	IO3_RES	Factory Test	3.3 V	I/O	–
–	P	0 V	Ground	DGND	A28	B28	RES_BC#	Factory Test	3.3 V	I	–
AH10	I	1.8 V	SERDES	SERDES1_RXP	A29	B29	SWD_CLK	Factory Test	3.3 V	I	–
AG9	I	1.8 V	SERDES	SERDES1_RXN	A30	B30	SWD_DIO	Factory Test	3.3 V	I/O	–
–	P	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	P	–
AH9	O	1.8 V	SERDES	SERDES1_TXN_C	A32	B32	DGND	Ground	0 V	P	–
AG8	O	1.8 V	SERDES	SERDES1_TXP_C	A33	B33	SERDES0_PCIe_REFCLK0P	SERDES	1.8 V	O	AF10
–	P	0 V	Ground	DGND	A34	B34	SERDES0_PCIe_REFCLK0N	SERDES	1.8 V	O	AF9
AE9	O	1.8 V	SERDES	SERDES1_PCIe_REFCLK1P	A35	B35	DGND	Ground	0 V	P	–
AE8	O	1.8 V	SERDES	SERDES1_PCIe_REFCLK1N	A36	B36	SERDES0_RXN	SERDES	1.8 V	I	AH3
–	P	0 V	Ground	DGND	A37	B37	SERDES0_RXP	SERDES	1.8 V	I	AG2
AH7	O	1.8 V	SERDES	SERDES1_REFCLKP	A38	B38	DGND	Ground	0 V	P	–
AH6	O	1.8 V	SERDES	SERDES1_REFCLKN	A39	B39	SERDES0_TXP_C	SERDES	1.8 V	O	AG3
–	P	0 V	Ground	DGND	A40	B40	SERDES0_TXN_C	SERDES	1.8 V	O	AH4
–	P	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	P	–
AD13	I/O	1.8 / 3.3 V	SPI	SPI0_D1	A42	B42	SERDES0_REFCLKP	SERDES	1.8 V	O	AG6
AE13	I/O	1.8 / 3.3 V	SPI	SPI0_D0	A43	B43	SERDES0_REFCLKN	SERDES	1.8 V	O	AG5
–	P	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	P	–
AG12	I/O	1.8 / 3.3 V	SPI	SPI1_CS1	A45	B45	UART0_CTS#	UART	1.8 / 3.3 V	I	AG11
AD12	I/O	1.8 / 3.3 V	SPI	SPI1_CS0	A46	B46	UART0_RXD	UART	1.8 / 3.3 V	I	AF11
–	P	0 V	Ground	DGND	A47	B47	UART0_TXD	UART	1.8 / 3.3 V	O	AE11
AH13	I/O	1.8 / 3.3 V	SPI	SPI0_CLK	A48	B48	UART0_RST#	UART	1.8 / 3.3 V	O	AD11
–	P	0 V	Ground	DGND	A49	B49	DGND	Ground	0 V	P	–
AH12	I/O	1.8 / 3.3 V	SPI	SPI1_CLK	A50	B50	USB0_VBUS_R	USB	VDDA_3P3_USB	P	AE7
–	P	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–	–
AG13	I/O	1.8 / 3.3 V	SPI	SPI0_CS0	A52	B52	USB0_ID	USB	3.3 V	–	AF1
AF13	I/O	1.8 / 3.3 V	SPI	SPI0_CS1	A53	B53	USB0_DRVVBUS	USB	1.8 / 3.3 V	–	AD9
–	P	0 V	Ground	DGND	A54	B54	DGND	Ground	0 V	P	–
AE12	I/O	1.8 / 3.3 V	SPI	SPI1_D0	A55	B55	USB0_DM	USB	3.3 V	–	AE2

3.1.2 Pinout TQMa65xx (continued)

Table 2: Pinout TQMa65xx connector X1 (continued)

AM65xx	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	AM65x
AF12	I/O	1.8 / 3.3 V	SPI	SPI1_D1	A56	B56	USB0_DP	USB	3.3 V	–	AF1
–	P	0 V	Ground	DGND	A57	B57	DGND	Ground	0 V	P	–
AC3	O	1.8 / 3.3 V	CAN	MCU_MCAN1_TX	A58	B58	USB1_VBUS_R	USB	VDDA_3P3_USB	–	AF6
AD3	I	1.8 / 3.3 V	CAN	MCU_MCAN1_RX	A59	B59	USB1_ID	USB	3.3 V	–	AF5
–	P	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A61	B61	USB1_DRVVBUS	USB	1.8 / 3.3 V	–	AC8
W2	I	1.8 / 3.3 V	CAN	MCU_MCAN0_RX	A62	B62	DGND	Ground	0 V	P	–
W1	O	1.8 / 3.3 V	CAN	MCU_MCAN0_TX	A63	B63	USB1_DP	USB	3.3 V	–	AE1
–	P	0 V	Ground	DGND	A64	B64	USB1_DM	USB	3.3 V	–	AD2
AD6	I/O/D	1.8 / 3.3 V	I2C	WKUP_I2C_SDA	A65	B65	DGND	Ground	0 V	P	–
AC7	I/O/D	1.8 / 3.3 V	I2C	WKUP_I2C_SCL	A66	B66	WKUP_GPIO0_11	GPIO	1.8 / 3.3 V	I/O	AB2
–	P	0 V	Ground	DGND	A67	B67	WKUP_GPIO0_10	GPIO	1.8 / 3.3 V	I/O	AB3
AD7	I/O/D	1.8 / 3.3 V	I2C	MCU_I2C_SDA	A68	B68	WKUP_GPIO0_9	GPIO	1.8 / 3.3 V	I/O	AB4
AD8	I/O/D	1.8 / 3.3 V	I2C	MCU_I2C_SCL	A69	B69	WKUP_GPIO0_8	GPIO	1.8 / 3.3 V	I/O	AC5
–	P	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	P	–
AC1	O	1.8 / 3.3 V	UART	WKUP_UART0_RTSn	A71	B71	WKUP_GPIO0_3	GPIO	1.8 / 3.3 V	I/O	AD1
AC2	I	1.8 / 3.3 V	UART	WKUP_UART0_CTSn	A72	B72	WKUP_GPIO0_2	GPIO	1.8 / 3.3 V	I/O	AE3
AB5	O	1.8 / 3.3 V	UART	WKUP_UART0_TXD	A73	B73	WKUP_GPIO0_1	GPIO	1.8 / 3.3 V	I/O	AF3
AB1	I	1.8 / 3.3 V	UART	WKUP_UART0_RXD	A74	B74	WKUP_GPIO0_0	GPIO	1.8 / 3.3 V	I/O	AF4
–	P	0 V	Ground	DGND	A75	B75	WKUP_GPIO0_33	GPIO	1.8 / 3.3 V	I/O	N3
Y2	I/O	1.8 / 3.3 V	SPI	MCU_SPI0_D1	A76	B76	DGND	Ground	0 V	P	–
Y3	I/O	1.8 / 3.3 V	SPI	MCU_SPI0_D0	A77	B77	DGND	Ground	0 V	P	–
Y4	I/O	1.8 / 3.3 V	SPI	MCU_SPI0_CS0	A78	B78	DGND	Ground	0 V	P	–
Y1	I/O	1.8 / 3.3 V	SPI	MCU_SPI0_CLK	A79	B79	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	P	–
N2	I/O	1.8 / 3.3 V	GPIO	WKUP_GPIO0_32	A81	B81	DGND	Ground	0 V	P	–
P1	I/O	1.8 / 3.3 V	GPIO	WKUP_GPIO0_31	A82	B82	MCU_POR#_OUT	SYSTEM	1.8 / 3.3 V	O	V2
P3	I/O	1.8 / 3.3 V	GPIO	WKUP_GPIO0_28	A83	B83	MCU_WARM_RESET#_OUT	SYSTEM	1.8 / 3.3 V	O	V3
P2	I/O	1.8 / 3.3 V	GPIO	WKUP_GPIO0_27	A84	B84	DGND	Ground	0 V	P	–
R1	I/O	1.8 / 3.3 V	GPIO	WKUP_GPIO0_26	A85	B85	MCU_RESET#_MB	SYSTEM	1.8 / 3.3 V	I	W4
T1	I/O	1.8 / 3.3 V	GPIO	WKUP_GPIO0_25	A86	B86	MCU_SAFETY_ERROR#	SYSTEM	1.8 / 3.3 V	I/O	W3
–	P	0 V	Ground	DGND	A87	B87	DGND	Ground	0 V	P	–
D19	O	1.8 V	SYSTEM	WARM_RESET#_OUT	A88	B88	MCU_UART0_TXD	UART	1.8 / 3.3 V	O	P5
F17	I	1.8 / 3.3 V	SYSTEM	WARM_RESET#_MB	A89	B89	MCU_UART0_RXD	UART	1.8 / 3.3 V	I	P4
–	P	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	P	–
N1	I/O	1.8 / 3.3 V	RGMII	MCU_RGMII1_TXC	A91	B91	MCU_RGMII1_RXC	RGMII	1.8 / 3.3 V	I	M1
N4	O	1.8 / 3.3 V	RGMII	MCU_RGMII1_TX_CTL	A92	B92	MCU_RGMII1_RX_CTL	RGMII	1.8 / 3.3 V	I	N5
M2	O	1.8 / 3.3 V	RGMII	MCU_RGMII1_TD3	A93	B93	MCU_RGMII1_RD0	RGMII	1.8 / 3.3 V	I	L6
M3	O	1.8 / 3.3 V	RGMII	MCU_RGMII1_TD2	A94	B94	MCU_RGMII1_RD1	RGMII	1.8 / 3.3 V	I	M6
M4	O	1.8 / 3.3 V	RGMII	MCU_RGMII1_TD1	A95	B95	MCU_RGMII1_RD2	RGMII	1.8 / 3.3 V	I	L5
M5	O	1.8 / 3.3 V	RGMII	MCU_RGMII1_TD0	A96	B96	MCU_RGMII1_RD3	RGMII	1.8 / 3.3 V	I	L2
–	P	0 V	Ground	DGND	A97	B97	DGND	Ground	0 V	P	–
L1	O	1.8 / 3.3 V	RGMII	MCU_RGMII1_MDC	A98	B98	DGND	Ground	0 V	P	–
L4	I/O	1.8 / 3.3 V	RGMII	MCU_RGMII1_MDIO	A99	B99	SOC_SAFETY_ERROR#	SYSTEM	1.8 V	I/O	E20
–	P	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A101	B101	DGND	Ground	0 V	P	–
H4	A	1.8 V	ADC	MCU_ADC1_AIN7	A102	B102	MCU_ADC0_AIN7	ADC	1.8 V	A	J6
G3	A	1.8 V	ADC	MCU_ADC1_AIN6	A103	B103	MCU_ADC0_AIN6	ADC	1.8 V	A	J2
G5	A	1.8 V	ADC	MCU_ADC1_AIN5	A104	B104	MCU_ADC0_AIN5	ADC	1.8 V	A	J4
F5	A	1.8 V	ADC	MCU_ADC1_AIN4	A105	B105	MCU_ADC0_AIN4	ADC	1.8 V	A	K4
H5	A	1.8 V	ADC	MCU_ADC1_AIN3	A106	B106	MCU_ADC0_AIN3	ADC	1.8 V	A	J5
G4	A	1.8 V	ADC	MCU_ADC1_AIN2	A107	B107	MCU_ADC0_AIN2	ADC	1.8 V	A	J1
G6	A	1.8 V	ADC	MCU_ADC1_AIN1	A108	B108	MCU_ADC0_AIN1	ADC	1.8 V	A	J3
F4	A	1.8 V	ADC	MCU_ADC1_AIN0	A109	B109	MCU_ADC0_AIN0	ADC	1.8 V	A	K5
–	P	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	P	–

3.1.2 Pinout TQMa65xx (continued)

Table 3: Pinout TQMa65xx connector X2

AM65xx	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	AM65x
–	P	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	P	–
AE16	O	1.8 / 3.3 V	RGMII	PRG2_RGMII1_TD3	A2	B2	PRG2_RGMII2_TD3	RGMII	1.8 / 3.3 V	O	AD14
AF16	O	1.8 / 3.3 V	RGMII	PRG2_RGMII1_TD2	A3	B3	PRG2_RGMII2_TD2	RGMII	1.8 / 3.3 V	O	AC15
AG16	O	1.8 / 3.3 V	RGMII	PRG2_RGMII1_TD1	A4	B4	PRG2_RGMII2_TD1	RGMII	1.8 / 3.3 V	O	AF14
AH16	O	1.8 / 3.3 V	RGMII	PRG2_RGMII1_TD0	A5	B5	PRG2_RGMII2_TD0	RGMII	1.8 / 3.3 V	O	AD15
–	P	0 V	Ground	DGND	A6	B6	DGND	Ground	0 V	P	–
AG18	I	1.8 / 3.3 V	RGMII	PRG2_RGMII1_RD3	A7	B7	PRG2_RGMII2_RD3	RGMII	1.8 / 3.3 V	I	AH14
AH17	I	1.8 / 3.3 V	RGMII	PRG2_RGMII1_RD2	A8	B8	PRG2_RGMII2_RD2	RGMII	1.8 / 3.3 V	I	AD17
AE18	I	1.8 / 3.3 V	RGMII	PRG2_RGMII1_RD1	A9	B9	PRG2_RGMII2_RD1	RGMII	1.8 / 3.3 V	I	AC16
AF18	I	1.8 / 3.3 V	RGMII	PRG2_RGMII1_RD0	A10	B10	PRG2_RGMII2_RD0	RGMII	1.8 / 3.3 V	I	AH15
–	P	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	P	–
AG17	I	1.8 / 3.3 V	RGMII	PRG2_RGMII1_RX_CTL	A12	B12	PRG2_RGMII2_RX_CTL	RGMII	1.8 / 3.3 V	I	AG14
AF17	I	1.8 / 3.3 V	RGMII	PRG2_RGMII1_RXC	A13	B13	PRG2_RGMII2_RXC	RGMII	1.8 / 3.3 V	I	AG15
AD16	I/O	1.8 / 3.3 V	RGMII	PRG2_RGMII1_TXC	A14	B14	PRG2_RGMII2_TXC	RGMII	1.8 / 3.3 V	I/O	AE14
AE17	O	1.8 / 3.3 V	RGMII	PRG2_RGMII1_TX_CTL	A15	B15	PRG2_RGMII2_TX_CTL	RGMII	1.8 / 3.3 V	O	AC17
–	P	0 V	Ground	DGND	A16	B16	DGND	Ground	0 V	P	–
AG19	O	1.8 / 3.3 V	RGMII	PRG1_RGMII2_TD3	A17	B17	PRG1_RGMII1_TD3	RGMII	1.8 / 3.3 V	O	AD19
AH19	O	1.8 / 3.3 V	RGMII	PRG1_RGMII2_TD2	A18	B18	PRG1_RGMII1_TD2	RGMII	1.8 / 3.3 V	O	AG20
AF19	O	1.8 / 3.3 V	RGMII	PRG1_RGMII2_TD1	A19	B19	PRG1_RGMII1_TD1	RGMII	1.8 / 3.3 V	O	AH21
AE20	O	1.8 / 3.3 V	RGMII	PRG1_RGMII2_TD0	A20	B20	PRG1_RGMII1_TD0	RGMII	1.8 / 3.3 V	O	AH20
–	P	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	P	–
AH22	I	1.8 / 3.3 V	RGMII	PRG1_RGMII2_RD3	A22	B22	PRG1_RGMII1_RD3	RGMII	1.8 / 3.3 V	I	AD21
AG21	I	1.8 / 3.3 V	RGMII	PRG1_RGMII2_RD2	A23	B23	PRG1_RGMII1_RD2	RGMII	1.8 / 3.3 V	I	AF23
AH23	I	1.8 / 3.3 V	RGMII	PRG1_RGMII2_RD1	A24	B24	PRG1_RGMII1_RD1	RGMII	1.8 / 3.3 V	I	AG24
AH24	I	1.8 / 3.3 V	RGMII	PRG1_RGMII2_RD0	A25	B25	PRG1_RGMII1_RD0	RGMII	1.8 / 3.3 V	I	AE22
–	P	0 V	Ground	DGND	A26	B26	DGND	Ground	0 V	P	–
AE21	I	1.8 / 3.3 V	RGMII	PRG1_RGMII2_RX_CTL	A27	B27	PRG1_RGMII1_RX_CTL	RGMII	1.8 / 3.3 V	I	AG23
AG22	I	1.8 / 3.3 V	RGMII	PRG1_RGMII2_RXC	A28	B28	PRG1_RGMII1_RXC	RGMII	1.8 / 3.3 V	I	AF22
AE19	I/O	1.8 / 3.3 V	RGMII	PRG1_RGMII2_TXC	A29	B29	PRG1_RGMII1_TXC	RGMII	1.8 / 3.3 V	I/O	AD20
AC20	O	1.8 / 3.3 V	RGMII	PRG1_RGMII2_TX_CTL	A30	B30	PRG1_RGMII1_TX_CTL	RGMII	1.8 / 3.3 V	O	AF21
–	P	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	P	–
AE27	O	1.8 / 3.3 V	RGMII	PRG0_RGMII2_TD3	A32	B32	PRG0_RGMII1_TD3	RGMII	1.8 / 3.3 V	O	AA24
AD24	O	1.8 / 3.3 V	RGMII	PRG0_RGMII2_TD2	A33	B33	PRG0_RGMII1_TD2	RGMII	1.8 / 3.3 V	O	AD26
AD25	O	1.8 / 3.3 V	RGMII	PRG0_RGMII2_TD1	A34	B34	PRG0_RGMII1_TD1	RGMII	1.8 / 3.3 V	O	AC26
AC25	O	1.8 / 3.3 V	RGMII	PRG0_RGMII2_TD0	A35	B35	PRG0_RGMII1_TD0	RGMII	1.8 / 3.3 V	O	AD27
–	P	0 V	Ground	DGND	A36	B36	DGND	Ground	0 V	P	–
AB26	I	1.8 / 3.3 V	RGMII	PRG0_RGMII2_RD3	A37	B37	PRG0_RGMII1_RD3	RGMII	1.8 / 3.3 V	I	AA27
AC27	I	1.8 / 3.3 V	RGMII	PRG0_RGMII2_RD2	A38	B38	PRG0_RGMII1_RD2	RGMII	1.8 / 3.3 V	I	W24
AC28	I	1.8 / 3.3 V	RGMII	PRG0_RGMII2_RD1	A39	B39	PRG0_RGMII1_RD1	RGMII	1.8 / 3.3 V	I	W25
AB28	I	1.8 / 3.3 V	RGMII	PRG0_RGMII2_RD0	A40	B40	PRG0_RGMII1_RD0	RGMII	1.8 / 3.3 V	I	V24
–	P	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	P	–
AA25	I	1.8 / 3.3 V	RGMII	PRG0_RGMII2_RX_CTL	A42	B42	PRG0_RGMII1_RX_CTL	RGMII	1.8 / 3.3 V	I	Y24
AB27	I	1.8 / 3.3 V	RGMII	PRG0_RGMII2_RXC	A43	B43	PRG0_RGMII1_RXC	RGMII	1.8 / 3.3 V	I	Y25
AC24	I/O	1.8 / 3.3 V	RGMII	PRG0_RGMII2_TXC	A44	B44	PRG0_RGMII1_TXC	RGMII	1.8 / 3.3 V	I/O	AD28
AB24	O	1.8 / 3.3 V	RGMII	PRG0_RGMII2_TX_CTL	A45	B45	PRG0_RGMII1_TX_CTL	RGMII	1.8 / 3.3 V	O	AB25
–	P	0 V	Ground	DGND	A46	B46	DGND	Ground	0 V	P	–
AH18	O	1.8 / 3.3 V	RGMII	PRG1_MDIO0_MDC	A47	B47	GPIO1_37	GPIO	1.8 / 3.3 V	I/O	V27
AD18	I/O	1.8 / 3.3 V	RGMII	PRG1_MDIO0_MDIO	A48	B48	PRG0_PRU0_GPO5	GPIO	1.8 / 3.3 V	I/O	V28
–	P	0 V	Ground	DGND	A49	B49	VOUT_DE	GPMC	1.8 / 3.3 V	O	T23
AE15	O	1.8 / 3.3 V	RGMII	PRG2_MDIO0_MDC	A50	B50	VOUT_PCLK	GPMC	1.8 / 3.3 V	O	R24
–	P	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	P	–
AC19	I/O	1.8 / 3.3 V	RGMII	PRG2_MDIO0_MDIO	A52	B52	VOUT_HSYNC	GPMC	1.8 / 3.3 V	O	T24
–	P	0 V	Ground	DGND	A53	B53	VOUT_VSYNC	GPMC	1.8 / 3.3 V	O	T25
AE28	O	1.8 / 3.3 V	RGMII	PRG0_MDIO0_MDC	A54	B54	VOUT_DATA23	GPMC	1.8 / 3.3 V	O	R23
AE26	I/O	1.8 / 3.3 V	RGMII	PRG0_MDIO0_MDIO	A55	B55	VOUT_DATA22	GPMC	1.8 / 3.3 V	O	R26

3.1.2 Pinout TQMa65xx (continued)

Table 3: Pinout TQMa65xx connector X2 (continued)

AM65xx	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	AM65x
–	P	0 V	Ground	DGND	A56	B56	VOUT_DATA21	GPMC	1.8 / 3.3 V	O	P23
AF27	I/O	1.8 / 3.3 V	RGMII	PRG1_PRU0_GPO5	A57	B57	VOUT_DATA20	GPMC	1.8 / 3.3 V	O	T28
AF28	I/O	1.8 / 3.3 V	GPIO	GPIO0_64	A58	B58	VOUT_DATA19	GPMC	1.8 / 3.3 V	O	U28
AG25	I/O	1.8 / 3.3 V	GPIO	GPIO0_74	A59	B59	VOUT_DATA18	GPMC	1.8 / 3.3 V	O	P26
–	P	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	P	–
AH26	I/O	1.8 / 3.3 V	GPIO	GPIO0_73	A61	B61	VOUT_DATA17	GPMC	1.8 / 3.3 V	O	P25
AH25	I/O	1.8 / 3.3 V	GPIO	GPIO0_66	A62	B62	VOUT_DATA16	GPMC	1.8 / 3.3 V	O	R28
AG26	I/O	1.8 / 3.3 V	GPIO	GPIO0_75	A63	B63	VOUT_DATA15	GPMC	1.8 / 3.3 V	O	R27
AG27	I/O	1.8 / 3.3 V	GPIO	GPIO0_63	A64	B64	VOUT_DATA14	GPMC	1.8 / 3.3 V	O	P24
AF25	I/O	1.8 / 3.3 V	GPIO	GPIO0_85	A65	B65	VOUT_DATA13	GPMC	1.8 / 3.3 V	O	N25
AF26	I/O	1.8 / 3.3 V	GPIO	GPIO0_65	A66	B66	VOUT_DATA12	GPMC	1.8 / 3.3 V	O	N26
AF24	I/O	1.8 / 3.3 V	GPIO	GPIO0_86	A67	B67	VOUT_DATA11	GPMC	1.8 / 3.3 V	O	P27
AE24	I/O	1.8 / 3.3 V	GPIO	GPIO0_84	A68	B68	VOUT_DATA10	GPMC	1.8 / 3.3 V	O	P28
AE23	I/O	1.8 / 3.3 V	GPIO	GPIO0_93	A69	B69	VOUT_DATA9	GPMC	1.8 / 3.3 V	O	M26
–	P	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	P	–
AD22	I/O	1.8 / 3.3 V	GPIO	GPIO0_94	A71	B71	VOUT_DATA8	GPMC	1.8 / 3.3 V	O	N23
AD23	I/O	1.8 / 3.3 V	GPIO	GPIO0_83	A72	B72	VOUT_DATA7	GPMC	1.8 / 3.3 V	O	M25
AC21	I/O	1.8 / 3.3 V	GPIO	GPIO0_95	A73	B73	VOUT_DATA6	GPMC	1.8 / 3.3 V	O	N28
–	P	0 V	Ground	DGND	A74	B74	VOUT_DATA5	GPMC	1.8 / 3.3 V	O	N27
–	P	0 V	Ground	DGND	A75	B75	VOUT_DATA4	GPMC	1.8 / 3.3 V	O	N24
Y26	I/O	1.8 / 3.3 V	GPIO	GPIO1_67	A76	B76	VOUT_DATA3	GPMC	1.8 / 3.3 V	O	M24
AA28	I/O	1.8 / 3.3 V	GPIO	GPIO1_59	A77	B77	VOUT_DATA2	GPMC	1.8 / 3.3 V	O	M28
Y27	I/O	1.8 / 3.3 V	GPIO	GPIO1_66	A78	B78	VOUT_DATA1	GPMC	1.8 / 3.3 V	O	M23
Y28	I/O	1.8 / 3.3 V	GPIO	GPIO1_58	A79	B79	VOUT_DATA0	GPMC	1.8 / 3.3 V	O	M27
–	P	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	P	–
W26	I/O	1.8 / 3.3 V	GPIO	GPIO1_68	A81	B81	DGND	Ground	0 V	P	–
W28	I/O	1.8 / 3.3 V	GPIO	GPIO1_56	A82	B82	I2C2_SCL	I2C	1.8 / 3.3 V	I/O/D	T27
W27	I/O	1.8 / 3.3 V	GPIO	GPIO1_57	A83	B83	I2C2_SDA	I2C	1.8 / 3.3 V	I/O/D	R25
V26	I/O	1.8 / 3.3 V	GPIO	GPIO1_38	A84	B84	DGND	Ground	0 V	P	–
U27	I/O	1.8 / 3.3 V	GPIO	GPIO1_36	A85	B85	OLDI0_A0P	LCD	1.8 V	I/O	K28
V25	I/O	1.8 / 3.3 V	GPIO	GPIO1_47	A86	B86	OLDI0_A0N	LCD	1.8 V	I/O	J28
U26	I/O	1.8 / 3.3 V	GPIO	GPIO1_46	A87	B87	DGND	Ground	0 V	P	–
U25	I/O	1.8 / 3.3 V	GPIO	GPIO1_39	A88	B88	OLDI0_A1P	LCD	1.8 V	I/O	K27
U24	I/O	1.8 / 3.3 V	GPIO	GPIO1_48	A89	B89	OLDI0_A1N	LCD	1.8 V	I/O	L27
–	P	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	P	–
U23	I/O	1.8 / 3.3 V	GPIO	PRG0_PRU1_GPO5	A91	B91	DGND	Ground	0 V	P	–
AC22	I/O	1.8 / 3.3 V	GPIO	PRG1_PRU1_GPO5	A92	B92	OLDI0_A2P	LCD	1.8 V	I/O	J24
A23	I/O	1.8 / 3.3 V	GPIO	GPIO1_13	A93	B93	OLDI0_A2N	LCD	1.8 V	I/O	K24
B23	I/O	1.8 / 3.3 V	GPIO	GPIO1_14	A94	B94	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A95	B95	OLDI0_A3P	LCD	1.8 V	I/O	K26
D28	I/O	1.8 / 3.3 V	MMC/SD	SD_DAT0	A96	B96	OLDI0_A3N	LCD	1.8 V	I/O	J26
E27	I/O	1.8 / 3.3 V	MMC/SD	SD_DAT1	A97	B97	DGND	Ground	0 V	P	–
D26	I/O	1.8 / 3.3 V	MMC/SD	SD_DAT2	A98	B98	OLDI0_CLKN	LCD	1.8 V	I/O	L25
D27	I/O	1.8 / 3.3 V	MMC/SD	SD_DAT3	A99	B99	OLDI0_CLKP	LCD	1.8 V	I/O	K25
–	P	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	P	–
C28	I/O	1.8 / 3.3 V	MMC/SD	SD_CMD	A101	B101	NMI#	SYSTEM	1.8 / 3.3 V	I	F18
C24	I	1.8 / 3.3 V	MMC/SD	SD_SDWP	A102	B102	ECAP0_IN_APWM_OUT	PWM	1.8 / 3.3 V	I/O	D21
B24	I	1.8 / 3.3 V	MMC/SD	SD_SDCD	A103	B103	TIMER_IO1	TIMER	1.8 / 3.3 V	I/O	C23
C27	O	1.8 / 3.3 V	MMC/SD	SD_CLK_R	A104	B104	TIMER_IO0	TIMER	1.8 / 3.3 V	I/O	B22
–	P	0 V	Ground	DGND	A105	B105	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A106	B106	I2C0_SDA	I2C	1.8 / 3.3 V	I/O/D	C21
A22	I	1.8 / 3.3 V	SYSTEM	EXT_REFCLK1	A107	B107	I2C0_SCL	I2C	1.8 / 3.3 V	I/O/D	D20
–	P	0 V	Ground	DGND	A108	B108	I2C1_SDA	I2C	1.8 / 3.3 V	I/O/D	E21
AD15	O	1.8 V	SYSTEM	OSC1	A109	B109	I2C1_SCL	I2C	1.8 / 3.3 V	I	B21
–	P	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	P	–

3.1.2 Pinout TQMa65xx (continued)

Table 4: Pinout TQMa65xx connector X3

AM65xx	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	AM65x
–	P	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	P	–
V1	O	1.8 / 3.3 V	XSPI	XSPI_CLK	A2	B2	NC	NC	–	–	–
–	P	0 V	Ground	DGND	A3	B3	NC	NC	–	–	–
R4	O	1.8 / 3.3 V	XSPI	XSPI_CS0	A4	B4	NC	NC	–	–	–
U2	I	1.8 / 3.3 V	XSPI	XSPI_DQS	A5	B5	NC	NC	–	–	–
–	P	0 V	Ground	DGND	A6	B6	DGND	Ground	0 V	P	–
U4	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ0	A7	B7	NC	NC	–	–	–
U5	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ1	A8	B8	NC	NC	–	–	–
T2	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ2	A9	B9	NC	NC	–	–	–
T3	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ3	A10	B10	NC	NC	–	–	–
T4	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ4	A11	B11	NC	NC	–	–	–
T5	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ5	A12	B12	NC	NC	–	–	–
R2	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ6	A13	B13	NC	NC	–	–	–
R3	I/O	1.8 / 3.3 V	XSPI	XSPI_DQ7	A14	B14	NC	NC	–	–	–
R5	O	1.8 / 3.3 V	XSPI	XSPI_CS1	A15	B15	NC	NC	–	–	–
–	P	0 V	Ground	DGND	A16	B16	DGND	Ground	0 V	P	–
U1	O	1.8 / 3.3 V	XSPI	XSPI_LBCLKO	A17	B17	JTAG_EMU1	JTAG	1.8 / 3.3 V	I/O	AA1
–	P	0 V	Ground	DGND	A18	B18	JTAG_EMU0	JTAG	1.8 / 3.3 V	I/O	AA1
–	–	–	NC	NC	A19	B19	JTAG_TRST#	JTAG	1.8 / 3.3 V	I	AA3
–	–	–	NC	NC	A20	B20	DGND	Ground	0 V	P	–
–	–	–	NC	NC	A21	B21	JTAG_TCK	JTAG	1.8 / 3.3 V	I	AA4
–	–	–	NC	NC	A22	B22	DGND	Ground	0 V	P	–
–	–	–	NC	NC	A23	B23	JTAG_TDO	JTAG	1.8 / 3.3 V	O/Z	A20
–	–	–	NC	NC	A24	B24	JTAG_TMS	JTAG	1.8 / 3.3 V	I	A21
–	–	–	NC	NC	A25	B25	JTAG_TDI	JTAG	1.8 / 3.3 V	I	C20
–	P	0 V	Ground	DGND	A26	B26	DGND	Ground	0 V	P	–
–	–	–	NC	NC	A27	B27	SE_ISO_7816_IO1	SECURITY	3.3 V	I/O	–
–	–	–	NC	NC	A28	B28	SE_ISO_7816_IO2	SECURITY	3.3 V	I/O	–
–	–	–	NC	NC	A29	B29	SE_ISO_14443_LA	SECURITY	–	I/O	–
–	–	–	NC	NC	A30	B30	SE_ISO_14443_LB	SECURITY	–	I/O	–
–	–	–	NC	NC	A31	B31	SE_ISO_7816_RST#	SECURITY	3.3 V	I	–
–	–	–	NC	NC	A32	B32	DGND	Ground	0 V	P	–
–	–	–	NC	NC	A33	B33	SE_ISO_7816_CLK	SECURITY	3.3 V	I	–
–	–	–	NC	NC	A34	B34	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A35	B35	DGND	Ground	0 V	P	–
B25	O	1.8 / 3.3 V	MMC/SD	eMMC_CLK	A36	B36	NC	NC	–	–	–
–	P	0 V	Ground	DGND	A37	B37	NC	NC	–	–	–
B27	O	1.8 / 3.3 V	MMC/SD	eMMC_CMD	A38	B38	NC	NC	–	–	–
C25	I	1.8 / 3.3 V	MMC/SD	eMMC_DS	A39	B39	NC	NC	–	–	–
A26	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT0	A40	B40	NC	NC	–	–	–
E25	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT1	A41	B41	DGND	Ground	0 V	P	–
C26	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT2	A42	B42	DGND	Ground	0 V	P	–
A25	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT3	A43	B43	CSI0_RXN4	CSI	1.8 V	I	G24
E24	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT4	A44	B44	CSI0_RXP4	CSI	1.8 V	I	F24
–	P	0 V	Ground	DGND	A45	B45	DGND	Ground	0 V	P	–
B24	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT5	A46	B46	CSI0_RXN3	CSI	1.8 V	I	H25
B26	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT6	A47	B47	CSI0_RXP3	CSI	1.8 V	I	G25
D25	I/O	1.8 / 3.3 V	MMC/SD	eMMC_DAT7	A48	B48	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A49	B49	CSI0_RXN2	CSI	1.8 V	I	F26
–	–	–	NC	NC	A50	B50	CSI0_RXP2	CSI	1.8 V	I	G26
–	–	–	NC	NC	A51	B51	DGND	CSI	0 V	P	–
–	–	–	NC	NC	A52	B52	CSI0_RXN1	CSI	1.8 V	I	H27
–	–	–	NC	NC	A53	B53	CSI0_RXP1	CSI	1.8 V	I	G27
–	–	–	NC	NC	A54	B54	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A55	B55	DGND	Ground	0 V	P	–
–	–	–	NC	NC	A56	B56	CSI0_RXN0	CSI	1.8 V	I	G28
–	–	–	NC	NC	A57	B57	CSI0_RXP0	CSI	1.8 V	I	F28
–	–	–	NC	NC	A58	B58	DGND	Ground	0 V	P	–
–	–	–	NC	NC	A59	B59	DGND	Ground	0 V	P	–
–	P	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	P	–

3.2 System components

3.2.1 AM65xx CPU

Depending on the TQMa65xx version, one of the following AM65xx derivatives is assembled:

- AM6526
- AM6527
- AM6528
- AM6546
- AM6548

Attention: Destruction or malfunction, AM65xx errata	
	Please take note of the current AM65xx errata (3).

Attention: MMCSD peripherals, no HS400 mode	
	MMCSD peripherals do not support the Multimedia Card HS400 mode. Please take note of the current AM65xx errata (3).

3.2.1.1 Boot Mode

The Boot Mode configuration of the AM65xx is selected via boot strapping pins when the reset is released.
At this time the correct levels must be applied to the corresponding AM65XX pins to ensure the desired configuration.
More information about boot interfaces and its configuration is to be taken from the AM65xx Data Sheet (1) and the AM65xx Reference Manual (2).
Standard boot devices are, e.g. the eMMC or the QSPI NOR flash on the TQMa65xx, or an SD card on the carrier board.
The boot configuration pins are multiplexed. For this reason, tri-state buffers should be used for other usage of these pins.

Note: Field software updates	
	When designing a carrier board, it is recommended to have a redundant update concept for field software updates.

3.2.1.2 MCU Boot Mode Selection

The MCU_BOOTMODE[9:0] pins have to be configured on the carrier board (e.g., MBa65xx).

Table 5: MCU_BOOTMODE Pin Mapping

9	8	7	6	5	4	3	2	1	0
1.8 V MMC/SD	POST [1]				Reserved [2]		Ref Clock		

Table 6: PLL Reference Clock Selection

MCU_BOOTMODE Pins			Ref Clock (MHz)
2	1	0	
0	0	0	19.2
0	0	1	20
0	1	0	24
0	1	1	25
1	0	0	26
1	0	1	27
1	1	0	Reserved
1	1	1	No PLL configuration (slow speed backup)

Table 7: POST Selection

MCU_BOOTMODE Pins				POST Select
8	7	6	5	
0	0	0	0	POST bypass
X	X	X	1	Enable POST DMSC, MCU LBIST Parallel
X	X	1	X	POST DMSC LBIST Enable
X	1	X	X	POST MCU LBIST Enable
1	X	X	X	POST PBIST Enable

Table 8: 1.8V LDO Configuration

MCU_BOOTMODE Pin	1.8V MMC/SD
9	
0	MMCSD0 connected to 1.8V LDO
1	MMCSD1 connected to 1.8V LDO

1: Only on safety-enabled devices. Refer to device Datasheet for device nomenclature.
2: Always set to 0s (via pulldowns to VSS).

3.2.1.3 Boot Mode pin mapping

In normal boot operation the ROM execution is directed through the main BOOTMODE[18:0] pins.

Table 9: BOOTMODE Pin Mapping

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Backup Config			Primary Config								Min	Backup Mode			Primary Mode			

Table 10: Primary Boot Mode Selection

BOOTMODE Pins				Primary Boot Mode Selected
3	2	1	0	
0	0	0	0	Sleep (No boot – debug mode)
0	0	0	1	OSPI
0	0	1	0	QSPI
0	0	1	1	Hyperflash
0	1	0	0	SPI (on QSPI/OSPI port 0 in legacy SPI mode)
0	1	0	1	I^2C
0	1	1	0	MMC/SD card, eMMC boot from UDA or file system
0	1	1	1	Ethernet
1	0	0	0	USB
1	0	0	1	PCIe
1	0	1	0	UART
1	0	1	1	Reserved
1	1	0	0	GPMC NOR
1	1	0	1	eMMC boot from boot partition (with auto-fall back to file system)
1	1	1	0	Reserved (acts as Sleep)
1	1	1	1	Reserved (acts as Sleep)

Table 11: Backup Mode Selection

BOOTMODE Pins			Backup Boot Mode Selected
6	5	4	
0	0	0	None (no backup boot will be attempted)
0	0	1	USB
0	1	0	UART
0	1	1	Ethernet
1	0	0	MMC/SD
1	0	1	SPI (on OSPI port 0 in legacy SPI mode)
1	1	0	Hyperflash
1	1	1	I^2C

3.2.1.3 Boot Mode pin mapping (continued)

Table 12: Min Pin Configuration

BOOTMODE Pin 7	Min Pin Configuration
0	All boot mode pins must be properly set
1	Certain boot mode pins are don't cares. ROM code uses built-in values instead.

Table 13: Primary Boot Mode Configuration

BOOTMODE Pins [3]									Boot Mode	Description
15	14	13	12	11	10	9	8	3 – 0		
								0000	Sleep	Boot not attempted
Pin Cmd		Iclk	Csel		Speed		Addr Width	0001	OSPI	–
Port	Pin Cmd	Iclk	Csel		Speed		Addr Width	0010	QSPI	–
			ns	Csel		Speed		0011	Hyperflash	–
Port	Mode		Csel		Read Cmd	Addr Width		0100	SPI	–
		Bus Reset		Mode	Speed	Addr		0101	I2C	–
		Volt	Port	Interface Config			1bit	0110	MMC/SD	–
Clken	Clkf	Interface		Speed	Duplex	Extern conf		0111	Ethernet	–
					Mode		Port	1000	USB	–
Port	Dual	Sref						1001	PCIe	–
								1010	UART	–
Base	A/D mux		Csel Size		Csel		Bus Width	1100	GPMC NOR	–
	Port	Alt	Bus Width		Speed		Ack	1101	eMMC	–

Table 14: Backup Boot Mode Configuration

BOOTMODE Pins [3]				Backup Boot Mode	Description
18	17	16	6 – 4		
			000	None	No backup boot performed
Mode		Port	001	USB	–
			010	UART	–
Clkout	Interface		011	Ethernet	–
Volt	Port	1bit	100	MMC/SD	–
Port	Addr Width/Cmd		101	SPI	–
Csel	Speed		110	Hyperflash	–
Bus Reset	Mode	Addr	111	I2C	–

3: Shaded cells are don't cares and pins can take any value.

3.2.2 Memory

3.2.2.1 DDR4 SDRAM

The DDR4 is connected to the AM65xx CPU via a 39-bit wide DDR interface. (32 bits data plus 7 bits ECC.)
The DDR4 SDRAM has a maximum throughput of 1600 MT/s (= 800 MHz DDR4 clock).
A maximum of 4 Gbyte DDR4 SDRAM plus optional ECC can be assembled on the TQMa65xx.

3.2.2.2 eMMC

The AM65XX provides two MMCSD controller. Both MMCSD interfaces are routed to the TQMa65xx connectors.
The eMMC on the TQMa65xx is connected with 8 bit to MMCSD0 and meets eMMC standard v5.1.
Up to 64 Gbyte eMMC can be assembled on the TQMa65xx.
Please note that HS400 is not possible on account of a CPU erratum.
MMCSD1 with 4-bit is intended for the SD card interface.
Devices, which meet SD 4.10 or SDIO 4.0 can be connected on the carrier board, if the eMMC on the TQMa65xx is not assembled.

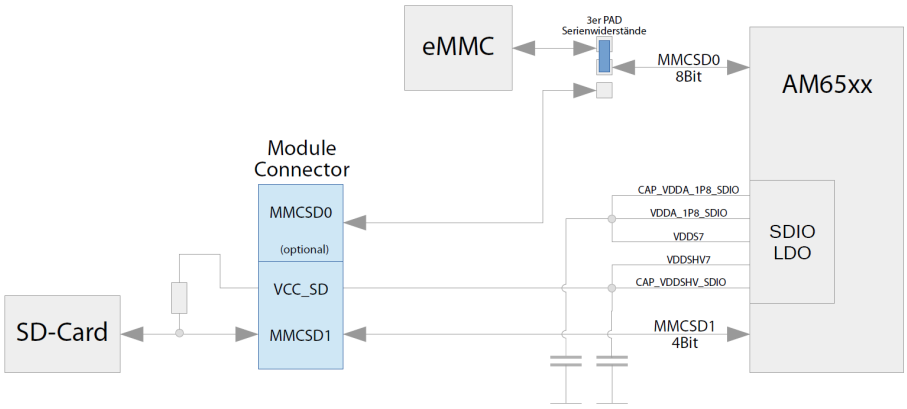


Figure 3: Block diagram MMCSD interface

The following eMMC modes are **not** supported at the AM65xx MMCSD ports:

Table 15: Unsupported eMMC modes

MMCSD port	MMC	SD card
MMCSD0	– 3.0 V and 1.8 V – HS400 DDR: 1.8 V, 2-200 MHz, 8-bit, 400 Mbyte/s	– UHS II
MMCSD1	– 3.0 V and 1.8 V – All 8-bit Modes	– UHS II

3.2.2.3 OSPI NOR flash

The AM65xx provides two Octal SPI interfaces OSPI0 (8 bits) and OSPI1 (4 bits), which can operate in Quad SPI, Octal SPI or HyperBus mode. All OSPI signals are routed to the TQMa65xx connectors.

- TQMa65xx variants:
  - Quad-SPI, Octal-SPI and HyperBus are supported.
  - No NOR assembled on TQMa65xx: OSPI0 and OSPI1 are available at TQMa65xx connectors
  - Single-Die NOR assembled on TQMa65xx: OSPI1 is available at TQMa65xx connectors

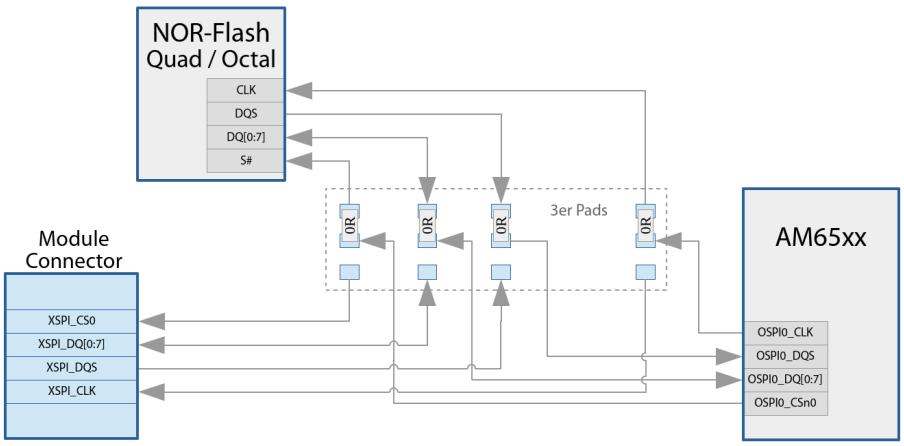


Figure 4: Block diagram OSPI interface

Attention: Malfunction or destruction, OSPI interface	
	The OSPI interface may only be used as memory interface. Other SPI devices have to be connected at the MCSPI interfaces.

3.2.2.4 EEPROM

A 64 Kbit serial EEPROM type 24LC64T, controlled by the WKUP_I2C bus, is assembled. Write-Protect (WP#) is not supported. To store data “read-only”, the EEPROM with temperature sensor must be used, see 3.2.2.5.

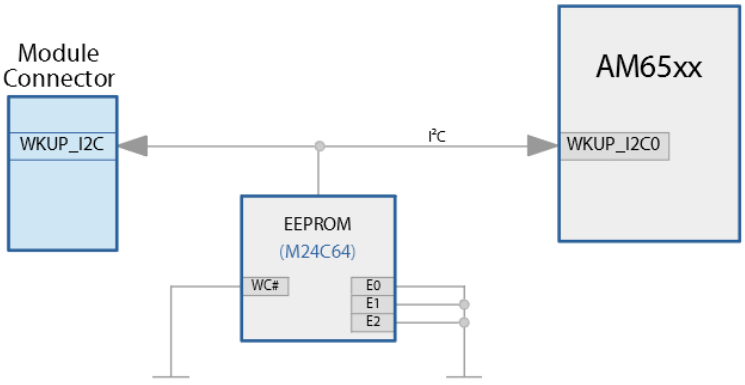


Figure 5: Block diagram EEPROM

➢ The EEPROM has I²C address `0x50 / 101 0000b`

3.2.2.5 EEPROM with temperature sensor

A serial EEPROM including temperature sensor NXP SE97BTP, controlled by the WKUP_I2C bus, is assembled on the TQMa65xx. The lower 128 bytes (addresses 00h to 7Fh) can be set to Permanent Write Protected (PWP) mode or Reversible Write Protected (RWP) mode by software. The upper 128 bytes (addresses 80h to FFh) cannot be write-protected and can be used for general data storage. The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa65xx.

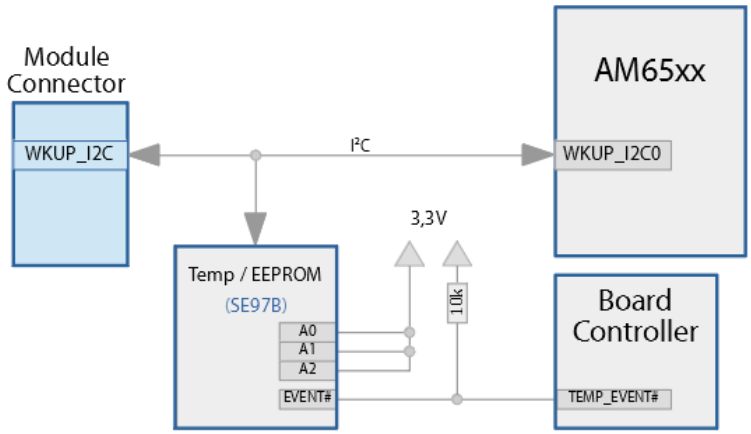


Figure 6: Block diagram temperature sensor interface

- The device has the following I²C addresses:
  - EEPROM (Normal Mode): 0x57 / 101 0111b
  - EEPROM (Protected Mode): 0x37 / 011 0111b
  - Temperature sensor: 0x1F / 001 1111b

The EEPROM with temperature sensor (D4) is assembled next to the AM65xx on the top side of the TQMa65xx, see Figure 14.

Table 16: Temperature sensor SE97BTP

Manufacturer	Device	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±1 °C Max. ±2 °C Max. ±3 °C	+75 °C to +95 °C +40 °C to +125 °C –40 °C to +125 °C

3.2.3 RTC

The TQMa65xx provides a discrete RTC PCF85063A. The accuracy of the RTC is essentially determined by the characteristics of the quartz used. The RTC on the TQMa65xx is clocked by a 32.768 kHz crystal with a tolerance of ±20 ppm (+25 °C). This equals to a deviation of 1.7 s/day or ±30 ppm (+85 °C) = 2.6 s/day. The RTC is connected to the WKUP_I2C bus.

Interrupt Signal RTC_INT# is connected to the TQMa65xx Board Controller.

The RTC can be supplied at pin V_BAT (X1-B19). V_BAT has to be between 0.9 V and 3.6 V.

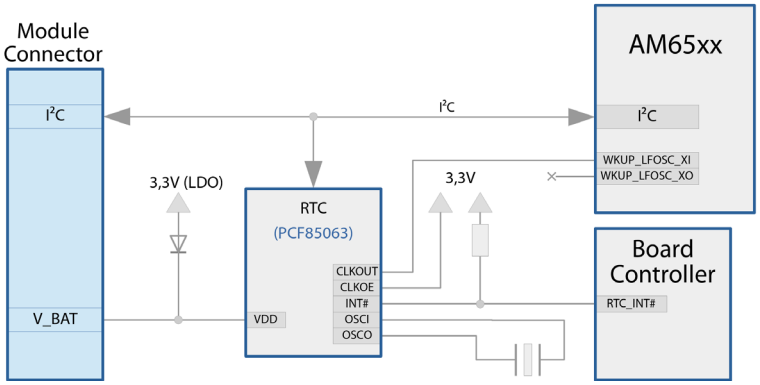


Figure 7: Block diagram RTC

➢ The RTC has I²C address `0x51 / 101 0001b`

3.2.4 Secure Element

An optional Secure Element type SE050 can be assembled on the TQMa65xx.

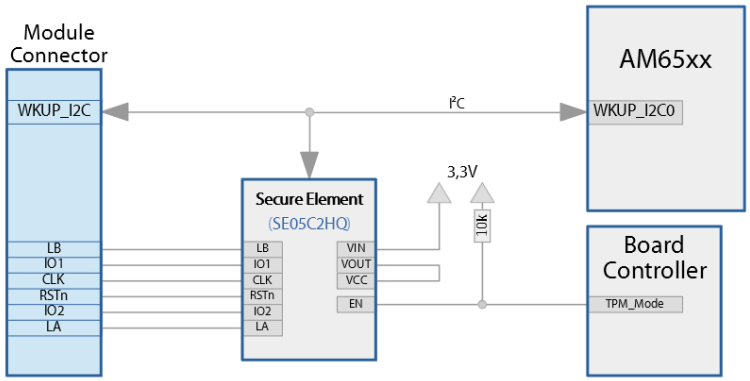


Figure 8: Block diagram Secure Element

➢ The Secure Element has I²C address `0x48 / 100 1000b`

3.2.5 I²C devices

WKUP_I2C is used for the I²C devices on the TQMa65xx. The bus has 4.7 kΩ Pull-Ups on the TQMa65xx.
The following I²C devices are connected to the WKUP_I2C bus on the TQMa65xx:

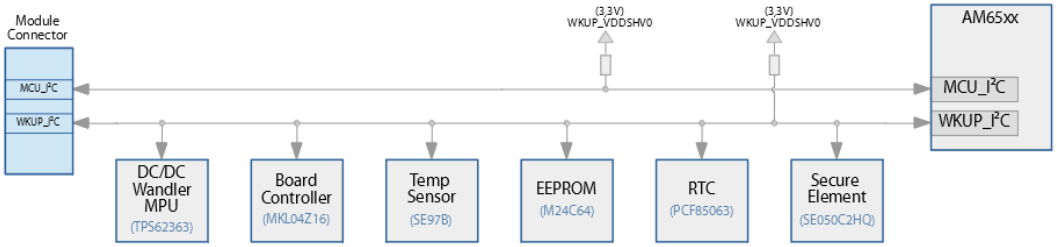


Figure 9: Block diagram I²C devices

Table 17: TQMa65xx WKUP_I2C addresses

Device	Function	Hex / 7-bit address	Remark
SE97BTP	Temperature sensor	0x1F / 001 1111b	Access to temperature registers
	EEPROM	0x57 / 101 0111b	R/W access in Normal Mode
	EEPROM	0x37 / 011 0111b	R/W access in Protected Mode
MKL04Z16	Board Controller	0x11 / 001 0001b	Should not be altered
SE050	Secure Element	0x48 / 100 1000b	Assembly option
M24LC64	EEPROM	0x50 / 101 0000b	For general usage
PCF85063A	RTC	0x51 / 101 0001b	Assembly option
TPS62363Y	Buck regulator	0x60 / 110 0000b	Should not be altered

If more I²C devices are connected to the WKUP_I2C bus on the carrier board, the maximum capacitive bus load according to the I²C standard must be observed. If necessary, additional Pull-Ups have to be provided on the carrier board.

3.2.6 Board Controller

The following housekeeping functions are handled by the Board Controller on the TQMa65xx:

- Voltage supervision
- Power-Up sequencing
- Power modes control
- Temperature monitoring
- Reset control

3.2.7 Reset

POR_MB# holds the TQMa65xx in reset. If POR_MB# is released, the Board Controller starts the initialization.
If no errors occur during power supply start-up and the initialization, the AM65xx is started.
The TQMa65xx reset signal is provided at the connector via POR#_OUT (X1-A27).
Additionally a red LED signals the reset condition. Further reset sources are:

- Requested by software via Board Controller
- Reset by nSRST_JTAG# signal
- Power Supply Error

Reset inputs and outputs are available at the TQMa65xx connectors.

3.3 Power

3.3.1 Power supply

The TQMa65xx only requires a single power supply of 5 V ±5 %.
The TQMa65xx provides the voltages VDD_SD, VCC3V3S, VCC3V3, VCC1V8L1 and VCC1V8, at the TQMa65xx connectors.
These voltages can be fed back to the TQMa65xx on the carrier board according to customer requirements.
The voltages generated on the TQMa65xx may only be used for the TQMa65xx itself.
A further load by circuitry on a carrier board is not permitted and can lead to errors in supply and monitoring.

Attention: Malfunction or destruction, overvoltage	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. A too high input voltage can lead to malfunctions, premature aging or destruction of the TQMa65xx.

3.3.2 TQMa65xx power-up sequencing

The power-up sequencing is carried out and monitored independently by the TQMa65xx.
During power-up the POR# is held low. The power-up sequence is controlled by the Board Controller.

Attention: Cross supply during power-up	
	To avoid cross-supply and errors during the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the sequence is indicated by a high level of signal POR#_OUT.

3.3.3 Power consumption

(TBD)

3.3.4 Power modes

The AM65xx supports several Standby-Modes. Further information can be found in the AM65x documentation (1), (2).
Not all Low-Power Modes are available. The DeeperSleep Mode is currently not supported.

4. MECHANICS

4.1 Connectors

The TQMa65xx is connected to the carrier board with 560 pins on three connectors.

Table 18: TQMa65xx connectors

Manufacturer	Part number	Remark
EPT	2 × 220-pin: 402-51101-51 1 × 120-pin: 402-51401-51	0.5 mm pitch

To avoid damaging the connectors of the TQMa65xx as well as the connectors on the carrier board while removing the TQMa65xx the use of the extraction tool MOZIa65 is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa65xx for the extraction tool MOZIa65.

The following table shows some suitable mating connectors for the carrier board.

Table 19: Carrier board mating connectors

Manufacturer	Part number	Remark	Stack height
EPT	2 × 220-pin: 401-51101-51 1 × 120-pin: 401-51401-51	On MBa65xx	5 mm
	2 × 220-pin: 401-55101-51 1 × 120-pin: 401-55401-51	–	8 mm

The pins assignment in Table 2 to Table 4 refers to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in Table 2 to Table 4 refer to the AM65xx data sheets (2), (3).

4.2 Dimensions

The TQMa65xx has overall dimensions (length × width) of 77 × 55 mm².
The TQMa65xx weighs approximately 30 grams.
The TQMa65xx provides four metalized mounting holes with a diameter 2.7 mm

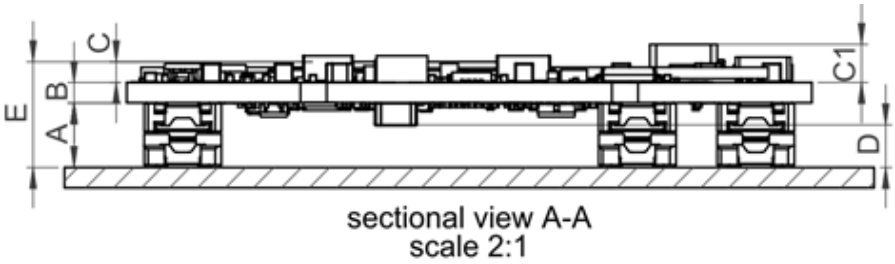


Figure 10: TQMa65xx dimensions, side view

Table 20: TQMa65xx, heights [4]

Dimension	Value / mm	Remark
A	5.10 ±0.07	Board-to-Board distance
B	1.72 ±0.17	PCB thickness
C	1.53 ±0.15	AM65xx height
C1	2.95 ±0.10	Inductor (highest component)
D	3.16 ±0.12	Free space under TQMa65xx
E	8.37 ±0.24	Height to AM65xx surface (not highest component)

A 3D STEP model is available on request. Please contact TQ-Support.

4: Statistical tolerance chain with Gaussian distribution: 99.7 % coverage.

4.2 Dimensions (continued)

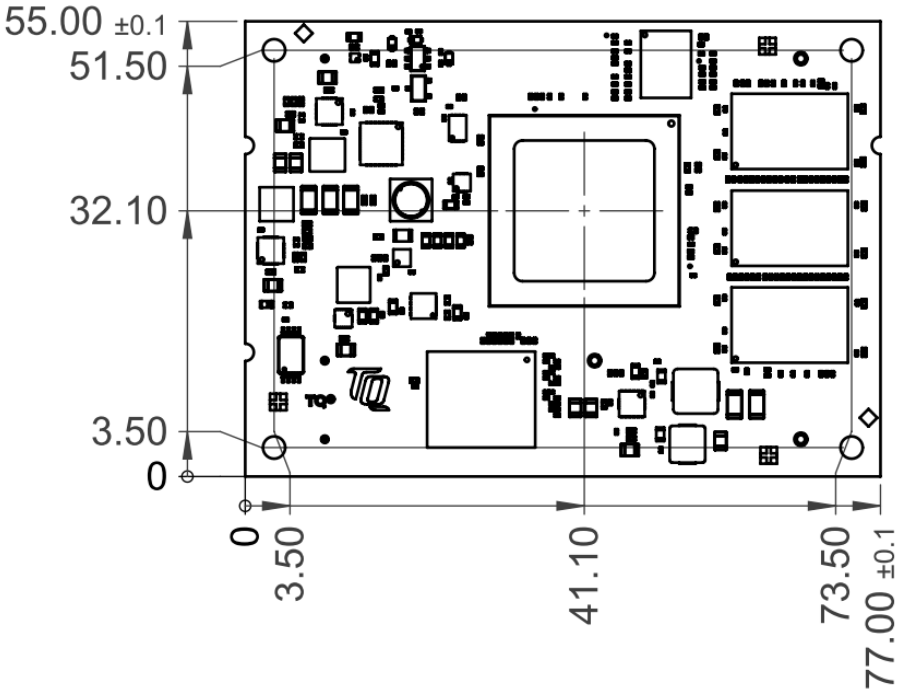


Figure 11: TQMa65xx CPU position, top view

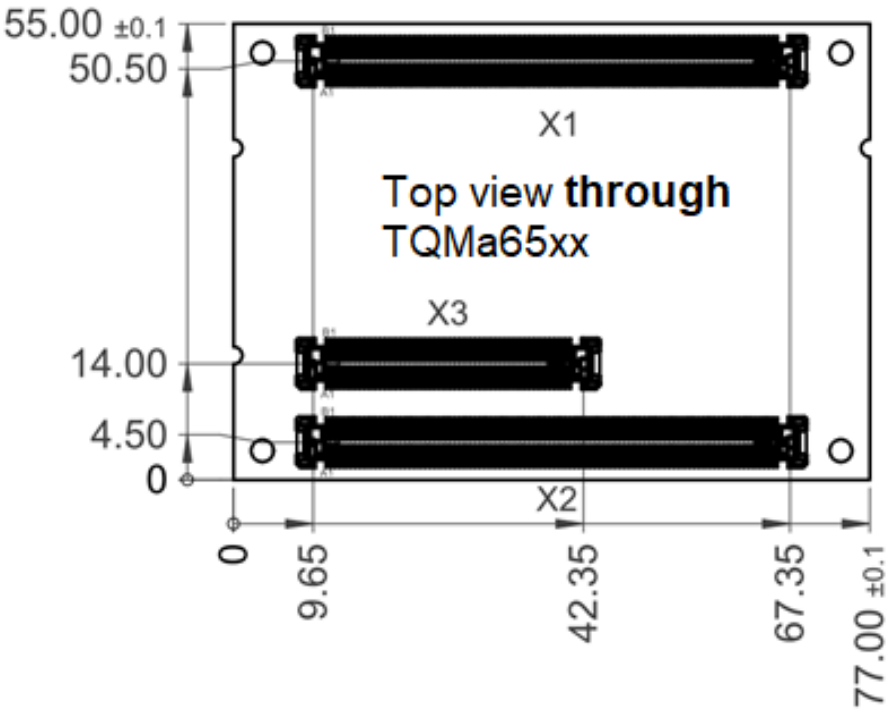


Figure 12: TQMa65xx dimensions, top view through TQMa65xx

4.3 Component placement

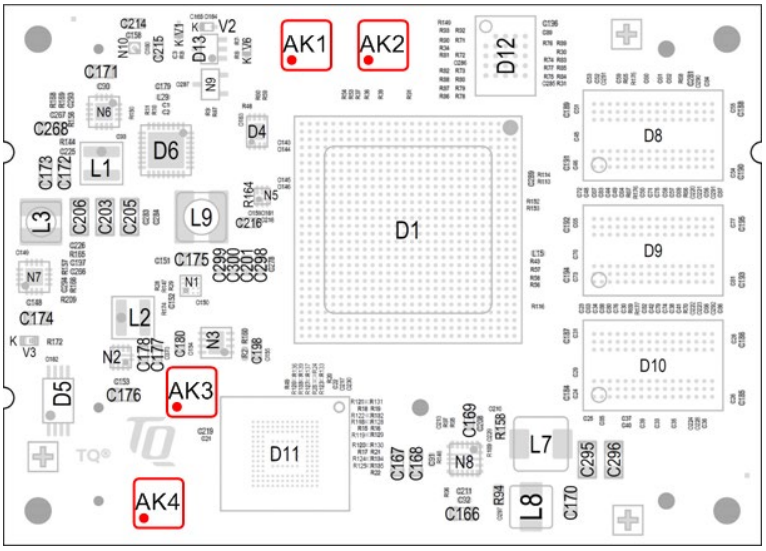


Figure 13: TQMa65xx, component placement top

The labels on the TQMa65xx show the following information:

Table 21: Labels on TQMa65xx

Label	Content
AK1	Serial number
AK2	TQMa65xx version and revision
AK3	MAC address
AK4	Tests performed

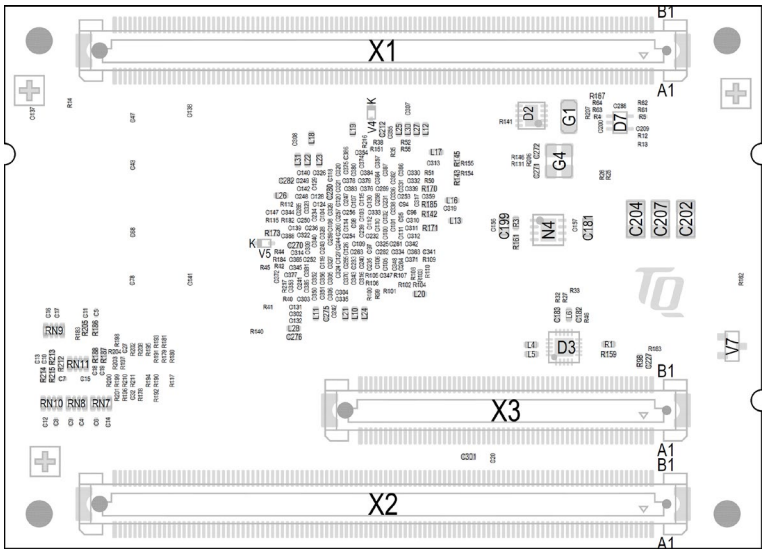


Figure 14: TQMa65xx, component placement bottom

4.4 Protection against external effects

As an embedded module, the TQMa65xx is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.5 Thermal management

To cool the TQMa65xx, in average approximately 6 watts must be dissipated.
The power dissipation originates primarily in the AM65xx, the buck regulators and the DDR4 SDRAM.
The power dissipation also depends on the software used and can vary according to the application.
See AM65xx Data Sheet (1) for further information.

Attention: Destruction or malfunction, TQMa65xx heat dissipation	
	The TQMa65xx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM65xx must be taken into consideration when connecting the heat sink. The AM65xx is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa65xx and thus malfunction, deterioration or destruction.

4.6 Structural requirements

The TQMa65xx is held in the mating connectors by the retention force of the pins (560). For high requirements with respect to vibration and shock firmness, an additional fastening has to be provided in the final product to keep the TQMa65xx in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

4.7 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa65xx may only be extracted from the carrier board by using the extraction tool MOZIa65 that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa65xx for the extraction tool MOZIa65.

5. SOFTWARE

The TQMa65xx is shipped with a preinstalled boot loader U-Boot and a BSP provided by TQ-Systems, which is tailored for the MBa65xx. The boot loader U-Boot provides TQMa65xx-specific as well as board-specific settings, e.g.:

- AM65xx configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.
More information can be found in the Support Wiki for the TQMa65xx.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa65xx was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Stable ground conditions (sufficient ground planes) on the carrier board.
- A sufficient number of block capacitors at all supply voltages
- Keep fast or constantly clocked lines short; avoid interference with other signals
  by means of distance and/or shielding; pay attention not only to the frequency but also to the signal rise times.
- Filtering of all signals which are connected externally (also "slow" and DC voltage signals can emit HF indirectly).
- For critical applications, an EMC shielding hood should be used.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the TQMa65xx.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Shock and vibration

Table 22: Shock resistance

Parameter	Details
Shocks	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 msec
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 23: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 – 9 Hz, 9 – 200 Hz, 200 – 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X – Y – Z axis
Amplitude	2 Hz … 9 Hz: 3.5 ms^{-2} 9 Hz … 200 Hz: 10 ms^{-2} 200 Hz … 500 Hz: 15 ms^{-2}

6.5 Climate and operational conditions

The operating temperature range for the TQMa65xx strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.
In general, reliable operation is ensured if the following conditions are met:

Table 24: Climate and operational conditions –25 °C to +85 °C

Parameter	Range	Remark
Ambient temperature	–25 °C to +85 °C	–
T_j AM65xx	–40 °C to +105 °C	Junction temperature
T_j PMIC	–40 °C to +125 °C	Junction temperature
Case temperature DDR4	–40 °C to +95 °C	–
Case temperature other ICs	–25 °C to +85 °C	–
Storage temperature TQMa65xx	–25 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 25: Climate and operational conditions –40 °C to +85 °C

Parameter	Range	Remark
Ambient temperature	–40 °C to +85 °C	–
T_j AM65xx	–40 °C to +105 °C	Junction temperature
T_j PMIC	–40 °C to +125 °C	Junction temperature
Case temperature DDR4	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Storage temperature TQMa65xx	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

For consumer applications, a version specified for a temperature range of 0 °C to +90 °C can be provided on request.
Detailed information concerning the thermal characteristics of the AM65xx is to be taken from the TI documents (1), and (2).

Attention: Destruction or malfunction, TQMa65xx heat dissipation	
	The TQMa65xx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM65xx must be taken into consideration when connecting the heat sink. The AM65xx is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa65xx and thus malfunction, deterioration or destruction.

6.6 Reliability and service life

The calculated MTBF of the TQMa65xx is 742,536 h @ +40 °C ambient temperature, Ground, Benign.
The TQMa65xx is designed to be insensitive to shock and vibration.
High quality industrial grade connectors are used on the TQMa65xx.

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa65xx is manufactured RoHS compliant. All components and assemblies are RoHS compliant.
The soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa65xx was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa65xx must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa65xx enable compliance with EuP requirements for the TQMa65xx.

7.5 Battery

No batteries are assembled on the TQMa65xx.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa65xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa65xx is delivered in reusable packaging.

7.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 26: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR	Double Data Rate
DIN	Deutsche Industrienorm
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card
EN	Europäische Norm (European Standard)
ESD	Electro-Static Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
GPU	Graphics Processor Unit
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCU	Microcontroller Unit
MMC/SD	Multimedia Card / Secure Digital
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures
NAND	Not-And
NC	Not Connected
NOR	Not-Or
OSPI	Octal Serial Peripheral Interface

8.1 Acronyms and definitions (continued)

Table 26: Acronyms (continued)

Acronym	Meaning
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PMIC	Power Management Integrated Circuit
POST	Power-On Self Test
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
STEP	Standard for Exchange of Products
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 27: Further applicable documents

No.	Name	Rev., Date	Company
(1)	AM65x/DRA80xM Processors Technical Reference Manual	Rev. 1.1, 06/2019	TI
(2)	AM65x/AM652x Sitara Processors Datasheet	Rev. 1, 06/2019	TI
(3)	AM65x/DRA80xM Processors Silicon Errata	Rev., 02/2019	TI
(4)	MKL04Z16 Reference Manual	Rev. 3.1, 11/2012	NXP
(5)	PCF85063A –RTC	Rev. 7, 23.01.2018	NXP
(6)	PROC062_REV E2_SCH Reference Manual	Rev. 1.0, 04.09.2018	TI
(7)	MBa65xx User's Manual	– current –	TQ-Systems
(8)	TQMa65xx Support-Wiki	– current –	TQ-Systems

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