TQMa335x
User's Manual

TQMa335x UM 0106
05.03.2024

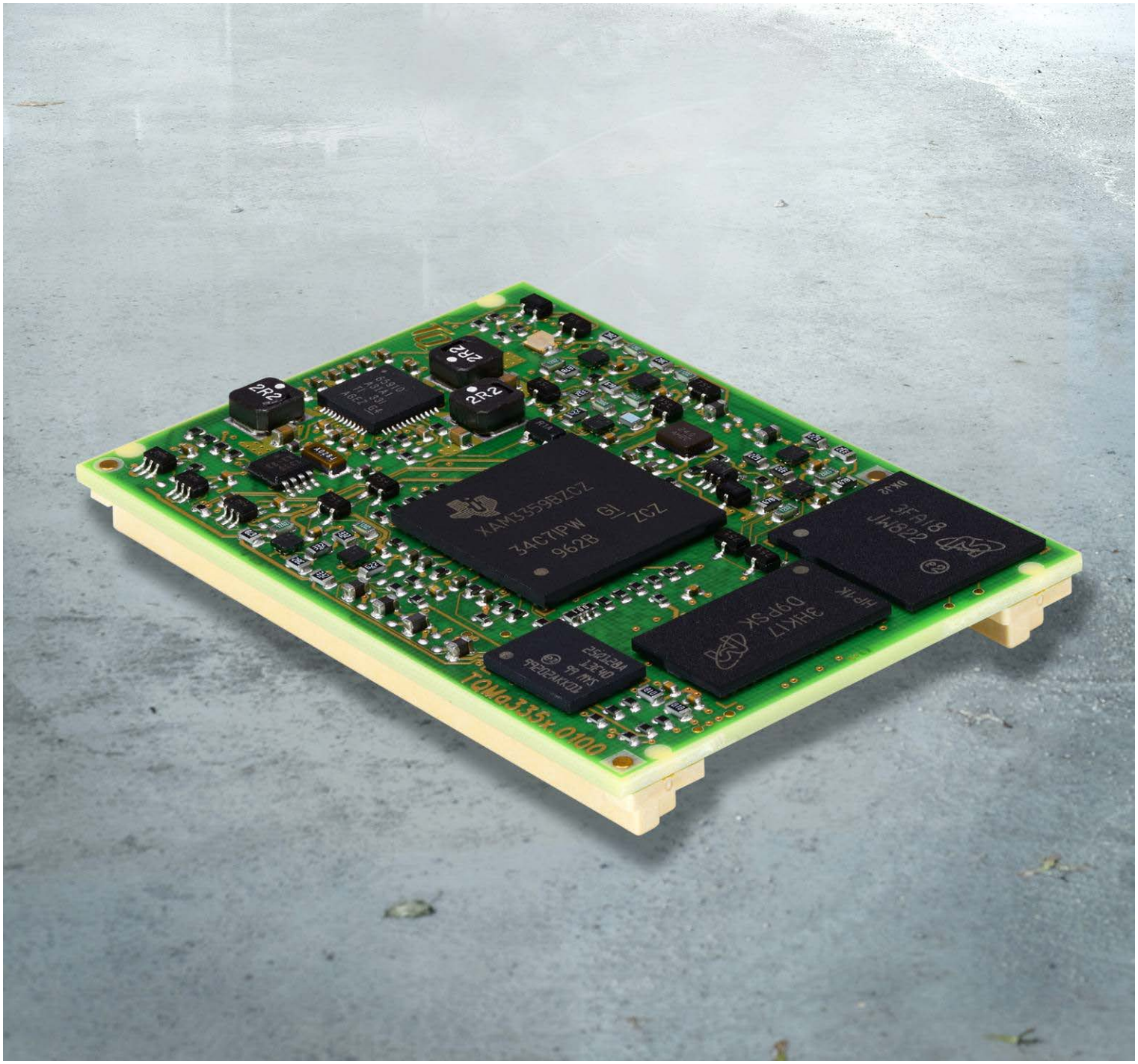

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TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	09.09.2013	Petz		Preliminary document created
0002	26.11.2013	Petz	All	Complete rework
0100	03.08.2015	Petz	All	Complete rework
0101	02.11.2016	Petz	1.4 3.2.3, 3.2.4 3.2.6.8 Table 25 Table 29 Table 38 Table 52	FAX number updated Information and illustrations added, “Note” added Information regarding V_{Ref} added “Direction” clarified Clarified Spelling corrected Updated and extended
0102	07.09.2017	Petz	All Table 14 3.2.3, 3.2.4, 3.2.9.8 Table 44 Table 46, Table 47, Table 51, 6.6.2	“Ball” in table headers replaced with “AM335x ball” Removed Updated, Battery voltage corrected from 3.3 V to 3 V Updated Footnotes added Updated
0103	25.04.2018	Petz	All 1.3, Illustration 16 Table 31 3.2.7, Illustration 12 Table 48	Typo Updated Remarks added Reset LED added Added
0104	04.06.2018	Petz	All Illustration 3 Table 23	External Links updated Updated Remark “22 Ω in series” added
0105	26.10.2018	Petz	All Table 7 3.2.9.5 Illustration 14, Illustration 17 Table 49, Table 50	Formatting, links updated “AM335x ball” in table headers changed to “AM335x” Information added Warning updated Updated “Package temperature” replaced with “Case temperature” Case temperature DDR3L SDRAM changed to +95 °C
0106	05.032024	Kreuzer	3.2.3	“battery” replaced with “electrolytic capacitor”

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive devices and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa335x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you power up the TQMa335x or the Starterkit, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manuals of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa335x circuit diagram
- MBa335x User's Manual
- Sitara AM335x Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqma335x

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa335x, and refers to some software settings.
It does not replace the AM335x Reference Manual.
The TQMa335x is a universal Minimodule based on the Texas Instruments ARM® Cortex® A8 Sitara™ AM335x.
The AM335x Cortex® A8 core works with up to 800 MHz.
The TQMa335x extends the TQC product range and offers an outstanding computing performance.

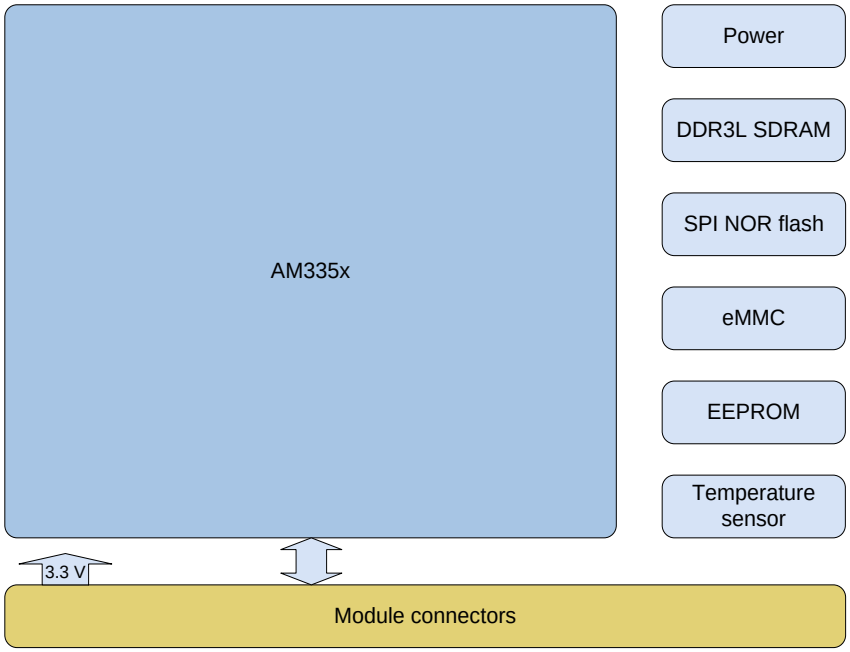


Illustration 1: Block diagram TQMa335x (simplified)

2.1 Key functions and characteristics

The TQMa335x provides the following key functions and characteristics:

- Texas Instruments AM335x
- Up to 512 Mbyte DDR3L SDRAM with 16 bit interface
- Up to 8 Gbyte eMMC NAND flash
- Up to 128 Mbyte SPI NOR flash
- 64 kbit EEPROM
- Texas Instruments PMIC
- Temperature sensor
- RTC (optional)
- All essential AM335x pins are routed to the connectors
- Extended temperature range
- Single power supply 3.3 V

2.2 Available interfaces

The TQMa335x provides the following interfaces at the connectors:

- 2 × Ethernet 10/100/1000 Mbit, RGMII
- 2 × USB 2.0 Hi-Speed
- 2 × CAN 2.0B
- 3 × UART (1 UART with handshake)
- 1 × SD 4 bit (SDIO / MMC / SD card)
- 2 × SPI
- 2 × I^2C
- 1 × I^2S (MCASP0)
- 3 × GPIO
- 4 × PWM
- 1 × parallel display RGB 24 bit
- 1 × JTAG
- 2 × General Purpose Clock
- 8 × AIN inclusive resistive touch controller (12 bit ADC)

As an alternative to the default interfaces further interfaces of the AM335x are available with an adapted pin configuration.
These are amongst others:

- GPMC (General-Purpose Memory Controller)
- PRU-MII1, PRU-MII2 (only available with AM3356, -7, -8, -9)
- PWMSS (Pulse-Width Modulation Subsystem)
- Enhanced Serial Audio Interface
- Ethernet 10/100 RMII
- More audio interfaces
- More I^2C interfaces
- More SPI interfaces
- More UARTs

All useful AM335x signals are routed to the connectors.
There are no restrictions for customers using the TQMa335x with respect to an integrated customised design.
Please take note of that not all listed interfaces can be used simultaneously.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa335x, and the BSP provided by TQ-Systems GmbH, see also section 5.

3.1 System overview

3.1.1 System architecture / block diagram

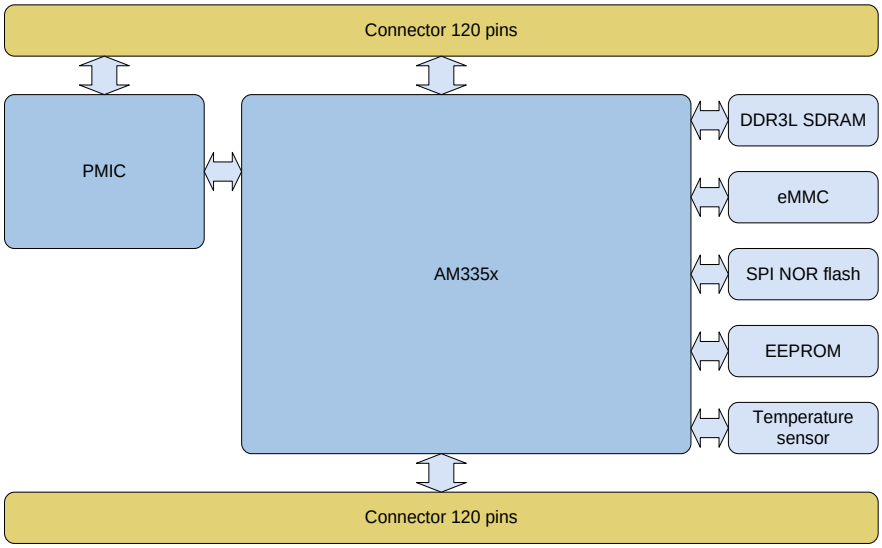


Illustration 2: TQMa335x block diagram

3.1.2 Functionality

The following key functions are implemented on the TQMa335x:

- AM335x (-2, -4, -8, -9, are standard, other on request)
- DDR3L SDRAM
- eMMC NAND flash
- SPI NOR flash
- EEPROM
- Temperature sensor
- Supervisor
- PMIC
- RTC (optional)

3.1.3 Pin multiplexing

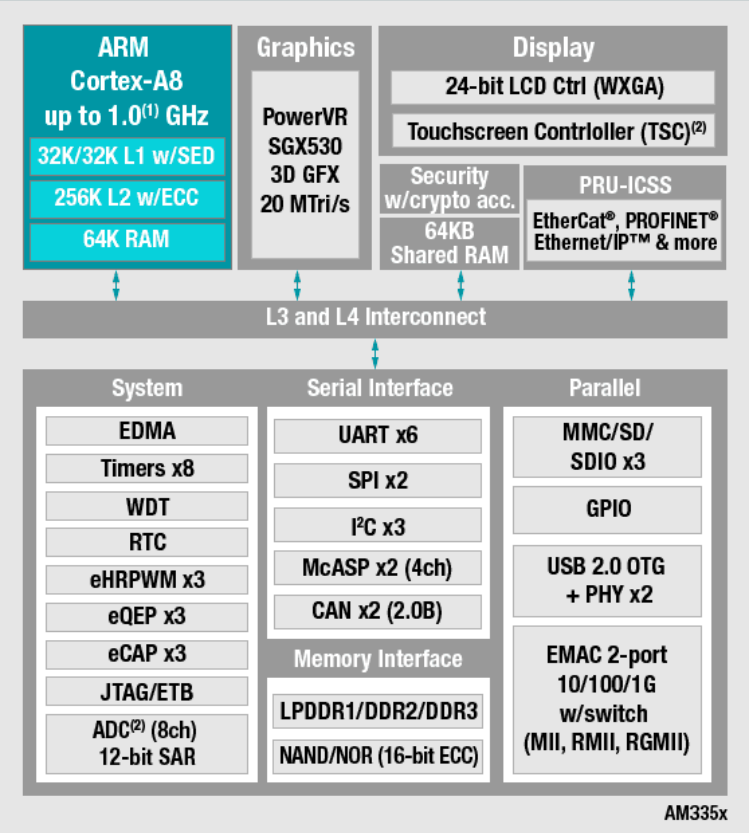
The pin multiplexing of the AM335x permits to use many pins for different interfaces.
The information provided in this User's Manual is based on the BSP provided by TQ-Systems GmbH.

Attention: Destruction or malfunction	
	Many AM335x pins can be configured as different function. Please take note of the information in the AM335x Data Sheet (1) concerning the configuration of these pins before integration / start-up of your carrier board / Starterkit. Please also take note of the latest AM335x errata (7).

3.2 System components

3.2.1 AM335x processor

The following illustration shows the block diagram of the AM335x processor family:



NOTES:
(1) >800MHz available on 15x15 package,13x13 supports up to 600MHz
(2) Use of TSC will limit available ADC channels
SED: Single error detection/parity

Illustration 3: Block diagram AM335x
(Source: Texas Instruments)

3.2.1.1 AM335x derivatives

Depending on the TQMa335x version, one of the following AM335x derivatives is assembled:

Table 2: AM335x derivatives

Description	Part number	Clock	$T_{junction}$	AM335x mask
AM3352	AM3352BZCZA80	800 MHz	–40 °C to +105 °C	2.1
AM3354	AM3354BZCZA80	800 MHz	–40 °C to +105 °C	2.1
AM3358	AM3358BZCZA80	800 MHz	–40 °C to +105 °C	2.1
AM3359	AM3359BZCZA80	800 MHz	–40 °C to +105 °C	2.1

Attention: Malfunction	
	Please take note of the latest AM335x errata (7).

3.2.1.2 Boot modes

The AM335x provides a ROM with integrated boot loader.
After power-up the boot code initialises the hardware and then loads the program image from the selected boot device.
The integrated eMMC or the optional SPI NOR flash can be selected as standard boot device for the TQMa335x.
More external boot devices are available as an alternative to eMMC or SPI NOR flash.
Information thereto can be found in the AM335x Data Sheet (1) and the AM335x Reference Manual (3).
The AM335x supports so-called boot-sequences, i.e. if it fails to boot from the first boot device, it will try to boot from the next one automatically.

Table 3: Boot sequence

Boot Sequence			
1st	2nd	3rd	4th
MMC0 / SD	SPI0 / NOR	UART0 / n.a.	USB0 / n.a.
MMC1/ eMMC	MMC0 / SD	UART0 / n.a.	USB0 / n.a.
SPI0 / NOR	MMC0 / SD	USB0 / n.a.	UART0 / n.a.

The boot device and its configuration as well as other AM335x settings have to be done via Boot Mode Register SYSBOOT.
The register SYSBOOT is read during reset from pins LCD_DATA[15:0].

Attention: Malfunction	
	It has to be ensured that even in the third and fourth boot sequence no pins drive against each other on the carrier board!

The settings for other boot devices are to be taken from the AM335x Data Sheet (1).

3.2.1.3 Boot configuration

The boot configuration of the TQMa335x is defined through 16 GPIO pins.

Note: Boot configuration	
	None of these 16 boot configuration pins are connected on the TQMa335x, which means, the TQMa335x is delivered with no preset boot configuration.

With bits SYSBOOT[15:14] and SYSBOOT[5] some general settings are carried out, independent from the boot device.
The value in the following table printed in **bold** is used on account of the 24 MHz oscillator assembled on the TQMa335x.
The bits SYSBOOT[15:14] set the frequency of the oscillator.

Table 4: Oscillator frequency

SYSBOOT[15:14]	Oscillator frequency / MHz
00b	19.2
01b (default)	**24**
10b	25
11b	26

Bit SYSBOOT[5] indicates whether CLKOUT1 is activated.

Table 5: General boot configuration CLKOUT1

SYSBOOT[5]	CLKOUT1
0	Deactivated
1	Activated

The boot device or the boot sequence is defined with bits SYSBOOT[4:0].
The following table shows the boot sequence defined for the MBa335x.

Table 6: Boot device selection

SYSBOOT[4:0]	Boot Sequence			
	1st	**2nd**	**3rd**	**4th**
10111b	MMC0 / SD	SPI0 / NOR	UART0 / n.a.	USB0 / n.a.
11100b	MMC1 / eMMC	MMC0 / SD	UART0 / n.a.	USB0 / n.a.
11000b	SPI0 / NOR	MMC0 / SD	USB0 / n.a.	UART0 / n.a.

Attention: Malfunction	
	It has to be ensured that even in the third and fourth boot sequence no pins drive against each other on the carrier board!

3.2.1.4 Boot interfaces

The configuration of the following boot devices is described in the next sections:

- MMC0 (external SD card)
- MMC1 (eMMC on TQMa335x)
- SPI0 (NOR flash on TQMa335x)

Attention: Destruction or malfunction	
	Many AM335x pins can be configured as different function. Please pay attention to the notes in the AM335x Data Sheet (1) concerning the configuration of these pins before integration / start-up of your carrier board / Starterkit. Please also take note of the latest AM335x errata (7).

3.2.1.4.1 Boot device SD card

The SD card boots from MMC0 of the AM335x. The following pins must be used for the boot process.

Table 7: Pins used for SD card boot

Signal	Dir.	TQMa335x	AM335x
MMC0_CLK	I/O	X1-41	G17
MMC0_CMD	I/O	X1-42	G18
MMC0_DAT3	I/O	X1-38	F17
MMC0_DAT2	I/O	X1-36	F18
MMC0_DAT1	I/O	X1-37	G15
MMC0_DAT0	I/O	X1-35	G16

3.2.1.4.2 Boot device eMMC

The eMMC boots from MMC1 of the AM335x. MMC1 supports eMMCs with a size of 4 Gbyte or greater.
The following pins are used for the boot process.

Table 8: Pins used for eMMC boot

Signal	Pin name	Remark
CLK	MMC1_CLK	–
CMD	MMC1_CMD	–
DAT0	MMC1_DAT0	4-bit boot
DAT1	MMC1_DAT1	
DAT2	MMC1_DAT2	
DAT3	MMC1_DAT3	

3.2.1.4.3 Boot device SPI NOR flash

The optional SPI NOR flash is connected to the following pins.

Table 9: Pins used for SPI NOR flash boot

Signal	Pin name
CS	SPI0_CS0#
MISO	SPI0_D0
MOSI	SPI0_D1
CLK	SPI0_SCLK

For other boot-configurations please refer to the AM335x Data Sheet (1).

3.2.2 Memory

3.2.2.1 DDR3L SDRAM

The TQMa335x is equipped with one DDR3L SDRAM chip with a data bus width of 16 bits.
The AM335x supports 303 to 400 MHz bus clock.
In the default BSP provided by TQ-Systems GmbH the memory is clocked with 400 MHz.
The following block diagram shows how the DDR3L SDRAM is connected to the AM335x.

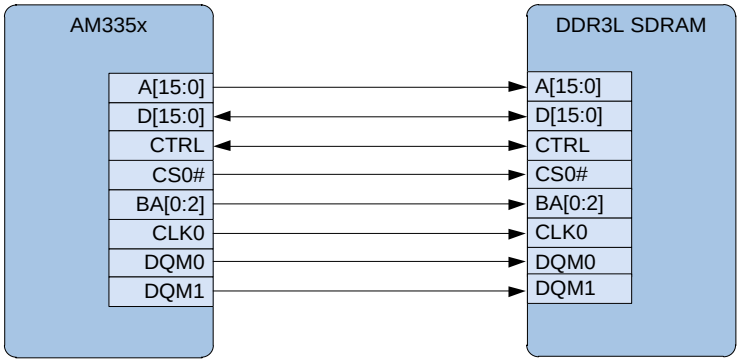


Illustration 4: Block diagram DDR3L SDRAM connection

The TQMa335x can be equipped with 256 Mbyte or 512 Mbyte of DDR3L SDRAM:

Table 10: DDR3L SDRAM

Placement option	Size
1 × DDR3L 128M16	256 Mbyte
1 × DDR3L 256M16	512 Mbyte

The SDRAM is mapped to the following address:

Table 11: DDR3 SDRAM address space

Start address	Size	Chip Select	Remark
0x8000_0000	0x4000_0000	CS0#	1 Gbyte

3.2.2.2 eMMC NAND flash

The eMMC NAND flash on the TQMa335x contains the boot loader and the application software.
The following block diagram shows how the eMMC flash is connected to the AM335x.

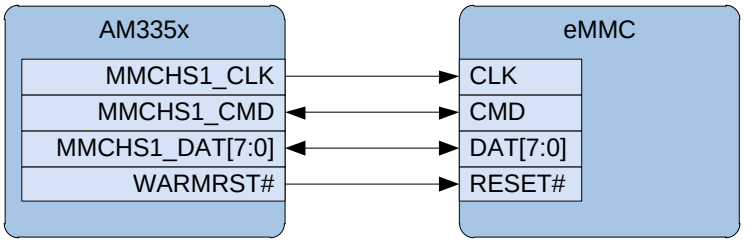


Illustration 5: Block diagram eMMC flash connection

3.2.2.3 SPI NOR flash

Optionally the TQMa335x can be equipped with an SPI NOR flash. It can, e.g., be used as a boot device or as a recovery device.
The following block diagram shows how the SPI NOR flash is connected to the AM335x.

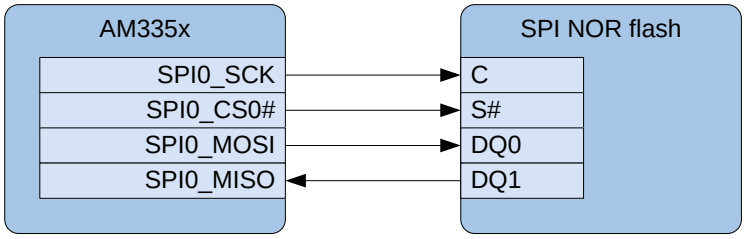


Illustration 6: Block diagram SPI NOR flash connection

The write protection pin of the SPI NOR flash is routed to the connector.

3.2.2.4 EEPROM

An optional serial EEPROM is available for permanent storage of e.g. TQMa335x characteristics or customers parameters.
The EEPROM is controlled via I²C bus 0 of the AM335x. The write protection pin (WP) of the EEPROM is not available.
The following block diagram shows how the EEPROM is connected to the AM335x.

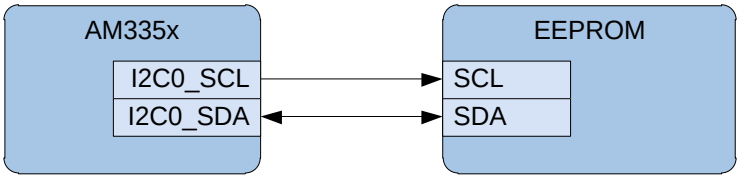


Illustration 7: Block diagram EEPROM connection

The following table shows the EEPROM used.

Table 12: EEPROM

Manufacturer	Part number	Size	Temperature range
STM	M24C64-WDW6TP	64 kbit	–40 °C to +85 °C

- The I²C address of the EEPROM is `0x50 / 101 0000b`.

In the EEPROM TQMa335x-specific data is stored. It is, however, not essential for the correct operation of the TQMa335x.
The data can be deleted or altered by the user.

In the following table the parameters stored in the EEPROM are shown.

Table 13: EEPROM TQMa335x-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
`0x00`	Variable	Variable	$32_{(10)}$	Binary	Hard Reset Configuration Word (HRCW), not used
`0x20`	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
`0x30`	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
`0x40`	Variable	Variable	$64_{(10)}$	ASCII	Order code
`0x80`	–	–	$8{,}064_{(10)}$	–	(Unused)

3.2.3 AM335x-RTC, PMIC-RTC

Both the AM335x and the PMIC on the TQMa335x provide an RTC.
On TQMa335x revision ≤ 0201 the clock output of the PMIC is routed to the RTC clock input of the AM335x.
Since TQMa335x revision 0202 the clock output of the PMIC is not routed to the RTC clock input of the AM335x anymore.
The PMIC is either supplied by V_{IN} (VCC3V3IN), or at the PMIC backup supply pin VBACKUP_PMIC, which is routed to X2-14.
The PMIC can charge an electrolytic capacitor or a SuperCap connected at X2-14.
Charging methods and electrical characteristics are to be taken from the PMIC User's Guide (6).
The typical current consumption of the PMIC_RTC is approximately 20 µA @ 3 V.
The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The 32.768 kHz crystal type FC-135 used on the TQMa335x has a standard frequency tolerance of ±20 ppm @ +25 °C.

Note: Current consumption	
	Long-term bridging with a coin cell is not possible due to the high current consumption of the PMIC-RTC. Depending on the use case a Li coin cell or a SuperCap can be used.

3.2.4 Optional I²C RTC

An RTC DS1339U-33 is available as an assembly option. During normal operation the RTC is supplied by V_{IN} (VCC3V3IN), in Backup-mode it can be supplied by a coin cell or a SuperCap connected at X2-13 (VBACKUP_RTC).
If the optional RTC is assembled, the 32.768 kHz crystal on the TQMa335x is connected to the RTC, but not to the PMIC.
The typical current consumption of the DS1339U-33 is approximately 400 nA @ 3 V.
The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The 32.768 kHz crystal type FC-135 used on the TQMa335x has a standard frequency tolerance of ±20 ppm @ +25 °C.

3.2.5 Temperature sensor

A temperature sensor provided on the TQMa335x.
The sensor is placed on the bottom side of the TQMa335x (D8 in Illustration 17).
The temperature sensor is connected to the I²C bus 0 of the AM335x.
The over-temperature detection output of the sensor is not connected to the AM335x.
The following block diagram shows how the temperature sensor is connected to the AM335x.

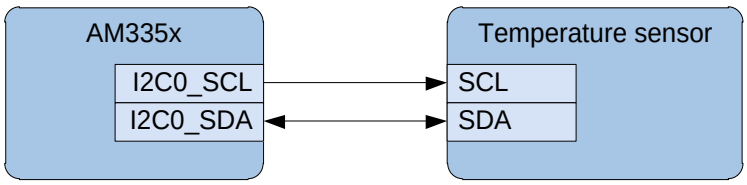


Illustration 8: Block diagram temperature sensor connection

The following table shows details the temperature sensor used.

Table 14: Temperature sensor

Manufacturer	Part number	Error	Temperature range	Remark
NXP	SE97BTP	Max. ±1 °C	–40 °C to +125 °C	11 bit ADC

➢ The I²C address of the temperature sensor is `0x1F / 001 1111b`.

3.2.6 Interfaces

3.2.6.1 Overview

The TQMa335x provides interfaces with primary function. These can be used simultaneously independent from its configuration. If a secondary function (e.g. MII0) is required, some primary functions may be omitted.
More information regarding availability and pinout can be found in the AM335x Data Sheet (1) and Reference Manual (3).

Table 15: Internal interfaces

Interface	Qty.	Function	Chapter	Remark
MMC1	1	Primary	3.2.2.2	eMMC, 8 bit
SPI0	1	Primary	3.2.2.3	ECSPI1 / SPI-NOR-Flash

Table 16: External interfaces

Interface	Qty.	Function	Chapter	Remark
AIN	8	Primary	3.2.6.14	AIN0 – AIN7
CLOCKOUT	2	Primary	3.2.6.22	General Purpose Clocks
CLOCKIN	1	–	–	–
CAN	2	Secondary	3.2.6.12	DCAN0 / DCAN1
JTAG / DEBUG	1	Primary	3.2.6.7	JTAG / EMU0 / EMU1
	3	Secondary		EMU2 / EMU3 / EMU4
ECAP	3	Secondary	–	ECAP0 – 2
ECAP_PRUSS	1	Secondary	–	–
ECAT_PRUSS	1	Secondary	–	–
EQEP	2	Primary	–	–
Gbit-Eth MAC	1	Primary	3.2.6.2	MII1
	1	Secondary	3.2.6.1	MII0
GLUE	2	Primary	–	XDMA_EVENT_INTR0 / 1
GPIO		Secondary	3.2.6.5	GPIO[0:2] (32 bit), GPIO3 (22 bit)
GPMC	1	Primary	3.2.6.3	12 address / 16 address/data
EMIF	1	Primary	3.2.2.1	DDR
I2C	1	Primary	3.2.6.13	I2C0
	2	Secondary		I2C1 / I2C2
LCD controller	1	Primary	3.2.6.10	RGB16
	1	Secondary		RGB24
MCASP	1	Primary	3.2.6.14	AUD3 / I2S
MCASP	3	Secondary		AUD4 / AUD5 / AUD6 | multiplexing has to be adapted
MDIO	1	Primary	–	–
MDIO_PRUSS	1	Secondary	–	–
MII_PRUSS	2	Secondary	3.2.6.2	MII0_PRUSS / MII1_PRUSS
MMC	1	Primary	3.2.6.4	MMC0 / SD card / 1/4 bit
	2	Secondary		MMC1 / eMMC / 1/4/8 bit
PRU_PRUSS	1	Secondary	–	16 bit interface
RTC	1	Primary	3.2.3	–
SPI	1	Primary	3.2.6.15	SPI0
	1	Secondary		SPI1
TIMER	4	Secondary	–	TIMER4 – 7
UART	2	Primary	3.2.6.16	UART0 / UART1
	4	Secondary	3.2.6.17	UART2 / UART3 / UART4 / UART5
UART_PRUSS	1	Secondary	–	UART_PRUSS0
USB	2	Primary	3.2.6.20	USB0_OTG / USB1_OTG
XTAL	2	Primary	–	XTALOSC0 / XTALOSC1

3.2.6.2 Gigabit Ethernet MAC

The AM335x provides a 10/100/1000 Mbit MAC Core.
Two Ethernet interfaces are routed to the connectors using the 3-port switch. The switch supports two MII, RMII and RGMII.
The following table shows the signals used.

Table 17: RGMII1

Signal	Pad	Dir.	TQMa335x	AM335x
RGMII1_TCLK	MII1_TX_CLK	I/O	X2-23	K18
RGMII1_RCLK	MII1_RX_CLK	I/O	X2-24	L18
RGMII1_TCTL	MII1_TX_EN	I/O	X2-27	J16
RGMII1_RCTL	MII1_RX_DV	I/O	X2-28	J17
RGMII1_TD0	MII1_TXD0	I/O	X2-29	K17
RGMII1_RD0	MII1_RXD0	I/O	X2-30	M16
RGMII1_TD1	MII1_TXD1	I/O	X2-31	K16
RGMII1_RD1	MII1_RXD1	I/O	X2-32	L15
RGMII1_TD2	MII1_TXD2	I/O	X2-33	K15
RGMII1_RD2	MII1_RXD2	I/O	X2-34	L16
RGMII1_TD3	MII1_TXD3	I/O	X2-35	J18
RGMII1_RD3	MII1_RXD3	I/O	X2-36	L17

Table 18: RGMII2

Signal	Pad	Dir.	TQMa335x	AM335x
RGMII2_TCLK	GPMC_A6	I/O	X2-45	U15
RGMII2_RCLK	GPMC_A7	I/O	X2-46	T15
RGMII2_TCTL	GPMC_A0	I/O	X2-49	R13
RGMII2_RCTL	GPMC_A1	I/O	X2-50	V14
RGMII2_TD0	GPMC_A5	I/O	X2-51	V15
RGMII2_RD0	GPMC_A11	I/O	X2-52	V17
RGMII2_TD1	GPMC_A4	I/O	X2-53	R14
RGMII2_RD1	GPMC_A10	I/O	X2-54	T16
RGMII2_TD2	GPMC_A3	I/O	X2-55	T14
RGMII2_RD2	GPMC_A9	I/O	X2-56	U16
RGMII2_TD3	GPMC_A2	I/O	X2-57	U14
RGMII2_RD3	GPMC_A8	I/O	X2-58	V16

3.2.6.3 GPMC [1]

The AM335x provides a General Purpose Memory Controller (GPMC). The GPMC signals are routed to the connectors as secondary function.

Note: Signal overlapping	
	There is an overlapping with an eMMC signal. GPMC-CLK is multiplexed with MMC1-CLK.

1: Currently not supported.

3.2.6.4 MMC / SD card

An SD card can be connected to the TQMa335x. The MMC0 controller is routed to the connectors for this purpose.
The MMC0 interface supports SD and SDIO as well.
The following table shows the signals used by the SD card interface.

Table 19: SD card signals

Signal	Pad	Dir.	TQMa335x	AM335x
MMC0_CLK	MMC0_CLK	I/O	X1-41	G17
MMC0_CMD	MMC0_CMD	I/O	X1-42	G18
MMC0_DAT3	MMC0_DAT3	I/O	X1-38	F17
MMC0_DAT2	MMC0_DAT2	I/O	X1-36	F18
MMC0_DAT1	MMC0_DAT1	I/O	X1-37	G15
MMC0_DAT0	MMC0_DAT0	I/O	X1-35	G16

The supported modes of operation, as well as MMC specifications are to be taken from the AM335x Data Sheet (1).
If desired port MMC0 can be configured as a boot device.
The control signals MMC0_CD# and MMC0_WP# are multiplexed with UART3 signal RxD and TxD.

3.2.6.5 GPIO

Besides their interface function most of the AM335x pins can also be used as GPIOs.
All these GPIOs are interrupt capable. Details are to be taken from the AM335x Data Sheet (1).
Moreover several pins marked as GPIO are already routed to the connectors.
The following table shows the signals, which can be used as GPIOs.

Table 20: GPIO signals

Signal	Pad	Dir.	TQMa335x	AM335x
GPIO1_28	GPMC_BE#1	I/O	X1-7	U18
GPIO1_29	GPMC_CS#0	I/O	X1-9	V6
GPIO2_0	GPMC_CS#3	I/O	X1-11	T13

The electrical characteristics of the GPIOs are to be taken from the respective Data Sheets provided by Texas Instruments (2), (3).

3.2.6.6 PWM

The AM335x provides several PWMs, which are routed to the connectors.
The following table shows the available PWM signals.

Table 21: PWM signals

Signal	Pad	Dir.	TQMa335x	AM335x
Timer4	GPMC_ADV#_ALE	I/O	X2-115	R7
Timer5	GPMC_BE#0_CLE	I/O	X2-117	T6
Timer6	GPMC_WE#	I/O	X2-116	U6
Timer7	GPMC_OE#_RE#	I/O	X2-118	T7

3.2.6.7 JTAG / DEBUG

The AM335x has two JTAG modes. The JTAG mode is defined by pins EMU0 and EMU1 during reset.
The following table shows the modes available and the mode selected on the TQMa335x:

Table 22: JTAG modes

EMU0	EMU1	Name	Remark
1	0	ICEPick	TAP only + WIR mode
1	1	ICEPick	TAP only (default mode)

The following table shows the signals used by the JTAG interface.

Table 23: JTAG signals

Signal	Pad	Dir.	TQMa335x	AM335x	Remark
TDO	TDO	O	X1-99	(A11)	22 Ω in series
TDI	TDI	I	X1-101	B11	–
TMS	TMS	I	X1-103	C11	–
TCK	TCK	I	X1-106	A12	–
TRST#	TRST#	I	X1-98	B10	–
EMU1	EMU1	I/O	X1-100	B14	–
EMU0	EMU0	I/O	X1-102	C14	–

3.2.6.8 Touch and analog inputs

The AM335x provides analog inputs including a touch interface. These inputs are routed to the connectors.
For the analog inputs a reference voltage of 1.8 V ±3 % is provided on the TQMa335x.
The following table shows the signals used by the analog interface.

Table 24: Touch signals

Signal	Pad	Dir.	TQMa335x	AM335x	Remark
AIN7	AIN7	A_{IN}	X1-71	C9	–
AIN3	AIN3	A_{IN}	X1-72	A7	On MBa335x: Y–
AIN6	AIN6	A_{IN}	X1-73	A8	–
AIN2	AIN2	A_{IN}	X1-74	B7	On MBa335x: Y+
AIN5	AIN5	A_{IN}	X1-77	B8	–
AIN1	AIN1	A_{IN}	X1-78	C7	On MBa335x: X–
AIN4	AIN4	A_{IN}	X1-79	C8	–
AIN0	AIN0	A_{IN}	X1-80	B6	On MBa335x: X+

Wake-up by touch is possible. The implementation and the selection of a certain power mode is software dependent.

3.2.6.9 External memory bus

Address and data bus, as well as AM335x memory interface control signals are routed to the connectors.
The interface is multiplexed with internal boot medium eMMC, LCD, RGMII2 and UART4.
However these pins are routed to the connectors.

3.2.6.10 LCD controller

The LCD controller of the AM335x supports up to 24-bit (RGB) with a resolution of up to WXGA (1366 × 768).
All necessary pins are routed to the connectors.
Information regarding supported displays and resolutions can be found in the AM335x Reference Manual (3).
The following table shows the signals used by the LCD controller.

Table 25: LCD signals

Signal	Pad	Dir.	TQMa335x	AM335x
LCD_MCLK	GPMC_CLK	I/O	X2-75	V12
LCD_HSYNC	LCD_HSYNC	I/O	X2-76	R5
LCD_VSYNC	LCD_VSYNC	I/O	X2-78	U5
LCD_PCLK	LCD_PCLK	I/O	X2-79	V5
LCD_AC_BIAS_EN	LCD_AC_BIAS_EN	I/O	X2-80	R6
LCD_DATA23	GPMC_AD8	I/O	X2-83	U10
LCD_DATA22	GPMC_AD9	I/O	X2-84	T10
LCD_DATA21	GPMC_AD10	I/O	X2-85	T11
LCD_DATA20	GPMC_AD11	I/O	X2-86	U12
LCD_DATA19	GPMC_AD12	I/O	X2-87	T12
LCD_DATA18	GPMC_AD13	I/O	X2-88	R12
LCD_DATA17	GPMC_AD14	I/O	X2-89	V13
LCD_DATA16	GPMC_AD15	I/O	X2-90	U13
LCD_DATA15	LCD_DATA15	I/O	X2-93	T5
LCD_DATA14	LCD_DATA14	I/O	X2-94	V4
LCD_DATA13	LCD_DATA13	I/O	X2-95	V3
LCD_DATA12	LCD_DATA12	I/O	X2-96	V2
LCD_DATA11	LCD_DATA11	I/O	X2-97	U4
LCD_DATA10	LCD_DATA10	I/O	X2-98	U3
LCD_DATA9	LCD_DATA9	I/O	X2-99	U2
LCD_DATA8	LCD_DATA8	I/O	X2-100	U1
LCD_DATA7	LCD_DATA7	I/O	X2-103	T4
LCD_DATA6	LCD_DATA6	I/O	X2-104	T3
LCD_DATA5	LCD_DATA5	I/O	X2-105	T2
LCD_DATA4	LCD_DATA4	I/O	X2-106	T1
LCD_DATA3	LCD_DATA3	I/O	X2-107	R4
LCD_DATA2	LCD_DATA2	I/O	X2-108	R3
LCD_DATA1	LCD_DATA1	I/O	X2-109	R2
LCD_DATA0	LCD_DATA0	I/O	X2-110	R1

3.2.6.11 Serial interfaces

The supported standards, transfer modes and rates of the following interfaces are to be taken from the AM335x Data Sheet (1).

3.2.6.12 CAN

The AM335x provides two integrated CAN controller. The signals of both CAN controllers are routed to the connectors.
The drivers have to be integrated on the carrier board.
The following table shows the signals used by the CAN interfaces.

Table 26: CAN1 / CAN2 signals

Signal	Pad	Dir.	TQMa335x	AM335x
DCAN0_TX	UART1_CTS#	I/O	X1-51	D18
DCAN0_RX	UART1_RTS#	I/O	X1-53	D17
DCAN1_TX	UART0_CTS#	I/O	X1-52	E18
DCAN1_RX	UART0_RTS#	I/O	X1-54	E17

3.2.6.13 I2C

The AM335x provides three I²C interfaces.
The I²C interfaces I2C0 and I2C1 are routed to the connectors and are available as a primary function.

The following table shows the signals used by the I2C buses.

Table 27: I2C0 and I2C1 signals

Signal	Pad	Dir.	TQMa335x	AM335x	Remark
I2C0_SDA	I2C0_SDA	I/O	X2-17	C17	3.3 kΩ PU to 3.3 V on TQMa335x
I2C0_SCL	I2C0_SCL	I/O	X2-19	C16	3.3 kΩ PU to 3.3 V on TQMa335x
I2C1_SDA	UART1_RXD	I/O	X1-91	D16	–
I2C1_SCL	UART1_TXD	I/O	X1-92	D15	–

The following devices are connected to the I2C0 bus on the TQMa335x:

Table 28: I2C0 addresses

Function	Device	Address
RTC (optional)	DS1339	0x68 / 110 1000b
EEPROM	M24C64	0x50 / 101 0000b
EEPROM SW PROTECT EEPROM Temperature sensor	SE97BTP SE97BTP SE97BTP	0x37 / 011 0111b 0x57 / 101 0111b 0x1F / 001 1111b
PMIC	TPS65910	0x12 / 001 0010b 0x2D / 010 1101b

If more devices have to be connected to the I2C0 bus on the carrier board, the maximum capacitive bus load accordingly to the I²C standard has to be adhered to. If required additional pull-ups should be provided on the carrier board at the bus.

3.2.6.14 I2S / AUDMUX

The Multichannel Audio Serial Port 0 (MCASP0) is routed to the connectors to connect an audio-codec via I²S.
The following table shows the signals used by the AUD3 interface.

Table 29: MCASP0 signals

Signal	Pad	Dir.	TQMa335x	AM335x
MCASP0_AXR0	MCASP0_AXR0	I/O	X1-61	D12
MCASP0_FSR	MCASP0_FSR	I/O	X1-62	C13
MCASP0_AXR1	MCASP0_AXR1	I/O	X1-63	D13
MCASP0_FSX	MCASP0_FSX	I/O	X1-64	B13
MCASP0_AXR2	MCASP0_AXR2	I/O	X1-65	C12
MCASP0_ACLKR	MCASP0_ACLKR	I/O	X1-66	B12
MCASP0_AXR3	MCASP0_AXR3	I/O	X1-67	A14
MCASP0_ACLKX	MCASP0_ACLKX	I/O	X1-68	A13

The Signal CCM_CLKO1 is used as I2C_MCLK in the BSP provided by TQ-Systems GmbH.
The MCASP-Interface supports I2S and other synchronous modes.
More information can be found in the AM335x Reference Manual (3).

3.2.6.15 SPI

The AM335x provides two MCSPIs (Multichannel Serial Port Interface). Both interfaces are routed to the connectors.
The following table shows the signals used by the SPI0 and SPI1 interfaces.

Table 30: SPI0 and SPI1 signals

Signal	Pad	Dir.	TQMa335x	AM335x	Remark
SPI1_MOSI	MII1_CRS	I/O	X1-45	H17	SPI1_D0
SPI1_MISO	MII1_RX_ER	I/O	X1-46	J15	SPI1_D1
SPI1_SCLK	MII1_COL	I/O	X1-47	H16	–
SPI1_CS0#	RMII1_REF_CLK	I/O	X1-48	H18	–
SPI0_MISO	SPI0_D0	I/O	X1-83	B17	MISO
SPI0_MOSI	SPI0_D1	I/O	X1-84	B16	MOSI
SPI0_SCLK	SPI0_SCLK	I/O	X1-85	A17	CLK
SPI0_CS0#	SPI0_CS0#	I/O	X1-86	A16	CS

Note: SPI0 as boot device	
	SPI0 can be configured as boot device. An SPI NOR flash can be assembled on the TQMa335x as an option.

3.2.6.16 UART

The AM335x provides five UART interfaces. UART0, UART3 and UART4 are routed to the connectors as primary functions. In the BSP provided by TQ-Systems GmbH UART4 is the serial console on the MBa335x.

3.2.6.17 UART0

The UART0 interface also provides handshake signals.

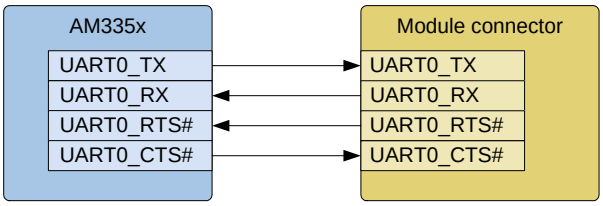


Illustration 9: Block diagram UART0 interface

The following table shows the signals used by the UART0 interface.

Table 31: UART0 signals

Signal	Pad	Dir.	TQMa335x	AM335x	Remark
UART0_RXD	UART0_RXD	I/O	X1-93	E15	–
UART0_TXD	UART0_TXD	I/O	X1-94	E16	–
DCAN1_TX	UART0_CTS#	I/O	X1-52	E18	Multiplexed as DCAN1_TX in TQ-BSP
DCAN1_RX	UART0_RTS#	I/O	X1-54	E17	Multiplexed as DCAN1_RX in TQ-BSP

UART0_CTS# and UART0_RTS# are only available if DCAN1 is not used.

3.2.6.18 UART3

The UART3 interface does not provide handshake signals. The UART3 signals are multiplexed with MMC0_CD# and MMC0_WP#.

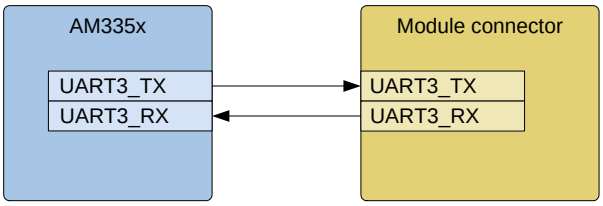


Illustration 10: Block diagram UART3 interface

The following table shows the signals used by the UART3 interface.

Table 32: UART3 signals

Signal	Pad	Dir.	TQMa335x	AM335x	Remark
UART3_RXD	SPI0_CS1#	I/O	X1-33	C15	MMC0_CD#
UART3_TXD	ECAP0_IN_PWM0_OUT	I/O	X1-34	C18	MMC0_WP#

3.2.6.19 UART4

The UART4 interface does not provide handshake signals.

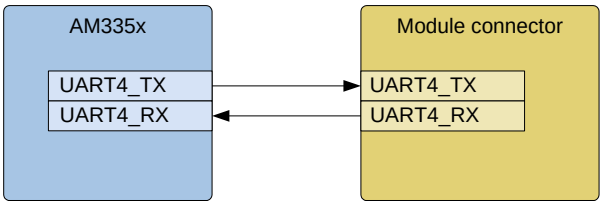


Illustration 11: Block diagram UART4 interface

The following table shows the signals used by the UART4 interface.

Table 33: UART4 signals

Signal	Pad	Dir.	TQMa335x	AM335x
UART4_RXD	GPMC_WAIT0	I/O	X2-41	T17
UART4_TXD	GPMC_WP#	I/O	X2-42	U17

3.2.6.20 USB

The AM335x provides two USB OTG cores with integrated High Speed PHYs.
All signals are routed to the connectors as primary functions.
The following table shows the signals used by the USB_H1 interface.

Table 34: USB_H1 signals

Signal	Pad	Dir.	TQMa335x	AM335x
USB0_DP	USB0_DP	I/O	X1-18	N17
USB0_DM	USB0_DM	I/O	X1-20	N18
USB0_CE	USB0_CE	O	X1-24	M15
USB0_ID	USB0_ID	I	X1-26	P16
USB0_VBUS	USB0_VBUS	P	X1-28	P15
USB0_DRVBUS	USB0_DRVBUS	O	X1-30	F16
USB1_DP	USB1_DP	I/O	X1-17	R17
USB1_DM	USB1_DM	I/O	X1-19	R18
USB1_CE	USB1_CE	O	X1-23	P18
USB1_ID	USB1_ID	I	X1-25	P17
USB1_VBUS	USB1_VBUS	P	X1-27	T18
USB1_DRVBUS	USB1_DRVBUS	O	X1-29	F15

3.2.6.21 EXTINT#

The signal EXTINT# of the AM335x is routed to the connector.

Table 35: EXTINT# signal

Signal	Pad	Dir.	TQMa335x	AM335x	Remark
EXTINT#	EXTINT#	I	X1-14	B18	Routed to NMI# of AM335x

3.2.6.22 Clock-out

The AM335x provides two clock-out signals, which are routed to the connectors.
The following table shows the signals used for clock-out.

Table 36: Clock-out signals

Signal	Pad	Dir.	TQMa335x	AM335x
Clkout1	XDMA_EVENT_INTR0	I/O	X1-58	A15
Clkout2	XDMA_EVENT_INTR1	I/O	X1-57	D14

3.2.7 Reset

The TQMa335x provides Reset inputs, and Reset outputs at the connectors. An orange LED lights up when the TQMa335x is in reset. The following block diagram shows the wiring of the reset signals.

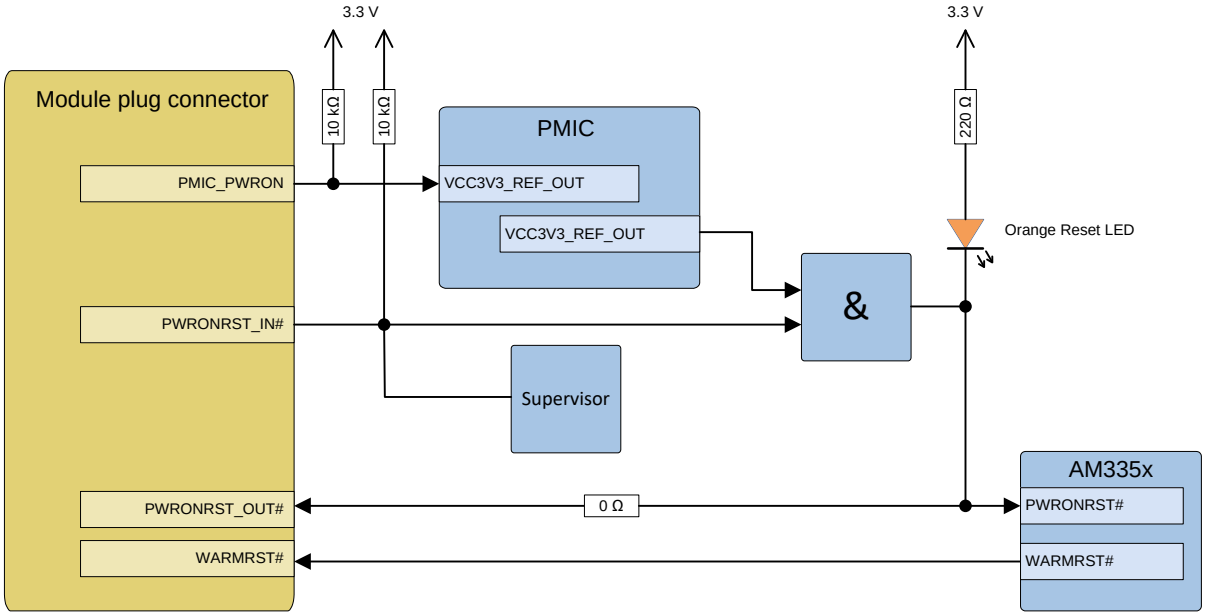


Illustration 12: Block diagram Reset

The following table describes the reset signals, which are routed to the connectors.

Table 37: Reset signals

Signal	TQMa335x	Dir.	Remark
PWRONRST_IN#	X1-10	I_{OD}	• Reset input PWRONRST (Power-On Reset) of the AM335x • Generates Cold-Reset at the AM335x • Connect to open-drain output only! • Low-active signal
PWRONRST_OUT#	X1-12	O	• Reset output RESETBMCU of the PMIC • Can be used to reset external periphery • Open drain, requires Pull-Up on carrier board (max. 3.3 V) • Low-active signal
WARMRST#	X1-97	O_{PU}	• Warm-Reset# of the AM335x • 10 kΩ PU to 3.3 V on the TQMa335x • Low-active signal

The reset output of the supervisor used on the TQMa335x can be connected to the POR_B input of the AM335x as a placement option.

3.2.8 WDOG

The AM335x provides a Watchdog Timer.
If the Watchdog-Timer is active and not reset within the specified time, a reset is signalled to the PRCM.
The PRCM then triggers a Warm-Reset. More information can be found in the AM335x Reference Manual (3).

3.2.9 Power supply

3.2.9.1 Main power supply

The TQMa335x input voltage is 3.3 V ±3 %. All IO voltages have a fixed supply voltage of 3.3 V.

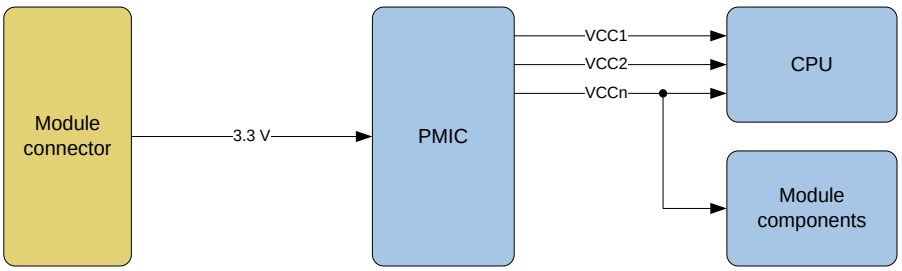


Illustration 13: Block diagram power supply

3.2.9.2 Overview TQMa335x supply

The given current consumption has to be seen as an approximate value.
To estimate the power consumption of the system the Texas Instruments Application Note AM335x Power Consumption Summary should be taken note of as the current consumption of the TQMa335x strongly depends on the application, the mode of operation and the operating system.
The following table shows some technical parameters of the TQMa335x supply and power consumption.

Table 38: Parameter TQMa335x supply

Parameter	Value typ.	Remark
Supply voltage V_{IN}	3.3 V	±3 % for TQMa335x without extended voltage supervision
Supply voltage V_{IN}	3.3 V	±2 % for TQMa335x with extended voltage supervision
Power consumption Linux (idle)	~ 1.2 W	AM335x 800 MHz / BSP without power management
Power consumption Linux (100 %)	~ 1.8 W	AM335x 800 MHz / BSP without power management
Power consumption standby	~ 210 mW	AM335x 800 MHz / BSP without power management

3.2.9.3 Adaptive Voltage Scaling (AVS)

The combination of AM335x and PMIC TPS65910A31 supports Adaptive Voltage Scaling (AVS) based on Smart Reflex.
The function is very limited due to several errata!

3.2.9.4 Voltage supervision

The TQMa335x is available with several voltage supervision options. On the primarily manufactured version of the TQMa335x, a MAX803 with a trigger level of 3.08 V monitors the supply voltage. Below 3.08 V a PORESET# is triggered at the AM335x.
On a second version of the TQMa335x all voltages, except the DVS-capable voltages VDDS_MPU and VDDS_CORE are monitored using precision comparators. If one of these voltages falls below the permitted level a PORESET# is triggered at the AM335x.
On a third version of the TQMa335x undervoltage and overvoltage of the supply voltages are monitored. If one of these voltages fall below or exceed the permitted level a PORESET# is triggered at the AM335x.

3.2.9.5 TQMa335x / carrier board Power-Up sequence

Since the AM335x is very sensitive to cross-supply it has to be ensured that the components on the carrier board are not supplied by the IO-voltages (VDDSHV3V3) during power-up.

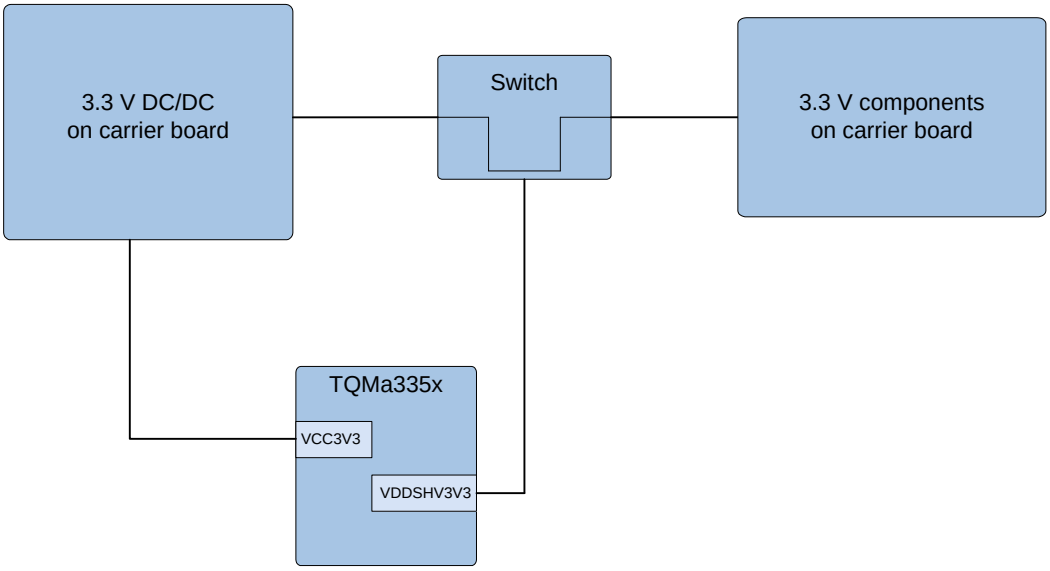


Illustration 14: Block diagram power supply carrier board

With the procedure described above it is certified that the pull-ups on the carrier board are already supplied with voltage when the boot-configuration pins are read.

Attention: Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the power-up sequence is indicated by a high level of signal VDDSHV3V3.

3.2.9.6 Start-up procedure

When tdONPWRHOLD (1 second) is elapsed, the pin PWRHOLD has to be set to “1“, else the PMIC switches the voltages off again.
PWRHOLD is connected to PMIC_POWER_EN. The function PMIC_POWER_EN is set in register RTC_PMIC of the AM335x.
It is activated by default. Because of that the Pin PMIC_POWER_EN is permanently high.
An activation can be necessary to use Wake-up events of the RTC-only-Mode.

3.2.9.7 Power-down procedure

The AM335x demands, that the voltage difference between VDDSHV3V3 and VDDS is never higher than 2 V.
The PMIC ensures this in the power-down procedure.

3.2.9.8 PMIC configuration

The PMIC can be configured via I2C0. The EEPROM in the PMIC is not writable!
During Power-up the PMIC always starts the default sequence stored in the EEPROM.
The PMIC can only be reset by a power-cycle. A software reset is not sufficient to reset the PMIC.

3.2.10 Power-Modes

The following modes are supported by the hardware in combination with AM335x, PMIC, RTC and supply.

3.2.10.1 RTC backup

In this mode the controller is switched off. Only the RTC is buffered by the battery. Wakeup features are not available. Depending on the placement option “external RTC” this results in the following conditions:

Table 39: External RTC

External RTC	Remark
PMIC	Is in OFF mode
Supply	VCC_MAIN <2.5 V; VBACKUP = 1.3 V to 3.7 V
VDDS_RTC	When supplied via LDO: Supply off
Current consumption	Approximately 400 nA

Table 40: PMIC RTC

RTC in PMIC	Remark
PMIC	Is in backup mode
BBCHEN=0	Battery charging has to be deactivated
Supply	VCC_MAIN <2.5 V; VBACKUP = 2.3 V to 3.0 V
VDDS_RTC	When supplied via LDO: Supply off
Current consumption	Approximately 20 µA

3.2.10.2 AM335x RTC-Only

In this mode the wakeup source PMIC_POWER_EN of the AM335x is supported.

To use the wakeup events the signal PMIC_POWER_EN has to be connected to the respective PMIC pin and VDDS_RTC has to be supplied with 1.8 V DC.

Table 41: AM335x RTC-Only

Conditions	Remark
PMIC	• Is in SLEEP MODE • Switch off voltages: (SLEEP_KEEP_LDO_ON, SLEEP_KEEP_RES_ON) • CLKOUT has to be activated (SLEEP_KEEP_RES:ON)
External RTC	The oscillator in the PMIC has to be activated, if the external RTC is assembled
Supply	VCC_MAIN > 3.0 V
PMIC_POWER_EN	Connected with PWRHOLD
VDDS_RTC	Supplied by PMIC

3.2.10.3 AM335x DEEP-SLEEP0-2, Standby

In this mode the following wakeup sources of the AM335x are supported.

- GPIO0
- Dmtimer1_1ms
- Both USB
- Touchscreen and ADC monitor functions
- UART0
- I2C0

Table 42: AM335x DEEP-SLEEP0-2, Standby

Conditions	Remark
PMIC	• Is in SLEEP MODE • Switch on voltages: (SLEEP_KEEP_LDO_ON, SLEEP_KEEP_RES_ON) • CLKOUT has to be activated (SLEEP_KEEP_RES:ON)
External RTC	The oscillator in the PMIC has to be activated, if the external RTC is assembled
Supply	VCC_MAIN = 3.3 V
PMIC_POWER_EN	Connected with PWRHOLD
VDDS_RTC	Supplied by PMIC

3.2.10.4 AM335x Active Mode

The default mode of operation is the Active Mode.

Table 43: AM335x Active Mode

Conditions	Remark
PMIC	Is in Active Mode
External RTC	The oscillator in the PMIC has to be activated, if external RTC is assembled
Supply	VCC_MAIN = 3.3 V
PMIC_POWER_EN	Connected with PWRHOLD
VDDS_RTC	Supplied by PMIC

3.2.11 TQMa335x supply on carrier board

It is recommended to buffer the supply for the TQMa335x on the carrier board with 3 × 100 nF and 3 × 100 µF.
The capacitors should be as close as possible to connector X2 pins 1 to 6.

3.2.12 Battery input VBACKUP

An additional VBACKUP pin is provided. The permitted voltage input range is 2.3 V to 3 V DC.

3.3 TQMa335x interface

3.3.1 Pinout

The multiple pin configurations of all AM335x-internal function units must be taken note of.
The pinout listed in Table 44 and Table 45 refer to the corresponding BSP provided by TQ-Systems GmbH.
The electrical and pin characteristics are to be taken from the AM335x (1), (3) and PMIC Data Sheets (6).

3.3.2 Pinout connector X1

Table 44: Pinout connector X1

AM335x	Dir.	Pad	Group	Signal	Pin		Signal	Group	Pad	Dir.	AM335x
–	P	–	Power	DGND	1	2	DGND	Power	–	P	–
–	I	TPS65910A31 pin SLEEP	PMIC	PMIC_SLEEP	3	4	PMIC_PWRON	PMIC	TPS65910A31 pin PWRON	I	–
–	O	DS1339u pin SQW/INT#	CTRL	RTC_INT#	5	6	PMIC_INT1	PMIC	TPS65910A31 pin INT1	O	–
U18	I/O	GPMC_BE#1	GPIO	GPIO1_28	7	8	TEMP_OS#	TEMP	SE97BTP pin EVENT#	O	–
V6	I/O	GPMC_CS#0	GPIO	GPIO1_29	9	10	PWRONRST_IN#	CTRL	PWRONRST# [2]	I	–
T13	I/O	GPMC_CS#3	GPIO	GPIO2_0	11	12	PWRONRST_OUT#	CTRL	PWRONRST# [3]	O	–
C5	I	EXT_WAKEUP	CTRL	EXT_WAKEUP	13	14	EXTINT# (NMI#)	CTRL	EXTINT#	I	B18
–	P	–	Power	DGND	15	16	DGND	Power	–	P	–
R17	I/O	USB1_DP	USB1	USB1_DP	17	18	USB0_DP	USB0	USB0_DP	I/O	N17
R18	I/O	USB1_DM	USB1	USB1_DM	19	20	USB0_DM	USB0	USB0_DM	I/O	N18
–	P	–	Power	DGND	21	22	DGND	Power	–	P	–
P18	O	USB1_CE	USB1	USB1_CE	23	24	USB0_CE	USB0	USB0_CE	O	M15
P17	I	USB1_ID	USB1	USB1_ID	25	26	USB0_ID	USB0	USB0_ID	I	P16
T18	P	USB1_VBUS	USB1	USB1_VBUS	27	28	USB0_VBUS	USB0	USB0_VBUS	P	P15
F15	O	USB1_DRVBUS	USB1	USB1_DRVBUS	29	30	USB0_DRVBUS	USB0	USB0_DRVBUS	O	F16
–	P	–	Power	DGND	31	32	DGND	Power	–	P	–
C15	I/O	SPI0_CS1#	UART	UART3_RXD	33	34	UART3_TXD	UART	ECAP0_IN_PWM0_OUT	I/O	C18
G16	I/O	MMC0_DAT0	MMC	MMC0_DAT0	35	36	MMC0_DAT2	MMC	MMC0_DAT2	I/O	F18
G15	I/O	MMC0_DAT1	MMC	MMC0_DAT1	37	38	MMC0_DAT3	MMC	MMC0_DAT3	I/O	F17
–	P	–	Power	DGND	39	40	DGND	Power	–	P	–
G17	I/O	MMC0_CLK	MMC	MMC0_CLK	41	42	MMC0_CMD	MMC	MMC0_CMD	I/O	G18
–	P	–	Power	DGND	43	44	DGND	Power	–	P	–
H17	I/O	RMII1_CRS	SPI	SPI1_D0	45	46	SPI1_D1	SPI	RMII1_RX_ER	I/O	J15
H16	I/O	RMII1_COL	SPI	SPI1_SCLK	47	48	SPI1_CS0#	SPI	RMII1_REF_CLK	I/O	H18
–	P	–	Power	DGND	49	50	DGND	Power	–	P	–
D18	I/O	UART1_CTS#	UART	DCAN0_TX	51	52	DCAN1_TX	UART	UART0_CTS#	I/O	E18
D17	I/O	UART1_RTS#	UART	DCAN0_RX	53	54	DCAN1_RX	UART	UART0_RTS#	I/O	E17
–	P	–	Power	DGND	55	56	DGND	Power	–	P	–
D14	I/O	XDMA_EVENT_INTR1	CLK	TCLKIN	57	58	CLKOUT1	CLK	XDMA_EVENT_INTR0	I/O	A15
–	P	–	Power	DGND	59	60	DGND	Power	–	P	–
D12	I/O	MCASP0_AXR0	MCASP0	MCASP0_AXR0	61	62	MCASP0_FSR	MCASP0	MCASP0_FSR	I/O	C13
D13	I/O	MCASP0_AXR1	MCASP0	MCASP0_AXR1	63	64	MCASP0_FSX	MCASP0	MCASP0_FSX	I/O	B13
C12	I/O	MCASP0_AXR2	MCASP0	MCASP0_AXR2	65	66	MCASP0_ACLKR	MCASP0	MCASP0_ACLKR	I/O	B12
A14	I/O	MCASP0_AXR3	MCASP0	MCASP0_AXR3	67	68	MCASP0_ACLKX	MCASP0	MCASP0_ACLKX	I/O	A13
–	P	–	Power	DGND	69	70	DGND	Power	–	P	–
C9	A	AIN7	AIN	AIN7	71	72	AIN3	AIN	AIN3	A	A7
A8	A	AIN6	AIN	AIN6	73	74	AIN2	AIN	AIN2	A	B7
–	P	–	Power	DGND	75	76	DGND	Power	–	P	–
B8	A	AIN5	AIN	AIN5	77	78	AIN1	AIN	AIN1	A	C7
C8	A	AIN4	AIN	AIN4	79	80	AIN0	AIN	AIN0	A	B6
–	P	–	Power	DGND	81	82	DGND	Power	–	P	–
B17	I/O	SPI0_D0	SPI	SPI0_D0	83	84	SPI0_D1	SPI	SPI0_D1	I/O	B16
A17	I/O	SPI0_SCLK	SPI	SPI0_SCLK	85	86	SPI0_CS0#	SPI	SPI0_CS0#	I/O	A16
–	P	–	Power	DGND	87	88	DGND	Power	–	P	–
–	–	–	RFU	RFU	89	90	RFU	RFU	–	–	–
D16	I/O	UART1_RXD	I2C	I2C1_SDA	91	92	I2C1_SCL	I2C	UART1_TXD	I/O	D15
E15	I/O	UART0_RXD	UART	UART0_RXD	93	94	UART0_TXD	UART	UART0_TXD	I/O	E16
–	P	–	Power	DGND	95	96	DGND	Power		P	–
A10	I/O	WARMRST#	CTRL	WARMRST#	97	98	TRST#	JTAG	TRST#	I	B10
A11	O	TDO	JTAG	TDO	99	100	EMU1	EMU	EMU1	I/O	B14
B11	I	TDI	JTAG	TDI	101	102	EMU0	EMU	EMU0	I/O	C14
C11	I	TMS	JTAG	TMS	103	104	DGND	Power	–	P	–
–	P	–	Power	DGND	105	106	TCK	JTAG	TCK	I	A12
–	O	Test voltage	VDDS	VDDS-DDR_TEST	107	108	DGND	Power	–	P	–
–	O	Test voltage	VDDS	VDDS_TEST	109	110	RFU	RFU	–		–
–	O	Test voltage	VDDS	VDD-PLL_TEST	111	112	RFU	RFU	–		–
–	O	Test voltage	VDDS	VDD-USB_TEST	113	114	VDDS-CORE_TEST	VDDS	Test voltage	O	–
–	O	Test voltage	VDDS	VDDA-ADC_TEST	115	116	VDDS-MPU_TEST	VDDS	Test voltage	O	–
–	O	Test voltage	VDDS	VDDS-RTC_TEST	117	118	DGND	Power	–	P	–
–	P	–	Power	DGND	119	120	DGND	Power	–	P	–

2: Input on TQMa335x !
3: Output on TQMa335x !

3.3.3 Pinout connector X2

Table 45: Pinout connector X2

AM335x	Dir.	Pad	Group	Signal	Pin		Signal	Group	Pad	Dir.	AM335x
–	P	–	Power	VCC3V3	1	2	VCC3V3	Power	–	P	–
–	P	–	Power	VCC3V3	3	4	VCC3V3	Power	–	P	–
–	P	–	Power	VCC3V3	5	6	VCC3V3	Power	–	P	–
–	P	–	Power	DGND	7	8	DGND	Power	–	P	–
–	P	–	Power	DGND	9	10	DGND	Power	–	P	–
–	P	–	Power	DGND	11	12	DGND	Power	–	P	–
–	P	Backup voltage for RTC	VBACKUP	VBACKUP_RTC	13	14	VBACKUP_PMIC	VBACKUP	Backup voltage for PMIC	P	–
–	P	–	Power	DGND	15	16	DGND	Power	–	P	–
C17	I/O	I2C0_SDA	I2C	I2C0_SDA	17	18	VDDSHV3V3	VDDS	Test voltage	O	
C16	I/O	I2C0_SCL	I2C	I2C0_SCL	19	20	RFU	RFU	–		
–	P	–	Power	DGND	21	22	DGND	Power	–	P	–
K18	I/O	MII1_TX_CLK	RGMII	RGMII1_TCLK	23	24	RGMII1_RCLK	RGMII	MII1_RX_CLK	I/O	L18
–	P	–	Power	DGND	25	26	DGND	Power	–	P	–
J16	I/O	MII1_TX_EN	RGMII	RGMII1_TCTL	27	28	RGMII1_RCTL	RGMII	MII1_RX_DV	I/O	J17
K17	I/O	MII1_TXD0	RGMII	RGMII1_TD0	29	30	RGMII1_RD0	RGMII	MII1_RXD0	I/O	M16
K16	I/O	MII1_TXD1	RGMII	RGMII1_TD1	31	32	RGMII1_RD1	RGMII	MII1_RXD1	I/O	L15
K15	I/O	MII1_TXD2	RGMII	RGMII1_TD2	33	34	RGMII1_RD2	RGMII	MII1_RXD2	I/O	L16
J18	I/O	MII1_TXD3	RGMII	RGMII1_TD3	35	36	RGMII1_RD3	RGMII	MII1_RXD3	I/O	L17
–	P	–	Power	DGND	37	38	DGND	Power	–	P	–
M18	I/O	MDC	MD	MDC	39	40	MDIO	MD	MDIO	I/O	M17
T17	I/O	GPMC_WAIT0	UART	UART4_RXD	41	42	UART4_TXD	UART	GPMC_WP#	I/O	U17
–	P	–	Power	DGND	43	44	DGND	Power	–	P	–
U15	I/O	GPMC_A6	RGMII	RGMII2_TCLK	45	46	RGMII2_RCLK	RGMII	GPMC_A7	I/O	T15
–	P	–	Power	DGND	47	48	DGND	Power	–	P	–
R13	I/O	GPMC_A0	RGMII	RGMII2_TCTL	49	50	RGMII2_RCTL	RGMII	GPMC_A1	I/O	V14
V15	I/O	GPMC_A5	RGMII	RGMII2_TD0	51	52	RGMII2_RD0	RGMII	GPMC_A11	I/O	V17
R14	I/O	GPMC_A4	RGMII	RGMII2_TD1	53	54	RGMII2_RD1	RGMII	GPMC_A10	I/O	T16
T14	I/O	GPMC_A3	RGMII	RGMII2_TD2	55	56	RGMII2_RD2	RGMII	GPMC_A9	I/O	U16
U14	I/O	GPMC_A2	RGMII	RGMII2_TD3	57	58	RGMII2_RD3	RGMII	GPMC_A8	I/O	V16
–	P	–	Power	DGND	59	60	DGND	Power	–	P	–
U7	I/O	GPMC_AD0	MMC	MMC1_DAT0	61	62	MMC1_DAT4	MMC	GPMC_AD4	I/O	U8
V7	I/O	GPMC_AD1	MMC	MMC1_DAT1	63	64	MMC1_DAT5	MMC	GPMC_AD5	I/O	V8
R8	I/O	GPMC_AD2	MMC	MMC1_DAT2	65	66	MMC1_DAT6	MMC	GPMC_AD6	I/O	R9
T8	I/O	GPMC_AD3	MMC	MMC1_DAT3	67	68	MMC1_DAT7	MMC	GPMC_AD7	I/O	T9
–	P	–	Power	DGND	69	70	DGND	Power	–	P	–
V9	I/O	GPMC_CS#2	MMC	MMC1_CMD	71	72	MMC1_CLK	MMC	GPMC_CS#1	I/O	U9
–	P	–	Power	DGND	73	74	DGND	Power	–	P	–
V12	I/O	GPMC_CLK	LCD	LCD_MCLK	75	76	LCD_HSYNC	LCD	LCD_HSYNC	I/O	R5
–	P	–	Power	DGND	77	78	LCD_VSYNC	LCD	LCD_VSYNC	I/O	U5
V5	I/O	LCD_PCLK	LCD	LCD_PCLK	79	80	LCD_AC_BIAS_EN	LCD	LCD_AC_BIAS_EN	I/O	R6
–	P	–	Power	DGND	81	82	DGND	Power	–	P	–
U10	I/O	GPMC_AD8	LCD	LCD_DATA23	83	84	LCD_DATA22	LCD	GPMC_AD9	I/O	T10
T11	I/O	GPMC_AD10	LCD	LCD_DATA21	85	86	LCD_DATA20	LCD	GPMC_AD11	I/O	U12
T12	I/O	GPMC_AD12	LCD	LCD_DATA19	87	88	LCD_DATA18	LCD	GPMC_AD13	I/O	R12
V13	I/O	GPMC_AD14	LCD	LCD_DATA17	89	90	LCD_DATA16	LCD	GPMC_AD15	I/O	U13
–	P	–	Power	DGND	91	92	DGND	Power	–	P	–
T5	I/O	LCD_DATA15	LCD	LCD_DATA15	93	94	LCD_DATA14	LCD	LCD_DATA14	I/O	V4
V3	I/O	LCD_DATA13	LCD	LCD_DATA13	95	96	LCD_DATA12	LCD	LCD_DATA12	I/O	V2
U4	I/O	LCD_DATA11	LCD	LCD_DATA11	97	98	LCD_DATA10	LCD	LCD_DATA10	I/O	U3
U2	I/O	LCD_DATA9	LCD	LCD_DATA9	99	100	LCD_DATA8	LCD	LCD_DATA8	I/O	U1
–	P	–	Power	DGND	101	102	DGND	Power	–	P	–
T4	I/O	LCD_DATA7	LCD	LCD_DATA7	103	104	LCD_DATA6	LCD	LCD_DATA6	I/O	T3
T2	I/O	LCD_DATA5	LCD	LCD_DATA5	105	106	LCD_DATA4	LCD	LCD_DATA4	I/O	T1
R4	I/O	LCD_DATA3	LCD	LCD_DATA3	107	108	LCD_DATA2	LCD	LCD_DATA2	I/O	R3
R2	I/O	LCD_DATA1	LCD	LCD_DATA1	109	110	LCD_DATA0	LCD	LCD_DATA0	I/O	R1
–	P	–	Power	DGND	111	112	DGND	Power	–	P	–
		–	RFU	RFU	113	114	RFU	RFU	–		
R7	I/O	GPMC_ADV#_ALE	Timer	TIMER4	115	116	TIMER6	Timer	GPMC_WE#	I/O	U6
T6	I/O	GPMC_BE#0_CLE	Timer	TIMER5	117	118	TIMER7	Timer	GPMC_OE#_RE#	I/O	T7
–	P	–	Power	DGND	119	120	DGND	Power	–	P	–

4. MECHANICS

4.1 TQMa335x connectors

The TQMa335x is connected to the carrier board with 240 pins on two connectors.

The following table shows details of the connector used.

Table 46: Connector assembled on TQMa335x

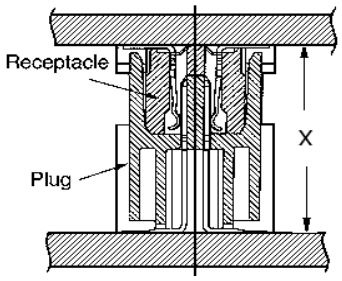
Manufacturer	Part number	Description
TE Connectivity	120-pin: 5-353999-5	• 0.8 mm pitch • Plating: Gold (30µ") 0.76 µm • –40 °C to +125 °C

The TQMa335x is held in the mating connectors with a retention force of approximately 24 N.
To avoid damaging the TQMa335x connectors as well as the carrier board connectors while removing the TQMa335x the use of the extraction tool MOZIA335 is strongly recommended. See chapter 4.8 for further information.

Attention: Component placement on the carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa335x for the extraction tool MOZIA335.

The following table shows some suitable mating connectors for the carrier board.

Table 47: Suitable carrier board mating connectors

Manufacturer	Part number	Remark	Stack height (X)	
TE connectivity	5177986-5	On MBa335x	5 mm	
	1-5177986-5	–	6 mm	
	2-5177986-5	–	7 mm	
	3-5177986-5	–	8 mm	

4.2 Dimensions

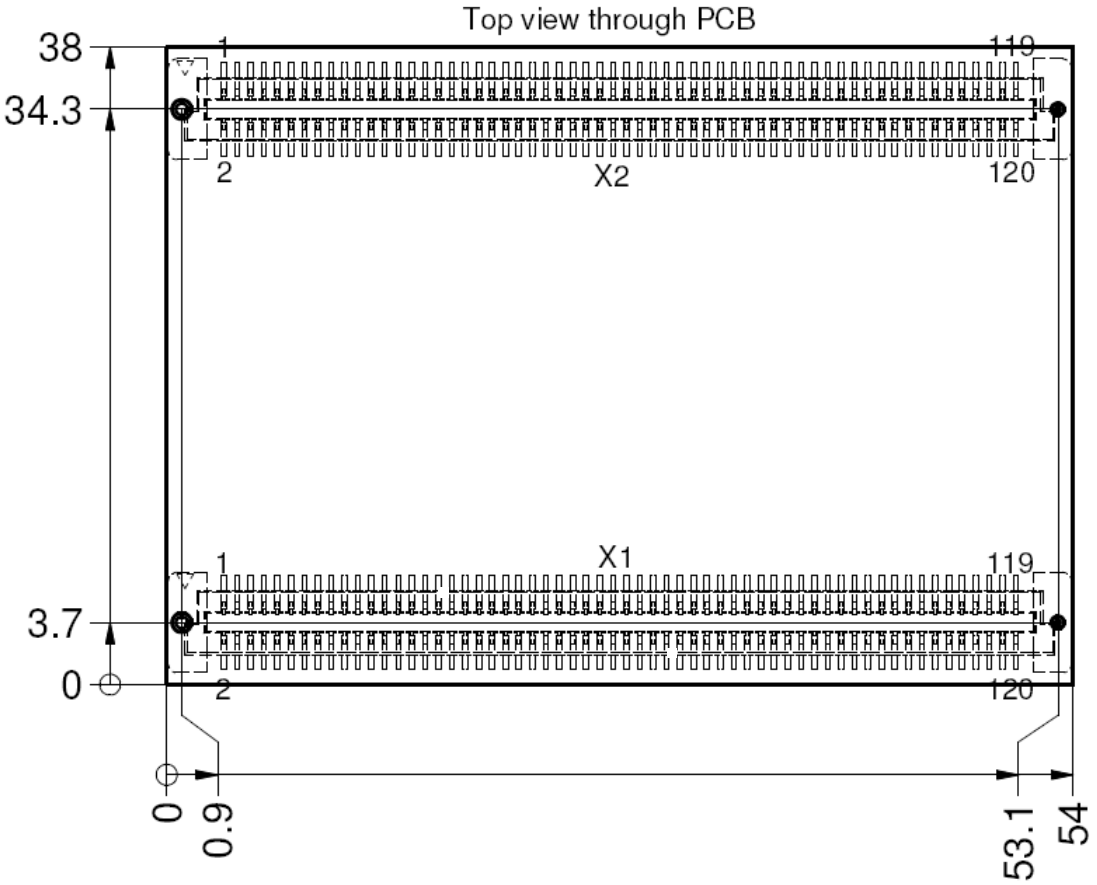


Illustration 15: TQMa335x dimensions, **top view through TQMa335x**

4.3 TQMa335x component placement

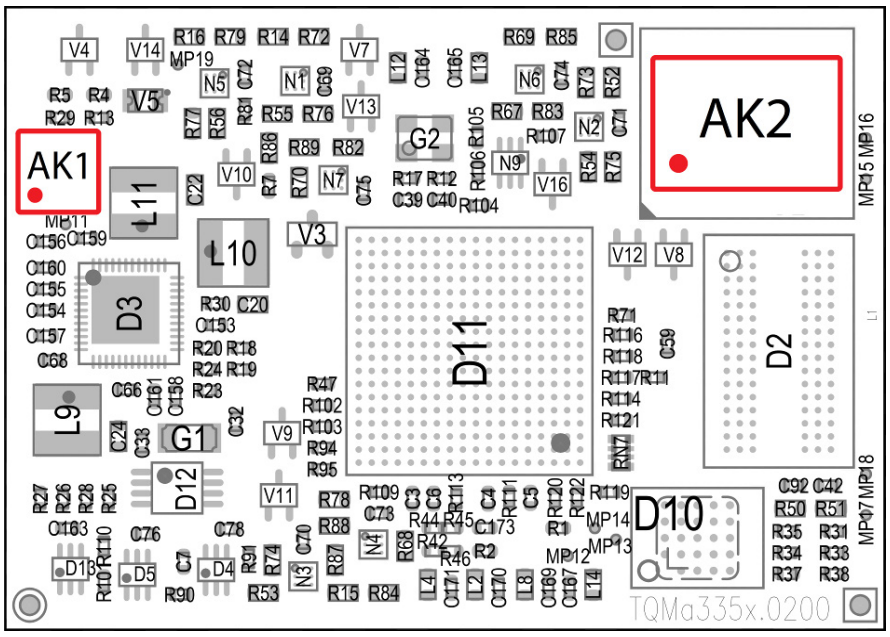


Illustration 16: TQMa335x, component placement top

The labels on the TQMa335x show the following information:

Table 48: Labels on TQMa335x

Label	Text
AK1	TQMa335x serial number
AK2	TQMa335x version and revision, tests performed

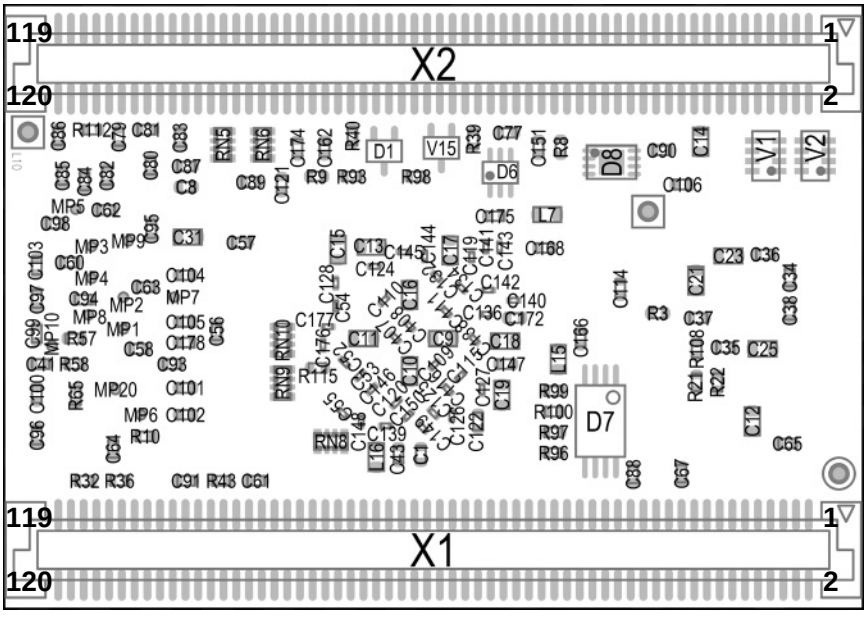


Illustration 17: TQMa335x, component placement bottom

4.4 Adaptation to the environment

The TQMa335x has overall dimensions (length × width × height) of 54 × 38 × 6.6 mm³.
The TQMa335x has a maximum height above the carrier board of approximately 8 mm.
The TQMa335x weighs approximately 12 grams.

4.5 Protection against external effects

As an embedded module the TQMa335x is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa335x, a maximum of 2 W have to be dissipated.
The power dissipation originates primarily in the AM335x and the DDR3L SDRAM.
The power dissipation mainly depends on the software used and can vary according to the application.
It is the responsibility of the customer to define a suitable cooling method for his use case.
In most cases passive cooling should be sufficient.
For further information see Texas Instruments Application Notes (4), (5).

Attention: Destruction or malfunction	
	The TQMa335x belongs to a performance category in which a cooling system is essential in most applications. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM335x must be taken into consideration when connecting the heat sink, see (4), (5). The AM335x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa335x and thus malfunction, deterioration or destruction.

4.7 Structural requirements

The TQMa335x is held in the mating connectors by the retention force of the pins (240). If high requirements are set for vibration and shock resistance, an additional retainer has to be provided in the final product to hold the TQMa335x in its position.

4.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa335x may only be extracted from the carrier board by using the extraction tool MOZIA335 that can also be obtained separately.

Attention: Note with respect to the component placement of the carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa335x for the extraction tool MOZIA335.

5. SOFTWARE

The TQMa335x comes with a preinstalled boot loader U-Boot and a BSP tailored for the MBa335x.
More information can be found in the Support Wiki for the TQMa335x.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa335x was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and/or shielding besides,
  take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa335x.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤3.3 V DC), tests with respect to the operational and personal safety haven't been carried out.

6.4 Climatic and operational conditions

The temperature range, in which the TQMa335x works reliably, strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 49: Climate and operational conditions extended temperature range –25 °C to +85 °C

Parameter	Range	Remark
Chip temperature AM335x	–40 °C to +95 °C	Tj = +105 °C
Environmental temperature AM335x	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	Tj = +150 °C
Environmental temperature PMIC	–40 °C to +85 °C	–
Case temperature DDR3L SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–25 °C to +85 °C	–
Storage temperature TQMa335x	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 50: Climate and operational conditions industrial temperature range –40 °C to +85 °C

Parameter	Range	Remark
Chip temperature AM335x	–40 °C to +95 °C	Tj = +105 °C
Environmental temperature AM335x	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	Tj = +150 °C
Environmental temperature PMIC	–40 °C to +85 °C	–
Case temperature DDR3L SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Storage temperature TQMa335x	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the thermal characteristics of the AM335x is to be taken from the Texas Instruments Data Sheets (1), (3), and (5).

6.5 Reliability and service life

The calculated theoretical MTBF of the TQMa335x is (TBD) h @ +40 °C environmental temperature, ground benign.

The TQMa335x is designed to be insensitive to vibration and impact.

High quality industrial grade connectors are assembled on the TQMa335x.

Detailed information concerning the service life of the AM335x under different operational conditions is to be taken from the Texas Instruments Data Sheets (1), (3), and (5).

6.6 Environment protection

6.6.1 RoHS

The TQMa335x is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

6.6.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa335x was designed to be recyclable and easy to repair.

6.7 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

6.8 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa335x must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the TQMa335x enable compliance with EuP requirements for the TQMa335x.

6.9 Battery

No batteries are used on the TQMa335x.

6.10 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa335x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa335x is delivered in reusable packaging.

6.11 Other entries

The energy consumption of this subassembly is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

7. APPENDIX

7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 51: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AIN	Analog In
ARM®	Advanced RISC Machine
AVS	Adaptive Voltage Scaling
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
DC	Direct Current
DDR	Double Data Rate
DDR3L	Double Data Rate Type three Low voltage
DIN	Deutsche Industrie Norm
DVS	Dynamic Voltage Scaling
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multi-Media Card
EN	Europäische Norm
ESD	Electro-Static Discharge
FR-4	Flame Retardant 4
GMII	Gigabit Media-Independent Interface
GPIO	General Purpose Input/Output
GPMC	General Purpose Memory Controller
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-Integrated Sound
IP	Ingress Protection
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MCASP	Multichannel Audio Serial Port
MCSPI	Multichannel Serial Port Interface
MD	Management Data
MII	Media-Independent Interface
MMC	Multimedia Card
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures

Table 51: Acronyms (continued)

Acronym	Meaning
n.a.	Not Assembled
NAND	Not-And
NMI	Non-Maskable Interrupt
NOR	Not-Or
O	Output
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection
WXGA	Wide Extended Graphics Array

7.2 References

Table 52: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	Sitara™ AM335x ARM® Cortex™-A8 Microprocessors (MPUs)	G / June 2014	Texas Instruments
(2)	Pinmux Utility for ARM® MPU Processors	Feb. 2013	Texas Instruments
(3)	AM335x ARM® Cortex™-A8 Microprocessors Technical Reference Manual	K / June 2014	Texas Instruments
(4)	AM335x Power Consumption Summary	May 2013	Texas Instruments
(5)	AM335x Thermal Considerations	Apr. 2013	Texas Instruments
(6)	TPS65910Ax PMIC	Oct. 2014	Texas Instruments
(7)	Sitara™ AM335x ARM® Cortex™-A8 Silicon Errata	E / Apr. 2013	Texas Instruments
(8)	MBa335x User's Manual	– current –	TQ-Systems
(9)	Support-Wiki for the TQMa335x	– current –	TQ-Systems

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