TQMa28
User's Manual

TQMa28 UM 0203
05.05.2020

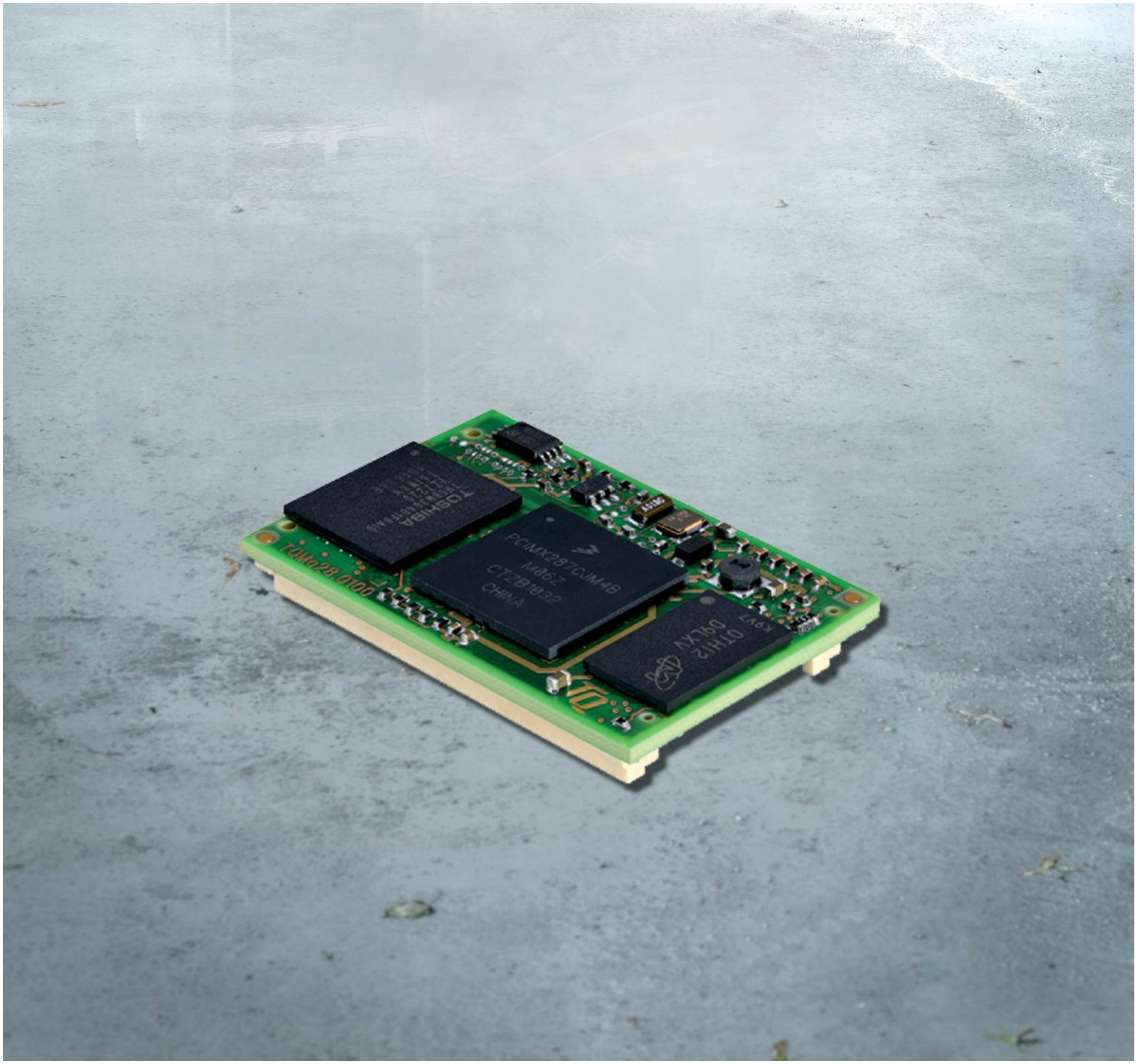

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
003	18.03.2011	Petz		Document created
004	14.07.2011	Petz	Table 6 Illustration 10	Pin assignment revised Replaced
100	25.10.2011	Petz	All	Complete rework
101	03.11.2011	Petz	Table 19	Unit corrected
102	19.12.2011	Petz	All	Expression “Accumulator” replaced with “battery” Expressions containing the word “battery” stated more precisely
103	24.05.2012	Petz	Table 4 Table 6 Table 6 Section 5	Values of plating corrected Typo corrected: LDADC4 ⇨ LRADC4 Negation removed: USB_0_PWR_EN, USB_1_PWR_EN Link to Support-Wiki added
104	28.03.2013	Petz	4.2.8 3.1.2.1 All	Info regarding LAN8720 clarified Max. size of eMMC corrected Signal description of SD_WP and SD_DETECT# corrected
200	11.02.2014	Petz	All	Complete rework
0201	30.11.2016	Petz	All 1.4 2 Table 4 Table 5 4.2.1.1 4.2.1.2 Table 13 7.6.4, 7.6.5, 7.6.6, 7.6.7 Table 45	Freescale replaced with NXP FAX number updated Info regarding Support-Wiki added PU / PD at signals LCD_D03 and LCD_D04 corrected (VCC3V3_REF) at pin X2-16 removed Warning added Correlation corrected: SSP0 ⇨ eMMC, SSP1 ⇨ SD card Updated Added Updated and extended
0202	26.10.2018	Petz	All 1.3, 7.6.2, Illustration 10, Illustration 11, Table 46 Table 8, Table 9 4.2.14.3 Table 41	Formatting, typo, links updated Updated “PU” voltage added Warning updated Added
0203	05.05.2020	Petz	All Table 6 Table 22 6.4.2	Non-functional changes MCIMX283CVM4B added Direction of signals SAIF0_SDATA0 and SAIF1_SDATA0 corrected Reworked

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TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa28 and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa28 circuit diagram
- MBa28 User's Manual
- MCIMX28RM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqma28

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa28 revision 02xx.

This User's Manual does not replace the Reference Manual of the CPU.

The TQMa28 is a universal Minimodule based on the NXP ARM® CPU i.MX287 or i.MX283.

The ARM926EJ-S™ core works with up to 454 MHz. The TQMa28 extends the TQ-Systems GmbH product range and provides a well-balanced ratio between computing performance and graphics power.

The TQMa28 provides the following key functions and characteristics:

- NXP i.MX287 (ARM9 architecture), 454 MHz
- All functional CPU pins are routed to TQMa28 connectors
- Up to 16 Gbyte eMMC NAND flash
- Up to 256 Mbyte DDR2 SDRAM
- 64 Kbit EEPROM
- Up to eight 12 bit A/D converter
- PWM
- Various serial interfaces depending on multiplexing (UART, SPI, I^2C, I^2S)
- 2 × CAN
- Temperature sensor
- 2 × USB 2.0 Hi-Speed Host interface with integrated PHY
- Industrial temperature range on request
- Low power consumption (0.11 to 2 W, depending on mode of operation)
- Dimensions: 40 × 26 mm^2
- Long term available
- Power supply: 5 V or Lithium-ion battery

All interfaces supported by software are described in the Support-Wiki.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 TQMa28, block diagram

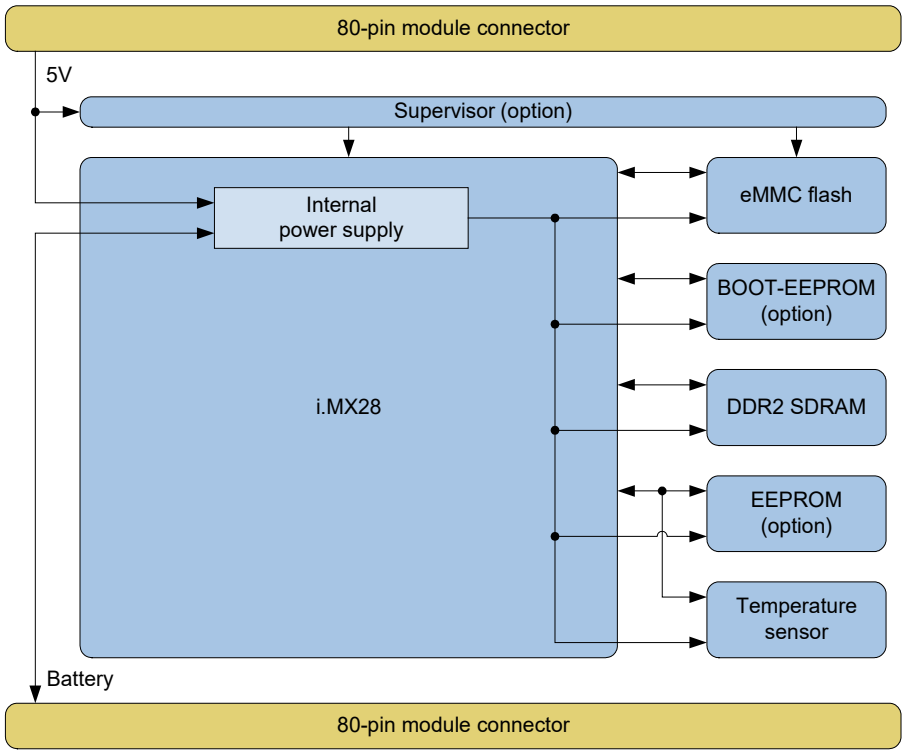


Illustration 1: TQMa28, block diagram

3.1.2 System functionality

The following elements are implemented on the TQMa28:

- i.MX287 CPU
- DDR2 SDRAM
- eMMC NAND flash
- EEPROM
- Temperature sensor
- 2 × 80-pin TQMa28 connector

The following interfaces are available at the TQMa28 connectors:

- 1 × parallel display interface
- 1 × SD card
- 5 × UART
- 2 × CAN
- 2 × I^2C
- 1 × I^2S
- 1 × SPI
- 2 × Ethernet
- 2 × USB 2.0 Hi-Speed
- JTAG
- ADCs
- PWMs
- GPIOs

4. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa28, and the BSP provided by TQ-Systems GmbH. See also section (5).

4.1 Interfaces to other systems and devices

The TQMa28 is connected to the carrier board with 160 pins on two connectors.

The TQMa28 is held in the connectors with a considerable retention force.

To avoid damaging the TQMa28 connectors as well as the carrier board connectors while removing the TQMa28 the use of an extraction tool is strongly recommended.

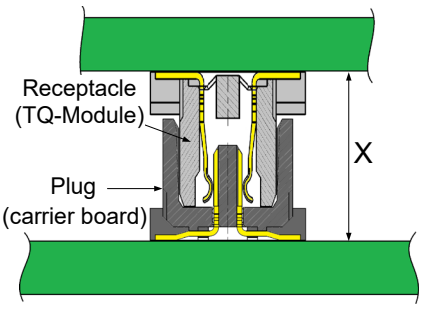
4.1.1 TQMa28, connectors

Table 2: TQMa28, connectors

Manufacturer	Order no.	Description
TE Connectivity	5177985-3	• 80-pin female connector • 0.8 mm pitch • –40 °C to +85 °C

In the following table applicable carrier board mating connectors are listed.

Table 3: Carrier board connectors

Manufacturer	Order code	No. of pins	Plating	Stack height (X)	
TE Connectivity	5177984-3	80	0.2 µm Gold	5 mm	
	5084614-3	80	0.76 µm Gold		
	5179029-3	80	0.2 µm Gold	6 mm	
	5084615-3	80	0.76 µm Gold		
	5179030-3	80	0.2 µm Gold	7 mm	
	1-5179030-3	80	0.76 µm Gold		
	5179031-3	80	0.2 µm Gold	8 mm	
	6123002-3	80	0.76 µm Gold		

The board to board distance results from the height of the TQMa28 connector and the connector on the carrier board. TQMa28 drawings can be found in section 6.

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of.

The TQMa28 pinout is described in detail in the following tables.

In addition to direction, pin name and pin number, external and internal Pull-Up or-down wirings as well as the references to I/O voltage and processor pin characteristics are listed.

4.1.1.1 Connector X1

Table 4: Pinout connector X1

PU/PD	I/O	Level	Usage	i.MX28 pin	Name	Pin		Name	i.MX28 pin	Usage	Level	I/O	PU/PD
		0 V	POWER		GND	1	2	GND		POWER	0 V		
	O	3V3	LCD	N1	LCD_DOTCLK	3	4	LCD_VSYNC	L1	LCD	3V3	O	
		0 V	POWER		GND	5	6	LCD_HSYNC	M1	LCD	3V3	O	
	O	3V3	LCD	K1	LCD_WR_RW#	7	8	GND		POWER	0 V		
	O	3V3	LCD	M6	LCD_RESET	9	10	LCD_RS	M4	LCD	3V3	O	
	O	3V3	LCD	P4	LCD_RD_E	11	12	LCD_ENABLE	N5	LCD	3V3	O	
	O	3V3	LCD	P5	LCD_CS#	13	14	LCD_D00	K2	LCD	3V3	O	10 kΩ ↑
10 kΩ ↓	O	3V3	LCD	K3	LCD_D01	15	16	LCD_D02	L2	LCD	3V3	O	10 kΩ ↓
10 kΩ [1]	O	3V3	LCD	L3	LCD_D03	17	18	LCD_D04	M2	LCD	3V3	O	10 kΩ ↓
	O	3V3	LCD	M3	LCD_D05	19	20	LCD_D06	N2	LCD	3V3	O	
	O	3V3	LCD	P1	LCD_D07	21	22	LCD_D08	P2	LCD	3V3	O	
	O	3V3	LCD	P3	LCD_D09	23	24	LCD_D10	R1	LCD	3V3	O	
	O	3V3	LCD	R2	LCD_D11	25	26	LCD_D12	T1	LCD	3V3	O	
	O	3V3	LCD	T2	LCD_D13	27	28	LCD_D14	U2	LCD	3V3	O	
	O	3V3	LCD	U3	LCD_D15	29	30	LCD_D16	T3	LCD	3V3	O	
	O	3V3	LCD	R3	LCD_D17	31	32	LCD_D18	U4	LCD	3V3	O	
	O	3V3	LCD	T4	LCD_D19	33	34	LCD_D20	R4	LCD	3V3	O	
	O	3V3	LCD	U5	LCD_D21	35	36	LCD_D22	T5	LCD	3V3	O	
	O	3V3	LCD	R5	LCD_D23	37	38	GPIO0_24	R6	GPIO	3V3	I/O	
		5 V	POWER		VCC5V	39	40	GPIO0_6	U6	GPIO	3V3	I/O	
		5 V	POWER		VCC5V	41	42	GPIO0_27	P7	GPIO	3V3	I/O	
		0 V	POWER		GND	43	44	GPIO0_4	T7	GPIO	3V3	I/O	
		0 V	POWER		GND	45	46	GPIO3_6	K5	GPIO	3V3	I/O	
	I/O	3V3	GPIO	N9	GPIO0_17	47	48	GPIO0_26	P6	GPIO	3V3	I/O	
	I/O	3V3	SD_CARD	U8	SD_D0	49	50	GPIO0_7	T6	GPIO	3V3	I/O	
	I/O	3V3	SD_CARD	R8	SD_D2	51	52	GPIO0_16	N7	GPIO	3V3	I/O	
	I/O	3V3	SD_CARD	N8	SD_CMD	53	54	GPIO0_5	R7	GPIO	3V3	I/O	
	I	3v3	SD_CARD	L9	SD_WP	55	56	SD_D1	T8	SD_CARD	3V3	I/O	
	O	3V3	SD_CARD	P8	SD_CLK	57	58	SD_D3	U7	SD_CARD	3V3	I/O	
	I	3V3	UART1	L4	AUART1_RX	59	60	SD_DETECT#	N6	SD_CARD	3V3	I	
	I	3V3	UART3	M5	AUART3_RX	61	62	AUART1_TX	K4	UART1	3V3	O	
	O	3V3	UART3	K6	AUART3_RTS#	63	64	AUART3_TX	L5	UART3	3V3	O	
	I	3V3	CAN1	M9	CAN1_RX	65	66	AUART3_CTS#	L6	UART3	3V3	I	
	O	3V3	CAN1	M7	CAN1_TX	67	68	PWM4	E10	PWM	3V3	O	
	O	3V3	LCD/PWM	K8	LCD_BL_PWM	69	70	PWM3 [2]	E9	PWM	3V3	O	
	O	3V3	DUART	L7	DUART_TX	71	72	DUART_RX	K7	DUART	3V3	I	10 kΩ ↑
4.7 kΩ ↑	I/O	3V3	I2C1	H7	I2C1_SDA	73	74	I2C1_SCL	H6	I2C1	3V3	I/O	4.7 kΩ ↑
	I	3V3	UART0	G5	AUART0_RX	75	76	AUART0_TX	H5	UART0	3V3	O	
	O	3V3	UART0	J7	AUART0_RTS#	77	78	AUART0_CTS#	J6	UART0	3V3	I	
		0 V	POWER		GND	79	80	GND		POWER	0 V		

1: Pull-Up or Pull-Down depends on version of TQMa28. See section 4.2.1.2.
2: Controlled by ROM code; pin PWM3 has the function POWER_GATE_GPIO-SD/MMC (output, low) during the boot process. Further information is to be taken from the Reference Manual (1).

4.1.1.2 Connector X2

Table 5: Pinout connector X2

PU/PD	I/O	Level	Usage	i.MX28 pin	Name	Pin		Name	i.MX28 pin	Usage	Level	I/O	PU/PD
		0 V	POWER		GND	1	2	GND		POWER	0 V		
	O	3V3	1588	B1	1588_Event2_out	3	4	1588_Event2_in	C1	1588	3V3	I	
	O	3V3	1588	D1	1588_Event3_out	5	6	1588_Event3_in	E1	1588	3V3	I	
	I	3V3	UART	C2	AUART4_RX	7	8	AUART4_TX	A2	UART	3V3	O	
	O	3V3	UART	B2	AUART4_RTS#	9	10	AUART4_CTS#	D2	UART	3V3	I	
	O	3V3	SPI	A3	SSP2_SCK	11	12	SSP2_MISO	B3	SPI	3V3	I	
	O	3V3	SPI	C3	SSP2_MOSI	13	14	SSP2_SS0#	C4	SPI	3V3	O	
	O	3V3	ENET	F3	ENET_RESET#	15	16	DEBUG	B9	CONFIG	3V3	I	10 kΩ ↑
		0 V	POWER		GND	17	18	GND		POWER	0 V		
	O	3V3	ENET	G4	ENET_MDC	19	20	ENET_CLK	E2	ENET	3V3	O	
	I/O	3V3	ENET	H4	ENET_MDIO	21	22	ENET_INT#	E3	ENET	3v3	I	
	I	3V3	ENET0	H1	ENET0_RXD0	23	24	ENET0_TXD0	F1	ENET0	3v3	O	
	I	3V3	ENET0	H2	ENET0_RXD1	25	26	ENET0_TXD1	F2	ENET0	3v3	O	
	I	3V3	ENET0	E4	ENET0_RX_EN	27	28	ENET0_TX_EN	F4	ENET0	3V3	O	
	I	3V3	ENET1	J3	ENET1_RX_EN	29	30	ENET1_TX_EN	J4	ENET1	3V3	O	
	I	3V3	ENET1	J1	ENET1_RXD0	31	32	ENET1_TXD0	G1	ENET1	3V3	O	
	I	3V3	ENET1	J2	ENET1_RXD1	33	34	ENET1_TXD1	G2	ENET1	3V3	O	
		0 V	POWER		GND	35	36	GND		POWER	0 V		
	O	3V3	USB1	F6	USB_1_PWR_EN	37	38	USB_1_DM	B8	USB1	5 V	I/O	
	I	3V3	USB1	D3	USB_1_OC#	39	40	USB_1_DP	A8	USB1	5 V	I/O	
	O	3V3	USB0	F5	USB_0_PWR_EN	41	42	USB_0_DM	A10	USB0	5 V	I/O	
	I	3V3	USB0	D4	USB_0_OC#	43	44	USB_0_DP	B10	USB0	5 V	I/O	
		0 V	POWER		GND	45	46	GND		POWER	0 V		
	I	3V3	USB0	J5	USB_0_ID	47	48	CAN0_RX	L8	CAN0	3V3	I	
	I	3V3	CONFIG	A11	PSWITCH	49	50	CAN0_TX	M8	CAN0	3V3	O	
4.7 kΩ ↑	I/O	3V3	I2C0	C7	I2C0_SCL	51	52	I2C0_SDA	D8	I2C0	3V3	I/O	4.7 kΩ ↑
	O	3V3	SPDIF	D7	SPDIF	53	54	GPIO2_9	D10	GPIO	3V3	I/O	
	O	3V3	I2S/AUDIO	E7	SAIF0_SDATA0	55	56	SAIF1_SDATA0	E8	I2S/AUDIO	3V3	I	
	I/O	3V3	I2S/AUDIO	F7	SAIF0_BITCLK	57	58	SAIF0_LRCLK	G6	I2S/AUDIO	3V3	I/O	
	O	3V3	I2S/AUDIO	G7	SAIF0_MCLK	59	60	RESET#	A14	CONFIG	3V3	I	10 kΩ ↑
		0 V	POWER		GND	61	62	GND		POWER	0 V		
	I	[3]	Touch/ADC	C14	LRADC6	63	64	HSADC0	B14	ADC	[3]	I	
	I	[3]	Touch/ADC	D13	LRADC4	65	66	LRADC5	D15	Touch/ADC	[3]	I	
	I	[3]	Touch/ADC	C8	LRADC2	67	68	LRADC3	D9	Touch/ADC	[3]	I	
	I	[3]	ADC	C15	LRADC0	69	70	LRADC1	C9	ADC	[3]	I	
10 kΩ ↑	I	3V3	JTAG	D12	JTAG_TMS	71	72	JTAG_TCK	E11	JTAG	3V3	I	10 kΩ ↑
10 kΩ ↑	I	3V3	JTAG	E12	JTAG_TDI	73	74	JTAG_TRST#	D14	JTAG	3V3	I	10 kΩ ↑
		4V2	POWER	A15	Battery	75	76	JTAG_RTCK	E14	JTAG	3V3	O	10 kΩ ↑
		4V2	POWER	A15	Battery	77	78	JTAG_TDO	E13	JTAG	3V3	O	
		0 V	POWER		GND	79	80	GND		POWER	0 V		

3: See NXP datasheet (2).

4.2 System components

4.2.1 Processor

The NXP processor i.MX28 (MCIMX287CVM4B) based on an ARM926EJ-S™ core is manufactured in 90 nm technology.
It provides a wide range of functions. Illustration 2 gives an overview.
More information about the i.MX28 processor is provided in the following table.

Table 6: Processor information

Manufacturer	Part number	Temperature range	Package	Silicon revision
NXP	MCIMX283CVM4B	–40 °C to +85 °C	BGA289	1.2
NXP	MCIMX287CVM4B	–40 °C to +85 °C	BGA289	1.2

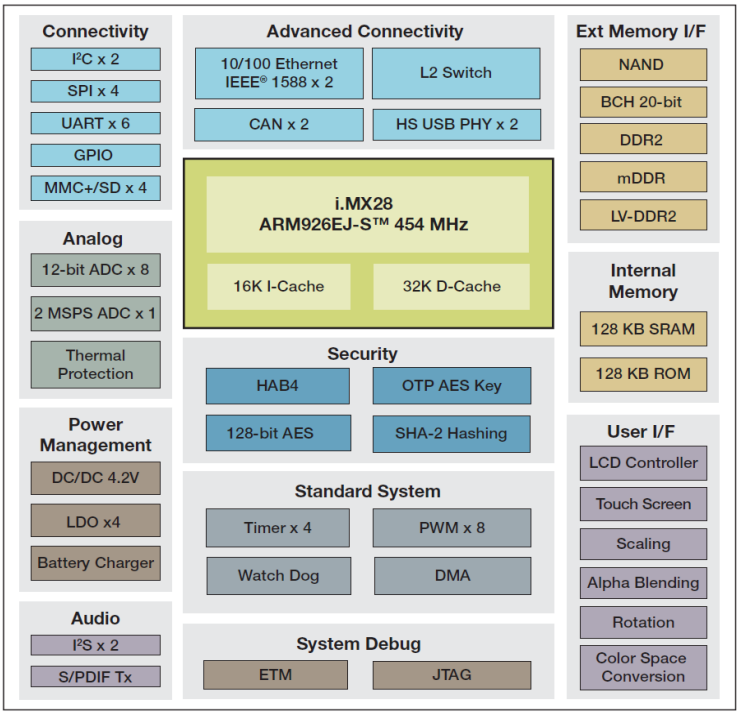


Illustration 2: i.MX28, block diagram
(Source: NXP)

Other processor functionality shown in the block diagram can be looked up in the NXP Reference Manual (1).
All essential processor pins, except the DDR2 SDRAM interface and the eMMC, are routed to the connectors.

4.2.1.1 Boot modes

The i.MX28 has of a ROM with integrated boot code. When the i.MX28 starts this boot code initializes the hardware and then loads the program image from the selected boot device.
Instead of booting from the integrated eMMC it is also possible to boot from one of the following interfaces:

- USB
- I²C
- SPI
- SSP
- GPMI

The boot device and its configuration can be defined with several boot mode registers.
For this the i.MX28 offers two possibilities:

- The settings are read from boot mode pins
- The settings are read from internal burnt OTP eFuses

The exact behaviour during the boot process depends on the value of eFuse ENABLE_PIN_BOOT_CHECK and the signal LCD_RS. The following table shows the possible combinations.

Table 7: Boot configuration

eFuse: ENABLE_PIN_BOOT_CHECK	Pin: LCD_RS	TQMa28 pin	Boot config read at	Remark
0	X	X1-10	Boot mode pins	Default
1	0		OTP eFuses	–
	1		Boot mode pins	–

Note: Malfunction	
	Burning an eFuse is irreversible! TQ-Systems GmbH takes no responsibility for the correct operation of the TQMa28, if eFuses are burnt by the user. Burning eFuses has to be coordinated with TQ-Systems GmbH, since the TQMa28 then no longer complies with the factory default (altered hardware).

4.2.1.2 Boot devices

On account of NXP CPU erratum TKT131240, two different boot modes are possible.

This erratum describes an error in the ROM code the CPU which leads to an inverted clock polarity when the boot mode is set to booting from SSP0 (eMMC) or SSP1 (SD card) (see also (3)). This may cause boot errors.

As a workaround the boot device has to be an EEPROM which has to be connected to I2C0 or SPI3. The EEPROM has to contain a binary patch provided by NXP, which corrects the clock polarity of either SSP0 or SSP1.

To fix this erratum an optional EEPROM, which is connected to I2C0, is provided on the TQMa28. It corrects the polarity error at SSP0, to enable an error-free boot process from eMMC. Existing designs must be checked whether this option can be used, as address conflicts may appear, or a different multiplexing function than I2C0 was selected.

Optionally an EEPROM can be connected to I2C0 or SPI3 on the carrier board to fix this erratum.

This results in different boot mode pin wirings for the TQMa28, which are shown in the following sections:

4.2.1.2.1 TQMa28 with EEPROM at I2C0

The EEPROM with boot patch is preset as the standard boot device (I2C0 MASTER 3V3).
Therefore the boot mode pins on the TQMa28 are connected as follows:

Table 8: Configuration boot mode pins EEPROM

Pin name	Boot mode name	TQMa28 pin	Boot mode	Remark
LCD_D00	BM0	X1-14	1	10 kΩ PU to 3.3 V on TQMa28
LCD_D01	BM1	X1-15	0	10 kΩ PD on TQMa28
LCD_D02	BM2	X1-16	0	10 kΩ PD on TQMa28
LCD_D03	BM3	X1-17	0	10 kΩ PD on TQMa28
LCD_D04	VOLTAGE SELECT	X1-18	0	10 kΩ PD on TQMa28

4.2.1.2.2 TQMa28 without EEPROM at I2C0

The eMMC is preset as the standard boot device (SD/MMC MASTER ON SSP0 3V3).
Therefore the boot mode pins on the TQMa28 are connected as follows:

Table 9: Configuration boot mode pins eMMC

Pin name	Boot mode name	TQMa28 pin	Boot mode	Remark
LCD_D00	BM0	X1-14	1	10 kΩ PU to 3.3 V on TQMa28
LCD_D01	BM1	X1-15	0	10 kΩ PD on TQMa28
LCD_D02	BM2	X1-16	0	10 kΩ PD on TQMa28
LCD_D03	BM3	X1-17	1	10 kΩ PU to 3.3 V on TQMa28
LCD_D04	VOLTAGE SELECT	X1-18	0	10 kΩ PD on TQMa28

4.2.1.2.3 Other boot modes

To boot from another source rather than the TQMa28-internal eMMC, or to use the function ENABLE_PIN_BOOT_CHECK, the default boot mode settings can be changed by resistors of about 1 kΩ at the pins LCD_D[4:0] or LCD_RS.

The necessary settings for other boot device are to be taken from the NXP Reference Manual (1).

4.2.1.3 Processor clock supply

A crystal oscillator on the TQMa28 supplies the processor with 24 MHz.
A 32.768 kHz crystal oscillator on the TQMa28 supplies the RTC domain with a clock signal.

4.2.1.4 Pin multiplexing

Depending on the configuration, the pin multiplexing enables different pins to have different functions. NXP provides the program “IOMUXCC“ on their website, which supports the selection of desired options.
The information in this User's Manual corresponds to the signals used on the Starter Kit STK-MBa28 and their support in the BSP.
TQ-Systems GmbH provides an xml file created with the program "IOMUXCC", which shows the TQMa28 pin-multiplexing.
The user can configure specific pin-multiplexing based on this xml file. The xml file can be obtained from TQ-Systems Support.
It cannot be guaranteed that the generated configuration is accurate!
It is the user's responsibility to conscientiously check the generated configuration.

Attention: Destruction or malfunction!	
	Many CPU pins can be used in several different ways. Please, pay attention to the notes about the wiring of these pins in the i.MX28 Reference Manual (1) before integration / start-up of your carrier board / Starterkit.

4.2.1.5 CPU errata

Attention: Destruction or malfunction!	
	Please pay attention to the latest NXP CPU errata (3).

4.2.2 Memory

4.2.2.1 DDR2 SDRAM

The following illustration shows how the DDR2 SDRAM is connected to the CPU.

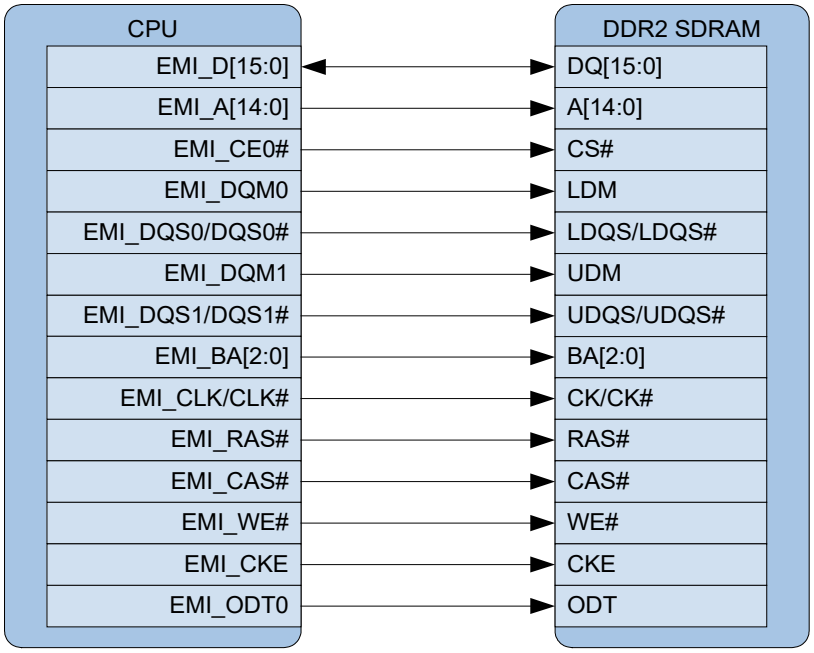


Illustration 3: DDR2 SDRAM interface

The following table gives an overview of possible alternatives.

Table 10: Types of DDR2 SDRAM

Manufacturer	Manufacturer's number	Type	Size	Temperature range	Remark
Micron	MT47H64M16HR-3IT:H	64M16	128 Mbyte	–40 °C to +85 °C	–
Micron	**MT47H64M16HR-25EIT:H**	**64M16**	**128 Mbyte**	**–40 °C to +85 °C**	**Default**
Micron	MT47H128M16RT-25EIT	128M16	256 Mbyte	–40 °C to +85 °C	–

The memory allocates the following address range:

Table 11: Address configuration DDR2 SDRAM

Start address	Size	Chip Select	Size
0x4000 0000	0x0800 0000	CE0#	128 Mbyte
0x4000 0000	0x1000 0000	CE0#	256 Mbyte

4.2.2.2 eMMC

The TQMa28 is equipped with an eMMC flash to store programs and data (boot loader and operating system).
It is controlled via the i.MX28 SD card controller SSP0.

The following illustration shows how the eMMC is connected to the processor.

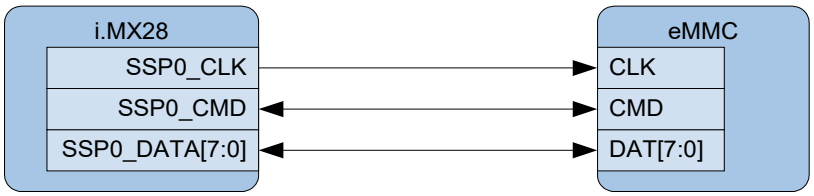


Illustration 4: eMMC interface

4.2.2.3 EEPROM

For permanent storage of e.g. TQMa28 characteristics or customers parameters a serial 64 kbit EEPROM is provided.
The EEPROM is controlled via I^2C bus 1.
Detailed information concerning the I^2C-address configuration can be found in section 4.2.8.1.
The EEPROM write protection (WP) is not available.

Table 12: Memory model EEPROM

Manufacturer	Part number	Size
ST Microelectronics	M24C64-WDW6TP	64 kbit

In the EEPROM TQMa28-specific data is stored. It is, however, not essential for the correct operation of the TQMa28.
The data can be deleted or altered by the user.

In the following table the parameters stored in the EEPROM are shown.

Table 13: EEPROM TQMa28-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	Variable	Variable	$32_{(10)}$	Binary	Hard Reset Configuration Word (HRCW), (optional)
0x20	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
0x30	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x40	Variable	Variable	$64_{(10)}$	ASCII	Order code
0x80	–	–	$8{,}064_{(10)}$	–	(Unused)

4.2.3 RTC

The TQMa28 provides a processor-internal RTC. The RTC current consumption is approximately 30 µA.
A 32.768 kHz crystal oscillator clocks the RTC.

In the following table the crystal oscillator parameters are given.

Table 14: 32.768 kHz crystal oscillator parameters

Parameter	Value	Unit	Remark
Frequency tolerance	±20	ppm	@ +25 °C
Frequency ageing	±3 max.	ppm	First year, @ +25 °C
Parabolic Coefficient	-0.04×10^{-6}	$°C^2$	Additional deviation at temp ≠ +25 °C

When the power supply is switched off the CPU-internal RTC has to be buffered by a lithium-ion battery to maintain its function.
As the RTC in the CPU is supplied by the same power plane than the CPU in normal operation the whole system supplies itself from this power plane. For this reason the RTC cannot be buffered with a normal button cell. If the characteristics of the internal RTC are not suitable, the DS1339 is proposed as an external RTC on the carrier board.

4.2.4 Temperature sensor

A National Semiconductor LM73 temperature sensor is provided. The sensor is placed on the topside of the TQMa28 (D6, Illustration 10). The sensor interface is described in section 4.2.8.1.

4.2.5 Graphics interfaces / LCD bus

Parallel displays with a maximum frame size of up to 800 × 480 pixels can be connected to the TQMa28.
The parallel data interface can be up to 24 bits wide. The LCD bus is directly routed to the connectors.

Table 15: Display signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
LCD_D[23:0]	LCD_D[23:0]	X1-[37:14]	O	LCD interface RGB-Data
LCD_HSYNC	LCD_HSYNC	X1-06	O	LCD interface Horizontal Sync
LCD_VSYNC	LCD_VSYNC	X1-04	O	LCD interface Vertical Sync
LCD_ENABLE	LCD_ENABLE	X1-12	O	LCD interface Enable
LCD_DOTCLK	LCD_DOTCLK	X1-03	O	LCD interface Dot Clock
LCD_CS	LCD_CS#	X1-13	O	LCD interface Chip Select
LCD_RS	LCD_RS	X1-10	O	LCD interface Register Select
LCD_WR_RWN	LCD_WR_RW#	X1-07	O	LCD interface 6800 R/W# / 8080 W
LCD_RD_E	LCD_RD_E	X1-11	O	LCD interface 6800 Enable / 8080 RD
LCD_RESET	LCD_RESET	X1-09	O	LCD interface Reset Out

4.2.6 Ethernet

The i.MX28 provides two built-in Fast Ethernet controllers, which are designed for 10 and 100 Mbps.
Both provided RMII interfaces are available to the user directly at the connectors.
The Ethernet interface is completed by a PHY on the carrier board.

Table 16: Ethernet signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
ENET0_RX_EN	ENET0_RX_EN	X2-29	I	Ethernet0 Data Valid / Carrier Sense
ENET0_RXD0	ENET0_RXD0	X2-23	I	Ethernet0 Input Receive Data
ENET0_RXD1	ENET0_RXD1	X2-25	I	Ethernet0 Input Receive Data
ENET0_TX_EN	ENET0_TX_EN	X2-28	O	Ethernet0 Output Transmit Enable
ENET0_TXD0	ENET0_TXD0	X2-24	O	Ethernet0 Output Transmit Data
ENET0_TXD1	ENET0_TXD1	X2-26	O	Ethernet0 Output Transmit Data
ENET1_RX_EN	ENET1_RX_EN	X2-27	I	Ethernet1 Data Valid / Carrier Sense
ENET1_RXD0	ENET1_RXD0	X2-31	I	Ethernet1 Input Receive Data
ENET1_RXD1	ENET1_RXD1	X2-33	I	Ethernet1 Input Receive Data
ENET1_TX_EN	ENET1_TX_EN	X2-30	O	Ethernet1 Output Transmit Enable
ENET1_TXD0	ENET1_TXD0	X2-32	O	Ethernet1 Output Transmit Data
ENET1_TXD1	ENET1_TXD1	X2-34	O	Ethernet1 Output Transmit Data
ENET_CLK	ENET_CLK	X2-20	I/O	Reference Clock
ENET_MDC	ENET_MDC	X2-19	O	Ethernet Output Management Data Clock
ENET_MDIO	ENET_MDIO	X2-21	I/O	Ethernet Management Data
GPIO4_13	ENET_RESET#	X2-15	O	Ethernet Output Reset (GPIO)
GPIO4_5	ENET_INT#	X2-22	I	Ethernet Input Interrupt (GPIO)

The i.MX28-internal clock generator does not meet the clock jitter values required by most Ethernet PHYs.
This may cause Ethernet connection problems during link-up.

It is recommended to provide an external clock generator with suitable precision on the carrier board to generate the clock signal for the input ENET_CLK. This can be achieved by using a quartz crystal or a crystal oscillator.

The CPU supplies additional functions according to IEEE® 1588.

The following signals are available at the connectors:

Table 17: IEEE 1588 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
ENET0_1588_EVENT2_OUT	1588_EVENT2_OUT	X2-03	O	–
ENET0_1588_EVENT2_IN	1588_EVENT2_IN	X2-04	I	–
ENET0_1588_EVENT3_OUT	1588_EVENT3_OUT	X2-05	O	–
ENET0_1588_EVENT3_IN	1588_EVENT3_IN	X2-06	I	–

By turning off pre-set functions and switching on 1588-features, more 1588_Events can be provided.

4.2.7 SD card

The TQMa28 provides an SD card controller (SSP1), whose signals are available at the connector X1.
The following table shows the signals used for the SD card interface.

Table 18: SD card interface signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
SSP1_SCK	SD_CLK	X1-57	O	SD Card Clock
SSP1_CMD	SD_CMD	X1-53	I/O	SD Card Command
SSP1_D3	SD_D3	X1-58	I/O	SD Card Data3
SSP1_D2	SD_D2	X1-51	I/O	SD Card Data2
SSP1_D1	SD_D1	X1-56	I/O	SD Card Data1
SSP1_D0	SD_D0	X1-49	I/O	SD Card Data0
SSP1_CARD_DETECT	SD_DETECT#	X1-60	I	SD Card Detect
GPIO0_28	SD_WP	X1-55	I	SD Card Write-Protection

4.2.8 Serial interfaces

The supported standards, transmission modes and transfer rates of the following interfaces are to be taken from the NXP Reference Manual (1).

4.2.8.1 I²C

The i.MX28 provides two I²C interfaces. Both interfaces are routed to the connectors.
The following table shows the signals used for the I²C interfaces.

Table 19: I²C signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
I2C0_SDA	I2C0_SDA	X2-52	I/O	4.7 kΩ PU to 3.3 V on TQMa28
I2C0_SCL	I2C0_SCL	X2-51	O	4.7 kΩ PU to 3.3 V on TQMa28
I2C1_SDA	I2C1_SDA	X1-73	I/O	4.7 kΩ PU to 3.3 V on TQMa28
I2C1_SCL	I2C1_SCL	X1-74	O	4.7 kΩ PU to 3.3 V on TQMa28

The following illustration shows the I²C signals used and how they are connected to the temperature sensor and the EEPROMs.

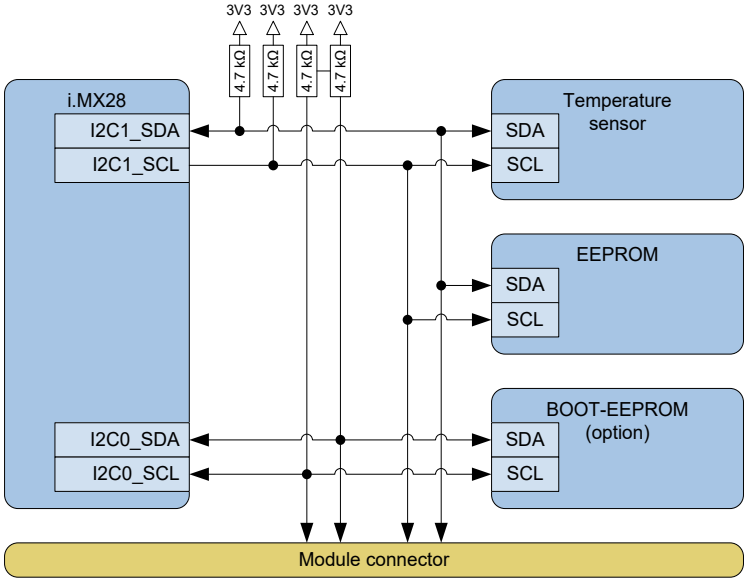


Illustration 5: I²C buses

The following table shows the I²C bus 0 address used on the TQMa28 in case the version with boot EEPROM was chosen:

Table 20: I2C0 address configuration

Component	Address	
EEPROM	0x50	101 0000b

There are two devices with an I²C interface on the TQMa28. Both devices are connected to I²C bus 1:

Table 21: I2C1 address configuration

Component	Address	
Temperature sensor	0x49	100 1001b
EEPROM	0x50	101 0000b

Attention: Pull-Up resistors	
	Pull-Up resistors for the I²C buses are already assembled on the TQMa28. If more devices are connected on the carrier board the maximum capacitive bus load according to the I²C standard has to be observed. If necessary additional Pull-Ups have to be assembled on the carrier board.

4.2.8.2 I²S

To connect an audio-codec via I²S the Serial Audio Interface (SAIF) signals are routed to the connectors.
The following table shows the signals used for the SAIF interface.

Table 22: I²S signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
SAIF0_MCLK	SAIF0_MCLK	X2-59	O	System Master Clock
SAIF0_LRCLK	SAIF0_LRCLK	X2-58	I/O	I²S Frame Clock
SAIF0_BITCLK	SAIF0_BITCLK	X2-57	I/O	I²S Bit Clock
SAIF0_SDATA0	SAIF0_SDATA0	X2-55	O	I²S Data Output
SAIF1_SDATA0	SAIF1_SDATA0	X2-56	I	I²S Data Input

The SAIF allows to connect 3, 4 or 5-wire interface, e.g., via I²S. Details are to be taken from the NXP Reference Manual (1).

4.2.8.3 SPDIF

The i.MX28 provides an SPDIF interface with transmit functionality.
The following table shows the signals used for the SPDIF interface.

Table 23: SPDIF signal

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
SPDIF	SPDIF	X2-53	O

4.2.8.4 SPI

The i.MX28 SPI interface is named SSP. The SSP2 interface signals are available at the connectors.
In addition to SPI on SSP2, a further SPI interface can be multiplexed on SSP3 as an alternative to AUART4.

Table 24: SPI signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
SSP2_SCK	SSP2_SCK	X2-11	O
SSP2_MOSI	SSP2_MOSI	X2-13	O
SSP2_MISO	SSP2_MISO	X2-12	I
SSP2_SS0	SSP2_SS0#	X2-14	O

4.2.8.5 UART

The i.MX28 provides five Application UART interfaces (AUART) and one debug UART (DUART).
AUART0, AUART1, AUART3, AUART4 and DUART signals are available at the connectors.

The following table shows the signals used for the AUART0 interface.

Table 25: AUART0 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
AUART0_TX	AUART0_TX	X1-76	O
AUART0_RX	AUART0_RX	X1-75	I
AUART0_RTS	AUART0_RTS#	X1-77	O
AUART0_CTS	AUART0_CTS#	X1-78	I

The following table shows the signals used for the AUART1 interface.

Table 26: AUART1 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
AUART1_TX	AUART1_TX	X1-62	O
AUART1_RX	AUART1_RX	X1-59	I

The following table shows the signals used for the AUART3 interface.

Table 27: AUART3 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
AUART3_TX	AUART3_TX	X1-64	O
AUART3_RX	AUART3_RX	X1-61	I
AUART3_RTS	AUART3_RTS#	X1-63	O
AUART3_CTS	AUART3_CTS#	X1-66	I

The following table shows the signals used for the AUART4 interface.

Table 28: AUART4 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
AUART4_TX	AUART4_TX	X2-08	O
AUART4_RX	AUART4_RX	X2-07	I
AUART4_RTS	AUART4_RTS#	X2-09	O
AUART4_CTS	AUART4_CTS#	X2-10	I

The following table shows the signals used for the DUART interface.

Table 29: DUART signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
DUART_TX	DUART_TX	X1-71	O	–
DUART_RX	DUART_RX	X1-72	I	10 kΩ PU to 3.3 V on TQMa28

The UART signals are routed to the connectors as LVTTL signals.
They may need driver's devices on the carrier board to be used as external signals.
In addition, filtering and EMC protection for the UART signals has to be provided on the carrier board.

4.2.8.6 USB

Two USB-High-Speed interfaces are available on the TQMa28. The first (USB0) is OTG capable. The second port exclusively provides a Hi-Speed host. For both ports the PHY is integrated in the i.MX28. The 5 V supply for the USB ports has to be implemented on the carrier board. In addition, filtering and EMC protection for the USB signals has to be provided on the carrier board. Notes are to be found in the USB standard.

The following table shows the signals used for the USB0 interface.

Table 30: USB0 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
USB0DM	USB_0_DM	X2-42	I/O	Negative Data Line
USB0DP	USB_0_DP	X2-44	I/O	Positive Data Line
USB0_ID	USB_0_ID	X2-47	I	Micro-A/-B Identification
GPIO3_9	USB_0_PWR_EN	X2-41	O	Enable Power Distributor (GPIO)
USB0_OVERCURRENT	USB_0_OC#	X2-43	I	Overcurrent Detection

The following table shows the signals used for the USB1 interface.

Table 31: USB1 signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
USB1DM	USB_1_DM	X2-38	I/O	Negative Data Line
USB1DP	USB_1_DP	X2-40	I/O	Positive Data Line
GPIO3_8	USB_1_PWR_EN	X2-37	O	Enable Power Distributor (GPIO)
USB1_OVERCURRENT	USB_1_OC#	X2-39	I	Overcurrent Detection

4.2.8.7 CAN

The i.MX28 provides depending on the version one or two integrated CAN controllers.
All four signals are routed to the connectors. The corresponding drivers have to be provided on the carrier board.
The following table shows the signals used for the CAN interfaces.

Table 32: CAN signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
CAN0_TX	CAN0_TX	X2-50	O
CAN0_RX	CAN0_RX	X2-48	I
CAN1_TX	CAN1_TX	X1-67	O
CAN1_RX	CAN1_RX	X1-65	I

4.2.9 PWM

Three of the eight i.MX28 PWM outputs are directly available at the connectors.
More PWMs are available if the pin multiplexing is adapted.
The following table shows the available PWM signals.

Table 33: PWM signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
PWM2	LCD_BL_PWM	X1-69	O
PWM3	PWM3	X1-70	O
PWM4	PWM4	X1-68	O

4.2.10 GPIO

The i.MX28 processor provides GPIO ports as a second or multiple configuration with other function units.
The configuration can be taken from the NXP Reference Manual (1).
Some GPIOs are directly routed to the connectors.
The following table shows the GPIO signals which can be used.

Table 34: GPIO signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.
BANK0_PIN04	GPIO0_4	X1-44	I/O
BANK0_PIN05	GPIO0_5	X1-54	I/O
BANK0_PIN06	GPIO0_6	X1-40	I/O
BANK0_PIN07	GPIO0_7	X1-50	I/O
BANK0_PIN16	GPIO0_16	X1-52	I/O
BANK0_PIN17	GPIO0_17	X1-47	I/O
BANK0_PIN24	GPIO0_24	X1-38	I/O
BANK0_PIN26	GPIO0_26	X1-48	I/O
BANK0_PIN27	GPIO0_27	X1-42	I/O
BANK2_PIN09	GPIO2_9	X2-54	I/O
BANK3_PIN06	GPIO3_6	X1-46	I/O

4.2.11 JTAG

The i.MX28 provides two JTAG modes. The mode is defined with the signal DEBUG.
To change the JTAG mode, the default can be changed by a Pull-Down resistor of approximately 1 kΩ at pin DEBUG.
The following table shows the available modes as well as the default mode used on the TQMa28.

Table 35: JTAG modes

Debug	Name	TQMa28 pin	Remark
0	JTAG interface works for boundary scan	X2-16	–
1	**JTAG interface works for ARM® debugging**		**10 kΩ PU to 3.3 V on TQMa28 (default)**

The JTAG signals are directly routed from the CPU to the connector. All necessary Pull-Up and Pull-Down resistors are already assembled on the TQMa28.
The following table shows the signals used for the JTAG interface.

Table 36: JTAG signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
JTAG_TCK	JTAG_TCK	X2-72	I	10 kΩ PU to 3.3 V on TQMa28
JTAG_TMS	JTAG_TMS	X2-71	I	10 kΩ PU to 3.3 V on TQMa28
JTAG_TDI	JTAG_TDI	X2-73	I	10 kΩ PU to 3.3 V on TQMa28
JTAG_TDO	JTAG_TDO	X2-78	O	–
JTAG_TRST	JTAG_TRST#	X2-74	I	10 kΩ PU to 3.3 V on TQMa28
JTAG_RTCK	JTAG_RTCK	X2-76	O	10 kΩ PU to 3.3 V on TQMa28

4.2.12 ADC

The TQMa28 provides eight ADC inputs. All inputs are blocked to GND with 10 nF.
The ADC supports resistive 4- or 5-wire touch screens.
An adequate protection circuit has to be implemented on the carrier board.

Table 37: ADC signals

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	4-wire touch	5-wire touch	Remark
LRADC0	LRADC0	X2-69	AI			–
LRADC1	LRADC1	X2-70	AI			–
LRADC2	LRADC2	X2-67	AI	Touch Right / X+	UL	Upper Left
LRADC3	LRADC3	X2-68	AI	Touch Top / Y+	LL	Lower Left
LRADC4	LRADC4	X2-65	AI	Touch Left / X–	UR	Upper Right
LRADC5	LRADC5	X2-66	AI	Touch Bottom / Y–	LR	Lower Right
LRADC6	LRADC6	X2-63	AI		Common	–
HSADC0	HSADC0	X2-64	AI			High-Speed ADC (not qualified)

4.2.13 Reset

Two sources on the carrier board can be used for a system reset:

- Power-on reset
- RESET# (e.g. reset push button)

The following table describes the Reset signal available at the connector:

Table 38: RESET signal

i.MX28 signal	TQMa28 signal	TQMa28 pin	Dir.	Remark
RESET IN	RESET#	X2-60	I	- 10 kΩ PU to 3.3 V on TQMa28 - Minimum required Low-Time: ≥100 msec

To improve the stability in case of voltage drops an optional supervisor is provided on the TQMa28.
The supervisor monitors the input voltage VCC5V. The supervisor output is connected to the CPU reset input.
The TQMa28 version with supervisor can only be used with systems which are exclusively supplied with 5 V.
The following illustration shows how the supervisor is connected.

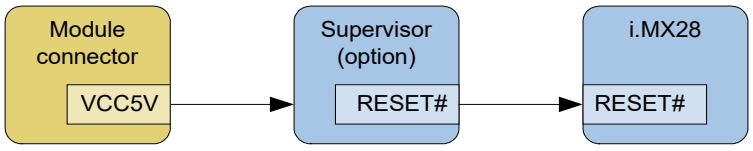


Illustration 6: Optional supervisor, block diagram

The supervisor has the following characteristics:

- Typical threshold voltage: 4.55 V
- Typical delay time: 200 msec

4.2.14 Power supply

4.2.14.1 TQMa28 supply

The TQMa28 works with a single supply of 5 V that must be provided by the carrier board.
Alternatively a lithium-ion battery can supply the TQMa28.
If a lithium-ion battery is connected at the BATTERY pin it is charged if the TQMa28 is supplied with 5 V.
Software settings can be done in the registers HW_LRADC_CONVERSION and HW_POWER_CHARGE.

Attention: Lithium primary batteries and lithium-ion secondary batteries	
	Lithium primary batteries may not be used with the i.MX28 or the TQMa28 (pin BATTERY) because of the CPU's charging function!

The following table shows the permitted supply voltage ranges.

Table 39: Supply voltages

Parameter	Min.	Typ.	Max.	Unit
Supply voltage V_{IN} VCC5V	4.75	5.00	5.25	V
Supply voltage V_{IN} BATTERY	3.10	–	4.20	V

The calculated current consumption (worst case) is 0.4 A. The current consumption strongly depends on component placement, software and wiring options. The values given are to be seen as indicative values.

Table 40: Current consumption

Parameter	V_{IN}	I_{ITYP}
Current consumption in standby	3.3 V	10 mA
	5.0 V	20 mA
Current consumption in Linux idle mode	3.3 V	140 mA
	5.0 V	130 mA
Current consumption in Linux boot mode	3.3 V	230 mA
	5.0 V	240 mA
Current consumption of internal RTC only	>1.3 V	30 µA
Inrush current [4]	5.25 V	1.77 A

4: Peak current for approximately 1.2 µs.

4.2.14.2 Power Management Unit

The i.MX28 has an integrated Power Management Unit (PMU). All voltages required on the TQMa28 are generated by the PMU. The following illustration shows the PMU-internal structure.

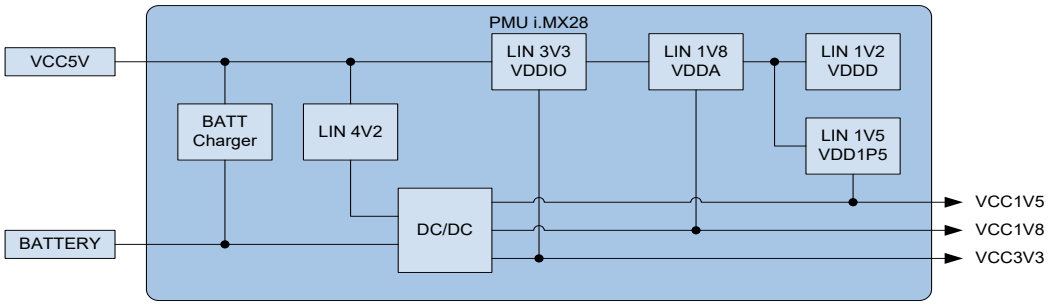


Illustration 7: PMU i.MX28, block diagram

The internal power supply consists of a chain of linear regulators a DC/DC converter and a battery charger.

If the TQMa28 is supplied via VCC5V the processor starts with the voltages generated by its internal linear regulators. During the boot process the linear regulator LIN 4V2 is switched on and supplies the DC/DC converter. From this point the DC/DC converter provides the necessary system voltages instead of the linear regulators. In BATTERY mode the DC/DC converter starts directly.

The i.MX28 provides an extensive set of registers to configure the PMU. Among other things the output voltage levels of all voltage regulators, the brown-out level, the start behaviour, the charging currents, the trigger levels, etc. can be configured.

These registers settings have to be checked or set for the respective design. Further information is to be taken from the NXP Reference Manual (1), the i.MX28 data sheet (2) and the Application Note for the i.MX28 power management (4).

4.2.14.3 Power-up/down

The TQMa28 start behaviour depends on the selected voltage source (VCC5V or BATTERY).

- TQMa28 supply with VCC5V: CPU power-up sequence starts immediately
- TQMa28 supply with BATTERY: CPU power-up sequence only starts when pin PSWITCH is supplied with a voltage between 0.65 V and 1.5 V.

The PSWITCH pin function depends on the applied voltage (see NXP Reference Manual (1)).

In case the function "Fast Falling Edge" is not used (which could be used to power-down the CPU) it is recommended to disable this function using the circuitry suggested by NXP (see Illustration 8).

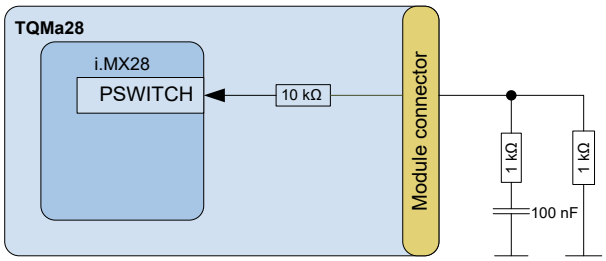


Illustration 8: PSWITCH wiring

Attention: Power-up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed.

5. SOFTWARE

The TQMa28 comes with a preinstalled boot loader. The boot loader and the also available BSP are tailored for the combination of TQMa28 and Starterkit STK-MBa28. More information can be found in the TQMa28 Support Wiki.

The boot loader contains TQMa28-specific as well as carrier-board adaptions as for example

- CPU/PMU configuration
- RAM configuration
- RAM timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strength

These settings have to be adapted if a different boot loader is used. More details can be requested from the TQ-Support.

6. MECHANICS

6.1 General information

Dimensions (L x W):	40 × 26 mm²
Maximum stack height:	Max. 1.5 mm (top side) / typ. 3.75 mm (bottom side)
Mounting holes:	None
Board to board distance:	Selectable by different mating connectors (standard: 5 mm), see also Table 3

The dimensions in the drawing are values without tolerances.

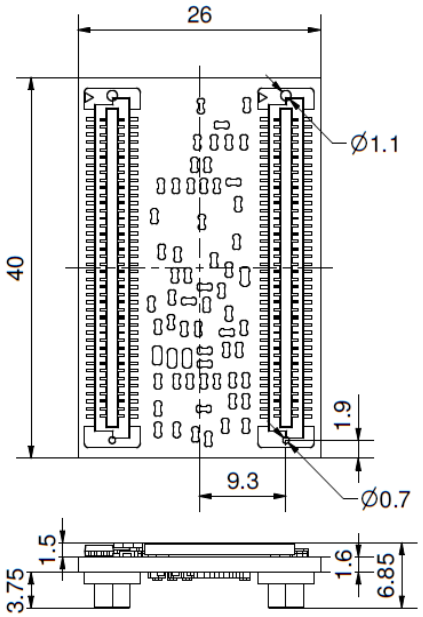


Illustration 9: TQMa28 dimensions, bottom view, side view

6.2 Notes of treatment

To avoid damages caused by mechanical stress, the TQMa28 may only be extracted from the carrier board by using the extraction tool MOZIa28. It can also be obtained separately.

Attention: Note with respect to the component placement of the carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa28 for the extraction tool MOZIa28.

6.3 Component placement

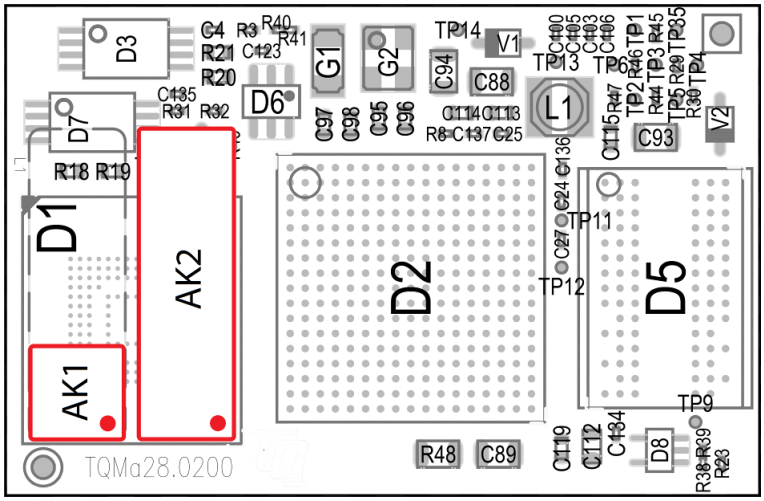


Illustration 10: TQMa28, component placement top

The labels on the TQMa28 show the following information:

Table 41: Labels on TQMa28

Label	Text
AK1	Serial number
AK2	TQMa28 version and revision, tests performed, MAC address (+ additional reserved MAC addresses)

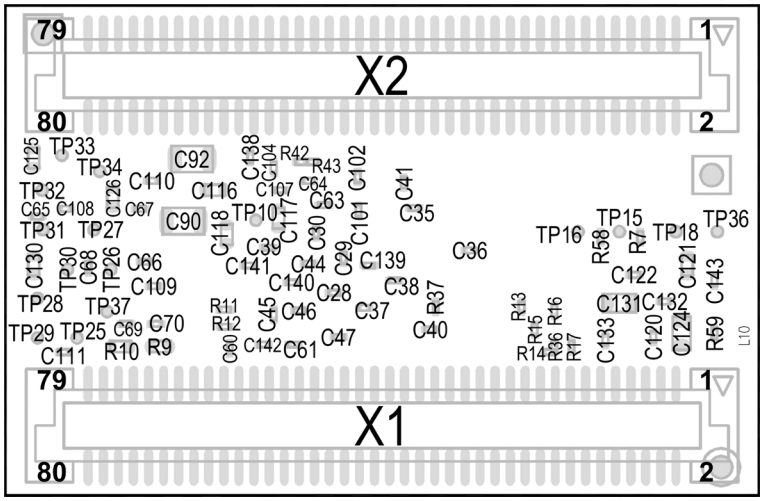


Illustration 11: TQMa28, component placement bottom

6.4 Requirements for the superior system

6.4.1 Protection against external effects

As an embedded module it is not protected against dust, external impact and contact (IP00).
An adequate protection has to be guaranteed by the surrounding system.

6.4.2 Thermal management

Up to 2 W (worst case) have to be dissipated to cool the TQMa28. The power dissipation originates primarily in the processor and in the DDR2 SDRAM. The user is responsible for the removal of this power dissipation in his application.
In most cases a passive cooling should be sufficient.

Attention: Destruction or malfunction!	
	The TQMa28 belongs to a performance category in which a cooling may be required. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX28 must be taken into consideration when connecting the heat sink. The i.MX28 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa28 and thus malfunction, deterioration or destruction.

6.4.3 Structural requirements

The TQMa28 is held in the mating connectors by the retention force of the pins (a total of 160). For high requirements with respect to vibration and shock firmness additional plastic retainers have to be provided in the final product to hold the TQMa28 in its position. As no heavy and big components are used, no further requirements are given.

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMa28 was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the TQMa28.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Reliability and service life

No detailed MTBF calculation has been done for the TQMa28.
The TQMa28 is designed to be insensitive to shock and vibration.
Product life limiting components like electrolyte capacitors were not used.
High quality industrial grade connectors are assembled on the TQMa28.

7.5 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly. In general, a reliable operation is given when following conditions are met:

Table 42: Climate and operating conditions "Commercial temperature range" 0 °C to +70 °C

Parameter	Range	Remark
CPU T_J temperature	–40 °C to +105 °C	Environment: –40 °C to +85 °C
DDR2 SDRAM case temperature	0 °C to +85 °C	–
Other ICs case temperature	0 °C to +70 °C	–
TQMa28 storage temperature	–40 °C to +85 °C	–
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Table 43: Climate and operating conditions "Extended temperature range" –25 °C to +85 °C

Parameter	Range	Remark
CPU T_J temperature	–40 °C to +105 °C	Environment: –40 °C to +85 °C
DDR2 SDRAM case temperature	–40 °C to +95 °C	–
Other ICs case temperature	–25 °C to +85 °C	–
TQMa28 storage temperature	–40 °C to +85 °C	–
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Table 44: Climate and operating conditions "Industrial temperature range" –40 °C to +85 °C

Parameter	Range	Remark
CPU T_J temperature	–40 °C to +105 °C	Environment: –40 °C to +85 °C
DDR2 SDRAM case temperature	–40 °C to +95 °C	Environment: –40 °C to +85 °C
Other ICs case temperature	–40 °C to +85 °C	–
TQMa28 storage temperature	–40 °C to +85 °C	–
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

7.6 Environment protection

7.6.1 RoHS

The TQMa28 is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

7.6.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa28 was designed to be recyclable and easy to repair.

7.6.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.6.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200.000.
Thus the TQMa28 always has to be considered in combination with the complete system.
The compliance regarding EuP directive is basically possible for the TQMa28 on account of the available Standby or Sleep-Modes of the components on the TQMa28.

7.6.5 Battery

No batteries are assembled on the TQMa28.

7.6.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa28, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa28 is delivered in reusable packaging.

7.6.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging.
Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 45: Acronyms

Acronym	Meaning
A/D	Analog/Digital
ADC	Analog/Digital Converter
AI	Analog In
ARM®	Advanced RISC Machine
AUART	Application Universal Asynchronous Receiver/Transmitter
BGA	Ball Grid Array
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR	Double Data Rate
DUART	Debug Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
ESD	Electrostatic Discharge
GND	Ground
GPIO	General Purpose Input/Output
GPMI	General Purpose Media Interface
I	Input
I/O	Input/Output
I²C	Inter-Integrated Circuit
I²S	Inter IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LVTTL	Low Voltage Transistor Transistor Logic
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures
NAND	Not-And
O	Output
OTG	On-The-Go
OTP	One-Time Programmable
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PMU	Power Management Unit
PU	Pull-Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Resistor Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGB	Red Green Blue
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SAIF	Serial Audio Interface
SD	Secure Digital
SD card	Secure Digital Card
SD/MMC	Secure Digital Multimedia Card
SDRAM	Synchronous Dynamic Random Access Memory
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
STK	Starterkit
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 46: Further applicable documents

No.	Description	Rev. / Date	Company
(1)	i.MX28 Applications Processor Reference Manual	2 / Aug. 2013	NXP
(2)	Datasheet i.MX28 Applications Processors for Consumer Products	3 / July 2012	NXP
(3)	Chip Errata for the i.MX28	2 / Sept. 2012	NXP
(4)	Application Note AN4199	1 / Mar. 2013	NXP
(5)	IO Mux tool for the i.MX28	2.0.27.30460	NXP
(6)	MBa28 User's Manual	– current –	TQ-Systems
(7)	TQMa28 pin multiplexing	0100A / 2012	TQ-Systems
(8)	TQMa28-MBa28 Tech Note	– current –	TQ-Systems
(9)	Support-Wiki for the TQMa28	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

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