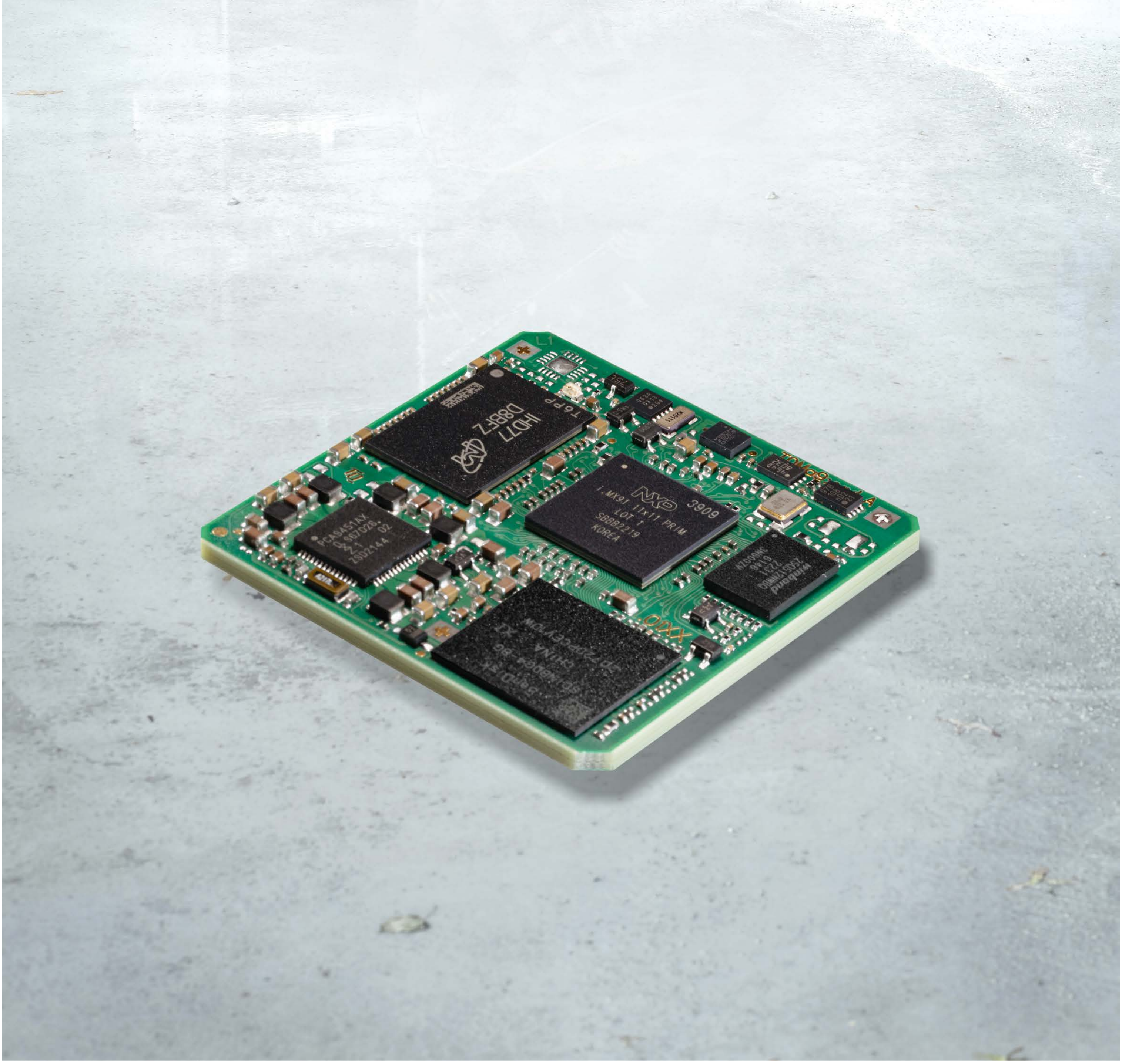
TQMa91xxLA
Preliminary User's Manual

TQMa91xxLA UM 0002
11.03.2024



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	30.11.2023	Kreuzer		First issue
0002	11.03.2024	Kreuzer	Table 14	Corrected

1. ABOUT THIS MANUAL

1.1 Copyright and license expenses

The drivers and utilities for the components used as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Bootloader-licence expenses are paid by TQ-Systems GmbH and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be calculated / declared separately.

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TQ-Systems GmbH explicitly reserves the rights to change or add to the contents of this Preliminary User's Manual or parts of it without special notification.

Important Notice:

Before using the Starterkit MBa91xxCA or parts of the schematics of the MBa91xxCA, you must evaluate it and determine if it is suitable for your intended application. You assume all risks and liability associated with such use. TQ-Systems GmbH makes no other warranties including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose. Except where prohibited by law, TQ-Systems GmbH will not be liable for any indirect, special, incidental or consequential loss or damage arising from the usage of the Starterkit MBa91xxCA or schematics used, regardless of the legal theory asserted.

1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa91xxLA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of.
  They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of.
  The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa91xxCA circuit diagram
- MBa91xxCA User's Manual
- i.MX 91 Data Sheet
- i.MX 91 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa91xxLA (in progress)

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of the TQMa91xxLA as of revision 01xx and the TQMa9xxxLA adapter and refers to some software settings. A certain TQMa91xxLA derivative does not necessarily provide all features described in this Preliminary User's Manual.

This Preliminary User's Manual does neither replace the i.MX 91 Reference Manual (1), nor the i.MX 91 Data Sheet (2), nor any other documents from NXP.

The TQMa91xxLA is a universal Minimodule based on the NXP ARM® Cortex®-A55 based i.MX 91 CPU family, see also Table 4.

2.1 Key functions and characteristics

The TQMa91xxLA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

All essential i.MX 91 signals are routed to the TQMa91xxLA LGA pads. There are therefore no restrictions for customers using the TQMa91xxLA with respect to an integrated customised design. All essential components like CPU, LPDDR4, eMMC, and PMIC are already integrated on the TQMa91xxLA.

The main features of the TQMa91xxLA are:

- 64 bit NXP i.MX 91 CPU, 1 × ARM Cortex®-A55
- Up to 2 Gbyte of LPDDR4 RAM
- Up to 256 Gbyte of eMMC NAND Flash, eMMC standard 5.1
- Up to 256 Mbyte QSPI NOR Flash (optional)
- 64 Kbit EEPROM (optional)
- Temperature sensor + EEPROM
- NXP Power Management Integrated Circuit PCA9451
- RTC (optional)
- Trust Secure Element (optional)
- Gyroscope (optional)
- All essential i.MX 91 signals are routed to the TQMa91xxLA LGA pads
- Single supply voltage 5 V

2.2 CPU block diagram

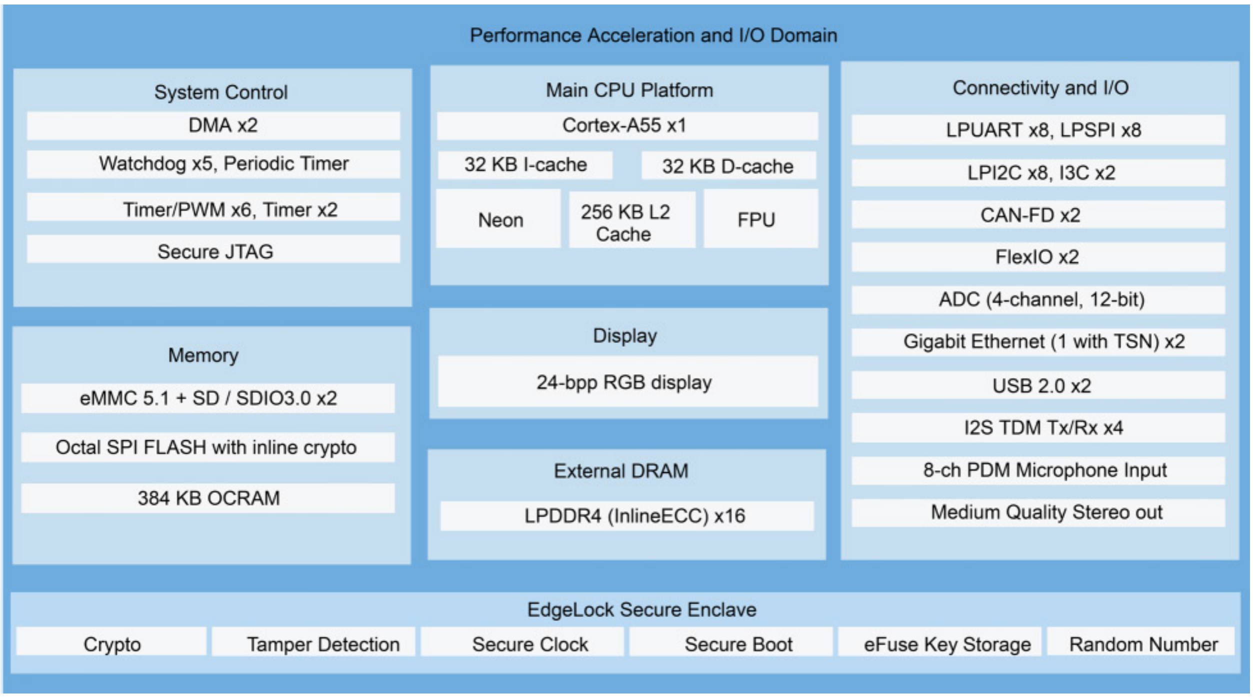

Figure 1: Block diagram i.MX 91
(Source: NXP)

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa91xxLA, and the BSP provided by TQ-Systems GmbH, see also chapter 4.

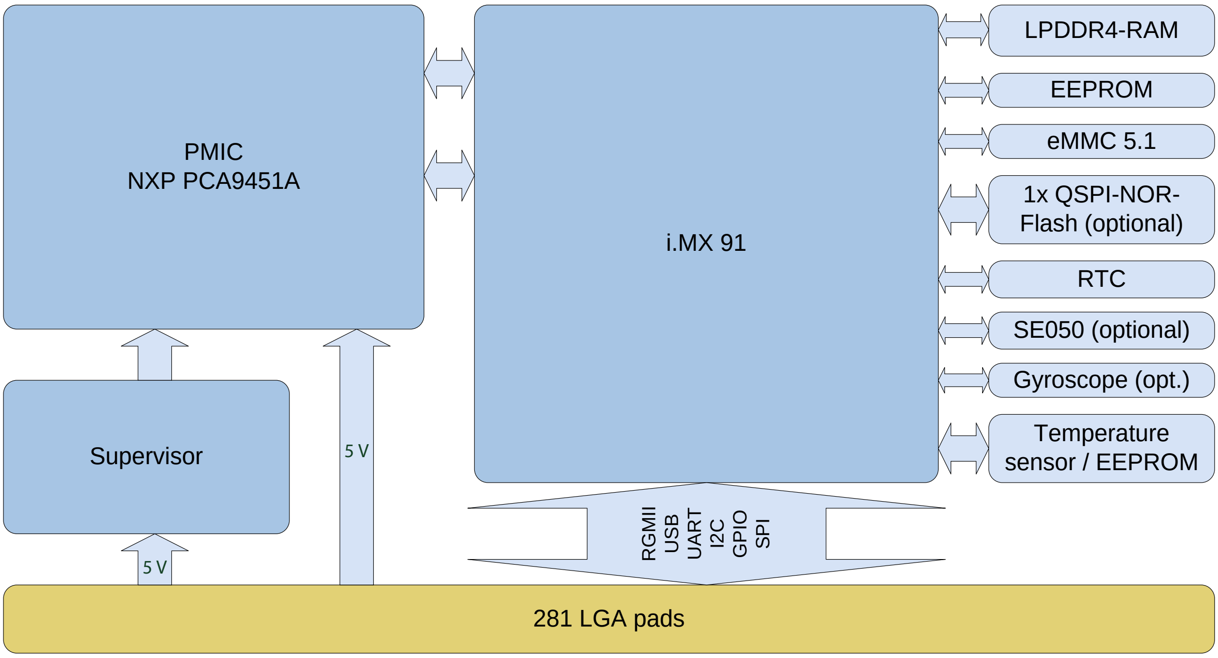

Figure 2: Block diagram TQMa91xxLA (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX 91 internal function units must be taken note of.

The pin assignment in Table 3 refers to a TQMa91xxLA with i.MX 91 CPU in combination with the carrier board MBa91xxCA and the TQMa9xxxLA adapter.

NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).

The electrical and pin characteristics are to be taken from the i.MX 91 and PMIC documentation, see Table 40.

Attention: Destruction or malfunction, pin multiplexing	
	Depending on the configuration, many i.MX 91 pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX 91 Reference Manual (1), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa91xxLA. The descriptions given in the following tables should be taken note of: – DNC: These pins must never be connected and have to be left open. Please contact TQ-Support for details.

3.1.1.1 Pinout TQMa91xxLA

The TQMa91xxLA has a total of 281 LGA pads. The TQMa91xxLA is soldered and thus permanently connected to the carrier board. It is not trivial and it is not recommended to remove the TQMa91xxLA.
The following table shows the TQMa91xxLA pad-out, top view through the TQMa91xxLA.

Table 2: Pinout TQMa91xxLA, top view through TQMa91xxLA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	
19		Ground	DNC	DNC	Ground	DNC	DNC	Ground	DNC	DNC	Ground	DNC	DNC	DNC	DNC	Ground	USB1_DP	USB1_DN		19
18	DNC	DNC	Ground	DNC	DNC	Ground	DNC	DNC	Ground	DNC	DNC	Ground	DNC	DNC	DNC	DNC	Ground	USB2_DP	USB2_DN	18
17	ISO_7816_IO1	Ground	ISO_14443_LB	Ground	DNC	DNC	Ground	DNC	DNC	Ground	DNC	DNC	Ground	USB1_VBUS	Ground	DNC	DNC	Ground	ADC_IN0	17
16	Ground	ISO_14443_LA	Ground	ISO_7816_RST	GPIO1_IO10	Ground	CAN1_RX	CAN1_TX	Ground	Tamper1	Tamper0	Ground	USB1_ID	USB2_ID	Ground	USB2_VBUS	Ground	ADC_IN2	ADC_IN1	16
15	ISO_7816_CLK	ISO_7816_IO2	Ground	V_LICELL	Ground	TEMP_EVENT#	Ground									GPIO1_IO02	CLK1_IN	Ground	ADC_IN3	15
14	Ground	ENET2_MDIO	RFU	Ground	RTC_EVENT#	Ground										CLK2_IN	Ground	QSPI_SCLK	Ground	14
13	ENET2_MDC	ENET2_RD0	RFU	RFU	Ground	RFU										Ground	QSPI_SS0#	QSPI_DATA0	QSPI_DATA2	13
12	ENET2_RD2	ENET2_RD1	RFU	Ground	UART2_RXD	RFU										RFU	QSPI_DATA1	Ground	QSPI_DATA3	12
11	Ground	ENET2_RD3	Ground	UART1_TXD	UART2_TXD	Ground										V_SD2	Ground	GPIO1_IO12	Ground	11
10	ENET2_RXC	Ground	I2C1_SCL	UART1_RXD	Ground	JTAG_TCK										Ground	GPIO1_IO11	GPIO1_IO14	UART2_RTS#	10
9	ENET2_TD0	ENET2_RX_CTL	I2C1_SDA	Ground	JTAG_TDI	JTAG_TMS										UART6_TXD	SPI6_PCS0#	Ground	V_GPIO	9
8	Ground	ENET2_TD1	Ground	RFU	Ground	JTAG_TDO	Ground									UART6_RXD	SPI6_SIN	SPI6_SOUT	SPI6_SCK	8
7	ENET2_TD3	Ground	ENET2_TD2	Ground	RFU	Ground	ONOFF	Ground							Ground	TPM5_CH0	Ground	Ground	Ground	7
6	ENET2_TXC	ENET2_TX_CTL	Ground	Ground	PMIC_RST#	V_3V3_SD	Ground	PMIC_WDOG_IN#	Ground	WDOG_ANY	Ground	RFU	RFU	Ground	GPIO2_IO07	Ground	TPM6_CH0	TPM3_EXTCLK	GPIO2_IO10	6
5	Ground	Ground	Ground	Ground	Ground	Ground	PMIC_SCLH	PMIC_SCLL	RESET_OUT#	Ground	CAN2_RX	CAN2_TX	GPIO2_IO24	I2C5_SDA	Ground	UART8_TXD	UART8_RXD	Ground	GPIO2_IO11	5
4	V_5V_IN	V_5V_IN	V_5V_IN	Ground	Ground	Ground	PMIC_SDAH	PMIC_SDAL	Ground	I2C3_SCL	I2C3_SDA	Ground	SAI3_TXFS	I2C5_SCL	UART3_TXD	UART3_RXD	Ground	SD2_DATA0	Ground	4
3	V_5V_IN	V_5V_IN	V_5V_IN	Ground	Ground	Ground	Ground	ENET1_RD2	ENET1_RX_CTL	Ground	ENET1_TD2	ENET1_TX_CTL	Ground	SAI3_RXFS	SAI3_TXD0	Ground	SD2_DATA2	SD2_DATA1	SD2_CMD	3
2	V_5V_IN	Ground	Ground	GPIO4_IO29	Ground	ENET1_MDIO	ENET1_RD0	Ground	ENET1_RXC	ENET1_TD0	Ground	ENET1_TXC	SAI3_RXD0	Ground	SAI3_RXC	SAI3_TXC	SD2_CD#	Ground	SD2_CLK	2
1		GPIO3_IO26	GPIO3_IO27	CLK3_OUT	Ground	ENET1_MDC	ENET1_RD1	ENET1_RD3	Ground	ENET1_TD1	ENET1_TD3	Ground	V_1V8	V_3V3	Ground	SAI3_MCLK	SD2_RST#	SD2_DATA3		1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	

3.1.1.2 TQMa91xxLA signals

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX 91 documentation (1), (2), (3), as well as the PMIC Data Sheet (4).

Table 3: TQMa91xxLA, signals

TQMa91xxLA pad	Ball name	TQ multiplexing	Group	Dir.	Level	CPU ball	Comment
W17	ADC_IN0	ADC_IN0	ADC	I	1,8 V	B19	
W16	ADC_IN1	ADC_IN1	ADC	I	1,8 V	A20	
V16	ADC_IN2	ADC_IN2	ADC	I	1,8 V	B20	
W15	ADC_IN3	ADC_IN3	ADC	I	1,8 V	B21	
B1	CCM_CLKO1	GPIO3_IO26	GPIO	I/O	1,8 V	AA2	
C1	CCM_CLKO2	GPIO3_IO27	GPIO	I/O	1,8 V	Y3	
D1	CCM_CLKO3	CLK3_OUT	CLK	O	1,8 V	U4	
D2	CCM_CLKO4	GPIO4_IO29	GPIO	I/O	1,8 V	V4	
U15	CLKIN1	CLK1_IN	CLK	I	1,8 V	B17	
T14	CLKIN2	CLK2_IN	CLK	I	1,8 V	A18	
F10	DAP_TCLK_SWCLK	JTAG_TCK	JTAG	O	1,8 V	Y1	
E9	DAP_TDI	JTAG_TDI	JTAG	I	1,8 V	W1	
F8	DAP_TDO_TRACESWO	JTAG_TDO	JTAG	O	1,8 V	Y2	
F9	DAP_TMS_SWDIO	JTAG_TMS	JTAG	I	1,8 V	W2	
F1	ENET1_MDC	ENET_MDC	ENET	O	1,8 V	AA11	
F2	ENET1_MDIO	ENET_MDIO	ENET	I/O	1,8 V	AA10	
G2	ENET1_RD0	ENET_RD0	ENET	I	1,8 V	AA8	
G1	ENET1_RD1	ENET_RD1	ENET	I	1,8 V	Y9	
H3	ENET1_RD2	ENET_RD2	ENET	I	1,8 V	AA9	
H1	ENET1_RD3	ENET_RD3	ENET	I	1,8 V	Y10	
J3	ENET1_RX_CTL	ENET_RX_CTL	ENET	I	1,8 V	Y8	
J2	ENET1_RXC	ENET_RXC	ENET	I	1,8 V	AA7	
K2	ENET1_TD0	ENET_TD0	ENET	O	1,8 V	W11	
K1	ENET1_TD1	ENET_TD1	ENET	O	1,8 V	T12	
L3	ENET1_TD2	ENET_TD2	ENET	O	1,8 V	U12	
L1	ENET1_TD3	ENET_TD3	ENET	O	1,8 V	V12	
M3	ENET1_TX_CTL	ENET_TX_CTL	ENET	O	1,8 V	V10	
M2	ENET1_TXC	ENET_TXC	ENET	O	1,8 V	U10	
A13	ENET2_MDC	ENET2_MDC	ENET	O	1,8 V	Y7	
B14	ENET2_MDIO	ENET2_MDIO	ENET	I/O	1,8 V	AA6	
B13	ENET2_RD0	ENET2_RD0	ENET	I	1,8 V	AA4	
B12	ENET2_RD1	ENET2_RD1	ENET	I	1,8 V	Y5	
A12	ENET2_RD2	ENET2_RD2	ENET	I	1,8 V	AA5	
B11	ENET2_RD3	ENET2_RD3	ENET	I	1,8 V	Y6	
B9	ENET2_RX_CTL	ENET2_RX_CTL	ENET	I	1,8 V	Y4	
A10	ENET2_RXC	ENET2_RXC	ENET	I	1,8 V	AA3	
A9	ENET2_TD0	ENET2_TD0	ENET	O	1,8 V	T8	
B8	ENET2_TD1	ENET2_TD1	ENET	O	1,8 V	U8	
C7	ENET2_TD2	ENET2_TD2	ENET	O	1,8 V	V8	
A7	ENET2_TD3	ENET2_TD3	ENET	O	1,8 V	T10	
B6	ENET2_TX_CTL	ENET2_TX_CTL	ENET	O	1,8 V	V6	
A6	ENET2_TXC	ENET2_TXC	ENET	O	1,8 V	U6	

3.1.1.2 TQMa91xxLA signals (continued)

Table 3: TQMa91xxLA, signals (continued)

TQMa91xxLA pad	Ball name	TQ multiplexing	Group	Dir.	Level	CPU ball	Comment
U9	GPIO_IO00	SPI6_PCS0#	SPI	O	V_GPIO	J21	
U8	GPIO_IO01	SPI6_SIN	SPI	I	V_GPIO	J20	
V8	GPIO_IO02	SPI6_SOUT	SPI	O	V_GPIO	K20	
W8	GPIO_IO03	SPI6_SCK	SPI	O	V_GPIO	K21	
T9	GPIO_IO04	UART6_TXD	UART	O	V_GPIO	L17	
T8	GPIO_IO05	UART6_RXD	UART	I	V_GPIO	L18	
T7	GPIO_IO06	TPM5_CH0	TPM	O	V_GPIO	L20	
R6	GPIO_IO07	GPIO2_IO07	GPIO	I/O	V_GPIO	L21	
U6	GPIO_IO08	TPM6_CH0	TPM	O	V_GPIO	M20	
V6	GPIO_IO09	TPM3_EXTCLK	TPM	I	V_GPIO	M21	
W6	GPIO_IO10	GPIO2_IO10	GPIO	I/O	V_GPIO	N17	
W5	GPIO_IO11	GPIO2_IO11	GPIO	I/O	V_GPIO	N18	
T5	GPIO_IO12	UART8_TXD	UART	O	V_GPIO	N20	
U5	GPIO_IO13	UART8_RXD	UART	I	V_GPIO	N21	
R4	GPIO_IO14	UART3_TXD	UART	O	V_GPIO	P20	
T4	GPIO_IO15	UART3_RXD	UART	I	V_GPIO	P21	
T2	GPIO_IO16	SAI3_TXC	SAI	O	V_GPIO	R21	
T1	GPIO_IO17	SAI3_MCLK	SAI	O	V_GPIO	R20	
R2	GPIO_IO18	SAI3_RXC	SAI	I	V_GPIO	R18	
P3	GPIO_IO19	SAI3_RXFS	SAI	I	V_GPIO	R17	
N2	GPIO_IO20	SAI3_RXD0	SAI	I	V_GPIO	T20	
R3	GPIO_IO21	SAI3_TXD0	SAI	O	V_GPIO	T21	
P5	GPIO_IO22	I2C5_SDA	I2C	I/O	V_GPIO	U18	Need external pull-ups if used as I2C5
P4	GPIO_IO23	I2C5_SCL	I2C	O	V_GPIO	U20	Need external pull-ups if used as I2C5
N5	GPIO_IO24	GPIO2_IO24	GPIO	I/O	V_GPIO	U21	
M5	GPIO_IO25	CAN2_TX	CAN	O	V_GPIO	V21	
N4	GPIO_IO26	SAI3_TXFS	SAI	O	V_GPIO	V20	
L5	GPIO_IO27	CAN2_RX	CAN	I	V_GPIO	W21	
L4	GPIO_IO28	I2C3_SDA	I2C	I/O	V_GPIO	W20	Need external pull-ups if used as I2C3
K4	GPIO_IO29	I2C3_SCL	I2C	O	V_GPIO	Y21	Need external pull-ups if used as I2C3
C10	I2C1_SCL	I2C1_SCL	I2C	O	3,3 V	C20	
C9	I2C1_SDA	I2C1_SDA	I2C	I/O	3,3 V	C21	
T15	I2C2_SCL	GPIO1_IO02	GPIO	I/O	3,3 V	D20	
B16	ISO_14443_LA	ISO_14443_LA	ISO_14443	I/O	3,3 V	-	
C17	ISO_14443_LB	ISO_14443_LB	ISO_14443	I/O	3,3 V	-	
A15	ISO_7816_CLK	ISO_7816_CLK	ISO_7816	I	3,3 V	-	
A17	ISO_7816_IO1	ISO_7816_IO1	ISO_7816	I/O	3,3 V	-	
B15	ISO_7816_IO2	ISO_7816_IO2	ISO_7816	I/O	3,3 V	-	
D16	ISO_7816_RST_N	ISO_7816_RST	ISO_7816	I	3,3 V	-	
G7	ONOFF	ONOFF	Config	I	1,8 V	A19	
G16	PDM_BIT_STREAM0	CAN1_RX	CAN	I	3,3 V	J17	
E16	PDM_BIT_STREAM1	GPIO1_IO10	GPIO	I/O	3,3 V	G18	
H16	PDM_CLK	CAN1_TX	CAN	O	3,3 V	G17	
E6	PMIC_RST_B	PMIC_RST#	Config	I	1,8 V	-	
J5	RESET_OUT#	RESET_OUT#	Config	O	OD	-	Open-Drain (up to 5,5 V)
E14	RTC_EVENT#	RTC_EVENT#	Config	O	OD	-	Open-Drain (0,7 V to 5,5 V)

3.1.1.2 TQMa91xxLA signals (continued)

Table 3: TQMa91xxLA, signals (continued)

TQMa91xxLA pad	Ball name	TQ multiplexing	Group	Dir.	Level	CPU ball	Comment
V10	SAI1_RXD0	GPIO1_IO14	GPIO	I/O	3,3 V	H20	
V11	SAI1_TXC	GPIO1_IO12	GPIO	I/O	3,3 V	G20	
W10	SAI1_TXD0	UART2_RTS#	UART	O	3,3 V	H21	Used as BOOT_MODE3 at startup
U10	SAI1_TXFS	GPIO1_IO11	GPIO	I/O	3,3 V	G21	Used as BOOT_MODE2 at startup
G5	SCLH	PMIC_SCLH	LVLTRL	I/O	3,3 V	-	
H5	SCLL	PMIC_SCLL	LVLTRL	I/O	1,8 V	-	
U2	SD2_CD_B	SD2_CD#	SD	I	1,8 / 3,3 V	Y17	
W2	SD2_CLK	SD2_CLK	SD	O	1,8 / 3,3 V	AA19	
W3	SD2_CMD	SD2_CMD	SD	I/O	1,8 / 3,3 V	Y19	
V4	SD2_DATA0	SD2_DATA0	SD	I/O	1,8 / 3,3 V	Y18	
V3	SD2_DATA1	SD2_DATA1	SD	I/O	1,8 / 3,3 V	AA18	
U3	SD2_DATA2	SD2_DATA2	SD	I/O	1,8 / 3,3 V	Y20	
V1	SD2_DATA3	SD2_DATA3	SD	I/O	1,8 / 3,3 V	AA20	
U1	SD2_RST_B	SD2_RST#	SD	O	1,8 / 3,3 V	AA17	
V14	SD3_CLK	QSPI_SCLK	QSPI	O	1,8 V	V16	
U13	SD3_CMD	QSPI_SS0#	QSPI	O	1,8 V	U16	
V13	SD3_DATA0	QSPI_DATA0	QSPI	I/O	1,8 V	T16	
U12	SD3_DATA1	QSPI_DATA1	QSPI	I/O	1,8 V	V14	
W13	SD3_DATA2	QSPI_DATA2	QSPI	I/O	1,8 V	U14	
W12	SD3_DATA3	QSPI_DATA3	QSPI	I/O	1,8 V	T14	
G4	SDAH	PMIC_SDAH	LVLTRL	I/O	3,3 V	-	
H4	SDAL	PMIC_SDAL	LVLTRL	I/O	1,8 V	-	
L16	TAMPER0	TAMPER0	Tamper	I/O	1,8 V	B16	
K16	TAMPER1	TAMPER1	Tamper	I/O	1,8 V	F14	
F15	TEMP_EVENT#	TEMP_EVENT#	Config	O	OD	-	Open-Drain (0,9 V to 3,6 V)
D10	UART1_RXD	UART1_RXD	UART	I	3,3 V	E21	
D11	UART1_TXD	UART1_TXD	UART	O	3,3 V	E21	Used as BOOT_MODE0 at startup.
E12	UART2_RXD	UART2_RXD	UART	I	3,3 V	F20	
E11	UART2_TXD	UART2_TXD	UART	O	3,3 V	F21	Used as BOOT_MODE1 at startup.
L16	TAMPER0	TAMPER0	Tamper	I/O	1,8 V	B16	
K16	TAMPER1	TAMPER1	Tamper	I/O	1,8 V	F14	
F15	TEMP_EVENT#	TEMP_EVENT#	Config	O	OD	-	Open-Drain (0,9 V to 3,6 V)
D10	UART1_RXD	UART1_RXD	UART	I	3,3 V	E21	
D11	UART1_TXD	UART1_TXD	UART	O	3,3 V	E21	Used as BOOT_MODE0 at startup.
E12	UART2_RXD	UART2_RXD	UART	I	3,3 V	F20	
E11	UART2_TXD	UART2_TXD	UART	O	3,3 V	F21	Used as BOOT_MODE1 at startup.

3.1.1.2 TQMa91xxLA signals (continued)

Table 3: TQMa91xxLA, signals (continued)

TQMa91xxLA pad	Ball name	TQ multiplexing	Group	Dir.	Level	CPU ball	Comment
V19	USB1_D_N	USB1_DN	USB	I/O	3,3 V	A14	
U19	USB1_D_P	USB1_DP	USB	I/O	3,3 V	B14	
N16	USB1_ID	USB1_ID	USB	I	1,8 V	C11	
P17	USB1_VBUS	USB1_VBUS	USB	P	5 V	F12	
W18	USB2_D_N	USB2_DN	USB	I/O	3,3 V	A15	
V18	USB2_D_P	USB2_DP	USB	I/O	3,3 V	B15	
P16	USB2_ID	USB2_ID	USB	I	1,8 V	E12	
T16	USB2_VBUS	USB2_VBUS	USB	P	5 V	E14	
K6	WDOG_ANY	WDOG_ANY	GPIO	O	3,3 V	J18	
H6	WDOG_B	PMIC_WDOG_IN#	Config	I	3,3 V	-	
M6, N6, E7, D8, C12, F12, T12, C13, D13, F13, C14	-	**RFU**	-	-	-	-	Reserved for future use
E17, F17, H17, J17, L17, M17, T17, U17, A18, B18, D18, E18, G18, H18, K18, L18, N18, P18, R18, T18, C19, D19, G19, J19, K19, M19, N19, P19, R19		**DNC**	-	-	-	-	Do not connect
N1	V_1V8	V_1V8	Power	P	1,8 V	-	Power-Output (max. 500 mA)
P1	V_3V3	V_3V3	Power	P	3,3 V	-	Power-Output (max. 500 mA)
F6	V_3V3_SD	V_3V3_SD	Power	P	3,3 V	-	Power-Output (max. 400 mA)
A2	V_5V_IN	V_5V_IN	Power	P	5 V	-	Power-Input
A3	V_5V_IN	V_5V_IN	Power	P	5 V	-	Power-Input
B3	V_5V_IN	V_5V_IN	Power	P	5 V	-	Power-Input
C3	V_5V_IN	V_5V_IN	Power	P	5 V	-	Power-Input
A4	V_5V_IN	V_5V_IN	Power	P	5 V	-	Power-Input
B4	V_5V_IN	V_5V_IN	Power	P	5 V	-	Power-Input
C4	V_5V_IN	V_5V_IN	Power	P	5 V	-	Power-Input
W9	V_GPIO	V_GPIO	Power	P	1,8 / 3,3 V	N15, N16	Power-Input
D15	V_LICELL	V_LICELL	Power	P	3 V	-	Power-Input
T11	V_SD2	V_SD2	Power	P	1,8 / 3,3 V	-	Power-Output (max. 75 mA)
E1, J1, M1, R1, B2, C2, E2, H2, L2, P2,V2, D3, E3, F3, G3, K3,N3, T3, D4, E4, F4, J4, M4, U4, W4, A5, B5, C5, D5, E5, F5, K5, R5, V5, C6, D6, G6, J6, L6, P6, T6, B7, D7, F7, H7, R7, U7, V7, W7, A8, C8, E8, G8, D9, V9, B10, E10, T10, A11, C11, F11, U11, W11, D12, V12, E13, T13, A14, D14, F14, U14, W14,C15, E15, G15, V15, A16, C16, F16, J16, M16, R16, U16, B17, D17, G17, K17, N17, R17, V17, C18, F18, J18, M18, U18, B19, E19, H19, L19, T19		Ground	Power	P	0 V	-	
A1, W1, J7, K7, L7, M7, N7, P7, H8, J8, K8, L8, M8, N8, P8, R8, G9, H9, J9, K9, L9, M9, N9, P9, R9, G10, H10, J10, K10, L10, M10, N10, P10, R10, G11, H11, J11, K11, L11, M11, N11, P11, R11, G12, H12, J12, K12, L12, M12, N12, P12, R12, G13, H13, J13, K13, L13, M13, N13, P13, R13, G14, H14, J14, K14, L14, M14, N14, P14, R14, H15, J15, K15, L15, M15, N15, P15, R15, A19, W19		Not available	-	-	-	-	Not available

3.2 System components

3.2.1 i.MX 91

3.2.1.1 i.MX 91 derivatives

Depending on the TQMa91xxLA version, one of the following i.MX 91 derivatives is assembled.

Table 4: i.MX 91 derivatives

TQMa91xxLA version	i.MX 91 derivative	i.MX 91 clocks	Temperature range
TQMa91x1LA	i.MX 91x1	1 x A55: 1.4 GHz	–25 °C … +85 °C
TBD	TBD	TBD	TBD

3.2.1.2 i.MX 91 errata

Attention: Destruction or malfunction, i.MX 91 errata	
	Please take note of the current i.MX 91 errata (5).

3.2.1.3 Boot modes

The i.MX 91 has a ROM with integrated boot loader. After the release of PMIC_POR# the System Controller (SCU) boots from the internal ROM and then loads the program image from the selected boot device. For example, the integrated eMMC or the optional QSPI NOR Flash can be selected as the default boot device. The following boot sources are supported by TQMa91xxLA:

- eMMC (SD1)
- QSPI/FlexSPI NOR Flash (SD1 + SD3)
- SD card (SD2)
- Serial Download (USB1)

Alternatively, an image can be loaded into the internal RAM using the serial downloader.
More information about the boot flow can be found in the Reference Manual (1), and the Data Sheet (2) of i.MX 91.

3.2.1.4 Boot configuration

This section provides information on boot mode configuration pads allocation and boot device interface allocation. The i.MX 91 uses four BOOT_MODE signals provided on the TQMa91xxLA's LGA pads. These require pull-up/pull-down (4.7 kΩ/ 100 kΩ) wiring to 3.3 V and Ground. However, the BOOT_MODE signals are not dedicated to this function, but have other functionalities in normal operation. The boot mode is initialized by sampling the BOOT_MODE[3:0] inputs when the reset is deactivated and are to be set high or low according to the desired boot source at the time of readout. After these inputs are sampled, their subsequent state does not affect the contents of the BOOT_MODE internal register.

The exact boot source configuration can be seen in the following table.

Table 5: Boot configuration i.MX 91

Boot source	Boot Core	BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0
Boot from eFuse	A55	0	0	0	0
Serial Downloader (USB1)		0	0	0	1
Boot from eMMC 5.1 (USDHC1, 8-bit))		0	0	1	0
Boot from SD 3.0 card (USDHC2, 4-bit)		0	0	1	1
Boot from FlexSPI Serial NOR		0	1	0	0
Boot from FlexSPI NAND 2K (not supported)		0	1	0	1

3.2.2 Memory

3.2.2.1 LPDDR4 SDRAM

The memory interface of the i.MX 91 supports LPDDR4 memory (16 bit bus) with a maximum clock rate of 1200 MHz, which meets JEDEC LPDDR4-2400 standard. 1 GByte is the standard configuration, a maximum of 2 Gbyte of LPDDR4 SDRAM is supported.

3.2.2.2 eMMC

An eMMC is provided on the TQMa91xxLA for boot loader, operating system and application software. It is connected to the i.MX 91 via SD1-interface. A maximum transfer rate of 400 MB/s is supported (HS400 mode). Resets have to be done via software.

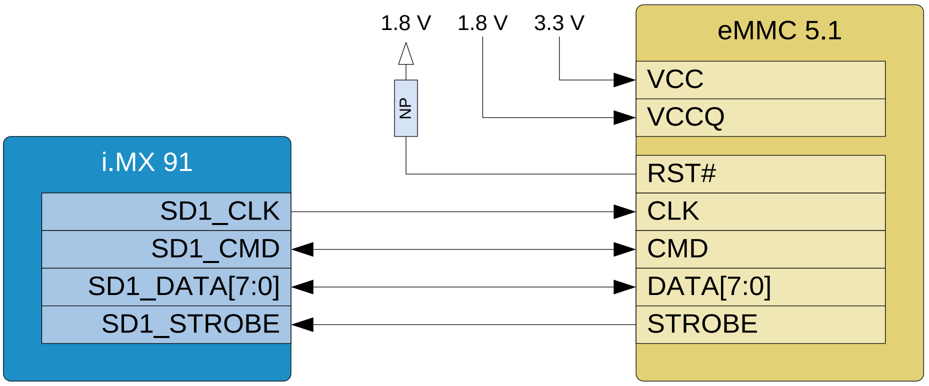

Figure 3: Block diagram eMMC

The boot configuration is described in chapter 3.2.1.3

3.2.2.3 QSPI NOR Flash / NAND Flash

QSPI NOR flash can optionally be assembled on the TQMa91xxLA. Because a separation of the signal paths is not possible, these LGA pads must not be wired when equipped with NOR Flash. With unpopulated NOR Flash the signals of the SD3 interface can be used outside the module.
The NOR flash signals use a part of the NAND pins of the i.MX 91. All other NAND pins of the i.MX 91 are used from the TQMa91xxLA for the eMMC as SD1 boot source and for the SD-Card (SD2).

Table 6: QSPI signals

Signal	i.MX 91	TQMa91xxLA	Power group
QSPI_DATA0	T16	V13	1.8 V
QSPI_DATA1	V14	U12	
QSPI_DATA2	U14	W13	
QSPI_DATA3	T14	W12	
QSPI_SCLK	V16	V14	
QSPI_SS0#	U16	U13	

3.2.2.4 EEPROM M24C64-D

A 64 Kbit EEPROM is assembled by default on the TQMa91xxLA. The serial EEPROM is controlled by the I2C1 bus. The M24C64-D offers an additional page, named the Identification Page (32 Byte). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

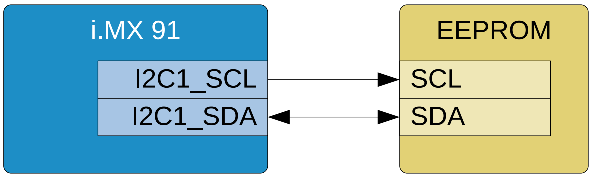

Figure 4: Block diagram EEPROM

- The EEPROM has I²C address `0x57 / 101 0111b`
- Identification Page (32 Byte) `0x5F / 101 1111b`

3.2.2.5 EEPROM with temperature sensor SE97BTP

A serial EEPROM including temperature sensor type SE97BTP, controlled by the I2C1 bus, is assembled on the TQMa91xxLA.
The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write-Protected mode (PWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage.
The overtemperature output of the SE97BTP is connected as open drain to TQMa91xxLA LGA pad F15 (TEMP_EVENT#). The device is assembled on the top side of the TQMa91xxLA (component D6).

The device provides the following I2C addresses:

- EEPROM (Normal Mode): `0x53 / 101 0011b`
- EEPROM (Protection Mode): `0x33 / 011 0011b`
- Temperature sensor: `0x1B / 001 1011b`

3.2.3 Trust Secure Element SE050

An NXP Trust Secure Element SE050 is available on the TQMa91xxLA as an assembly option.

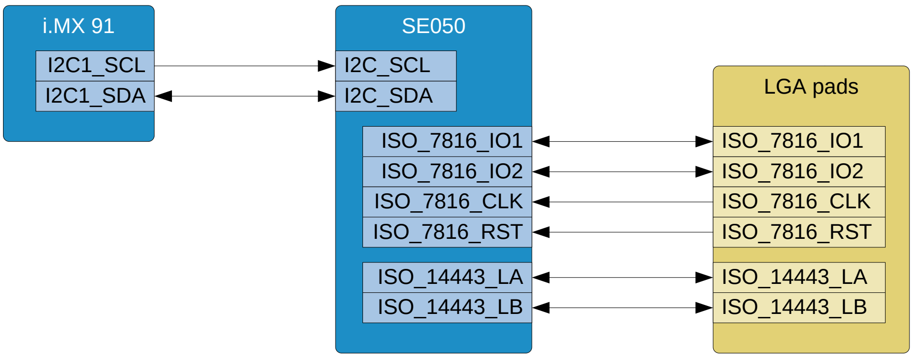

Figure 5: Block diagram SE050

When equipped, the chip provides two interfaces according to ISO 7816 and ISO 14443. Among other things, antennas can be connected to these.

Table 7: ISO_7816 and ISO_14443 signals

Signal	Direction	TQMa91xxLA	Remark
ISO_7816_CLK	I	A15	Only with populated Trust Secure Element
ISO_7816_RST	I	D16	
ISO_7816_IO1	I/O	A17	
ISO_7816_IO2	I/O	B15	
ISO_14443_LA	I/O	B16	
ISO_14443_LB	I/O	C17	

The SE050 is controlled by the I2C1 bus. More details can be found in (8).

- The Trust Secure Element has I^2C address `0x48 / 100 1000b`

3.2.4 Accelerometer/Gyroscope

As an optional extension a 3D Digital Accelerometer / 3D Digital Gyroscope (ISM330DHCX from STMicroelectronics) is provided on theTQMa91xxLA, which has an I^2C interface. It allows to determine the position of the module and provides two interrupts. However, these are not routed to the outside.

- The Accelerometer/Gyroscope has I^2C address `0x6A / 110 1010b`

3.2.5 RTC

The TQMa91xxLA can use the internal Real Time Clock of the i.MX 91 or can be provided with an optional discrete RTC PCF85063A.

3.2.5.1 i.MX 91 internal RTC

The i.MX 91 provides an internal RTC, which has its own power domain, supplied by the PMIC. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

Note: RTC power supply	
	The CPU internal RTC can be used in regular operation. If the TQMa91xxLA supply (5 V) fails, it is no longer available, since the i.MX 91 power rail is no longer supplied.

3.2.5.2 Discrete RTC PCF85063A

In addition to the i.MX 91 internal RTC the TQMa91xxLA provides a discrete RTC PCF85063A as an assembly option, which is controlled by the I2C1 bus. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

The discrete RTC has an interrupt output which provides the open-drain signal RTC_EVENT# at LGA pad E14. This pad requires a pull-up to 3.3 V (maximum 3.6 V) on the carrier board.

The RTC PCF85063A is only directly supplied by V_LICELL when the PMIC or the TQMa91xxLA supply is switched off.

During normal operation of the TQMa91xxLA, the PMIC supplies 3.3 V. To prevent charging a non-rechargeable backup supply, a diode on the baseboard is needed for V_LICELL.

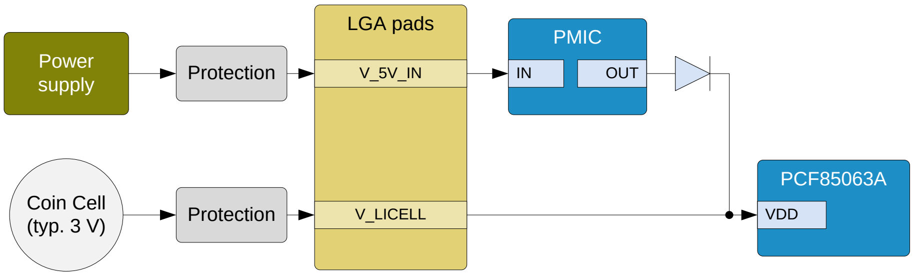

Figure 6: Block diagram RTC supply (TQMa91xxLA with discrete RTC)

- The discrete RTC has I2C address `0x51 / 101 0001b`

Note: RTC power supply	
⚠	The BBSM functions of the i.MX 91 can only be used if the TQMa91xxLA is supplied with 5 V. Because the BBSM rail is not supplied when the TQMa91xxLA is not powered-up, we recommend using the optional RTC PCF85063A.

3.2.6 Interfaces

3.2.6.1 Overview

Except for the internal interfaces, all functional pins of the i.MX 91 are routed to TQMa91xxLA LGA pads. Each customer must check the suitability of the multiplexing in the respective project and adapt it if necessary. The following table shows one exemplary multiplexing with the TQMa91xxLA to utilize the most primary interfaces simultaneously:

Table 8: TQMa91xxLA interfaces

i.MX 91 Interface	Quantity	Remark
Internal interfaces		
LPDDR4	1	LPDDR4, x16
SD3 (QSPI)	1	
SD1 (eMMC)	1	8 bit (HS400)
External interfaces		
ADC	1	4 x inputs
CAN	2	
GPIO	6	
I2C	3	1 x for internal components, 2x for other peripherals
JTAG	1	
RGMII	2	
SAI (Audio)	1	
SPI	2	1 x CS each (2x CS possible with omission of GPIOs)
SmartCard ISO14443 / ISO7816	1	optionally provided by TSE
TAMPER	2	
UART	5	1 x incl. RTS/CTS
USB 2.0	2	
SD2 (SD-Card)	1	4 bit

3.2.6.2 ADC

The i.MX 91 has a 12-bit analog-digital converter with a reference voltage of 1.8 V and max. 4 channels.

Figure 7: Block diagram ADC

The reference voltage is provided on the module by the PMIC and is additionally filtered. The supply of an external reference voltage is not provided.

Table 9: Pin assignment ADC

Signal	i.MX 91	TQMa91xxLA	Power group
ADC_IN0	B19	W17	VDD_ANA_1P8 (1.8 V)
ADC_IN1	A20	W16	
ADC_IN2	B20	V16	
ADC_IN3	B21	W15	

3.2.6.3 CAN FD

The i.MX 91 provides two CAN FD interfaces. Both are specified according to the CAN 2.0B protocol but have different electrical properties due to their multiplexing. CAN1 has a 3.3 V level. The levels of CAN2 are dependent on the voltage V_GPIO which is set via LGA pad W9.

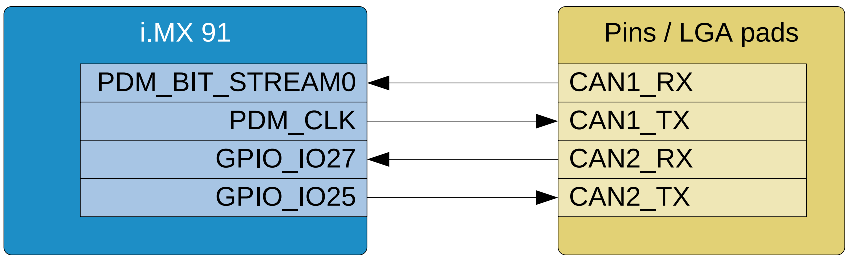

Figure 8: Block diagram CAN

Table 10: CAN FD signals

Signal	i.MX 91	TQMa91xxLA	Power group
CAN1_TX	G17	H16	NVCC_AON (3.3 V)
CAN1_RX	J17	G16	
CAN2_TX	V21	M5	NVCC_GPIO (1.8 V / 3.3 V)
CAN2_RX	W21	L5	

3.2.6.4 Ethernet / RGMII

The i.MX 91 has two Ethernet MACs, each operating in maximum Gigabit full-duplex mode. MII, RMII or RGMII can be used as interfaces, the latter being used for standard multiplexing. Each MAC unit has its own MDIO/SMI interface. ENET1 supports both QOS (Quality-of-Service) and TSN (Time-sensitive Network).

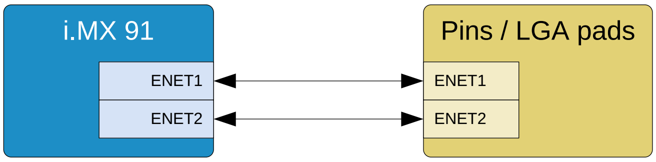

Figure 9: Block diagram RGMII

For RGMII an IO voltage of 1.8 V and for RMII an IO voltage of either 1.8 V or 3.3 V is specified. Due to an operation of both modes with 1.8 V the rail NVCC_WAKEUP is set to 1.8 V. The signals are length matched on the TQMa91xxLA and routed with a differential impedance of 100 Ω. On the carrier board, they have to be connected according to RGMII specifications.

The following table shows the signals used in RGMII mode.

Table 11: ENET signals in RGMII mode

Signal	i.MX 91	TQMa91xxLA	Power group
ENET1_RX_CTL	Y8	J3	NVCC_WAKEUP (1.8 V)
ENET1_RXC	AA7	J2	
ENET1_RD0	AA8	G2	
ENET1_RD1	Y9	G1	
ENET1_RD2	AA9	H3	
ENET1_RD3	Y10	H1	
ENET1_TX_CTL	V10	M3	
ENET1_TXC	U10	M2	
ENET1_TD0	W11	K2	
ENET1_TD1	T12	K1	
ENET1_TD2	U12	L3	
ENET1_TD3	V12	L1	
ENET1_MDC	AA11	F1	
ENET1_MDIO	AA10	F2	
ENET2_RX_CTL	Y4	A9	
ENET2_RXC	AA3	F10	
ENET2_RD0	AA4	B13	
ENET2_RD1	Y5	B12	
ENET2_RD2	AA5	A12	
ENET2_RD3	Y6	B11	
ENET2_TX_CTL	V6	B6	
ENET2_TXC	U6	A6	
ENET2_TD0	T8	T8	
ENET2_TD1	U8	B8	
ENET2_TD2	V8	C7	
ENET2_TD3	T10	A7	
ENET2_MDC	Y7	A13	
ENET2_MDIO	AA6	B14	

3.2.6.5 I²C

The i.MX 91 provides up to eight I²C interfaces. I2C1 serves as system bus for internal components (RTC, EEPROM, temperature sensor, TSE, gyroscope and PMIC), has pull-ups on the module and is additionally available at LGA pads.

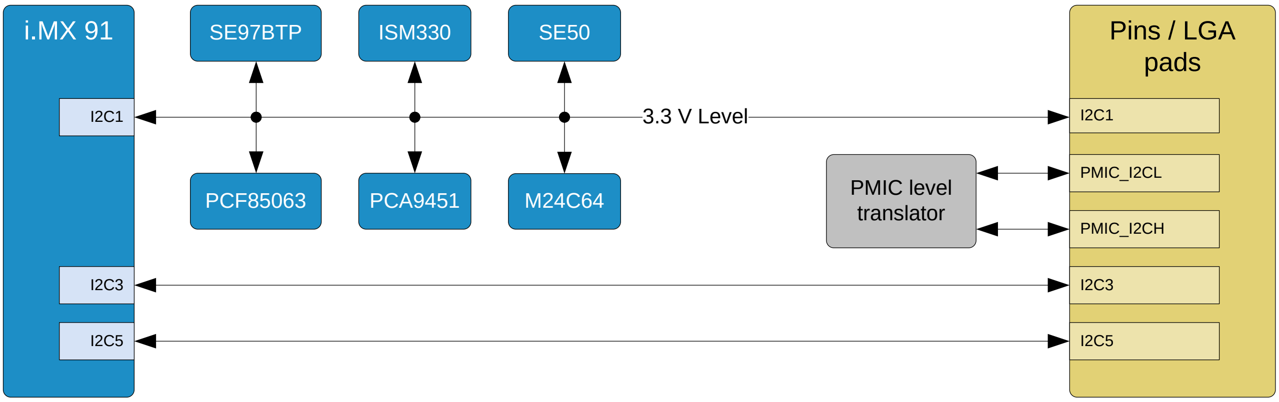

Figure 10: Block diagram I²C

I2C3 and I2C5 are provided as further buses, but without wiring on the TQMa91xxLA. Voltage levels and pull-up resistors are to be defined or placed outside the module.
The PMIC PCA9451 additionally provides an integrated I2C level translator. It is connected to four LGA pads and can thus be used in customer designs. The corresponding wiring by means of pull-ups is to be provided outside TQMa91xxLA.
The TQMa91xxLA internal components with their associated addresses are listed in the following table.

Table 12: Address assignment I2C1 bus

Component	Function		7-bit address
PCA9451	PMIC		0x25 / 010 0101b
M24C64	EEPROM	Memory array	0x57 / 101 0111b
		Identification page (32 Byte)	0x5F / 101 1111b
PCF85063A	RTC		0x51 / 101 0001b
SE97BTP	EEPROM	Read / Write	0x53 / 101 0011b
		Protection command	0x33 / 011 0011b
	Temperature sensor in EEPROM		0x1B / 001 1011b
SE050 (optional)	Trust Secure Element		0x48 / 100 1000b
ISM330 (optional)	Gyroscope		0x6A / 110 1010b

The following table shows the I²C pin assignment on the TQMa91xxLA.

Table 13: Pin assignment I²C

Signal	i.MX 91	TQMa91xxLA	Power group
I2C1_SCL	C20	A10	NVCC_AON (3.3 V)
I2C1_SDA	C21	B9	
I2C3_SCL	Y21	K4	NVCC_GPIO (1.8 V / 3.3 V)
I2C3_SDA	W20	L4	
I2C5_SCL	U20	P4	
I2C5_SDA	U18	P5	
PMIC_SCLL	-	H5	V_1V8
PMIC_SDAL	-	H4	
PMIC_SCLH	-	G5	V_3V3
PMIC_SDAH	-	G4	

If more devices are connected to the I2C1 bus on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional pull-ups should be provided at the I²C bus on the carrier board, if required.

3.2.6.6 JTAG

The processor provides a JTAG interface that can be used to debug the programs executed on the processor. A corresponding hardware tool is required for this. The JTAG signals are routed directly to the LGA pads. Pull resistors must be provided on the mainboard.

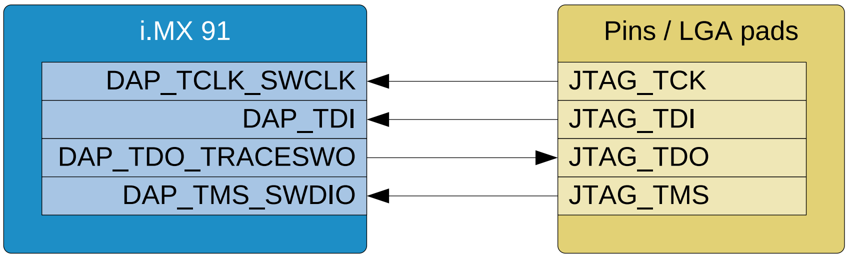

Figure 11: Block diagram JTAG interface

The following table shows the signals used by the JTAG interface. An external circuit on the mainboard has not to be provided.

Table 14: JTAG signals

Signal	i.MX 91	TQMa91xxLA	Power group
JTAG_TCK	Y1	F10	NVCC_WAKEUP (1.8 V)
JTAG_TDI	W1	E9	
JTAG_TDO	Y2	F8	
JTAG_TMS	W2	F9	

3.2.6.7 GPIO

Except for dedicated differential signals, e.g. USB, most CPU signals routed to the TQMa91xxLA LGA pads can be configured as GPIO. GPIO1_IO03 is not routed to the outside and is used internally in the module to connect the open drain signal PMIC_IRQ_B. The electrical characteristics of the GPIOs are to be taken from the i.MX 91 Data Sheet (2).
The following table shows the GPIO signals primarily configured as GPIO.

Table 15: GPIO signals

Signal	i.MX 91	TQMa91xxLA	Power group
GPIO1_IO02	D20	T15	NVCC_AON (3.3 V)
GPIO1_IO06	F20	E12	
GPIO1_IO07	F21	E11	
GPIO1_IO010	G18	E16	
GPIO2_IO06	L20	T7	NVCC_GPIO (1.8 V / 3.3 V)
GPIO2_IO07	L21	R6	
GPIO2_IO24	U21	N5	
GPIO3_IO26	AA2	B1	NVCC_WAKEUP
GPIO3_IO27	Y3	C1	
GPIO4_IO29	V4	D2	

3.2.6.8 SAI

The i.MX 91 has several SAI interfaces with different data bus widths. Due to limited multiplexing options, only the SAI3 interface is provided at the LGA pads. SAI2 as the most extensive SAI interface (4-bit) can only be used if the second Ethernet interface is omitted.

The SAI interface is full-duplex capable and supports I2S, AC97, TDM and other codec interfaces.

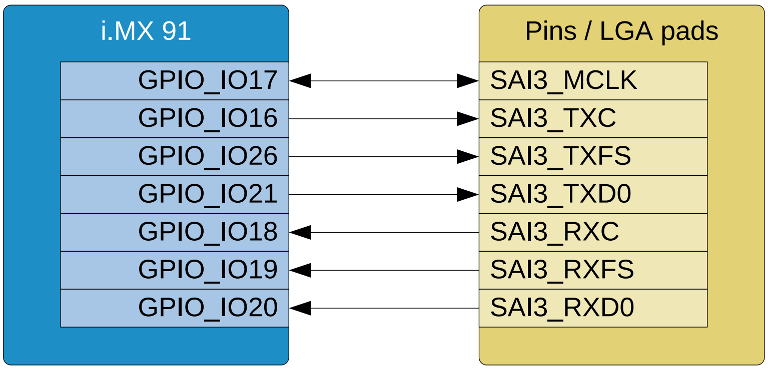

Figure 12: Block diagram SAI3

The following table lists all SAI signals provided by the TQMa91xxLA:

Table 16: SAI signals

Signal	i.MX 91	TQMa91xxLA	Power group
SAI3_MLCK	R20	T1	NVCC_GPIO (1.8 V / 3.3 V)
SAI3_TXC	R21	T2	
SAI3_TXFS	V20	N4	
SAI3_TXD0	T21	R3	
SAI3_RXD0	T20	N2	
SAI3_RXFS	R17	P3	
SAI3_RXC	R18	R2	

3.2.6.9 SPI

The TQMa91xxLA provides in the TQ standard multiplexing a SPI interface, which can be operated in both master and slave mode.

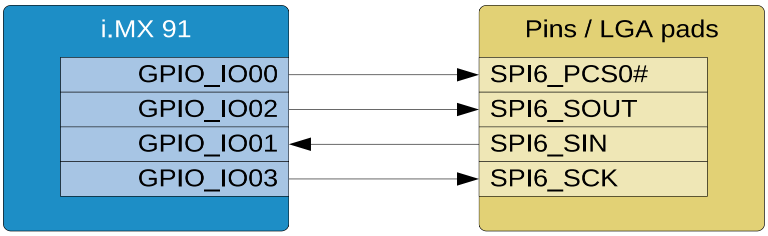

Figure 13: Block diagram SPI

Table 17: Pinning SPI

Signal	i.MX 91	TQMa91xxLA	Power group
SPI6_PCS0#	J21	U9	NVCC_GPIO (1.8 V / 3.3 V)
SPI6_SIN	J20	U8	
SPI6_SOUT	K20	V8	
SPI6_SCK	K21	W8	

3.2.6.10 Tamper

As one of the safety functions of the BBSM unit of the i.MX 91, two tamper signals are provided - one active and one passive. These are routed to the outside without any further circuitry.

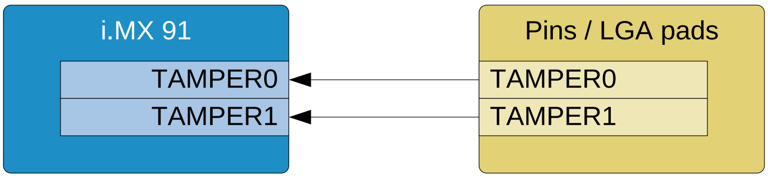

Figure 14: Block diagram Tamper

Table 18: Pinning Tamper

Signal	i.MX 91	TQMa91xxLA	Power group
TAMPER0	B16	L16	NVCC_BBSM (1.8 V)
TAMPER1	F14	K16	

3.2.6.11 UART

In standard TQ multiplexing five of eight possible UART interfaces are provided.
If less UARTs are required in customer applications, further interfaces, e.g. SPI or I2C, can be multiplexed at the same CPU pins.

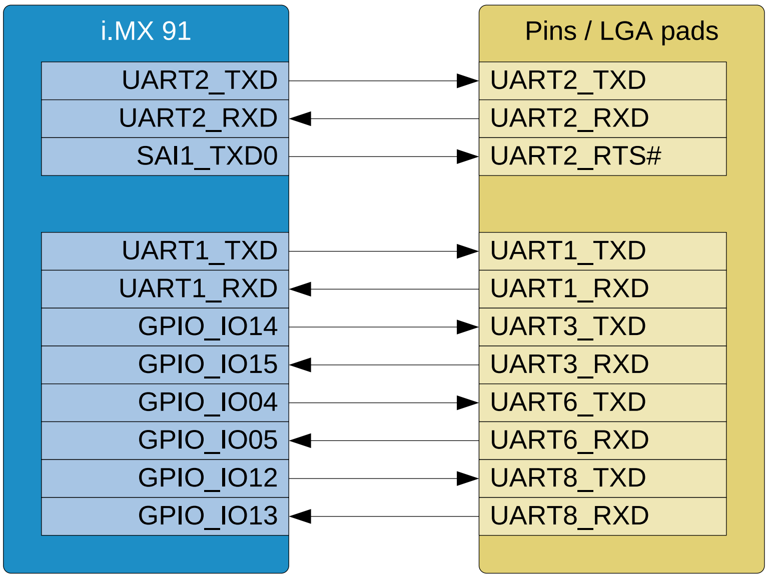

Figure 15: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces:

Table 19: UART signals

Signal	i.MX 91	TQMa91xxLA	Power group
UART1_RXD	E20	D10	NVCC_AON (3.3 V)
UART1_TXD	E21	D11	
UART2_RTS#	H21	W10	
UART2_RXD	F20	E12	
UART2_TXD	F21	E11	
UART3_RXD	P21	T4	NVCC_GPIO (1.8 V / 3.3 V)
UART3_TXD	P20	R4	
UART6_RXD	L18	T8	
UART6_TXD	L17	T9	
UART8_RXD	N21	U5	
UART8_TXD	N20	T5	

3.2.6.12 USB

The i.MX 91 has two USB 2.0 OTG controllers, each providing device, host or OTG ports at high speed (480 Mbps). The OTG signals are not available by default because their multiplexing overlaps with the ENET1 interface.

Up to 5 V can be applied to the VBUS pins. The 30 kΩ resistors required by NXP are already provided on the module. The differential signals are length matched on the TQMa91xxLA and routed with a differential impedance of 90 Ω.

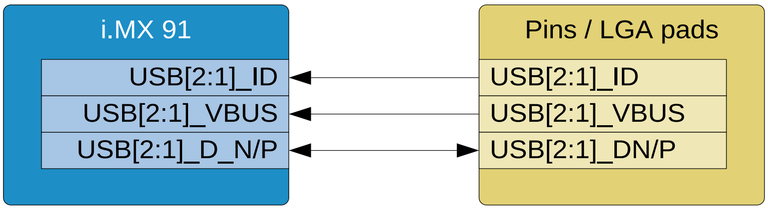

Figure 16: Block diagram USB interfaces

Table 20: USB signals

Signal	i.MX 91	TQMa91xxLA	Power group
USB1_ID	C11	N16	VDD_USB_1P8 (1.8 V)
USB2_ID	E12	P16	
USB1_DN	A14	V19	VDD_USB_3P3 (3.3 V)
USB1_DP	B14	U19	
USB1_VBUS	F12	P17	
USB2_DN	A15	W18	
USB2_DP	B15	V18	
USB2_VBUS	E14	T16	

3.2.6.13 SD2 (SD-Card)

The i.MX 91 supports SD cards up to UHS-I in SDR104/DDR50 mode. This corresponds to SD card specification v3.0 and a maximum data width of 4 bit.

To enable booting from SD cards, the SD2 interface is routed to LGA pads with the exception of SD2_VSELECT. SD2_RESET_B is available at an LGA pad, but can remain unconnected because the actual reset function of this signal is already implemented on TQMa91xxLA.

A separate PMIC LDO whose IO voltage can be set to a 1.8 V or 3.3 V range by the signal SD2_VSELECT supplies the signals of the SD2 interface. The driver automatically switches SD2_VSELECT so that the fastest possible mode is used depending on the SD card used. The default setting at boot is 3.3 V.

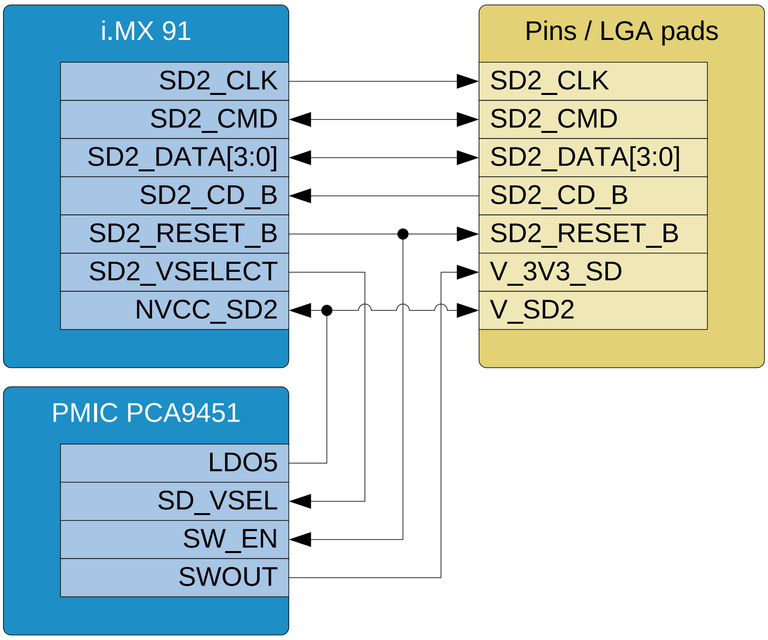

Figure 17: Block diagram SD card interface

Additionally the supply voltage V_SD2 is provided externally by the TQMa91xxLA. In customer designs, this voltage can be used to connect the pull-up resistors of the SD card interface. Alternatively, the use of CPU internal pull-up resistors is possible.

The voltage V_3V3_SD serves as main supply for SD cards. The TQMa91xxLA-internal wiring allows to interrupt the SD card supply at a module reset and thus to enable a reset of the SD card.

Table 21: SD2 signals

Signal	i.MX 91	TQMa91xxLA	Power group
SD2_CD#	Y17	U2	NVCC_SD2 (1.8 V / 3.3 V)
SD2_CLK	AA19	W2	
SD2_CMD	Y19	W3	
SD2_DATA0	Y18	V4	
SD2_DATA1	AA18	V3	
SD2_DATA2	Y20	U3	
SD2_DATA3	AA20	V1	
SD2_RST#	AA17	U1	

3.2.6.14 External clock sources

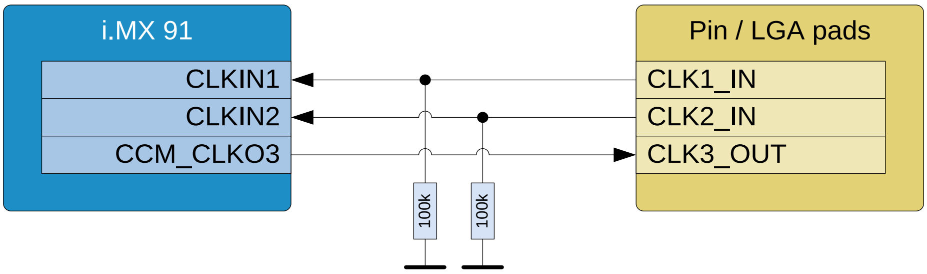

Figure 18: Block diagram external clocks

The i.MX 91 has the option to use two external oscillators as clock sources. Depending on the configuration of the internal clock tree, further reference clocks can be created.
All three i.MX 91 signals provided for this purpose are routed to TQMa91xxLA LGA pads. The following table shows these clock signals.

Table 22: CLK signals

Signal	i.MX 91	TQMa91xxLA	Level
CLK1_IN	B17	U15	1.8 V
CLK2_IN	A18	T14	
CLK3_OUT	U4	D1	

3.2.6.15 TPM / PWM

The TPM (Timer/PWM Module) of the i.MX 91 is a multi-channel timer that supports input capture, output compare, and the generation of PWM signals to control electrical motor and power management applications. The counter, compare, and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

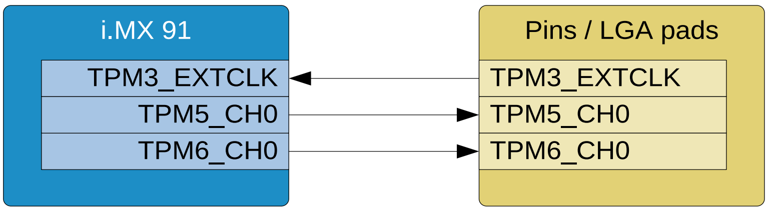

Figure 19: Block diagram TPM

Table 23: TPM Signals

Signal	i.MX 91	TQMa91xxLA	Power group
TPM3_EXTCLK	M21	V6	V_GPIO
TPM5_CH0	L20	T7	
TPM6_CH0	M20	U6	

3.2.7 Reset and unspecific signals

Two reset options are provided by the TQMa91xxLA. A reset is triggered by the signal PMIC_RST#. This signal is fed to the PMIC from outside, is low-active and has an internal pull-up. By default, the PMIC is configured so that activation triggers a cold reset. The cold reset is a power cycle, with the exception of the LDO1 controller. The BBSM voltage is thus retained.
A second reset possibility is given by the signal PMIC_WDOG_IN#. This is a 3.3 V signal which has a pull-up on the module. The corresponding PMIC behavior can be set via I2C. By default, a response to this signal is disabled.
The ONOFF pin of the CPU offers two reaction possibilities. It has an internal pull-up and is low-active. If this signal is held low for more than 5 s, the CPU enters OFF mode. If the signal is briefly pulled low in OFF mode, the CPU switches back to ON mode. A short low impuls in ON mode triggers an interrupt.
In addition, a reset is triggered by a module-internal supervisor when the module supply voltage drops.

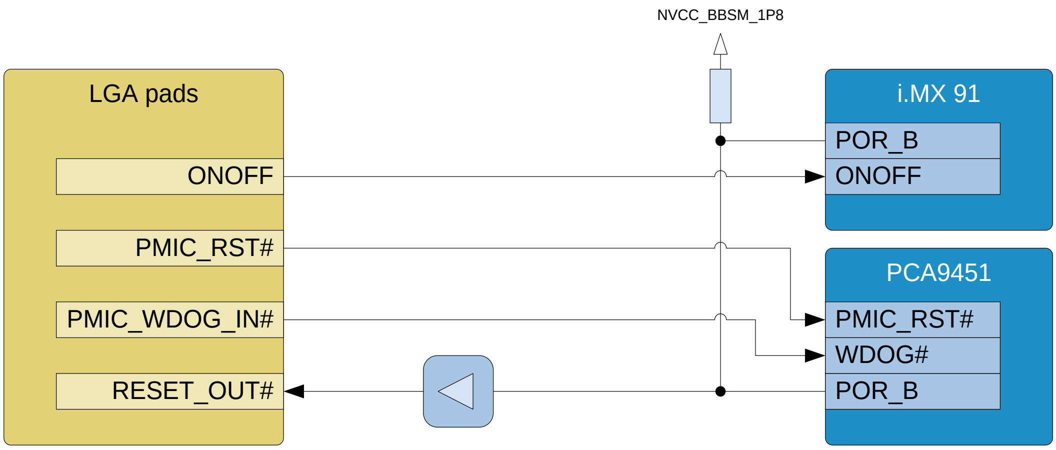

Figure 20: Block diagram Reset

RESET_OUT# is an open-drain output and is routed to a LGA pad. In customer applications, this ensures feedback on a reset of the module to external components. In customer designs a pull-up is required at this output.

Table 24: Reset and unspecific signals

Signal	i.MX 91	Power group	Remark
PMIC_RST#	-	NVCC_BBSM (1.8 V)	• No pull-up on carrier board required; low-active. • Programmable PMIC response (warm / cold reset).
ONOFF	[A19] ONOFF		• ON/OFF function of the i.MX 91. • No pull-up on carrier board required; low-active. • Pull to GND for 5 s to activate.
RESET_OUT#	[A16] POR_B		• Open drain output; low-active. • Activates RESET of carrier board components. • External pull-up required.
WDOG_ANY	[J18] WDOG_ANY	NVCC_AON (3.3 V)	
PMIC_WDOG_IN#	-	BUCK4 (3.3 V)	
RTC_EVENT#	-	Open Drain	
TEMP_EVENT#	-		

3.2.8 Power

3.2.8.1 Power supply

The TQMa91xxLA requires a main supply voltage of 5 V ±5 %. All power supply and ground pads should be connected.

Through V_LICELL the TQMa91xxLA has an input for the backup voltage supply of the optional discrete RTC PCF85063A. Please refer to chapter 3.2.5.2

The characteristics and functions of a certain pin or signal is to be taken from the PMIC Data Sheet (4), and the i.MX 91 Data Sheet (2).

3.2.8.2 Configurable voltages

V_GPIO must be powered by the baseboard to supply the CPU rail NVCC_GPIO. The required voltage is either 1.8 V (1.65…1.95 V) or 3.3 V (3.00…3.60 V).

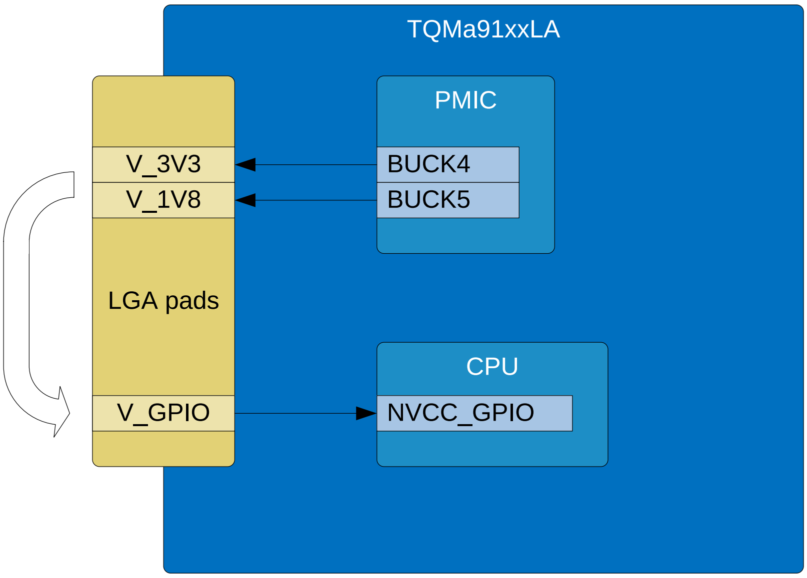

Figure 21: Possible power supply of the CPU-rail NVCC_GPIO

Attention: Destruction or malfunction	
	If V_GPIO is not connected to a power supply the corresponding CPU-Rail is not powered. This can cause malfunction or damage the CPU.

3.2.8.3 Power consumption

The given power consumption has to be seen as an approximate value.
The TQMa91xxLA power consumption strongly depends on the application, the mode of operation and the operating system.

The following table shows TQMa91xxLA power supply and power consumption parameters:

Table 25: Power consumption

Mode of operation	Current @ 5 V	Power consumption @ 5 V
Theoretical calculated peak (worst case)	TBD	TBD
U-Boot prompt	TBD	TBD
Linux prompt	TBD	TBD
Linux stress test	TBD	TBD
Reset	TBD	TBD

3.2.8.4 Voltage monitoring

The TQMa91xxLA features a supervisor which monitors the input voltage (V_{IN}).
If the input voltage drops below 4.38 V, a Reset (PMIC_ON_REQ) is triggered and the TQMa91xxLA is held in reset until the input voltage is in the permitted range again.

Attention: Destruction or malfunction, supply voltage exceedance	
	The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa91xxLA.

3.2.8.5 Supply outputs

The TQMa91xxLA provides three voltages that can be used on the carrier board.

Table 26: Voltages provided by TQMa91xxLA

Voltage	TQMa91xxLA	Usage	Max. load
V_1V8	N1	General usage on carrier board	500 mA
V_3V3	P1	General usage on carrier board	500 mA
V_3V3_SD	F6	SD card supply	400 mA

The voltage V_3V3 can be used as Power-Good signal for the supply of circuitry on the carrier board.

Attention: Destruction or malfunction, current exceedance	
	A load of up to 500 mA at V_1V8 or V_3V3, as well as up to 400 mA at V_3V3_SD causes an increased power consumption of the TQMa91xxLA and thus a higher self-heating. These three voltages are outputs and must never be supplied from external sources! Furthermore, the outputs are not short-circuit proof. Overloading the voltage outputs can damage the TQMa91xxLA.

3.2.8.6 Power-Up sequence TQMa91xxLA / carrier board

As the TQMa91xxLA operates with 5 V and the I/O voltages of the CPU signals are generated on the TQMa91xxLA, there are timing requirements for the carrier board design with respect to the voltages generated on the carrier board:
After power up of the 5V supply for the TQMa91xxLA, the PMIC power-up sequence starts. External TQMa91xxLA inputs driven by the carrier board may only be switched on after the power-up of V_3V3. LGA pad P1 (V_3V3) can be used as feedback.

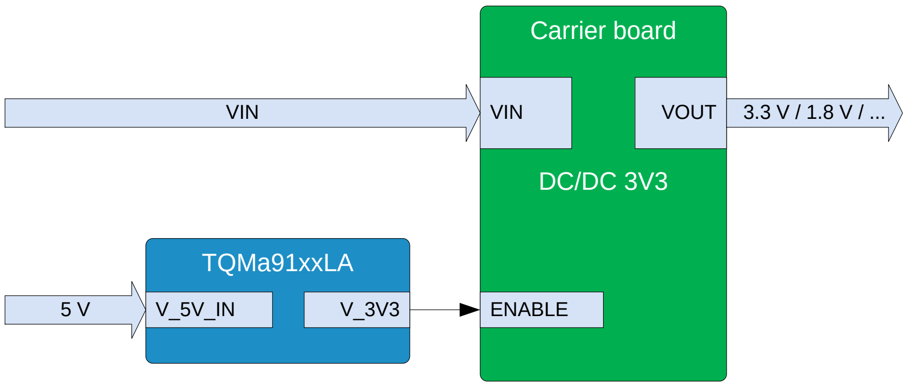

Figure 22: Block diagram power supply of carrier board

Attention: Destruction or malfunction, Power-Up sequence	
	To avoid cross supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the power-up sequence is indicated by a high level of signal V_3V3, LGA pad P1.

3.2.8.7 Standby and BBSM

In standby mode, several voltage controllers on the TQMa91xxLA are switched off.
The rail V_1V8_BBSM remain active, which ensures the correct function of the BBSM.

3.2.8.8 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX 91 Reference Manual (1) and the PMIC Data Sheet (4). The PMIC is controlled by the I2C1 bus.

- The PMIC has I^{2}C address `0x25 / 010 0101b`

The following PMIC and power management signals are available on the TQMa91xxLA LGA pads

Table 27: PMIC signals

Signal	Direction	TQMa91xxLA	Power group	Remark
PMIC_WDOG_IN#	I	H6	3.3 V	• Low-active input
PMIC_RST#	I	E6	1.8 V	• Low-active input
RESET_OUT#	O	J5	1.8 V	• Low-active output • Connected to PMIC POR# • Can signal a TQMa91xxLA reset
SD_VSEL	–	–	–	• See chapter 3.2.6.16

Attention: Destruction or malfunction, PMIC programming	
	Improper programming of the PMIC may result in the i.MX 91 or periphery being operated outside its specification. This may lead to malfunctions, accelerated aging or destruction of the TQMa91xxLA.

3.2.9 Impedances

By default, all single-ended signals have a nominal impedance of 50 Ω ±10 %.
However, some interfaces on the TQMa91xxLA are routed with different impedances, depending on the signal requirements.

The following table is taken from the Hardware Developer's Guide (3) and shows the respective interfaces:

Table 28: Trace impedance recommendations

Signal / Interface	Impedance on TQMa91xxLA	Recommendation for carrier board
DDR DQS/CLK	85 Ω, differential	85 Ω ±10 %, differential
Differential USB signals	90 Ω, differential	90 Ω ±10 %, differential
Differential signals, including Ethernet	100 Ω, differential	100 Ω ±10 %, differential

4. SOFTWARE

The TQMa91xxLA is delivered with a preinstalled boot loader U-Boot.
The BSP provided by TQ-Systems GmbH is configured for the combination of TQMa91xxLA and MBa91xxCA.
The boot loader U-Boot provides TQMa91xxLA-specific as well as board-specific settings, e.g.:

- i.MX 91 configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

Further information can be found in the https://support.tq-group.com/TQMa91xxLA.

If another bootloader is used, this data must be adapted. Contact TQ-Support for detailed information.

5. MECHANICS

5.1 Dimensions

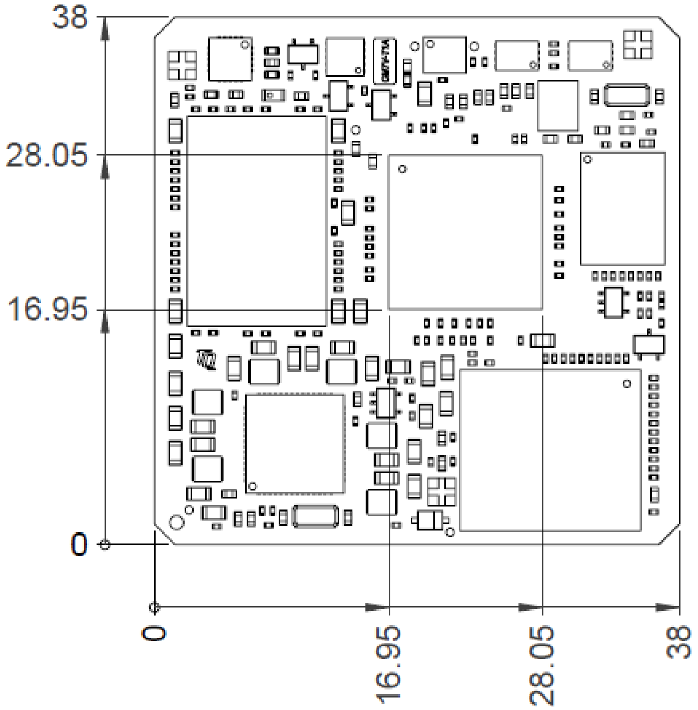

Figure 23: TQMa91xxLA dimensions, top view

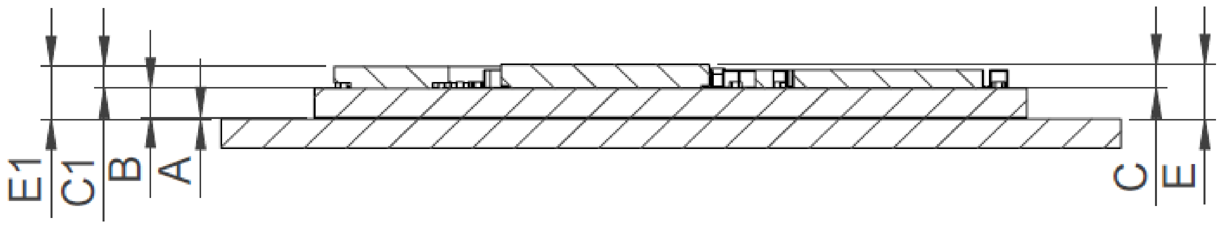

Figure 24: TQMa91xxLA dimensions, side view

Table 29: TQMa91xxLA heights

Dim.	Value	Tolerance	Remark
A	0.125 mm	+0.0075 mm / -0.025 mm	TQMa91xxLA LGA pads height
B	1.60 mm	±0.16 mm	PCB without solder resist
C	1.05 mm	±0.10 mm	Height of CPU
C1	1.08 mm	±0.06 mm	Height of NOR Flash
E	2.80 mm	±0.19 mm	Overall height to CPU surface
E1	2.83 mm	±0.18 mm	Overall height to NOR Flash

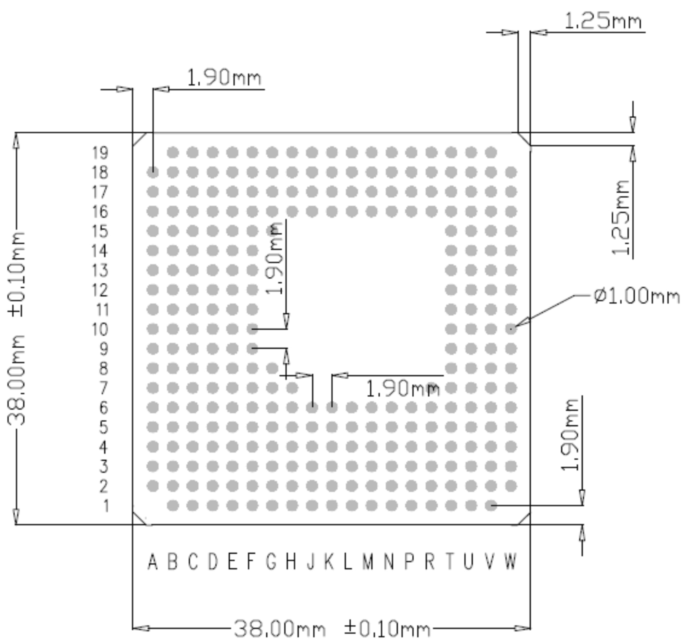

Figure 25: TQMa91xxLA dimensions, top through view

5.2 Component placement and labeling

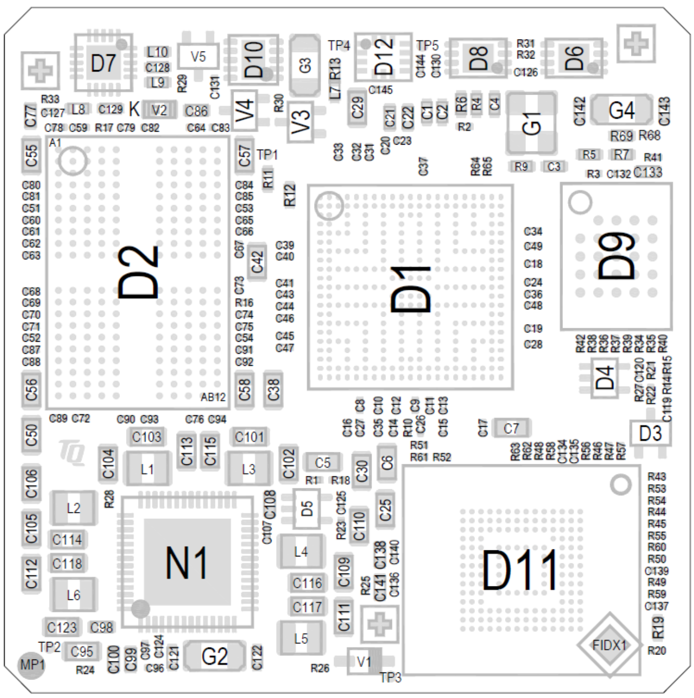

Figure 26: TQMa91xxLA, component placement top

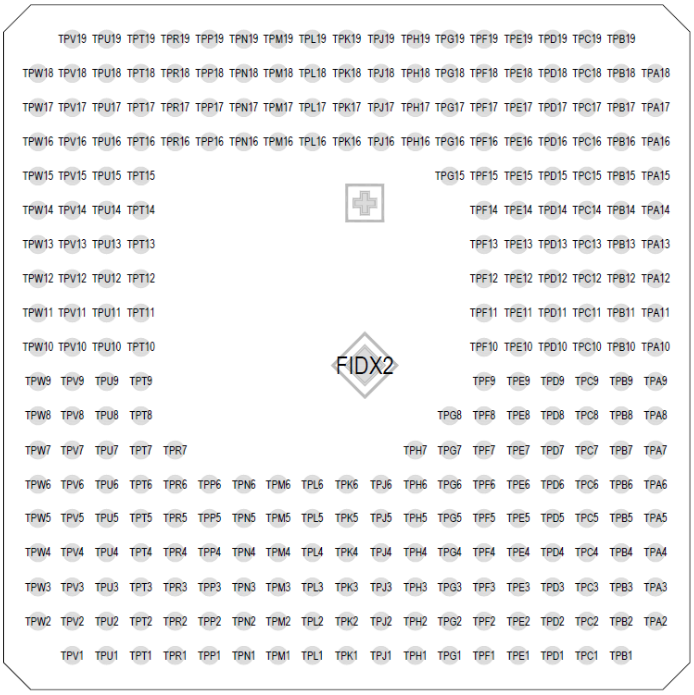

Figure 27: TQMa91xxLA, LGA pad numbering scheme, bottom view

The labels on the TQMa91xxLA show the following information:

Table 30: Labels on TQMa91xxLA

Label	Content
AK1	Serial number
AK2	MAC address
AK3	TQMa91xxLA version and revision

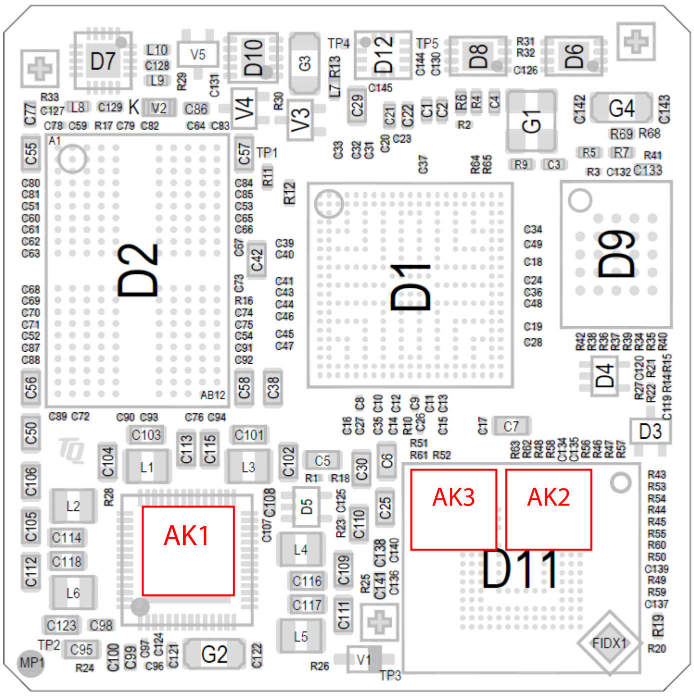

Figure 28: Labels on TQMa91xxLA

5.3 Adaptation to the environment

The TQMa91xxLA has overall dimensions (length × width) of 38.0 mm × 38.0 mm (± 0.1 mm).
The TQMa91xxLA has a maximum height above the carrier board of approximately 2.80 mm (±0.19 mm).
The TQMa91xxLA has 281 LGA pads with a diameter of 1.0 mm and a grid of 1.9 mm.
The TQMa91xxLA weighs approximately 8 g.

5.4 Protection against external effects

The TQMa91xxLA does not provide protection against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

To cool the TQMa91xxLA, note Table 27. The power dissipation originates primarily in the i.MX 91, the LPDDR4 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (6) and (7) for further information.

Attention: Destruction or malfunction, TQMa91xxLA cooling	
	The i.MX 91 belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 91 must be taken into consideration when connecting the heat sink, see (6). The i.MX 91 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa91xxLA and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMa91xxLA has to be soldered on the carrier board. To ensure a high-quality connection of the LGA pads during reflow soldering of the TQMa91xxLA, the LGA pads must be free of grease and dirt.
Please contact TQ-Support for soldering instructions (11).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa91xxLA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa91xxLA.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Shock and Vibration

Table 31: Shock resistance

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 ms
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 32: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 ~ 9 Hz, 9 ~ 200 Hz, 200 ~ 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Acceleration	2 Hz to 9 Hz: 3.5 m/s^2 9 Hz to 200 Hz: 10 m/s^2 200 Hz to 500 Hz: 15 m/s^2

6.4 Climate and operational conditions

The TQMa91xxLA is available in different variants with different ambient temperature ranges. The operating temperature range for the TQMa91xxLA strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa91xxLA.
In general, a reliable operation is given when following conditions are met:

Table 33: Climate and operational conditions

Parameter		Range	Remark
Ambient temperature TQMa91xxLA	Standard	–25 °C to +85 °C	–
	Extended	TBD	–
T_J temperature i.MX 91		–40 °C to +105 °C	–
T_J temperature PMIC		–40 °C to +125 °C	–
Case temperature LPDDR4		–40 °C to +95 °C	–
Case temperature other ICs	Standard	–25 °C to +85 °C	–
	Extended	–40 °C to +85 °C	–
Storage temperature TQMa91xxLA		–40 °C to +100 °C	–
Relative humidity (operating / storage)		10 % to 90 %	Not condensing

Detailed information concerning the i.MX 91 thermal characteristics is to be taken from NXP documents (6) and (7).

Attention: Destruction or malfunction, TQMa91xxLA cooling

The i.MX 91 belongs to a performance category in which a cooling system is essential.
It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).
Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 91 must be taken into consideration when connecting the heat sink, see (6). The i.MX 91 is not necessarily the highest component.
Inadequate cooling connections can lead to overheating of the TQMa91xxLA and thus malfunction, deterioration or destruction.

6.5 Intended Use

TQ DEVICES, PRODUCTS AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION IN NUCLEAR FACILITIES, AIRCRAFT OR OTHER TRANSPORTATION NAVIGATION OR COMMUNICATION SYSTEMS, AIR TRAFFIC CONTROL SYSTEMS, LIFE SUPPORT MACHINES, WEAPONS SYSTEMS, OR ANY OTHER EQUIPMENT OR APPLICATION REQUIRING FAIL-SAFE PERFORMANCE OR IN WHICH THE FAILURE OF TQ PRODUCTS COULD LEAD TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE. (COLLECTIVELY, "HIGH RISK APPLICATIONS")

You understand and agree that your use of TQ products or devices as a component in your applications are solely at your own risk. To minimize the risks associated with your products, devices and applications, you should take appropriate operational and design related protective measures.

You are solely responsible for complying with all legal, regulatory, safety and security requirements relating to your products. You are responsible for ensuring that your systems (and any TQ hardware or software components incorporated into your systems or products) comply with all applicable requirements. Unless otherwise explicitly stated in our product related documentation, TQ devices are not designed with fault tolerance capabilities or features and therefore cannot be considered as being designed, manufactured or otherwise set up to be compliant for any implementation or resale as a device in high risk applications. All application and safety information in this document (including application descriptions, suggested safety precautions, recommended TQ products or any other materials) is for reference only. Only trained personnel in a suitable work area are permitted to handle and operate TQ products and devices. Please follow the general IT security guidelines applicable to the country or location in which you intend to use the equipment.

6.6 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.7 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.8 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.9 Reliability and service life

The MTBF calculated for the TQMa91xxLA is 1,113,855 hours with a constant error rate @ +40 °C, Ground Benign.

The TQMa91xxLA is designed to be insensitive to shock and vibration.

The TQMa91xxLA must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.

Detailed information concerning the i.MX 91 service life under different operational conditions is to be taken from the NXP Application Note (7).

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa91xxLA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa91xxLA was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa91xxLA always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa91xxLA on account of available Standby or Sleep-Modes of the components on the TQMa91xxLA.

7.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7.6 Battery

No batteries are assembled on the TQMa91xxLA.

7.7 Packaging

The TQMa91xxLA is delivered in reusable packaging.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa91xxLA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa91xxLA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
(Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
(Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
(Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
(Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 34: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
BBSM	Battery Backed Secure Module
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CAN-FD	CAN with Flexible Data-Rate
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DDR	Double Data Rate
DIN	Deutsche Industrienorm (German industry standard)
DNC	Do Not Connect
DSI	Display Serial Interface
EARC	Enhanced Audio Return Channel
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
Gbps	Gigabit per second
GPIO	General Purpose Input/Output
GPT	General-Purpose Timer
HDMI	High-Definition Multimedia Interface
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IP00	Ingress Protection 00
IPU	Input with Pull-Up
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LGA	Land Grid Array
LPDDR4	Low Power DDR4
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
ML/AI	Machine Learning / Artificial Intelligence
MMC	Multimedia Card
MTBF	Mean operating Time Between Failures

8.1 Acronyms and definitions (continued)

Table 37: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
O	Output
OD	Open Drain
OOD	Output with Open Drain
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protection
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TBD	To Be Determined
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 35: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 91 Applications Processor Reference Manual	TBD	NXP
(2)	i.MX 91 Application Processors Data Sheet	Rev. 1 Draft F, Sep 2023	NXP
(3)	i.MX 91 Hardware Developer's Guide	TBD	NXP
(4)	Power management IC for i.MX 91 application processor	TBD	NXP
(5)	i.MX 91 Mask Set Errata	TBD	NXP
(6)	i.MX 91 Power Consumption Measurement	TBD	NXP
(7)	i.MX 91 Product Lifetime Usage	TBD	NXP
(8)	SE050 Trust Secure Element Data Sheet	Rev. 3.1, Dec 2020	NXP
(9)	MBa91xxCA User's Manual	– current –	TQ-Systems
(10)	TQMa91xxLA Support-Wiki	– current –	TQ-Systems
(11)	TQMa91xxLA Processing instructions	– current –	TQ-Systems

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