



TQMa6ULxL User's Manual

TQMa6ULxL UM 0108
23.07.2020





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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	17.05.2017	Petz		First issue
0101	16.01.2018	Petz	3.2.1.2, Table 18, 3.2.5.14 4.4, 4.6 Table 44	Added Updated AN4871 added
0102	23.03.2018	Petz	All 1.9 3.2.1.4, Table 5, Table 6, Table 7, Table 9, Table 10 Figure 10, Figure 21, Figure 22 Figure 14	Typo "iMX6ULCEC Data Sheet" added Information clarified Updated Colour of Reset LED added
0103	04.04.2018	Petz	Table 3 3.2.2.3 3.2.5.8, Table 28 3.2.5.14	Footnotes 7, and 8 added "QSPIA" replaced with "QSPI_A" Completely reworked Content clarified
0104	18.12.2018	Petz	All Table 3 4, 9, 12 Table 8 3.2.2, Table 14 Table 17 3.2.5.14 3.2.5.7, 3.2.7.6 3.2.7.1 3.2.7.8 Figure 16 Table 3, Table 34 Table 38 4.1 Table 41, Table 42	Hyperlinks updated, ® and ™ symbols added Function of i.MX6UL balls J14 and K15 corrected Revision-dependent eMMC and QSPI voltages added Footnotes added High-Speed (HS) support added Updated Moved from 3.2.2.5 to 3.2.2.4 Removed Warnings updated Supply voltage tolerance added Note and Warning added Updated Direction of "USDHC1_WP" corrected Remarks added Removed "Package temperature" replaced with "Case temperature" Case temperature DDR3L SDRAM changed to +95 °C
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0106	20.09.2019	Petz	4.6 (11)	Updated Added
0107	29.11.2019	Petz	Footnote 1 1.9, 8.2	Added Link to Yocto documentation added, links updated
0108	23.07.2020	Petz	1.9, 2, 2.1, Table 4 2, 2.1, Figure 1 Figure 2 Table 16, Table 17 Table 42	Information about i.MX6ULL CPUs added Updated Added Removed Updated and extended



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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.


1.6 Symbols and typographic conventions

Table 1: Terms and conventions


Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	<p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.</p> <p>Violation of this guideline may result in damage / destruction of the TQMa6ULxL and be dangerous to your health.</p> <p>Improper handling of your TQ-product would render the guarantee invalid.</p>
---	--

Proper ESD handling

	<p>The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).</p> <p>Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.</p>
---	--



1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring. The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa6ULx schematics
- MBa6ULx User's Manual
- i.MX6UL and i.MX6ULL Data Sheets
- i.MX6UL and i.MX6ULL Reference Manuals
- IMX6ULCEC Data Sheet
- IMX6ULRM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa6ULx



2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa6ULxL Rev. **01xx** and Rev. **02xx**, and refers to some software settings. Existing differences between Rev. 01xx and Rev. 02xx are pointed out specifically.

The TQMa6ULxL is the LGA-version of the TQMa6ULx. A certain TQMa6ULxL derivative does not necessarily provide all features described in this User's Manual. This User's Manual does also not replace the NXP i.MX6UL documentation (Table 42).

The TQMa6ULxL is a universal Minimodule based on the NXP Cortex[®]-A7 ARM CPU MCIMX6GxCVM05 i.MX6UL or i.MX6ULL.

The Cortex[®]-A7 core of this i.MX6UL is typically clocked with 528 MHz. ¹

For reasons of clarity, it is not referred to the i.MX6ULL with every mention of the i.MX6UL in this User's Manual. If necessary, however, this will be pointed out.

2.1 Block diagrams i.MX6UL, i.MX6ULL

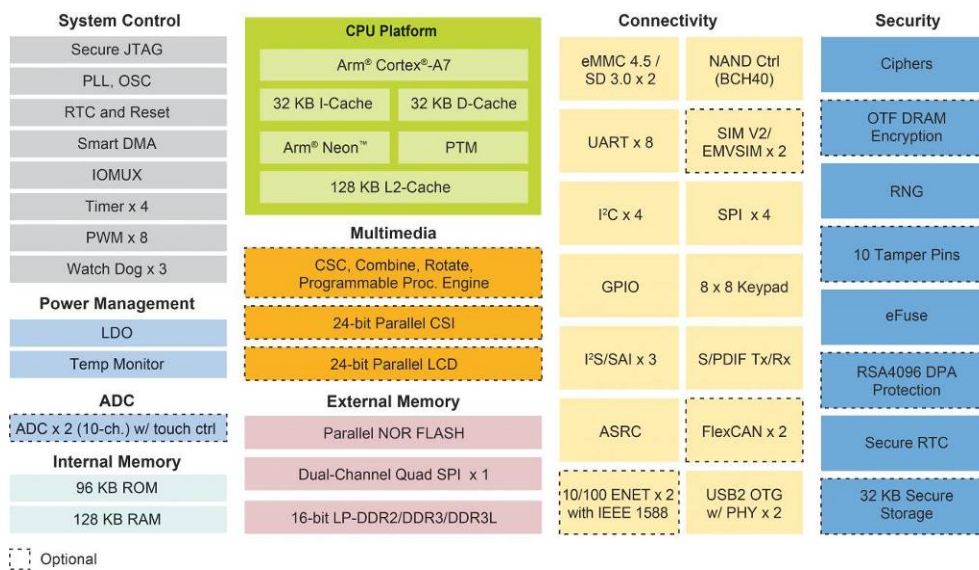


Figure 1: Block diagram i.MX6UL (Source: [NXP](#))

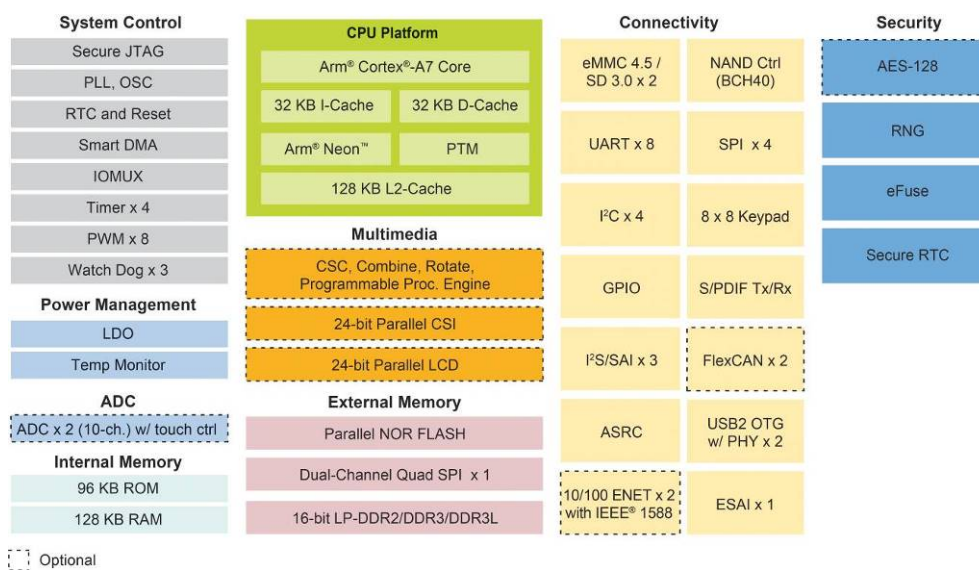


Figure 2: Block diagram i.MX6ULL (Source: [NXP](#))

1: Up to 700 MHz with selected i.MX6UL.



2.1 Block diagrams i.MX6UL, i.MX6ULL (continued)

The TQMa6ULxL extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX6UL derivative (G1, G2, G3, Y0, Y1 or Y2) can be selected for each requirement.

All essential i.MX6UL pins are routed to the TQMa6ULxL LGA pads. There are therefore no restrictions for customers using the TQMa6ULxL with respect to an integrated customised design. All essential components like i.MX6UL, DDR3L SDRAM, eMMC, and power management are already integrated on the TQMa6ULxL.

The main features of the TQMa6ULxL are:

- NXP i.MX6UL or i.MX6ULL CPU
- Up to 1 Gbyte DDR3L SDRAM with 16 bit interface (standard: 256 Mbyte)
- Up to 32 Gbyte eMMC NAND flash (standard: 4 Gbyte)
- Up to 256 Mbyte QSPI NOR flash (standard: 32 Mbyte)
- 64 kbit EEPROM
- EEPROM (128 byte for protection mode, 128 byte for normal usage)
- Temperature sensor
- NXP Power Management Integrated Circuit PF3000
- All essential i.MX6UL pins are routed to the TQMa6ULxL LGA pads
- Extended temperature range
- Single supply voltage 3.3 V

With a TQMa6ULxL soldered on the adapter "TQMa6ULxL-MB-ADAP", the TQMa6ULxL can be evaluated on the MBa6ULx.

The adapter comprises a 5 V to 3.3 V LDO to supply the TQMa6ULxL.



2.2 Key functions and characteristics

The following components are implemented on the TQMa6ULxL:

- i.MX6UL(L) CPU
- DDR3L SDRAM
- eMMC NAND flash
- QSPI NOR flash
- EEPROM
- EEPROM with temperature sensor
- RTC
- Supervisor with Reset structure
- Power supply by PMIC with Power Sequencing and 3.3 V direct via adapter
- 226 pre-tinned LGA pads

The following interfaces are provided at the TQMa6ULxL contacts: ²

- 2 × Ethernet 10/100 RMII
- 2 × I²C (1 × for the I²C devices on the TQMa6ULxL)
- 1 × JTAG
- 1 × Parallel LCD RGB 24-bit interface
- 2 × CAN
- 1 × SPI
- 2 × USB 2.0 OTG
- 11 × GPIO
- 3 × UART
- 1 × SD 4-bit (SDIO / MMC / SD card)
- 10 × Tamper
- 1 × differential clock (CCM)
- 1 × QSPI (for second SPI NOR flash; SS1)
- 1 × WDOG1

By adapting the pin configuration, further i.MX6UL interfaces are also available as an alternative to the mentioned factory configuration. These are amongst others:

- Camera Sensor-Interfaces 8-bit (CSI – CMOS Sensor Interface)
- Synchronous Audio Interface (SAI – e.g., I²S)
- PWM
- ADC
- NAND flash interface
- EIM bus (External Interface Module)
- Enhanced Periodic Interrupt Timer
- General Purpose Media Interface
- General Purpose Timer
- Keypad Port
- More audio interfaces
- More I²C interfaces
- More SPI interfaces
- More UARTs

2: Number of interfaces depend on i.MX6UL derivative.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa6ULxL, and the [BSP provided](#) by TQ-Systems, see also chapter 5.

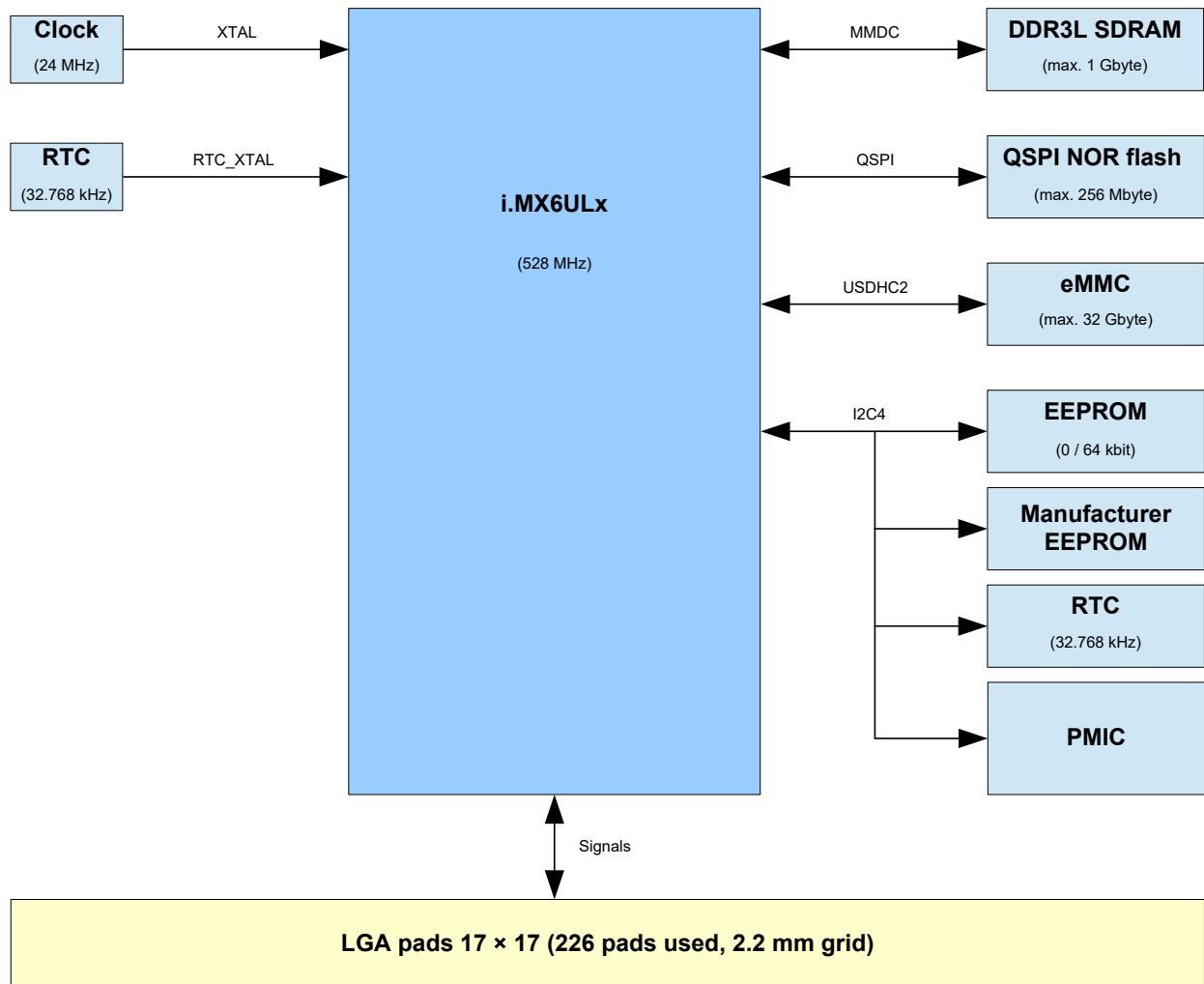


Figure 3: Block diagram TQMa6ULxL (simplified)

3.1 Interfaces to other systems and devices


3.1.1 Pin multiplexing

When using the i.MX6UL, the multiple pin configurations by different i.MX6UL-internal function units must be taken note of. The pinout in Table 3 refers to the [BSP provided](#) by TQ-Systems in combination with the carrier board MBa6ULx.

NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).

The electrical and pin characteristics are to be taken from the i.MX6UL Data Sheets and Reference Manuals (see Table 42) as well as the PMIC Data Sheet (10).

3.1.2 LGA pad-out

Attention: Destruction or malfunction, pin multiplexing	
	<p>Depending on the configuration, many i.MX6UL pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX6UL Reference Manual (see Table 42), before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa6ULxL.</p> <p>The information given in the following chapters is to be taken note of:</p> <p><u>NA:</u> These pins may not be connected under any circumstances and have to be left open. (No LGA pad present.)</p>

The TQMa6ULxL provides 226 pads. The following table shows the **top view** of the pad-out with i.MX6UL2 or i.MX6UL3. Please take note of the different i.MX6UL1 pad-out!



3.1.2.1 Pinout TQMa6ULxL

Table 2: Pinout TQMa6ULxL, TOP VIEW through TQMa6ULxL

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	NA	CCM_CLK1_P	CCM_CLK1_N	DGND	USB_OTG1_DN	DGND	USB_OTG1_DP	DGND	USB_OTG2_DN	USB_OTG2_DP	UART1_TX_DATA	GPIO1_IO18	GPIO1_IO09	UART3_TX_DATA	CAN1_TX	MX6UL_ONOFF	NA	17
16	VIN	VIN	DGND	USB_OTG1_CHD#	DGND	USB_OTG1_VBUS	DGND	USB_OTG2_PWR	DGND	USB_OTG2_VBUS	UART1_RX_DATA	GPIO1_IO19	DGND	UART3_RX_DATA	CAN1_RX	DGND	PMIC_PWRON	16
15	VIN	VIN	VSNV5_REF_OUT	DGND	VCCDDR_OUT	USB_OTG1_PWR	USB_OTG1_OC	USB_OTG2_ID/SD_VSEL	USB_OTG2_OC	DGND	DRAM_SDQ50_N	DRAM_SDQ50_P	SNVS_TAMPER4	DRAM_SDCLK0_P	DRAM_SDCLK0_N	DGND	RESET_OUT#	15
14	VIN	VIN	LICELL	VCC2V5_OUT	VCC3V3_V33_OUT	USB_OTG1_ID	DGND	SNVS_TAMPER0	SNVS_TAMPER1	SNVS_TAMPER2	DRAM_DS	DGND	SNVS_TAMPER3	DGND	DRAM_A0	RESET_IN#	BOOT_MODE1	14
13	DGND	DGND	DGND	DGND	NVCC_ENET	NA	NA	NA	NA	NA	NA	NA	DGND	SNVS_TAMPER5	SNVS_TAMPER6	DGND	BOOT_MODE0	13
12	DGND	DGND	DGND	DGND	NA	NA	NA	NA	NA	NA	NA	NA	NA	SNVS_TAMPER7	SNVS_TAMPER8	CAN2_RX	CAN2_TX	12
11	SPI2_SCLK	SPI2_SSO#	SPI2_MOSI	SPI2_MISO	NA	NA	JTAG_TMS	DGND	JTAG_TRST#	DGND	VDDSOC_CAP	NA	NA	SNVS_TAMPER9	DGND	I2C4_SDA	I2C4_SCL	11
10	DGND	DGND	VCC3V3_REF_OUT	VCCCORE_OUT	NA	NA	JTAG_TDI	NA	NA	NA	DGND	NA	NA	SD1_DATA0	SD1_CMD	DGND	SD1_CLK	10
9	VCC3V3_IN	VCC3V3_IN	WDOG1#	VCC1V8_OUT	NA	NA	JTAG_TDO	NA	NA	NA	DGND	NA	NA	DGND	SD1_DATA3	SD1_DATA2	SD1_DATA1	9
8	ENET1_TDATA0	ENET1_TDATA1	DGND	DGND	NA	NA	DGND	NA	NA	NA	VDDSOC_CAP	NA	NA	UART6_RX_DATA	UART6_TX_DATA	DGND	I2C2_SCL	8
7	ENET1_TX_CLK	DGND	ENET1_TX_EN	DGND	NA	NA	JTAG_MOD	DGND	JTAG_TCK	DGND	VDDARM_CAP	NA	NA	DGND	GPIO4_IO22	GPIO4_IO21	I2C2_SDA	7
6	ENET1_RDATA0	ENET1_RDATA1	DGND	ENET_MGMT_MDC	DGND	NA	NA	NA	NA	NA	NA	NA	NA	GPIO4_IO25	GPIO4_IO24	DGND	GPIO4_IO23	6
5	ENET1_RX_EN	DGND	ENET1_RX_ER	ENET_MGMT_MDIO	eMMC_SCL	DGND	NA	NA	NA	NA	NA	NA	NVCC_CSI	DGND	GPIO4_IO29	GPIO4_IO27	GPIO4_IO26	5
4	ENET2_TDATA0	ENET2_TDATA1	DGND	DGND	eMMC_CMD	eMMC_RST#	QSPI_A_SS1#	QSPI_A_SCK	LCD_DATA23	LCD_DATA19	LCD_DATA16	LCD_DATA12	LCD_DATA09	LCD_DATA05	DGND	LCD_RESET	LCD_VSYNC	4
3	ENET2_TX_CLK	DGND	ENET2_TX_EN	eMMC_DATA6	DGND	eMMC_DATA5	QSPI_A_SS0#	DGND	LCD_DATA22	LCD_DATA18	LCD_DATA15	LCD_DATA11	LCD_DATA08	LCD_DATA04	LCD_DATA02	DGND	LCD_HSYNC	3
2	ENET2_RDATA0	ENET2_RDATA1	DGND	eMMC_DATA7	eMMC_DATA4	eMMC_DATA2	QSPI_A_DATA1	QSPI_A_DATA0	LCD_DATA21	DGND	LCD_DATA14	DGND	LCD_DATA7	DGND	LCD_DATA01	DGND	LCD_ENABLE	2
1	NA	ENET2_RX_EN	ENET2_RX_ER	eMMC_DATA2	eMMC_DATA1	eMMC_DATA0	QSPI_A_DATA3	QSPI_A_DATA2	LCD_DATA20	LCD_DATA17	LCD_DATA13	LCD_DATA10	LCD_DATA06	LCD_DATA03	LCD_DATA00	LCD_CLK	NA	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

The secondary functions of CSI and NAND flash interfaces are pattern coded as follows:

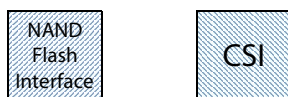


Figure 4: Secondary function of some TQMa6ULxL LGA pads

3.1.2.2 TQMa6ULxL signals

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX6UL Reference Manual and Data Sheet (see Table 42), as well as the PMIC Data Sheet (10).

Table 3: TQMa6ULxL, signals

i.MX6UL ball	Dir.	Level	Group	Signal name	TQMa6ULxL
T10	I	3.0 V ³	Boot	BOOT_MODE0	U13
U10	I	3.0 V ³	Boot	BOOT_MODE1	U14
G14	I	3.3 V	CAN	CAN1_RX	R16
H15	O	3.3 V	CAN	CAN1_TX	R17
H14	I	3.3 V	CAN	CAN2_RX	T12
J15	O	3.3 V	CAN	CAN2_TX	U12
P16	O	2.5 V	CCM	CCM_CLK1_N	C17
P17	O	2.5 V	CCM	CCM_CLK1_P	B17
R8	I	3.3 V	Config	MX6UL_ONOFF	T17
T9	I	3.3 V	Config	PMIC_PWRON	U16
P8	I	3.3 V	Config	RESET_IN#	T14
–	O	3.3 V	Config	RESET_OUT#	U15
N17	O	3.3 V	Config	WDOG1#	C9
–	O	0.675 V	DRAM	DRAM_A0	R14
–	O	0.675 V	DRAM	DRAM_D5	L14
–	O	0.675 V	DRAM	DRAM_SDCLK0_N	R15
–	O	0.675 V	DRAM	DRAM_SDCLK0_P	P15
–	O	0.675 V	DRAM	DRAM_SDQS0_N	L15
–	O	0.675 V	DRAM	DRAM_SDQS0_P	M15
C8	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_CMD	E4
D7	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA0	F1
B7	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA1	E1
A7	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA2	D1
D6	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA3	F2
C6	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA4	E2
B6	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA5	F3
A6	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA6	D3
A5	I/O	1.8 V / 3.3 V ⁴	EMMC	EMMC_DATA7	D2
B4	O	1.8 V / 3.3 V ⁴	EMMC	EMMC_RST#	F4
D8	O	1.8 V / 3.3 V ⁴	EMMC	EMMC_SCK	E5
L16	O	2.5 V or 3.3 V ⁵	ENET	ENET_MGMT_MDC	D6
K17	I/O	2.5 V or 3.3 V ⁵	ENET	ENET_MGMT_MDIO	D5
F16	I	2.5 V or 3.3 V ⁵	ENET	ENET1_RDATA0	A6
E17	I	2.5 V or 3.3 V ⁵	ENET	ENET1_RDATA1	B6
E16	I	2.5 V or 3.3 V ⁵	ENET	ENET1_RX_EN	A5
D15	I	2.5 V or 3.3 V ⁵	ENET	ENET1_RX_ER	C5
E15	O	2.5 V or 3.3 V ⁵	ENET	ENET1_TDATA0	A8
E14	O	2.5 V or 3.3 V ⁵	ENET	ENET1_TDATA1	B8
F14	O	2.5 V or 3.3 V ⁵	ENET	ENET1_TX_CLK	A7
F15	O	2.5 V or 3.3 V ⁵	ENET	ENET1_TX_EN	C7
C17	I	2.5 V or 3.3 V ⁵	ENET	ENET2_RDATA0	A2
C16	I	2.5 V or 3.3 V ⁵	ENET	ENET2_RDATA1	B2
B17	I	2.5 V or 3.3 V ⁵	ENET	ENET2_RX_EN	B1
D16	I	2.5 V or 3.3 V ⁵	ENET	ENET2_RX_ER	C1
A15	O	2.5 V or 3.3 V ⁵	ENET	ENET2_TDATA0	A4
A16	O	2.5 V or 3.3 V ⁵	ENET	ENET2_TDATA1	B4
D17	O	2.5 V or 3.3 V ⁵	ENET	ENET2_TX_CLK	A3
B15	O	2.5 V or 3.3 V ⁵	ENET	ENET2_TX_EN	C3

3: Use VSNVS_REF_OUT as reference voltage for BOOT_CFG resistors.

4: 3.3 V on TQMa6ULxL Rev. 01xx. 1.8 V on TQMa6ULxL Rev. 02xx.

5: 2.5 V if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V if NVCC_ENET is connected to VCC3V3_REF_OUT.

3.1.2.2 TQMa6ULxL signals (continued)

Table 3: TQMa6ULxL, signals (continued)

i.MX6UL ball	Dir.	Level	Group	Signal name	TQMa6ULxL
M15	I/O	3.3 V	GPIO	GPIO1_IO09	N17
K15	I/O	3.3 V	GPIO	GPIO1_IO18	M17
J14	I/O	3.3 V	GPIO	GPIO1_IO19	M16
E4	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO21	T7
E3	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO22	R7
E2	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO23	U6
E1	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO24 ⁷	R6
D4	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO25	P6
D3	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO26	U5
D2	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO27	T5
D1	I/O	1.8 V / 3.3 V ⁶	GPIO	GPIO4_IO28	R5
F3	I/O	3.3 V	I2C	I2C2_SCL	U8
F2	I/O	3.3 V	I2C	I2C2_SDA	U7
J17	I/O	3.3 V	I2C	I2C4_SCL	U11
J16	I/O	3.3 V	I2C	I2C4_SDA	T11
P15	I	3.3 V	JTAG	JTAG_MOD	G7
M14	I	3.3 V	JTAG	JTAG_TCK	J7
N16	I	3.3 V	JTAG	JTAG_TDI	G10
N15	O	3.3 V	JTAG	JTAG_TDO	G9
P14	I	3.3 V	JTAG	JTAG_TMS	G11
N14	I	3.3 V	JTAG	JTAG_TRST#	J11
A8	O	3.3 V	LCD	LCD_CLK	T1
B9	I/O	3.3 V ⁸	LCD	LCD_DATA00	R1
A9	I/O	3.3 V ⁸	LCD	LCD_DATA01	R2
E10	I/O	3.3 V ⁸	LCD	LCD_DATA02	R3
D10	I/O	3.3 V ⁸	LCD	LCD_DATA03	P1
C10	I/O	3.3 V ⁸	LCD	LCD_DATA04	P3
B10	I/O	3.3 V ⁸	LCD	LCD_DATA05	P4
A10	I/O	3.3 V ⁸	LCD	LCD_DATA06	N1
D11	I/O	3.3 V ⁸	LCD	LCD_DATA07	N2
B11	I/O	3.3 V ⁸	LCD	LCD_DATA08	N3
A11	I/O	3.3 V ⁸	LCD	LCD_DATA09	N4
E12	I/O	3.3 V ⁸	LCD	LCD_DATA10	M1
D12	I/O	3.3 V ⁸	LCD	LCD_DATA11	M3
C12	I/O	3.3 V ⁸	LCD	LCD_DATA12	M4
B12	I/O	3.3 V ⁸	LCD	LCD_DATA13	L1
A12	I/O	3.3 V ⁸	LCD	LCD_DATA14	L2
D13	I/O	3.3 V ⁸	LCD	LCD_DATA15	L3
C13	I/O	3.3 V ⁸	LCD	LCD_DATA16	L4
B13	I/O	3.3 V ⁸	LCD	LCD_DATA17	K1
A13	I/O	3.3 V ⁸	LCD	LCD_DATA18	K3
D14	I/O	3.3 V ⁸	LCD	LCD_DATA19	K4
C14	I/O	3.3 V ⁸	LCD	LCD_DATA20	J1
B14	I/O	3.3 V ⁸	LCD	LCD_DATA21	J2
A14	I/O	3.3 V ⁸	LCD	LCD_DATA22	J3
B16	I/O	3.3 V ⁸	LCD	LCD_DATA23	J4
B8	O	3.3 V	LCD	LCD_ENABLE	U2
D9	O	3.3 V	LCD	LCD_HSYNC	U3
E9	O	3.3 V	LCD	LCD_RESET	T4
C9	I/O	3.3 V	LCD	LCD_VSYNC	U4
A3	I/O	1.8 V / 3.3 V ⁹	QSPI	QSPI_A_DATA0	H2
C5	I/O	1.8 V / 3.3 V ⁹	QSPI	QSPI_A_DATA1	G2
B5	I/O	1.8 V / 3.3 V ⁹	QSPI	QSPI_A_DATA2	H1
A4	I/O	1.8 V / 3.3 V ⁹	QSPI	QSPI_A_DATA3	G1
D5	O	1.8 V / 3.3 V ⁹	QSPI	QSPI_A_SCK	H4
E6	O	1.8 V / 3.3 V ⁹	QSPI	QSPI_A_SS0# ¹⁰	G3
A5	O	1.8 V / 3.3 V ⁹	QSPI	QSPI_A_SS1# ¹¹	G4

- 6: 1.8 V if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V if NVCC_CSI is connected to VCC3V3_V33_OUT.
 7: Signal can be connected to PMIC_INT# or TEMP_EVENT# as an assembly option. Default: None.
 8: Use VCC3V3_REF_OUT as reference voltage for BOOT_CFG resistors.
 9: 3.3 V on TQMa6ULxL Rev. 01xx. 1.8 V on TQMa6ULxL Rev. 02xx.
 10: Only available when no QSPI NOR is assembled on the TQMa6ULxL.
 11: Only available on request, and when no eMMC is assembled on the TQMa6ULxL.

3.1.2.2 TQMa6ULxL signals (continued)

Table 3: TQMa6ULxL, signals (continued)

i.MX6UL ball	Dir.	Level	Group	Signal name	TQMa6ULxL
C1	O	3.3 V	SD	SD1_CLK	U10
C2	I/O	3.3 V	SD	SD1_CMD	R10
A2	I/O	3.3 V	SD	SD1_DATA3	R9
B1	I/O	3.3 V	SD	SD1_DATA2	T9
B2	I/O	3.3 V	SD	SD1_DATA1	U9
B3	I/O	3.3 V	SD	SD1_DATA0	P10
R10	I	3.0 V	SNVS	SNVS_TAMPER0	H14
R9	I	3.0 V	SNVS	SNVS_TAMPER1	J14
P11	I	3.0 V	SNVS	SNVS_TAMPER2	K14
P10	I	3.0 V	SNVS	SNVS_TAMPER3	N14
P9	I	3.0 V	SNVS	SNVS_TAMPER4	N15
N8	I	3.0 V	SNVS	SNVS_TAMPER5	P13
N11	I	3.0 V	SNVS	SNVS_TAMPER6	R13
N10	I	3.0 V	SNVS	SNVS_TAMPER7	P12
N9	I	3.0 V	SNVS	SNVS_TAMPER8	R12
R6	I	3.0 V	SNVS	SNVS_TAMPER9	P11
G13	I	3.3 V	SPI	SPI2_MISO	D11
F17	O	3.3 V	SPI	SPI2_MOSI	C11
G17	O	3.3 V	SPI	SPI2_SCLK	A11
G16	O	3.3 V	SPI	SPI2_SS0#	B11
K16	I	3.3 V	UART	UART1_RX_DATA	L16
K14	O	3.3 V	UART	UART1_TX_DATA	L17
H16	I	3.3 V	UART	UART3_RX_DATA	P16
H17	O	3.3 V	UART	UART3_TX_DATA	P17
E5	I	3.3 V	UART	UART6_RX_DATA	P8
F5	O	3.3 V	UART	UART6_TX_DATA	R8
U16	O	Open-Drain	USB	USB_OTG1_CHD#	D16
T15	I/O	3 V	USB	USB_OTG1_DN	E17
U15	I/O	3 V	USB	USB_OTG1_DP	G17
K13	I	3.3 V	USB	USB_OTG1_ID	F14
L15	I	3.3 V	USB	USB_OTG1_OC	G15
M16	O	3.3 V	USB	USB_OTG1_PWR	F15
T13	I/O	3 V	USB	USB_OTG2_DN	J17
U13	I/O	3 V	USB	USB_OTG2_DP	K17
M17	I	3.3 V	USB	USB_OTG2_ID / SD_VSEL ¹²	H15
L17	I	3.3 V	USB	USB_OTG2_OC	J15
L14	O	3.3 V	USB	USB_OTG2_PWR	H16
-	P	3.3 V	Power	VIN	A14, A15, A16, B14, B15, B16
-	P	3.3 V	Power	LICELL ¹³	C14
F4	P	1.8 V or 3.3 V ¹⁴	Power	NVCC_CSI	N5
F13	P	2.5 V or 3.3 V ¹⁵	Power	NVCC_ENET	E13
T12	P	5 V	Power	USB_OTG1_VBUS	F16
U12	P	5 V	Power	USB_OTG2_VBUS	K16
-	P	1.8 V	Power	VCC1V8_OUT	D9
-	P	2.5 V	Power	VCC2V5_OUT	D14
-	P	3.3 V	Power	VCC3V3_IN	A9, B9
-	P	3.3 V	Power	VCC3V3_REF_OUT	C10
-	P	3.3 V	Power	VCC3V3_V33_OUT	E14
-	P	1.4 V	Power	VCCCORE_OUT	D10
-	P	0.675 V	Power	VCCDDR_OUT	E15
-	P	3.0 V	Power	VSNVS_REF_OUT	C15
-	P	1.2 V	VDDARM_CAP	VDDARM_CAP	L7
-	P	1.2 V	VDDSOC_CAP	VDDSOC_CAP	L8, L11
-	P	0 V	Ground	DGND	A10, A12, A13, B10, B12, B13, B3, B5, B7, C12, C13, C16, C2, C4, C6, C8, D12, D13, D15, D17, D4, D7, D8, E16, E3, E6, F17, F5, G14, G16, G8, H11, H17, H3, H7, J16, K11, K15, K2, K7, L10, L9, M14, M2, N13, N16, P14, P2, P5, P7, P9, R11, R4, T10, T13, T15, T16, T2, T3, T6, T8

12: If USB_OTG2_ID is not used, it can be used to switch the NVCC_SD1 voltage level.

13: LICELL can be left open if RTC-Backup or another function of the SNVS domain is not used (see NXP documentation).

14: 1.8 V if NVCC_CSI is connected to VCC1V8_OUT. 3.3 V if NVCC_CSI is connected to VCC3V3_V33_OUT.

15: 2.5 V if NVCC_ENET is connected to VCC2V5_OUT. 3.3 V if NVCC_ENET is connected to VCC3V3_REF_OUT.

3.2 System components

3.2.1 i.MX6UL

3.2.1.1 i.MX6UL derivatives

Depending on the TQMa6ULxL derivative, one of the following i.MX6UL derivatives is assembled.

Table 4: i.MX6UL derivatives

CPU	Description	CPU clock	Temperature range
i.MX6UL	MCIMX6G1CVM	528 MHz	-40 °C ... +105 °C
	MCIMX6G2CVM	528 MHz	-40 °C ... +105 °C
	MCIMX6G3CVM	528 MHz	-40 °C ... +105 °C
i.MX6ULL	MCIMX6Y0CVM	528 MHz	-40 °C ... +105 °C
	MCIMX6Y1CVM	528 MHz	-40 °C ... +105 °C
	MCIMX6Y2CVM	528 MHz	-40 °C ... +105 °C


3.2.1.2 eFuses

The eFuses in the i.MX6UL are available for the user, except for the MAC address eFuses.

TQMa6ULxL modules are delivered pre-programmed with MAC addresses from the TQ-Systems MAC address pool.

The MAC address LOCK-FUSE WP (Write Protect) is burnt, which permits to temporarily overwrite the MAC address for test purposes. If this is not desired, the MAC address LOCK-FUSE OP (Overwrite Protect) can be burned by the user.

3.2.1.3 i.MX6UL errata

Attention: Destruction or malfunction, i.MX6UL errata	
	Please take note of the current i.MX6UL errata (5).

3.2.1.4 Boot Modes

The i.MX6UL contains a ROM with integrated boot loader.

After power-up, the boot code initializes the hardware and then loads the program image from the selected boot device.

The eMMC or the QSPI NOR flash integrated on the TQMa6ULxL can for example be selected as the standard boot device.

Additional boot interfaces are available as an alternative to booting from the integrated eMMC or the QSPI NOR flash, see 3.2.1.6.

More information about boot interfaces and its configuration is to be taken from the i.MX6UL documentation, see Table 42.

The boot device and its configuration, as well as different i.MX6UL settings have to be set via different boot registers.

Therefore, the i.MX6UL provides two possibilities:

- Burning internal eFuses
- Reading dedicated BOOT_CFG pins

The exact behaviour during booting depends on the value of register BT_FUSE_SEL (default = 0).

The following table shows the behaviour of bit BT_FUSE_SEL in dependence of the boot Mode selected.

Table 5: Boot Modes and BT_FUSE_SEL

BOOT_MODE[1:0]	Boot type	BT_FUSE_SEL	Usage
00 (default)	Boot from eFuses	BT_FUSE_SEL = 0: Boot using Serial Loader (default) BT_FUSE_SEL = 1: Boot configuration is taken from eFuses	Series production
01	Serial Downloader	n/a	Development / production
10	Internal Boot	BT_FUSE_SEL = 0: Boot configuration is taken from BOOT_CFG pins (default) BT_FUSE_SEL = 1: Boot configuration is taken from eFuses	Development
11	Reserved	n/a	n/a

3.2.1.5 Boot configuration

Some general settings are done with some eFuses independent from the boot device.

Table 6: General boot settings

i.MX6UL		TQMa6ULxL		
eFuse	Option	Setting ¹⁶	Signal name	Contact
BOOT_CFG1[7:0]	Boot configuration 1: Specific to selected boot Mode	–	LCD_DATA_7:0	–
BOOT_CFG2[7:3] BOOT_CFG2[1:0]	Boot configuration 2: Specific to selected boot Mode	–	LCD_DATA_15:11 LCD_DATA_9:8	–
BOOT_CFG2[2]	Boot frequencies (ARM / DDR): 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	LCD_DATA10	M1
BOOT_CFG3[7:0]	Reserved	–	–	–
BOOT_CFG4[6:0]	Boot configuration 4: Specific to selected boot Mode	–	LCD_DATA_22:16	–
BOOT_CFG4[7]	Debug loop: 0 = Loop disabled 1 = Loop enabled	0	LCD_DATA23	J4

Note: Boot configuration



No boot device is configured on the TQMa6ULxL at delivery.

3.2.1.6 Boot interfaces

In the next chapters, the configuration of the following boot devices is described:

- eMMC
- QSPI NOR flash
- SD card

¹⁶: Voltage level or condition of eFuse.

3.2.1.7 Boot device eMMC

Table 7: Boot configuration eMMC at USDHC2

i.MX6UL		TQMa6ULxL		
eFuse	Option	Setting ¹⁷	Signal name	Contact
BOOT_CFG1[7]	Boot Device Selection: 01 = Boot from USDHC Interface	0	LCD_DATA07	N2
BOOT_CFG1[6]		1	LCD_DATA06	N1
BOOT_CFG1[5]	SD/MMC Selection: 0 = SD/eSD/SDXC 1 = MMC/eMMC	1	LCD_DATA05	P4
BOOT_CFG1[4]	Fast Boot: 0 = Regular 1 = Fast boot	0	LCD_DATA04	P3
BOOT_CFG1[3]	MMC Speed: 0x = Normal Speed Mode 1x = High Speed Mode	0	LCD_DATA03	P1
BOOT_CFG1[2]		0	LCD_DATA02	R3
BOOT_CFG1[1]	eMMC Reset Enable: 0 = No action 1 = eMMC reset enabled (SD_RST pad)	0	LCD_DATA01	R2
BOOT_CFG1[0]	SD Loopback Clock Source Selection: 0 = Through SD pad 1 = Direct	0	LCD_DATA00	R1
BOOT_CFG2[7]	eMMC Bus Width: 000 = 1-bit 001 = 4-bit 010 = 8-bit 101 = 4-bit DDR (MMC 4.4) 110 = 8-bit DDR (MMC 4.4)	0	LCD_DATA15	L3
BOOT_CFG2[6]		1	LCD_DATA14	L2
BOOT_CFG2[5]		0	LCD_DATA13	L1
BOOT_CFG2[4]	Port Select: 00 = USDHC1 01 = USDHC2	0	LCD_DATA12	M4
BOOT_CFG2[3]		1	LCD_DATA11	M3
BOOT_CFG2[2]	Boot Frequencies (ARM / DDR): 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	LCD_DATA10	M1
BOOT_CFG2[1]	USDHC Voltage Selection: 0 = 3.3 V 1 = 1.8 V	0	LCD_DATA09	N4

In addition to the mode listed above the following eMMC modes are supported at port USDHC2.

Table 8: USDHC2 modes eMMC

eMMC mode	1 bit	4 bit	8 bit	8 bit DDR
Normal speed	Yes	Yes	Yes	Yes
High-Speed (HS)	Yes	Yes	Yes	n/a

¹⁷: Voltage level or condition of eFuse.

3.2.1.8 Boot device QSPI NOR flash

Table 9: Boot configuration QSPI NOR flash at QSPI1

i.MX6UL		TQMa6ULxL		
eFuse	Option	Setting ¹⁸	Signal name	Contact
BOOT_CFG1[7]	Boot Device Selection: 0001 = Boot from QuadSPI	0	LCD_DATA07	N2
BOOT_CFG1[6]		0	LCD_DATA06	N1
BOOT_CFG1[5]		0	LCD_DATA05	P4
BOOT_CFG1[4]		1	LCD_DATA04	P3
BOOT_CFG1[3]	QuadSPI Interface Selection: 0 = QSPI1 1 = Reserved	0	LCD_DATA03	P1
BOOT_CFG1[2]	DDRSMP: 000 = Default	0	LCD_DATA02	R3
BOOT_CFG1[1]		0	LCD_DATA01	R2
BOOT_CFG1[0]		0	LCD_DATA00	R1

18: Voltage level or condition of eFuse.

3.2.1.9 Boot device SD card

Table 10: Boot configuration SD card at USDHC1

i.MX6UL		TQMa6ULxL		
eFuse	Option	Setting ¹⁹	Signal name	Contact
BOOT_CFG1[7]	Boot Device Selection: 01 = Boot from USDHC Interface	0	LCD_DATA07	N2
BOOT_CFG1[6]		1	LCD_DATA06	N1
BOOT_CFG1[5]	SD/MMC Selection: 0 = SD/eSD/SDXC 1 = MMC/eMMC	0	LCD_DATA05	P4
BOOT_CFG1[4]	Fast Boot: 0 = Regular 1 = Fast boot	0	LCD_DATA04	P3
BOOT_CFG1[3]	SD Speed: 00 = Normal/SDR12 01 = High/SDR25 10 = SDR50 11 = SDR104	0	LCD_DATA03	P1
BOOT_CFG1[2]		1	LCD_DATA02	R3
BOOT_CFG1[1]	SD Power Cycle Enable: 0 = No power cycle 1 = Enable via USDHC_RST pad	0	LCD_DATA01	R2
BOOT_CFG1[0]	SD Loopback Clock Source Sel: 0 = through SD pad 1 = direct	0	LCD_DATA00	R1
BOOT_CFG2[7]	SD Calibration Step: 00 = 0 delay cells 01 = 1 delay cells 10 = 2 delay cells 11 = 3 delay cells	0	LCD_DATA15	L3
BOOT_CFG2[6]		0	LCD_DATA14	L2
BOOT_CFG2[5]	Bus Width: 0 = 1-bit 1 = 4-bit	1	LCD_DATA13	L1
BOOT_CFG2[4]	Port Select: 00 = USDHC1 01 = USDHC2	0	LCD_DATA12	M4
BOOT_CFG2[3]		0	LCD_DATA11	M3
BOOT_CFG2[2]	Boot Frequencies (ARM / DDR): 0 = 500 / 400 MHz 1 = 250 / 200 MHz	0	LCD_DATA10	M1
BOOT_CFG2[1]	USDHC Voltage Selection: 0 = 3.3 V 1 = 1.8 V	0	LCD_DATA09	N4

In addition to the mode listed above the following SD card modes are supported at port USDHC1.

Table 11: USDHC1 SD card modes

SD mode	Fast boot	1 bit	4 bit
Normal speed	Yes	Yes	Yes
High speed	Yes	Yes	Yes
SDR50	n/a	n/a	n/a
SDR104	n/a	n/a	n/a

¹⁹: Voltage level or condition of eFuse.

3.2.2 Memory

The TQMa6ULxL standard variant features the following memories:

- 256 Mbyte DDR3L SDRAM with 16 bit interface
- 64 Mbyte QSPI NOR flash
- 8 Gbyte eMMC NAND flash
- 64 kbit EEPROM
- 256 bytes EEPROM (128 byte for protection mode, 128 byte for normal usage)

3.2.2.1 DDR3L SDRAM

One DDR3L SDRAM chip is assembled on the TQMa6ULxL. The chip is connected to the i.MX6UL with a bus width of 16 bit. The following block diagram shows how the DDR3L SDRAM is connected to the i.MX6UL.

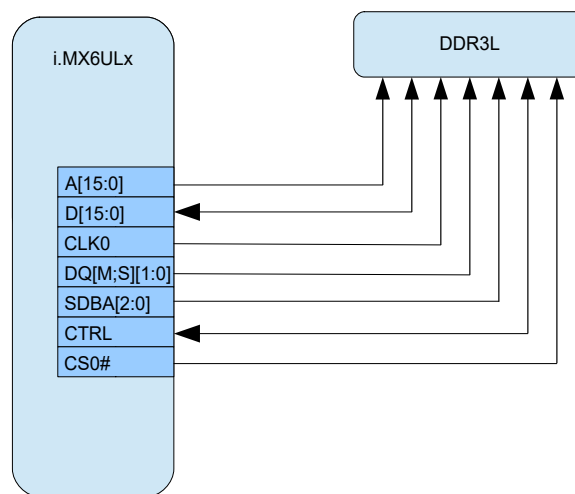


Figure 5: Block diagram DDR3L SDRAM interface

The memory interface characteristics are shown in the following table.

Table 12: i.MX6UL SDRAM interface

i.MX6UL derivative	Bus width	Frequency	No. of SDRAM chips
i.MX6UL	×16	400 MHz	1

The assembly options of DDR3L SDRAM on the TQMa6ULxL are listed in the following table.

Table 13: DDR3L SDRAM

Manufacturer	Part number	Type	Temperature range
Micron	MT41K128M16JT-125 IT:K	DDR3L-1600 128M16	-40 °C ... +95 °C
Samsung	K4B2G1646F-BMK0	DDR3L-1600 128M16	-40 °C ... +95 °C

3.2.2.2 eMMC NAND flash

An eMMC NAND flash is provided for the boot loader and the application software. The following block diagram shows how the eMMC flash is connected to the i.MX6UL.

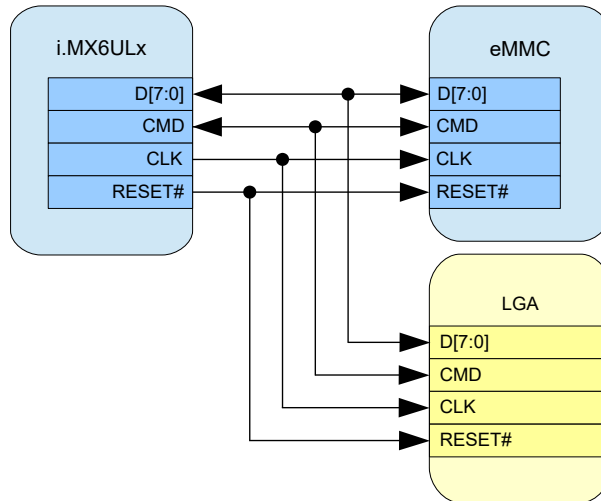


Figure 6: Block diagram eMMC interface


The Hardware Reset functionality depends on the BSP.

The following table shows the eMMC devices, which can be assembled on the TQMa6ULxL.

Table 14: eMMC NAND flash

Manufacturer	Part number	Type	Temperature range
Micron	MTFC8GAKAJCN-1M WT	8 Gbyte / eMMC 5.0 / MLC	-25 °C ... +85 °C
SanDisk	SDINBDG4-8G-T	8 Gbyte / eMMC 5.0 / MLC	-25 °C ... +85 °C

Attention: Destruction or malfunction, eMMC interface



The eMMC interface can only be used on the carrier board if the eMMC on the TQMa6ULxL is not assembled.

3.2.2.3 QSPI NOR flash

A QSPI NOR flash is also available. It can e.g., serve as boot device or as recovery device. The following block diagram shows how the QSPI NOR flash is connected to the i.MX6UL.

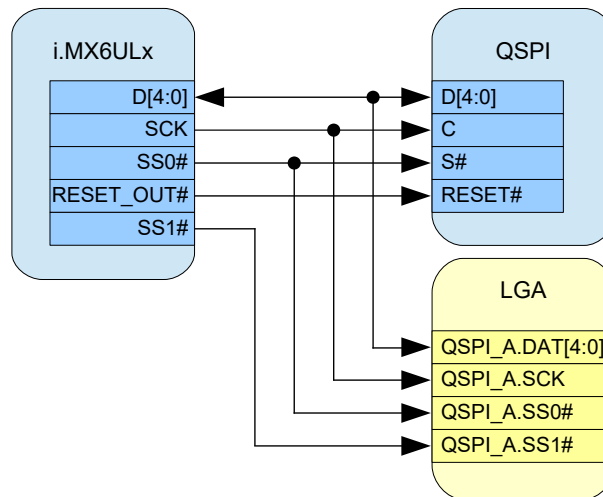



Figure 7: Block diagram QSPI NOR flash interface

The QSPI NOR flash Reset-Out pin as well as the QSPI signals are routed to the TQMa6ULxL contacts. See also 3.1.1.

The following table shows the QSPI NOR flash devices, which can be assembled on the TQMa6ULxL.

Table 15: QSPI NOR flash

Manufacturer	Part number	Size		Temperature range
Micron	MT25QL512ABB8E12-0SIT	512 Mbit	64 Mbyte	-40 °C ... +85 °C
Micron	MT25QL02GCBB8E12-0SIT	2048 Mbit	256 Mbyte	-40 °C ... +85 °C

Attention: Destruction or malfunction, QSPI NOR flash	
	<p>QSPI_A_SS1# is primarily used for the eMMC on the TQMa6ULxL. The BSP provided by TQ-Systems supports the Extended I/O protocol in STR mode.</p>

3.2.2.4 EEPROM 24LC64T

A serial EEPROM, controlled by the I2C4 bus, is assembled. Write-Protection (WP) is not supported by default but available as an assembly option. The following block diagram shows how the EEPROM is connected to the i.MX6UL.

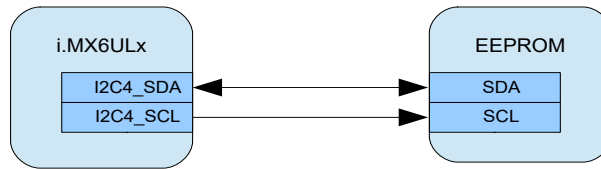


Figure 8: Block diagram EEPROM interface

- The EEPROM has I²C address 0x50 / 101 0000b

In the EEPROM, module-specific data is stored. It is, however, not essential for the correct operation of the TQMa6ULxL. The user can delete or alter the data. In the following table, the parameters stored in the EEPROM are shown.

Table 16: TQMa6ULxL specific data in the EEPROM

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	Variable	Variable	32 ₍₁₀₎	Binary	Hard Reset Configuration Word (HRCW), (optional)
0x20	6 ₍₁₀₎	10 ₍₁₀₎	16 ₍₁₀₎	Binary	MAC address
0x30	8 ₍₁₀₎	8 ₍₁₀₎	16 ₍₁₀₎	ASCII	Serial number
0x40	Variable	Variable	64 ₍₁₀₎	ASCII	Order code
0x80	–	–	8,064 ₍₁₀₎	–	(Unused)

3.2.2.5 EEPROM with temperature sensor, SE97BTP

A serial EEPROM including temperature sensor, controlled by the I2C4 bus, is assembled on the TQMa6ULxL.

The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write-Protected mode (PWP) or to Reversible Write-Protected mode (RWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage. The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa6ULxL.

The SE97BTP (D11) is assembled on the top side of the TQMa6ULxL, see Figure 21.

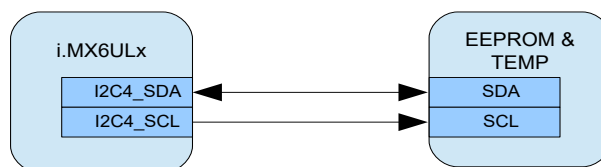


Figure 9: Block diagram EEPROM with temperature sensor, SE97BTP

- The device provides the following I²C addresses:
 - EEPROM (Normal Mode): 0x52 / 101 0010b
 - EEPROM (Protection Mode): 0x32 / 011 0010b
 - Temperature sensor: 0x1A / 001 1010b

3.2.3 i.MX6UL-internal RTC

The i.MX6UL provides an RTC, which has its own power domain (SNVS). The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The type FC-135 used on the TQMa6ULxL has a standard frequency tolerance of ± 20 ppm at +25 °C.

The following block diagram shows the implementation on the TQMa6ULxL.

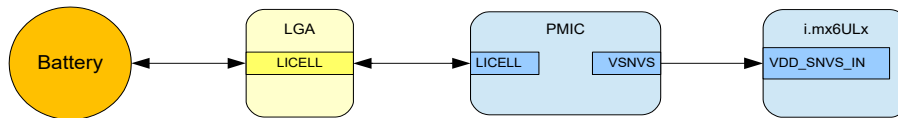



Figure 10: Block diagram i.MX6UL-internal RTC

The RTC power domain SNVS of the i.MX6UL is supplied by the PMIC-internal regulator VSNVS. This regulator is supplied either by VIN or by LICELL. LICELL supports simple coin cells as well as Lithium coin cells or SuperCaps, which can also be charged by the PMIC. Charging methods and electrical characteristics of the LICELL pin are to be taken from the PMIC Data Sheet (10).

Note: RTC power consumption	
	<p>A coin cell is not suitable for long term bridging on account of the high current consumption. A Lithium coin cell or a SuperCap[®] might be an option depending on the use case. It is to be taken note of that the typical charging current is only 60 μA. For long term bridging the discrete RTC on the TQMa6ULxL is recommended.</p>

3.2.4 Discrete RTC

In addition to the i.MX6UL-internal RTC the TQMa6ULxL provides a discrete RTC DS1339U, which is connected to I2C4. The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The type CM7V-T1A used on the TQMa6ULxL has a standard frequency tolerance of ± 20 ppm at +25 °C.

The following block diagram shows the implementation on the TQMa6ULxL.

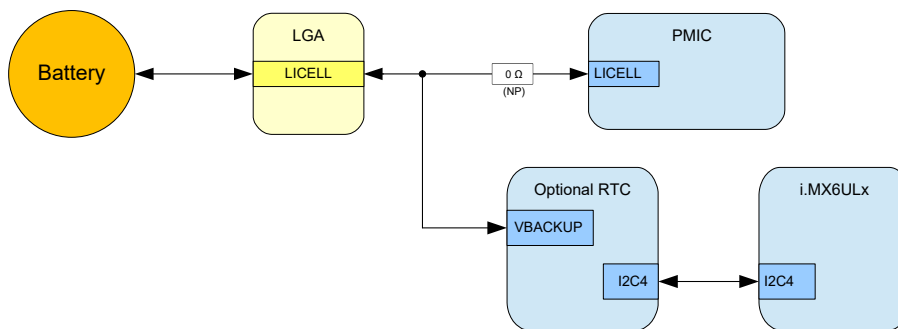



Figure 11: Block diagram discrete RTC

The discrete RTC is supplied with 3.3 V. VBACKUP of the RTC is available as LICELL at TQMa6ULxL contact C14. LICELL supports simple coin cells as well as Lithium coin cells or SuperCaps, which can also be charged by the PMIC. Charging methods and electrical characteristics of the LICELL pin are to be taken from the PMIC Data Sheet (10).

- The discrete RTC has I²C address 0x68 / 110 1000b

Note: RTC power consumption	
	<p>It is to be taken note of that the typical charging current is only 60 μA. A Lithium coin cell is recommended for long term bridging of the discrete RTC.</p>

3.2.5 Interfaces

3.2.5.1 Overview

The TQMa6ULxL provides interfaces with primary functions. They can all be used simultaneously independent of their configuration. Some primary functions are not available if a secondary function is used (e.g. EIM bus).

In the following chapters, only the external primary interfaces are described.

Table 17: Internal interfaces

Interface	Qty.	Function	Chapter	Remark
USDHC	1	Primary	3.2.5.13	USDHC2 eMMC, 8 data bits ²⁰
MMDC	1	Primary	3.2.2.1	DDR3L SDRAM, 16 data bits
QSPI	1	Primary	3.2.5.8	QSPI NOR flash, 4 data bits ²⁰

Table 18: External interfaces

Interface	Qty.	Function	Chapter	Remark
CCM	2	Secondary	–	Multiplexing has to be adapted
CSI	1	Secondary	–	Multiplexing has to be adapted
ECSPI	1	Primary	3.2.5.2	ECSPI2
ECSPI	2	Secondary	3.2.5.2	ECPSI1 / ECPSI3 / ECPSI4 Multiplexing has to be adapted
EIM	1	Secondary	–	Multiplexing has to be adapted
ENET	2	Primary	3.2.5.3	RMII (10/100 Mbit/s) / 1588 Multiplexing has to be adapted
EPIT	2	Secondary	–	Multiplexing has to be adapted
FLEXCAN	2	Primary	3.2.5.4	FLEXCAN[2:1]
GPIO	11	Primary	3.2.5.5	GPIO1 / GPIO4
GPT	2	Secondary	–	GPT[2:1] Multiplexing has to be adapted
I ² C	2	Primary	3.2.5.6	I2C2 / I2C4
I ² C	2	Secondary	3.2.5.6	I2C1 / I2C3 Multiplexing has to be adapted
KPP	1	Secondary	–	Multiplexing has to be adapted
LCDIF	1	Primary	3.2.5.7	Graphics interface
MQS	1	Secondary	–	Multiplexing has to be adapted
NAND	1	Secondary	–	Multiplexing has to be adapted
PWM	8	Secondary	–	PWM[8:1] Multiplexing has to be adapted
SAI	3	Secondary	–	SAI[3:1] Multiplexing has to be adapted
SIM	2	Secondary	–	Multiplexing has to be adapted
SJC	1	Primary	3.2.5.9	JTAG
SNVS	1	Primary	3.2.5.10	SNVS_TAMPER[9-0]
SRC	1	Secondary	–	Depends on BOOT_MODE0 BOOT_MODE1
SPDIF	1	Secondary	–	Multiplexing has to be adapted
UART	3	Primary	3.2.5.11	UART1 / UART3 / UART6
UART	5	Secondary	3.2.5.11	UART2 / UART4 / UART[8:7] Multiplexing has to be adapted
USB	2	Primary	3.2.5.12	USB_OTG1 / USB_OTG2
USDHC	1	Primary	3.2.5.13	SD card interface
WDOG	1	Primary	3.2.6	WDOG1#
WDOG	2	Secondary	–	WDOG[3:2] Multiplexing has to be adapted
XTALOSC	1	Primary	3.2.5.14	CCM_CLK1_N / CCM_CLK1_P

²⁰: Corresponding LGA pads can be configured for external interfaces, if TQMa6ULxL-internal interfaces are not used.

3.2.5.2 ECSPi

The i.MX6UL provides four full-duplex ECSPi interfaces, which can also be configured as Master/Slave.

Primarily ECSPi2 is available at the TQMa6ULxL contacts.

The following table shows the signals used by the ECSPi2 interface.

Table 19: ECSPi2 signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL
ECSPi2_MISO	I	G13	D11
ECSPi2_MOSI	O	F17	C11
ECSPi2_SCLK	O	G17	A11
ECSPi2_SS0#	O	G16	B11

3.2.5.3 Ethernet

The i.MX6UL provides a 10/100 MAC core, which supports MII (4 bit) and RMII (2 bit).

The RMII signals are available as primary function at the TQMa6ULxL contacts.

The following table shows the signals used by the RMII interface.

Table 20: RMII signals

Signal name	Power-Group	Direction	i.MX6UL ball	TQMa6ULxL
ENET_MDC	NVCC_GPIO (3.3 V)	O	L16	D6
ENET_MDIO		I/O	K17	D5
ENET1_RDATA0	NVCC_ENET (2.5 V or 3.3 V)	I	F16	A6
ENET1_RDATA1		I	E17	B6
ENET1_RX_EN		I	E16	A5
ENET1_RX_ER		I	D15	C5
ENET1_TDATA0		O	E15	A8
ENET1_TDATA1		O	E14	B8
ENET1_TX_CLK		O	F14	A7
ENET1_TX_EN		O	F15	C7
ENET2_RDATA0		I	C17	A2
ENET2_RDATA1		I	C16	B2
ENET2_RX_EN		I	B17	B1
ENET2_RX_ER		I	D16	C1
ENET2_TDATA0		O	A15	A4
ENET2_TDATA1		O	A16	B4
ENET2_TX_CLK		O	D17	A3
ENET2_TX_EN		O	B15	C3

Note: NVCC_ENET, VCC3V3_REF_OUT



NVCC_ENET has to be connected externally!
VCC3V3_REF_OUT has to supply an RMII PHY on the MBa6ULx with approximately 60 mA. It has to be ensured that the load on the customer's carrier board is not higher than approximately 60 mA.

The i.MX6UL RMII interface can operate with an I/O voltage of 2.5 V or 3.3 V. In order to use the interface, additional signals of the ENET signal group are required. The accompanying power supply pin is routed to TQMa6ULxL contact E13 to operate these signals on the same I/O voltage, if RMII is used. The MII interface can be used with an adapted pin multiplexing. Details are to be taken from the i.MX6UL documentation (see Table 42).

3.2.5.4 CAN

The i.MX6UL provides two integrated CAN 2.0B controllers. Both signals pairs are available at the TQMa6ULxL contacts. The signal drivers required have to be implemented on the carrier board. The following table shows the signals used by the CAN interface.

Table 21: FLEXCAN signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL
FLEXCAN1_RX	I	G14	R16
FLEXCAN1_TX	O	H15	R17
FLEXCAN2_RX	I	H14	T12
FLEXCAN2_TX	O	J15	U12

3.2.5.5 GPIO

Beside their interface function, most i.MX6UL pins can also be configured as GPIO. All GPIOs can trigger an interrupt. The electrical characteristics of the GPIOs are to be taken from the i.MX6UL documentation see Table 42. Several pins are available as GPIO at the TQMa6ULxL contacts. The following table shows the GPIO signals provided.

Table 22: GPIO signals

Signal name	Power-Group	Direction	i.MX6UL ball	TQMa6ULxL	Remark
GPIO1_IO09	3.3 V	I/O	M15	N17	–
GPIO1_IO18		I/O	K15	M17	Alternative function: USDHC1_WP
GPIO1_IO19		I/O	J14	M16	Alternative function: USDHC1_CD#
GPIO4_IO21	NVCC_CSI (1.8 V or 3.3 V)	I/O	E4	T7	–
GPIO4_IO22		I/O	E3	R7	–
GPIO4_IO23		I/O	E2	U6	–
GPIO4_IO24 ²¹		I/O	E1	R6	Assembly option: PMIC_INT# or TEMP_EVENT#
GPIO4_IO25		I/O	D4	P6	–
GPIO4_IO26		I/O	D3	U5	–
GPIO4_IO27		I/O	D2	T5	–
GPIO4_IO28		I/O	D1	R5	–

Note: NVCC_CSI



NVCC_CSI has to be connected externally!

21: Can be used as temperature and PMIC interrupt. For more information please contact [TQ-Support](#).

3.2.5.6 I²C

The i.MX6UL provides four I²C interfaces.

I2C2 and I2C4 are available as primary function and routed to the TQMa6ULxL contacts.

The following table shows the signals used by the I²C interfaces.

Table 23: I²C signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL	Power-Group	Remark
I2C2_SCL	O	F3	U8	NVCC_CSI (1.8 V or 3.3 V)	–
I2C2_SDA	I/O	F2	U7		–
I2C4_SCL	O	J17	U11	3.3 V	PU 2.2 kΩ to 3.3 V on TQMa6ULxL
I2C4_SDA	I/O	J16	T11		PU 2.2 kΩ to 3.3 V on TQMa6ULxL

Note: NVCC_CSI



NVCC_CSI has to be connected externally!

The following table shows the I²C devices connected to the I2C4 bus on the TQMa6ULxL.

Table 24: I2C4 bus addresses

Component	7-bit address
EEPROM (M24C64)	0x50 / 101 0000b
PMIC (MC32PF3000A7EP)	0x08 / 000 1000b
RTC (DS1339U-33) (optional)	0x68 / 110 1000b
EEPROM (SE97BTP) (Normal Mode)	0x52 / 101 0010b
EEPROM (SE97BTP) (Protection Mode)	0x32 / 011 0010b
Temperature sensor in EEPROM (SE97BTP)	0x1A / 001 1010b

If more devices are connected to the I2C4 bus on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional Pull-Ups should be provided at the I²C bus on the carrier board, if required.

3.2.5.7 eLCDIF

The i.MX6UL provides a display controller, which supports displays of different size and performance. Information regarding types of displays and supported formats are to be taken from the i.MX6UL Reference Manual (2). The LCD signals routed to the TQMa6ULxL contacts as primary function. The following table shows the signals used by the LCD interface.

Table 25: LCD signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL
LCDIF_DATA23	I/O	B16	J4
LCDIF_DATA22	I/O	A14	J3
LCDIF_DATA21	I/O	B14	J2
LCDIF_DATA20	I/O	C14	J1
LCDIF_DATA19	I/O	D14	K4
LCDIF_DATA18	I/O	A13	K3
LCDIF_DATA17	I/O	B13	K1
LCDIF_DATA16	I/O	C13	L4
LCDIF_DATA15	I/O	D13	L3
LCDIF_DATA14	I/O	A12	L2
LCDIF_DATA13	I/O	B12	L1
LCDIF_DATA12	I/O	C12	M4
LCDIF_DATA11	I/O	D12	M3
LCDIF_DATA10	I/O	E12	M1
LCDIF_DATA09	I/O	A11	N4
LCDIF_DATA08	I/O	B11	N3
LCDIF_DATA07	I/O	D11	N2
LCDIF_DATA06	I/O	A10	N1
LCDIF_DATA05	I/O	B10	P4
LCDIF_DATA04	I/O	C10	P3
LCDIF_DATA03	I/O	D10	P1
LCDIF_DATA02	I/O	E10	R3
LCDIF_DATA01	I/O	A9	R2
LCDIF_DATA00	I/O	B9	R1
LCDIF_CLK	O	A8	T1
LCDIF_ENABLE	O	B8	U2
LCDIF_HSYNC	O	D9	U3
LCDIF_RESET	O	E9	T4
LCDIF_VSYNC	O	C9	U4

Attention: Destruction or malfunction, faulty boot procedure or malfunction



To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the power-up sequence is indicated by a high level of signal VCC3V3_REF_OUT. Suitable precautions have to be implemented on the carrier board to avoid violations caused e.g. by a display connected at the boot configuration pins. It also has to be ensured that the circuitry at the boot configuration pins (e.g., Pull-Downs) does not interfere with the function of a display connected at these pins.

3.2.5.8 QSPI

The optional QSPI NOR flash on the TQMa6ULxL is connected to the i.MX6UL QSPI interface.

The QSPI interface is also routed to the TQMa6ULxL contacts to add more NOR flash on the carrier board.

QSPI_A_SS1# is only available on request and when no eMMC is assembled on the TQMa6ULxL.

The following table shows the signals used by the QSPI interface.

Table 26: QSPI signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL	Remark
QSPI_A_DATA3	I/O	A4	G1	–
QSPI_A_DATA2	I/O	B5	H1	–
QSPI_A_DATA1	I/O	C5	G2	–
QSPI_A_DATA0	I/O	A3	H2	–
QSPI_A_SS1#	O	A5	G4	Only available when no eMMC is assembled on the TQMa6ULxL
QSPI_A_SS0#	O	E6	G3	Only available when no QSPI NOR is assembled on the TQMa6ULxL
QSPI_A_SCK	O	D5	H4	–

Attention: Destruction or malfunction QSPI interface



The QSPI signal pins of the TQMa6ULxL have to be treated as NC, if not used on the carrier board. QSPI_A_SS1# can only be used on the carrier board, if no eMMC is assembled on the TQMa6ULxL. The QSPI interface may only be used as a memory interface. SPI devices can be connected to the eCSPI interfaces.

3.2.5.9 SJC

The i.MX6UL can operate in two different JTAG modes. The pin JTAG_MOD defines the mode.

The following table shows the modes as well as the mode set on the TQMa6ULxL.

Table 27: JTAG modes

JTAG_MOD	Name	Remark
0 (default)	Daisy Chain All	For common SW debug (High speed and series production) ⇒ default
1	SJC only	IEEE® 1149.1 JTAG compliant mode

The following table shows the signals used by the JTAG interface.

Table 28: JTAG signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL	Remark
JTAG_TCK	I	M14	J7	i.MX6UL-internal PU 47 kΩ
JTAG_TMS	I	P14	G11	i.MX6UL-internal PU 47 kΩ
JTAG_TDI	I	N16	G10	i.MX6UL-internal PU 47 kΩ
JTAG_TDO	O	N15	G9	i.MX6UL-internal keeper
JTAG_TRST#	I	N14	J11	i.MX6UL-internal PU 47 kΩ
JTAG_MOD	I	P15	G7	PD 4.7 kΩ on TQMa6ULxL + i.MX6UL-internal PU 100 kΩ

3.2.5.10 TAMPER

The i.MX6UL provides protection against unauthorised opening or manipulation of a device by tamper detection.

The TAMPER pins are available at the TQMa6ULxL contacts. Details about the TAMPER pins function are to be taken from the i.MX6UL Reference Manual (2). The following table shows the available signals.

Table 29: TAMPER signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL
SNVS_TAMPER9	I	R6	P11
SNVS_TAMPER8	I	N9	R12
SNVS_TAMPER7	I	N10	P12
SNVS_TAMPER6	I	N11	R13
SNVS_TAMPER5	I	N8	P13
SNVS_TAMPER4	I	P9	N15
SNVS_TAMPER3	I	P10	N14
SNVS_TAMPER2	I	P11	K14
SNVS_TAMPER1	I	R9	J14
SNVS_TAMPER0	I	R10	H14

3.2.5.11 UART

The i.MX6UL provides eight UART interfaces. No handshake signals are configured as primary function. More UARTs as well as handshake signals can be configured in the multiplexing. Details are to be taken from the i.MX6UL Reference Manual (2).

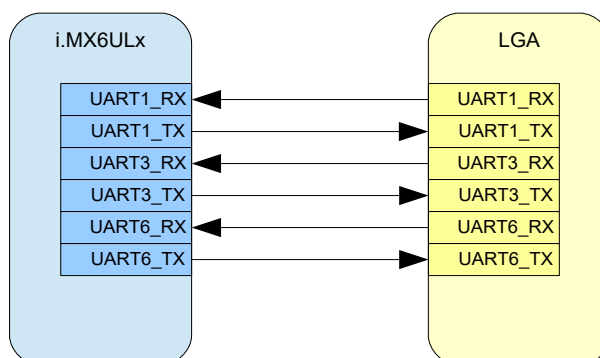


Figure 12: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces.

Table 30: UART signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL
UART1_RX_DATA	I	K16	L16
UART1_TX_DATA	O	K14	L17
UART3_RX_DATA	I	H16	P16
UART3_TX_DATA	O	H17	P17
UART6_RX_DATA	I	E5	P8
UART6_TX_DATA	O	F5	R8

Note: UART1



UART1 is configured as RS-232 on the MBa6ULx.

3.2.5.12 USB

The i.MX6UL provides two independent USB-OTG controllers with integrated High-Speed PHY. Both controllers can operate in Host or in Device mode. The signals of both controllers are available at the TQMa6ULxL contacts as primary function.

The following table shows the signals used by the USB_OTG interfaces:

Table 31: USB_OTG signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL	Remark
USB_OTG1_CHD#	O	U16	D16	–
USB_OTG1_ID	I	K13	F14	Device Mode: USB_OTG_ID signal is high Host Mode: USB_OTG_ID signal is low
USB_OTG1_OC	I	L15	G15	–
USB_OTG1_PWR	O	M16	F15	–
USB_OTG1_VBUS	P	T12	F16	–
USB_OTG1_DN	I/O	T15	E17	–
USB_OTG1_DP	I/O	U15	G17	–
USB_OTG2_ID ²²	I	M17	H15	Device Mode: USB_OTG_ID signal is high Host Mode: USB_OTG_ID signal is low
USB_OTG2_OC	I	L17	J15	–
USB_OTG2_PWR	O	L14	H16	–
USB_OTG2_VBUS	P	U12	K16	–
USB_OTG2_DN	I/O	T13	J17	–
USB_OTG2_DP	I/O	U13	K17	

Note: USB mode



Currently the [BSP provided](#) by TQ-Systems only supports the Host mode.

22: If USB_OTG2_ID is not used, it can be used to switch the NVCC_SD1 voltage level.

3.2.5.13 USDHC

The i.MX6UL provides a USDHC controller, which is the interface between Host system and SD/SDIO/MMC cards. The i.MX6UL USDHC1 port is routed to the TQMa6ULxL contacts, to connect an MMC, SD, or SDIO card.

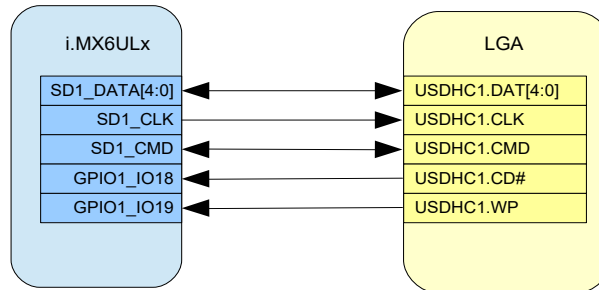


Figure 13: Block diagram USDHC interface

The following table shows the signals used by the USDHC interface.

Table 32: USDHC1 signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL	Remark
USDHC1_CLK	O	C1	U10	–
USDHC1_CMD	I/O	C2	R10	–
USDHC1_DATA3	I/O	A2	R9	–
USDHC1_DATA2	I/O	B1	T9	–
USDHC1_DATA1	I/O	B2	U9	–
USDHC1_DATA0	I/O	B3	P10	–
USDHC1_CD#	I	J14	M17	Default: Muxed as GPIO1_IO18
USDHC1_WP	I	K15	M16	Default: Muxed as GPIO1_IO19

3.2.5.14 XTAL

The i.MX6UL provides a programmable differential clock output, which is routed to the TQMa6ULxL contacts. CCM_CLK1_N/P can be configured as differential (LVDS) clock input or clock output.

The following table shows details of the XTAL signals.

Table 33: XTAL signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL
CCM_CLK1_N	O	P16	C17
CCM_CLK1_P	O	P17	B17

3.2.6 Reset signals

Reset inputs or outputs are available at the TQMa6ULxL contacts.
A red LED on the TQMa6ULxL indicates the RESET# condition.

The following block diagram shows the wiring of the reset signals.

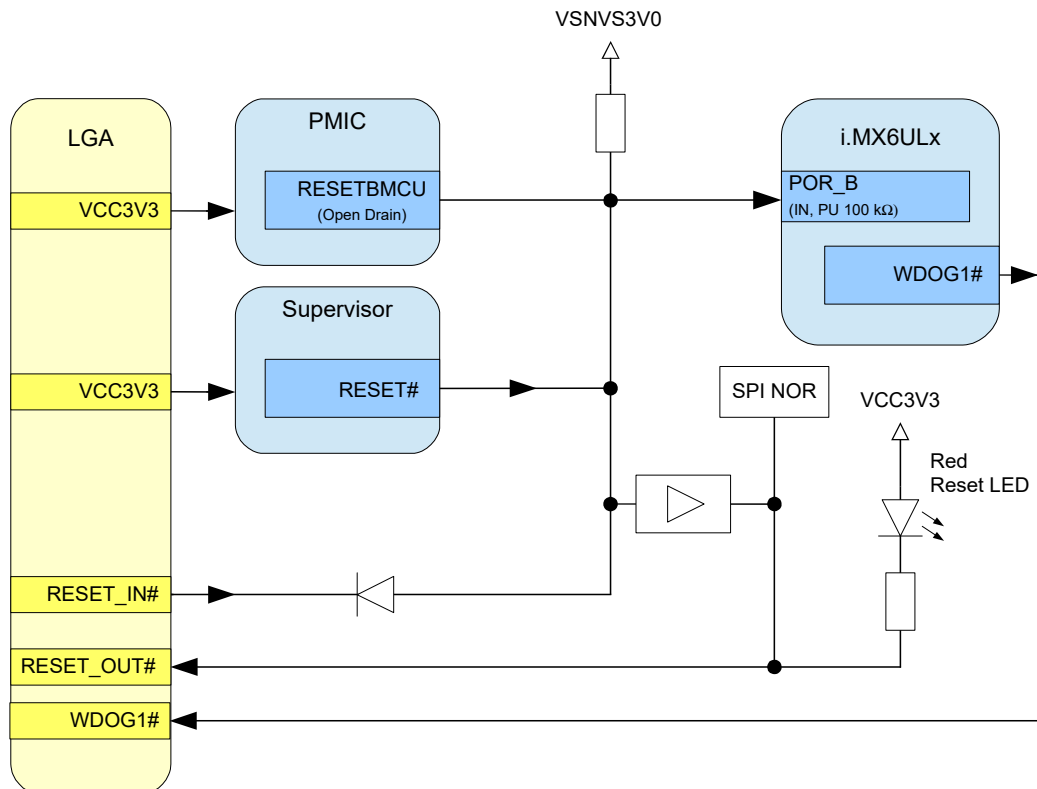


Figure 14: Block diagram Reset

The following table describes the reset signals available at the TQMa6ULxL contacts:

Table 34: Reset signals

Signal name	Direction	i.MX6UL ball	TQMa6ULxL	Remark
RESET_IN#	I _{PU 100kΩ}	P8	T14	<ul style="list-style-type: none"> Reset input POR_B (Power-On Reset) of the i.MX6UL Triggers COLD-Reset of the i.MX6UL Low-active signal Minimal duration to trigger a reliable Reset: app. 30 μs, see (2)
RESET_OUT#	O	–	U15	<ul style="list-style-type: none"> Reset output RESETBMCU of the PMIC Can be used to reset external periphery
WDOG1#	O	N17	C9	<ul style="list-style-type: none"> Low-active signal Triggers Reset of the i.MX6UL in error case

Other RESET# sources are:

- VIN – RESET#
- PMIC – RESETBMCU

3.2.7 Power supply

3.2.7.1 TQMa6ULxL power supply

The TQMa6ULxL requires a supply voltage of 3.3 V \pm 5 %.

The following block diagram shows the TQMa6ULxL power supply.

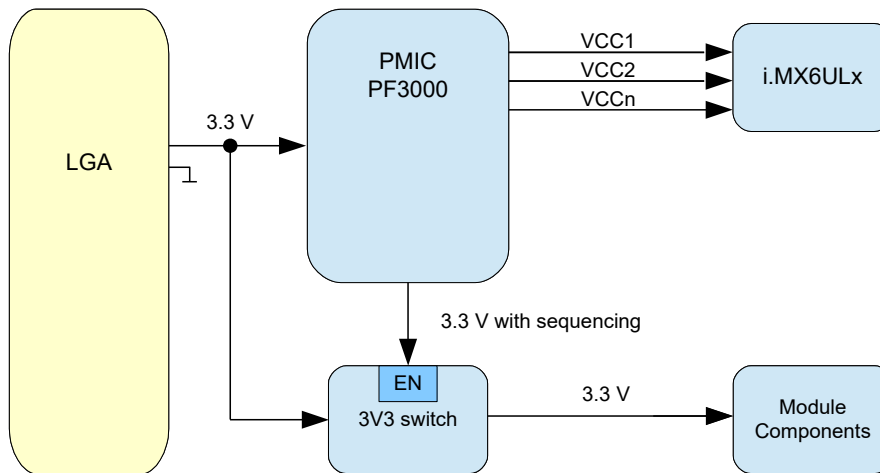


Figure 15: Block diagram TQMa6ULxL power supply

The characteristics and functions of the single pins and signals are to be taken from the PMIC Data Sheet (10) and the i.MX6UL Reference Manual (2).

3.2.7.2 TQMa6ULxL power consumption

The given power consumption has to be seen as an approximate value. The TQMa6ULxL power consumption strongly depends on the application, the mode of operation and the operating system.

The following table shows TQMa6ULxL power supply and power consumption parameters:


Table 35: TQMa6ULxL power consumption

Mode of operation	Current at 3.3 V	Power at 3.3 V	Remark
Theoretical calculated peak	2015 mA	6650 mW	–
U-Boot prompt	123 mA	406 mW	–
Linux prompt	83 mA	275 mW	–
Linux stress test	163 mA	537 mW	No external interfaces active
Suspend to RAM	16 mA	53 mW	–
Standby	25 mA	84 mW	–

3.2.7.3 Voltage monitoring

The TQMa6ULxL features a supervisor which monitors the input voltage (VIN). If the input voltage is too low, a Reset is triggered until the input voltage is in the permitted range again. The block diagram in Figure 14 shows the wiring.

The Supervisor triggers typically at 2.93 V (min: 2.87 V / max: 2.99 V) and has a delay of 200 msec. All other voltages generated on the TQMa6ULxL are routed to the TQMa6ULxL contacts and can be monitored on the carrier board.

Attention: Destruction or malfunction, supply voltage exceedance	
	<p>The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa6ULxL.</p>

3.2.7.4 TQMa6ULxL supply voltages

In addition to the TQMa6ULxL supply voltage (VIN), some internal voltages are provided at the TQMa6ULxL contacts. The following table shows the voltages provided.

Table 36: TQMa6ULxL supply voltages

Voltage	TQMa6ULxL	Remark
NVCC_CSI	N5	–
NVCC_ENET	E13	–
VCC1V8_OUT	D9	Max. load 100 mA
VCC2V5_OUT	D14	Max. load 100 mA
VCC3V3_IN	A9, B9	Used on TQMa6ULxL, switched on by VCC3V3_V33_OUT
VCC3V3_REF_OUT	C10	Pull-Up voltage for LCD.DAT[24:0] „Enable“ for VCC3V3_IN (3.3 V) switch-through
VCC3V3_V33_OUT	E14	Reference only, no additional load
VCCCORE_OUT	D10	Reference only, no additional load
VCCDDR_OUT	E15	Reference only, no additional load
VDDARM_CAP	L7	No additional load
VDDSOC_CAP	L8, L11	No additional load
VSNVS_REF_OUT	C15	Pull-Up voltage for BOOTMODE[1:0] Pull-Up voltage for EXT_WAKEUP

3.2.7.5 Other supply voltages

In addition to the 3.3 V VIN, the TQMa6ULxL offers voltage inputs for the USB OTG controllers.

Table 37: TQMa6ULxL USB_OTG supply voltages


Signal name	Direction	TQMa6ULxL	Remark
USB_OTG1_VBUS	P	F16	VBUS voltage for USB controller For details see i.MX6UL data sheet (1)
USB_OTG2_VBUS	P	K16	

3.2.7.6 Power-Up sequence TQMa6ULxL / carrier board

The TQMa6ULxL meets the required sequencing of the i.MX6UL by using the PMIC (10).

The TQMa6ULxL operates at 3.3 V; the 3.3 V I/O voltage of the i.MX6UL signals is generated on the TQMa6ULxL.

This leads to requirements for the carrier board design concerning the chronological characteristics of the voltages generated on the carrier board.

Attention: Destruction or malfunction, Power-Up sequence	
	<p>To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed.</p> <p>The end of the power-up sequence is indicated by a high level of signal VCC3V3_REF_OUT.</p> <p>To ensure a correct power-up, the following sequence must be met on the carrier board:</p> <p>The supply voltage of 3.3 V for the TQMa6ULxL is present and the carrier board supply of 3.3 V is activated by the TQMa6ULxL pin VCC3V3_REF_OUT. This activates the 3.3 V on the carrier board.</p>

The following block diagram shows the voltage regulator control on the MBa6ULx:

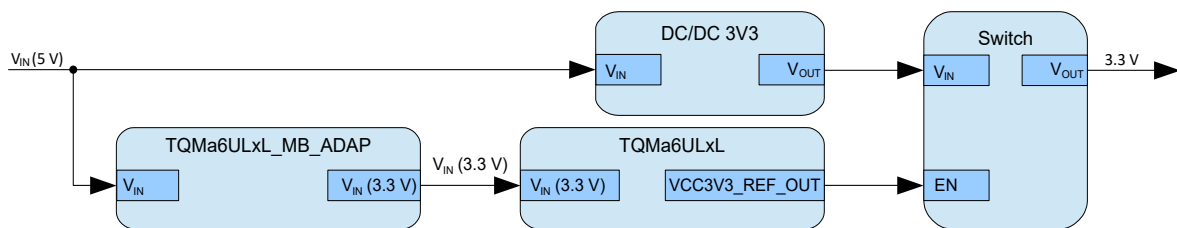


Figure 16: Block diagram power supply carrier board

- The BOOT_MODE and BOOT_CFG pins have dedicated reference voltages, which are present at the right time. See also schematics of MBa6ULx.

3.2.7.7 Power modes

- Suspend to RAM (deep sleep mode – DSM)
- Standby

DSM und Standby are extremely efficient energy saving modes, in which parts of the core supply are switched off. Details are to be taken from the i.MX6UL Reference Manual (2). These features have to be supported by the software.

3.2.7.8 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX6UL Reference Manual (2) and the PMIC Data Sheet (10). The PMIC is connected to the I2C4 bus.

The following block diagram shows the connection between PMIC and i.MX6UL:

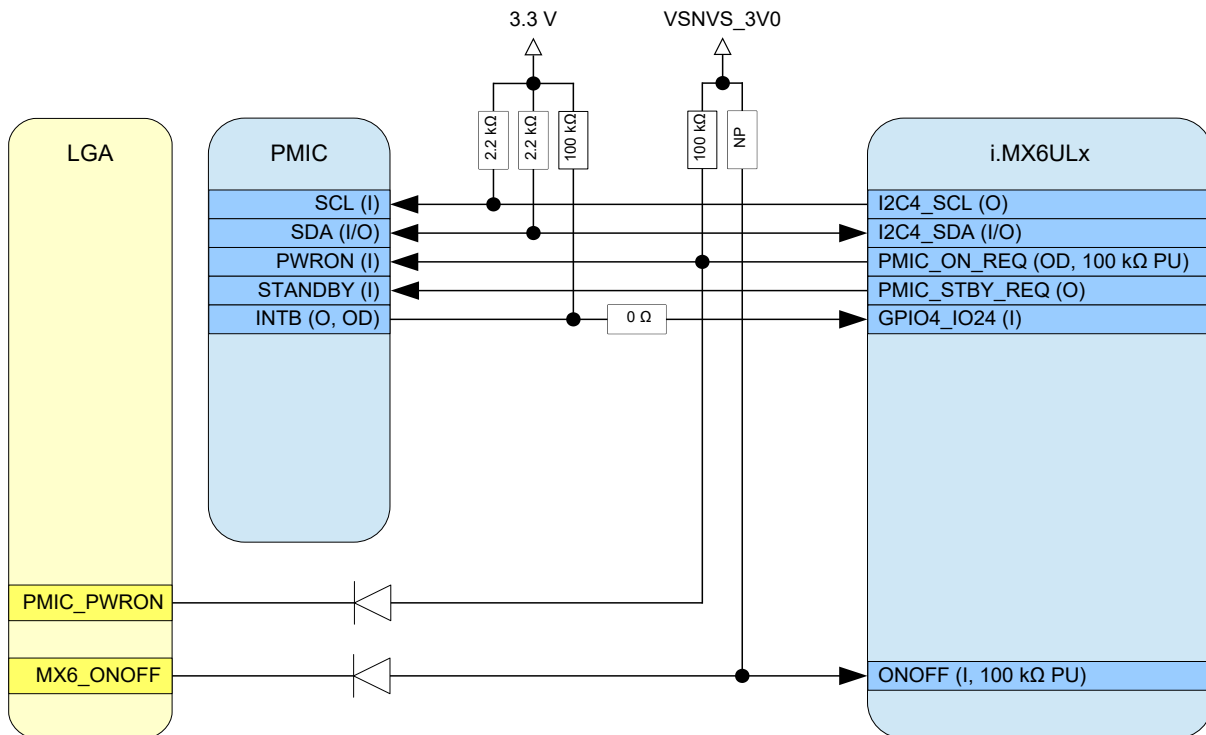


Figure 17: Block diagram PMIC interface

- The PMIC has I²C address 0x08 / 000 1000b

Note: PMIC INTB



Signal PMIC INTB is routed to GPIO4_IO24, depending on TQMa6ULxL derivative. Contact [TQ-Support](#) for detailed information.

Attention: Destruction or malfunction, PMIC programming



Improper programming of the PMIC may result in the i.MX6UL or periphery being operated outside its specification. This leads to malfunctions, accelerated aging or destruction of the TQMa6ULxL.

4. MECHANICS

4.1 Dimensions

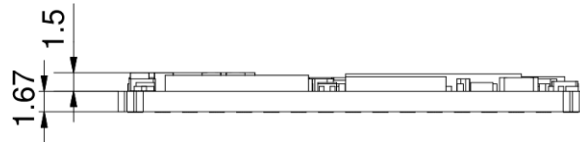


Figure 18: TQMa6ULxL dimensions side view

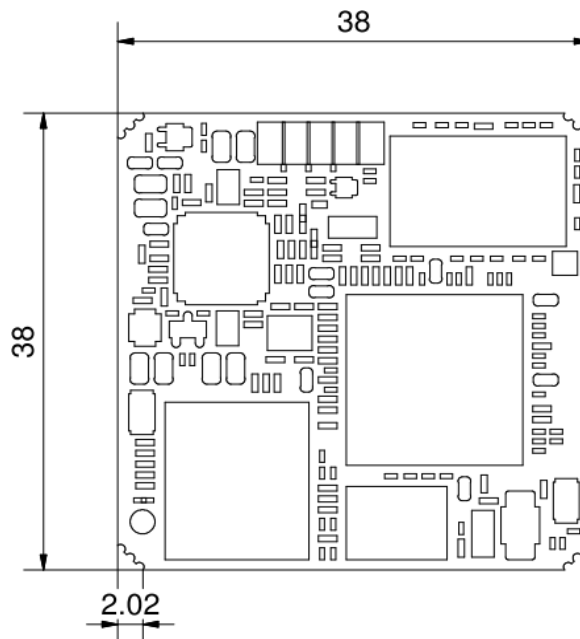


Figure 19: TQMa6ULxL dimensions, top view

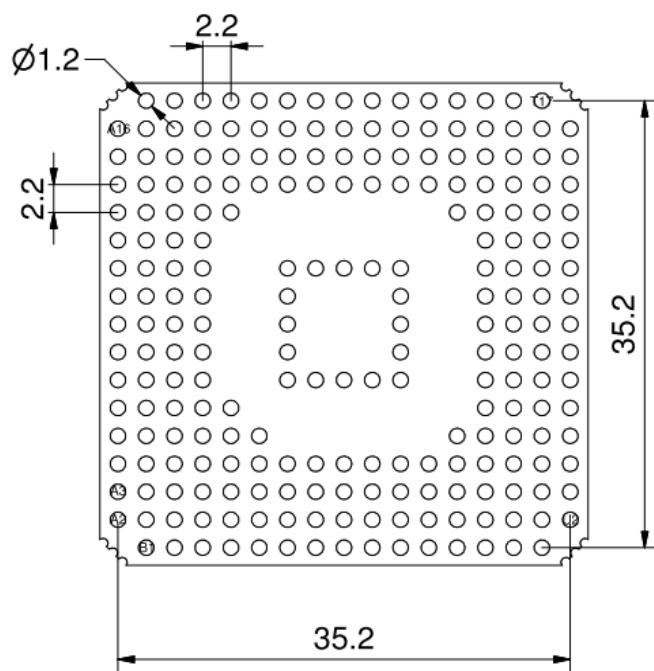


Figure 20: TQMa6ULxL dimensions, top view through TQMa6ULxL

4.2 Component placement

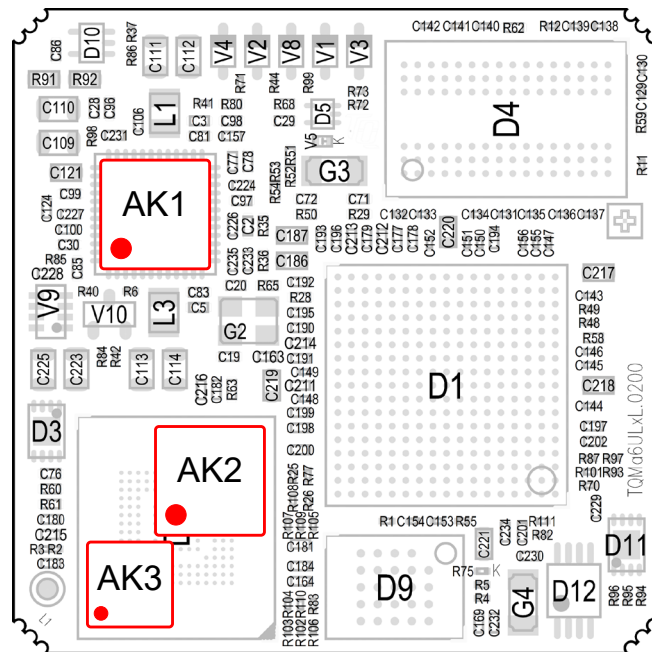


Figure 21: TQMa6ULxL, component placement top

The labels on the TQMa6ULxL show the following information:

Table 38: Labels on TQMa6ULxL

Label	Text
AK1	MAC address + tests performed
AK2	TQMa6ULxL version and revision
AK3	Serial number

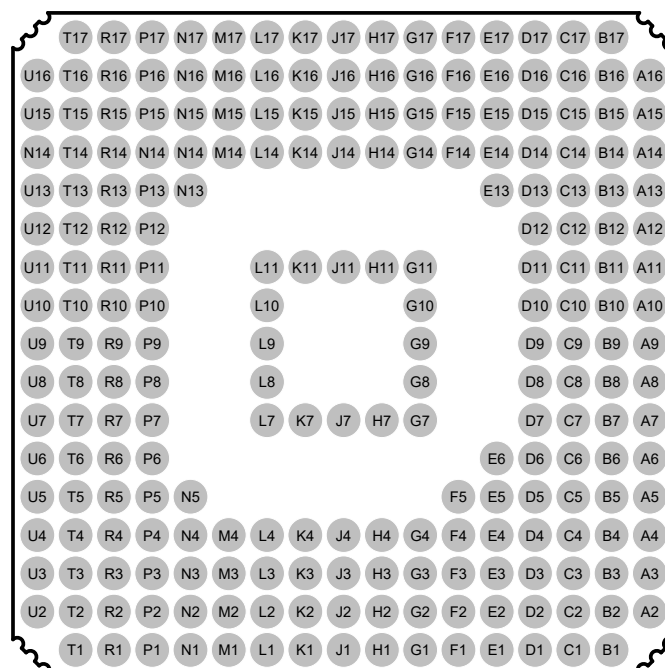


Figure 22: TQMa6ULxL, contact numbering scheme, bottom view

4.3 Adaptation to the environment


The TQMa6ULxL has overall dimensions (length × width × height) of 38 × 38 mm × 3.3 mm³.
The TQMa6ULxL has a maximum height above the carrier board of approximately 3.3 mm.
The TQMa6ULxL weighs approximately 8 grams.

4.4 Protection against external effects

As an embedded module, the TQMa6ULxL is not protected against dust, external impact and contact (IP00). Adequate protection has to be guaranteed by the surrounding system.

4.5 Thermal management

To cool the TQMa6ULxL, a theoretical maximum of approximately 6.65 W have to be dissipated, see Table 35. The power dissipation originates primarily in the i.MX6UL, the DDR3L SDRAM and the PMIC. The power dissipation also depends on the software used and can vary according to the application. See NXP documents in Table 42 for further information.

Attention: Destruction or malfunction, TQMa6ULxL cooling	
	<p>The i.MX6UL belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).</p> <p>Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX6UL must be taken into consideration when connecting the heat sink, see (8). The i.MX6UL is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa6ULxL and thus malfunction, deterioration or destruction.</p>

4.6 Structural requirements

The TQMa6ULxL has to be soldered on the carrier board. Please contact [TQ-Support](#) for soldering instructions (13).

5. SOFTWARE

The TQMa6ULxL is delivered with a preinstalled boot loader U-Boot.

The [BSP provided](#) by TQ-Systems is configured for the combination of TQMa6ULxL and MBa6ULx.

The boot loader U-Boot provides TQMa6ULxL-specific as well as board-specific settings, e.g.:

- i.MX6UL configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

Further information can be found in the [Support Wiki for the TQMa6ULx](#).

If another bootloader is used, this data must be adapted. Contact [TQ-Support](#) for detailed information.



6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa6ULxL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short; avoid interference of other signals by distance and/or shielding, also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

Since the TQMa6ULxL operates on an application-specific carrier board, EMC or ESD tests only make sense for the whole device. The TQMa6ULxL it designed to pass the following test:

- EMC-Interference radiation:
Measurement of electrically radiated emission for standard, residential, commercial and light industrial environments in the range of 30 MHz to 6 GHz according to DIN EN 55022 A1:2007.

6.2 ESD

In order to avoid interspersions on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa6ULxL.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering, perhaps Zener diode(s)
- Fast signals: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤ 3.3 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

Detailed information concerning the i.MX6UL thermal characteristics is to be taken from NXP documents (6) and (10).

In general, a reliable operation is given when following conditions are met:

Table 39: Climate and operational conditions extended temperature range –25 °C ... +85 °C

Parameter	Range	Remark
Chip temperature i.MX6UL	–40 °C ... +105 °C	Typical max +90 °C
Environmental temperature i.MX6UL	–40 °C ... +85 °C	–
Chip temperature PMIC	–40 °C ... +125 °C	–
Environment temperature PMIC	–40 °C ... +85 °C	–
Case temperature DDR3L SDRAM	–40 °C ... +95 °C	–
Case temperature other ICs	–25 °C ... +85 °C	–
Permitted storage temperature TQMa6ULxL	–40 °C ... +85 °C	–
Relative humidity (operating / storage)	10 % ... 90 %	Not condensing

Table 40: Climate and operational conditions industrial temperature range –40 °C ... +85 °C

Parameter	Range	Remark
Chip temperature i.MX6UL	–40 °C ... +105 °C	Typical max +90 °C
Environmental temperature i.MX6UL	–40 °C ... +85 °C	–
Chip temperature PMIC	–40 °C ... +125 °C	–
Environmental temperature PMIC	–40 °C ... +85 °C	–
Case temperature DDR3L SDRAM	–40 °C ... +95 °C	–
Case temperature other ICs	–40 °C ... +85 °C	–
Permitted storage temperature TQMa6ULxL	–40 °C ... +85 °C	–
Relative humidity (operating / storage)	10 % ... 90 %	Not condensing

6.5 Reliability and service life

The calculated MTBF for the TQMa6ULxL is 1,472,325 hours with a constant error rate at +40 °C Ground Benign.

The TQMa6ULxL is designed to be insensitive to shock and vibration.

The TQMa6ULxL must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.

Detailed information concerning the i.MX6UL service life under different operational conditions is to be taken from the NXP Application Note (8).



7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa6ULxL is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa6ULxL was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa6ULxL always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa6ULxL on account of available Standby or Sleep-Modes of the components on the TQMa6ULxL.

7.5 Battery

No batteries are assembled on the TQMa6ULxL.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa6ULxL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa6ULxL is delivered in reusable packaging.

7.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94 (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96 (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98 (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01 (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 41: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CCM	Clock Control Module
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrie Norm (German industry standard)
DSM	Deep Sleep Mode
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIM	External Interface Module
eLCDIF	Enhanced LCD Interface
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	European Standard (Europäische Norm)
EPIT	Enhanced Periodic Interrupt Timer
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GPT	General Purpose Timer
HS	High-Speed
I/O	Input/Output
I ² C	Inter-Integrated Circuit
I ² S	Integrated Interchip Sound
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
IPU	Image Processing Unit
JTAG®	Joint Test Action Group
KPP	Key Pad Port
LCD	Liquid Crystal Display
LCDIF	LCD Interface
LDO	Low Drop-Out
LED	Light Emitting Diode
LGA	Land Grid Array
LICELL	Lithium Cell
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Control
MDIO	Management Data Input/Output
MII	Media-Independent Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MMDC	Multi-Mode DDR Controller
MQS	Medium Quality Sound
MTBF	Mean operating Time Between Failures

8.1 Acronyms and definitions (continued)

Table 41: Acronyms (continued)

Acronym	Meaning
n/a	Not Applicable
NA	Not Available
NAND	Not-And
NC	Not Connected
NOR	Not-Or
OTG	On-The-Go
PC	Personal Computer
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGB	Red Green Blue
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
RWP	Reversible Write Protection
SAI	Serial Audio Interface
SD/eSD/SDXC	Secure Digital / enhanced Secure Digital / SD eXtended Capacity
SD/MMC	Secure Digital Multimedia Card
SDIO	Secure Digital Input/Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SJC	System JTAG Controller
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SRC	System Reset Controller
SVHC	Substances of Very High Concern
SW	Software
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
USDHC	Ultra-Secured Digital Host Controller
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection



8.2 References

Table 42: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 6UltraLite Data Sheet	Rev. 2.2, 30 May 2017	NXP
(2)	i.MX 6UltraLite Reference Manual	Rev. 2, 12 Apr 2016	NXP
(3)	i.MX6ULL Data Sheet	Rev. 1.2, 20 Nov 2017	NXP
(4)	i.MX6ULL Reference Manual	Rev. 1, 12 Nov 2017	NXP
(5)	Chip Errata for the i.MX 6UltraLite	Rev. 2.3, 10 Oct 2017	NXP
(6)	AN5170, i.MX 6UltraLite Power Consumption Measurement	Rev. 2, 08 May 2016	NXP
(7)	AN5198, i.MX 6UltraLite Product Usage Lifetime Estimates	Rev. 2, 29 Aug 2016	NXP
(8)	AN4871, Application Note Assembly Handling for Lidless FCBGAs Packages	Rev. 0, 07 Feb 2014	NXP
(9)	Hardware Development Guide for the i.MX 6UltraLite Applications Processor	Rev. 3, 04 Sep 2018	NXP
(10)	PF3000, PMIC	Rev. 9, Aug 2017	NXP
(11)	MBa6ULx User's Manual	– current –	TQ-Systems
(12)	TQMa6ULx Support-Wiki	– current –	TQ-Systems
(13)	TQMa6ULxL Processing instructions	– current –	TQ-Systems

