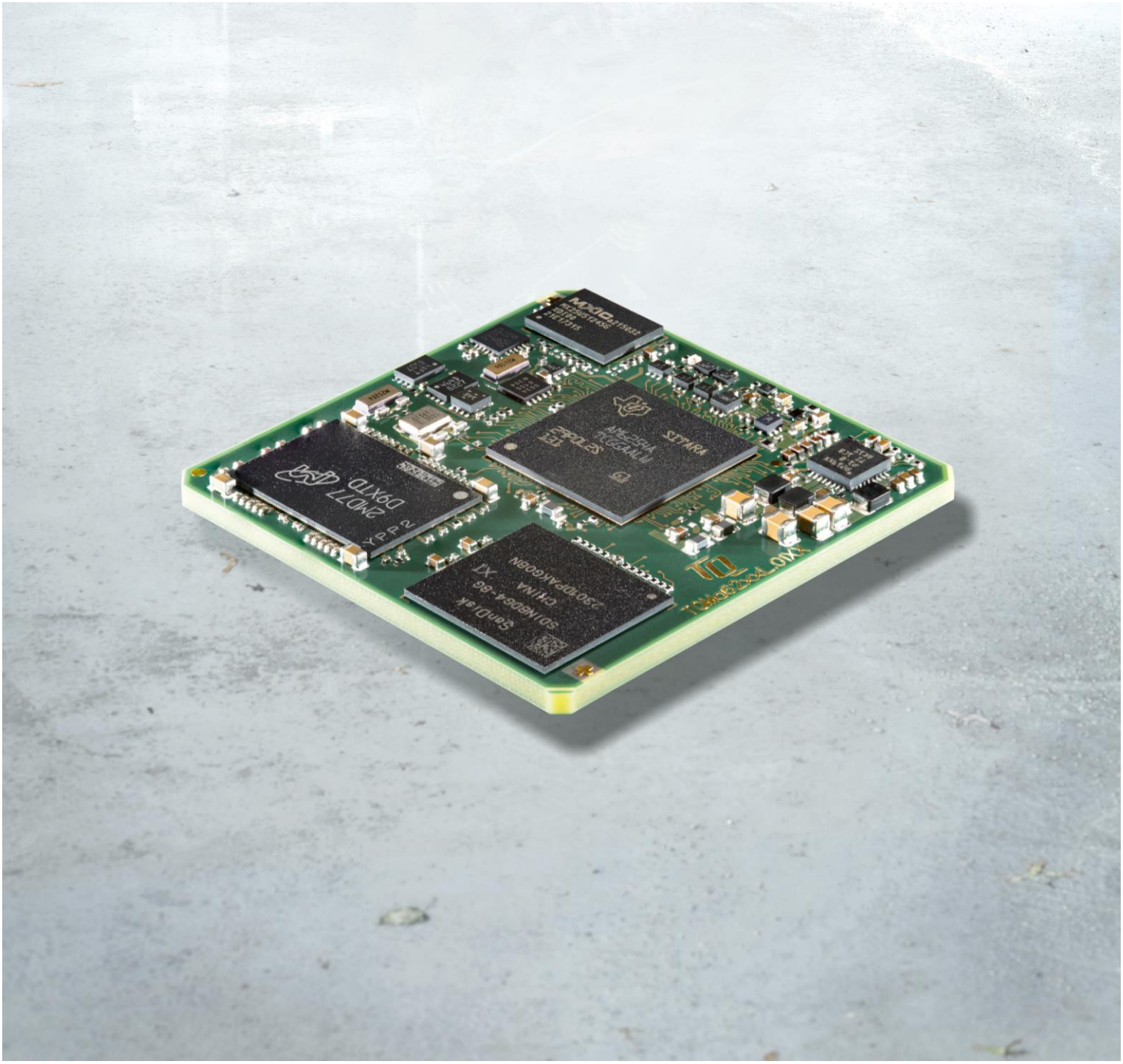
TQMa62xxL
Preliminary User's Manual

TQMa62xxL UM 0001
30.11.2023



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	30.11.2023	M. Kreuzer	All	Initial release

1. ABOUT THIS MANUAL

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1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive devices and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa62xxL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you power up the TQMa62xxL or the Starterkit, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manuals of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa62xx circuit diagram
- MBa62xx User's Manual
- Sitara™ AM62x Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqmax62xx

2. BRIEF DESCRIPTION

The TQMa62xxL is a universal TQ-LGA mini module based on the TI Sitara family AM62x with ARM Cortex A53 and Cortex M4F cores.

This Preliminary User's Manual describes the hardware of the TQMa62xxL Rev.010x and refers to some software settings.
It does not replace the AM62x Reference Manual (2).

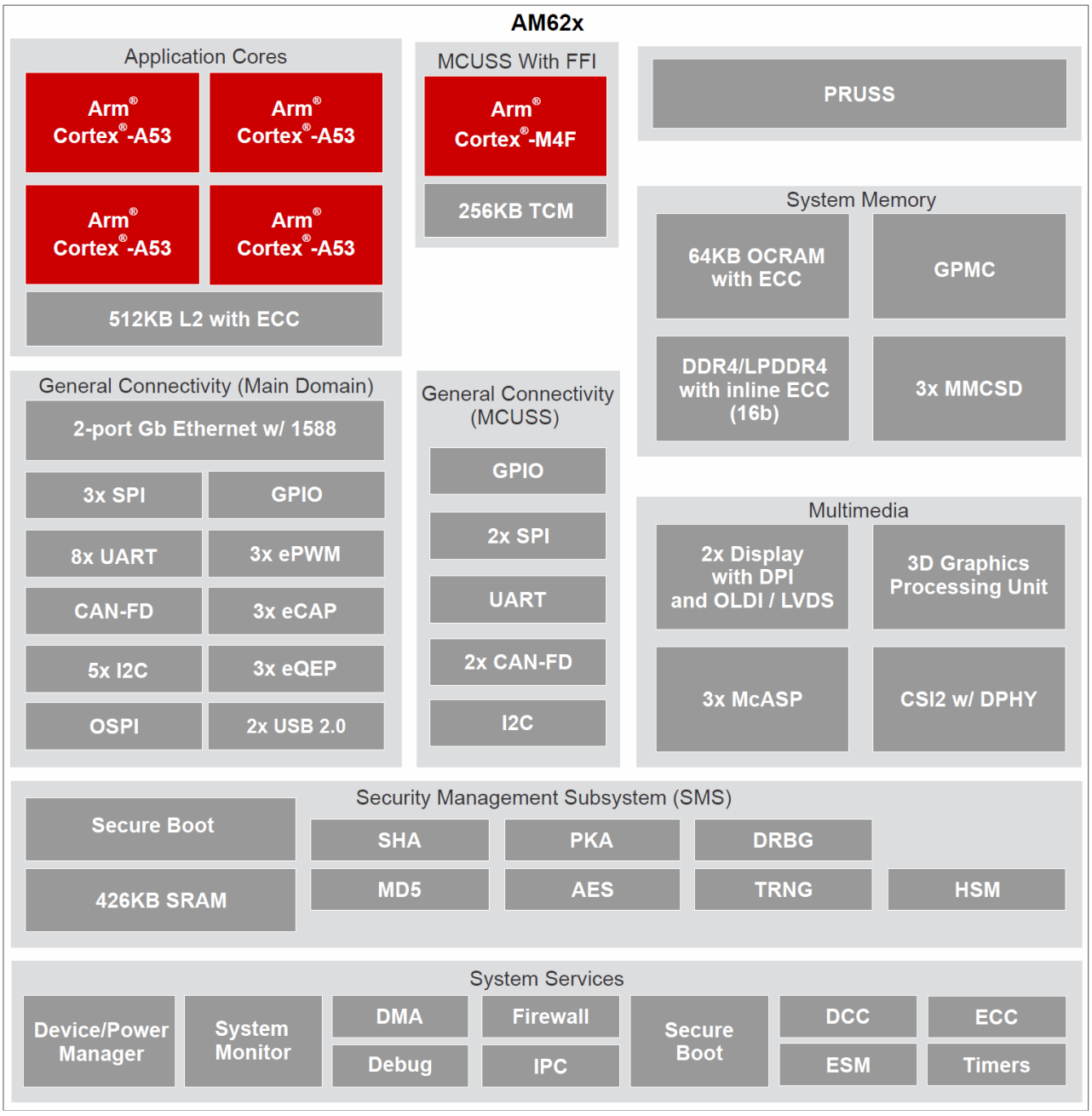


Figure 1: Block diagram AM62x

(Source: Texas Instruments)

All useful AM62x signals are routed to the TQMa62xxL LGA pads. There are no restrictions for customers using the TQMa62xxL with respect to an integrated customised design.

Please take note of that not all interfaces can be used simultaneously.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa62xxL, and the BSP provided by TQ-Systems GmbH, see also section 4.

3.1 System overview

3.1.1 System architecture / block diagram

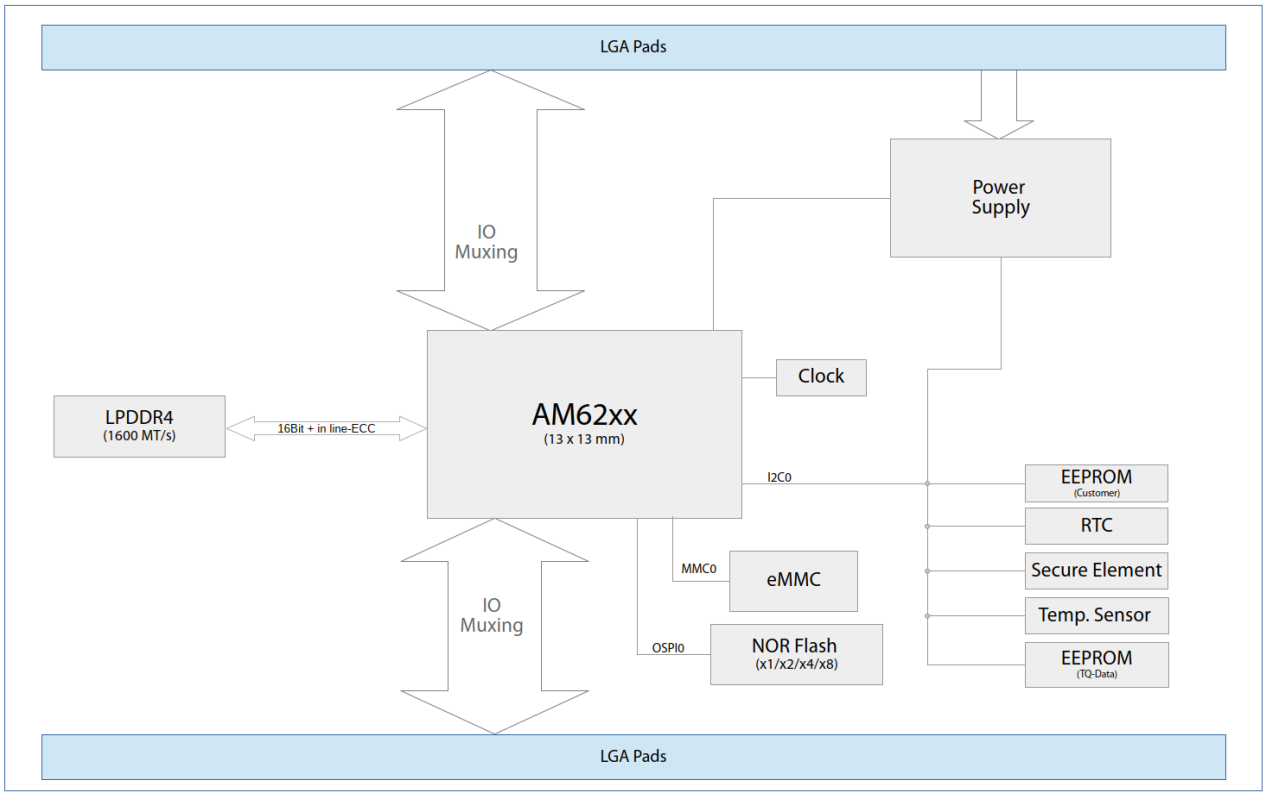


Figure 2: Block diagram TQMa62xxL

3.1.2 Functionality

The following key functions are implemented on the TQMa62xxL:

- Mini module with form factor 38 mm x 38 mm
- AM62x CPU (up to 4 x A53 and/ 1 x M4F)
- 16-bit LPDDR4 memory
- 1x eMMC NAND-Flash 5.1
- 1x QSPI-NOR-Flash (optional)
- Clock supply
- EEPROM (optional)
- Real-time clock (optional)
- Secure Element chip (optional)
- Temperature sensor (optional)
- EEPROM (TQ-Data)
- Supervisor
- Single Power Supply 3.3 V
- Availability of all essential signals of the CPU at the LGA pads

3.1.3 Pin multiplexing

The pin multiplexing of the AM62x permits to use many pins for different interfaces.
The information provided in this User's Manual is based on the BSP provided by TQ-Systems GmbH.

Attention: Destruction or malfunction	
	Many AM62x pins can be configured as different function. Please take note of the information in the AM62 data sheet (1) concerning the configuration of these pins before integration / start-up of your carrier board / Starter kit. Please also take note of the latest AM62x errata (3).

3.2 System components

3.2.1 Processor derivatives

Depending on the TQMa62xxL version, one of the following AM62x derivatives is assembled:
AM6254 / AM6252 / AM6251 / AM6234 / AM6232 / AM6231

Table 2: AM62x derivatives (Source: Texas Instruments)

FEATURES	REFERENCE NAME	AM625			AM623		
		AM6254	AM6252	AM6251	AM6234	AM6232	AM6231
CTRLMMR_WKUP_JTAG_DEVICE_ID[31:13] DEVICE_ID register bit field value(1)		C: 0x1D123 G: 0x1D127	C: 0x1D0A3 G: 0x1D0A7	G: 0x1D067	C: 0x1D103 G: 0x1D107	C: 0x1D083 G: 0x1D087	G: 0x1D047
PROCESSORS AND ACCELERATORS							
Speed Grades (See Table 7-1)		T, S, K, G					
Arm Cortex-A53 Microprocessor Subsystem	Arm A53	Quad Core	Dual Core	Single Core	Quad Core	Dual Core	Single Core
Arm Cortex-M4F in MCU domain	Arm M4F	Single Core Functional Safety Optional(5)					
3D Graphics Engine (OpenGL ES 3.1, Vulkan 1.2)	3D Graphics engine	Yes	Yes	Yes	No	No	No
Device Management Subsystem	WKUP_R5F	Single core					
Crypto Accelerators	Security	Yes					
PROGRAM AND DATA STORAGE							
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	64KB (with SECDED ECC)					
On-Chip Shared Memory (RAM) in M4F Domain	MCU_MSRAM	256KB					
DDR4/LPDDR4 DDR Subsystem	DDRSS	16-bit data with inline ECC; up to 8GB using DDR4 or 4GB using LPDDR4					
General-Purpose Memory Controller	GPMC	Up to 1GB with ECC					
PERIPHERALS							
Display Subsystem	DSS	1x DPI					
		1x LVDS					
Modular Controller Area Network Interface with Full CAN-FD Support	MCAN	3					
General-Purpose I/O	GPIO	Up to 170					
Inter-Integrated Circuit Interface	I2C	6					
Multichannel Audio Serial Port	MCASP	3					
Multichannel Serial Peripheral Interface	MCSPI	5					
Multi-Media Card/ Secure Digital Interface	MM/CSD	1x eMMC (8-bits)					
		2x SD/SDIO (4-bits)					
Flash Subsystem (FSS)(2)	OSPI0/QSPI0	Yes(2)					
Programmable Real-Time Unit Subsystem(3)	PRUSS	2x PRU Cores (Optional)					
Industrial Communication Subsystem Support(4)	PRUSS	No					
Gigabit Ethernet Interface	CPSW3G	Yes					
General-Purpose Timers	TIMER	12 (4 in MCU Channel)					
Enhanced Pulse-Width Modulator Module	EPWM	3					
Enhanced Capture Module	ECAP	3					
Enhanced Quadrature Encoder Pulse Module	EQEP	3					
Universal Asynchronous Receiver and Transmitter	UART	9					
CSI2-RX Controller with DPHY	CSI-RX	1					
USB2.0 Controller with PHY	USB 2.0	2					

3.2.2 Booting

3.2.2.1 Boot source

The boot source is selected via the boot strapping pins of the AM62x. The signals are directly routed to the module connectors and will be available again as GPIO after reading the boot configuration.

After the release of MCU_PORz the boot configuration is read in at the BOOTMODE[15:0] pins. Independent of the boot device, the ROM bootloader is executed first, which assists in reading and executing the application code. The data can be read and loaded either directly from the memory device or by a peripheral.

The following figure shows the implementation of boot strapping on the module:

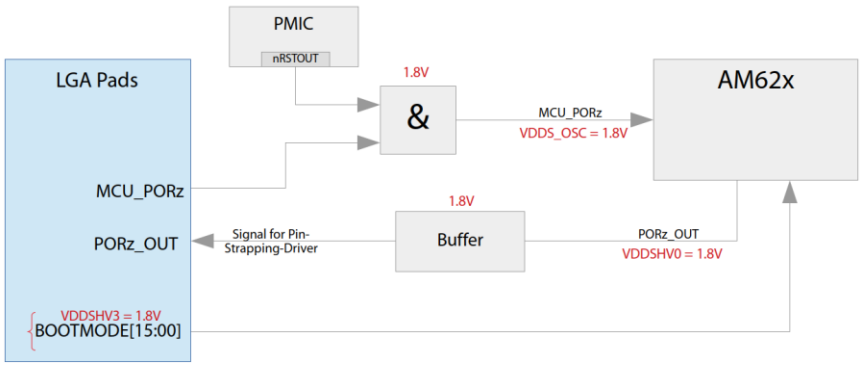


Figure 3: Block diagram boot strapping

According to the Reference Manual (2) the general boot configuration at the TQMa62xxL can be set as follows:

Table 3: Selecting the General Boot Configuration

Boot configuration pin	Setting	TQMa62xxL
BOOTMODE[15:14]	Reserved, fixed to 0	00
BOOTMODE[13:10]	Select the backup boot mode, if primary boot device failed	Don't care
BOOTMODE[9:3]	See following chapters for boot devices	-
BOOTMODE[2:0]	Ref Clock Select: 000 = 19.2 MHz 001 = 20 MHz 010 = 24 MHz 011 = 25 MHz 100 = 26 MHz 101 = 27 MHz 110 = Reserved 111 = Reserved	011

Attention: Malfunction	
	All BOOTMODE[15:00] signals must have either a pullup (to V_1V8) or pulldown (to Ground). Undefined levels can lead to a malfunction during booting.

3.2.2.2 Boot device eMMc

Table 4: Boot device selection eMMC

Boot configuration pin	Setting	TQMa62xxL
BOOTMODE[9]	Port: MMCSD Port 0 (8 bit width) This bit must be set to 0	000
BOOTMODE[8]	Reserved	
BOOTMODE[7]	0 = Filesystem Mode 1 = Raw Mode	
BOOTMODE[6:3]	Primary Boot Mode: 0000 = Reserved 0001 = OSPI 0010 = QSPI 0011 = SPI 0100 = Ethernet RGMII 0101 = Ethernet RMII 0110 = I2C 0111 = UART 1000 = MMCSD boot 1001 = eMMC 1010 = USB 1011 = GPMC NAND 1100 = GPMC NOR 1101 = PCIe 1110 = xSPI 1111 = No-boot/Dev boot	1000

3.2.2.3 Boot device NOR-flash

Table 5: Selection of the boot device NOR flash

Boot configuration pin	Setting	TQMa62xxL
BOOTMODE9	Reserved, fixed to 0	Don't Care
BOOTMODE8	SPI mode: 0 = SPI Mode 0 1 = SPI Mode 3	1
BOOTMODE7	Chip-Select: 0 = Boot-Flash is on CS0 1 = Boot-Flash is on CS1	0
BOOTMODE[6:3]	Primary Boot Mode: 0000 = Reserved 0001 = OSPI 0010 = QSPI 0011 = SPI 0100 = Ethernet RGMII 0101 = Ethernet RMII 0110 = I2C 0111 = UART 1000 = MMCSD card 1001 = eMMC 1010 = USB 1011 = GPMC NAND 1100 = GPMC NOR 1101 = PCIe 1110 = xSPI 1111 = No-boot/Dev boot	0011

Further boot configurations can be found in the Reference Manual (2).

Besides the mentioned boot configurations above, it is recommended to consider an alternative boot source during development, e.g. USB boot or no-boot mode for JTAG debug.

Note: Update	
	When designing a mainboard, it is recommended to plan a redundant update concept for software updates in the field. Furthermore, it is recommended to switch the conversion of the boot strap pins to high impedance after reading in.

3.2.3 Memory

3.2.3.1 LPDDR4 SDRAM

The TQMa62xxL has an LPDDR4 memory with the use of in-line ECC:

- 16-bit bus width with optional ECC (8-bit data + 8-bit ECC)
- Up to 1600 Mbps = 800 MHz
- 1 GByte (=8 Gbit) / 2 GByte (=16 Gbit)

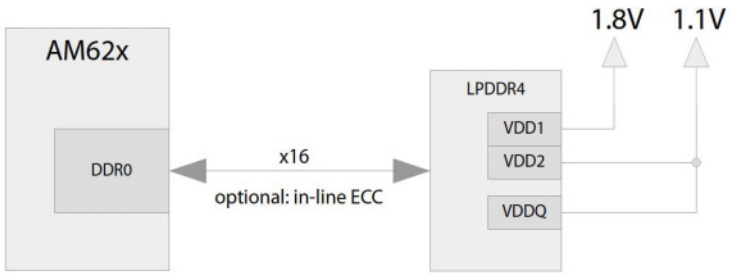


Figure 4: Block diagram DDR3L SDRAM connection

3.2.3.2 eMMC

An eMMC is available to the TQMa62xxL as non-volatile data memory for programs and data (e.g. boot loader, operating system). The used MMC0 signals are not available to the Pinout.

- MMC0 Interface is connected to the eMMC Flash
- 8 / 16 / 32 / 64 GByte

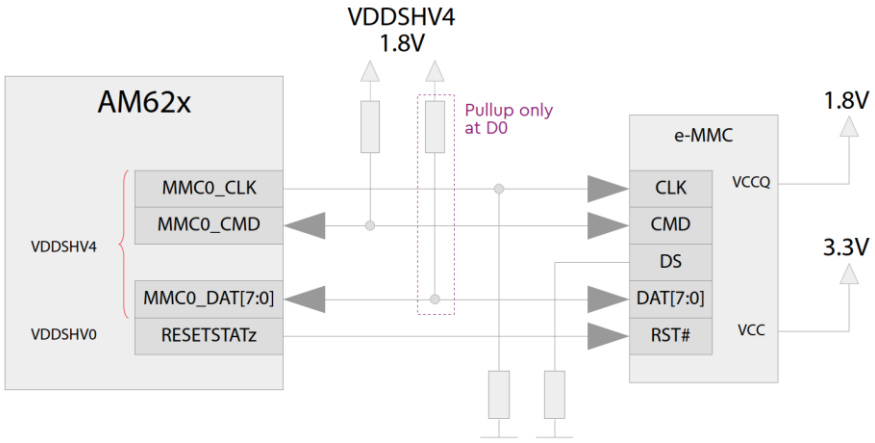


Figure 5: Block diagram eMMC flash interface

The TQMa62xxL supports the following transmission modes:

Table 6: eMMC Flash modes

Mode	1-bit	4-bit	8-bit	Note
Default Speed	n/a	n/a	n/a	
High Speed	n/a	n/a	Yes	Boot process
HS200	n/a	n/a	Yes	U-boot / Linux
HS400	n/a	n/a	n/a	MMCSD not supported features

3.2.3.3 NOR-Flash

A NOR-Flash on the TQMa62xxL is available as non-volatile memory. The used OSPI0 signals are not available to the pinout.

- OSPI0 Interface is connected to the NOR Flash
- The NOR-Flash variants Quad SPI Flash and Octal SPI Flash are usable
- 512 / 1024 / 2048 Mbit

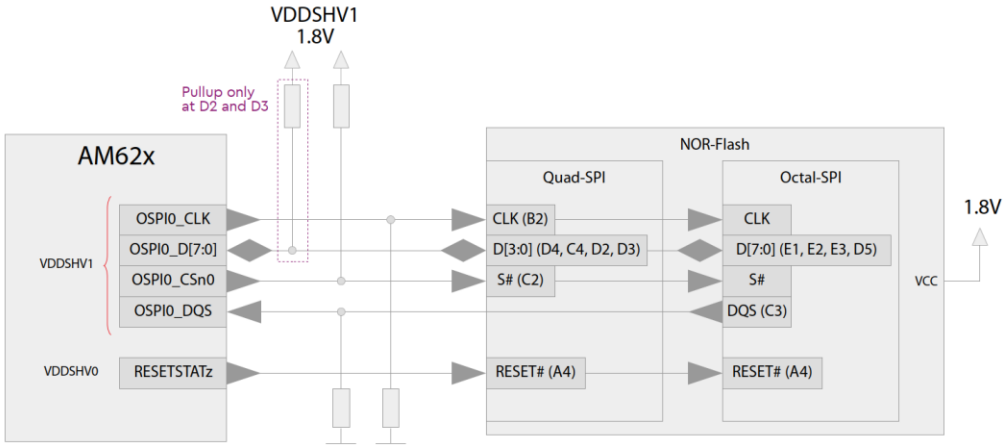


Figure 6: Block diagram NOR-Flash

The NOR-Flash variants Quad SPI Flash and Octal SPI Flash are usable. The TQMa62xxL supports the following transmission modes:

Table 7: NOR-Flash modes

Mode	Read	Write	Note
Extended SPI (SDR)	1-4-4	1-4-4	Clock = max. 83.33 MHz

3.2.3.4 EEPROMs

I²C EEPROMs are provided on the TQMa62xxL for non-volatile storage. A distinction is made here between:

- Customer data, freely accessible
- TQ manufacturing data (Serial Number, MAC, ...)

All I²C slave address and bus structure are summarized in chapter 3.2.8.3.

3.2.4 Clock supply

The clock supply of the TQMa62xxL is represented as follows:

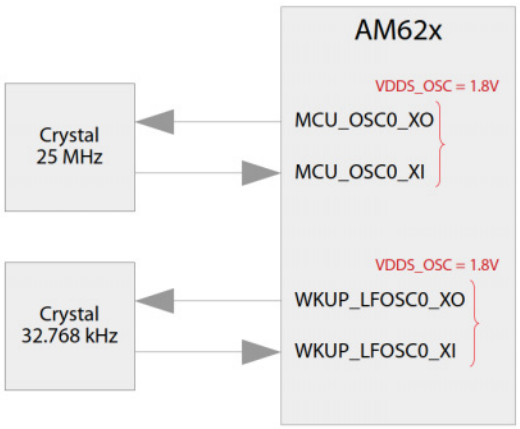


Figure 7: Block diagram clock supply

To get the module executable only with a 3.3 V supply, MCU_OSC0_XO / XI and WKUP_LFOSC_XO / XI were implemented as clock on the module. The remaining clock inputs can either be derived from the system clock or fed externally via the module connectors, as an example the following clocks can be fed externally:

- EXT_REFCLK1
- MCU_EXT_REFCLK0 (optional external System Clock inputs)
- CPTS0_RFT_CLK (optional CPTS Reference Clock input)
- AUDIO_EXT_REFCLK0/1 (optional, External Clock input to McASP)

Further information can be obtained from the associated data sheets (1).

3.2.5 RTC

An optional RTC (NXP PCF85063A) can be equipped on the TQMa62xx. The connection is realized as follows:

- The RTC can be supplied from the base board via V_RTC_IN. V_RTC_IN = 2.0 V to 5.5V
- RTC_INT# and RTC_CLKOUT is accessible at the module connectors.
- RTC_CLKOUT is only activated as soon as the TQMa62xxL is supplied with V_3V3_IN.
- I2C0 is connected via I2C0 (I^2C addresses are described in chapter 3.2.8.3)

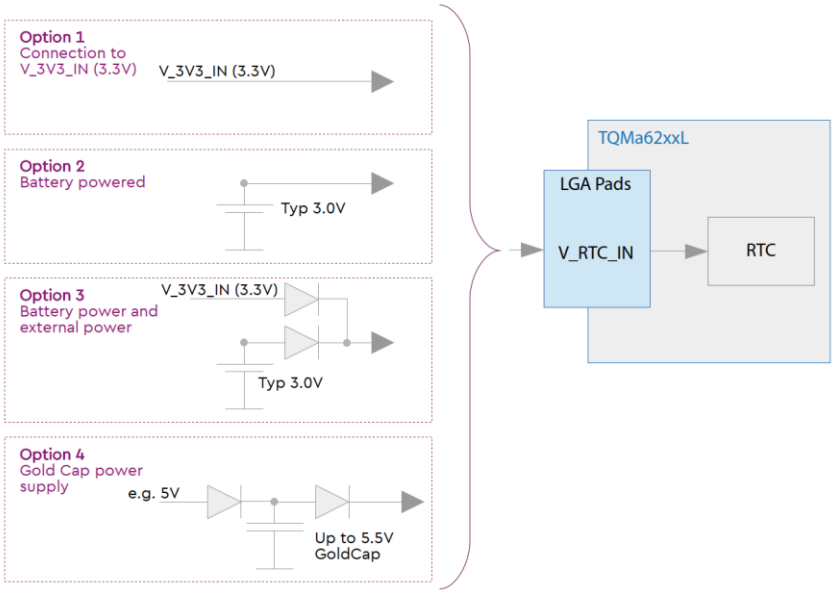


Figure 8: Block diagram RTC

Note: Equipping the base board	
	The RTC is supplied internally by a LDO (1.8V) via V_RTC_IN. This allows the user an easy use of Gold-Caps or Coin cells on the main board.

3.2.6 Secure Element

A Secure Element Chip can optionally be fitted on the TQMa62xx. The connection can be seen in the following figure:

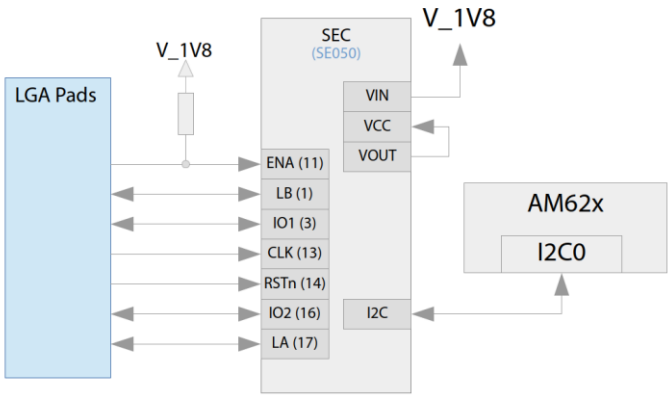


Figure 9: Block diagram SEC

The SE050E2HQ1/Z01Z3 from NXP is used as the secure element. All I²C addresses are described in chapter 3.2.8.3.

3.2.7 Temperature sensor

A temperature sensor (TI TMP1075DSGR) is placed on the TQMa62xxL to monitor the module temperature.
The over temperature output (TEMP_ALERT) of the sensor is available at the module connectors as an open drain output.
The I²C addresses are described in chapter 3.2.8.3.

3.2.8 Interfaces

In general, except for the memory connection, all IO pins of the CPU are provided at the module connectors.
For further information about the interfaces and the pin multiplexing refer to the CPU Reference Manual (2).

3.2.8.1 GPIO

Besides their interface function, most AM62x pins can also be used as GPIOs. Details are to be taken from the AM62x Data Sheet (1).

3.2.8.2 JTAG

The CPU has a JTAG interface that is directly accessible at the module connectors. The following default configuration is provided on the TQMa62xxL:

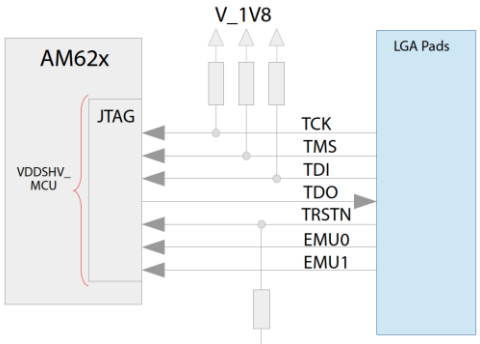


Figure 10: Block diagram JTAG

The following table shows the signals used by the JTAG interface.

Table 8: JTAG signals

Signal / Multiplexing	I/O	Power domain	Note
TCK	I	VDDSHV_MCU (1,8 V)	10 kΩ Pull-up on module
TDI	I		10 kΩ Pull-up on module
TDO	OZ		Three-state output
TMS	I		10 kΩ Pull-up on module
TRST#	I		4.7 kΩ Pull-up on module
EMU[1:0]	IO		Optional signals, not required for JTAG

For more information please refer to the Reference Manual (2).

3.2.8.3 I²C

The accessible I²C buses depend on the pin multiplexing. To use the internal I²C devices, the I2C0 bus is permanently provided on the TQMa62xx. The following devices are connected to the module:

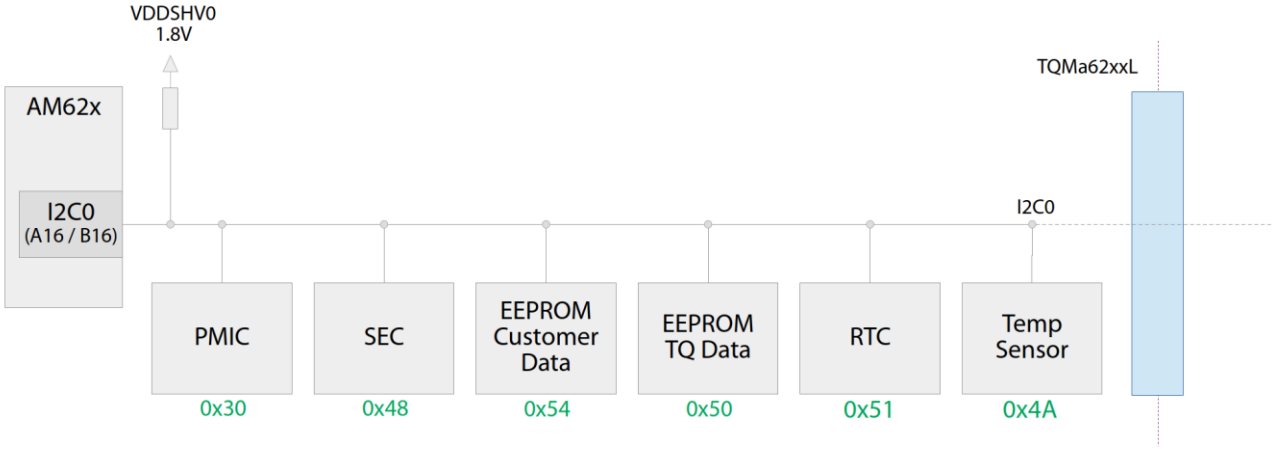


Figure 11: Block diagram I2C bus on the TQMa62xx

Table 9: I2C address assignment on the module

Bus	Component	Address	Note
I2C0	Temperature sensor TMP1075	0x4A / 0b100 1010	
	EEPROM M24C02	0x50 / 0b101 0000	TQ-Data
	EEPROM M24C64	0x54 / 0b101 0100	Customer EEPROM
	RTC PCF85063ATL	0x51 / 0b101 0001	
	SEC	0x48 / 0b100 1000	
	PMIC TPS6521902	0x30 / 0b011 0000	

If additional devices should be connected to this bus, optional external pullups should be provided to improve the rise / fall times. I2C0 relates to 1.8V.

3.2.8.4 UART

UART0 is routed to the TQMa62xxL pins as primary function.

3.2.8.5 EXTINT#

The signal EXTINT# of the AM62x is routed to TQMa62xxL pin X2-B32 as primary function.

3.2.9 Reset

The following figure describes the implementation of the reset structure of the TQMa62xxL:

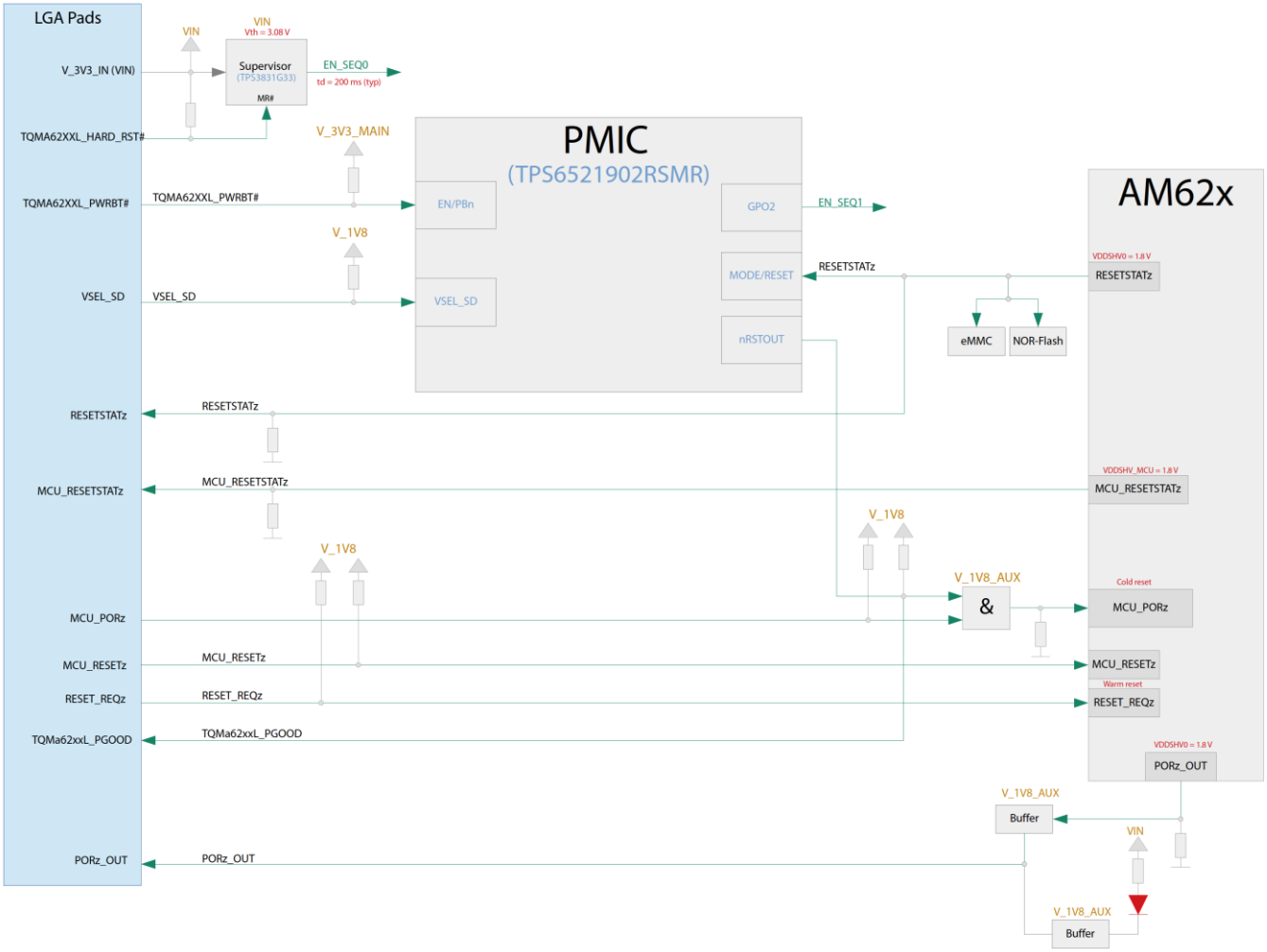


Figure 12: Block diagram Reset

3.2.9.1 Reset Options (Input)

3.2.9.1.1 TQMa62xxL_HARD_RST#

The input signal TQM62xxL_HARD_RST# is used to control the entire module. Coming from the module connectors a reset with power cycle of the module is executed. As soon as the signal becomes HIGH, the power-up sequencing takes place after a delay of approx. 200 ms.

Per default the signal is connected with a pullup to V_3V3_IN (3.3 V), therefore only a LOW can reset the module with power cycle.

3.2.9.1.2 TQMa62xxL_PWRBT#

The input signal TQMa62xxL_PWRBT# is used to control the entire module. Coming from the module connector an ON/OFF request at the PMIC is performed by the signal. An 8 s LOW level event leads to an OFF request of the PMIC. A 600 ms HIGH level event leads to an ON request of the PMIC.

It must be ensured that the "First Supply Detection" is activated on the PMIC. The TQMa62xxL_PWRBT# signal is only ignored during the first power-up of the module.

Per default the signal is connected with a pullup to V_3V3_IN (3.3 V), therefore only a LOW can reset the module with power cycle.

3.2.9.1.3 MCU_PORz

The MCU_PORz signal is used to control a cold reset. Between the module connector signal MCU_PORz and the AM62x MCU_PORz signal is an AND element and a PMIC, which keeps the signal at LOW during power sequencing and pulls it HIGH afterwards.

By default the signal is connected with a pullup to 1.8 V, so only a LOW can trigger a cold reset of the module.

3.2.9.1.4 MCU_RESETz

The MCU_RESETz signal is used to control a warm reset of the MCU domain of the AM62x.

By default the signal is connected to a pullup to 1.8 V, so only a LOW can trigger a warm reset of the MCU domain on the module.

3.2.9.1.5 RESET_REQz

The RESET_REQz signal is used to control a warm reset of the main domain of the AM62x.

By default the signal is connected to a pullup to 1.8 V, so only a LOW can trigger a warm reset of the main domain on the module.

3.2.9.2 Reset Status (Output)

3.2.9.2.1 PORz_OUT

The PORz_OUT signal serves as status signal for a cold reset of the main domain of the AM62x.

By default the signal is driven via a buffer with 1.8 V.

3.2.9.2.2 MCU_RESETSTATz

The MCU_RESETSTATz signal serves as a status signal for a warm reset of the MCU domain.

By default the signal is connected with a pulldown to ground.

3.2.9.2.3 RESETSTATz

The RESETSTATz signal serves as a status signal for a warm reset of the main domain.

By default the signal is connected with a pulldown to ground.

3.2.9.3 Control signals

3.2.9.3.1 TQMa62xxL_PGOOD

TQMa62xxL_PGOOD serves as a status signal to the base board that the voltages on the main board can now be switched on. Power GOOD (PGOOD) is only active when the power sequencing on the module has been successfully completed.

3.2.9.3.2 VSEL_SD

VSEL_SD is used to select the V_VDDSHV5 supply voltage:

- LOW: V_VDDSHV5 = 1.8 V
- HIGH: V_VDDSHV5 = 3.3 V

By default the signal is connected with a pullup to 3.3 V, thus initially V_VDDSHV5 is always supplied with 3.3 V.

3.2.10 Watchdog

The AM62 provides a Watchdog Timer. If the Watchdog Timer is active and not reset within the specified time, triggers a Warm-Reset. For more information, refer to the AM62 Reference Manual (2).

3.2.11 Power supply

3.2.11.1 Main power supply

The main supply of the TQMa62xxL is defined to typ. 3.3 V. By applying the 3.3 V voltage the module generates all required voltages.

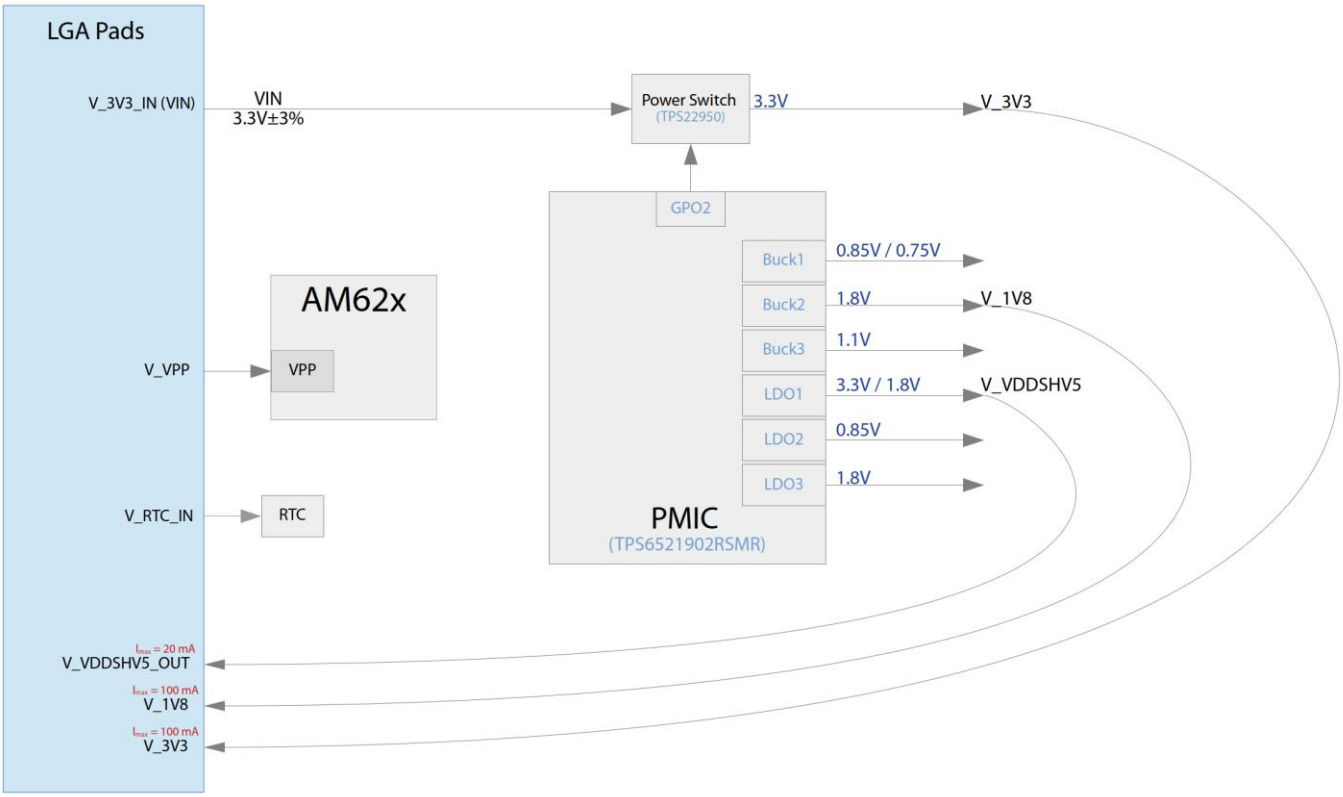


Figure 13: Block diagram power supply

3.2.11.2 Overview TQMa62xxL supply

The following table shows all relevant supply voltages of the TQMa62xxL.

Table 10: Supply voltages

Module pin / Signal	Voltage	Current	Use
V_3V3_IN	3.201 V to 3.399 V	see Table 11	Input: module supply
V_3V3	3.201 V to 3.399 V	max. 100 mA	Output
V_1V8	1.746 V to 1.854 V	max. 100 mA	Output: for boot configuration
V_VDDSHV5	1.8 V / 3.3 V	< 10 mA	Output: MMC1 IO-Bank supply
V_RTC_IN	2.0 V to 5.5 V	See 3.2.5	Input: supply for module RTC
V_VPP	1.8 V	max. 400 mA	Input: supply for eFuse programming
USB0_VBUS USB1_VBUS	typ. 5 V	< 1 mA	Input: Used to detect the USB-VBUS voltage and is usually supplied with the VBUS voltage switched by the USB host. External circuitry is required – see (2).

Attention: Malfunction	
	If the absolute maximum voltages of the CPU are exceeded, malfunctions and component failures may occur. The mentioned outputs may not be supplied externally under any circumstances.

3.2.11.3 Power sequenzing

After switching on the module supply V_3V3_IN and TQMa62xxL_HARD_RST# to HIGH the power-up sequence starts. With completion of the power sequencing the supply of the external mainboard components is signaled via TQM62xxL_PGOOD. The following figure shows the chronological sequence of the signals involved.

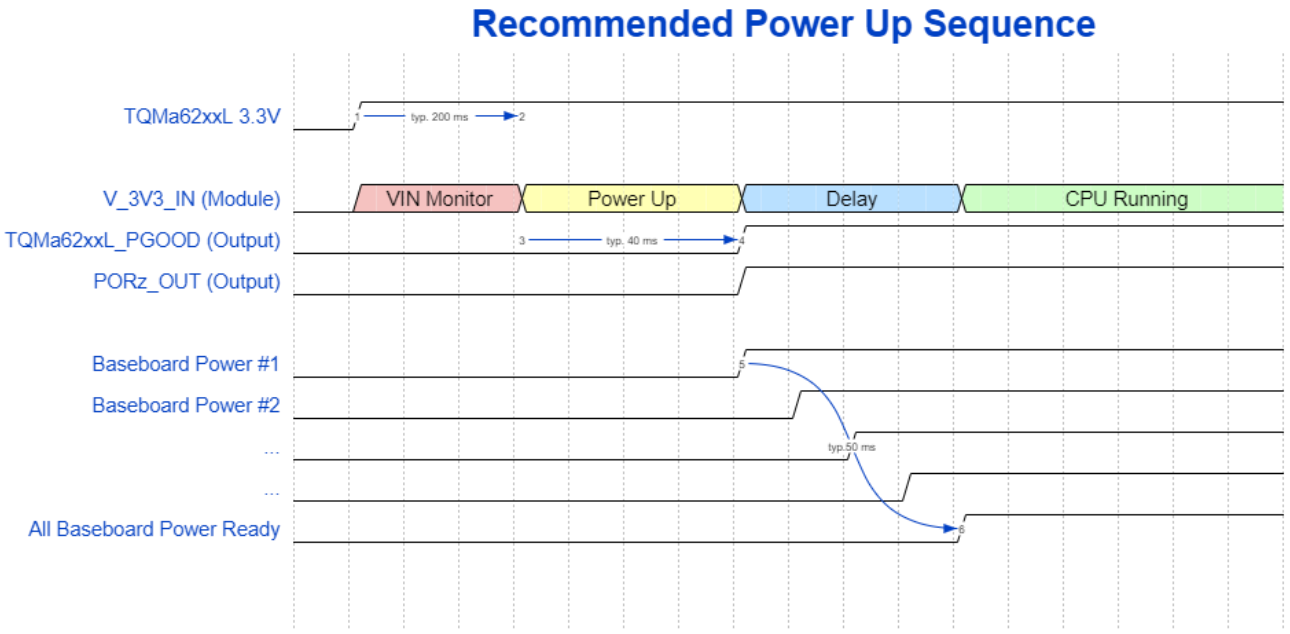


Figure 14: Recommended power up sequence

Attention: Malfunction	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence is completed. The end of the power-up sequence is signaled by a high level of the TQM62xxL_PGOOD signal.

3.2.11.4 Power modes

The TQMa62xxL has the following power modes:

- Active Mode - The module is powered and everything is active.

Depending of the CPU, the following low power modes can be provided:

- Deep Sleep Mode
  - Module is completely powered
  - All power domains - except GP_Core_CTL - and all clocks OFF
  - DDR interface in self-refresh
- MCU Only
  - Module is completely supplied
  - All power domains - except GP_Core_CTL - and all clocks ON
  - DDR interface in self-refresh
- Standby
  - Module is completely supplied
  - All power domains and clocks ON
  - DDR interface in self-refresh

More information can be found in the AM62x Reference Manual (2).

Independent of the CPU, the following low power modes can be provided:

- Module RTC Mode
  - Module is no longer supplied via V_3V3_IN
  - Only the V_RTC_IN remains supplied and active
  - The current consumption is then only determined by the current consumption of the RTC.
- Self-Refresh Mode (Suspend to RAM)
  - The LPDDR4 memory can be put into self-refresh mode by an SRE command.
  - IDD6 is specified in self-refresh, typ. current consumption at 25 °C ambient temperature is approx. 0.4 mA to 2.7 mA

3.2.11.5 Power consumption

The following table lists some technical parameters of the module supply. The specified current consumptions are to be regarded as a guide value. Since the current consumption of the TQMa62xxL can differ greatly depending on the application, modes and operating system, the values listed here should only be used for a performance estimate.

Table 11: Current consumption TQMa62xxL

TQMa62xxL		
Current consumption Power OFF	TBD mA	TQMa62xxL_HARD_RST# = LOW
Current consumption Reset mode	TBD mA	MCU_PORz = LOW
Current consumption Power Down	TBD mA	TQMa62xxL_PWRBT# = LOW
Current consumption theoretical worst case	2.4 A	Current consumption @ 3.3 V
Current consumption U-Boot prompt	TBD mA	U-Boot Idle
Current consumption Linux prompt	TBD mA	Linux Idle
Current consumption Linux (stressapptest -W -s 31536000 -M 256 -m 4 -C 4 -i 4 stress-ng --cpu-load 100 --cpu 4 --timeout 31536000)	TBD mA	Higher current consumption must be expected when using additional interfaces in parallel

3.3 TQMa62xxL interface

3.3.1 Pin assignment

The TQMa62xxL has a total of 366 LGA pads. By using the LGA design, the module is soldered on once and thus has a permanent, stable connection to its peripherals. Removing the module from its soldered-on position is not possible without further ado, is not recommended and can lead to a reduction in service life or to its destruction.

The electrical and pin characteristics are to be taken from the AM62x datasheet / manual (1)(2)

Attention: Destruction or malfunction	
	The multiple pin configurations of all AM62x internal function units must be taken note of. The pin assignment shown in Figure 15 refers to the corresponding BSP provided by TQ-Systems GmbH. Table 12 shows all pin multiplexing options.

Figure 15: Pad placement

3.3.2 Pinout TQMa62xxL

Table 12: Pinout

Module Pad	Signal	CPU BALL	IO	Description / Usage
Main Domain				
P22	VOUT0_PCLK	AC24	O	IO Muxing Options
	GPMC0_A19		OZ	
	PR0_PRU1_GPO19		O	
	PR0_PRU1_GPI19		I	
	UART2_CTSn		I	
	PR0_PRU0_GPO19		IO	
	PR0_PRU0_GPI19		I	
	GPIO0_64		IO	
	PR0_ECAP0_IN_APWM_OUT		IO	
N21	VOUT0_HSYNC	AB24	O	
	GPMC0_A16		OZ	
	PR0_PRU1_GPO15		O	
	PR0_PRU1_GPI15		I	
	UART3_RTSn		O	
	PR0_PRU0_GPO6		IO	
	PR0_PRU0_GPI6		I	
	GPIO0_61		IO	
N22	VOUT0_VSYNC	AC25	O	
	GPMC0_A18		OZ	
	PR0_PRU1_GPO18		O	
	PR0_PRU1_GPI18		I	
	UART2_RTSn		O	
	PR0_PRU0_GPO18		IO	
	PR0_PRU0_GPI18		I	
	GPIO0_63		IO	
M21	VOUT0_DE	Y20	O	
	GPMC0_A17		OZ	
	PR0_PRU1_GPO17		O	
	PR0_PRU1_GPI17		I	
	UART3_CTSn		I	
	PR0_PRU0_GPO7		IO	
	PR0_PRU0_GPI7		I	
	GPIO0_62		IO	
M20	VOUT0_DATA0	U22	O	
	GPMC0_A0		OZ	
	PR0_PRU1_GPO0		O	
	PR0_PRU1_GPI0		I	
	UART2_RXD		I	
	PR0_PRU0_GPO8		IO	
	PR0_PRU0_GPI8		I	
	GPIO0_45		IO	
L20	VOUT0_DATA1	V24	O	
	GPMC0_A1		OZ	
	PR0_PRU1_GPO1		O	
	PR0_PRU1_GPI1		I	
	UART2_TXD		O	
	PR0_PRU0_GPO9		IO	
	PR0_PRU0_GPI9		I	
	GPIO0_46		IO	
L19	VOUT0_DATA2	W25	O	
	GPMC0_A2		OZ	
	PR0_PRU1_GPO2		O	
	PR0_PRU1_GPI2		I	
	UART3_RXD		I	
	PR0_PRU0_GPO10		IO	
	PR0_PRU0_GPI10		I	
	GPIO0_47		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
K19	VOUT0_DATA3	W24	O	IO Muxing Options
	GPMC0_A3		OZ	
	PR0_PRU1_GPO3		O	
	PR0_PRU1_GPI3		I	
	UART3_TXD		O	
	PR0_PRU0_GPO11		IO	
	PR0_PRU0_GPI11		I	
	GPIO0_48		IO	
K18	VOUT0_DATA4	Y25	O	
	GPMC0_A4		OZ	
	PR0_PRU1_GPO4		O	
	PR0_PRU1_GPI4		I	
	UART4_RXD		I	
	PR0_PRU0_GPO12		IO	
	PR0_PRU0_GPI12		I	
	GPIO0_49		IO	
J18	VOUT0_DATA5	Y24	O	
	GPMC0_A5		OZ	
	PR0_PRU1_GPO5		O	
	PR0_PRU1_GPI5		I	
	UART4_TXD		O	
	PR0_PRU0_GPO13		IO	
	PR0_PRU0_GPI13		I	
	GPIO0_50		IO	
U22	VOUT0_DATA6	Y23	O	
	GPMC0_A6		OZ	
	PR0_PRU1_GPO6		O	
	PR0_PRU1_GPI6		I	
	UART5_RXD		I	
	PR0_PRU0_GPO14		IO	
	PR0_PRU0_GPI14		I	
	GPIO0_51		IO	
T22	VOUT0_DATA7	AA25	O	
	GPMC0_A7		OZ	
	PR0_PRU1_GPO7		O	
	PR0_PRU1_GPI7		I	
	UART5_TXD		O	
	PR0_PRU0_GPO15		IO	
	PR0_PRU0_GPI15		I	
	GPIO0_52		IO	
T21	VOUT0_DATA8	V21	O	
	GPMC0_A8		OZ	
	PR0_PRU1_GPO16		O	
	PR0_PRU1_GPI16		I	
	UART6_RXD		I	
	PR0_PRU0_GPO17		IO	
	PR0_PRU0_GPI17		I	
	GPIO0_53		IO	
R21	VOUT0_DATA9	W21	O	
	GPMC0_A9		OZ	
	PR0_PRU1_GPO8		O	
	PR0_PRU1_GPI8		I	
	UART6_TXD		O	
	PR0_PRU0_GPO16		IO	
	PR0_PRU0_GPI16		I	
	GPIO0_54		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
R20	VOUT0_DATA10	V20	O	IO Muxing Options
	GPMC0_A10		OZ	
	PR0_PRU1_GPO9		O	
	PR0_PRU1_GPI9		I	
	UART6_RTSn		O	
	PR0_PRU0_GPO0		IO	
	PR0_PRU0_GPI0		I	
	GPIO0_55		IO	
P20	VOUT0_DATA11	AA23	O	
	GPMC0_A11		OZ	
	PR0_PRU1_GPO10		O	
	PR0_PRU1_GPI10		I	
	UART6_CTSn		I	
	PR0_PRU0_GPO1		IO	
	PR0_PRU0_GPI1		I	
	GPIO0_56		IO	
P19	VOUT0_DATA12	AB25	O	
	GPMC0_A12		OZ	
	PR0_PRU1_GPO11		O	
	PR0_PRU1_GPI11		I	
	UART5_RTSn		O	
	PR0_PRU0_GPO2		IO	
	PR0_PRU0_GPI2		I	
	GPIO0_57		IO	
N19	VOUT0_DATA13	AA24	O	
	GPMC0_A13		OZ	
	PR0_PRU1_GPO12		O	
	PR0_PRU1_GPI12		I	
	UART5_CTSn		I	
	PR0_PRU0_GPO3		IO	
	PR0_PRU0_GPI3		I	
	GPIO0_58		IO	
N18	VOUT0_DATA14	Y22	O	
	GPMC0_A14		OZ	
	PR0_PRU1_GPO13		O	
	PR0_PRU1_GPI13		I	
	UART4_RTSn		O	
	PR0_PRU0_GPO4		IO	
	PR0_PRU0_GPI4		I	
	GPIO0_59		IO	
M18	VOUT0_DATA15	AA21	O	
	GPMC0_A15		OZ	
	PR0_PRU1_GPO14		O	
	PR0_PRU1_GPI14		I	
	UART4_CTSn		I	
	PR0_PRU0_GPO5		IO	
	PR0_PRU0_GPI5		I	
	GPIO0_60		IO	
C21	GPMC0_AD0	M25	IO	
	PR0_PRU1_GPO8		O	
	PR0_PRU1_GPI8		I	
	MCASP2_AXR4		IO	
	PR0_PRU0_GPO0		IO	
	PR0_PRU0_GPI0		I	
	TRC_CLK		O	
	GPIO0_15		IO	
	BOOTMODE00		I	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
D21	GPMC0_AD1	N23	IO	IO Muxing Options
	PR0_PRU1_GPO9		O	
	PR0_PRU1_GPI9		I	
	MCASP2_AXR5		IO	
	PR0_PRU0_GPO1		IO	
	PR0_PRU0_GPI1		I	
	TRC_CTL		O	
	GPIO0_16		IO	
	BOOTMODE01		I	
B20	GPMC0_AD2	N24	IO	
	PR0_PRU1_GPO10		O	
	PR0_PRU1_GPI10		I	
	MCASP2_AXR6		IO	
	PR0_PRU0_GPO2		IO	
	PR0_PRU0_GPI2		I	
	TRC_DATA0		O	
	GPIO0_17		IO	
	BOOTMODE02		I	
C20	GPMC0_AD3	N25	IO	
	PR0_PRU1_GPO11		O	
	PR0_PRU1_GPI11		I	
	MCASP2_AXR7		IO	
	PR0_PRU0_GPO3		IO	
	PR0_PRU0_GPI3		I	
	TRC_DATA1		O	
	GPIO0_18		IO	
	BOOTMODE03		I	
G22	GPMC0_AD4	P24	IO	
	PR0_PRU1_GPO12		O	
	PR0_PRU1_GPI12		I	
	MCASP2_AXR8		IO	
	PR0_PRU0_GPO4		IO	
	PR0_PRU0_GPI4		I	
	TRC_DATA2		O	
	GPIO0_19		IO	
	BOOTMODE04		I	
H22	GPMC0_AD5	P22	IO	
	PR0_PRU1_GPO13		O	
	PR0_PRU1_GPI13		I	
	MCASP2_AXR9		IO	
	PR0_PRU0_GPO5		IO	
	PR0_PRU0_GPI5		I	
	TRC_DATA3		O	
	GPIO0_20		IO	
	BOOTMODE05		I	
F21	GPMC0_AD6	P21	IO	
	PR0_PRU1_GPO14		O	
	PR0_PRU1_GPI14		I	
	MCASP2_AXR10		IO	
	PR0_PRU0_GPO6		IO	
	PR0_PRU0_GPI6		I	
	TRC_DATA4		O	
	GPIO0_21		IO	
	BOOTMODE06		I	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
G21	GPMC0_AD7	R23	IO	IO Muxing Options
	PR0_PRU1_GPO15		O	
	PR0_PRU1_GPI15		I	
	MCASP2_AXR11		IO	
	PR0_PRU0_GPO7		IO	
	PR0_PRU0_GPI7		I	
	TRC_DATA5		O	
	GPIO0_22		IO	
	BOOTMODE07		I	
E20	GPMC0_AD8	R24	IO	
	VOUT0_DATA16		O	
	UART2_RXD		I	
	MCASP2_AXR0		IO	
	PR0_PRU1_GPO0		O	
	PR0_PRU1_GPI0		I	
	GPIO0_23		IO	
	BOOTMODE08		I	
F20	GPMC0_AD9	R25	IO	
	VOUT0_DATA17		O	
	UART2_TXD		O	
	MCASP2_AXR1		IO	
	PR0_PRU1_GPO1		O	
	PR0_PRU1_GPI1		I	
	GPIO0_24		IO	
	BOOTMODE09		I	
K22	GPMC0_AD10	T25	IO	
	VOUT0_DATA18		O	
	UART3_RXD		I	
	MCASP2_AXR2		IO	
	PR0_PRU1_GPO2		O	
	PR0_PRU1_GPI2		I	
	GPIO0_25		IO	
	OBSCLK0		O	
	BOOTMODE10		I	
L22	GPMC0_AD11	R21	IO	
	VOUT0_DATA19		O	
	UART3_TXD		O	
	MCASP2_AXR3		IO	
	PR0_PRU1_GPO3		O	
	PR0_PRU1_GPI3		I	
	TRC_DATA23		O	
	GPIO0_26		IO	
	BOOTMODE11		I	
J21	GPMC0_AD12	T22	IO	
	VOUT0_DATA20		O	
	UART4_RXD		I	
	MCASP2_AFSX		IO	
	PR0_PRU0_GPO0		IO	
	PR0_PRU0_GPI0		I	
	TRC_DATA22		O	
	GPIO0_27		IO	
	BOOTMODE12		I	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
K21	GPMC0_AD13	T24	IO	IO Muxing Options
	VOUT0_DATA21		O	
	UART4_TXD		O	
	MCASP2_ACLKX		IO	
	PR0_PRU0_GPO1		IO	
	PR0_PRU0_GPI1		I	
	TRC_DATA21		O	
	GPIO0_28		IO	
	BOOTMODE13		I	
H20	GPMC0_AD14	U25	IO	
	VOUT0_DATA22		O	
	UART5_RXD		I	
	MCASP2_AFSR		IO	
	PR0_PRU0_GPO2		IO	
	PR0_PRU0_GPI2		I	
	TRC_DATA20		O	
	GPIO0_29		IO	
	UART2_CTSn		I	
	BOOTMODE14		I	
J20	GPMC0_AD15	U24	IO	
	VOUT0_DATA23		O	
	UART5_TXD		O	
	MCASP2_ACLKR		IO	
	PR0_PRU0_GPO3		IO	
	PR0_PRU0_GPI3		I	
	TRC_DATA19		O	
	GPIO0_30		IO	
	UART2_RTSn		O	
	BOOTMODE15		I	
D19	GPMC0_WP#	K25	O	
	AUDIO_EXT_REFCLK1		IO	
	GPMC0_A22		OZ	
	UART6_TXD		O	
	PR0_PRU0_GPO15		IO	
	PR0_PRU0_GPI15		I	
	TRC_DATA13		O	
	GPIO0_39		IO	
G19	GPMC0_WAIT0	U23	I	
	MCASP1_AFSX		IO	
	PR0_PRU0_GPO14		IO	
	PR0_PRU0_GPI14		I	
	TRC_DATA12		O	
	GPIO0_37		IO	
H19	GPMC0_WAIT1	V25	I	
	VOUT0_EXTPCLKIN		I	
	GPMC0_A21		OZ	
	UART6_RXD		I	
	GPIO0_38		IO	
	EQEP2_I		IO	
A21	GPMC0_OE#_RE#	L24	O	
	MCASP1_AXR1		IO	
	PR0_PRU0_GPO10		IO	
	PR0_PRU0_GPI10		I	
	TRC_DATA8		O	
	GPIO0_33		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
E19	GPMC0_WE#	L25	O	IO Muxing Options
	MCASP1_AXR0		IO	
	PR0_PRU0_GPO11		IO	
	PR0_PRU0_GPI11		I	
	TRC_DATA9		O	
	GPIO0_34		IO	
C18	GPMC0_CS0#	M21	O	
	MCASP2_AXR14		IO	
	PR0_PRU0_GPO17		IO	
	PR0_PRU0_GPI17		I	
	TRC_DATA15		O	
	GPIO0_41		IO	
D18	GPMC0_CS1#	L21	O	
	PR0_PRU1_GPO16		O	
	PR0_PRU1_GPI16		I	
	MCASP2_AXR15		IO	
	PR0_PRU0_GPO18		IO	
	PR0_PRU0_GPI18		I	
	TRC_DATA16		O	
	GPIO0_42		IO	
F18	GPMC0_CS2#	K22	O	
	I2C2_SCL		IO	
	MCASP1_AXR4		IO	
	UART4_RXD		I	
	PR0_PRU0_GPO19		IO	
	PR0_PRU0_GPI19		I	
	TRC_DATA17		O	
	GPIO0_43		IO	
	MCASP1_AFSR		IO	
G18	GPMC0_CS3#	K24	O	
	I2C2_SDA		IO	
	GPMC0_A20		OZ	
	UART4_TXD		O	
	MCASP1_AXR5		IO	
	TRC_DATA18		O	
	GPIO0_44		IO	
	MCASP1_ACLKR		IO	
E22	GPMC0_CLK	P25	O	
	MCASP1_AXR3		IO	
	GPMC0_FCLK_MUX		O	
	PR0_PRU0_GPO8		IO	
	PR0_PRU0_GPI8		I	
	TRC_DATA6		O	
	GPIO0_31		IO	
D22	GPMC0_BE0#_CLE	M24	O	
	MCASP1_ACLKX		IO	
	PR0_PRU0_GPO12		IO	
	PR0_PRU0_GPI12		I	
	TRC_DATA10		O	
	GPIO0_35		IO	
B19	GPMC0_ADV#_ALE	L23	O	
	MCASP1_AXR2		IO	
	PR0_PRU0_GPO9		IO	
	PR0_PRU0_GPI9		I	
	TRC_DATA7		O	
	GPIO0_32		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
A18	GPMC0_BE1#	N20	O	IO Muxing Options
	MCASP2_AXR12		IO	
	PR0_PRU0_GPO13		IO	
	PR0_PRU0_GPI13		I	
	TRC_DATA11		O	
	GPIO0_36		IO	
A19	GPMC0_DIR	M22	O	
	PR0_ECAP0_IN_APWM_OUT		IO	
	MCASP2_AXR13		IO	
	PR0_PRU0_GPO16		IO	
	PR0_PRU0_GPI16		I	
	TRC_DATA14		O	
	GPIO0_40		IO	
	EQEP2_S		IO	
D13	MMC1_SDCD	D17	I	
	UART6_RXD		I	
	TIMER_IO6		IO	
	UART3_RTSn		O	
	GPIO1_48		IO	
E13	MMC1_SDWP	C17	I	
	UART6_TXD		O	
	TIMER_IO7		IO	
	UART3_CTSn		I	
	GPIO1_49		IO	
D12	MMC1_CMD	A21	IO	
	TIMER_IO5		IO	
	UART3_TXD		O	
	GPIO1_47		IO	
A12	MMC1_CLK	B22	IO	
	TIMER_IO4		IO	
	UART3_RXD		I	
	GPIO1_46		IO	
B10	MMC1_DAT0	A22	IO	
	CP_GEMAC_CPTS0_HW2TSPUSH		I	
	TIMER_IO3		IO	
	UART2_CTSn		I	
	ECAP2_IN_APWM_OUT		IO	
	GPIO1_45		IO	
B11	MMC1_DAT1	B21	IO	
	CP_GEMAC_CPTS0_HW1TSPUSH		I	
	TIMER_IO2		IO	
	UART2_RTSn		O	
	ECAP1_IN_APWM_OUT		IO	
	GPIO1_44		IO	
C11	MMC1_DAT2	C21	IO	
	CP_GEMAC_CPTS0_TS_SYNC		O	
	TIMER_IO1		IO	
	UART2_TXD		O	
	GPIO1_43		IO	
C12	MMC1_DAT3	D22	IO	
	CP_GEMAC_CPTS0_TS_COMP		O	
	TIMER_IO0		IO	
	UART2_RXD		I	
	GPIO1_42		IO	
D15	MMC2_SDCD	A23	I	
	MCASP1_ACLKX		IO	
	UART4_RXD		I	
	GPIO0_71		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
D16	MMC2_SDWP	B23	I	IO Muxing Options
	MCASP1_AFSX		IO	
	UART4_TXD		O	
	GPIO0_72		IO	
A16	MMC2_CLK	D25	IO	
	MCASP1_ACLKR		IO	
	MCASP1_AXR5		IO	
	UART6_RXD		I	
	GPIO0_69		IO	
B16	MMC2_DAT0	B24	IO	
	MCASP1_AXR0		IO	
	GPIO0_68		IO	
B17	MMC2_DAT1	C25	IO	
	MCASP1_AXR1		IO	
	GPIO0_67		IO	
C15	MMC2_DAT2	E23	IO	
	MCASP1_AXR2		IO	
	UART5_TXD		O	
	GPIO0_66		IO	
C17	MMC2_DAT3	D24	IO	
	MCASP1_AXR3		IO	
	UART5_RXD		I	
	GPIO0_65		IO	
A15	MMC2_CMD	C24	IO	
	MCASP1_AFSR		IO	
	MCASP1_AXR4		IO	
	UART6_TXD		O	
	GPIO0_70		IO	
K4	I2C0_SCL	B16	IO	
	PR0_IEP0_EDIO_DATA_IN_OUT30		IO	
	SYNC0_OUT		O	
	OBSCLK0		O	
	UART1_DCDn		I	
	EQEP2_A		I	
	EHRPWM_SOCA		O	
	GPIO1_26		IO	
	ECAP1_IN_APWM_OUT		IO	
	SPI2_CS0		IO	
L4	I2C0_SDA	A16	IO	
	PR0_IEP0_EDIO_DATA_IN_OUT31		IO	
	SPI2_CS2		IO	
	TIMER_IO5		IO	
	UART1_DSRn		I	
	EQEP2_B		I	
	EHRPWM_SOCB		O	
	GPIO1_27		IO	
	ECAP2_IN_APWM_OUT		IO	
E16	I2C1_SDA	A17	IO	
	UART1_TXD		O	
	TIMER_IO1		IO	
	SPI2_CLK		IO	
	EHRPWM0_SYNCO		O	
	GPIO1_29		IO	
	EHRPWM2_B		IO	
	MMC2_SDWP		I	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
E17	I2C1_SCL	B17	IO	IO Muxing Options
	UART1_RXD		I	
	TIMER_IO0		IO	
	SPI2_CS1		IO	
	EHRPWM0_SYNCI		I	
	GPIO1_28		IO	
	EHRPWM2_A		IO	
	MMC2_SDCD		I	
D4	UART0_CTS#	A15	I	
	SPI0_CS2		IO	
	I2C3_SCL		IO	
	UART2_RXD		I	
	TIMER_IO6		IO	
	AUDIO_EXT_REFCLK0		IO	
	PR0_ECAP0_SYNC_OUT		O	
	GPIO1_22		IO	
	MCASP2_AFSX		IO	
	MMC2_SDCD		I	
D3	UART0_RTS#	B15	O	
	SPI0_CS3		IO	
	I2C3_SDA		IO	
	UART2_TXD		O	
	TIMER_IO7		IO	
	AUDIO_EXT_REFCLK1		IO	
	PR0_ECAP0_IN_APWM_OUT		IO	
	GPIO1_23		IO	
	MCASP2_ACLKX		IO	
	MMC2_SDWP		I	
E5	UART0_RXD	D14	I	
	ECAP1_IN_APWM_OUT		IO	
	SPI2_D0		IO	
	EHRPWM2_A		IO	
	GPIO1_20		IO	
E4	UART0_TXD	E14	O	
	ECAP2_IN_APWM_OUT		IO	
	SPI2_D1		IO	
	EHRPWM2_B		IO	
	GPIO1_21		IO	
A9	MCASP0_ACLKX	B20	IO	
	SPI2_CS1		IO	
	ECAP2_IN_APWM_OUT		IO	
	GPIO1_11		IO	
	EQEP1_A		I	
A7	MCASP0_ACLKR	A20	IO	
	SPI2_CLK		IO	
	UART1_TXD		O	
	EHRPWM0_B		IO	
	GPIO1_14		IO	
	EQEP1_I		IO	
D7	MCASP0_AFSR	E19	IO	
	SPI2_CS0		IO	
	UART1_RXD		I	
	EHRPWM0_A		IO	
	GPIO1_13		IO	
	EQEP1_S		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
E7	MCASP0_AFSX	D20	IO	IO Muxing Options
	SPI2_CS3		IO	
	AUDIO_EXT_REFCLK1		IO	
	GPIO1_12		IO	
	EQEP1_B		I	
D6	MCASP0_AXR3	B19	IO	
	SPI2_D0		IO	
	UART1_CTSn		I	
	UART6_RXD		I	
	PR0_IEP0_EDIO_DATA_IN_OUT28		IO	
	ECAP1_IN_APWM_OUT		IO	
	PR0_UART0_RXD		I	
	GPIO1_7		IO	
	EQEP0_A		I	
B8	MCASP0_AXR2	A19	IO	
	SPI2_D1		IO	
	UART1_RTSn		O	
	UART6_TXD		O	
	PR0_IEP0_EDIO_DATA_IN_OUT29		IO	
	ECAP2_IN_APWM_OUT		IO	
	PR0_UART0_TXD		O	
	GPIO1_8		IO	
	EQEP0_B		I	
C8	MCASP0_AXR1	B18	IO	
	SPI2_CS2		IO	
	ECAP1_IN_APWM_OUT		IO	
	PR0_UART0_RXD		I	
	EHRPWM1_A		IO	
	GPIO1_9		IO	
	EQEP0_S		IO	
B7	MCASP0_AXR0	E18	IO	
	PR0_ECAP0_IN_APWM_OUT		IO	
	AUDIO_EXT_REFCLK0		IO	
	PR0_UART0_TXD		O	
	EHRPWM1_B		IO	
	GPIO1_10		IO	
	EQEP0_I		IO	
A4	MCAN0_RX	E15	I	
	UART5_TXD		O	
	TIMER_IO3		IO	
	SYNC3_OUT		O	
	UART1_RIn		I	
	EQEP2_S		IO	
	PR0_UART0_TXD		O	
	GPIO1_25		IO	
	MCASP2_AXR1		IO	
	EHRPWM_TZn_IN4		I	
A3	MCAN0_TX	C15	O	
	UART5_RXD		I	
	TIMER_IO2		IO	
	SYNC2_OUT		O	
	UART1_DTRn		O	
	EQEP2_I		IO	
	PR0_UART0_RXD		I	
	GPIO1_24		IO	
	MCASP2_AXR0		IO	
	EHRPWM_TZn_IN3		I	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
A6	SPI0_CLK	A14	IO	IO Muxing Options
	CP_GEMAC_CPTS0_TS_SYNC		O	
	EHRPWM1_A		IO	
	GPIO1_17		IO	
B5	SPI0_D0	B13	IO	
	CP_GEMAC_CPTS0_HW1TSPUSH		I	
	EHRPWM1_B		IO	
	GPIO1_18		IO	
B4	SPI0_D1	B14	IO	
	CP_GEMAC_CPTS0_HW2TSPUSH		I	
	EHRPWM_TZn_IN0		I	
	GPIO1_19		IO	
C6	SPI0_CS0	A13	IO	
	EHRPWM0_A		IO	
	PR0_ECAP0_SYNC_IN		I	
	GPIO1_15		IO	
C5	SPI0_CS1	C13	IO	
	CP_GEMAC_CPTS0_TS_COMP		O	
	EHRPWM0_B		IO	
	ECAP0_IN_APWM_OUT		IO	
	GPIO1_16		IO	
	EHRPWM_TZn_IN5		I	
B14	OSPI0_CS1#	G21	O	
	GPIO0_12		IO	
C14	OSPI0_CS2#	H21	O	
	SPI1_CS1		IO	
	OSPI0_RESET_OUT1		O	
	MCASP1_AFSR		IO	
	MCASP1_AXR2		IO	
	UART5_RXD		I	
	GPIO0_13		IO	
B13	OSPI0_CS3#	E24	O	
	OSPI0_RESET_OUT0		O	
	OSPI0_ECC_FAIL		I	
	MCASP1_ACLKR		IO	
	MCASP1_AXR3		IO	
	UART5_TXD		O	
	GPIO0_14		IO	
A13	OSPI0_LBCLKO	G25		
	UART5_RTSn			
	GPIO0_1			
AB13	RGMII1_TXC	AE19	IO	
	RMII1_CRS_DV		I	
	GPIO0_74		IO	
V12	RGMII1_TX_CTL	AD19	O	
	RMII1_TX_EN		O	
	GPIO0_73		IO	
Y13	RGMII1_TD0	AE20	O	
	RMII1_TXD0		O	
	GPIO0_75		IO	
W13	RGMII1_TD1	AD20	O	
	RMII1_TXD1		O	
	GPIO0_76		IO	
AA12	RGMII1_TD2	AE18	O	
	PR0_UART0_RXD		I	
	GPIO0_77		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
W12	RGMII1_TD3	AD18	O	
	PR0_UART0_TXD		O	
	GPIO0_78		IO	
AA11	RGMII1_RXC	AD17	I	
	RMII1_REF_CLK		I	
	PR0_UART0_CTSn		I	
	GPIO0_80		IO	
Y11	RGMII1_RX_CTL	AE17	I	
	RMII1_RX_ER		I	
	GPIO0_79		IO	
AB12	RGMII1_RD0	AB17	I	
	RMII1_RXD0		I	
	GPIO0_81		IO	
V11	RGMII1_RD1	AC17	I	
	RMII1_RXD1		I	
	GPIO0_82		IO	
W10	RGMII1_RD2	AB16	I	
	PR0_UART0_RTSn		O	
	GPIO0_83		IO	
Y10	RGMII1_RD3	AA15	I	
	GPIO0_84		IO	
Y17	RGMII2_TXC	AE21	IO	
	RMII2_CRS_DV		I	
	MCASP2_AXR5		IO	
	PR0_PRU1_GPO1		O	
	PR0_PRU1_GPI1		I	
	GPIO0_88		IO	IO Muxing Options
W16	RGMII2_TX_CTL	AA19	O	
	RMII2_TX_EN		O	
	MCASP2_AXR4		IO	
	PR0_PRU1_GPO0		O	
	PR0_PRU1_GPI0		I	
	GPIO0_87		IO	
AA15	RGMII2_TD0	Y18	O	
	RMII2_TXD0		O	
	MCASP2_AXR6		IO	
	PR0_PRU1_GPO2		O	
	PR0_PRU1_GPI2		I	
	GPIO0_89		IO	
AB15	RGMII2_TD1	AA18	O	
	RMII2_TXD1		O	
	MCASP2_ACLKR		IO	
	PR0_PRU1_GPO3		O	
	PR0_PRU1_GPI3		I	
	MCASP2_AXR8		IO	
	GPIO0_90		IO	
V17	RGMII2_TD2	AD21	O	
	MCASP2_AFSX		IO	
	PR0_PRU1_GPO4		O	
	PR0_PRU1_GPI4		I	
	PR0_ECAP0_IN_APWM_OUT		IO	
	GPIO0_91		IO	
	EQEP2_I		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
Y16	RGMII2_TD3	AC20	O	IO Muxing Options
	MCASP2_ACLKX		IO	
	PR0_PRU1_GPO16		O	
	PR0_PRU1_GPI16		I	
	PR0_ECAP0_SYNC_OUT		O	
	PR0_UART0_CTSn		I	
	GPIO1_0		IO	
	EQEP2_S		IO	
AB18	RGMII2_RXC	AD23	I	
	RMII2_REF_CLK		I	
	MCASP2_AXR1		IO	
	PR0_PRU0_GPO1		IO	
	PR0_PRU0_GPI1		I	
	PR0_ECAP0_SYNC_IN		I	
	GPIO1_2		IO	
AA17	RGMII2_RX_CTL	AD22	I	
	RMII2_RX_ER		I	
	MCASP2_AXR3		IO	
	PR0_PRU0_GPO0		IO	
	PR0_PRU0_GPI0		I	
	GPIO1_1		IO	
AA18	RGMII2_RD0	AE23	I	
	RMII2_RXD0		I	
	MCASP2_AXR2		IO	
	PR0_PRU0_GPO2		IO	
	PR0_PRU0_GPI2		I	
	PR0_UART0_RTSn		O	
	GPIO1_3		IO	
V18	RGMII2_RD1	AB20	I	
	RMII2_RXD1		I	
	MCASP2_AFSR		IO	
	PR0_PRU0_GPO3		IO	
	PR0_PRU0_GPI3		I	
	MCASP2_AXR7		IO	
	GPIO1_4		IO	
W18	RGMII2_RD2	AC21	I	
	MCASP2_AXR0		IO	
	PR0_PRU0_GPO4		IO	
	PR0_PRU0_GPI4		I	
	PR0_UART0_RXD		I	
	GPIO1_5		IO	
	EQEP2_A		I	
AB16	RGMII2_RD3	AE22	I	
	AUDIO_EXT_REFCLK0		IO	
	PR0_PRU0_GPO16		IO	
	PR0_PRU0_GPI16		I	
	PR0_UART0_TXD		O	
	GPIO1_6		IO	
	EQEP2_B		I	
U19	MDIO0_MDIO	AB22	IO	
	GPIO0_85		IO	
T19	MDIO0_MDC	AD24	O	
	GPIO0_86		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
A10	EXT_REFCLK1	A18	I	IO Muxing Options
	SYNC1_OUT		O	
	SPI2_CS3		IO	
	SYSCLKOUT0		O	
	TIMER_IO4		IO	
	CLKOUT0		O	
	CP_GEMAC_CPTS0_RFT_CLK		I	
	GPIO1_30		IO	
	ECAP0_IN_APWM_OUT		IO	
W19	EXTINT#	D16	I	
	GPIO1_70		IO	
System Signals				
V21	TQMa62xxL_HARD_RST#	-	I	Hard Reset to TQMa62xxL including Power Cycle 4.7kΩ Pullup on TQMa62xxL
B22	MCU_PORz	D2	I	Cold reset to CPU via MCU_PORz 10kΩ Pullup on TQMa62xxL
R6	MCU_RESETz	E11	I	MCU Domain warm reset 10kΩ Pullup on TQMa62xxL
T18	RESET_REQz	F20	I	Main Domain warm reset 10kΩ Pullup on TQMa62xxL
AA14	PORz_OUT	E21	O	Main Domain POR status 10kΩ Pulldown on TQMa62xxL
M5	MCU_RESETSTATz	B12	O	MCU Domain warm reset status 10kΩ Pulldown on TQMa62xxL
U20	RESETSTATz	F22	O	Main Domain warm reset status 10kΩ Pulldown on TQMa62xx
V20	TQMa62xxL_PGOOD	-	O	TQMa62xxL PGOOD Status
V14	TQMa62xxL_PWRBT#	-	I	TQMa62xxL PMIC Power Button 10kΩ Pullup on TQMa62xxL
G6	MCU_ERROR#	D1	IO	Error signal output from MCU Domain
V15	VSEL_SD	-	I	V_VDDSHV5 Power Control Low: V_VDDSHV5 = 1.8V High: V_VDDSHV5 = 3.3V 10K Pullup on TQMa62xxL
Debug				
H5	TRST#	B10	I	JTAG Interface TCK, TMS, TDI: 10kΩ Pullup on TQMa62xxL TRST#: 4.7kΩ Pulldown on TQMa62xxL
J5	TDI	A11	I	
J6	TMS	B11	I	
H4	TDO	D12	OZ	
K6	TCK	A10	I	
G4	EMU0	E12	IO	
G3	EMU1	C11	IO	
Factory Test Only				
R8	TQ_EEPROM_WC#	-	I	Factory Test only, do not connect
Y14	V_0V85	-	P	
W22	V_1V8_AUX	-	P	
H8	V_RTC	-	P	
M6	V_1V1	-	P	
T9	V_VDD_CORE	-	P	
V9	V_1V8A	-	P	
U5, V5, V6, W6	RFU_OR_DGND	-	-	Reserved for future use, do not connect

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
I2C Devices				
F5	RTC_INT#	-	O	RTC Interrupt, Open-Drain. Pullup required (typ. 10kΩ)
H7	RTC_CLKOUT	-	O	RTC Clock Output
L5	TEMP_ALERT	-	O	Programmable Alert Output, Open-Drain. Pullup required (typ. 4.7kΩ)
F6	CUST_EEPROM_WC#	-	I	Customer EEPROM Write Protection Control Low / Float: Write enabled High: Read only
F9	SE_ISO7816_IO1	-	IO	SEC Interface
D9	SE_ISO7816_IO2	-	IO	
E8	SE_ISO7816_CLK	-	I	
F8	SE_ISO7816_RST#	-	I	
D10	SE_ISO14443_LA	-	IO	
G9	SE_ISO14443_LB	-	IO	
C9	SE_ENA	-	I	
CSI				
Y8	CSI0_RXCLKN	AD15	I	CSI-2 Differential Receive Clock Input
Y7	CSI0_RXCLKP	AE15	I	
AB10	CSI0_RXN0	AB14	I	CSI-2 Differential Receive Input
AB9	CSI0_RXP0	AC15	I	
AA9	CSI0_RXN1	AD14	I	
AA8	CSI0_RXP1	AE14	I	
AB7	CSI0_RXN2	AD13	I	
AB6	CSI0_RXP2	AE13	I	
AA6	CSI0_RXN3	AB12	I	
AA5	CSI0_RXP3	AC13	I	
OLDI				
Y1	OLDI0_CLK0P	AE3	IO	OLDI Differential Clock
W1	OLDI0_CLK0N	AD4	IO	
AA2	OLDI0_CLK1P	AD5	IO	
Y2	OLDI0_CLK1N	AE4	IO	
L1	OLDI0_A0P	Y6	IO	OLDI Differential Data
K1	OLDI0_A0N	AA5	IO	
M2	OLDI0_A1P	AB4	IO	
L2	OLDI0_A1N	AD3	IO	
P1	OLDI0_A2P	AA8	IO	
N1	OLDI0_A2N	Y8	IO	
R2	OLDI0_A3P	AA7	IO	
P2	OLDI0_A3N	AB6	IO	
T3	OLDI0_A4P	AC5	IO	
R3	OLDI0_A4N	AC6	IO	
U1	OLDI0_A5P	AD6	IO	
T1	OLDI0_A5N	AE5	IO	
V2	OLDI0_A6P	AD7	IO	
U2	OLDI0_A6N	AE6	IO	
W3	OLDI0_A7P	AE7	IO	
V3	OLDI0_A7N	AD8	IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
MCU Domain				
D1	MCU_SPI0_CLK	A7	IO	IO Muxing Options
	MCU_GPIO0_2		IO	
E1	MCU_SPI0_D0	D9	IO	
	MCU_GPIO0_3		IO	
E2	MCU_SPI0_D1	C9	IO	
	MCU_GPIO0_4		IO	
F2	MCU_SPI0_CS0	E8	IO	
	WKUP_TIMER_IO1		IO	
	MCU_GPIO0_0		IO	
F3	MCU_SPI0_CS1	B8	IO	
	MCU_OBSCLK0		O	
	MCU_SYSCLKOUT0		O	
	MCU_EXT_REFCLK0		I	
	MCU_TIMER_IO1		IO	
	MCU_GPIO0_1		IO	
J3	MCU_UART0_RXD	B5	I	
	MCU_GPIO0_5		IO	
K3	MCU_UART0_TXD	A5	O	
	MCU_GPIO0_6		IO	
N4	MCU_UART0_CTS#	A6	I	
	MCU_TIMER_IO0		IO	
	MCU_SPI1_D0		IO	
	MCU_GPIO0_7		IO	
P4	MCU_UART0_RTS#	B6	O	
	MCU_TIMER_IO1		IO	
	MCU_SPI1_D1		IO	
	MCU_GPIO0_8		IO	
M3	MCU_I2C0_SCL	A8	IO	
	MCU_GPIO0_17		IO	
N3	MCU_I2C0_SDA	D10	IO	
	MCU_GPIO0_18		IO	
G1	MCU_MCAN0_RX	B3	I	
	MCU_TIMER_IO0		IO	
	MCU_SPI1_CS3		IO	
	MCU_GPIO0_14		IO	
H1	MCU_MCAN0_TX	D6	O	
	WKUP_TIMER_IO0		IO	
	MCU_SPI0_CS3		IO	
	MCU_GPIO0_13		IO	
H2	MCU_MCAN1_RX	D4	I	
	MCU_TIMER_IO3		IO	
	MCU_SPI0_CS2		IO	
	MCU_SPI1_CS2		IO	
	MCU_SPI1_CLK		IO	
	MCU_GPIO0_16		IO	
J2	MCU_MCAN1_TX	E5	O	
	MCU_TIMER_IO2		IO	
	MCU_SPI1_CS1		IO	
	MCU_EXT_REFCLK0		I	
	MCU_GPIO0_15		IO	

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
WKUP Domain				
E14	WKUP_CLKOUT0	A12	O	IO Muxing Options
	MCU_GPIO0_23		IO	
C3	WKUP_UART0_RXD	B4	I	
	MCU_SPI0_CS2		IO	
	MCU_GPIO0_9		IO	
C2	WKUP_UART0_TXD	C5	O	
	MCU_SPI1_CS2		IO	
	MCU_GPIO0_10		IO	
B2	WKUP_UART0_CTS#	C6	I	
	WKUP_TIMER_IO0		IO	
	MCU_SPI1_CS0		IO	
	MCU_GPIO0_11		IO	
B1	WKUP_UART0_RTS#	A4	O	
	WKUP_TIMER_IO1		IO	
	MCU_SPI1_CLK		IO	
	MCU_GPIO0_12		IO	
R5	WKUP_I2C0_SDA	A9	IO	
	MCU_GPIO0_20		IO	
P5	WKUP_I2C0_SCL	B9	IO	
	MCU_GPIO0_19		IO	
USB				
AB4	USB0_DP	AD11	IO	Differential Data Line USB2.0
AB3	USB0_DM	AE11	IO	
AA3	USB0_VBUS	AC11	I	USB Level-shifted VBUS Input See Chapter **Error! Reference source not found.**
G7	USB0_DRVVBUS	C20	O	USB VBUS Control Output (active high)
	GPIO1_50		IO	IO Muxing Options
Y5	USB1_DP	AE9	IO	Differential Data Line USB2.0
Y4	USB1_DM	AD10	IO	
W4	USB1_VBUS	AB10	I	USB Level-shifted VBUS Input See Chapter **Error! Reference source not found.**
R18	USB1_DRVVBUS	F18	O	USB VBUS Control Output (active high)
	GPIO1_51		IO	IO Muxing Options
Input Power Supply				
Y20, Y21, AA20, AA22, AB20, AB21	V_3V3_IN	-	P	Module Main Power supply Add some blocking capacitors for heavy load transients (typ. 47…100µF)
E11	V_RTC_IN	-	P	RTC Power supply
U8	V_VPP	J8	P	Used for OTP eFuses programming. Must be ramped up after device power up
Output Power Supply				
T7	V_1V8	-	O	V_1V8 power supply Max. 100 mA Should be used for Boot-Strapping
N6	V_3V3	-	O	V_3V3 power supply Max. 100 mA
W15	V_VDDSHV5	G17	O	V_VDDSHV5 power supply Max. 20 mA

3.3.2 Pinout TQMa62xxL (Table continued)

Module Pad	Signal	CPU BALL	IO	Description / Usage
Ground				
A2, A5, A8, A11, A14, A17, A20, B3, B6, B9, B12, B15, B18, B21, C1, C4, C7, C10, C13, C16, C19, C22, D2, D5, D8, D11, D14, D17, D20, E3, E6, E9, E10, E12, E15, E18, E21, F1, F4, F7, F19, F22, G2, G5, G8, G20, H3, H6, H9, H18, H21, J1, J4, J19, J22, K2, K5, K20, L3, L6, L18, L21, M1, M4, M19, M22, N2, N5, N20, P3, P6, P18, P21, R1, R4, R7, R9, R19, R22, T2, T4, T5, T6, T8, T20, U3, U4, U6, U7, U9, U18, U21, V1, V4, V7, V8, V10, V13, V16, V19, V22, W2, W5, W7, W8, W9, W11, W14, W17, W20, W21, Y3, Y6, Y9, Y12, Y15, Y18, Y19, Y22, AA1, AA4, AA7, AA10, AA13, AA16, AA19, AA21, AB2, AB5, AB8, AB11, AB14, AB17, AB19	DGND	-	P	Digital Ground

4. SOFTWARE

The TQMa62xxL is shipped with a specially adapted bootloader, which is configured for use on an MBa62xx.
This bootloader contains module specific as well as board specific adjustments like e.g.

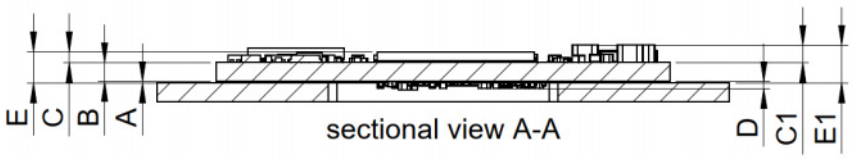
- CPU configuration
- RAM configuration / timing
- Muxing
- Clocks
- Driver strengths

When using a different bootloader this data has to be adapted. Details can be requested from TQ support. More information can be found in the Support Wiki for the TQMa62xxL.

5. MECHANICS

5.1 TQMa62xxL dimensions and footprint

The overall dimensions (length × width) of the TQMa62xxL are 38.0 mm × 38.0 mm (± 0.1 mm).
The mass of TQMa62xxL is TBD.



Heigth [mm]			
Dimension	Value	Tolerance	Comment
A	0.125	+0.075/-0.025	Board to board distance
B	1.60	±0.16	PCB thickness
C	0.93	±0.08	CPU height
C1	1.32	±0.20	Ceramic capacitor (highest part)
D	0.57	±0.15	Component height below module
E	2.68	±0.18	Overall height to CPU surface
E1	3.07	±0.26	Overall height to ceramic capacitor

99.73 % of all modules will meet the tolerance specified in table above.
Height values of 3D model may differ from this drawing.

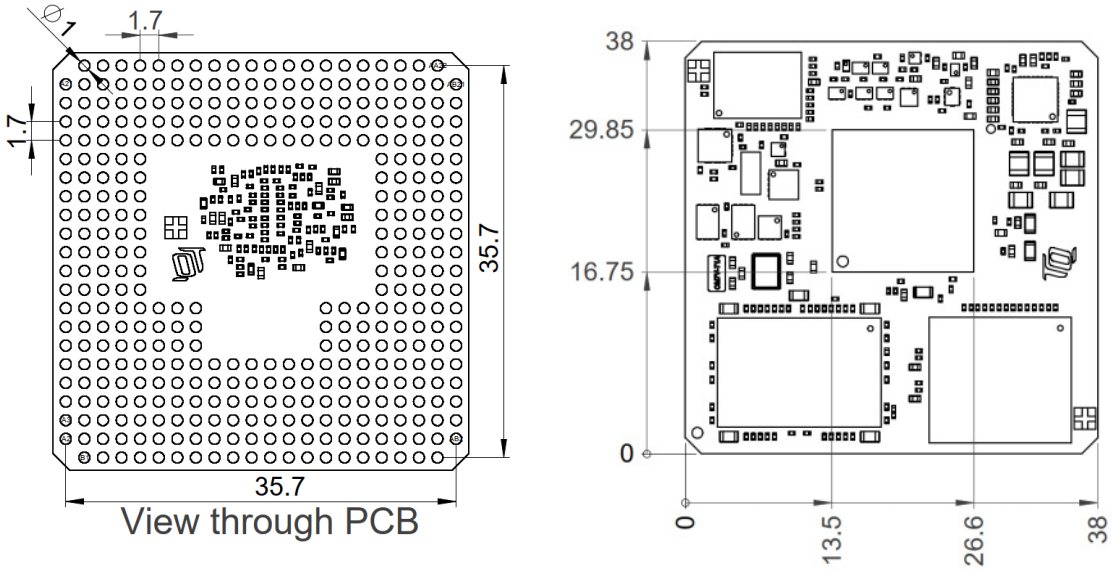


Figure 16: Dimensions TQMa62xxL

5.2 TQMa62xxL component placement and labeling

The label AK1 includes TQ serial number, MAC address, and product name.

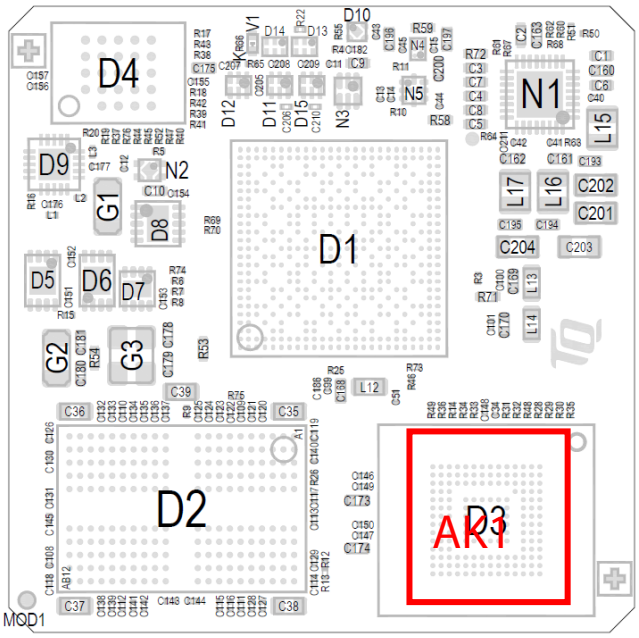


Figure 17: TQMa62xxL top view

5.3 Protection against external effects

As an embedded module the TQMa62xxL is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.4 Thermal management

The power dissipation mainly depends on the software used and can vary according to the application. The power dissipation mainly arises at the processor, the switching regulators and the LPDDR4 devices. It is the customer's responsibility to define a suitable cooling method for his use case.

Attention: Destruction or malfunction, TQMa62xxL cooling	
	The AM62x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM62x must be taken into consideration when connecting the heat sink, see **Error! Reference source not found.**. The AM62x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa62xxL and thus malfunction, deterioration or destruction.

5.5 Structural requirements

The TQMa62xxL has to be soldered on the carrier board. The TQMa62xxL is held on the mainboard by the holding force of the solder connections from the LGA pads and requires no further fastening measures. If there are high requirements for vibration and shock resistance, a module holder must be provided in the final application to additionally hold the module in position. Since no heavy and large components are used, there are no further requirements.

Attention: Note on equipping the base board	
	To ensure a high-quality connection of the LGA pads when reflow soldering the TQMa62xxL, the LGA pads must be free of grease and contamination. Please contact TQ-Support for soldering instructions (6).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa62xxL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding besides, take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.
As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa62xxL.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤ 3.3 V DC), tests with respect to the operational and personal safety haven't been carried out.

6.4 Climatic and operational conditions

The temperature range, in which the TQMa62xxL works reliably, strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.
In general, a reliable operation is given when following conditions are met:

Table 13: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Environmental temperature	–40 °C to +85 °C	With appropriate cooling
Permitted storage temperature	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

6.5 Intended Use

TQ DEVICES, PRODUCTS AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION IN NUCLEAR FACILITIES, AIRCRAFT OR OTHER TRANSPORTATION NAVIGATION OR COMMUNICATION SYSTEMS, AIR TRAFFIC CONTROL SYSTEMS, LIFE SUPPORT MACHINES, WEAPONS SYSTEMS, OR ANY OTHER EQUIPMENT OR APPLICATION REQUIRING FAIL-SAFE PERFORMANCE OR IN WHICH THE FAILURE OF TQ PRODUCTS COULD LEAD TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE. (COLLECTIVELY, "HIGH RISK APPLICATIONS")

You understand and agree that your use of TQ products or devices as a component in your applications are solely at your own risk. To minimize the risks associated with your products, devices and applications, you should take appropriate operational and design related protective measures.

You are solely responsible for complying with all legal, regulatory, safety and security requirements relating to your products. You are responsible for ensuring that your systems (and any TQ hardware or software components incorporated into your

systems or products) comply with all applicable requirements. Unless otherwise explicitly stated in our product related documentation, TQ devices are not designed with fault tolerance capabilities or features and therefore cannot be considered as being designed, manufactured or otherwise set up to be compliant for any implementation or resale as a device in high risk applications. All application and safety information in this document (including application descriptions, suggested safety precautions, recommended TQ products or any other materials) is for reference only. Only trained personnel in a suitable work area are permitted to handle and operate TQ products and devices. Please follow the general IT security guidelines applicable to the country or location in which you intend to use the equipment.

6.6 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.7 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.8 Reliability and service life

For the TQMa62xxL, a constant error rate results in an MTBF of approximately 1,123,152 hours (TQMa6254L).

Attention must be paid to a construction that is insensitive to vibration and shock.

Service life-limiting components such as electrolytic capacitors were not used.

6.9 Environment protection

6.9.1 RoHS

The TQMa62xxL is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

6.9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa62xxL was designed to be recyclable and easy to repair.

6.10 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic).

Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

6.11 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa62xxL must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMa62xxL enable compliance with EuP requirements for the TQMa62xx.

6.12 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

6.13 Battery

No batteries are used on the TQMa62xxL.

6.14 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa62xxL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa62xxL is delivered in reusable packaging.

6.15 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

7. APPENDIX

7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 14: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AIN	Analog In
ARM®	Advanced RISC Machine
AVS	Adaptive Voltage Scaling
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
DC	Direct Current
DDR3L	Double Data Rate Type three Low voltage
DIN	Deutsche Industrie Norm
DVS	Dynamic Voltage Scaling
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multi-Media Card
EN	Europäische Norm
ESD	Electro-Static Discharge
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input/Output
GPMC	General Purpose Memory Controller
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IP	Ingress Protection
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MCSPI	Multichannel Serial Port Interface
MD	Management Data
MII	Media-Independent Interface
MMC	Multi-Media Card
MTBF	Mean operating Time Between Failures

7.1 Acronyms and definitions (continued)

Table 14: Acronyms (continued)

Acronym	Meaning
n.a.	Not Available
NC	Not Connected
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRCM	Power and Clock Management
PU	Pull-Up
PWM	Pulse-Width Modulation
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection
WXGA	Wide Extended Graphics Array

7.2 References

Table 15: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	AM62x Sitara Processors Datasheet	A / Nov. 2022	Texas Instruments
(2)	AM62x Processors Silicon Revision 1.0 Technical Reference Manual	A / Nov 2022	Texas Instruments
(3)	AM62x Processor Errata	A / Jul. 2022	Texas Instruments
(4)	MBa62xx User's Manual	– current –	TQ-Systems
(5)	Support-Wiki for the TQMa62xxL	– current –	TQ-Systems
(6)	Processing instructions for TQMa62xxL	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

Technology in Quality