TQMa335xL
User's Manual

TQMa335xL UM 0102
05.03.2024

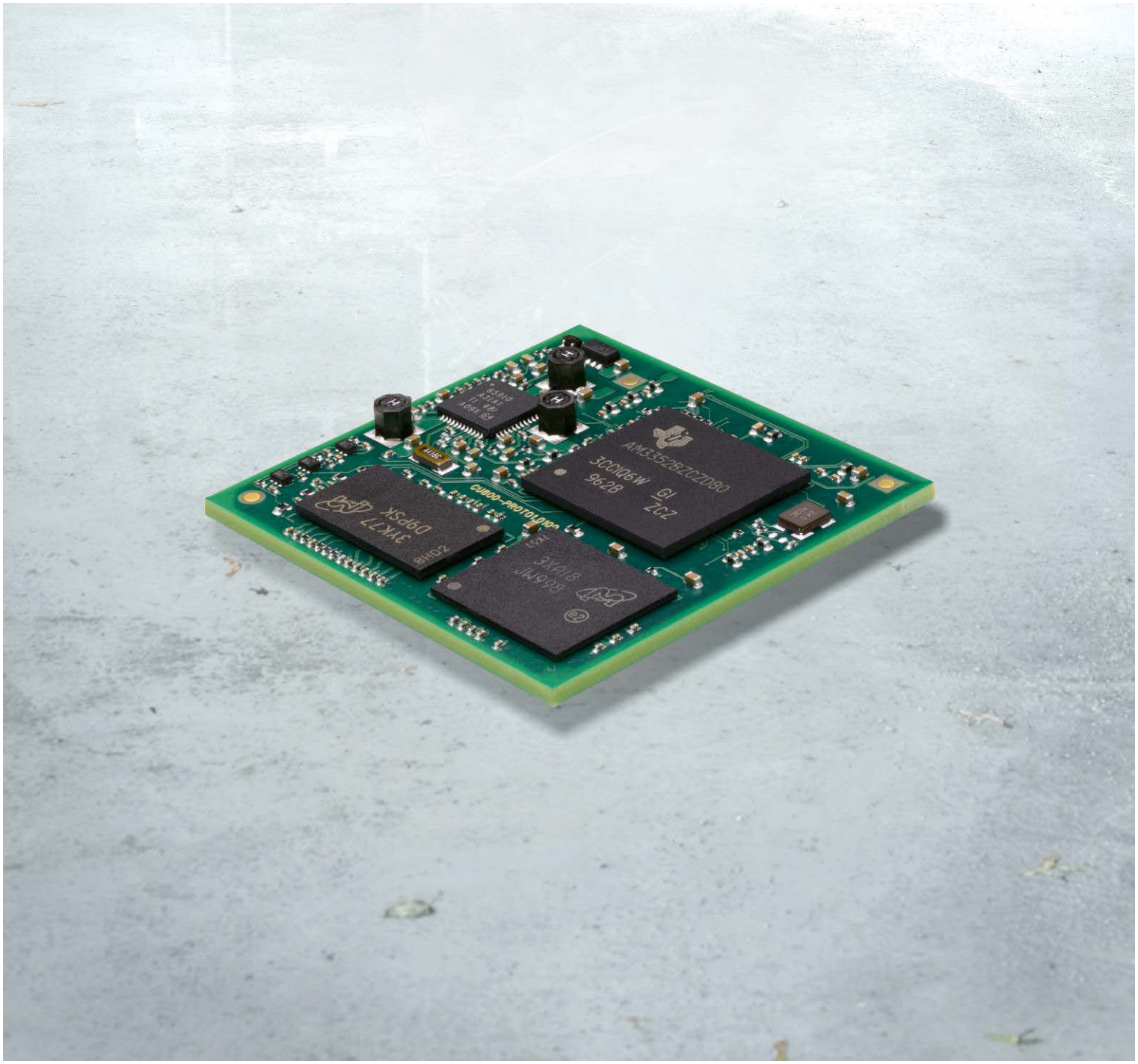

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ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	03.04.2019	Petz		Initial release
0101	20.09.2019	Petz	3.2.1.4.3 5.5, 5.6 (10)	Boot device NOR flash removed Updated Added
0102	05.03.2024	Kreuzer	3.2.3	“battery” replaced with “electrolytic capacitor”

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive devices and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa335xL and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you power up the TQMa335xL or the Starterkit, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manuals of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa335x circuit diagram
- MBa335x User's Manual
- Sitara™ AM335x Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqma335x

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa335xL revision 02xx, and refers to some software settings.
It does not replace the AM335x Reference Manual.
The TQMa335xL is a universal Minimodule based on the Texas Instruments ARM® Cortex® A8 Sitara™ AM335x.
The AM335x Cortex® A8 core works with up to 800 MHz.
The TQMa335xL extends the TQC product range and offers an outstanding computing performance.

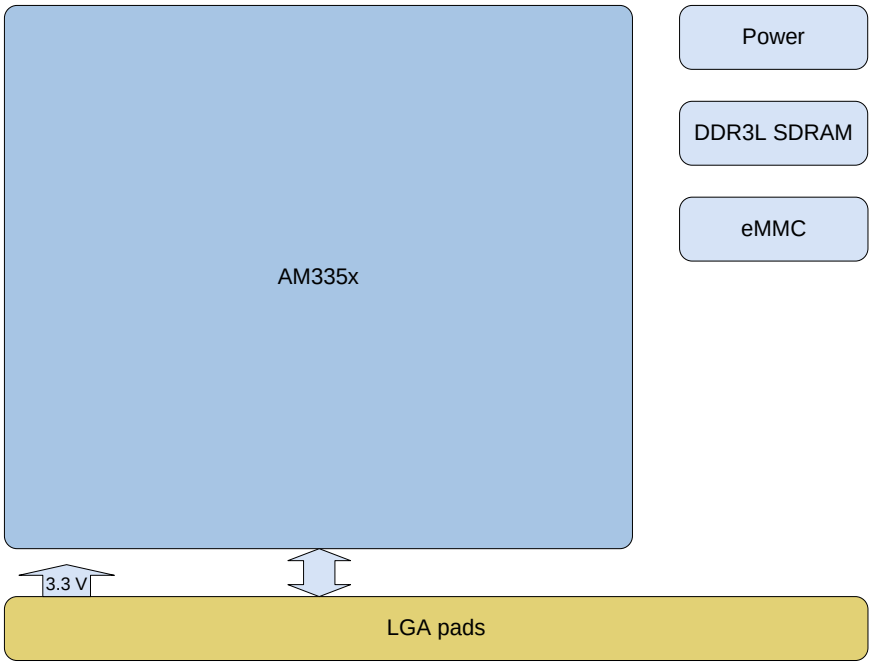

Illustration 1: Block diagram TQMa335xL (simplified)

2.1 Key functions and characteristics

The TQMa335xL provides the following key functions and characteristics:

- Texas Instruments AM335x
- Up to 512 Mbyte DDR3L SDRAM with 16 bit interface
- Up to 8 Gbyte eMMC NAND flash
- Texas Instruments PMIC
- All essential AM335x pins are routed to the TQMa335xL pads
- Extended temperature range
- Single power supply 3.3 V

2.2 Available interfaces

The TQMa335xL provides the following interfaces at the TQMa335xL pads:

- 2 × Ethernet 10/100/1000 Mbit, RGMII
- 2 × USB 2.0 Hi-Speed
- 2 × CAN 2.0B
- 3 × UART (1 UART with handshake)
- 1 × SD 4 bit (SDIO / MMC / SD card)
- 2 × SPI
- 2 × I^2C
- 1 × I^2S (MCASP0)
- 3 × GPIO
- 4 × PWM
- 1 × parallel display RGB 24 bit
- 1 × JTAG
- 2 × General Purpose Clock
- 8 × AIN inclusive resistive touch controller (12 bit ADC)

As an alternative to the default interfaces, more AM335x interfaces are available with an adapted pin configuration.
These are amongst others:

- GPMC (General-Purpose Memory Controller)
- PRU-MII1, PRU-MII2 (only available with AM3356, -7, -8, -9)
- PWMSS (Pulse-Width Modulation Subsystem)
- Enhanced Serial Audio Interface
- Ethernet 10/100 RMII
- More audio interfaces
- More I^2C interfaces
- More SPI interfaces
- More UARTs

All useful AM335x signals are routed to the TQMa335xL pads.
There are no restrictions for customers using the TQMa335xL with respect to an integrated customised design.
Please take note of that not all listed interfaces can be used simultaneously.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa335xL, and the BSP provided by TQ-Systems GmbH, see also section 4.

3.1 System overview

3.1.1 System architecture / block diagram

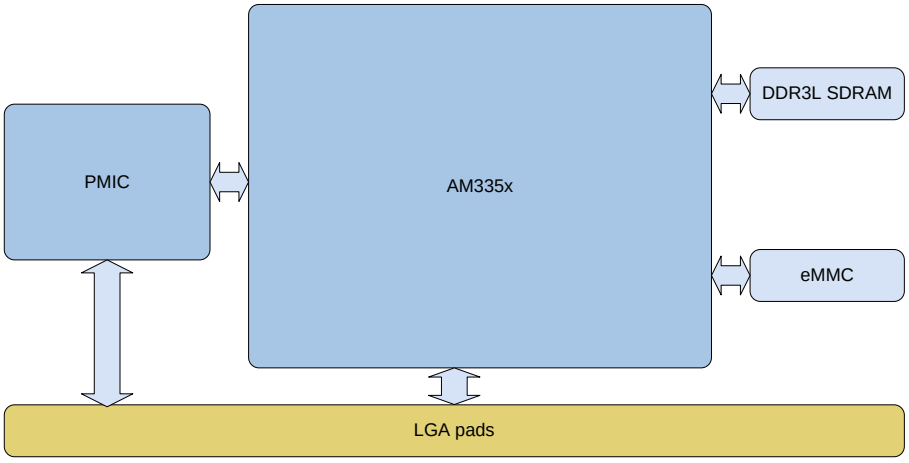

Illustration 2: TQMa335xL block diagram

3.1.2 Functionality

The following key functions are implemented on the TQMa335xL:

- AM335x (-2, -4, -8, -9, are standard, -1, -6, -7 on request)
- DDR3L SDRAM
- eMMC NAND flash
- PMIC

3.1.3 Pin multiplexing

The pin multiplexing of the AM335x permits to use many pins for different interfaces.
The information provided in this User's Manual is based on the BSP provided by TQ-Systems GmbH.

Attention: Destruction or malfunction	
	Many AM335x pins can be configured as different function. Please take note of the information in the AM335x Data Sheet (1) concerning the configuration of these pins before integration / start-up of your carrier board / Starterkit. Please also take note of the latest AM335x errata (7).

3.2 System components

3.2.1 AM335x processor

The following illustration shows the AM335x processor family block diagram:

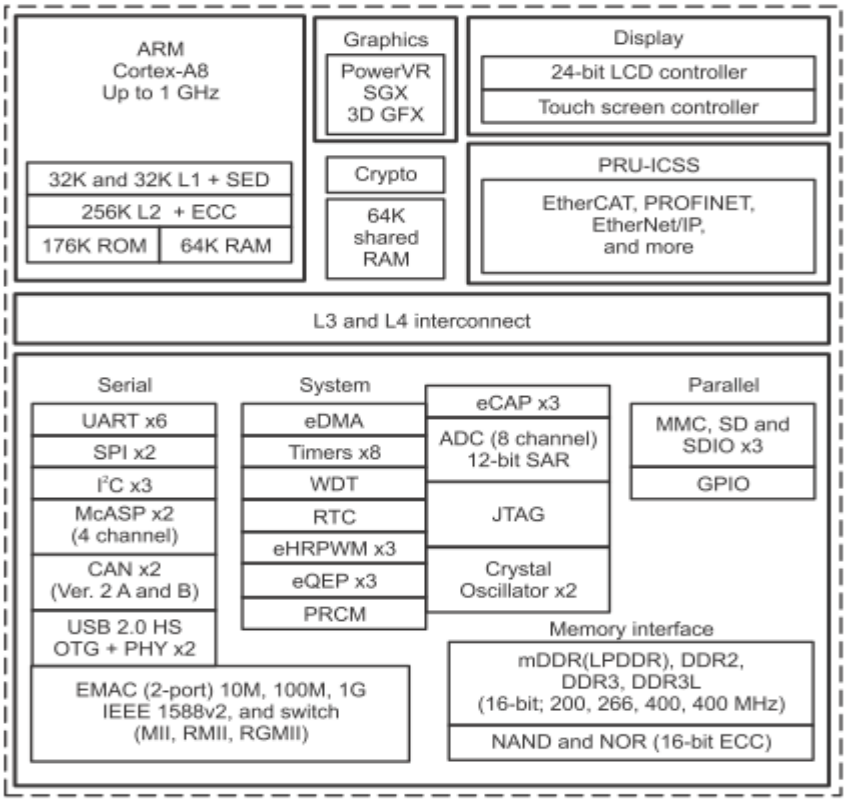

Figure 1-1. AM335x Functional Block Diagram

Illustration 3: Block diagram AM335x
(Source: Texas Instruments)

3.2.1.1 AM335x derivatives

Depending on the TQMa335xL version, one of the following AM335x derivatives is assembled:

Table 2: AM335x derivatives

Description	Part number	Clock	$T_{junction}$	AM335x mask
AM3352	AM3352BZCZA80	800 MHz	–40 °C to +105 °C	2.1
AM3354	AM3354BZCZA80	800 MHz	–40 °C to +105 °C	2.1
AM3358	AM3358BZCZA80	800 MHz	–40 °C to +105 °C	2.1
AM3359	AM3359BZCZA80	800 MHz	–40 °C to +105 °C	2.1

Attention: Malfunction	
	Please take note of the latest AM335x errata (7).

3.2.1.2 Boot modes

The AM335x provides a ROM with integrated boot loader.
After power-up the boot code initialises the hardware and then loads the program image from the selected boot device.
The integrated eMMC can be selected as standard boot device for the TQMa335xL.
More external boot devices are available as an alternative to eMMC.
Information thereto can be found in the AM335x Data Sheet (1) and the AM335x Reference Manual (3).
The AM335x supports so-called boot-sequences, i.e. if it fails to boot from the first boot device, it will try to boot from the next one automatically.

Table 3: Boot sequence

Boot Sequence			
1st	2nd	3rd	4th
MMC0 / SD	SPI0 / NOR (not available on TQMa335xL)	UART0 / n.a.	USB0 / n.a.
MMC1/ eMMC	MMC0 / SD	UART0 / n.a.	USB0 / n.a.
SPI0 / NOR (not available on TQMa335xL)	MMC0 / SD	USB0 / n.a.	UART0 / n.a.

The boot device and its configuration as well as other AM335x settings have to be done via Boot Mode Register SYSBOOT.
The register SYSBOOT is read during reset from pins LCD_DATA[15:0].

Attention: Malfunction	
	On the carrier board must be ensured that even in the third and fourth boot sequence no pins drive against each other!

The settings for other boot devices are to be taken from the AM335x Data Sheet (1).

3.2.1.3 Boot configuration

The boot configuration of the TQMa335xL is defined through 16 GPIO pins.

Note: Boot configuration	
	None of these 16 boot configuration pins are connected on the TQMa335xL, which means, the TQMa335xL is delivered with no preset boot configuration.

With bits SYSBOOT[15:14] and SYSBOOT[5] some general settings are carried out, independent from the boot device.
The value in the following table printed in **bold** is used on account of the 24 MHz oscillator assembled on the TQMa335xL.
The bits SYSBOOT[15:14] set the frequency of the oscillator.

Table 4: Oscillator frequency

SYSBOOT[15:14]	Oscillator frequency / MHz	Remark
00b	19.2	–
01b	**24**	**Default**
10b	25	–
11b	26	–

Bit SYSBOOT[5] indicates whether CLKOUT1 is activated.

Table 5: General boot configuration CLKOUT1

SYSBOOT[5]	CLKOUT1
0	Deactivated
1	Activated

The boot device or the boot sequence is defined with bits SYSBOOT[4:0].
The following table shows the boot sequence defined for the MBa335x.

Table 6: Boot device selection

SYSBOOT[4:0]	Boot Sequence			
	1st	**2nd**	**3rd**	**4th**
10111b	MMC0 / SD	SPI0 / NOR (not available on TQMa335xL)	UART0 / n.a.	USB0 / n.a.
11100b	MMC1 / eMMC	MMC0 / SD	UART0 / n.a.	USB0 / n.a.
11000b	SPI0 / NOR (not available on TQMa335xL)	MMC0 / SD	USB0 / n.a.	UART0 / n.a.

Attention: Malfunction	
	On the carrier board must be ensured that even in the third and fourth boot sequence no pins drive against each other!

3.2.1.4 Boot interfaces

The configuration of the following boot devices is described in the next sections:

- MMC0 (external SD card)
- MMC1 (eMMC on TQMa335xL)
- SPI0 NOR flash (not available on TQMa335xL)

Attention: Destruction or malfunction	
	Many AM335x pins can be configured as different function. Please pay attention to the notes in the AM335x Data Sheet (1) concerning the wiring of these pins before integration / start-up of your carrier board / Starterkit. Please also take note of the latest AM335x errata (7).

3.2.1.4.1 Boot device SD card

The SD card boots from MMC0 of the AM335x. The following pins must be used for the boot process.

Table 7: Pins used for SD card boot

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
F17	MMC0_CLK	MMC0_CLK	I/O	G17	–
F15	MMC0_CMD	MMC0_CMD	I/O	G18	–
E14	MMC0_DAT3	MMC0_DAT3	I/O	F17	–
E15	MMC0_DAT2	MMC0_DAT2	I/O	F18	–
E16	MMC0_DAT1	MMC0_DAT1	I/O	G15	–
E17	MMC0_DAT0	MMC0_DAT0	I/O	G16	–

3.2.1.4.2 Boot device eMMC

The eMMC boots from MMC1 of the AM335x. MMC1 supports eMMCs with a size of 4 Gbyte or greater.
The following pins are used for the boot process.

Table 8: Pins used for eMMC boot

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
P3	MMC1_CLK	GPMC_CS#1	I/O	U9	–
R3	MMC1_CMD	GPMC_CS#2	I/O	V9	–
M2	MMC1_DAT3	GPMC_AD3	I/O	T8	4-bit boot
L4	MMC1_DAT2	GPMC_AD2	I/O	R8	
L3	MMC1_DAT1	GPMC_AD1	I/O	V7	
L2	MMC1_DAT0	GPMC_AD0	I/O	U7	

3.2.2 Memory

3.2.2.1 DDR3L SDRAM

The TQMa335xL is equipped with one DDR3L SDRAM chip with a data bus width of 16 bits.
The AM335x supports 303 to 400 MHz bus clock. In the BSP provided by TQ-Systems GmbH the memory is clocked with 400 MHz.
The following block diagram shows how the DDR3L SDRAM is connected to the AM335x.

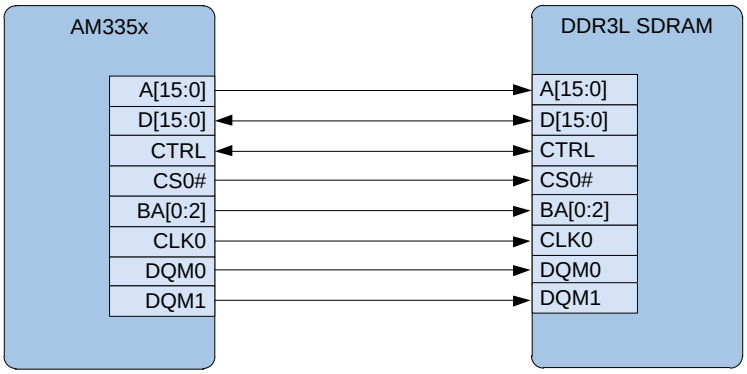

Illustration 4: Block diagram DDR3L SDRAM connection

The TQMa335xL can be equipped with 256 Mbyte or 512 Mbyte of DDR3L SDRAM:

Table 9: DDR3L SDRAM

Placement option	Size
1 × DDR3L 128M16	256 Mbyte
1 × DDR3L 256M16	512 Mbyte

The SDRAM is mapped to the following address:

Table 10: SDRAM address space

Start address	Size	Chip Select	Remark
0x8000_0000	0x4000_0000	CS0#	1 Gbyte

3.2.2.2 eMMC NAND flash

The eMMC NAND flash on the TQMa335xL contains the boot loader and the application software.
The following block diagram shows how the eMMC flash is connected to the AM335x.

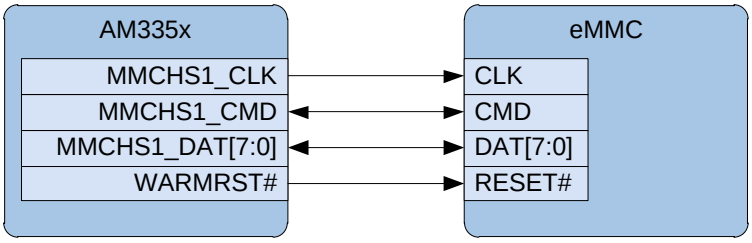

Illustration 5: Block diagram eMMC flash connection

3.2.3 AM335x-RTC, PMIC-RTC

Both the AM335x and the PMIC on the TQMa335xL provide an RTC, which have their own power domain VRTC.

The RTC power domain VRTC of the CPU is supplied by the PMIC through an internal regulator.

The PMIC is either supplied by V_{IN} (VCC3V3IN), or through the PMIC backup supply pin VBACKUP_PMIC, which is routed to TQMa335xL pad C9.

The PMIC can charge an electrolytic capacitor or a SuperCap connected through TQMa335xL pad C9.

Charging methods and electrical characteristics are to be taken from the PMIC User's Guide (6).

The typical current consumption of the PMIC_RTC is approximately 20 µA @ 3 V.

The accuracy of the RTC is mainly determined by the characteristics of the quartz used. The 32.768 kHz crystal type FC-135 used on the TQMa335xL has a standard frequency tolerance of ±20 ppm @ +25 °C. (Parabolic coefficient: max. -0.04×10^{-6} / °C^2.)

Note: Current consumption	
	Long-term bridging with a coin cell is not possible due to the high current consumption of the PMIC-RTC. Depending on the use case a Li coin cell or a SuperCap can be used.

3.2.4 Interfaces

3.2.4.1 Overview

The TQMa335xL provides interfaces with primary function. These can be used simultaneously independent from its configuration. If a secondary function (e.g. MII0) is required, some primary functions may be omitted. More information regarding availability and pinout can be found in the AM335x Data Sheet (1) and the AM335x Reference Manual (3).

Table 11: Internal interfaces

Interface	Qty.	Function	Chapter	Remark
MMC1	1	Primary	3.2.2.2	eMMC, 8 bit

Table 12: External interfaces

Interface	Qty.	Function	Chapter	Remark
AIN	8	Primary	3.2.4.13	AIN0 – AIN7
CLOCKOUT	2	Primary	3.2.4.21	General Purpose Clocks
CLOCKIN	1	–	–	–
CAN	2	Secondary	3.2.4.11	DCAN0 / DCAN1
JTAG / DEBUG	1	Primary	3.2.4.7	JTAG / EMU0 / EMU1
	3	Secondary		EMU2 / EMU3 / EMU4
ECAP	3	Secondary	–	ECAP0 – 2
ECAP_PRUSS	1	Secondary	–	–
ECAT_PRUSS	1	Secondary	–	–
EQEP	2	Primary	–	–
Gbit-Eth MAC	1	Primary	3.2.4.2	MII1
	1	Secondary	3.2.4.1	MII0
GLUE	2	Primary	3.2.4.21	XDMA_EVENT_INTR0 / 1
GPIO	–	Secondary	3.2.4.5	GPIO[0:2] (32 bit), GPIO3 (22 bit)
GPMC	1	Primary	3.2.4.3	12 address / 16 address/data
EMIF	1	Primary	3.2.2.1	DDR
I2C	1	Primary	3.2.4.12	I2C0
	2	Secondary		I2C1 / I2C2
LCD controller	1	Primary	3.2.4.9	RGB16
	1	Secondary		RGB24
MCASP	1	Primary	3.2.4.13	AUD3 / I2S
MCASP	3	Secondary		AUD4 / AUD5 / AUD6 | multiplexing has to be adapted
MDIO	1	Primary	–	–
MDIO_PRUSS	1	Secondary	–	–
MII_PRUSS	2	Secondary	3.2.4.2	MII0_PRUSS / MII1_PRUSS
MMC	1	Primary	3.2.4.4	MMC0 / SD card / 1/4 bit
	2	Secondary		MMC1 / eMMC / 1/4/8 bit
PRU_PRUSS	1	Secondary	–	16 bit interface
RTC	1	Primary	3.2.3	–
SPI	1	Primary	3.2.4.14	SPI0
	1	Secondary		SPI1
TIMER	4	Secondary	–	TIMER4 – 7
UART	2	Primary	3.2.4.15	UART0 / UART1
	4	Secondary	3.2.4.16	UART2 / UART3 / UART4 / UART5
UART_PRUSS	1	Secondary	–	UART_PRUSS0
USB	2	Primary	3.2.4.19	USB0_OTG / USB1_OTG
XTAL	2	Primary	–	XTALOSC0 / XTALOSC1

3.2.4.2 Gigabit Ethernet MAC

The AM335x provides a 10/100/1000 Mbit MAC Core.
Two Ethernet interfaces are routed to the TQMa335xL pads using the 3-port switch. The switch supports two MII, RMII and RGMII.
The following table shows the signals used.

Table 13: RGMII1

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
M15	RGMII1_RCLK	MII1_RX_CLK	I/O	L18
R14	RGMII1_RCTL	MII1_RX_DV	I/O	J17
M16	RGMII1_RD3	MII1_RXD3	I/O	L17
M17	RGMII1_RD2	MII1_RXD2	I/O	L16
N16	RGMII1_RD1	MII1_RXD1	I/O	L15
N17	RGMII1_RD0	MII1_RXD0	I/O	M16
K15	RGMII1_TCLK	MII1_TX_CLK	I/O	K18
L15	RGMII1_TCTL	MII1_TX_EN	I/O	J16
K16	RGMII1_TD3	MII1_TXD3	I/O	J18
K17	RGMII1_TD2	MII1_TXD2	I/O	K15
L16	RGMII1_TD1	MII1_TXD1	I/O	K16
L17	RGMII1_TD0	MII1_TXD0	I/O	K17

Table 14: RGMII2

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
P13	RGMII2_RCLK	GPMC_A7	I/O	T15
R14	RGMII2_RCTL	GPMC_A1	I/O	V14
T14	RGMII2_RD3	GPMC_A8	I/O	V16
U14	RGMII2_RD2	GPMC_A9	I/O	U16
T15	RGMII2_RD1	GPMC_A10	I/O	T16
U15	RGMII2_RD0	GPMC_A11	I/O	V17
R12	RGMII2_TCLK	GPMC_A6	I/O	U15
R13	RGMII2_TCTL	GPMC_A0	I/O	R13
T12	RGMII2_TD3	GPMC_A2	I/O	U14
U12	RGMII2_TD2	GPMC_A3	I/O	T14
T13	RGMII2_TD1	GPMC_A4	I/O	R14
U13	RGMII2_TD0	GPMC_A5	I/O	V15

3.2.4.3 GPMC / External memory bus [1]

The AM335x provides a General Purpose Memory Controller (GPMC), whose pins are routed to the TQMa335xL pads.
The GPMC signals are routed to the TQMa335xL pads as secondary function. GPMC-CLK is multiplexed with MMC1-CLK.

Note: Signal overlapping	
	There is an overlapping with an eMMC signal. GPMC-CLK is multiplexed with MMC1-CLK.

1: Currently not supported.

3.2.4.4 MMC / SD card

An SD card can be connected to the TQMa335xL. The MMC0 controller is routed to the TQMa335xL pads for this purpose.
The MMC0 interface supports SD and SDIO as well.
The following table shows the signals used by the SD card interface.

Table 15: SD card signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
F17	MMC0_CLK	MMC0_CLK	I/O	G17
F15	MMC0_CMD	MMC0_CMD	I/O	G18
E14	MMC0_DAT3	MMC0_DAT3	I/O	F17
E15	MMC0_DAT2	MMC0_DAT2	I/O	F18
E16	MMC0_DAT1	MMC0_DAT1	I/O	G15
E17	MMC0_DAT0	MMC0_DAT0	I/O	G16

3.2.4.5 GPIO

Besides their interface function, most AM335x pins can also be used as GPIOs.
All these GPIOs are interrupt capable. Details are to be taken from the AM335x Data Sheet (1).
Moreover several pins marked as GPIO are already routed to the TQMa335xL pads.
The following table shows the signals, which can be used as GPIOs.

Table 16: GPIO signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
R1	GPIO1_29	GPMC_CS#0	I/O	V6
P1	GPIO1_28	GPMC_BE#1	I/O	U18
T1	GPIO2_0	GPMC_CS#3	I/O	T13

The electrical characteristics of the GPIOs are to be taken from the respective Data Sheets provided by Texas Instruments (2), (3).

3.2.4.6 PWM

The AM335x provides several PWMs, which are routed to the TQMa335xL pads.
The following table shows the available PWM signals.

Table 17: PWM signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
U2	Timer4	GPMC_ADV#_ALE	I/O	R7
T2	Timer5	GPMC_BE#0_CLE	I/O	T6
U3	Timer6	GPMC_WE#	I/O	U6
T3	Timer7	GPMC_OE#_RE#	I/O	T7

3.2.4.7 JTAG / DEBUG

The AM335x has two JTAG modes. The JTAG mode is defined by pins EMU0 and EMU1 during reset.
The following table shows the modes available and the mode selected on the TQMa335xL:

Table 18: JTAG modes

EMU0	EMU1	Name	Remark
1	0	ICEPick	TAP only + WIR mode
1	1	ICEPick	TAP only (default mode)

The following table shows the signals used by the JTAG interface.

Table 19: JTAG signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
C4	TDI	TDI	I	B11	–
D4	TDO	TDO	O	A11	–
C3	TMS	TMS	I	C11	–
D5	TCK	TCK	I	A12	–
D3	TRST#	TRST#	I	B10	–
E3	EMU1	EMU1	I/O	B14	–
E4	EMU0	EMU0	I/O	C14	–

3.2.4.8 Touch and analog inputs

The AM335x provides analog inputs including a touch interface. These inputs are routed to the TQMa335xL pads.
For the analog inputs a reference voltage of 1.8 V ±3 % is provided on the TQMa335xL.
The following table shows the signals used by the analog interface.

Table 20: Touch signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
B5	AIN7	AIN7	A_{IN}	C9	–
B3	AIN3	AIN3	A_{IN}	A7	On MBa335x: Y–
A5	AIN6	AIN6	A_{IN}	A8	–
A3	AIN2	AIN2	A_{IN}	B7	On MBa335x: Y+
B4	AIN5	AIN5	A_{IN}	B8	–
B2	AIN1	AIN1	A_{IN}	C7	On MBa335x: X–
A4	AIN4	AIN4	A_{IN}	C8	–
A2	AIN0	AIN0	A_{IN}	B6	On MBa335x: X+

Wake-up by touch is possible. The implementation and the selection of a certain power mode is software dependent.

3.2.4.9 LCD controller

The LCD controller of the AM335x supports up to 24-bit (RGB) with a resolution of up to WXGA (1366 × 768).
All necessary pins are routed to the TQMa335xL pads.
Information regarding supported displays and resolutions can be found in the AM335x Reference Manual (3).
The following table shows the signals used by the LCD controller.

Table 21: LCD signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
R5	LCD_MCLK	GPMC_CLK	I/O	V12
P5	LCD_HSYNC	LCD_HSYNC	I/O	R5
P4	LCD_VSYNC	LCD_VSYNC	I/O	U5
U5	LCD_PCLK	LCD_PCLK	I/O	V5
T5	LCD_AC_BIAS_EN	LCD_AC_BIAS_EN	I/O	R6
P11	LCD_DATA23	GPMC_AD8	I/O	U10
R11	LCD_DATA22	GPMC_AD9	I/O	T10
T11	LCD_DATA21	GPMC_AD10	I/O	T11
U11	LCD_DATA20	GPMC_AD11	I/O	U12
P10	LCD_DATA19	GPMC_AD12	I/O	T12
R10	LCD_DATA18	GPMC_AD13	I/O	R12
T10	LCD_DATA17	GPMC_AD14	I/O	V13
U10	LCD_DATA16	GPMC_AD15	I/O	U13
P9	LCD_DATA15	LCD_DATA15	I/O	T5
R9	LCD_DATA14	LCD_DATA14	I/O	V4
T9	LCD_DATA13	LCD_DATA13	I/O	V3
U9	LCD_DATA12	LCD_DATA12	I/O	V2
P8	LCD_DATA11	LCD_DATA11	I/O	U4
R8	LCD_DATA10	LCD_DATA10	I/O	U3
T8	LCD_DATA9	LCD_DATA9	I/O	U2
U8	LCD_DATA8	LCD_DATA8	I/O	U1
P7	LCD_DATA7	LCD_DATA7	I/O	T4
R7	LCD_DATA6	LCD_DATA6	I/O	T3
T7	LCD_DATA5	LCD_DATA5	I/O	T2
U7	LCD_DATA4	LCD_DATA4	I/O	T1
P6	LCD_DATA3	LCD_DATA3	I/O	R4
R6	LCD_DATA2	LCD_DATA2	I/O	R3
T6	LCD_DATA1	LCD_DATA1	I/O	R2
U6	LCD_DATA0	LCD_DATA0	I/O	R1

3.2.4.10 Serial interfaces

The supported standards, transfer modes and rates of the following interfaces are to be taken from the AM335x Data Sheet (1).

3.2.4.11 CAN

The AM335x provides two integrated CAN controller. The signals of both CAN controllers are routed to the TQMa335xL pads.
The drivers have to be integrated on the carrier board.
The following table shows the signals used by the CAN interfaces.

Table 22: CAN1 / CAN2 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
H1	DCAN0_RX	UART1_RTS#	I/O	D17
G1	DCAN0_TX	UART1_CTS#	I/O	D18
K1	DCAN1_RX	UART0_RTS#	I/O	E17
J1	DCAN1_TX	UART0_CTS#	I/O	E18

3.2.4.12 I2C

The AM335x provides three I²C interfaces.
I2C0 and I2C1 are routed to the TQMa335xL pads and are available as a primary function.
The following table shows the signals used by the I2C buses.

Table 23: I2C0 and I2C1 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
C1	I2C0_SCL	I2C0_SCL	I/O	C16	3.3 kΩ PU to 3.3 V on TQMa335xL
D1	I2C0_SDA	I2C0_SDA	I/O	C17	3.3 kΩ PU to 3.3 V on TQMa335xL
F1	I2C1_SCL	UART1_TXD	I/O	D15	–
E1	I2C1_SDA	UART1_RXD	I/O	D16	–

The I2C0 bus is also used for the PMIC on the TQMa335xL. It has the following I²C addresses:

Table 24: I2C0 addresses

Function	Device	Address
PMIC	TPS65910	0x12 / 0b001 0010 0x2D / 0b010 1101

If more devices have to be connected to the I2C0 bus on the carrier board, the maximum capacitive bus load accordingly to the I²C standard has to be adhered to. If required additional pull-ups should be provided on the carrier board at the bus.

3.2.4.13 I2S / AUDMUX

The Multichannel Audio Serial Port 0 (MCASP0) is routed to the TQMa335xL pads to connect an audio-codec via I²S.
The following table shows the signals used by the AUD3 interface.

Table 25: MCASP0 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
C16	MCASP0_ACLKR	MCASP0_ACLKR	I/O	B12	–
C15	MCASP0_ACLKX	MCASP0_ACLKX	I/O	A13	–
B17	MCASP0_FSX	MCASP0_FSX	I/O	B13	–
C17	MCASP0_FSR	MCASP0_FSR	I/O	C13	–
B15	MCASP0_AXR3	MCASP0_AXR3	I/O	A14	–
A15	MCASP0_AXR2	MCASP0_AXR2	I/O	C12	–
B16	MCASP0_AXR1	MCASP0_AXR1	I/O	D13	–
A16	MCASP0_AXR0	MCASP0_AXR0	I/O	D12	–

The MCASP-Interface supports I2S and other synchronous modes.
More information can be found in the AM335x Reference Manual (3).

3.2.4.14 SPI

The AM335x provides two MCSPIs (Multichannel Serial Port Interface). Both interfaces are routed to the TQMa335xL pads.
The following table shows the signals used by the SPI0 and SPI1 interfaces.

Table 26: SPI0 and SPI1 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
F14	SPI0_CS0#	SPI0_CS0#	I/O	A16	CS
G14	SPI0_SCLK	SPI0_SCLK	I/O	A17	CLK
J14	SPI0_MOSI	SPI0_D1	I/O	B16	MOSI
H14	SPI0_MISO	SPI0_D0	I/O	B17	MISO
N15	SPI1_CS0#	RMII1_REF_CLK	I/O	H18	–
P14	SPI1_SCLK	MII1_COL	I/O	H16	–
N14	SPI1_MOSI	MII1_CRS	I/O	H17	SPI1_D0
M14	SPI1_MISO	MII1_RX_ER	I/O	J15	SPI1_D1

Note: SPI0 as boot device	
	SPI0 can be configured as boot device. An SPI NOR flash can be assembled on the carrier board.

3.2.4.15 UART

The AM335x provides five UART interfaces. UART0, UART3 and UART4 are routed to the TQMa335xL pads as primary functions. In the BSP provided by TQ-Systems GmbH UART4 is the serial console on the MBa335x.

3.2.4.16 UART0

The UART0 interface also provides handshake signals.

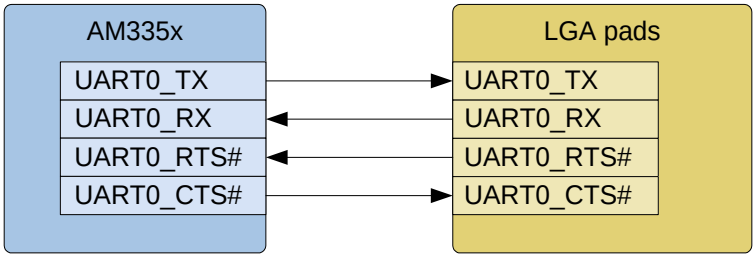

Illustration 6: Block diagram UART0 interface

The following table shows the signals used by the UART0 interface.

Table 27: UART0 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
M1	UART0_RXD	UART0_RXD	I/O	E15	–
L1	UART0_TXD	UART0_TXD	I/O	E16	–
K1	DCAN1_RX	UART0_RTS#	I/O	E17	Muxed as DCAN1_RX in TQ-BSP
J1	DCAN1_TX	UART0_CTS#	I/O	E18	Muxed as DCAN1_TX in TQ-BSP

UART0_CTS# and UART0_RTS# are only available if DCAN1 is not used.

3.2.4.17 UART3

The UART3 interface does not provide handshake signals. The UART3 signals are multiplexed with MMC0_CD# and MMC0_WP#.

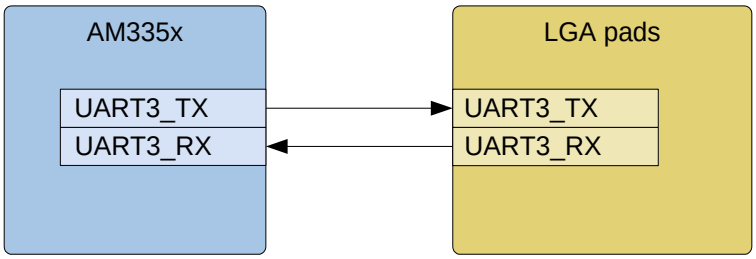

Illustration 7: Block diagram UART3 interface

The following table shows the signals used by the UART3 interface.

Table 28: UART3 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
K2	UART3_RXD	SPI0_CS1#	I/O	C15	MMC0_CD#
J2	UART3_TXD	ECAP0_IN_PWM0_OUT	I/O	C18	MMC0_WP#

3.2.4.18 UART4

The UART4 interface does not provide handshake signals.

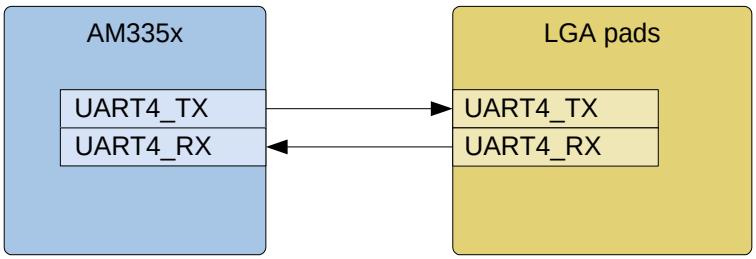

Illustration 8: Block diagram UART4 interface

The following table shows the signals used by the UART4 interface.

Table 29: UART4 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
P15	UART4_RXD	GPMC_WAIT0	I/O	T17
R15	UART4_TXD	GPMC_WP#	I/O	U17

3.2.4.19 USB

The AM335x provides two USB OTG cores with integrated High Speed PHYs.
All signals are routed to the TQMa335xL pads as primary functions.
The following table shows the signals used by the USB_H1 interface.

Table 30: USB_H1 signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
G16	USB0_CE	USB0_CE	A	M15
G17	USB0_DM	USB0_DM	A	N18
H17	USB0_DP	USB0_DP	A	N17
J16	USB0_DRVBUS	USB0_DRVBUS	I/O	F16
H16	USB0_ID	USB0_ID	A	P16
J17	USB0_VBUS	USB0_VBUS	A	P15
R16	USB1_CE	USB1_CE	A	P18
P17	USB1_DM	USB1_DM	A	R18
R17	USB1_DP	USB1_DP	A	R17
U16	USB1_DRVBUS	USB1_DRVBUS	I/O	F15
T16	USB1_ID	USB1_ID	A	P17
T17	USB1_VBUS	USB1_VBUS	A	T18

3.2.4.20 EXTINT#

The signal EXTINT# of the AM335x is routed to TQMa335xL pad A12.

Table 31: EXTINT# signal

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball	Remark
A12	EXTINT# (NMI#)	EXTINT#	I	B18	Routed to NMI# of AM335x

3.2.4.21 Clockout

The AM335x provides two Clockout signals, which are routed to the TQMa335xL pads.
The following table shows the signals used for Clockout.

Table 32: Clockout signals

TQMa335xL pad	Signal	Pad	Dir.	AM335x ball
D17	Clkout1	XDMA_EVENT_INTR0	I/O	A15
D15	TCLKIN / Clkout2	XDMA_EVENT_INTR1	I/O	D14

3.2.5 Reset

The TQMa335xL provides Reset inputs, and Reset outputs at the TQMa335xL pads.
The following block diagram shows the reset signals.

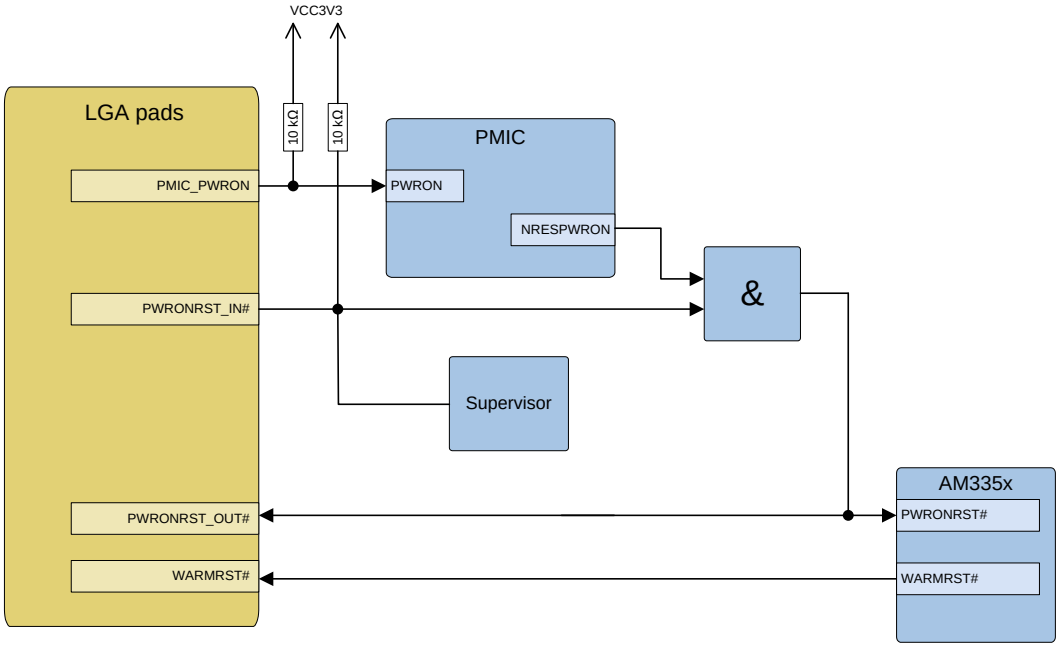

Illustration 9: Block diagram Reset

The following table describes the reset signals, which are routed to the TQMa335xL pads.

Table 33: Reset signals

TQMa335xL pad	Signal name	Dir.	Remark
D2	PWRONRST_IN#	I_{OD}	• Reset input PWRONRST (Power-On Reset) of the AM335x • Generates Cold-Reset at the AM335x • Connect to open-drain output only! • Low-active signal
E2	PWRONRST_OUT#	O	• Reset output RESETBMCU of the PMIC • Can be used to reset external periphery • Open drain, requires Pull-Up on carrier board (max. 3.3 V) • Low-active signal
D7	WARMRST#	O_{PU}	• Warm-Reset# of the AM335x • 10 kΩ PU to 3.3 V on the TQMa335xL • Low-active signal

The reset output of the supervisor used on the TQMa335xL can be connected to the POR_B input of the AM335x as a placement option.

3.2.6 WDOG

The AM335x provides a Watchdog Timer. If the Watchdog-Timer is active and not reset within the specified time, a reset is signalled to the PRCM. The PRCM then triggers a Warm-Reset.
More information can be found in the AM335x Reference Manual (3).

3.2.7 Power supply

3.2.7.1 Main power supply

The input voltage for the TQMa335xL is 3.3 V ±3 %. All I/O voltages have a fixed supply voltage of 3.3 V.

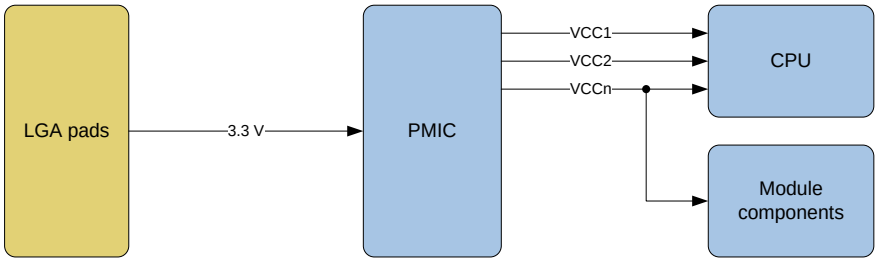

Illustration 10: Block diagram power supply

3.2.7.2 Overview TQMa335xL supply

The given current consumption has to be seen as an approximate value.

To estimate the power consumption of the system, the Texas Instruments Application Note AM335x Power Consumption Summary should be taken note of, as the current consumption of the TQMa335xL strongly depends on the application, the mode of operation and the operating system.

The following table shows some technical parameters of the TQMa335xL supply and power consumption.

Table 34: Parameter TQMa335xL supply

Parameter	Value typ.	Remark
Supply voltage V_{IN}	3.3 V	±3 % for TQMa335xL without extended voltage supervision
Supply voltage V_{IN}	3.3 V	±2 % for TQMa335xL with extended voltage supervision
Power consumption Linux (idle)	~ 1.2 W	AM335x 800 MHz / BSP without power management
Power consumption Linux (100 %)	~ 1.8 W	AM335x 800 MHz / BSP without power management
Power consumption standby	~ 210 mW	AM335x 800 MHz / BSP without power management

3.2.7.3 Adaptive Voltage Scaling (AVS)

The combination of AM335x and PMIC TPS65910A31 supports Adaptive Voltage Scaling (AVS) based on Smart Reflex.
The function is very limited due to several errata!

3.2.7.4 Voltage supervision

The TQMa335xL is available with several voltage supervision options.

On the primarily manufactured version of the TQMa335xL a MAX803 with a trigger level of 3.08 V monitors the supply voltage. Below 3.08 V a PORESET# is triggered at the AM335x.

On a second version of the TQMa335xL all voltages, except the DVS-capable voltages VDDS_MPU and VDDS_CORE are monitored. If one of these voltages falls below the permitted level a PORESET# is triggered at the AM335x.

On a third version of the TQMa335xL undervoltage and overvoltage of the supply voltages are monitored.
If one of these voltages fall below or exceed the permitted level a PORESET# is triggered at the AM335x.

3.2.7.5 TQMa335xL / carrier board Power-Up sequence

Since the AM335x is very sensitive to cross-supply it has to be ensured that the components on the carrier board are not supplied by the I/O-voltages (VDDSHV) during power-up.

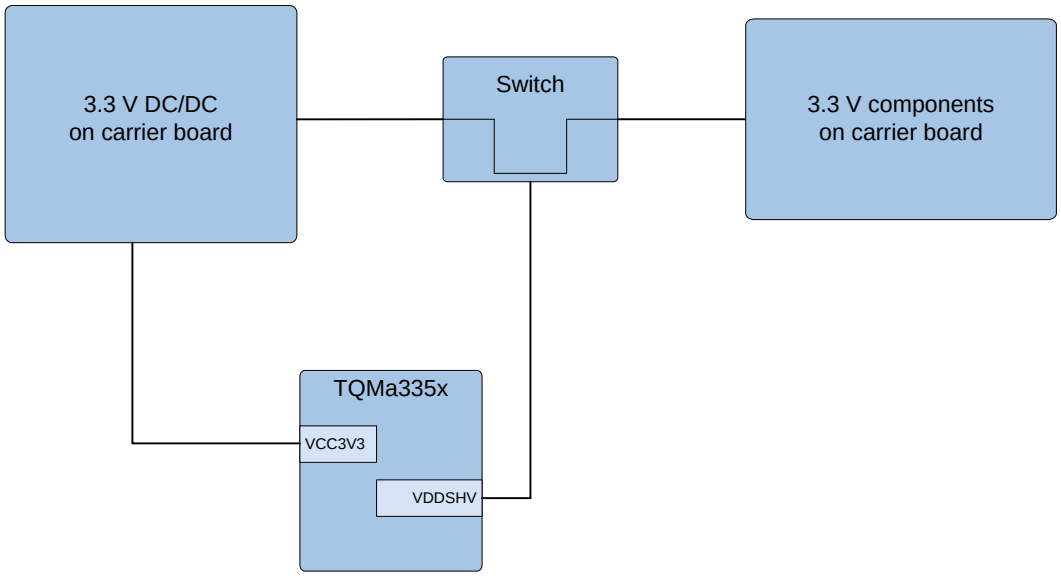

Illustration 11: Block diagram power supply carrier board

With the procedure described above it is certified that the pull-ups on the carrier board are already supplied with voltage when the boot-configuration pins are read.

Attention: Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the power-up sequence is indicated by a high level of signal VDDSHV.

3.2.8 Power-Modes

The following modes are supported by the hardware in combination of AM335x with PMIC, RTC and supply.

3.2.8.1 RTC backup

In this mode the controller is switched off. Only the RTC is buffered by the battery. Wakeup features are not available.

Table 35: PMIC RTC

RTC in PMIC	Remark
PMIC	Is in backup mode
BBCHEN=0	Battery charging has to be deactivated
Supply	VCC_MAIN <2.5 V; VBACKUP = 2.3 V to 3.0 V
VDDS_RTC	When supplied via LDO: Supply off
Current consumption	Approximately 20 µA

3.2.8.2 AM335x DEEP-SLEEP0-2, Standby

In this mode the following wakeup sources of the AM335x are supported.

- GPIO0
- Dmtimer1_1ms
- Both USB
- Touchscreen and ADC monitor functions
- UART0
- I2C0

Table 36: AM335x DEEP-SLEEP0-2, Standby

Conditions	Remark
PMIC	• Is in SLEEP MODE • Switch on voltages: (SLEEP_KEEP_LDO_ON, SLEEP_KEEP_RES_ON) • CLKOUT has to be activated (SLEEP_KEEP_RES:ON)
Supply	VCC_MAIN = 3.3 V
PMIC_POWER_EN	Connected with PWRHOLD
VDDS_RTC	Supplied by PMIC

3.2.8.3 AM335x Active Mode

The default mode of operation is the Active Mode.

Table 37: AM335x Active Mode

Conditions	Remark
PMIC	Is in Active Mode
Supply	VCC_MAIN = 3.3 V
PMIC_POWER_EN	Connected with PWRHOLD
VDDS_RTC	Supplied by PMIC

3.3 TQMa335xL interface

3.3.1 Pin assignment

The multiple pin configurations of all AM335x-internal function units must be taken note of.
The pin assignment shown in Table 38 refers to the corresponding BSP provided by TQ-Systems GmbH.
The electrical and pin characteristics are to be taken from the AM335x (1), (3) and PMIC Data Sheet (6).

3.3.2 Pinout TQMa335xL

The TQMa335xL has a total of 209 pads. The following table shows the pad-out as top view through the TQMa335xL.
(NC: the pad does not exist.)

Table 38: Pinout TQMa335xL, **top view through TQMa335xL**

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
17	NC	MCASP0_FSX	MCASP0_FSR	CLKOUT1	MMC0_DAT0	MMC0_CLK	USB0_DM	USB0_DP	USB0_VBUS	RGMII1_TD2	RGMII1_TD0	RGMII1_RD2	RGMII1_RD0	USB1_DM	USB1_DP	USB1_VBUS	NC
16	MCASP0_AXR0	MCASP0_AXR1	MCASP0_ACLKR	DGND	MMC0_DAT1	DGND	USB0_CE	USB0_ID	USB0_DRVVBUS	RGMII1_TD3	RGMII1_TD1	RGMII1_RD3	RGMII1_RD1	DGND	USB1_CE	USB1_ID	USB1_DRVVBUS
15	MCASP0_AXR2	MCASP0_AXR3	MCASP0_ACLKX	TCLKIN	MMC0_DAT2	MMC0_CMD	DGND	MDC	MDIO	RGMII1_TCLK	RGMII1_TCTL	RGMII1_RCLK	SPI1_CS0	UART4_RXD	UART4_TXD	RGMII2_RD1	RGMII2_RD0
14	VDDSHV	VDD-USB	DGND	DGND	MMC0_DAT3	SPI0_CS0	SPI0_SCLK	SPI0_D0_MISO	SPI0_D1_MOSI	DGND	RGMII1_RCTL	SPI1_D1	SPI1_D0	SPI1_SCLK	RGMII2_RTCL	RGMII2_RD3	RGMII2_RD2
13	PMIC_PWRON	PMIC_INT1	VDDS-CORE	VDDS-MPU	DGND	NC	DGND	NC	NC	NC	NC	NC	NC	RGMII2_RCLK	RGMII2_TCTL	RGMII2_TD1	RGMII2_TD0
12	EXTINT#	DGND	DGND	PMIC_SLEEP	NC	NC	NC	NC	NC	NC	NC	NC	NC	DGND	RGMII2_TCLK	RGMII2_TD3	RGMII2_TD2
11	VDD-PLL	DGND	DGND	DGND	NC	NC	NC	NC	NC	NC	NC	NC	NC	LCD_DATA23	LCD_DATA22	LCD_DATA21	LCD_DATA20
10	DGND	DGND	VDDS-RTC	VDDS	NC	NC	NC	NC	NC	NC	NC	NC	NC	LCD_DATA19	LCD_DATA18	LCD_DATA17	LCD_DATA16
9	VCC 3V3IN	VCC 3V3IN	VBACKUP_PMIC	VDDA-ADC	NC	NC	NC	NC	NC	NC	NC	NC	NC	LCD_DATA15	LCD_DATA14	LCD_DATA13	LCD_DATA12
8	VCC 3V3IN	VCC 3V3IN	DGND	DGND	NC	NC	NC	NC	NC	NC	NC	NC	NC	LCD_DATA11	LCD_DATA10	LCD_DATA9	LCD_DATA8
7	VCC 3V3IN	VCC 3V3IN	VDDS-DDR	WARM RST#	NC	NC	NC	NC	NC	NC	NC	NC	DGND	LCD_DATA7	LCD_DATA6	LCD_DATA5	LCD_DATA4
6	DGND	DGND	EXT_WAKEUP	DGND	NC	NC	NC	NC	NC	NC	NC	NC	NC	LCD_DATA3	LCD_DATA2	LCD_DATA1	LCD_DATA0
5	AIN6	AIN7	DGND	TCK	DGND	NC	NC	NC	NC	NC	NC	NC	DGND	LCD_HSYNC	LCD_M_CLK	LCD_AS_BIAS_EN	LCD_PCLK
4	AIN4	AIN5	TDI	TDO	EMU0	DDR_A0	DDR_DQS#0	DDR_DQS0	DGND	DDR_DQ15	MMC1_DAT2	MMC1_DAT5	DGND	LCD_VSYNC	DGND	DGND	DGND
3	AIN2	AIN3	TMS	TRST#	EMU1	DDR_CK#	DDR_CK	DDR_DQ7	DDR_DQS1	DDR_DQS#1	MMC1_DAT1	MMC1_DAT4	MMC1_DATA7	MMC1_CLK	MMC1_CMD	TIMER7	TIMER6
2	AIN0	AIN1	DGND	PWRONRST_IN#	PWRONRST_OUT#	DGND	DGND	DGND	UART3_TXD	UART3_RXD	MMC1_DAT0	MMC1_DAT3	MMC1_DATA6	DGND	DGND	TIMER5	TIMER4
1	NC	DGND	I2C0_SCL	I2C0_SDA	I2C1_SDA	I2C1_SCL	DCAN0_TX	DCAN0_RX	DCAN1_TX	DCAN1_RX	UART0_TXD	UART0_RXD	DGND	GPIO1_28	GPIO1_29	GPIO2_0	NC

3.3.2 Pinout TQMa335xL (continued)

Table 39: TQMa335xL pad description

TQMa335xL ball	Signal	Pad name	I/O	AM335x ball
A10	DGND	–	P	–
A11	VDD-PLL_TEST	Test voltage	O	–
A12	EXTINT# (NMI#)	EXTINT#	I	B18
A13	PMIC_PWRON	TPS65910A31 Pin PWRON	I	–
A14	VDDSHV	Test voltage	O	–
A15	MCASP0_AXR2	MCASP0_AXR2	I/O	C12
A16	MCASP0_AXR0	MCASP0_AXR0	I/O	D12
A2	AIN0	AIN0	A	B6
A3	AIN2	AIN2	A	B7
A4	AIN4	AIN4	A	C8
A5	AIN6	AIN6	A	A8
A6	DGND	–	P	–
A7	VCC3V3	–	P	–
A8	VCC3V3	–	P	–
A9	VCC3V3	–	P	–
B1	DGND	–	P	–
B10	DGND	–	P	–
B11	DGND	–	P	–
B12	DGND	–	P	–
B13	PMIC_INT1	TPS65910A31 Pin INT1	O	–
B14	VDD-USB_TEST	Test voltage	O	–
B15	MCASP0_AXR3	MCASP0_AXR3	I/O	A14
B16	MCASP0_AXR1	MCASP0_AXR1	I/O	D13
B17	MCASP0_FSX	MCASP0_FSX	I/O	B13
B2	AIN1	AIN1	A	C7
B3	AIN3	AIN3	A	A7
B4	AIN5	AIN5	A	B8
B5	AIN7	AIN7	A	C9
B6	DGND	–	P	–
B7	VCC3V3	–	P	–
B8	VCC3V3	–	P	–
B9	VCC3V3	–	P	–
C1	I2C0_SCL	I2C0_SCL	I/O	C16
C10	VDDS-RTC_TEST	Test voltage	O	–
C11	DGND	–	P	–
C12	DGND	–	P	–
C13	VDDS-CORE_TEST	Test voltage	O	–
C14	DGND	–	P	–
C15	MCASP0 ACLKX	MCASP0 ACLKX	I/O	A13
C16	MCASP0 ACLKR	MCASP0 ACLKR	I/O	B12
C17	MCASP0_FSR	MCASP0_FSR	I/O	C13
C2	DGND	–	P	–
C3	TMS	TMS	I	C11
C4	TDI	TDI	I	B11
C5	DGND	–	P	–
C6	EXT_WAKEUP	EXT_WAKEUP	I	C5
C7	VDDS-DDR_TEST	Test voltage	O	–
C8	DGND	–	P	–
C9	VBACKUP_PMIC	Backup Voltage for PMIC	P	–

3.3.2 Pinout TQMa335xL (continued)

Table 39: TQMa335xL pad description (continued)

TQMa335xL ball	Signal	Pad name	I/O	AM335x ball
D1	I2C0_SDA	I2C0_SDA	I/O	C17
D10	VDDS_TEST	Test voltage	O	–
D11	DGND	–	P	–
D12	PMIC_SLEEP	TPS65910A31 Pin SLEEP	I	–
D13	VDDS-MPU_TEST	Test voltage	O	–
D14	DGND	–	P	–
D15	TCLKIN	XDMA_EVENT_INTR1	I/O	D14
D16	DGND	–	P	–
D17	CLKOUT1	XDMA_EVENT_INTR0	I/O	A15
D2	PWRONRST_IN#	PWRONRST# Input to Modul	I	–
D3	TRST#	TRST#	I	B10
D4	TDO	TDO	O	A11
D5	TCK	TCK	I	A12
D6	DGND	–	P	–
D7	WARMRST#	WARMRST#	I/O	A10
D8	DGND	–	P	–
D9	VDDA-ADC_TEST	Test voltage	O	–
E1	I2C1_SDA	UART1_RXD	I/O	D16
E13	DGND	–	–	–
E14	MMC0_DAT3	MMC0_DAT3	I/O	F17
E15	MMC0_DAT2	MMC0_DAT2	I/O	F18
E16	MMC0_DAT1	MMC0_DAT1	I/O	G15
E17	MMC0_DAT0	MMC0_DAT0	I/O	G16
E2	PWRONRST_OUT#	PWRONRST# Output from Modul	O	–
E3	EMU1	EMU1	IO	B14
E4	EMU0	EMU0	IO	C14
E5	DGND	–	P	–
F1	I2C1_SCL	UART1_TXD	I/O	D15
F14	SPI0_CS0	SPI0_CS0	I/O	A16
F15	MMC0_CMD	MMC0_CMD	I/O	G18
F16	DGND	–	P	–
F17	MMC0_CLK	MMC0_CLK	I/O	G17
F2	DGND	–	P	–
F3	DDR_CK#	Test-Pin do not connect on Mainboard	–	–
F4	DDR_A0	Test-Pin do not connect on Mainboard	–	–
G1	DCAN0_TX	UART1_CTS#	I/O	D18
G13	DGND	–	P	–
G14	SPI0_SCLK	SPI0_SCLK	I/O	A17
G15	DGND	–	P	–
G16	USB0_CE	USB0_CE	A	M15
G17	USB0_DM	USB0_DM	A	N18
G2	DGND	–	P	–
G3	DDR_CK	Test-Pin do not connect on Mainboard	–	–
G4	DDR_DQS0	Test-Pin do not connect on Mainboard	–	–
H1	DCAN0_RX	UART1_RTS#	I/O	D17
H14	SPI0_D0	SPI0_D0	I/O	B17
H15	MDC	MDC	I/O	M18
H16	USB0_ID	USB0_ID	A	P16
H17	USB0_DP	USB0_DP	A	N17
H2	–	–	P	–
H3	DDR_DQ_7	Test-Pin do not connect on Mainboard	–	–
H4	DDR_DQS0#	Test-Pin do not connect on Mainboard	–	–

3.3.2 Pinout TQMa335xL (continued)

Table 39: TQMa335xL pad description (continued)

TQMa335xL ball	Signal	Pad name	I/O	AM335x ball
J1	DCAN1_TX	UART0_CTS#	I/O	E18
J14	SPI0_D1	SPI0_D1	I/O	B16
J15	MDIO	MDIO	I/O	M17
J16	USB0_DRVBUS	USB0_DRVBUS	IO	F16
J17	USB0_VBUS	USB0_VBUS	A	P15
J2	UART3_TXD	ECAP0_IN_PWM0_OUT	I/O	C18
J3	DDR_DQS1#	Test-Pin do not connect on Mainboard	–	–
J4	DGND	–	P	–
K1	DCAN1_RX	UART0_RTS#	I/O	E17
K14	DGND	–	P	–
K15	RGMII1_TCLK	MMI1_TX_CLK	I/O	K18
K16	RGMII1_TD3	MMI1_TXD3	I/O	J18
K17	RGMII1_TD2	MMI1_TXD2	I/O	K15
K2	UART3_RXD	SPI0_CS1	I/O	C15
K3	DDR_DQS1	Test-Pin do not connect on Mainboard	–	–
K4	DDR_DQ15	Test-Pin do not connect on Mainboard	–	–
L1	UART0_TXD	UART0_TXD	I/O	E16
L15	RGMII1_TCTL	MMI1_TX_EN	I/O	J16
L16	RGMII1_TD1	MMI1_TXD1	I/O	K16
L17	RGMII1_TD0	MMI1_TXD0	I/O	K17
L2	MMC1_DAT0	GPMC_AD0	I/O	U7
L3	MMC1_DAT1	GPMC_AD1	I/O	V7
L4	MMC1_DAT2	GPMC_AD2	I/O	R8
M1	UART0_RXD	UART0_RXD	I/O	E15
M14	SPI1_D1	MII1_RX_ER	I/O	J15
M15	RGMII1_RCLK	MMI1_RX_CLK	I/O	L18
M16	RGMII1_RD3	MMI1_RXD3	I/O	L17
M17	RGMII1_RD2	MMI1_RXD2	I/O	L16
M2	MMC1_DAT3	GPMC_AD3	I/O	T8
M3	MMC1_DAT4	GPMC_AD4	I/O	U8
M4	MMC1_DAT5	GPMC_AD5	I/O	V8
N1	DGND	–	P	–
N14	SPI1_D0	MII1_CRS	I/O	H17
N15	SPI1_CS0	RMII1_REF_CLK	I/O	H18
N16	RGMII1_RD1	MMI1_RXD1	I/O	L15
N17	RGMII1_RD0	MMI1_RXD0	I/O	M16
N2	MMC1_DAT6	GPMC_AD6	I/O	R9
N3	MMC1_DAT7	GPMC_AD7	I/O	T9
N4	DGND	–	P	–
N5	DGND	–	P	–
N7	DGND	–	P	–
P1	GPIO1_28	GPMC_BE#1	I/O	U18
P10	LCD_DATA19	GPMC_AD12	I/O	T12
P11	LCD_DATA23	GPMC_AD8	I/O	U10
P12	DGND	–	P	–
P13	RGMII2_RCLK	GPMC_A7	I/O	T15
P14	SPI1_SCLK	MII1_COL	I/O	H16
P15	UART4_RXD	GPMC_WAIT0	I/O	T17
P16	DGND	–	P	–
P17	USB1_DM	USB1_DM	A	R18
P2	DGND	–	P	–
P3	MMC1_CLK	GPMC_CS#1	I/O	U9

3.3.2 Pinout TQMa335xL (continued)

Table 39: TQMa335xL pad description (continued)

TQMa335xL ball	Signal	Pad name	I/O	AM335x ball
P4	LCD_VSYNC	LCD_VSYNC	I/O	U5
P5	LCD_HSYNC	LCD_HSYNC	I/O	R5
P6	LCD_DATA3	LCD_DATA3	I/O	R4
P7	LCD_DATA7	LCD_DATA7	I/O	T4
P8	LCD_DATA11	LCD_DATA11	I/O	U4
P9	LCD_DATA15	LCD_DATA15	I/O	T5
R1	GPIO1_29	GPMC_CS#0	I/O	V6
R10	LCD_DATA18	GPMC_AD13	I/O	R12
R11	LCD_DATA22	GPMC_AD9	I/O	T10
R12	RGMII2_TCLK	GPMC_A6	I/O	U15
R13	RGMII2_TCTL	GPMC_A0	I/O	R13
R14	RGMII1_RCTL	MMI1_RX_DV	I/O	J17
R14	RGMII2_RCTL	GPMC_A1	I/O	V14
R15	UART4_TXD	GPMC_WP#	I/O	U17
R16	USB1_CE	USB1_CE	A	P18
R17	USB1_DP	USB1_DP	A	R17
R2	DGND	–	P	–
R3	MMC1_CMD	GPMC_CS#2	I/O	V9
R4	DGND	–	P	–
R5	LCD_MCLK	GPMC_CLK	I/O	V12
R6	LCD_DATA2	LCD_DATA2	I/O	R3
R7	LCD_DATA6	LCD_DATA6	I/O	T3
R8	LCD_DATA10	LCD_DATA10	I/O	U3
R9	LCD_DATA14	LCD_DATA14	I/O	V4
T1	GPIO2_0	GPMC_CS#3	I/O	T13
T10	LCD_DATA17	GPMC_AD14	I/O	V13
T11	LCD_DATA21	GPMC_AD10	I/O	T11
T12	RGMII2_TD3	GPMC_A2	I/O	U14
T13	RGMII2_TD1	GPMC_A4	I/O	R14
T14	RGMII2_RD3	GPMC_A8	I/O	V16
T15	RGMII2_RD1	GPMC_A10	I/O	T16
T16	USB1_ID	USB1_ID	A	P17
T17	USB1_VBUS	USB1_VBUS	A	T18
T2	TIMER5	GPMC_BE#0_CLE	I/O	T6
T3	TIMER7	GPMC_OE#_RE#	I/O	T7
T4	DGND	–	P	–
T5	LCD_AC_BIAS_EN	LCD_AC_BIAS_EN	I/O	R6
T6	LCD_DATA1	LCD_DATA1	I/O	R2
T7	LCD_DATA5	LCD_DATA5	I/O	T2
T8	LCD_DATA9	LCD_DATA9	I/O	U2
T9	LCD_DATA13	LCD_DATA13	I/O	V3
U10	LCD_DATA16	GPMC_AD15	I/O	U13
U11	LCD_DATA20	GPMC_AD11	I/O	U12
U12	RGMII2_TD2	GPMC_A3	I/O	T14
U13	RGMII2_TD0	GPMC_A5	I/O	V15
U14	RGMII2_RD2	GPMC_A9	I/O	U16
U15	RGMII2_RD0	GPMC_A11	I/O	V17
U16	USB1_DRVBUS	USB1_DRVBUS	IO	F15
U2	TIMER4	GPMC_ADV#_ALE	I/O	R7
U3	TIMER6	GPMC_WE#	I/O	U6
U4	DGND	–	P	–
U5	LCD_PCLK	LCD_PCLK	I/O	V5
U6	LCD_DATA0	LCD_DATA0	I/O	R1
U7	LCD_DATA4	LCD_DATA4	I/O	T1
U8	LCD_DATA8	LCD_DATA8	I/O	U1
U9	LCD_DATA12	LCD_DATA12	I/O	V2

4. SOFTWARE

The TQMa335xL comes with a preinstalled boot loader U-Boot and a BSP tailored for the MBa335x.
More information can be found in the Support Wiki for the TQMa335x.

5. MECHANICS

5.1 TQMa335xL dimensions and footprint

The overall dimensions (length × width) of the TQMa335xL are 38 × 38 mm².
The maximum height of the TQMa335xL above the carrier board is approximately 3.3 mm.

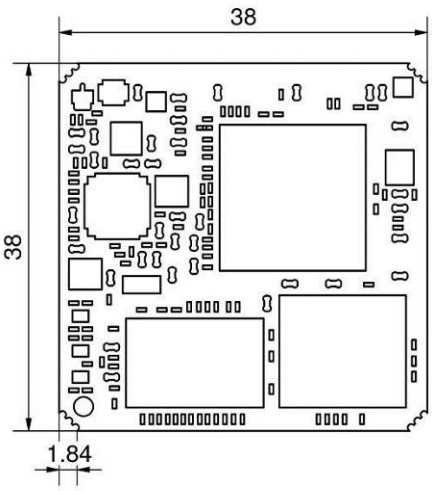

Illustration 12: TQMa335xL dimensions (1)

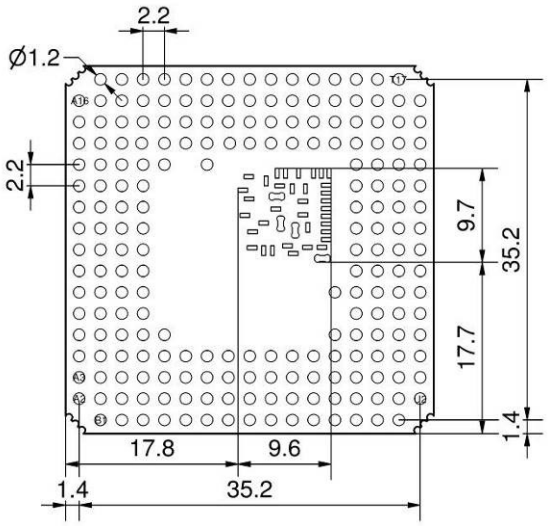

Illustration 13: TQMa335xL dimensions (2)
Top view through TQMa335xL

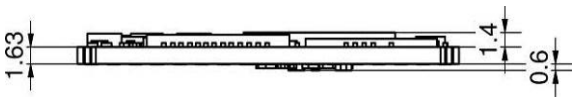

Illustration 14: TQMa335xL side view

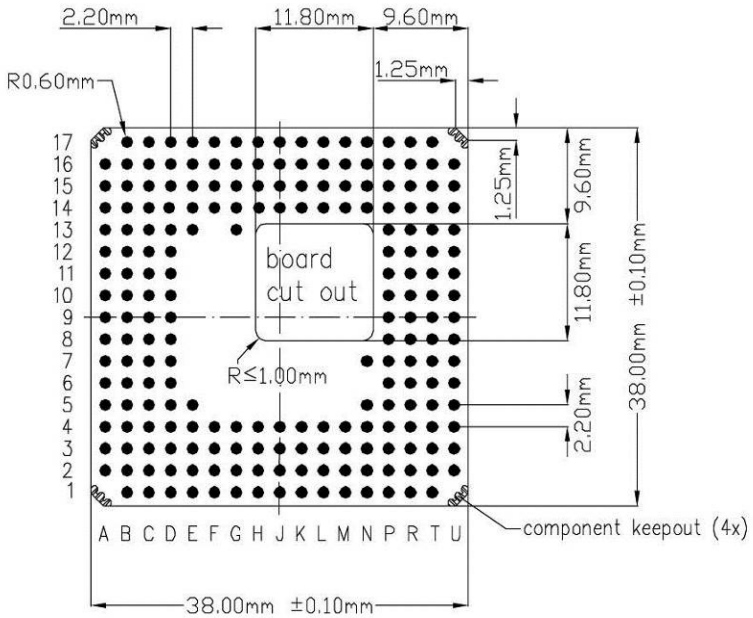

Illustration 15: Recommended PCB land pattern for TQMa335xL, t**op view through TQMa335xL**

5.2 TQMa335xL 3D views

Illustration 16: TQMa335xL top view (3D)

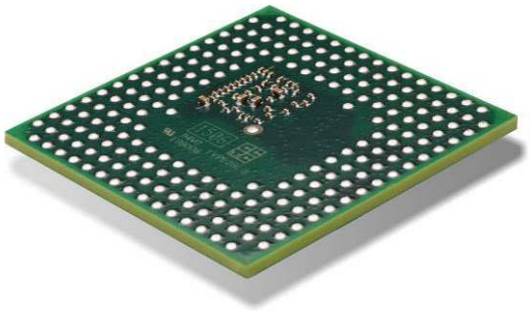

Illustration 17: TQMa335xL bottom view (3D)

5.3 TQMa335xL component placement

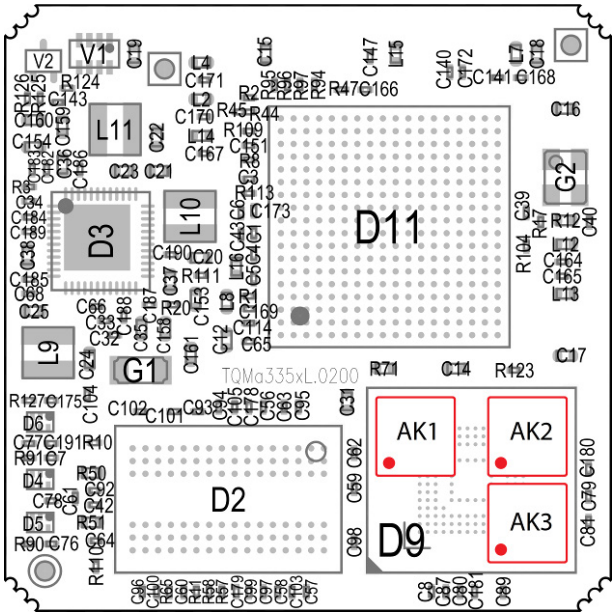

Illustration 18: TQMa335xL component placement top

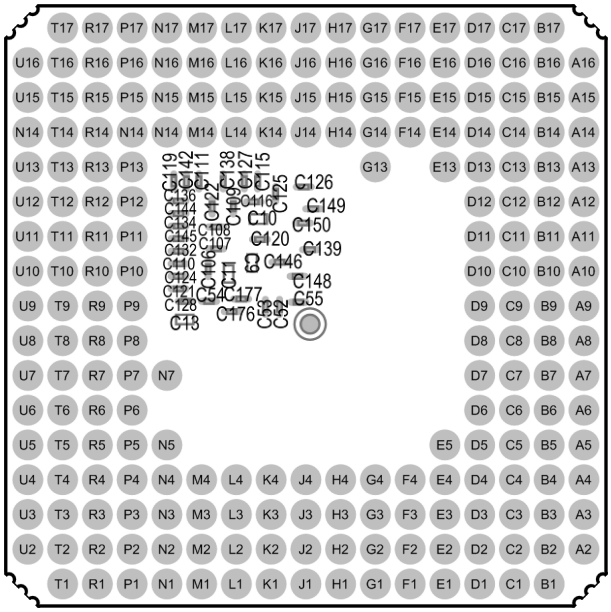

Illustration 19: TQMa335xL component placement bottom

The labels on the TQMa335xL show the following information:

Table 40: Labels on TQMa335xL

Label	Text
AK1	TQMa335xL 2D serial number
AK2	TQMa335xL version and revision
AK3	TQMa335xL tests performed

5.4 Protection against external effects

As an embedded module the TQMa335xL is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

To cool the TQMa335xL, a maximum of 2 W have to be dissipated.
The power dissipation originates primarily in the AM335x and the DDR3L SDRAM.
The power dissipation mainly depends on the software used and can vary according to the application.
It is the customer's responsibility to define a suitable cooling method for his use case.
In most cases passive cooling should be sufficient.
For further information see Texas Instruments Application Notes (4), (5).

Attention: Destruction or malfunction, TQMa335xL cooling	
	The AM335x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM335x must be taken into consideration when connecting the heat sink, see (5). The AM335x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa335xL and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMa335xL has to be soldered on the carrier board. Please contact TQ-Support for soldering instructions (10).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa335xL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding besides, take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.
As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa335xL.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤3.3 V DC), tests with respect to the operational and personal safety haven't been carried out.

6.4 Climatic and operational conditions

The temperature range, in which the TQMa335xL works reliably, strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 41: Climate and operational conditions extended temperature range –25 °C to +85 °C

Parameter	Range	Remark
Chip temperature AM335x	–40 °C to +95 °C	Tj = +105 °C
Environmental temperature AM335x	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	Tj = +150 °C
Environmental temperature PMIC	–40 °C to +85 °C	–
Case temperature DDR3L SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–25 °C to +85 °C	–
Permitted storage temperature TQMa335xL	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 42: Climate and operational conditions industrial temperature range –40 °C to +85 °C

Parameter	Range	Remark
Chip temperature AM335x	–40 °C to +95 °C	Tj = +105 °C
Environmental temperature AM335x	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	Tj = +150 °C
Environmental temperature PMIC	–40 °C to +85 °C	–
Case temperature DDR3L SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Permitted storage temperature TQMa335xL	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the thermal characteristics of the AM335x is to be taken from the Texas Instruments Data Sheets (1), (3), and (5).

6.5 Reliability and service life

No detailed MTBF calculation has been done for the TQMa335xL.

Detailed information concerning the service life of the AM335x under different operational conditions is to be taken from the Texas Instruments Data Sheets (1), (3), and (5).

6.6 Environment protection

6.6.1 RoHS

The TQMa335xL is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

6.6.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa335xL was designed to be recyclable and easy to repair.

6.7 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

6.8 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa335xL must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMa335xL enable compliance with EuP requirements for the TQMa335xL.

6.9 Battery

No batteries are used on the TQMa335xL.

6.10 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa335xL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa335xL is delivered in reusable packaging.

6.11 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

7. APPENDIX

7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 43: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AIN	Analog In
ARM®	Advanced RISC Machine
AVS	Adaptive Voltage Scaling
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
DC	Direct Current
DDR3L	Double Data Rate Type three Low voltage
DIN	Deutsche Industrie Norm
DVS	Dynamic Voltage Scaling
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multi-Media Card
EN	Europäische Norm
ESD	Electro-Static Discharge
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input/Output
GPMC	General Purpose Memory Controller
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IP	Ingress Protection
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MCSPI	Multichannel Serial Port Interface
MD	Management Data
MII	Media-Independent Interface
MMC	Multi-Media Card
MTBF	Mean operating Time Between Failures

7.1 Acronyms and definitions (continued)

Table 43: Acronyms (continued)

Acronym	Meaning
n.a.	Not Available
NC	Not Connected
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRCM	Power and Clock Management
PU	Pull-Up
PWM	Pulse-Width Modulation
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection
WXGA	Wide Extended Graphics Array

7.2 References

Table 44: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	Sitara™ AM335x ARM® Cortex®-A8 Microprocessors (MPUs) Data Sheet	G / June 2014	Texas Instruments
(2)	Pinmux Utility for ARM® MPU Processors	Feb. 2013	Texas Instruments
(3)	AM335x ARM® Cortex®-A8 Microprocessors Technical Reference Manual	K / June 2014	Texas Instruments
(4)	AM335x Power Consumption Summary	May 2013	Texas Instruments
(5)	AM335x Thermal Considerations	Apr. 2013	Texas Instruments
(6)	TPS65910Ax PMIC	October 2014	Texas Instruments
(7)	Sitara™ AM335x ARM® Cortex®-A8 Silicon Errata	E / Apr. 2013	Texas Instruments
(8)	MBa335x User's Manual	– current –	TQ-Systems
(9)	Support-Wiki for the TQMa335x	– current –	TQ-Systems
(10)	Processing instructions for TQMa335xL	– current –	TQ-Systems

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