TQMa28L
User's Manual

TQMa28L UM 0104
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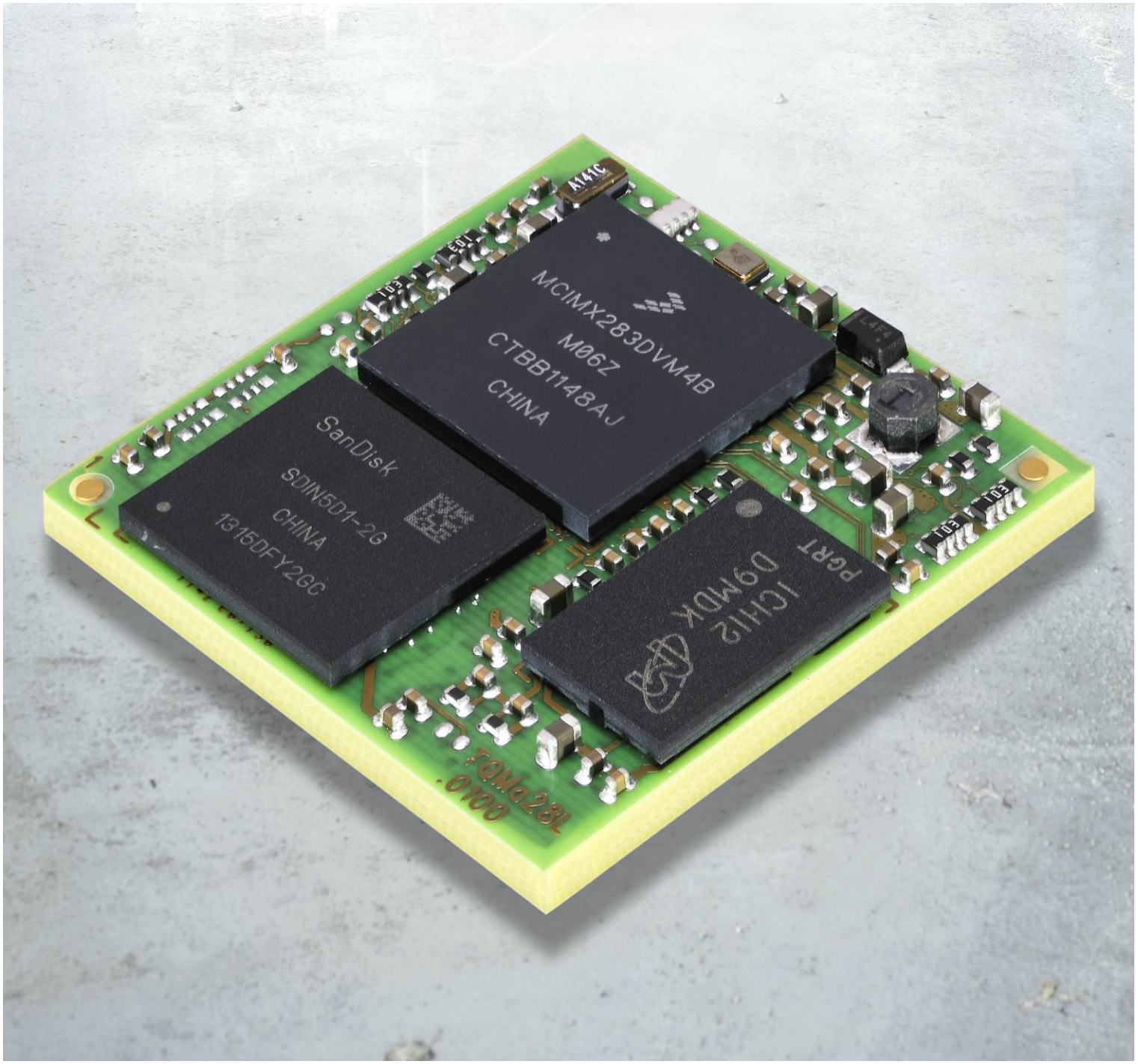

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the module and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa28 circuit diagram
- MBa28 User's Manual
- MCIMX28RM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqma28

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa28L revision 01xx.

This User's Manual does not replace the Reference Manual of the CPU.

The TQMa28L is a universal Minimodule based on the NXP ARM-CPU i.MX283 or i.MX287.

The ARM926EJ-S core works with up to 454 MHz. The TQMa28L extends the TQ-Systems GmbH product range and provides a well-balanced ratio between computing performance and graphics power.

The TQMa28L provides the following key functions and characteristics:

- NXP i.MX28 (ARM9 architecture), 454 MHz
- All functional CPU signals are routed to TQMa28L's contacts
- Up to 16 Gbyte eMMC NAND flash
- Up to 256 Mbyte DDR2 SDRAM
- Up to eight 12 bit A/D converter
- PWM
- Various serial interfaces depending on multiplexing (UART, SPI, I^2C, I^2S)
- 2 × CAN (i.MX287), 1 × CAN (i.MX283)
- 2 × USB 2.0 Hi-Speed Host interface with integrated PHY
- Industrial temperature range on request
- Low power consumption (depending on mode of operation)
- Dimensions: 30.6 × 30.6 mm^2
- Long term available
- Power supply: 5 V, or 3.3 V

All interfaces supported by software are described in the Support-Wiki.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 TQMa28L block diagram

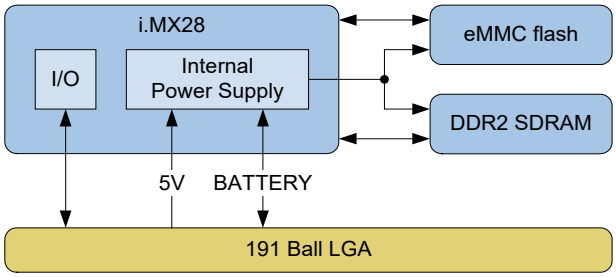

Illustration 1: TQMa28L, block diagram

3.1.2 System functionality

The following elements are implemented on the TQMa28L:

- i.MX283 or i.MX287 CPU
- DDR2 SDRAM
- eMMC NAND flash

Interfaces:

- 191 contacts, pre-tinned Land Grid Array (LGA)

A detailed overview of all available user's interfaces can be found in section 4.1.

4. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa28L, and the BSP provided by TQ-Systems GmbH. See also section (5).

4.1 Interfaces to other systems and devices

The name of the TQMa28L version depends on the assembled CPU:

Table 2: TQMa28L versions

TQMa28L version	Processor
TQMa28L-AA	MCIMX287CVM4B
TQMa28L-AB	MCIMX283CVM4B

4.1.1 TQMa28L connection

The TQMa28L has to be soldered onto the carrier board.
It is not possible to remove the TQMa28L from the carrier board without damaging it.

4.1.2 TQMa28L pinout

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The TQMa28L pin assignments described in the following tables refer to the corresponding BSP provided by TQ-Systems GmbH. The electric or pin characteristics are to be taken from the data sheet of the CPU (2).
In addition to direction, contact name and contact number, external and internal pull-up or-down resistors and other wiring, as well as the references to I/O voltage and processor signal characteristics are listed.

4.1.2.1 TQMa28L-AA pinout

Table 3: TQMa28L-AA pinout, top view **through** TQMa28L-AA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	GND	LCD_D18 U4	LCD_D12 T1	LCD_D06 N2	LCD_D00 K2	LCD_WR_RW# K1	ENET1_RXD1 J2	ENET1_TXD1 G2	ENET0_RXD1 H2	ENET0_TXD1 F2	GND	1588_EVENT2_OUT B1	NC
B	SD_DATA3 A5	NC	LCD_D19 T4	LCD_D13 T2	LCD_D07 P1	LCD_D01 K3	LCD_DOTCLK N1	ENET1_RXD0 J1	ENET1_TXD0 G1	ENET0_RXD0 H1	ENET0_TXD0 F1	1588_EVENT3_OUT D1	1588_EVENT2_IN C1	DUART_RX K7
C	SD_DATA2 D6	SD_DATA4 B5	LCD_D20 R4	LCD_D14 U2	LCD_D08 P2	LCD_D02 L2	GND	ENET1_RX_EN J3	ENET1_TX_EN J4	ENET0_RX_EN E4	ENET0_TX_EN F4	1588_EVENT3_IN E1	ENET_RESET# F3	DUART_TX L7
D	SD_DATA1 C6	SD_DATA6 D5	LCD_D21 U5	LCD_D15 U3	LCD_D09 P3	LCD_D03 L3	LCD_VSYNC L1	ENET_MDIO H4	ENET_MDC G4	GND	ENET_CLK E2	GND	ENET_INT# E3	USB_1_OC# D3
E	SD_DATA0 B6	SD_DATA5 C5	LCD_D22 T5	LCD_D16 T3	LCD_D10 R1	LCD_D04 M2	LCD_HSYNC M1	GPIO0_20 N6	SAIF0_LRCLK G6	SAIF0_MCLK G7	SAIF0_BITCLK F7	LRADC2 C8	USB_1_DP A8	USB_0_OC# D4
F	SD_CMD A4	SD_DATA7 B4	LCD_D23 R5	LCD_D17 R3	LCD_D11 R2	LCD_D05 M3	GND	DNC (EMMC_CLK) P8	SPDIF D7	GND	LRADC1 C9	LRADC3 D9	USB_1_DM B8	USB_0_DP B10
G	SD_CLK A6	GND	LCD_C5 P5	LCD_RD_E P4	LCD_RS M4	LCD_ENABLE N5	LCD_BL_PWM K8	GPIO0_16 N7	SAIF0_SDATA0 E7	GND	LRADC0 C15	DNC (VCC1V8)	GND	USB_0_DM A10
H	SD_DETECT# D10	DNC (EMMC_DATA2) R8	DNC (EMMC_DATA5) R7	GPIO0_24 R6	LCD_RESET M6	GND	GPIO0_27 P7	GPIO0_26 P6	SAIF1_SDATA0 E8	GND	LRADC4 D13	HSADC0 B14	GND	USB_0_ID J5
J	SD_WP L9	DNC (EMMC_DATA1) T8	DNC (EMMC_DATA4) T7	DNC (EMMC_DATA7) T6	GND	I2C1_SDA H7	GPIO0_17 N9	GND	SSP2_MOSI C3	SSP2_SCK A3	LRADC5 D15	LRADC6 C14	USB_1_PWR_EN F6	GND
K	CAN1_TX M7	DNC (EMMC_DATA0) U8	DNC (EMMC_DATA3) U7	DNC (EMMC_DATA6) U6	AUART4_RX C2	I2C1_SCL H6	DNC (EMMC_CMD) N8	GND	SSP2_SS0# C4	SSP2_MISO B3	DNC (VCC1V2)	DNC (VCC3V3)	USB_0_PWR_EN F5	DNC (VCC4V2)
L	CAN1_RX M9	AUART3_RX M5	AUART0_RX G5	GND	AUART4_TX A2	I2C0_SDA D8	GPIO3_6 K5	GND	DEBUG B9	JTAG_TRST# D14	GND	GND	GND	BATTERY
M	CAN0_TX M8	AUART3_TX L5	AUART0_TX H5	AUART0_CTS# J6	AUART4_CTS# D2	I2C0_SCL C7	DNC (EMI_D03) N14	DNC (EMI_D11) J14	RESET# A14	JTAG_TMS D12	PWM3 E9	PSWITCH A11	PWM4 E10	BATTERY
N	CAN0_RX L8	AUART3_CTS# L6	GND	AUART0_RTS# J7	AUART4_RTS# B2	DNC (EMI_CLK#) L16	GND	GND	DNC (EMI_DQS1) J17	JTAG_TCK E11	GND	VCC5V	VCC5V	VCC5V
P	NC	AUART3_RTS# K6	AUART1_TX K4	AUART1_RX L4	DNC (EMI_A00) U15	DNC (EMI_CLK) L17	DNC (EMI_DQS0) K17	DNC (EMI_DQS0#) K16	DNC (EMI_DQS1#) J16	GND	JTAG_RTCK E14	JTAG_TDO E13	JTAG_TDI E12	NC

4.1.2.2 TQMa28L-AB pinout

Table 4: TQMa28L-AB pinout, top view **through** TQMa28L-AB

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	GND	LCD_D18 U4	LCD_D12 T1	LCD_D06 N2	LCD_D00 K2	LCD_WR_RW# K1	NC	NC	ENET0_RXD1 H2	ENET0_TXD1 F2	GND	NC	NC
B	SD_DATA3 A5	NC	LCD_D19 T4	LCD_D13 T2	LCD_D07 P1	LCD_D01 K3	NC	NC	NC	ENET0_RXD0 H1	ENET0_TXD0 F1	NC	NC	DUART_RX K7
C	SD_DATA2 D6	SSP2_MISO B5	LCD_D20 R4	LCD_D14 U2	LCD_D08 P2	LCD_D02 L2	GND	NC	NC	ENET0_RX_EN E4	ENET0_TX_EN F4	NC	NC	DUART_TX L7
D	SD_DATA1 C6	SSP2_MOSI D5	LCD_D21 U5	LCD_D15 U3	LCD_D09 P3	LCD_D03 L3	NC	ENET_MDIO H4	ENET_MDC G4	GND	ENET_CLK E2	GND	NC	USB_1_OC# D3
E	SD_DATA0 B6	SSP2_SS0 C5	LCD_D22 T5	LCD_D16 T3	LCD_D10 R1	LCD_D04 M2	NC	GPIO0_20 N6	AUART4_RTS# G6	AUART4_CTS# G7	AUART4_RX F7	LRADC2 C8	USB_1_DP A8	USB_0_OC# D4
F	SD_CMD A4	SSP2_SCK B4	LCD_D23 R5	LCD_D17 R3	LCD_D11 R2	LCD_D05 M3	GND	DNC (EMMC_CLK) P8	NC	GND	LRADC1 C9	LRADC3 D9	USB_1_DM B8	USB_0_DP B10
G	SD_CLK A6	GND	LCD_CS P5	LCD_RD_E P4	LCD_RS M4	NC	USB_0_ID K8	GPIO0_16 N7	AUART4_TX E7	GND	LRADC0 C15	DNC (VCC1V8)	GND	USB_0_DM A10
H	SD_DETECT# D10	DNC (EMMC_DATA2) R8	DNC (EMMC_DATA5) R7	GPIO0_24 R6	LCD_RESET M6	GND	GPIO0_27 P7	GPIO0_26 P6	GPIO3_26 E8	GND	LRADC4 D13	HSADC0 B14	GND	NC
J	SD_WP L9	DNC (EMMC_DATA1) T8	DNC (EMMC_DATA4) T7	DNC (EMMC_DATA7) T6	GND	NC	GPIO0_17 N9	GND	AUART2_TX C3	AUART2_RX A3	LRADC5 D15	LRADC6 C14	NC	GND
K	NC	DNC (EMMC_DATA0) U8	DNC (EMMC_DATA3) U7	DNC (EMMC_DATA6) U6	NC	NC	DNC (EMMC_CMD) N8	GND	AUART3_TX C4	AUART3_RX B3	DNC (VCC1V2)	DNC (VCC3V3)	NC	DNC (VCC4V2)
L	NC	NC	AUART0_RX G5	GND	NC	I2C0_SDA D8	NC	GND	DEBUG B9	JTAG_TRST# D14	GND	GND	GND	BATTERY
M	NC	NC	AUART0_TX H5	AUART0_CTS# J6	NC	I2C0_SCL C7	DNC (EMI_D03) N14	DNC (EMI_D11) J14	RESET# A14	JTAG_TMS D12	PWM3 E9	PSWITCH A11	PWM4 E10	BATTERY
N	NC	NC	GND	AUART0_RTS# J7	NC	DNC (EMI_CLK#) L16	GND	GND	DNC (EMI_DQS1) J17	JTAG_TCK E11	GND	VCC5V	VCC5V	VCC5V
P	NC	NC	AUART1_TX K4	AUART1_RX L4	DNC (EMI_A00) U15	DNC (EMI_CLK) L17	DNC (EMI_DQS0) K17	DNC (EMI_DQS0#) K16	DNC (EMI_DQS1#) J16	GND	JTAG_RTCK E14	JTAG_TDO E13	JTAG_TDI E12	NC

4.2 System components

4.2.1 Processor

The NXP processor i.MX28 (MCIMX287CVM4B) based on an ARM926EJ-S™ core is manufactured in 90 nm technology.
It provides a wide range of functions. Illustration 2 gives an overview.
More information about the i.MX28 processor is provided in the following table.

Table 5: Processor information

Manufacturer	Part number	Temperature range	Package	Silicon revision
NXP	MCIMX283CVM4B	–40 °C … +85 °C	BGA 289	1.2
NXP	MCIMX287CVM4B	–40 °C … +85 °C	BGA 289	1.2

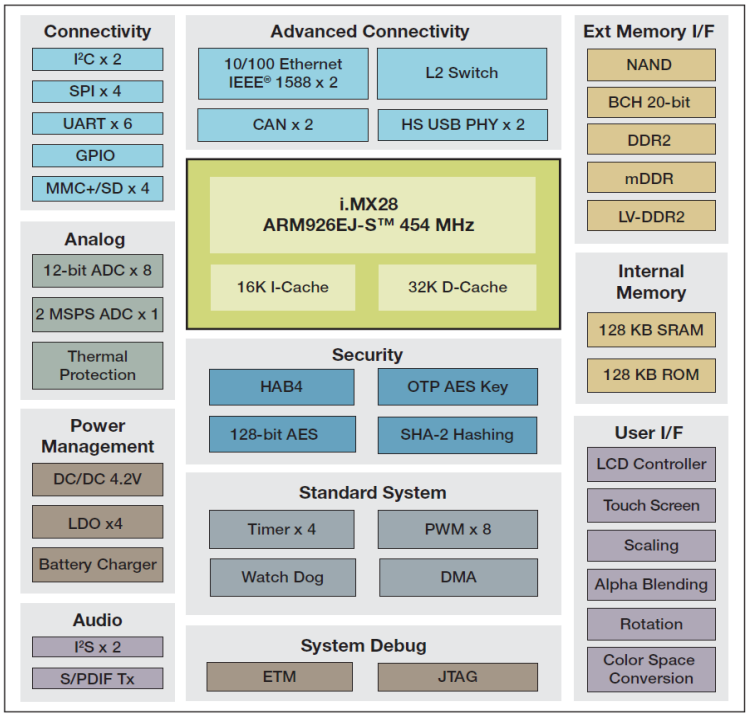

Illustration 2: i.MX28, block diagram
(Source: NXP)

Other functionality of the processor shown in the block diagram can be looked up in the NXP Reference Manual (1).
All essential signals of the processor, except the DDR2 SDRAM interface and the eMMC, are routed to the TQMa28L's contacts.

4.2.1.1 Boot modes

The i.MX28 has of a ROM with integrated boot code. When the i.MX28 starts this boot code initializes the hardware and then loads the program image from the selected boot device.
Instead of booting from the integrated eMMC it is also possible to boot from one of the following interfaces:

- USB
- I^2C
- SPI
- SSP
- GPMI

The boot device and its configuration can be defined with several boot mode registers.
For this the i.MX28 offers two possibilities:

- The settings are read from boot mode pins
- The settings are read from internal burnt OTP eFuses

The exact behaviour during the boot process depends on the value of eFuse ENABLE_PIN_BOOT_CHECK and the signal LCD_RS.
The following table shows the possible combinations.

Table 6: Boot configuration

eFuse: ENABLE_PIN_BOOT_CHECK	Pin: LCD_RS	TQMa28L contact	Boot config read at	Remark
0	X	M4	Boot mode pins	Default
1	0		OTP eFuses	–
	1		Boot mode pins	–

4.2.1.2 Boot device

The eMMC is preset as the standard boot device (SD/MMC MASTER ON SSP1 3V3).
Therefore the boot mode pins on the TQMa28L are connected as follows:

Table 7: Boot mode pin configuration for eMMC-boot

Pin name	Boot mode name	TQMa28L contact	Boot mode	Remark
LCD_D04	Voltage Select	E6	0	10 kΩ PD on TQMa28L
LCD_D03	BM3	D6	1	10 kΩ PU to 3.3 V on TQMa28L
LCD_D02	BM2	C6	0	10 kΩ PD on TQMa28L
LCD_D01	BM1	B6	1	10 kΩ PU to 3.3 V on TQMa28L
LCD_D00	BM0	A6	0	10 kΩ PD on TQMa28L

Note: Malfunction	
	Burning an eFuse is irreversible! TQ-Systems GmbH takes no responsibility for the correct operation of the TQMa28L, if eFuses are burnt by the user. Burning eFuses has to be coordinated with TQ-Systems GmbH, since the TQMa28L then no longer complies with the factory default (altered hardware).

4.2.1.3 Other boot devices

To boot from another source rather than the TQMa28L-internal eMMC, or to use the function ENABLE_PIN_BOOT_CHECK, the default boot mode settings can be changed by resistors of about 1 kΩ at the pins LCD_D[4:0] or LCD_RS.

The necessary settings for other boot device are to be taken from the NXP Reference Manual (1).

4.2.1.4 Processor clock supply

A crystal oscillator on the TQMa28L supplies the processor with 24 MHz.

A 32.768 kHz crystal oscillator on the TQMa28L supplies the RTC domain with a clock signal.

4.2.1.5 Pin multiplexing

Depending on the configuration, the pin multiplexing enables different pins to have different functions. NXP provides on their website the program “IOMUXCC“, which supports the selection of the desired options. TQ-Systems GmbH provides an xml file created with the program "IOMUXCC", which shows the pin-multiplexing of the TQMa28L. The user can configure specific pin-multiplexing based on this xml file. The xml file can be obtained from TQ-Systems Support. The accuracy of the generated configuration cannot be guaranteed! It is the user's responsibility to conscientiously check the generated configuration.

Attention: Destruction or malfunction!	
	Many CPU pins can be used in several different ways. Please, notice the notes about the wiring of these pins in the i.MX28 Reference Manual (1) before integration / start-up of your carrier board / Starterkit.

4.2.1.6 CPU errata

Attention: Destruction or malfunction!	
	Please pay attention to the latest i.MX28 errata (3) and the latest TechNote (8).

4.2.1.7 NXP erratum TKT131240

Attention: Destruction or malfunction!	
	To fix NXP erratum TKT131240 and to ensure a reliable boot process an EEPROM has to be provided on the carrier board.

On account of silicon erratum TKT131240 of the i.MX28 processor, the polarity of both SSP clock domains is inverted during the boot process. The reason is a faulty boot ROM code. When executed during the system start the clock polarity is set wrong. Devices (eMMC, SD card, etc.) connected at SSP0 and SSP1 may not be recognized properly and the processor will not boot.

TQ-Systems GmbH recommends using an additional SPI or I²C EEPROM containing a ROM patch. This EEPROM has to be provided on the carrier board as a boot device. If an I²C EEPROM is used, the boot mode has to be set to I2C0 (EEPROM address 0x50).

In case an SPI EEPROM is used it has to be connected to SPI3. The patch executes from the EEPROM, patches the ROM SSP driver code for one SSP (SSP0 or SSP1), and then switches to boot from the desired boot device. The EEPROM has to be programmed with the patch only once. This can be done using the I²C bus while the TQMa28L is held in reset or directly under Linux.
It is also possible to assemble a pre-programmed EEPROM.

The following table shows two possibilities of how configure the I²C0 or SPI3 boot EEPROM:

Table 8: Boot mode pin configuration for EEPROM-boot connected to I²C or SPI3

Name	TQMa28L contact	Boot from I²C0	Boot from SPI3	Remark
LCD_D03	D6	0	0	10 kΩ PU to 3.3 V on TQMa28L
LCD_D02	C6	0	0	10 kΩ PD on TQMa28L
LCD_D01	B6	0	1	10 kΩ PU to 3.3 V on TQMa28L
LCD_D00	A6	1	1	10 kΩ PD on TQMa28L

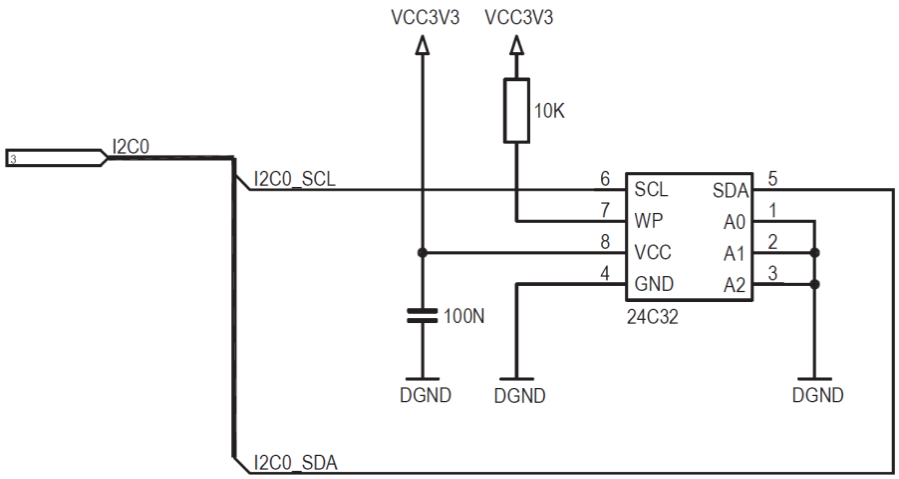

Illustration 3: EEPROM with ROM patch on carrier board

4.2.2 Memory

4.2.2.1 DDR2 SDRAM

The following illustration shows how the DDR2 SDRAM is connected to the CPU.

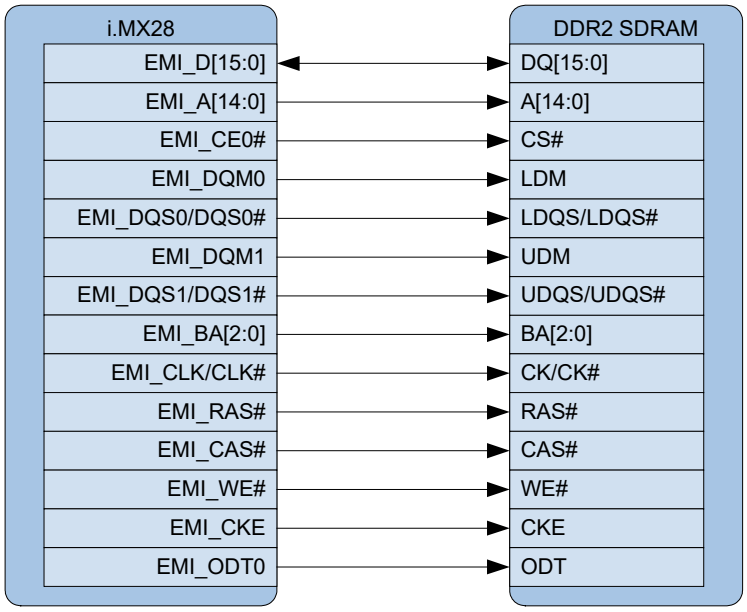

Illustration 4: DDR2 SDRAM interface

The following table gives an overview of the possible alternatives.

Table 9: Memory models DDR2 SDRAM

Manufacturer	Manufacturer's number	Type	Size	Temperature range	Remark
Micron	MT47H64M16HR-3IT:H	64M16	128 Mbyte	–40 °C … +85 °C	–
Micron	**MT47H64M16HR-25EIT:H**	**64M16**	**128 Mbyte**	**–40 °C … +85 °C**	**Default**
Micron	MT47H128M16RT-25EIT	128M16	256 Mbyte	–40 °C … +85 °C	–

The memory allocates the following address range:

Table 10: Address configuration DDR2 SDRAM

Start address	Size	Chip Select	Size
0x4000_000	0x0800_000	CE0#	128 Mbyte
0x4000_000	0x1000_000	CE0#	256 Mbyte

4.2.2.2 eMMC

The TQMa28L provides an eMMC flash to store programs and data (boot loader and operating system).
It is controlled via the SD card controller SSP1 of the i.MX28.

The following illustration shows how the eMMC is connected to the processor.

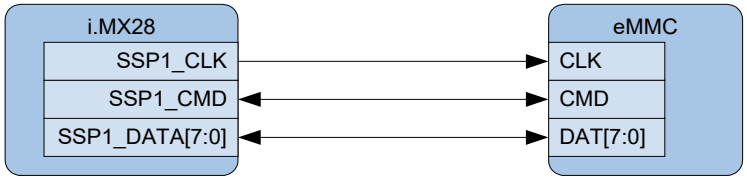

Illustration 5: eMMC interface

4.2.3 RTC

The TQMa28L provides a processor internal RTC. The current consumption of the RTC is approximately 30 µA.
A 32.768 kHz crystal oscillator clocks the RTC.

In the following table the parameters of the 32.768 kHz crystal oscillator are shown.

Table 11: Parameters crystal oscillator

Parameter	Value	Remark
Frequency tolerance	±20 ppm	At +25 °C
Frequency ageing	±3 max. ppm	First year, at +25 °C
Parabolic Coefficient	-0.04×10^{-6} °C^2	Additional deviation at temp ≠ 25 °C

When the power supply is switched off the CPU internal RTC has to be buffered by a lithium-ion battery to maintain its function.
As the RTC in the CPU is supplied by the same power plane than the CPU in normal operation the whole system supplies itself from this power plane. For this reason the RTC cannot be buffered with a normal button cell. If the characteristics of the internal RTC are not suitable, the DS1339 is proposed as an external RTC on the carrier board.

4.2.4 Graphics interfaces / LCD bus

Parallel displays with a maximum frame size of up to 800 × 480 pixels can be connected to the TQMa28L.
The parallel data interface can be up to 24 bits wide. The LCD bus is directly routed to the TQMa28L's contacts.

Table 12: Display signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
LCD_D[23:0]	LCD_D[23:0]	A:F – 3:6	O	LCD-Interface RGB-Data
LCD_HSYNC	LCD_HSYNC	E7	O	LCD-Interface Horizontal Sync
LCD_VSYNC	LCD_VSYNC	D7	O	LCD-Interface Vertical Sync
LCD_ENABLE	LCD_ENABLE	G6	O	LCD-Interface Enable
LCD_DOTCLK	LCD_DOTCLK	B7	O	LCD-Interface Dot clock
LCD_CS	LCD_CS#	G3	O	LCD-Interface Chip Select
LCD_RS	LCD_RS	G5	O	LCD-Interface Register Select
LCD_WR_RWN	LCD_WR_RW#	A7	O	LCD-Interface 6800 R/W# / 8080 W
LCD_RD_E	LCD_RD_E	G4	O	LCD-Interface 6800 Enable / 8080 RD
LCD_RESET	LCD_RESET	H5	O	LCD-Interface Reset Out

4.2.5 Ethernet

The i.MX283 (TQMa28L-AB) provides one; the i.MX287 (TQMa28L-AA) provides two built-in Fast Ethernet controllers, which are designed for 10 and 100 Mbps. Each Ethernet interfaces requires a PHY on the carrier board.

Table 13: Ethernet signals ENET0

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
ENET0_MDIO	ENET_MDIO	D8	I/O	Ethernet Management Data
ENET0_MDC	ENET_MDC	D9	O	Ethernet Output Management Data Clock
ENET0_TXD[0:1]	ENET0_TXD[0:1]	B11:A11	O	Ethernet Output Transmit Data
ENET0_TX_EN	ENET0_TX_EN	C11	O	Ethernet Output Transmit Enable
ENET0_RXD[0:1]	ENET0_RXD[0:1]	B10:A10	I	Ethernet Input Receive Data
ENET0_RX_EN	ENET0_RX_EN	C10	I	Ethernet Data Valid / Carrier Sense
ENET_CLK	ENET_CLK	D11	I/O	Reference Clock
GPIO4_5	ENET_INT#	D13	I	Ethernet Input Interrupt (GPIO)
GPIO4_13	ENET_RESET#	C13	O	Ethernet Output Reset (GPIO)

Table 14: Ethernet signals ENET1 (TQMa28L-AA)

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
ENET1_TXD[0:1]	ENET1_TXD[0:1]	B9:A9	O	Ethernet Output Transmit Data
ENET1_TX_EN	ENET1_TX_EN	C9	O	Ethernet Output Transmit Enable
ENET1_RXD[0:1]	ENET1_RXD[0:1]	B8:A8	I	Ethernet Input Receive Data
ENET1_RX_EN	ENET1_RX_EN	C8	I	Ethernet Data Valid / Carrier Sense

The processor-internal clock generator of the i.MX28 does not meet the clock jitter values required by most Ethernet PHYs. This may cause Ethernet connection problems during link-up.

It is recommended to provide an external clock generator with suitable precision on the carrier board to generate the clock signal for the input ENET_CLK. This can be achieved by using a quartz crystal or a crystal oscillator.

The CPU supplies additional functions according to IEEE1588.

The following signals are available at the TQMa28L's contacts:

Table 15: IEEE1588 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.
ENET0_1588_EVENT2_OUT	1588_EVENT2_OUT	A13	O
ENET0_1588_EVENT2_IN	1588_EVENT2_IN	B13	I
ENET0_1588_EVENT3_OUT	1588_EVENT3_OUT	B12	O
ENET0_1588_EVENT3_IN	1588_EVENT3_IN	C12	I

By turning off pre-set functions and switching on 1588-features, more 1588_Events can be provided.

4.2.6 SD card

The TQMa28L provides an SD card controller (SSP0), whose signals are available at the TQMa28L's contacts.
The following table shows the signals used for the SD card interface.

Table 16: SD card interface signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
SSP0_SCK	SD_CLK	G1	O	SD Card Output Clock
SSP0_CMD	SD_CMD	F1	I/O	SD Card Command
SSP0_D[7:4]	SD_D[7:4]	F2:D2:E2:C2	I/O	SD Card Data / only on TQMa28L-AA
SSP0_D[3:0]	SD_D[3:0]	B1:E1	I/O	SD Card Data
SSP0_CARD_DETECT	SD_DETECT#	H1	I	SD Card Input Card-Detect
GPIO0_28	SD_WP	J1	I	SD Card Input Write-Protection

4.2.7 Serial interfaces

The supported standards, transmission modes and transfer rates of the following interfaces are to be taken from the NXP Reference Manual (1).

4.2.7.1 CAN

The TQMa28L-AA provides two integrated CAN controllers. All four signals are routed to the TQMa28L's contacts. The corresponding drivers have to be provided on the carrier board.

The following table shows the signals used for the CAN interfaces.

Table 17: CAN signals on TQMa28L-AA

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
CAN0_TX	CAN0_TX	M1	O	Only on TQMa28L-AA
CAN0_RX	CAN0_RX	N1	I	
CAN1_TX	CAN1_TX	K1	O	
CAN1_RX	CAN1_RX	L1	I	

4.2.7.2 I²C

Depending on the version the TQMa28L provides up to two I²C interfaces.

The following tables show the signals used for the I²C interfaces.

Table 18: I²C signals on TQMa28L-AA

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
I2C0_SCL	I2C0_SCL	M6	O	10 kΩ PU to 3.3 V on TQMa28L-AA
I2C0_SDA	I2C0_SDA	L6	I/O	10 kΩ PU to 3.3 V on TQMa28L-AA
I2C1_SCL	I2C1_SCL	K6	O	10 kΩ PU to 3.3 V on TQMa28L-AA
I2C1_SDA	I2C1_SDA	J6	I/O	10 kΩ PU to 3.3 V on TQMa28L-AA

Table 19: I²C signals on TQMa28L-AB

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
I2C0_SCL	I2C0_SCL	M6	O	10 kΩ PU to 3.3 V on TQMa28L-AB
I2C0_SDA	I2C0_SDA	L6	I/O	10 kΩ PU to 3.3 V on TQMa28L-AB

Note: pull-up resistors	
	Pull-up resistors for the I²C buses are already assembled on the TQMa28L. If more devices are connected on the carrier board the maximum capacitive bus load according to the I²C standard has to be observed. If necessary additional pull-ups have to be assembled on the carrier board.

4.2.7.3 I²S

To connect an audio-codec via I²S the signals of the Serial Audio Interface (SAIF) are routed to the TQMa28L's contacts.
The following table shows the signals used for the SAIF interface.

Table 20: I²S signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
SAIF0_MCLK	SAIF0_MCLK	E10	O	System Master Clock
SAIF0_LRCLK	SAIF0_LRCLK	E9	I/O	I²S Frame Clock
SAIF0_BITCLK	SAIF0_BITCLK	E11	I/O	I²S Bit Clock
SAIF0_SDATA0	SAIF0_SDATA0	G9	O	I²S Data Output
SAIF1_SDATA0	SAIF1_SDATA0	H9	I	I²S Data Input

The SAIF allows to connect 3, 4 or 5-wire interface, e.g., via I²S. Details are to be taken from the NXP Reference Manual (1).

4.2.7.4 SPDIF

The TQMa28L-AA provides an SPDIF interface with transmit functionality.
The following table shows the signals used for the SPDIF interface.

Table 21: SPDIF signal

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.
SPDIF	SPDIF	F9	O

4.2.7.5 SPI

The following table shows the signals used for the SPI interface.

Table 22: SPI signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
SSP2_SCK	SSP2_SCK	J10	O	Only on TQMa28L-AA
SSP2_MOSI	SSP2_MOSI	J9	O	
SSP2_MISO	SSP2_MISO	K10	I	
SSP2_SS0	SSP2_SS0#	K9	O	

More SPI interfaces can be made available by adapting the multiplexing.

4.2.7.6 UART

The i.MX28 provides five Application UART interfaces (AUART) and one Debug UART (DUART).
The following table shows the signals used for the AUART0 interface.

Table 23: AUART0 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.
AUART0_TX	AUART0_TX	M3	O
AUART0_RX	AUART0_RX	L3	I
AUART0_RTS	AUART0_RTS#	N4	O
AUART0_CTS	AUART0_CTS#	M4	I

The following table shows the signals used for the AUART1 interface.

Table 24: AUART1 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.
AUART1_TX	AUART1_TX	P3	O
AUART1_RX	AUART1_RX	P4	I

The following table shows the signals used for the AUART2 interface.

Table 25: AUART2 signals

i.MX28 signal	TQMa28L signal	TQMa28L-AB contact	Dir.	Remark
AUART2_TX	AUART2_TX	J9	O	Only on TQMa28L-AB
AUART2_RX	AUART2_RX	J10	I	

The following table shows the signals used for the AUART3 interface.

Table 26: AUART3 signals

i.MX28 signal	TQMa28L signal	TQMa28L-AA contact	TQMa28L-AB contact	Dir.
AUART3_TX	AUART3_TX	M2	K9	O
AUART3_RX	AUART3_RX	L2	K10	I
AUART3_RTS	AUART3_RTS#	P2	(NA)	O
AUART3_CTS	AUART3_CTS#	N2	(NA)	I

The following table shows the signals used for the AUART4 interface.

Table 27: AUART4 signals

i.MX28 signal	TQMa28L signal	TQMa28L-AA contact	Dir.	Remark
AUART4_TX	AUART4_TX	L5	O	Only on TQMa28L-AA
AUART4_RX	AUART4_RX	K5	I	
AUART4_RTS	AUART4_RTS#	N5	O	
AUART4_CTS	AUART4_CTS#	M5	I	

The following table shows the signals used for the DUART interface.

Table 28: DUART signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
DUART_TX	DUART_TX	C14	O	–
DUART_RX	DUART_RX	B14	I	10 kΩ PU to 3.3 V on carrier board required

4.2.7.7 USB

The i.MX28 provides two USB-High-Speed controller. Controller USB0 is OTG capable. The second port exclusively provides a Hi-Speed host. For both ports the PHY is integrated in the i.MX28. The 5 V supply for the USB ports has to be implemented on the carrier board. In addition, filtering and EMC protection for the USB signals has to be provided on the carrier board. Notes are to be found in the USB standard.

The following table shows the signals used for the USB0 interface.

Table 29: USB0 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
USB0DM	USB_0_DM	G14	I/O	–
USB0DP	USB_0_DP	F14	I/O	–
USB0_ID	USB_0_ID	H14	I	Only on TQMa28L-AA
GPIO3_9	USB_0_PWR_EN	K13	O	Only on TQMa28L-AA
USB0_OVERCURRENT	USB_0_OC#	E14	I	–

The following table shows the signals used for the USB1 interface.

Table 30: USB1 signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
USB1DM	USB_1_DM	F13	I/O	–
USB1DP	USB_1_DP	E13	I/O	–
GPIO3_8	USB_1_PWR_EN	J13	O	Only on TQMa28L-AA
USB1_OVERCURRENT	USB_1_OC#	D14	I	–

4.2.8 PWM

Three of the eight PWM outputs of the i.MX28 are directly available at the TQMa28L's contacts.
More PWMs are available if the pin multiplexing is adapted.

The following table shows the available PWM signals.

Table 31: PWM signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.
PWM2	LCD_BL_PWM	G7	O
PWM3	PWM3	M11	O
PWM4	PWM4	M13	O

4.2.9 GPIO

Besides their interface function most of the pins of the i.MX28 can also be used as GPIOs. All these GPIOs are interrupt and therefore wake-up capable. The configuration can be taken from the NXP Reference Manual (1).
Some of the GPIOs are directly named as GPIO and directly routed to the TQMa28L's contacts.

The following table shows the GPIO signals which can be used.

Table 32: GPIO signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
BANK0_PIN16	GPIO0_16	G8	I/O	–
BANK0_PIN17	GPIO0_17	J7	I/O	–
BANK0_PIN20	GPIO0_20	E8	I/O	–
BANK0_PIN24	GPIO0_24	H4	I/O	–
BANK0_PIN26	GPIO0_26	H8	I/O	–
BANK0_PIN27	GPIO0_27	H7	I/O	–
BANK3_PIN06	GPIO3_6	L7	I/O	Only on TQMa28L-A**A**
BANK3_PIN26	GPIO3_26	H9	I/O	Only on TQMa28L-A**B**

4.2.10 JTAG

The i.MX28 provides two JTAG modes. The mode is defined with the signal DEBUG.
To change the JTAG mode, the default can be changed by a pull-down resistor of approximately 1 kΩ at pin DEBUG.

The following table shows the available modes. The default mode used on the TQMa28L is printed in **bold**.

Table 33: JTAG modes

TQMa28L signal	Level	Function	TQMa28L contact	Remark
Debug	0	JTAG interface: Boundary scan	L9	–
	1	**JTAG interface: ARM debugging**		**10 kΩ PU to 3.3 V on TQMa28L**

The JTAG signals are directly routed from the CPU to the TQMa28L's contacts. All necessary pull-up and pull-down resistors are already assembled on the TQMa28L.

The following table shows the signals used for the JTAG interface.

Table 34: JTAG signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
JTAG_TCK	JTAG_TCK	N10	I	10 kΩ PU to 3.3 V on TQMa28L
JTAG_TMS	JTAG_TMS	M10	I	10 kΩ PU to 3.3 V on TQMa28L
JTAG_TDI	JTAG_TDI	P13	I	10 kΩ PU to 3.3 V on TQMa28L
JTAG_TDO	JTAG_TDO	P12	O	–
JTAG_TRST	JTAG_TRST#	L10	I	10 kΩ PU to 3.3 V on TQMa28L
JTAG_RTCK	JTAG_RTCK	P11	O	10 kΩ PU to 3.3 V on TQMa28L

4.2.11 ADC

The TQMa28L provides eight ADC inputs. The inputs are purposefully not equipped with filter capacitors to GND.
Filter capacitors have to be designed on the carrier board, if required.
The ADC supports resistive 4- or 5-wire touch screens.
Adequate protection circuitry has to be implemented on the carrier board.

The following table describes the ADC signals available at the TQMa28L's contacts:

Table 35: ADC signals

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	4-wire touch	5-wire touch	Remark
LRADC0	LRADC0	G11	AI	–	–	–
LRADC1	LRADC1	F11	AI	–	–	–
LRADC2	LRADC2	E12	AI	Touch Right / X+	UL	–
LRADC3	LRADC3	F12	AI	Touch Top / Y+	LL	–
LRADC4	LRADC4	H11	AI	Touch Left / X–	UR	–
LRADC5	LRADC5	J11	AI	Touch Bottom / Y–	LR	–
LRADC6	LRADC6	J12	AI	–	Common	–
HSADC0	HSADC0	H12	AI	–	–	High-Speed ADC (not qualified)

4.2.12 Reset

There are two ways to reset the TQMa28L:

- Power-on reset
- RESET# input

The following table describes the Reset signal available at the TQMa28L's contacts:

Table 36: RESET signal

i.MX28 signal	TQMa28L signal	TQMa28L contact	Dir.	Remark
RESETN	RESET#	M9	I	- 10 kΩ PU to 3.3 V on TQMa28L - Minimum required Low-Time: ≥100 msec

To improve the stability of the TQMa28L in case of voltage dips, it is recommended to implement a supervisor for voltage monitoring on the carrier board. A supervisor with a reset time of at least 200 msec should be used.
The following illustration shows a possible implementation.

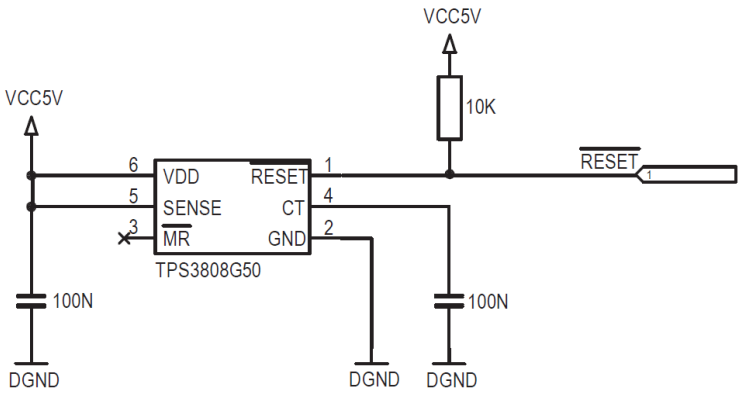

Illustration 6: Optional supervisor on carrier board

4.2.13 Power supply

4.2.13.1 TQMa28L supply

The TQMa28L works with a single supply of 5 V that must be provided by the carrier board.

Alternatively a lithium-ion battery can supply the TQMa28L.

If a lithium-ion battery is connected at the BATTERY pin it is charged if the TQMa28L is supplied with 5 V.
Software settings can be done in the registers HW_LRADC_CONVERSION and HW_POWER_CHARGE.

Attention: Lithium primary batteries and lithium-ion secondary batteries	
	Lithium primary batteries may not be used at the i.MX28 or TQMa28L (pin BATTERY) because of the CPU's charging function!

The following table shows the permitted ranges of the supply voltages.

Table 37: Supply voltages

Parameter	Min.	Typ.	Max.
Supply voltage V_{IN} VCC5V	4.75 V	5.00 V	5.25 V
Supply voltage V_{IN} BATTERY	3.10 V	–	4.20 V

The calculated current consumption (worst case) is 0.4 A. The current consumption strongly depends on component placement, software and wiring options. The values given are to be seen as indicative values.

Table 38: Current consumption

Parameter	V_{IN}	I_{ITYP}	Remark
Current consumption in Linux idle mode	5.0 V	147 mA	–
Current consumption in Linux boot mode	5.0 V	234 mA	–
Inrush current	5.0 V	3.56 A	Peak current for approximately 1.2 µs

4.2.13.2 Power Management Unit

The i.MX28 has an integrated Power Management Unit (PMU). All voltages required on the TQMa28L are generated by the PMU. The following illustration shows the internal structure of the PMU.

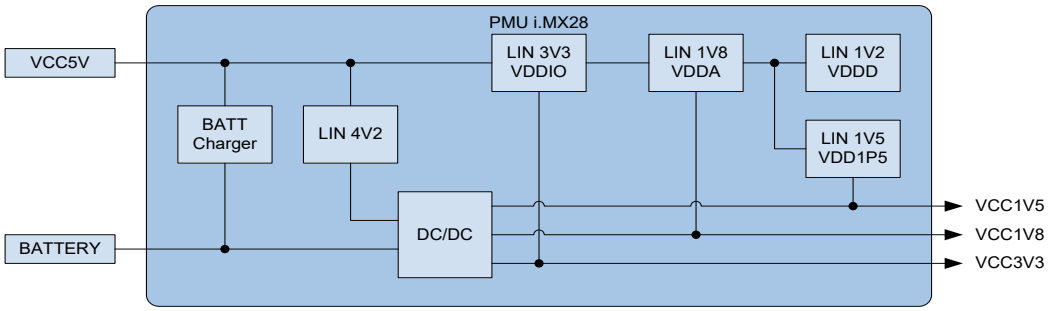

Illustration 7: i.MX28 PMU, block diagram

The internal power supply consists of a chain of linear regulators a DC/DC converter and a battery charger.

If the TQMa28L is supplied via VCC5V the processor starts with the voltages generated by its internal linear regulators. During the boot process the linear regulator LIN 4V2 is switched on and supplies the DC/DC converter. From this point the DC/DC converter provides the necessary system voltages instead of the linear regulators. In BATTERY mode the DC/DC converter starts directly.

The i.MX28 provides an extensive set of registers to configure the PMU. Among other things the output voltages of all voltage regulators, the brown-out level, the start behaviour, the charging currents, the trigger levels, etc. can be configured.

The settings of these registers have to be checked or set for the respective design. Further information is to be taken from the NXP Reference Manual (1), the i.MX28 data sheet (2) and the Application Note for the power management (4) of the i.MX28.

4.2.13.3 Power-up/down

The start behaviour of the TQMa28L depends on the selected voltage source (VCC5V or BATTERY).

- TQMa28L supply with VCC5V: Power-up sequence of the CPU starts immediately
- TQMa28L supply with BATTERY: Power-up sequence of the CPU only starts when PSWITCH is supplied with a valid start-up voltage between 0.65 V and 1.5 V.

The function of PSWITCH depends on the applied voltage (see NXP Reference Manual (1)).

In case the function "Fast Falling Edge" is not used (which could be used to power-down the CPU) it is recommended to disable this function using the circuitry suggested by NXP (see Illustration 8).

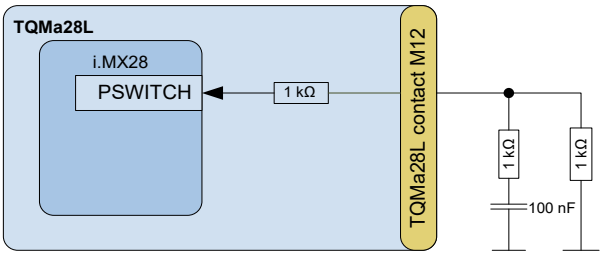

Illustration 8: Wiring of PSWITCH

Attention: TQMa28L Power-up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the TQMa28L power-up sequence has been completed.

5. SOFTWARE

The TQMa28L comes with a preinstalled especially tailored boot loader.
The boot loader contains TQMa28L-specific adaptions as for example:

- CPU/PMU configuration
- RAM configuration
- RAM timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strength

These settings have to be adapted if a different boot loader is used. More details can be requested from the TQ-Support.

6. MECHANICS

6.1 TQMa28L dimensions

Dimensions (L x W): 30.6 × 30.6 mm²
Maximum height: 3.5 mm

6.2 TQMa28L views

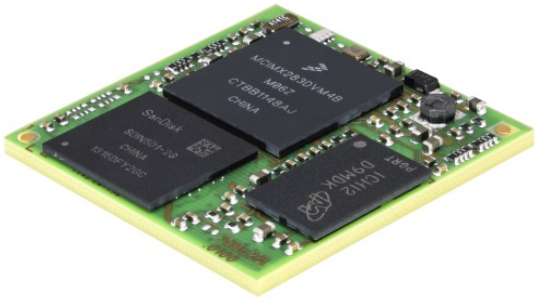

Illustration 9: TQMa28L top view (3D)

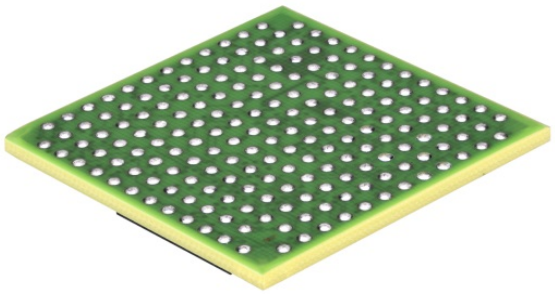

Illustration 10: TQMa28L bottom view (3D)

6.3 TQMa28L component placement

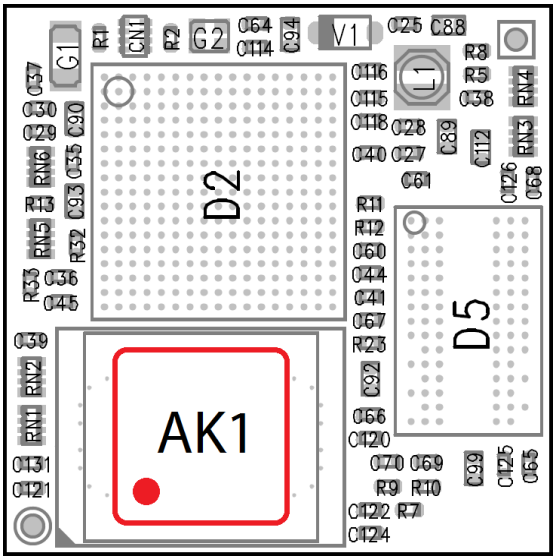

Illustration 11: TQMa28L component placement top

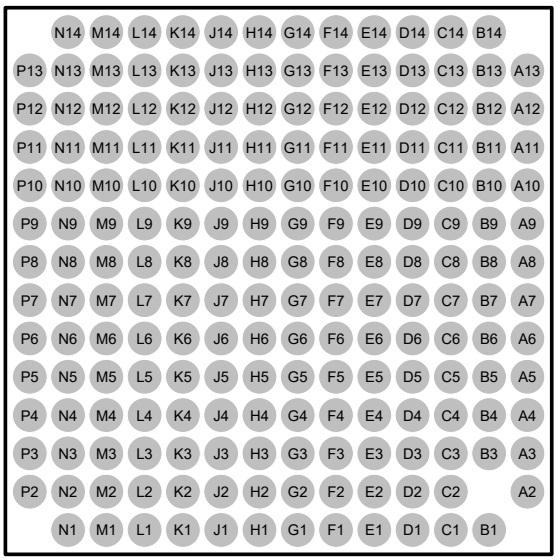

Illustration 12: TQMa28L **bottom view**

The label on the TQMa28L shows:

- MAC address
- Tests performed
- TQMa28L version and revision

The MAC address is the TQMa28L serial number.
The "(+1)" indicates the second subsequent MAC address reserved for the TQMa28L.

6.4 TQMa28L footprint

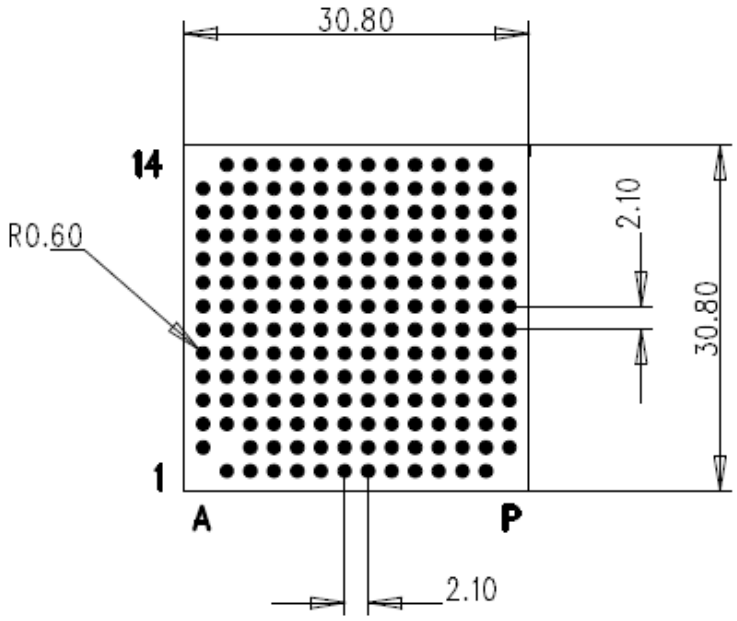

Illustration 13: TQMa28L, recommended carrier board footprint, **top view through TQMa28L**

Attention: Note with respect to the placement of the carrier board	
	The free space at position B2 serves as indicator for automatic placement detection.

6.5 Requirements for the superior system

6.5.1 Protection against external effects

As an embedded module the TQMa28L is not protected against dust, external impact and contact (IP00).
An adequate protection has to be guaranteed by the surrounding system.

6.5.2 Thermal management

Up to 2 W (worst case) have to be dissipated to cool the TQMa28L. The power dissipation originates primarily in the CPU and in the DDR2 SDRAM. The user is responsible for an adequate cooling system in his application.
In most cases a passive cooling should be sufficient.

Attention: Destruction or malfunction, TQMa28L cooling	
	The TQMa28L belongs to a performance category in which a cooling may be required. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX28 must be taken into consideration when connecting the heat sink. The i.MX28 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa28L and thus malfunction, deterioration or destruction.

6.5.3 Structural requirements

The TQMa28L has to be soldered on the carrier board. Please contact TQ-Support for soldering instructions (10).

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMa28L was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the TQMa28L.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Reliability and service life

No detailed MTBF calculation has been done for the TQMa28L. It is designed to be insensitive to vibration and impact.
Product life limiting components like electrolyte capacitors were not used.

7.5 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly. In general, a reliable operation is given when following conditions are met:

Table 39: Climate and operating conditions "Commercial temperature range" 0 °C … +70 °C

Parameter	Range	Remark
Chip temperature	–40 °C … +105 °C	Environment: –40 °C … +85 °C
DDR2 SDRAM case temperature	0 °C … +85 °C	–
Other ICs case temperature	0 °C … +70 °C	–
TQMa28L storage temperature	–40 °C … +85 °C	–
Relative humidity (operation / storing)	10 % … 90 %	Not condensing

Table 40: Climate and operating conditions "Extended temperature range" –25 °C … +85 °C

Parameter	Range	Remark
CPU T_J temperature	–40 °C … +105 °C	Environment: –40 °C … +85 °C
DDR2 SDRAM case temperature	–40 °C … +95 °C	–
Other ICs case temperature	–25 °C … +85 °C	–
TQMa28L storage temperature	–40 °C … +85 °C	–
Relative humidity (operation / storing)	10 % … 90 %	Not condensing

Table 41: Climate and operating conditions "Industrial temperature range" –40 °C … +85 °C

Parameter	Range	Remark
CPU T_J temperature	–40 °C … +105 °C	Environment: –40 °C … +85 °C
DDR2 SDRAM case temperature	–40 °C … +95 °C	Environment: –40 °C … +85 °C
Other ICs case temperature	–40 °C … +85 °C	–
TQMa28L storage temperature	–40 °C … +85 °C	–
Relative humidity (operation / storing)	10 % … 90 %	Not condensing

7.6 Environment protection

7.6.1 RoHS

The TQMa28L is manufactured RoHS compliant.

- All components used and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

7.6.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa28L was designed to be recyclable and easy to repair.

7.6.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.6.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200.000.
Thus the TQMa28L always has to be considered in combination with the complete system.
The compliance regarding EuP directive is basically possible for the TQMa28L on account of the available Standby or Sleep-Modes of the components on the TQMa28L.

7.6.5 Battery

No batteries are assembled on the TQMa28L.

7.6.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa28L, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa28L is delivered in reusable packaging.

7.6.7 Other entries

The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging.
Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 42: Acronyms

Acronym	Meaning
A/D	Analog/Digital
ADC	Analog/Digital Converter
AI	Analog In
ARM®	Advanced RISC Machine
AUART	Application Universal Asynchronous Receiver/Transmitter
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR	Double Data Rate
DNC	Do Not Connect
DUART	Debug Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
GPMI	General Purpose Media Interface
I	Input
I/O	Input/Output
I²C	Inter-Integrated Circuit
I²S	Inter Integrated Circuit Sound
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LGA	Land Grid Array
LL	Lower Left
LR	Lower Right
MTBF	Mean operating Time Between Failures
NA	Not Available
NAND	Not-And
NC	Not Connected
NP	Not Present
O	Output
OTG	On-The-Go
OTP	One-Time Programmable
PCMCIA	People Can't Memorize Computer Industry Acronyms
PMU	Power Management Unit
PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Resistor Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGB	Red Green Blue
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SAIF	Serial Audio Interface
SD card	Secure Digital Card
SD/MMC	Secure Digital Multimedia Card
SDRAM	Synchronous Dynamic Random Access Memory
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Port
UART	Universal Asynchronous Receiver/Transmitter
UL	Upper Left
UR	Upper Right
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 43: Further applicable documents

No.	Description	Rev. / Date	Company
(1)	i.MX28 Applications Processor Reference Manual	2 / Aug. 2013	NXP
(2)	Datasheet i.MX28 Applications Processors for Consumer Products	3 / July 2012	NXP
(3)	Chip Errata for the i.MX28	2 / Sept. 2012	NXP
(4)	Application Note AN4199	1 / Mar. 2013	NXP
(5)	IO Mux tool for the i.MX28	2.0.27.30460	NXP
(6)	TQMa28L pin multiplexing	0102 / 2014	TQ-Systems
(7)	TQMa28-MBa28 Tech Note	– current –	TQ-Systems
(8)	TQMa28L-Tech Note	– current –	TQ-Systems
(9)	Support-Wiki for the TQMa28	– current –	TQ-Systems
(10)	Processing instructions for TQMa28L	– current –	TQ-Systems

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