MBa93xxLA
User's Manual

MBa93xxLA UM 0001
13.04.2023

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	12.04.2023	Kreuzer		First edition

1. ABOUT THIS MANUAL

1.1 Copyright and license expenses

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa93xxLA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa93xxLA schematics
- TQMa93xxLA User's Manual
- i.MX 93 Data Sheet
- i.MX 93 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa93xxLA

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa93xxLA as of revision 02xx. The MBa93xxLA is designed as a carrier board for the TQ-Minimodules TQMa93xxLA. Core of the MBa93xxLA is the TQMa93xxLA with an NXP i.MX 93 CPU.

The TQMa93xxLA connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, etc., all other available signals of the TQMa93xxLA are routed on 50 mil standard pin headers on the MBa93xxLA.
CPU features and interfaces can be evaluated, software development for a TQMa93xxLA based project can start immediately.
Currently four i.MX 93 derivatives are supported:

1. i.MX 9352 (2 x Cortex®-A55, M33, NPU)
2. i.MX 9351 (1 x Cortex®-A55, M33, NPU)
3. i.MX 9332 (2 x Cortex®-A55, M33)
4. i.MX 9331 (1 x Cortex®-A55, M33)

Note: i.MX 933x, reduced functionality	
	The information in this document refers to the i.MX 9352 and i.MX 9351. The i.MX 933x is not considered in this document because some functions are not available or have limitations. Details can be found in the TQMa93xxLA User's Manual.

2.1 MBa93xxLA block diagram

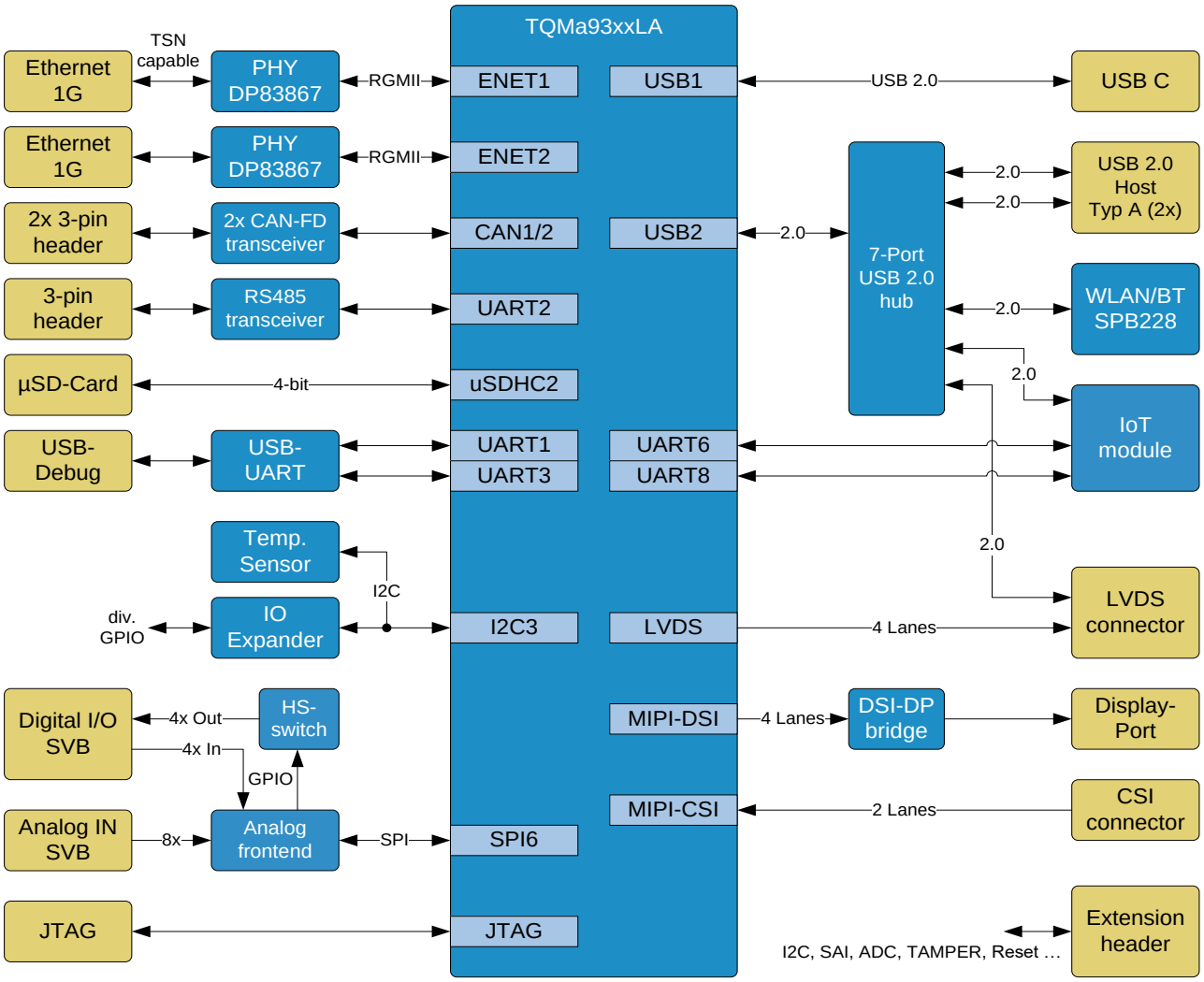


Figure 1: Block diagram MBa93xxLA

2.2 MBa93xxLA data interfaces

The following interfaces/functions and user interfaces are available on the MBa93xxLA:

Table 2: Data interfaces & power connectors

Interface	Connector	Type
Analog frontend	X28	DMC 1,5/ 8-G1F-3,5-LR Phoenix
CAN-FD	X8, X9	3-pin Phoenix
Coin cell	X14	CR2032 holder
Digital IO	X27	DMC 1,5/10-G1F-3,5-LR Phoenix
DisplayPort	X21	20-pin, 90°
Ethernet, 1000 Base-T	X6, X7	RJ-45, integrated magnetics
Extension header	X1	50 mil header, 30-pin
External battery	X3	2-pin header
IoT antennas (main, GNSS)	X25, X26	2 x U.FL-R
IoT SIM card	X24	Micro-SIM card holder
ISO 14443	X4	2-pin header for antenna
LVDS	X12	30-pin, DF19G
LVDS CMD	X11	20-pin, DF19G
MIPI CSI	X13	60-pin, Board-to-Board
Power In	X23	MC 1,5/ 2-GF-3,5 LR Phoenix
RS485	X10	3-pin Phoenix
SD card, UHS-I	X15	Push-Pull
USB 2.0 Host	X19	USB, stacked Type A
USB Type C	X17	USB, Type C
USB debug	X22	USB, Micro AB
WLAN / Bluetooth	D6-A, D6-B	MHF4

The MBa93xxLA provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	7 × Green LED	Power LEDs
	4 × Green LED	3 × USB Host, 1 × USB Type-C
	1 × Green LED	Debug LED for USB debug interface
	1 × Green LED	User LED1
	1 × Yellow LED	User LED2
	1 x Green LED	IoT net status
	1 × Red LED	Reset LED
	2 × Green / 2 x Yellow LED	Ethernet LEDs (Activity / Speed)
	2 x Green LED	WLAN / Bluetooth
	1 x Green LED	SD card
Temperature sensor	1 × SE97BTP	Digital I^2C temperature sensor
Power / Reset button	2 × Push button	PMIC_RST, ONOFF
General Purpose button	2 × Push button	GP push button at port expander
Boot Mode configuration	1 × 4-fold DIP switch	Boot Mode configuration
CAN termination	2 × 2-fold DIP switch	S4, S5
JTAG	1 × 10-pin, 100 mil header	X20
RS485 termination	1 x 2-fold DIP switch	S6

3. ELECTRONICS

The following chapters describe the interfaces of the MBa93xxLA as of revision 02xx in connection with a TQMa93xxLA with maximum configuration.
In any case the TQMa93xxLA User's Manual must be complied with.

3.1 TQMa93xxLA

The TQMa93xxLA is the central system on the MBa93xxLA. It provides LPDDR4 SDRAM, eMMC, NOR flash, RTC, EEPROM, power supply and power management functionality.

All TQMa93xxLA internal voltages are derived from the 5 V supply voltage. All functionally relevant pins of the CPU are routed to the TQMa93xxLA pads. This enables the user to use the TQMa93xxLA with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa93xxLA User's Manual.

On the MBa93xxLA the standard interfaces like USB, Ethernet, etc., provided by the TQMa93xxLA are routed to industry standard connectors. All other signals and buses provided by the TQMa93xxLA are routed to 50 mil headers.

The boot behaviour of the TQMa93xxLA can be configured. The Boot Mode configuration is set by a DIP switch on the MBa93xxLA, see chapter 3.2.

Furthermore the MBa93xxLA provides all power supplies and configurations required for the operation of the TQMa93xxLA.

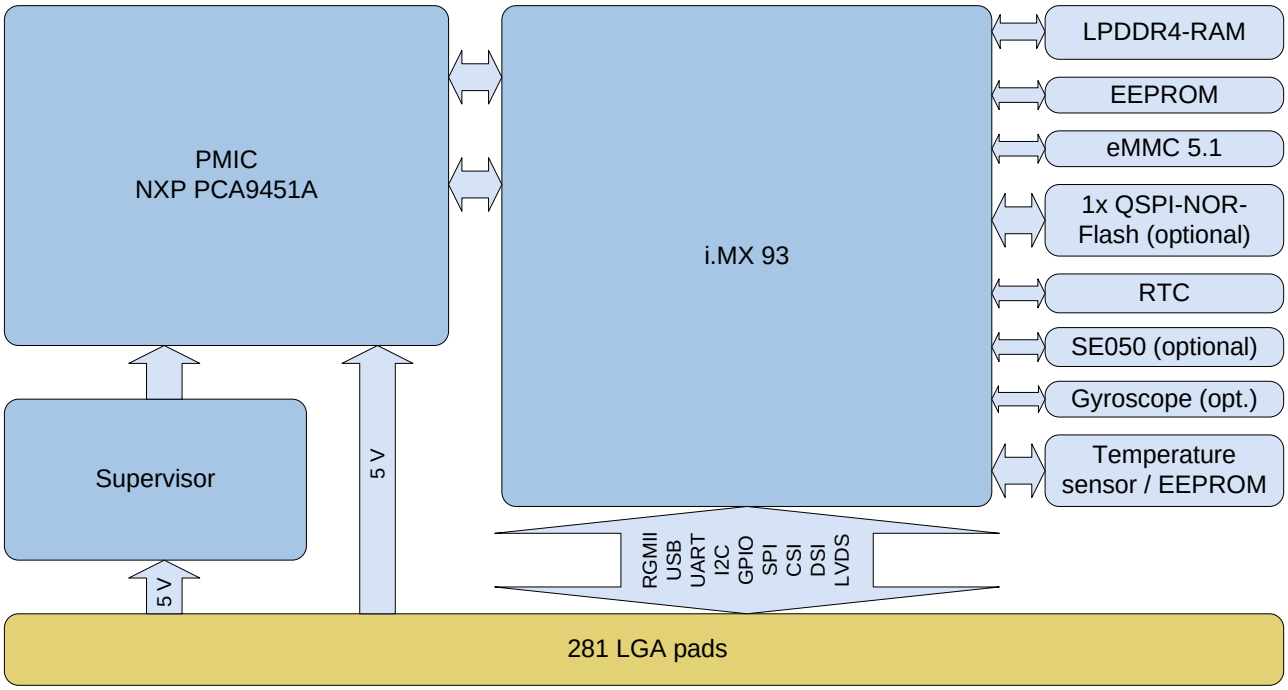


Figure 2: Block diagram TQMa93xxLA

3.2 Boot Mode configuration

The TQMa93xxLA can boot from different boot sources. The boot source is selected on the MBa93xxLA via DIP switches (S1). The following table shows the possible boot configurations of the i.MX93, where Serial NAND is not supported by the MBa93xxLA.

The four BOOT_MODE pins of the CPU are not dedicated pins, but are multiplexed with functional IO pins. So that neither connected periphery influences the boot mode nor the boot configuration influences the connected periphery, the pins are switched via analog switch. The RESET_OUT# signal is used for toggling, which triggers the switch with a delay (approx. 5 ms) after RESET_OUT# has been released by the logic and RC element. The switch back to the DIP switch is done almost without delay at a low edge at RESET_OUT#.

At the BOOT_MODE signals 100 kΩ pull-down resistors are provided. The 3.3 V provided by the module are used as pull-up voltage for the switchable 4.7 kΩ resistors.

Table 4: Boot Mode configuration

Boot-Mode	S1-4 (BM3)		S1-3 (BM2)		S1-2 (BM1)		S1-1 (BM0)		Remark
	Pos.	Level	Pos.	Level	Pos.	Level	Pos.	Level	
Boot from eFuses	OFF	0	OFF	0	OFF	0	OFF	0	–
Serial Downloader (USB 1)	OFF	0	OFF	0	OFF	0	ON	1	–
eMMC (USDCH1)	OFF	0	OFF	0	ON	1	OFF	0	–
SD card (USDHC2)	OFF	0	OFF	0	ON	1	ON	1	–
FlexSPI Serial NOR	OFF	0	ON	1	OFF	0	OFF	0	–
LPB: Boot from eFuses	ON	1	OFF	0	OFF	0	OFF	0	Low Power Boot
LPB: Serial Downloader (USB 1)	ON	1	OFF	0	OFF	0	ON	1	
LPB: eMMC (USDCH1)	ON	1	OFF	0	ON	1	OFF	0	
LPB: SD card (USDHC2)	ON	1	OFF	0	ON	1	ON	1	
LPB: FlexSPI Serial NOR	ON	1	ON	1	OFF	0	OFF	0	

Note: Boot from NAND	
	Booting from NAND is not supported on the MBa93xxLA.

3.3 I²C devices

Due to the large number of I2C devices on the TQMa93xxLA, special attention must be paid to the I2C1 addresses already in use. Depending on the application and software load the number of used I2C devices may limit the data throughput or block the bus. For this reason several devices used on the MBa93xxLA are connected to I2C3 and I2C5.

Table 5: I²C signals

Signal	TQMa93xxLA name
I2C1_SDA	I2C1_SDA
I2C1_SCL	I2C1_SCL
I2C3_SDA	GPIO_IO28
I2C3_SCL	GPIO_IO29
I2C5_SDA	GPIO_IO22
I2C5_SCL	GPIO_IO23

The following table shows the default I²C device addresses on the MBa93xxLA and the TQMa93xxLA.
For some devices the address can be changed by assembly options. The options are described in detail in the given chapter.

Table 6: I²C devices, address mapping on TQMa93xxLA and MBa93xxLA

Location	Bus	Device	Function		7-bit address	Remark
TQMa93xxLA	I2C1	PCA9451	PMIC		0x25 / 010 0101b	
		SE97BTP	Temperature sensor in EEPROM		0x1B / 001 1011b	
			EEPROM	Read / Write	0x53 / 101 0011b	
				Protection command	0x33 / 011 0011b	
		SE050 (opt.)	Trust Secure Element		0x48 / 100 1000b	
		PCF85063A	RTC		0x51 / 101 0001b	
		M24C64	EEPROM	Memory array	0x57 / 101 0111b	
				Identification page (32 Byte)	0x5F / 101 1111b	
		ISM330 (opt.)	Gyroscope		0x6A / 110 1010b	
MBa93xxLA	I2C3	X1	Pin header		NA	
		PTN5110	USB-C PD-Controller		0x50 / 101 0000b	available at pin header
		SE97BTP	Temperature sensor in EEPROM		0x1C / 001 1100b	
			EEPROM	Read / Write	0x54 / 101 0100b	
				Protection command	0x34 / 011 0100b	
		PCA9538	Port expander #1		0x70 / 111 0000b	
		PCA9538	Port expander #2		0x71 / 111 0001b	
		PCA9538	Port expander #3		0x72 / 111 0010b	
	I2C5	X13	MIPI-CSI		NA	
		TC9595	Display-Port Bridge		0x0F / 000 1111b	

Note: I²C address conflicts

When changing the address due to assembly options or when connecting further I²C components, it must be ensured that no address conflicts occur. Otherwise malfunctions may occur. The addresses preassigned by the TQMa93xxLA must also be observed (depending on the TQMa93xxLA variant used).

3.4 GPIO port expander

Three I2C IO expanders with 8 ports each are used on the on the MBa93xxLA. The port expanders are controlled via I2C3. The addresses of the port expanders can be altered by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 6. The assembly options are documented in the schematic of the MBa93xxLA.

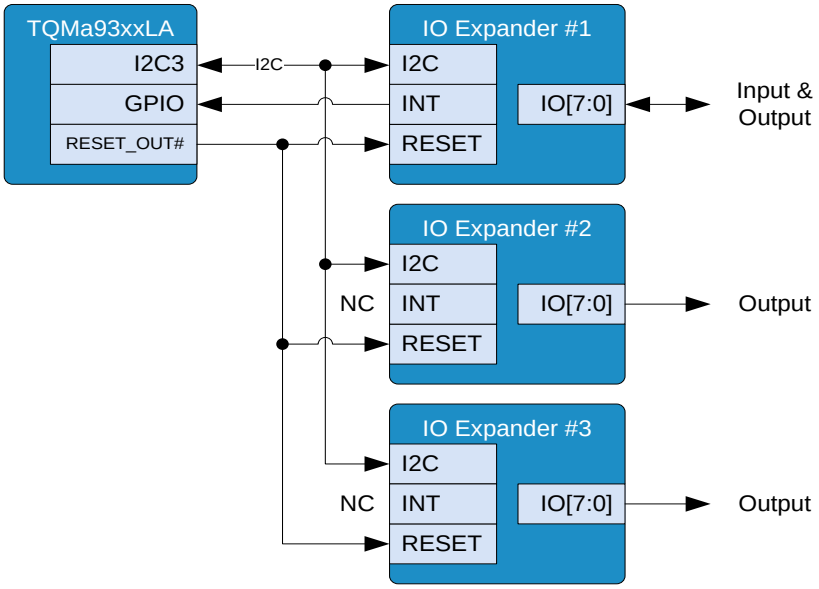


Figure 3: Block diagram GPIO expanders

The IO expanders are supplied with V_3V3. Due to the lack of GPIO pins at the TQMa93xxLA, only one IO expander, to which input signals are connected, sends the interrupt signal to the CPU. The other expanders only contain output signals. The interrupt signal is not necessary for this. The used IO expanders have a reset input that is connected to RESET_OUT#. This resets all signals at a reset of the CPU (High-Z).

Table 7: Port expander functions

Expander	I²C device address	Port	Signal	Dir.
1	0x70	IO_0	3V8_EN	O
		IO_1	(NC)	–
		IO_2	(NC)	–
		IO_3	IOT_PWRKEY	O
		IO_4	IOT_RESET	O
		IO_5	IOT_W_DISABLE	O
		IO_6	BUTTON_A#	I
		IO_7	BUTTON_B#	I
2	0x71	IO_0	ENET1_RESET#	O
		IO_1	ENET2_RESET#	
		IO_2	USB_RESET#	
		IO_3	NC	–
		IO_4	WLAN_PD#	O
		IO_5	WLAN_W_DISABLE#	
		IO_6	WLAN_PERST#	
		IO_7	12V_EN	
3	0x72	IO_0	LCD_RESET#	O
		IO_1	LCD_PWR_EN	
		IO_2	LCD_BLT_EN	
		IO_3	DP_EN	
		IO_4	MIPI_CSI_EN	
		IO_5	MIPI_CSI_RST#	
		IO_6	USER_LED1	
		IO_7	USER_LED2	

3.5 Temperature sensor and EEPROM

A temperature sensor SE97BTP is populated on the MBa93xxLA to monitor the temperature. The same type of sensor is also used on the TQMa93xxLA. The sensor of MBa93xxLA is read out via I2C3, the sensor of TQMa93xxLA is read out via I2C1, see Table 6.

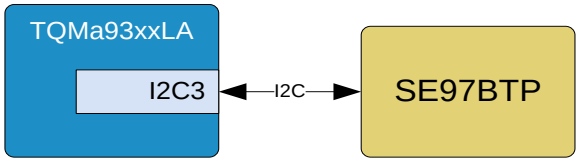


Figure 4: Block diagram temperature sensor

The sensor address on the MBa93xxLA can be changed by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 6. The assembly options are documented in the MBa93xxLA schematics.

The SE97BTP has an additional EEPROM. Further specifications of the SE97BTP can be found in the data sheet.

The EVENT# output of the sensor is not used.

3.6 RTC backup

The TQMa93xxLA has an optional RTC and a voltage rail for standby functions. This is supplied via pin V_LICELL.
On the MBa93xxLA there are two possibilities to supply the LICELL input [1]:

- CR2032-Battery holder
- 2-pin header (X3) for alternative connection of an external voltage or batteries

The maximum input voltage at X3 is described in the TQMa93xxLA User's Manual.

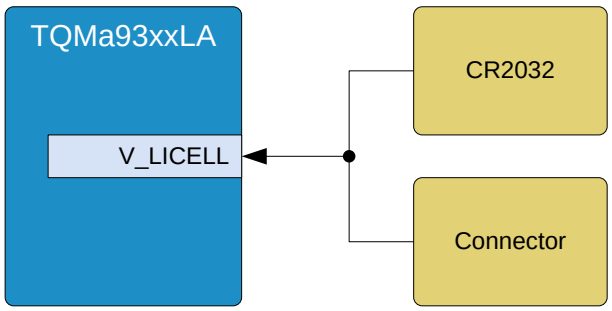


Figure 5: Block diagram RTC backup

Table 8: Pinout RTC backup (X3)

Pin	Signal	Level	Remark
1	V_LICELL	3 V	Supply voltage for RTC on TQMa93xxLA
2	GND	0 V	Ground

To meet regulatory requirements for protection against accidental battery charging, a 1 kΩ resistor and diode is connected in series between X3/X14 and the V_LICELL input of the TQMa93xxLA.

1: Only one of the two options may be used at a time!

The diode has a very low forward voltage (<0.1 V) in order not to unnecessarily reduce the battery runtime and a very low reverse current to keep residual charging currents as low as possible.

If it is necessary to reduce the forward voltage to 0 V for test purposes, the protective diode can be removed according to Table 9 and a corresponding resistor can be fitted.

Table 9: Assembly option RTC-Backup

Reverse current protection	V56	R216	Remark
Active	BAS70	NP	Default
Not active	NP	0 Ω	Note: 1 kΩ in series is still present in this case

Attention: Loss of reverse current protection	
	The reverse current protection is lost when the protective diode is replaced with a resistor! This is especially critical for TQMa93xxLA with external RTC, since here the 3.3 V supply of the TQMa93xxLA in ON mode[1] drives directly into the RTC backup battery!

3.7 USB hub

The 7-port USB 2.0 hub USB2517 is used to provide the USB interfaces on the USB host sockets as well as for the WLAN module, IoT module and LVDS connectors. The USB hub is connected to the CPU at the USB2 port.

VBUS with max. 500 mA each port is provided at the USB type A double jack.

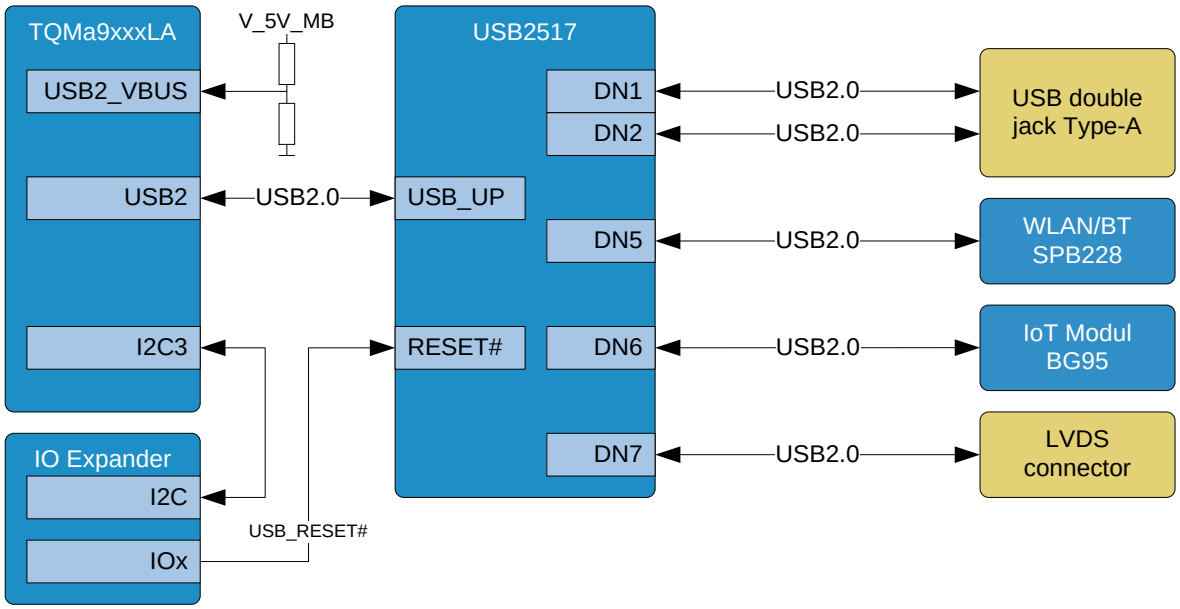


Figure 6: Block diagram USB hub

1: TQMa93xxLA is supplied at V_3V3_IN.

3.8 Data interfaces

3.8.1 CAN-FD

Both CAN interfaces of the MBa93xxLA are available at the two 3-pin connectors X8 and X9. Both interfaces are galvanically isolated with 1 kV. The CAN interfaces are not electrically isolated from each other.

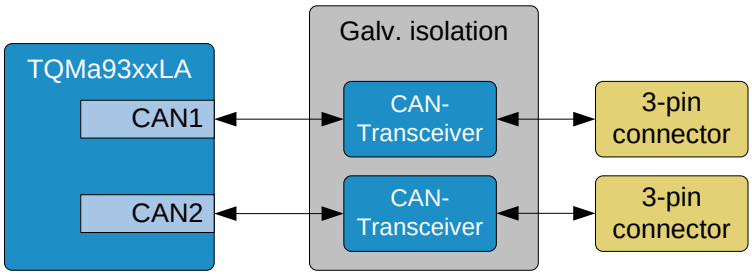


Figure 7: Block diagram CAN

The CAN signals can be terminated with 120 Ω via DIP switches S4 (CAN1) and S5 (CAN2).

Table 10: CAN termination

Sx-1	Sx-2	Modus
OFF	OFF	No termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Termination with 120 Ω

Table 11: Pinout CAN1 / 2 (X8, X9)

CAN	Pin	Signal	Dir.	Level	Remark
CAN0	1	CAN0_H	I/O	Spec. (1)	CAN High-Level I/O from CAN0 / galvanically isolated
	2	CAN0_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN0 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated
CAN1	1	CAN1_H	I/O	Spec. (1)	CAN High-Level I/O from CAN1 / galvanically isolated
	2	CAN1_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN1 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated

3.8.2 Debug USB / UART

For debug purposes, two UARTs of the i.MX93 CPU are made available at USB socket X22 by using a Silicon Labs USB bridge. UART1 and UART3 are used for this purpose. UART1 can be multiplexed to the A55 core as well as to the Cortex M33 core of the i.MX93. UART3 can only be multiplexed to the A55 core. Thus for both cores one UART each is available for debugging.

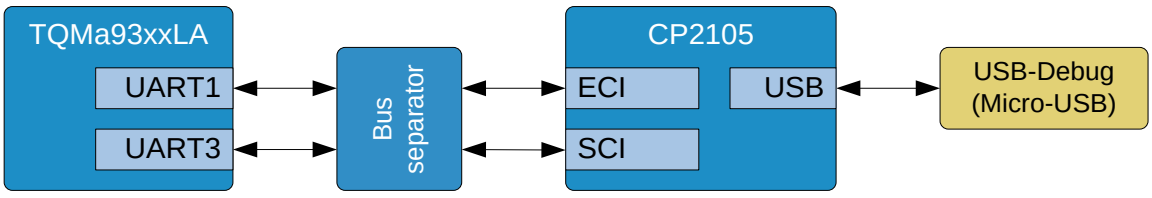


Figure 8: Block diagram USB debug

1: According to CAN standard.

Note: Connection to the host cannot be established	
	If no connection to the host can be established, the host may require drivers: https://www.silabs.com/developers/usb-to-uart-bridge-vcp-drivers

3.8.3 Ethernet

The i.MX93 processor has two independent RGMII interfaces. On the MBa93xxLA, both interfaces are used to provide two Gigabit Ethernet ports. The ENET1 interface (ENET QOS) of the CPU provides Time Sensitive Network (TSN) features and is therefore used for the TSN-capable interface. The 1588_EVENT signals of the CPU can only be multiplexed to balls of the SD2 interface. Since this is already occupied by the SD card, the EVENT signals cannot be used by default. Placement options are provided on the MBa93xxLA to make the EVENT signals of the ENET1 optionally available at the starter kit header. When using these signals, the SD Card cannot be used.
The ENET2 interface does not support TSN. The Ethernet ports are provided on two RJ45 jacks.

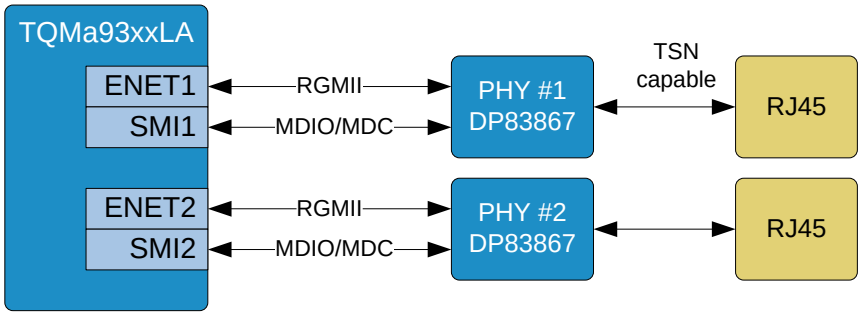


Figure 9: Block diagram Ethernet

The PHY DP83867 has configurable GPIO signals, which can be used for SFD (Start of Frame) detection outputs for debug purposes, among other things. For the TSN-enabled Ethernet interface, these pins are provided on pin header X5 on the MBa93xxLA.

Both transceivers are each connected with their own reset and interrupt signals. For the interrupt signals two GPIO signals of the TQMa93xxLA are used. For the reset signals two IO-Signals of the I2C3 port expander of the MBa93xxLA are used. The following table shows the signals used.

Table 12: Ethernet reset and interrupt signals

Ethernet port	Transceiver function	MBa93xxLA signal	TQMa93xxLA signal	MBa93xxLA I2C3 address	Remark
Ethernet 1	Interrupt output (Pin: INT)	ENET1_INT#	GPIO3_IO26	–	Low-active / pulled-up to V_1V8
	Reset input (Pin: RESET#)	ENET1_RESET#	–	0x71, IO_0	Low-active
Ethernet 2	Interrupt output (Pin: INT)	ENET2_INT#	GPIO3_IO27	–	Low-active / pulled-up to V_1V8
	Reset input (Pin: RESET#)	ENET2_RESET#	–	0x71, IO_1	Low-active

3.8.3 Ethernet (continued)

The Transceiver DP83867 has boot straps to start with configurable default values. The standard configuration on the MBa93xxLA is shown in the following table, alternatively, these can be changed via register settings or via placement options.

Table 13: Standard configuration of Ethernet transceivers (boot straps)

Config-Pin on Ethernet-Transceiver (1)	Default MBa93xxLA Mode (2)	Description
RX_D0	1	Addresses for Management Interface (SMI): Transceiver #1 - 0b0000 Transceiver #2 - 0b0000
RX_D2	1	
RX_CTRL	3	Autonegotiation enabled
GPIO_0	1	RGMII RX CLOCK SKEW = 2.0 ns
GPIO_1	1	
LED_2	1	RGMII TX CLOCK SKEW = 2.0 ns
LED_1	1	
		Mode 10/100/1000 Mbit/s available (ANEG_SEL = 0)
LED_0	1	Port Mirroring disabled, SGMII Mode disabled

The activity status of the respective Ethernet port is indicated by the LEDs in the RJ45 sockets. The table shows the default configuration. This can be adapted via register settings in the transceivers. The status messages are identical for both Ethernet ports.

Table 14: Ethernet-LEDs

LED	Colour	Function / Indication
LED left	Green	Connection is established
LED right	Yellow	Send and receive activity

3.8.4 WLAN / Bluetooth

A WLAN module (SPB228 from H&D Wireless) with integrated Bluetooth 5.0 interface is available on the MBa93xxLA. It supports IEEE 802.11 ac/a/b/g/n and offers a dual-band RF interface (2.4 / 5 GHz). The antennas have to be connected separately to the MHF4 sockets of the SPB228 and are not part of the MBa93xxLA.

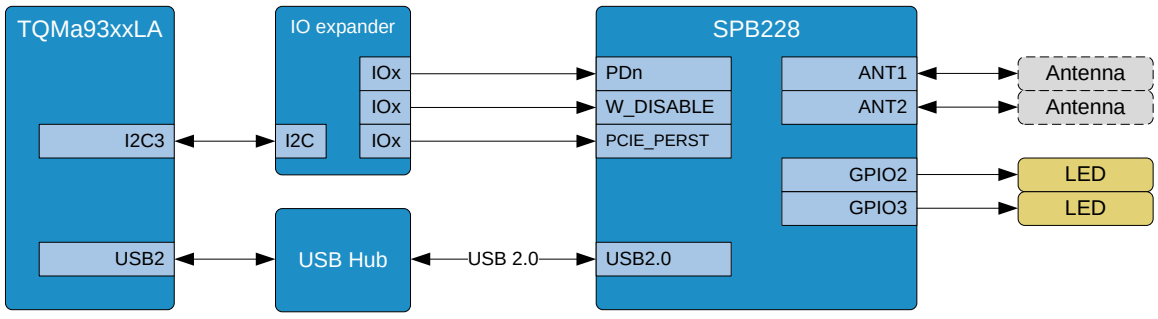


Figure 10: Block diagram WLAN / Bluetooth

The module is connected via USB 2.0. However, the theoretically achievable maximum data rate of the SPB228 of 866 Mbit/s is reduced due to the connection via USB2.0.
The host interface configuration of the SPB228 must be done for USB 2.0 as follows:

Table 15: SPB288 host interface configuration

CONFIG_HOST[2:0]	WLAN interface	Bluetooth BLE Interface	Driver Name
101	USB 2.0	USB 2.0	linux-usb-driver-228

1: Identical for both transceivers unless explicitly stated.
2: A detailed description of the modes and their configuration can be found in data sheet (5)

3.8.5 IoT interface

The BG95 module from Quectel is used to implement the IoT interface. This is an LTE module with an integrated GNSS receiver. A USB 2.0 interface of the USB hub is used as the host interface.

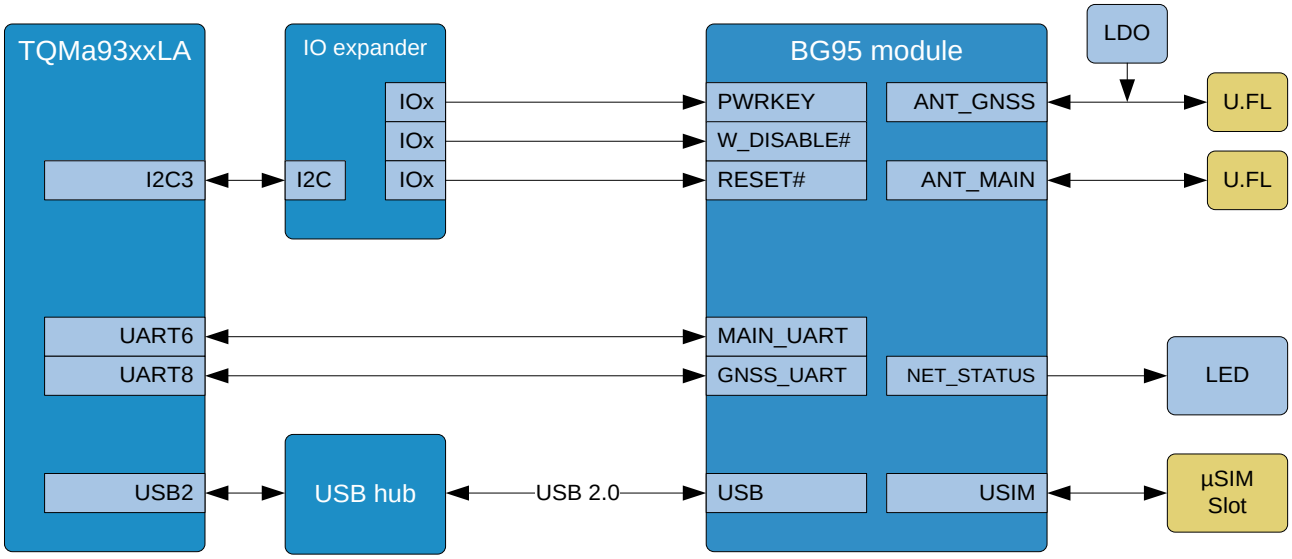


Figure 11: Block diagram IoT interface

A micro SIM card holder (X24) is implemented for contacting a SIM card. U.FL sockets (X25, X26) for connecting antennas are equipped on the mainboard. A phantom power supply for active antennas is provided at the GNSS antenna socket. The antennas are not part of the MBa93xxLA.
The Main UART as well as GNSS UART signals are connected to two UART interfaces of the TQMa93xxLA.
Due to the very limited number of available GPIO pins of the TQMa9xxxLA, the control signals are operated via I2C port expander.

3.8.6 DisplayPort

In addition to the standard LVDS interface (X12, X11), the DisplayPort connection X21 is also available on the MBa93xxLA to connect monitors. This is implemented with a DSI-to-DP-Bridge, which converts DSI ports of the TQMa93xxLA to DisplayPort.

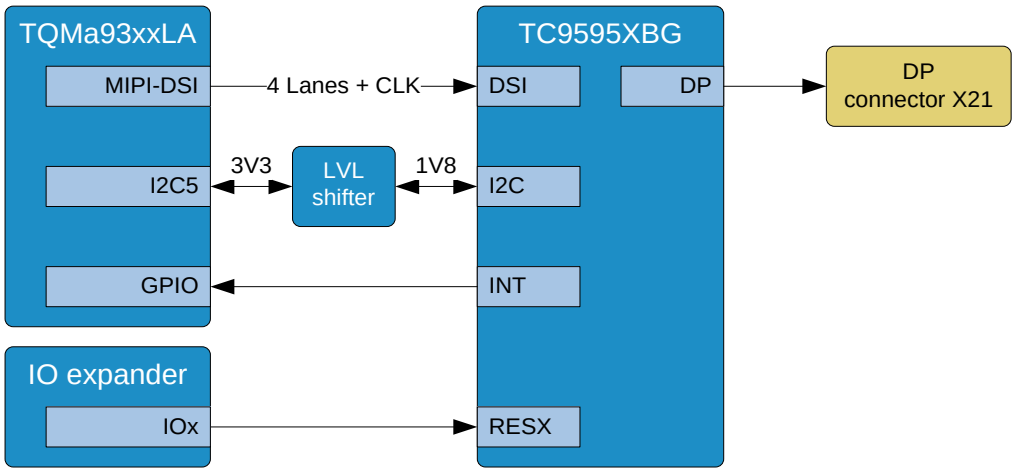


Figure 12: Block diagram DisplayPort

3.8.7 LVDS

The i.MX93 processor has an LVDS interface with four lanes. These are provided on the connector X12 on the MBa93xxLA. An additional CMD connector (X11) is also provided on the MBa93xxLA to provide supply voltages, a USB interface as well as display and backlight control signals.

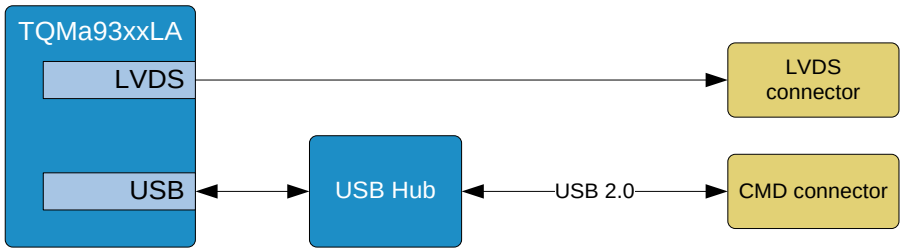


Figure 13: Block diagram LVDS

Table 16: Pinout LVDS (X12)

Pin	Signal	Dir.	Level	Remark
1	LVDS_DATA0–	O	1.8 V	LVDS interface (Lane 0)
2	LVDS_DATA0+	O	1.8 V	
3	LVDS_DATA1–	O	1.8 V	LVDS interface (Lane 1)
4	LVDS_DATA1+	O	1.8 V	
5	LVDS_DATA2–	O	1.8 V	LVDS interface (Lane 2)
6	LVDS_DATA2+	O	1.8 V	
7	GND	P	0 V	Ground
8	LVDS_CLOCK–	O	1.8 V	LVDS interface (Clock)
9	LVDS_CLOCK+	O	1.8 V	
10	LVDS_DATA3–	O	1.8 V	LVDS interface (Lane 3)
11	LVDS_DATA3+	O	1.8 V	
12	(NC)	O	1.8 V	–
13	(NC)	O	1.8 V	
14	GND	P	0 V	Ground
15	(NC)	O	1.8 V	–
16	(NC)	O	1.8 V	
17	GND	P	0 V	Ground
18	(NC)	O	1.8 V	–
19	(NC)	O	1.8 V	
20	(NC)	O	1.8 V	–
21	(NC)	O	1.8 V	
22	(NC)	O	1.8 V	–
23	(NC)	O	1.8 V	
24	GND	P	0 V	Ground
25	V_5V_LVDS	P	5 V	5 V supply voltage (1 A max. output)
26	V_5V_LVDS	P	5 V	
27	V_5V_LVDS	P	5 V	
28	V_3V3_LVDS	P	3.3 V	3.3 V supply voltage (1 A max. output)
29	V_3V3_LVDS	P	3.3 V	
30	V_3V3_LVDS	P	3.3 V	
M1, M2	GND	P	0 V	Ground

Table 17: Pinout LVDS (X11)

Pin	Signal	Dir.	Level	Remark
1	V_12V	P	12 V	12 V supply voltage (1 A max.)
2	V_12V	P	12 V	
3	V_12V	P	12 V	
4	GND	P	0 V	Ground
5	GND	P	0 V	
6	GND	P	0 V	
7	V_5V	P	5 V	5 V supply voltage (1 A max.)
8	V_5V	P	5 V	
9	GND	P	0 V	Ground
10	GND	P	0 V	
11	V_USB_H4_VBUS	P	5 V	VBUS USB Host 4 (0.5 A max.)
12	GND	P	0 V	Ground
13	USBH4_D–	I/O	3.3 V	Data USB Host 4
14	USBH4_D+	I/O	3.3 V	
15	GND	P	0 V	Ground
16	LCD_RESET#	O_{PD}	3.3 V	Reset
17	LCD_BLT_EN	O_{PD}	3.3 V	Backlight-Enable
18	LCD_PWR_EN	O_{PD}	3.3 V	Power-Enable
19	LCD_PWM	O	3.3 V	PWM Contrast-/ Brightness
20	GND	P	0 V	Ground
M1, M2	GND	P	0 V	Ground

3.8.8 MIPI CSI

The Camera Serial Interface (CSI) of the TQMa93xxLA is available with two lanes on the MBa93xxLA with the dedicated connector X13.

Figure 14: Block diagram MIPI CSI

Table 18: Pinout MIPI-CSI (X13)

Signal	Pin	Pin	Signal
GND	1	2	GND
MIPI_CSI_EN_1V8	3	4	(NC)
MIPI_CSI_RST_1V8#	5	6	(NC)
MIPI_CSI_TRIGGER_1V8	7	8	(NC)
MIPI_CSI_SYNC_1V8	9	10	(NC)
(NC)	11	12	(NC)
GND	13	14	GND
(NC)	15	16	(NC)
(NC)	17	18	(NC)
GND	19	20	GND
(NC)	21	22	(NC)
(NC)	23	24	(NC)
GND	25	26	GND
MIPI_CSI_D1-_L	27	28	(NC)
MIPI_CSI_D1+_L	29	30	(NC)
GND	31	32	GND
MIPI_CSI_D0-_L	33	34	(NC)
MIPI_CSI_D0+_L	35	36	(NC)
GND	37	38	GND
MIPI_CSI_CLK-_L	39	40	(NC)
MIPI_CSI_CLK+_L	41	42	(NC)
GND	43	44	GND
I2C5_SDA_1V8	45	46	(NC)
I2C5_SCL_1V8	47	48	(NC)
GND	49	50	(NC)
CLK3_OUT	51	52	(NC)
GND	53	54	GND
(NC)	55	56	V_V5_MB
(NC)	57	58	V_V5_MB
(NC)	59	60	V_V5_MB

3.8.9 Analog frontend

The analog front end is implemented with the NXP NAFE13388, which is connected to the TQMa93xxLA via SPI. This provides a total of 8 analog inputs. The NAFE13388 is a high precision and very flexible configurable analog-to-digital converter with integrated 24-bit delta-sigma converter. The measurement inputs can be used as single-ended or differential inputs and offer various configuration options for measuring voltage, current, resistance and thermocouples.

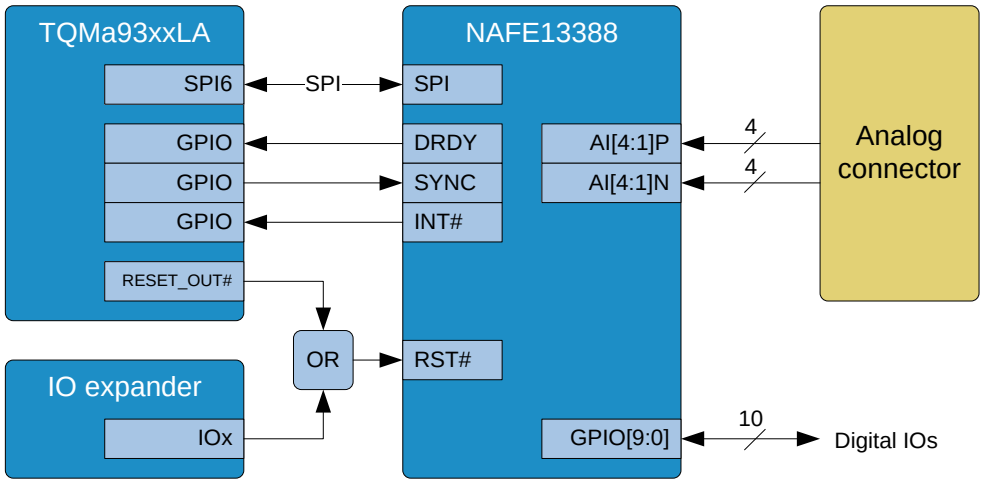


Figure 15: Block diagram Analog frontend

Due to the limited number of available GPIO pins of the TQMa93xxLA, the integrated GPIO pins of the NAFE13388 are used to connect the digital IO expansion. Through the fast SPI interface, the IO signals can be operated in high-speed mode, in contrast to a connection via I2C IO expander.

3.8.10 Digital IO expansion

The IO expansion has 4 digital inputs and 4 digital outputs with external 24 V supply.
The external supply via connector X27 is provided with a protective circuit against overcurrent, overvoltage as well as reverse polarity.
There is a mounting option to provide the internal 24 V to the highside switches.

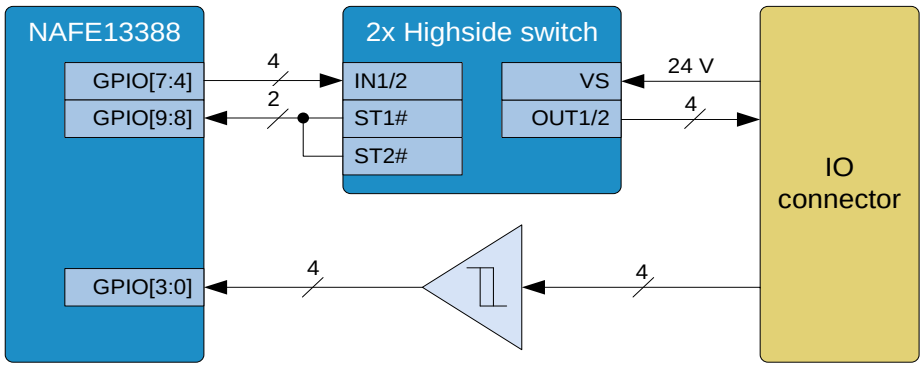


Figure 16: Block diagram Digital IO expansion

For the digital inputs a circuit with logic gates with Schmitt trigger inputs is implemented.
Due to the very limited number of available GPIO pins of the TQMa93xxLA, the GPIO signals of the inputs and outputs are connected to the integrated GPIO pins of the NAFE13388 of the analog front end. Through the fast SPI interface, the IO signals can be operated in high-speed mode, in contrast to a connection via I2C IO expander.

Table 19: IO threshold range

Threshold	min.	typ.	max.
positiv	-	11,25 V	13,86 V
negativ	3,35 V	6,19 V	-

3.8.11 USB Type-C

TQMa93xxLA has a USB Type-C interface. The VBUS switch is controlled by a corresponding USB Power Delivery Controller. VBUS is used on the MBa93xxLA only as source (supply of an external device), not as sink (supply of mainboard from VBUS). The current limitation is fixed at approx. 500 mA.

This interface is connected to the USB1 port of the i.MX93. The Serial Download Mode is possible.

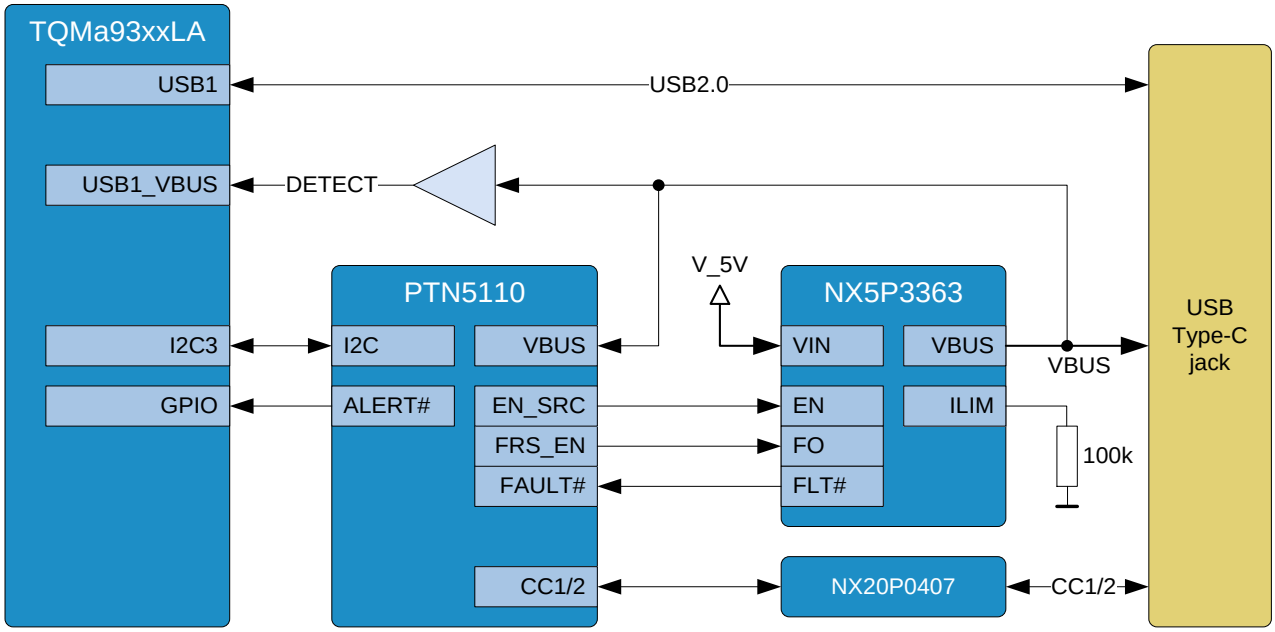


Figure 17: Block diagram USB Type-C

3.8.12 Micro-SD card

The micro SD card connector is directly connected to the uSDHC2 interface of the TQMa93xxLA. A 4-bit wide data interface is used. The uSDHC controller in the i.MX93 supports UHS-I mode.

The switching of the IO voltage is performed by the module-internal signal SD2_VSELECT. No measures are necessary on the mainboard for this. The SD card is supplied with V_3V3_SD, which is provided by the TQMa93xxLA.

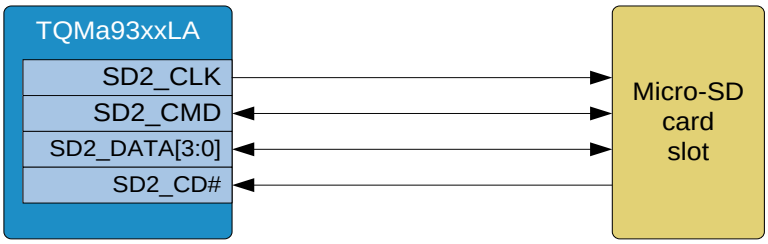


Figure 18: Block diagram Micro-SD card

3.8.13 RS485

On the MBa93xxLA a RS485 interface (halfduplex) is realized. This interface is not galvanically isolated. It is connected to the UART2 interface of the TQMa93xxLA. The RTS signal of the UART interface (possibly used as GPIO) is used for automatic direction switching.

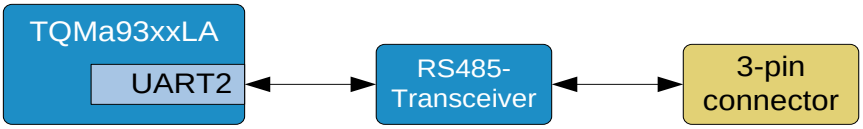


Figure 19: Block diagram RS485

The bus termination for RS485 is done via DIP switch S6. By default the termination components are equiped to use it for RS485 bus. There is a assembly option to use a Profibus compliant termination. The assembly option is documented in the MBa93xxLA schematic.

The RS485 Bus is provided at a 3-pin connector.

Table 20: Pinout RS485 (X10)

Pin	Signal
1	RS485_A
2	RS485_B
3	GND

Table 21: Termination switch S6

S6-1	S6-2	Modus
OFF	OFF	No bus termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Bus terminated

3.8.14 Extension header X1

The MBa93xxLA provides a 50 mil header with 30 pins. Some unused signals are made available on these.

Besides the signals, 1.8 V, 3.3 V and 5 V are available on the header. The maximum current is divided among the pin header as well as the connectors of LVDS, MIPI-CSI and display port. In total, no more than the specified maximum current may be drawn at the following interfaces:

Table 22: Power consumption headers

Rail	I_{max}	Remark
V_5V_MB	1,5 A	Sum of currents at X1, X11, X12 and X13
V_3V3	1 A	Sum of currents at X1, X12 and X21
V_1V8	250 mA	Sum of currents at X1

Note: Observe power consumption with regard to the overall system	
	The supply voltages (1.8 V, 12 V, etc.) provided at the MBa93xxLA headers are not individually fused. Technically, an overload of the fuse at the 24 V supply input is therefore possible, see also chapter 3.10. Please note the resulting total current consumption of the MBa93xxLA, which must be less than 4 A!

Table 23: Pinout header X1

Level	Signal	Pin		Signal	Level
5 V	V_5V_MB	1	2	V_3V3_MB	5 V
0 V	GND	3	4	V_1V8	1.8 V
1.8 V	ADC_IN0	5	6	GND	0 V
1.8 V	ADC_IN1	7	8	TAMPER0	1.8 V
1.8 V	ADC_IN2	9	10	TAMPER1	1.8 V
1.8 V	ADC_IN3	11	12	RESET_OUT#	3.3 V
0 V	GND	13	14	PMIC_RST#	1.8 V
3.3 V	SAI3_TXFS	15	16	PMIC_WDOG_IN#	3.3 V
3.3 V	SAI3_TXD0	17	18	WDOG_ANY	3.3 V
3.3 V	SAI3_TXC	19	20	M33_NMI	3.3 V
3.3 V	SAI3_RXFS	21	22	ENET1_EVENT0_IN	V_SD2
3.3 V	SAI3_RXD0	23	24	ENET1_EVENT0_OUT	V_SD2
3.3 V	SAI3_RXC	25	26	GND	0 V
0 V	GND	27	28	I2C3_SDA	3.3 V
3.3 V	SAI3_MCLK	29	30	I2C3_SCL	3.3 V

3.8.15 JTAG

The JTAG interface is routed to a 10-pin header (X20). The required pull-ups of the lines TDI, TMS, and SRST# are available on the MBa93xxLA. All signal lines use 1.8 V as reference voltage. The JTAG interface is not ESD protected.

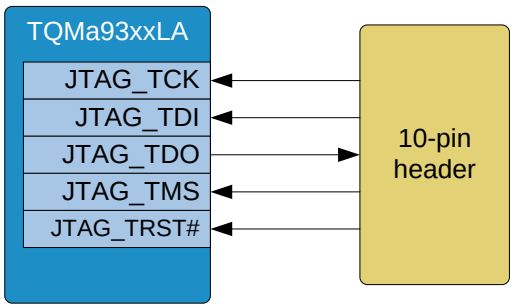


Figure 20: Block diagram JTAG

Table 24: Pinout JTAG (X20)

Remark	Level	Dir.	Signal	Pin	Pin	Signal	Dir.	Level	Remark
Test Mode Select	1.8 V	I_{PU}	JTAG_TMS	2	1	V_1V8	P	1.8 V	1.8 V
Test Clock	1.8 V	I_{PD}	JTAG_TCK	4	3	GND	P	0 V	Ground
Test Data Out	1.8 V	O	JTAG_TDO	6	5	GND	P	0 V	Ground
Test Data In	1.8 V	I_{PU}	JTAG_TDI	8	7	(NC)	–	–	Not used
System Reset	1.8 V	I/O_{PU}	JTAG_SRST#	10	9	GND	P	0 V	Pulled to ground

3.9 User interfaces

3.9.1 Reset button

Reset button S2 resets the PMIC and CPU on the TQMa93xxLA. The generated reset signal simultaneously activates the RESET_OUT# signal, which also resets various components on the MBa93xxLA.

3.9.2 On/Off button

Button S3 is directly connected to pin ONOFF of the TQMa93xxLA. Pressing the button triggers the ON/OFF function of the i.MX 93.

3.9.3 GPI buttons

Two buttons (S8, S9) are available on the MBa93xxLA for user-specific use. They are connected to the IO expander.

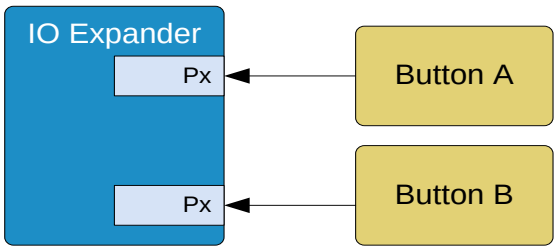
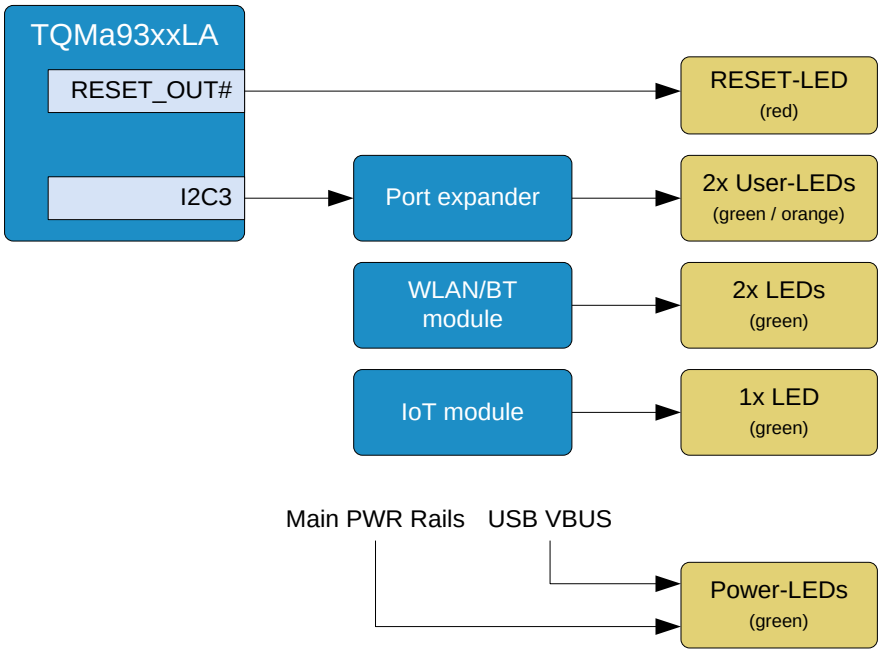


Figure 21: Block diagram GPI buttons

Table 25: General Purpose buttons

Button	Signal
S8	Button_A#
S9	Button_B#

3.9.4 Status LEDs



In addition to the status LEDs of the two Ethernet sockets, the MBa93xxLA provides more indicator LEDs:

Table 26: Status-LEDs

Function group	LED	Colour	Indication
Reset	V1	Red	Indicates the reset status of the des TQMa93xxLA (at signal RESET_OUT#)
USB	V5	Green	Indicates the presence of VBUS for USB Host 1
	V6	Green	Indicates the presence of VBUS for USB Host 2
	V12	Green	Indicates the presence of VBUS for USB Host 7 (LVDS-CMD)
	V7	Green	Indicates the presence of VBUS for USB Type C
Ethernet	X6	Green/yellow	Shows the status of Link/Activity
	X7	Green/yellow	Shows the status of Link/Activity
WLAN	V8	Green	Shows the status of the WLAN# signal on the WLAN/Bluetooth module
Bluetooth	V9	Green	Shows the status of the BT# signal on the WLAN/Bluetooth module
IoT	V10	Green	Shows the status of network on the IoT module
User LEDs	V2	Green	Programmable LED (User LED1) on I²C GPIO Expander (1)
	V3	Yellow	Programmable LED (User LED2) on I²C GPIO Expander (1)
SD Card	V4	Green	Indicates the presence of the internal 3.3 V supply voltage (V_3V3_SD)
Power (2)	V14	Green	Indicates the presence of the external 24 V supply voltage (V_24V)
	V15	Green	Indicates the presence of the internal 12 V supply voltage (V_12V)
	V16	Green	Indicates the presence of the internal 5 V supply voltage (V_5V)
	V17	Green	Indicates the presence of the internal 5 V supply voltage (V_5V_MB)
	V18	Green	Indicates the presence of the internal 3.3 V supply voltage (V_3V3)
	V19	Green	Indicates the presence of the internal 1.8 V supply voltage (V_1V8)
	V20	Green	Indicates the presence of the internal 5 V supply voltage (V_3V8)
Debug	V13	Green	Indicates the presence of an external USB supply voltage

3.10 Power supply

The MBa93xxLA must be supplied with 24 V DC (typ.) via connector X23 (Phoenix Contact MC 1,5/ 2-GF-3,5 LR).

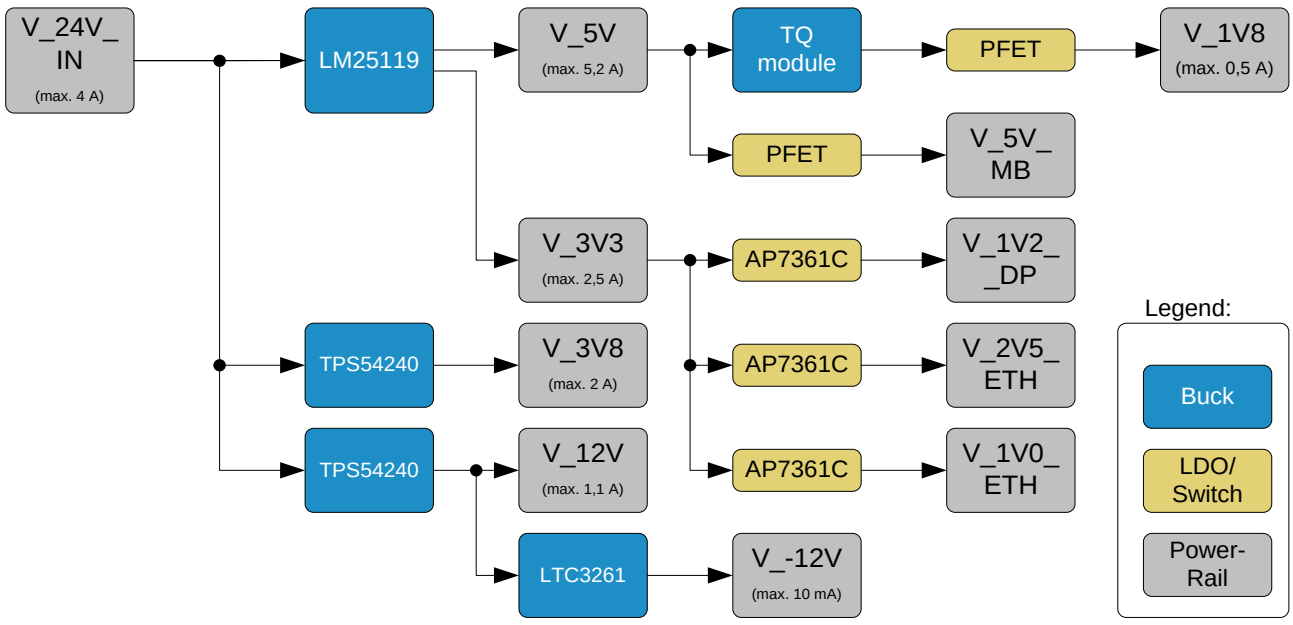


Figure 22: Block diagram MBa93xxLA power supply

1: For further information, see chapter 3.4.
2: For details on the supply concept and the distribution of the internal supply voltages, refer to chapter 3.10.

Figure 22 shows all voltages (rails) on the MBa93xxLA, which are divided into three main paths consisting of one LM25119 and two TPS54240. These supply the largest loads (TQMa93xxLA, USB supply, IoT module, 12 V display supply)
The design also allows power sequencing of all voltage levels used. With the exception of V_5V, all voltages are switched on after the TQMa93xxLA boots. A 1.8 V supply is already provided by the TQMa93xxLA and delivers up to 500 mA.

3.10.1 Input protection

The following protective circuits are provided for the input voltage V_24V of the MBa93xxLA:

- Fuse 5 A, slow blow
- Overvoltage protection
- PI Filter (CLC element)
- Reverse polarity protection
- Voltage stabilization

Figure 23: Block diagram Power-In

Attention: Voltages at headers	
	The internal voltages (1.8 V, 12 V, etc.) provided at the MBa93xxLA headers are not separately fused. Technically an overload of the fuse is therefore possible. The resulting total current consumption of the MBa93xxLA should be kept below 4 A in total.

Table 27: Supply voltage V_24V_IN at Power-In (X23)

Parameter	Min.	Typ.	Max.	Remark
Input voltage	16 V	24 V	30 V	–
Power consumption	–	TBD (1)	TBD (2)	–
Rated current of the fuse	–	5 A	–	–
Voltage limitation in case of overvoltage	TBD	–	TBD	Note: The MBa93xxLA may be damaged in case of permanent overvoltage!

Table 28: Pinout Power-In (X23)

Pin	Pin	Signal	Type	Level	Remark
X23	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground

1: Typical scenario is not defined.
2: Theoretical full load. All supply voltages are loaded with maximum current, e.g. by connecting additional load to the pin headers, and all system components have maximum power consumption.

3.10.2 Power sequencing

The following figure shows the power-on sequences of the different voltage levels of the main board, without taking into account the rise times of the voltages:

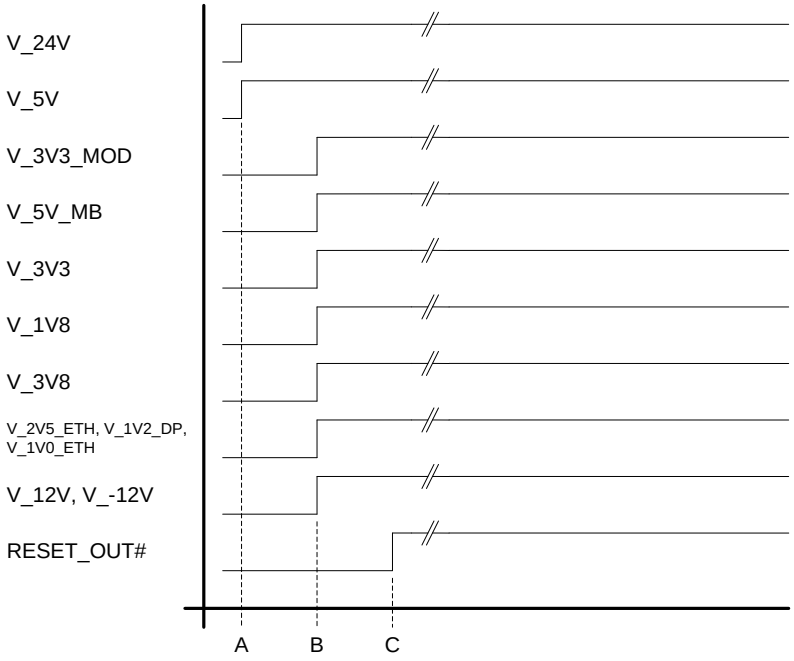


Figure 24: Power sequencing MBa93xxLA

The following table shows the sequence steps from Figure 24:

Table 29: Power sequencing

Sequence	Time	Description
A	–	Start point: Power-up MBa93xxLA supplies.
B	174…494 ms (t_B)	Release MBa93xxLA supplies by V_3V3_MOD as last part of the internal power sequence of the TQMa93xxLA.
C	t_B + 22 ms	Release RESET_OUT# after completion of TQMa93xxLA power sequencing plus preconfigured delay.

V_3V3_MOD controls the second regulator of the LM25119 (V_3V3) as well as the power FET for V_5V_MB and V_1V8 by means of supervisor. Automatically the three AP7361 for V_1V0_ETH, V_2V5_ETH and V_1V2_DP are activated.

Determined by the internal power sequence of the TQMa93xxLA, RESET_OUT# is only released with a corresponding time offset (22 ms) after the last voltage level V_3V3_MOD (TQMa93xxLA internal V_3V3) is switched on. Thus all necessary voltages on the TQMa93xxLA and the carrier board are stable when the system starts.

3.10.3 V_5V and V_3V3

3.3 V and 5 V are required to supply the TQMa93xxLA, some components on the mainboard and the USB voltage. The dual regulator LM25119 is used for this purpose, which generates the two voltages from the 16...30 V input voltage.
The voltage V_5V is automatically activated when the mainboard supply is switched on and supplies the TQMa93xxLA. V_3V3 is activated after completion of the module-internal power sequencing with the V_3V3_MOD provided by the module by means of supervisor (LM25119 pin EN2). The designs have the following specification:

Table 30: Specifications V_5V and V_3V3

Voltage	Parameter	Value	Remark
V_5V	V_{IN}	16…30 V	V_24V
	V_{OUT}	4.91…5.08 V	V_5V
	I_{OUT}	5.0 A	Load: 4.72 A (realistic use case)
V_3V3	V_{IN}	16…30 V	V_24V
	V_{OUT}	3.25…3.35 V	V_3V3
	I_{OUT}	2.8 A	Load: max. 2.65 A (realistic use case)

3.10.4 V_5V_MB

Besides the TQMa93xxLA, the mainboard needs a 5 V supply for some components. This voltage V_5V_MB is switched on after completion of the module-internal power sequencing.
Components whose power is not switched via separate enable signals are supplied from V_5V_MB. The power distribution switches for USB is powered directly from V_5V.

3.10.5 V_1V8

Because the power requirement by the components on the mainboard for 1.8 V is very low, the 1.8 V provided by the TQMa93xxLA is used for V_1V8. The module supplies up to 500 mA. A maximum of 250 mA of this remains for the header X1. As the 1.8 V are switched on by the module at an early stage in sequencing, they must be activated with a delay for the mainboard components. Otherwise, the power timing of the Ethernet PHYs and the DisplayPort bridge will be violated.

3.10.6 V_1V0_ETH

The voltage of 1.0 V required for the Ethernet PHYs is generated from V_3V3.

Table 31: Specification V_1V0_ETH

Voltage	Parameter	Value	Remark
V_1V0_ETH	V_{IN}	3.25…3.35 V	V_3V3
	V_{OUT}	0.97…1.03 V	V_1V0_ETH
	I_{OUT}	250 mA	

3.10.7 V_1V2_DP

The voltage of 1.2 V required for the DSI-to-DP bridge is generated from V_3V3.

Table 32: Specification V_1V2_DP

Voltage	Parameter	Value	Remark
V_1V2_DP	V_{IN}	3.25…3.35 V	V_3V3
	V_{OUT}	1.18…1.22 V	V_1V2_DP
	I_{OUT}	250 mA	Load: max. 190 mA

3.10.8 V_2V5_ETH

The Ethernet PHYs need among others a supply of 2.5 V, which is generated for both PHYs from V_3V3. The supply of the PHYs is thus automatically started after the boot process.

Table 33: Specification V_2V5_ETH

Voltage	Parameter	Value	Remark
V_1V2_DP	V_{IN}	3.25…3.35 V	V_3V3
	V_{OUT}	2.44…2.56 V	V_2V5_ETH
	I_{OUT}	320 mA	Load: max. 170 mA

3.10.9 V_3V8

A voltage of 3.8 V with load peaks of up to 2 A is required for the IoT module. The voltage is generated from V_24V via a step-down converter. The controller can be switched on or off via GPIO signal by software.
The design has the following specification:

Table 34: Specification V_3V8

Voltage	Parameter	Value	Remark
V_3V8	V_{IN}	16…30 V	V_24V
	V_{OUT}	3.695…3.929 V	V_3V8
	I_{OUT}	2 A	–

3.10.10 V_12V

A voltage of 12 V is required for the backlight supply at the LVDS as well as the analog frontend, which is specified with 1.1 A in total. The voltage is generated from V_24V by a step-down converter.
The design has the following specification:

Table 35: Specification V_12V

Voltage	Parameter	Value	Remark
V_12V	V_{IN}	16…30 V	V_24V
	V_{OUT}	11.660…12.471 V	V_12V
	I_{OUT}	1.1 A	

3.10.11 V_-12

The analog frontend requires a negative voltage of -7...-32 V. Therefore a voltage of -12 V is generated from V_12V by the LTC3261 charge pump.

3.11 Reset & Configuration

Figure 25 shows the reset structure on the MBa93xxLA.

In addition to the reset signals of the TQMa93xxLA, the MBa93xxLA also provides further software-controlled reset signals for individual function blocks, e.g. ENET reset for the Ethernet transceivers. These are implemented by GPIO signals and named accordingly in the respective chapters when applicable.

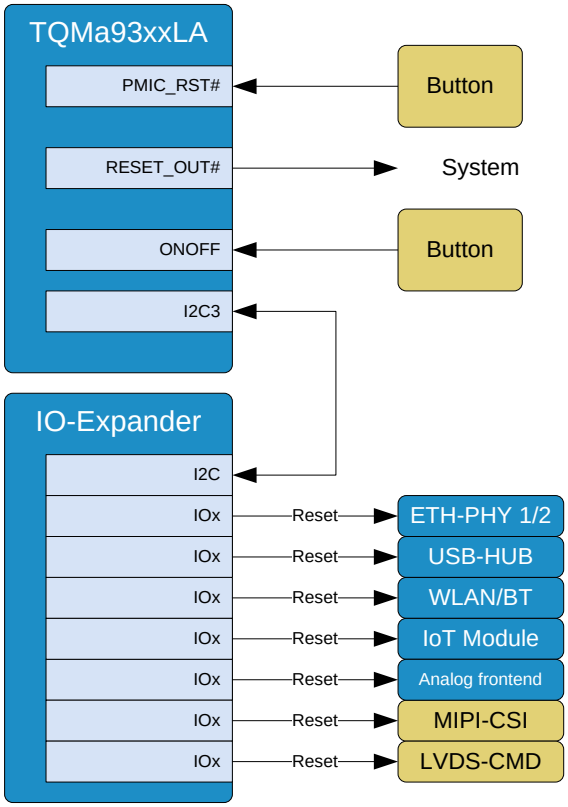


Figure 25: Block diagram Reset & Configuration

The following signals from the TQMa93xxLA are used on the MBa93xxLA:

Table 36: Reset signals

Signal	Type	Level	Remark
PMIC_RST#	I	1.8 V	• activates RESET of the PMIC (low-active) • reset behavior of PMIC configurable (see data sheet) • no pull-up on mainboard necessary • connect to GND for activation (push button)
RESET_OUT#	O	-	• open drain output (low-active) • activates RESET of mainboard components • requires pull-up on mainboard (max. 5.5 V)
ONOFF	I	1.8 V	• ON/OFF function of the i.MX93 (see data sheet) • no pull-up on mainboard necessary • connect to GND to activate (push button)

Pushbuttons are connected to PMIC_RST# and ONOFF.

RESET_OUT is connected with a pull-up to V_3V3 and resets followed blocks:

- IO Expander
- Analog switch for boot mode signals
- Analog frontend (parallel to reset via IO expander for resetting the digital outputs)
- External components at starter kit headers

The reset signal is linked to an LED.

4. SOFTWARE

No software is required for the MBa93xxLA.
Suitable software is only required on the TQMa93xxLA and is not a part of this User's Manual.
More information can be found in the TQ-Support Wiki for the TQMa93xx.

5. MECHANICS

5.1 MBa93xxLA dimensions

The MBa93xxLA has overall dimensions (length × width × height) of 160 mm × 100 mm × TBD mm.
The MBa93xxLA has four 4.2 mm mounting holes for the housing, and four 2.7 mm mounting holes for a heat sink.
The MBa93xxLA weighs approximately TBD grams.

5.2 Embedding in the target system

The MBa93xxLA serves as a design base for customer products, as well as a reference platform during development.

5.3 Housing

The form factor and the mounting holes of the MBa93xxLA are designed for installation in a standard Eurocard housing.

5.4 Thermal management

The largest power dissipation on the MBa93xxLA is caused by the voltage regulators. In addition, the TQMa93xxLA is a heat source that acts indirectly on the MBa93xxLA. Depending on the application, further power dissipation can occur, mainly at additional external loads on the pin headers on the MBa93xxLA, etc.
For evaluation of the TQMa93xxLA under high load conditions an optional heat sink is provided. Four holes are provided on the MBa93xxLA for this purpose.

Attention: TQMa93xxLA heat dissipation	
	The i.MX 93 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa93xxLA must be taken into consideration when connecting the heat sink. The TQMa93xxLA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa93xxLA or the MBa93xxLA and thus malfunction, deterioration or destruction.

5.5 Assembly & Labels

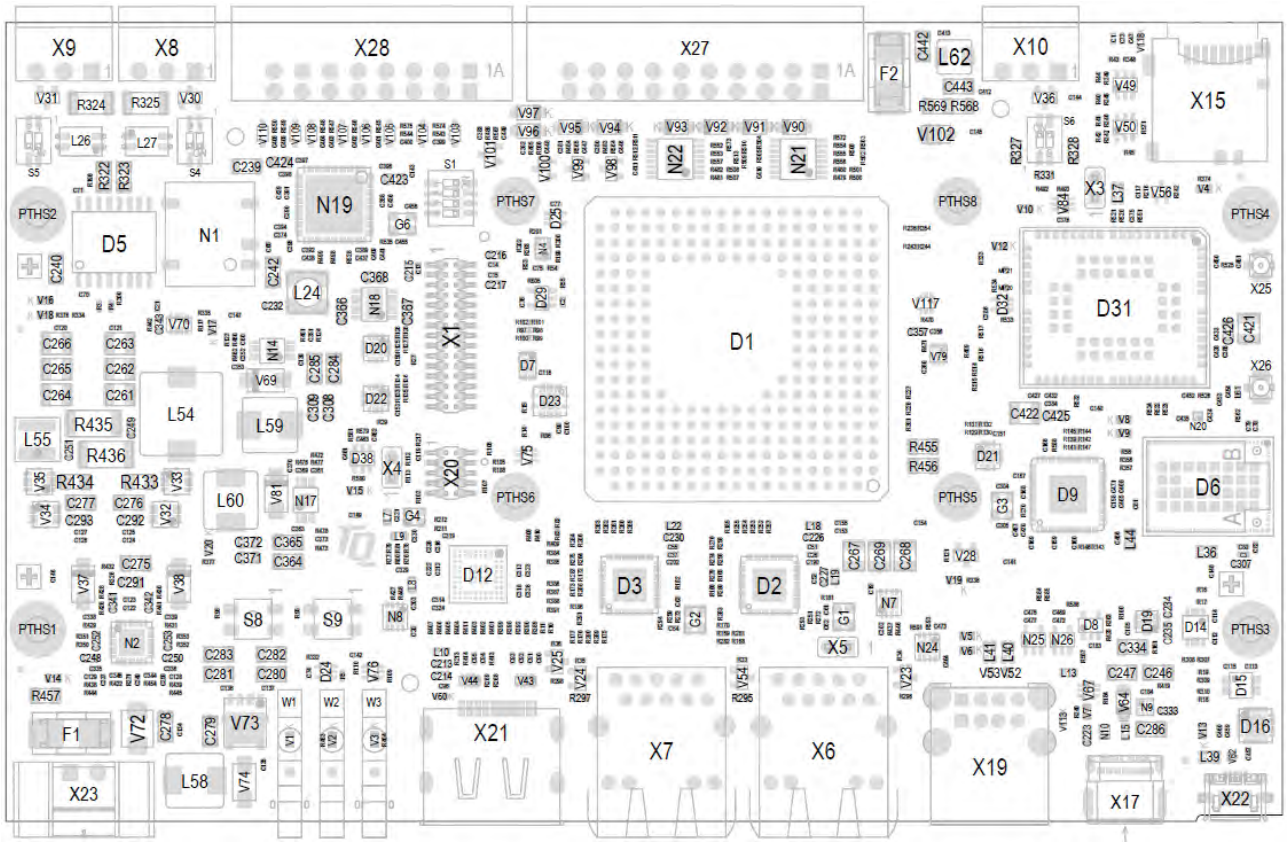


Figure 26: MBa93xxLA top view

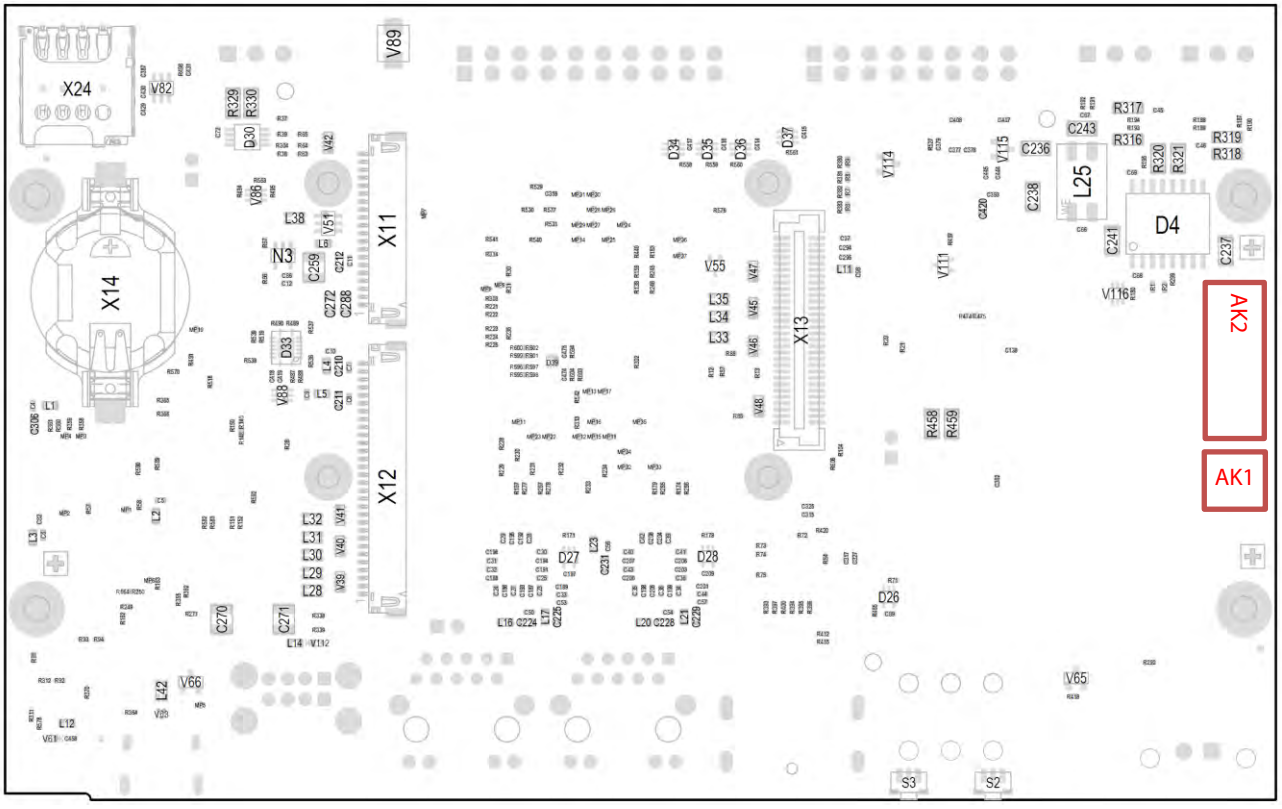


Figure 27: MBa93xxLA bottom view and label position

The labels on the MBa93xxLA show the following information:

Table 37: Labels on MBa93xxLA

Label	Content
AK1	Serial number
AK2	MBa93xxLA version and revision, tests performed

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBa93xxLA is a development platform, no EMC tests have been performed.
During the development of the MBa93xxLA the standard DIN EN 55022:2010 limit class A was taken into account.

6.2 ESD

ESD protection is provided on most interfaces of the MBa93xxLA.
The MBa93xxLA schematics show, which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 38: Climatic and operational conditions MBa93xxLA

Parameter	Range	Remark
Ambient temperature	–20 °C to +70 °C	With Lithium battery
	–25 °C to +85 °C	Without Lithium battery
Storage temperature	–40 °C to +70 °C	With Lithium battery
	–40 °C to +100 °C	Without Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa93xxLA heat dissipation	
	The i.MX 93 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa93xxLA must be taken into consideration when connecting the heat sink. The TQMa93xxLA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa93xxLA and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa93xxLA. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa93xxLA.
The MBa93xxLA is designed to be insensitive to vibration and impact.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa93xxLA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa93xxLA was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa93xxLA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa93xxLA enable compliance with EuP requirements for the MBa93xxLA.

8.5 Packaging

The MBa93xxLA is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

For technical reasons a battery is necessary for the MBa93xxLA. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa93xxLA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa93xxLA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 39: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AI	Analog Input
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CLC	Capacitor-Inductor-Capacitor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communication
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
I_{PD}	Input with Pull-Down
I_{PU}	Input with Pull-Up
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display

9.1 Acronyms and definitions (continued)

Table 39: Acronyms (continued)

Acronym	Meaning
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures
NAND	Not-And (flash memory)
(NC)	Not Connected
NOR	Not-Or
NP	Not Placed
O_{OD}	Open-Drain Output
O_{PD}	Output with Pull-Down
O_{PU}	Output with Pull-Up
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PD	Pull-Down
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media-Independent Interface
SIM	Subscriber Identification Module
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 40: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX93 Industrial Application Processors Data Sheet Rev. E	June 2022	NXP
(2)	i.MX93 Hardware Developer's Guide	TBD	NXP
(3)	i.MX 93 – Reference Manual	TBD	NXP
(4)	i.MX 93 – Mask Set Errata	TBD	NXP
(5)	Ethernet Transceiver DP83867– Data Sheet	December 2019	TI
(6)	TQMa93xxLA User's Manual	– current –	TQ-Systems
(7)	TQMa93xxLA Support Wiki	– current –	TQ-Systems

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