MBa8x
User's Manual

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1. ABOUT THIS MANUAL

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1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: info@tq-group.com
Web: www.tq-group.com

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa8x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8x schematics
- TQMa8x User's Manual
- i.MX 8 Data Sheet
- i.MX 8 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8x

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa8x as of revision 02xx. The MBa8x is designed as a carrier board for the TQ-Minimodule TQMa8x and essentially serves as a design basis for customer-specific product ideas, as well as a platform to support development. CPU features and interfaces can be evaluated, software development for a TQMa8x based project can start immediately.

Core of the MBa8x is the TQMa8x with an NXP i.MX 8 CPU. Currently two i.MX 8 derivatives are supported:

1. i.MX 8QuadPlus (1 × Cortex®-A72, 4 × Cortex®-A53)
2. i.MX 8QuadMax (2 × Cortex®-A72, 4 × Cortex®-A53)

The TQMa8x connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, etc., all other available signals of the TQMa8x are routed on 100 mil standard pin headers on the MBa8x.

2.1 MBa8x block diagram

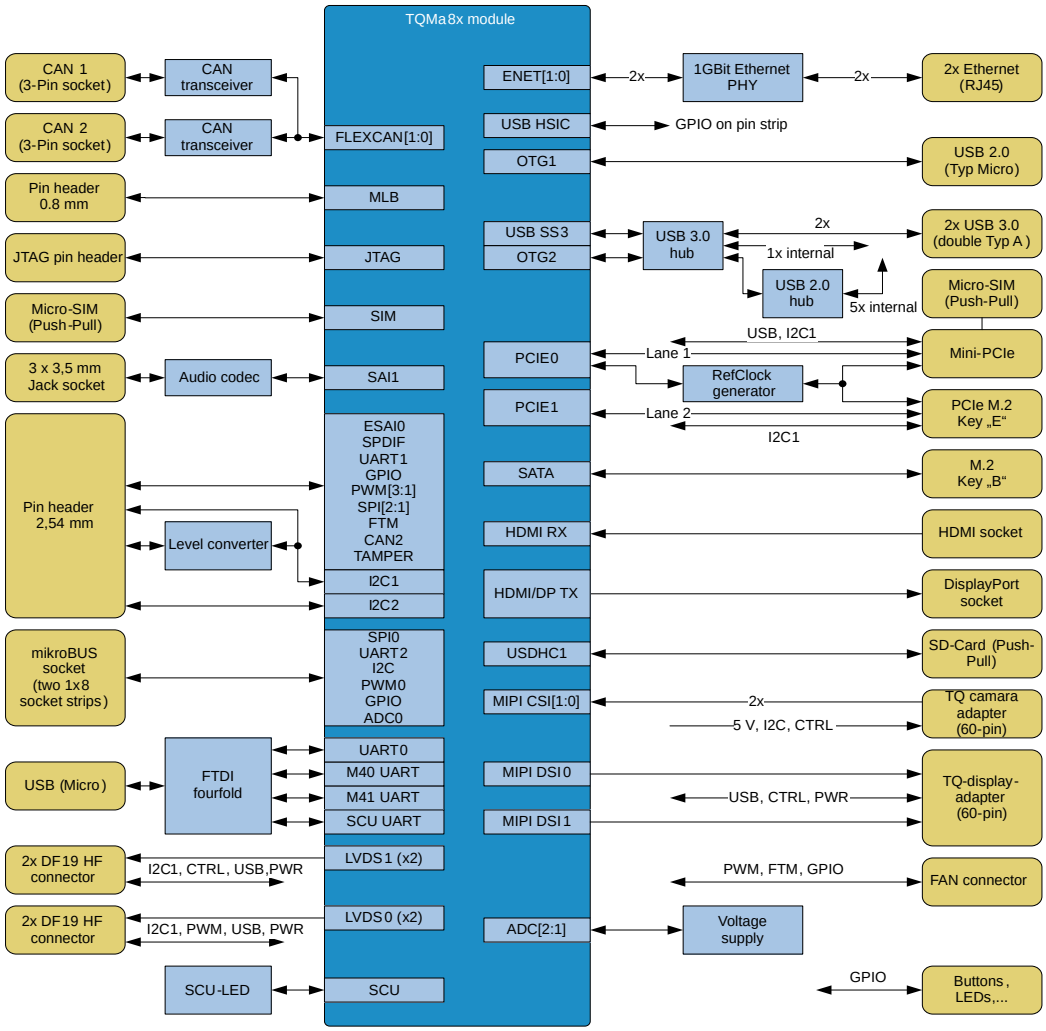

Figure 1: Block diagram MBa8x

2.2 MBa8x interfaces

The following interfaces and auxiliary functions are provided on the MBa8x:

Table 2: MBa8x interfaces and auxiliary functions

Interface	Connector	Type
Audio	X15 X16 X17	3.5 mm jack MIC (mono, pink) Line-in (stereo, blue) Line-out (stereo, green)
CAN-FD	X18, X19	3-pin, Phoenix (galvanically isolated)
Coin cell	X56	CR2032 holder
External battery	X55	2-pin, header, optional
V_LICELL ⇔ V_BAT	X23	2-pin, header
USB debug	X28	USB, Micro AB
DisplayPort	X43	DisplayPort connector
Ethernet, 1000 Base-T	X39, X40	RJ-45, integrated magnetics
LVDS0	X11	30-pin, DF19G
LVDS0 CMD	X7	20-pin, DF19G
LVDS1	X8	30-pin, DF19G
LVDS1 CMD	X4	20-pin, DF19G
MIPI CSI	X57	60-pin, Board-to-Board, header
mPCIe	X45	Mini PCIe slot (USB included)
	X46	SIM card slot
Power In	X13	DC jack (2.5 mm / 5.5 mm)
	X14	2-pin screw terminal block
SD card (UHS-Modes up to 52 MHz)	X42	Micro SD (Push-Pull type)
USB 2.0 Hi-Speed Host	X4, X7, X45, X47	2 × 20-pin, DF19G, mPCIe, PCIe M.2
USB 2.0 Hi-Speed OTG	X29	USB, Micro AB
USB 3.0 SS Host	X36	2 x USB, stacked Type A (max. 900 mA per port)
SATA M.2	X48	M.2, B key
PCIe M.2	X47	M.2, E key
HDMI-In	X44	HDMI connector
MIPI DSI	X60	60-pin, Board-to-Board, receptacle
MLB	X21	40-pin, Board-to-Board, header
mikroBUS®	D29	2 × 8-pin, 100 mil
Fan	X24	4-pin, 100 mil, friction lock
Extension header 1	X62	40-pin, 100 mil (see chapter 3.2.13)
Extension header 2	X63	40-pin, 100 mil (see chapter 3.2.13)
Extension header 3	X61	40-pin, 100 mil (see chapter 3.2.13)
Extension header 4	X64	40-pin, 100 mil (see chapter 3.2.13)

The MBa8x provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	9 × Green LED	Power LEDs (24 V, 12 V, 5 V-Mainboard, 5 V-Modul, 3,3 V, 3,3 V-Mainboard, 3,3 V-Modul, 1,8 V, 3,3 V-MPCIe, 1,5 V-MPCIe)
	3 × Green LED	2 × VBUS USB Host, 1 × VBUS USB OTG
	1 × Green LED	Debug LED for USB debug interface
	2 × Green LED	GP LEDs at port expander
	1 x Orange LED	GP LED of SCU
	3 × Green LED	WWAN, WLAN, WPAN
	1 x Green LED	SATA-M.2
	2 x Green LED	PCIe-M.2
	1 × Red LED	Reset LED
	2 × Green / Yellow LED	Ethernet LEDs (Activity / Speed)
Temperature sensor	1 × SE97BTP	Digital I²C temperature sensor
Power / Reset buttons	3 × Push button	RESET-IN#, PMIC_PWRON, IMX_ONOFF
GP buttons	2 × Push button	GP push buttons at port expander
Boot-Mode configuration	1 × 6-fold DIP switch	Boot-Mode configuration
CAN-FD/RS485 termination	2 × 2-fold DIP switch	–
JTAG	1 × 20-pin, 100 mil header	–

3. ELECTRONICS

3.1 MBa8x functional groups

The following chapters describe the interfaces on the MBa8x as of revision 02xx in connection with a TQMa8x with maximum configuration.

3.2 TQMa8x

The TQMa8x is the central system on the MBa8x. It provides LPDDR4 SDRAM, eMMC, NOR flash, RTC, an EEPROM, power supply and power management functionality.

All TQMa8x internal voltages are derived from the 5 V supply voltage. All functionally relevant pins of the CPU are routed to the TQMa8x connectors. This enables the user to use the TQMa8x with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa8x User's Manual.

On the MBa8x the standard interfaces like USB, Ethernet, etc., provided by the TQMa8x are routed to industry standard connectors. All other signals and buses provided by the TQMa8x are routed to 100 mil headers.

The boot behaviour of the TQMa8x can be configured. The Boot-Mode configuration is set by a DIP switch on the MBa8x, see chapter 3.1.1.3.

Furthermore the MBa8x provides all power supplies and configurations required for the operation of the TQMa8x.

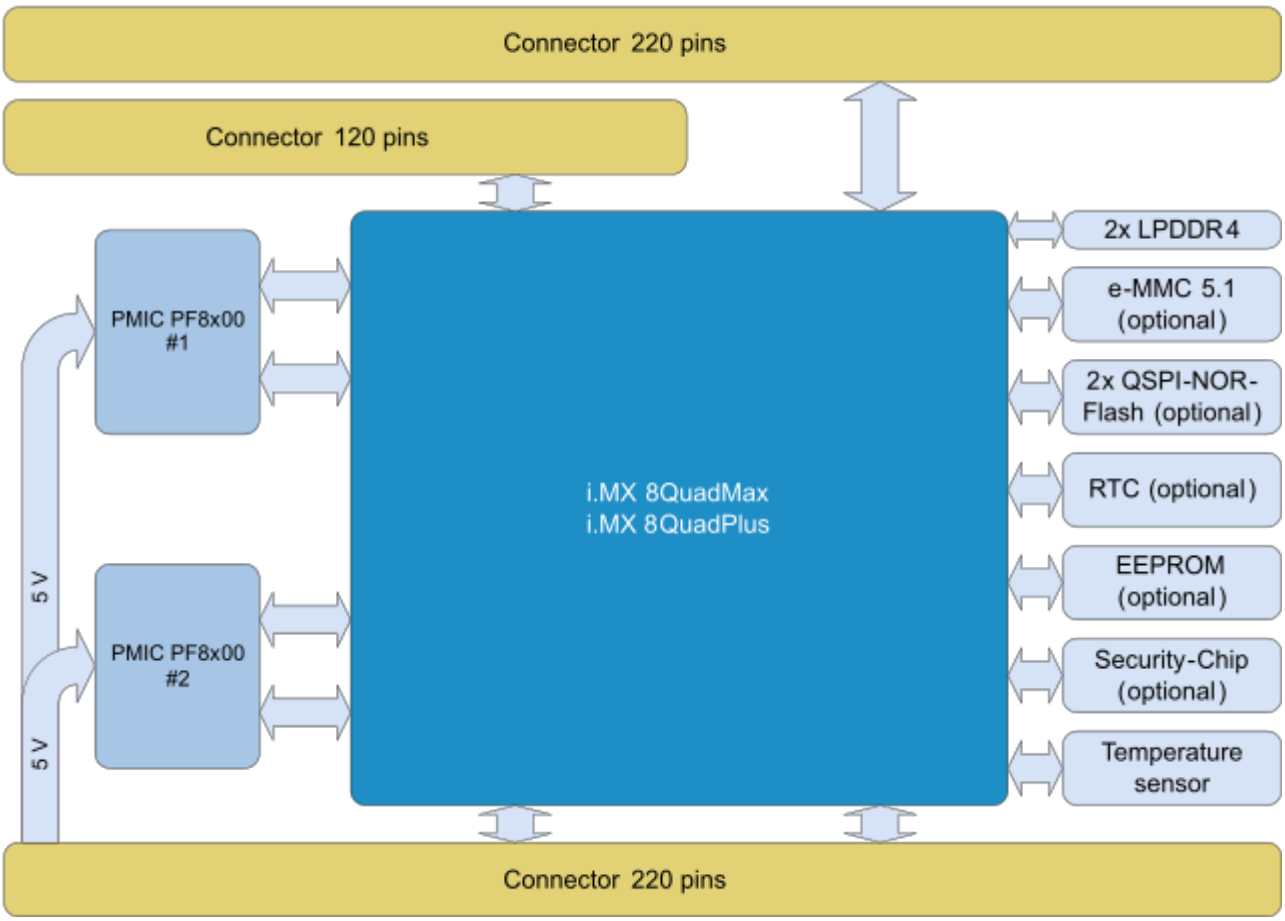

Figure 2: Block diagram TQMa8x

3.3 TQMa8x mating connectors

The TQMa8x is connected to the MBa8x with 560 pins on three connectors. The following table shows some suitable mating connectors for a carrier board:

Table 4: Carrier board mating connectors

Manufacturer	Part number	Remark	Stack height
EPT	220-pin: 401-51101-51 120-pin: 401-51401-51	On MBa8x	5 mm

If a different board-to-board distance is required, connectors with a different height can be used. Suitable types can be found on the manufacturer's website.

To avoid damaging the connectors of the MBa8x or the TQMa8x while removing the TQMa8x, the use of the extraction tool MOZIA8X is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa8x for the extraction tool MOZIA8X.

3.4 TQMa8x pinout

All available TQMa8x signals are available at three connectors on the MBa8x.

Note: Available interfaces	
	Depending on the TQMa8x derivative not all interfaces are available. More information about available interfaces can be found in the TQMa8x User's Manual.

3.1.1.2 TQMa8x pinout (continued)

Table 5: Pinout TQMa8x connector X1

i.MX 8 ball	DIR.	Level	Group	Signal	Pin		Signal	Group	Level	DIR.	i.MX 8 ball
–	–	–	Ground	GND(FIXED)	A1	B1	GND(FIXED)	Ground	–	–	–
–	P	5 V	Power	V_5V_IN	A2	B2	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A3	B3	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A4	B4	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A5	B5	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A6	B6	V_5V_IN	Power	5 V	P	–
–	–	–	Ground	GND	A7	B7	GND	Ground	–	–	–
–	P	VAR	Power	V_ENET_IN	A8	B8	V_SIM_IN	Power	VAR	P	AK42
–	P	1.8 V	Power	V_1V8_OUT	A9	B9	V_ADC_IN	Power	1.8 V	P	–
–	P	1.8 V	Power	V_1V8_OUT	A10	B10	V_3V3_OUT	Power	3.3 V	P	–
–	–	–	Ground	GND(FIXED)	A11	B11	GND(FIXED)	Ground	–	–	–
BC3	I	1.8 V	MCLK	MCLK_IN	A12	B12	PWM3_OUT	PWM	1.8 V	O	AW53
–	–	–	Ground	GND	A13	B13	PWM2_OUT	PWM	1.8 V	O	BA51
–	OD	VAR	SYSTEM	RESET_OUT#	A14	B14	PMIC_I2C_SCL	I2C	1.8 V	O	AY46
–	I	1.8 V	SYSTEM	RESET_IN#	A15	B15	PMIC_I2C_SDA	I2C	1.8 V	I/O	BG51
J11	O	1.8 V	QSPI	QSPI1A_SS[0]#	A16	B16	FTM_CH[0]	FTM	1.8 V	I/O	BF2
G11	O	1.8 V	QSPI	QSPI1A_SS[1]#	A17	B17	FTM_CH[1]	FTM	1.8 V	I/O	BE5
H12	I	1.8 V	QSPI	QSPI1A_DQS	A18	B18	FTM_CH[2]	FTM	1.8 V	I/O	BG5
–	–	–	Ground	GND	A19	B19	GPIO2_IO[17]	GPIO	1.8 V	I/O	BF6
F10	O	1.8 V	QSPI	QSPI1A_SCLK	A20	B20	GPIO2_IO[21]	GPIO	1.8 V	I/O	BD8
–	–	–	Ground	GND(FIXED)	A21	B21	GND(FIXED)	Ground	–	–	–
E11	I/O	1.8 V	QSPI	QSPI1A_DATA[3]	A22	B22	CAN2_RX	CAN	1.8 V	I	C3
E13	I/O	1.8 V	QSPI	QSPI1A_DATA[2]	A23	B23	CAN2_TX	CAN	1.8 V	O	E7
D14	I/O	1.8 V	QSPI	QSPI1A_DATA[1]	A24	B24	CAN1_RX	CAN	1.8 V	I	E5
D12	I/O	1.8 V	QSPI	QSPI1A_DATA[0]	A25	B25	CAN1_TX	CAN	1.8 V	O	G7
–	–	–	Ground	GND	A26	B26	CAN0_RX	CAN	1.8 V	I	C5
D2	O	1.8 V	MLB	MLB_CLK	A27	B27	CAN0_TX	CAN	1.8 V	O	H6
–	–	–	Ground	GND	A28	B28	GND	Ground	–	–	–
E1	O	1.8 V	MLB	MLB_SIG	A29	B29	PCIE0_REFCLK100M_P	PCIE	1.8 V	I/O	F26
E3	O	1.8 V	MLB	MLB_DATA	A30	B30	PCIE0_REFCLK100M_N	PCIE	1.8 V	I/O	E25
–	–	–	Ground	GND(FIXED)	A31	B31	GND(FIXED)	Ground	–	–	–
A9	O	1.8 V	ENET	ENET0_MDC	A32	B32	USB_HSIC_DATA	HSIC	1.8 V	I/O	H26
D10	I/O	1.8 V	ENET	ENET0_MDIO	A33	B33	GND	Ground	–	–	–
–	–	–	Ground	GND	A34	B34	USB_HSIC_STROBE	HSIC	1.8 V	I/O	F28
B10	O	1.8 V	ENET	ENET0_REFCLK_125M_25M	A35	B35	GND	Ground	–	–	–
–	–	–	Ground	GND	A36	B36	PCIE1_RX_P	PCIE	1.8 V	I	A21
A11	O	1.8 V	ENET	ENET1_REFCLK_125M_25M	A37	B37	PCIE1_RX_N	PCIE	1.8 V	I	B22
–	–	–	Ground	GND	A38	B38	GND	Ground	–	–	–
A13	O	VAR	ENET	ENET1_MDC	A39	B39	PCIE1_TX_P	PCIE	1.8 V	O	B24
C13	I/O	VAR	ENET	ENET1_MDIO	A40	B40	PCIE1_TX_N	PCIE	1.8 V	O	C25
–	–	–	Ground	GND(FIXED)	A41	B41	GND(FIXED)	Ground	–	–	–
D20	O	3.3 V	PCIE	PCIE0_PERST#	A42	B42	PCIE1_PERST#	PCIE	3.3 V	O	G25
A15	I	3.3 V	PCIE	PCIE0_WAKE#	A43	B43	PCIE1_WAKE#	PCIE	3.3 V	I	A27
A17	I	3.3 V	PCIE	PCIE0_CLKREQ#	A44	B44	PCIE1_CLKREQ#	PCIE	3.3 V	I	A25
–	–	–	DNC	NC	A45	B45	GND	Ground	–	–	–
H22	I	1.8 V	QSPI	QSPI0B_DQS	A46	B46	PCIE0_TX_P	PCIE	1.8 V	O	B26
F16	O	1.8 V	QSPI	QSPI0A_SS[1]#	A47	B47	PCIE0_TX_N	PCIE	1.8 V	O	C27
H24	O	1.8 V	QSPI	QSPI0B_SS[1]#	A48	B48	GND	Ground	–	–	–
A5	I/O	1.8 V	GPIO	GPIO4_IO[07]	A49	B49	PCIE0_RX_P	PCIE	1.8 V	I	A29
J43	I/O	VAR	GPIO	GPIO5_IO[23]	A50	B50	PCIE0_RX_N	PCIE	1.8 V	I	B30
–	–	–	Ground	GND(FIXED)	A51	B51	GND(FIXED)	Ground	–	–	–
J39	I/O	VAR	SD	USDHC1_CLK	A52	B52	USB_SS_TX_N	USB	1.8 V	O	B32
–	–	–	Ground	GND	A53	B53	USB_SS_TX_P	USB	1.8 V	O	A33
G41	I/O	VAR	SD	USDHC1_CMD	A54	B54	GND	Ground	–	–	–
H42	I/O	VAR	SD	USDHC1_CD#	A55	B55	USB_SS_RX_N	USB	1.8 V	I	B34

3.1.1.2 TQMa8x pinout (continued)

Table 5: Pinout TQMa8x connector X1 (continued)

i.MX 8 ball	DIR.	Level	Group	Signal	Pin		Signal	Group	Level	DIR.	i.MX 8 ball
E37	I/O	VAR	SD	USDHC1_DATA0	A56	B56	USB_SS_RX_P	USB	1.8 V	I	C35
F38	I/O	VAR	SD	USDHC1_DATA1	A57	B57	GND	Ground	–	–	–
E39	I/O	VAR	SD	USDHC1_DATA2	A58	B58	NC	DNC	–	–	–
F40	I/O	VAR	SD	USDHC1_DATA3	A59	B59	USB_OTG2_OC	OTG	3.3 V	I	H10
–	–	–	Ground	GND(FIXED)	A60	B60	GND(FIXED)	Ground	–	–	–
H40	I/O	VAR	GPIO	GPIO5_IO[19]	A61	B61	USB_OTG2_PWR	OTG	3.3 V	O	L9
G43	I/O	VAR	GPIO	GPIO5_IO[20]	A62	B62	USB_OTG2_ID	OTG	3.3 V	I	F30
F42	I/O	VAR	SD	USDHC1_WP	A63	B63	USB_OTG2_VBUS	OTG	3.3 V	P	A35
–	–	–	Ground	GND	A64	B64	GND	Ground	–	–	–
D30	O	1.8 V	MLB	MLB_SIG_P	A65	B65	USB_OTG2_DN	OTG	3.3 V	I/O	C37
E31	O	1.8 V	MLB	MLB_SIG_N	A66	B66	USB_OTG2_DP	OTG	3.3 V	I/O	B38
–	–	–	Ground	GND	A67	B67	GND	Ground	–	–	–
D32	O	1.8 V	MLB	MLB_CLK_P	A68	B68	USB_OTG1_DN	OTG	3.3 V	I/O	C39
E33	O	1.8 V	MLB	MLB_CLK_N	A69	B69	USB_OTG1_DP	OTG	3.3 V	I/O	B40
–	–	–	Ground	GND(FIXED)	A70	B70	GND(FIXED)	Ground	–	–	–
F34	O	1.8 V	MLB	MLB_DATA_P	A71	B71	USB_OTG1_OC	OTG	3.3 V	I	F8
E35	O	1.8 V	MLB	MLB_DATA_N	A72	B72	USB_OTG1_PWR	OTG	3.3 V	O	J9
–	–	–	Ground	GND	A73	B73	USB_OTG1_ID	OTG	1.8 V	I	A37
–	–	–	DNC	NC	A74	B74	USB_OTG1_VBUS	OTG	5 V	P	A39
–	–	–	Ground	GND	A75	B75	GND	Ground	–	–	–
A41	O	1.8 V	ENET	ENET0_TXC	A76	B76	ENET1_TXC	ENET	1.8 V	O	D46
–	–	–	Ground	GND	A77	B77	GND	Ground	–	–	–
E41	O	1.8 V	ENET	ENET0_TX_CTL	A78	B78	ENET1_TX_CTL	ENET	1.8 V	O	B48
A43	O	1.8 V	ENET	ENET0_TXD[0]	A79	B79	ENET1_TXD[0]	ENET	1.8 V	O	A49
–	–	–	Ground	GND(FIXED)	A80	B80	GND(FIXED)	Ground	–	–	–
B42	O	1.8 V	ENET	ENET0_TXD[1]	A81	B81	ENET1_TXD[1]	ENET	1.8 V	O	C47
A45	O	1.8 V	ENET	ENET0_TXD[2]	A82	B82	ENET1_TXD[2]	ENET	1.8 V	O	G47
D42	O	1.8 V	ENET	ENET0_TXD[3]	A83	B83	ENET1_TXD[3]	ENET	1.8 V	O	D48
–	–	–	Ground	GND	A84	B84	GND	Ground	–	–	–
B44	I	1.8 V	ENET	ENET0_RXC	A85	B85	ENET1_RXC	ENET	1.8 V	I	B50
–	–	–	Ground	GND	A86	B86	GND	Ground	–	–	–
E43	I	1.8 V	ENET	ENET0_RX_CTL	A87	B87	ENET1_RX_CTL	ENET	1.8 V	I	E49
A47	I	1.8 V	ENET	ENET0_RXD[0]	A88	B88	ENET1_RXD[0]	ENET	1.8 V	I	E51
D44	I	1.8 V	ENET	ENET0_RXD[1]	A89	B89	ENET1_RXD[1]	ENET	1.8 V	I	C51
–	–	–	Ground	GND(FIXED)	A90	B90	GND(FIXED)	Ground	–	–	–
C45	I	1.8 V	ENET	ENET0_RXD[2]	A91	B91	ENET1_RXD[2]	ENET	1.8 V	I	D52
E45	I	1.8 V	ENET	ENET0_RXD[3]	A92	B92	ENET1_RXD[3]	ENET	1.8 V	I	E53
–	–	–	Ground	GND	A93	B93	GND	Ground	–	–	–
AL45	O	VAR	SIM	SIM_CLK	A94	B94	M41_GPIO0_00	M4 GPIO	1.8 V	I/O	AP44
AL43	I	VAR	SIM	SIM_PD	A95	B95	M41_GPIO0_01	M4 GPIO	1.8 V	I/O	AU47
AN45	I/O	VAR	SIM	SIM_IO	A96	B96	M41_UART_TX	M4 UART	1.8 V	O	AU49
AP46	I/O	VAR	SIM	GPIO0_IO[05]	A97	B97	M41_UART_RX	M4 UART	1.8 V	I	AR45
AP48	O	VAR	SIM	SIM_RST	A98	B98	M40_UART_RX	M4 UART	1.8 V	I	AM44
AT48	O	VAR	SIM	SIM_PWR_EN	A99	B99	M40_UART_TX	M4 UART	1.8 V	O	AU51
–	–	–	Ground	GND(FIXED)	A100	B100	GND(FIXED)	Ground	–	–	–
BC51	O	1.8 V	JTAG	JTAG_TCK	A101	B101	UART0_RX	UART	1.8 V	I	AV50
BA49	I	1.8 V	JTAG	JTAG_TMS	A102	B102	UART0_TX	UART	1.8 V	O	AV48
BD52	O	1.8 V	JTAG	JTAG_TDO	A103	B103	UART0_CTS#	UART	1.8 V	I	AV46
BE53	I	1.8 V	JTAG	JTAG_TRST#	A104	B104	UART0_RTS#	UART	1.8 V	O	AU45
BE51	I	1.8 V	JTAG	JTAG_TDI	A105	B105	GND	Ground	–	–	–
–	–	–	Ground	GND	A106	B106	UART1_RX	UART	1.8 V	I	AT44
–	–	–	DNC	NC	A107	B107	UART1_TX	UART	1.8 V	O	AY48
–	OD	VAR	SYSTEM	RTC_EVENT#	A108	B108	UART1_CTS#	UART	1.8 V	I	AV46
BE47	I	1.8 V	JTAG	IMX_ONOFF	A109	B109	UART1_RTS#	UART	1.8 V	O	AR43
–	–	–	Ground	GND(FIXED)	A110	B110	GND(FIXED)	Ground	–	–	–

3.1.1.2 TQMa8x pinout (continued)

Table 6: Pinout TQMa8x connector X2

i.MX 8 ball	DIR.	Level	Group	Signal	Pin		Signal	Group	Level	DIR.	i.MX 8 ball
–	–	–	Ground	GND(FIXED)	A1	B1	GND(FIXED)	Ground	–	–	–
BC1	O	1.8 V	SPI	SPI0_CS[0]	A2	B2	ADC_IN[0]	ADC	1.8 V	A	AP10
BA3	O	1.8 V	SPI	SPI0_CS[1]	A3	B3	ADC_IN[1]	ADC	1.8 V	A	AN11
BA5	I	1.8 V	SPI	SPI0_SDI	A4	B4	ADC_IN[2]	ADC	1.8 V	A	AP8
AY6	O	1.8 V	SPI	SPI0_SDO	A5	B5	GND	Ground	–	–	–
BB4	O	1.8 V	SPI	SPI0_SCK	A6	B6	IMX_MEMC_ON	SYSTEM	1.8 V	O	BC53
AL9	O	1.8 V	SPI	SPI1_CS[0]	A7	B7	PMIC_PWR_ON	SYSTEM	1.8 V	I	–
AP6	O	1.8 V	SPI	SPI1_CS[1]	A8	B8	GND	Ground	–	–	–
AR7	I	1.8 V	SPI	SPI1_SDI	A9	B9	HDMI_TX_AUX_N	HDMI	1.8 V	O	BG3
AN9	O	1.8 V	SPI	SPI1_SDO	A10	B10	HDMI_TX_AUX_P	HDMI	1.8 V	O	BH2
–	–	–	Ground	GND(FIXED)	A11	B11	GND(FIXED)	Ground	–	–	–
AR9	O	1.8 V	SPI	SPI1_SCK	A12	B12	GND	Ground	–	–	–
AW1	O	1.8 V	SPI	SPI2_CS[0]	A13	B13	HDMI_TX_CLK_N	HDMI	1.8 V	O	BK2
AY2	O	1.8 V	SPI	SPI2_CS[1]	A14	B14	HDMI_TX_CLK_P	HDMI	1.8 V	O	BL3
AY4	I	1.8 V	SPI	SPI2_SDI	A15	B15	GND	Ground	–	–	–
BA1	O	1.8 V	SPI	SPI2_SDO	A16	B16	HDMI_TX_DATA[0]_N	HDMI	1.8 V	O	BM4
AW5	O	1.8 V	SPI	SPI2_SCK	A17	B17	HDMI_TX_DATA[0]_P	HDMI	1.8 V	O	BL5
AU1	O	1.8 V	SAI	SAI1_TXD	A18	B18	GND	Ground	–	–	–
AV2	O	1.8 V	SAI	SAI1_TXFS	A19	B19	HDMI_TX_DATA[1]_N	HDMI	1.8 V	O	BM6
AU5	O	1.8 V	SAI	SAI1_TXC	A20	B20	HDMI_TX_DATA[1]_P	HDMI	1.8 V	O	BL7
–	–	–	Ground	GND(FIXED)	A21	B21	GND(FIXED)	Ground	–	–	–
AU3	I	1.8 V	SAI	SAI1_RXFS	A22	B22	HDMI_TX_DATA[2]_N	HDMI	1.8 V	O	BM8
AV6	I	1.8 V	SAI	SAI1_RXC	A23	B23	HDMI_TX_DATA[2]_P	HDMI	1.8 V	O	BL9
AV4	I	1.8 V	SAI	SAI1_RXD	A24	B24	GND	Ground	–	–	–
BN35	I/O	1.8 V	GPIO	GPIO1_IO[15]	A25	B25	HDMI_TX_DDC_SCL	HDMI	1.8 V	O	BG1
–	–	–	Ground	GND	A26	B26	HDMI_TX_DDC_SDA	HDMI	1.8 V	I/O	BN5
AT10	I/O	1.8 V	ESAI	ESAI1_TX5_RX0	A27	B27	HDMI_TX_CEC	HDMI	1.8 V	O	BJ1
AY12	I/O	1.8 V	ESAI	ESAI1_TX4_RX1	A28	B28	HDMI_TX_HPD	HDMI	1.8 V	O	BH8
AV10	I/O	1.8 V	ESAI	ESAI1_TX3_RX2	A29	B29	GPIO2_IO[02]	GPIO	3.3 V	I/O	BN9
AU11	I/O	1.8 V	ESAI	ESAI1_TX2_RX3	A30	B30	GPIO2_IO[03]	GPIO	3.3 V	I/O	BN7
–	–	–	Ground	GND(FIXED)	A31	B31	GND(FIXED)	Ground	–	–	–
BA11	O	1.8 V	ESAI	ESAI1_TX1	A32	B32	MCLK_OUT	MCLK	1.8 V	O	BD4
BF10	O	1.8 V	ESAI	ESAI1_TX0	A33	B33	GND	Ground	–	–	–
BD12	O	1.8 V	ESAI	ESAI1_SCKR	A34	B34	GPIO1_IO[14]	GPIO	1.8 V	I/O	BD32
BE11	O	1.8 V	ESAI	ESAI1_FSR	A35	B35	PMIC2_FSOB	SYSTEM	1.8 V	O	–
AY10	O	1.8 V	ESAI	ESAI1_SCKT	A36	B36	PMIC2_PGOOD	SYSTEM	1.8 V	OD	–
BF12	O	1.8 V	ESAI	ESAI1_FST	A37	B37	V_LICELL	Power	3.3 V	P	–
–	–	–	Ground	GND	A38	B38	GND	Ground	–	–	–
AR47	I/O	1.8 V	M4 GPIO	M40_GPIO0_00	A39	B39	MIPI_CSI0_SDA	CSI	1.8 V	I/O	BN19
AU53	I/O	1.8 V	M4 GPIO	M40_GPIO0_01	A40	B40	MIPI_CSI0_SCL	CSI	1.8 V	O	BH24
–	–	–	Ground	GND(FIXED)	A41	B41	GND(FIXED)	Ground	–	–	–
–	P	1.8 V	Power	V_1V8_ANA_OUT	A42	B42	NC	DNC	–	–	–
–	–	–	Ground	GND	A43	B43	GND	Ground	–	–	–
BN15	I/O	1.8 V	CSI	MIPI_CSI1_RST#	A44	B44	MIPI_CSI0_MCLK_OUT	CSI	1.8 V	O	BJ23
BN13	O	1.8 V	CSI	MIPI_CSI1_EN	A45	B45	GND	Ground	–	–	–
BM22	O	1.8 V	CSI	MIPI_CSI0_EN	A46	B46	MIPI_CSI0_DATA[3]_N	CSI	1.8 V	I	BE17
BL23	I/O	1.8 V	CSI	MIPI_CSI0_RST#	A47	B47	MIPI_CSI0_DATA[3]_P	CSI	1.8 V	I	BF16
–	OD	VAR	SYSTEM	TEMP_EVENT#	A48	B48	GND	Ground	–	–	–
–	–	–	Ground	GND	A49	B49	MIPI_CSI0_DATA[2]_N	CSI	1.8 V	I	BE25
BN23	O	1.8 V	CSI	MIPI_CSI1_MCLK_OUT	A50	B50	MIPI_CSI0_DATA[2]_P	CSI	1.8 V	I	BF24
–	–	–	Ground	GND(FIXED)	A51	B51	GND(FIXED)	Ground	–	–	–
–	O	1.8 V	SYSTEM	PMIC1_FSOB	A52	B52	MIPI_CSI0_CLK_N	CSI	1.8 V	I	BE21
–	OD	1.8 V	SYSTEM	PMIC1_PGOOD	A53	B53	MIPI_CSI0_CLK_P	CSI	1.8 V	I	BF20
–	–	–	Ground	GND	A54	B54	GND	Ground	–	–	–
BH12	I	1.8 V	CSI	MIPI_CSI1_DATA[3]_N	A55	B55	MIPI_CSI0_DATA[1]_N	CSI	1.8 V	I	BE19

3.1.1.2 TQMa8x pinout (continued)

Table 6: Pinout TQMa8x connector X2 (continued)

i.MX 8 ball	DIR.	Level	Group	Signal	Pin		Signal	Group	Level	DIR.	i.MX 8 ball
BJ13	I	1.8 V	CSI	MIPI_CSI1_DATA[3]_P	A56	B56	MIPI_CSI0_DATA[1]_P	CSI	1.8 V	I	BF18
–	–	–	Ground	GND	A57	B57	GND	Ground	–	–	–
BH20	I	1.8 V	CSI	MIPI_CSI1_DATA[2]_N	A58	B58	MIPI_CSI0_DATA[0]_N	CSI	1.8 V	I	BE23
BJ21	I	1.8 V	CSI	MIPI_CSI1_DATA[2]_P	A59	B59	MIPI_CSI0_DATA[0]_P	CSI	1.8 V	I	BF22
–	–	–	Ground	GND(FIXED)	A60	B60	GND(FIXED)	Ground	–	–	–
BH16	I	1.8 V	CSI	MIPI_CSI1_CLK_N	A61	B61	I2C2_SCL	I2C	1.8 V	O	BA53
BJ17	I	1.8 V	CSI	MIPI_CSI1_CLK_P	A62	B62	I2C2_SDA	I2C	1.8 V	I/O	AY50
–	–	–	Ground	GND	A63	B63	MIPI_DSI0_GPIO0_01	DSI	1.8 V	I/O	BD28
BH14	I	1.8 V	CSI	MIPI_CSI1_DATA[1]_N	A64	B64	MIPI_DSI0_PWM	DSI	1.8 V	O	BD30
BJ15	I	1.8 V	CSI	MIPI_CSI1_DATA[1]_P	A65	B65	MIPI_DSI0_SCL	DSI	1.8 V	O	BE29
–	–	–	Ground	GND	A66	B66	MIPI_DSI0_SDA	DSI	1.8 V	I/O	BE31
BH18	I	1.8 V	CSI	MIPI_CSI1_DATA[0]_N	A67	B67	GND	Ground	–	–	–
BJ19	I	1.8 V	CSI	MIPI_CSI1_DATA[0]_P	A68	B68	MIPI_DSI0_DATA[3]_N	DSI	1.8 V	O	BN25
–	–	–	Ground	GND	A69	B69	MIPI_DSI0_DATA[3]_P	DSI	1.8 V	O	BL25
–	–	–	Ground	GND(FIXED)	A70	B70	GND(FIXED)	Ground	–	–	–
BE15	I/O	1.8 V	CSI	MIPI_CSI1_SDA	A71	B71	GND	Ground	–	–	–
BN17	O	1.8 V	CSI	MIPI_CSI1_SCL	A72	B72	MIPI_DSI0_DATA[2]_N	DSI	1.8 V	O	BN29
BE39	O	1.8 V	LVDS	LVDS0_PWM	A73	B73	MIPI_DSI0_DATA[2]_P	DSI	1.8 V	O	BL29
BD40	I/O	1.8 V	LVDS	LVDS0_GPIO01	A74	B74	GND	Ground	–	–	–
BD36	I/O	1.8 V	LVDS	LVDS0_I2C0_SDA	A75	B75	MIPI_DSI0_CLK_N	DSI	1.8 V	O	BN27
BD38	O	1.8 V	LVDS	LVDS0_I2C0_SCL	A76	B76	MIPI_DSI0_CLK_P	DSI	1.8 V	O	BL27
–	–	–	Ground	GND	A77	B77	GND	Ground	–	–	–
BG37	O	1.8 V	LVDS	LVDS0_CH1_TX[3]_N	A78	B78	MIPI_DSI0_DATA[1]_N	DSI	1.8 V	O	BM26
BH38	O	1.8 V	LVDS	LVDS0_CH1_TX[3]_P	A79	B79	MIPI_DSI0_DATA[1]_P	DSI	1.8 V	O	BK26
–	–	–	Ground	GND(FIXED)	A80	B80	GND(FIXED)	Ground	–	–	–
–	–	–	Ground	GND	A81	B81	GND	Ground	–	–	–
BG39	O	1.8 V	LVDS	LVDS0_CH1_TX[2]_N	A82	B82	MIPI_DSI0_DATA[0]_N	DSI	1.8 V	O	BM28
BH40	O	1.8 V	LVDS	LVDS0_CH1_TX[2]_P	A83	B83	MIPI_DSI0_DATA[0]_P	DSI	1.8 V	O	BK28
–	–	–	Ground	GND	A84	B84	GND	Ground	–	–	–
BG41	O	1.8 V	LVDS	LVDS0_CH1_TX[1]_N	A85	B85	SCU_UART_RX	SCU	1.8 V	I	AU43
BH42	O	1.8 V	LVDS	LVDS0_CH1_TX[1]_P	A86	B86	SCU_UART_TX	SCU	1.8 V	O	AV44
–	–	–	Ground	GND	A87	B87	SCU_GPIO0_[02]	SCU	1.8 V	I/O	AW45
BG43	O	1.8 V	LVDS	LVDS0_CH1_TX[0]_N	A88	B88	SCU_GPIO0_[03]	SCU	1.8 V	I/O	BB46
BH44	O	1.8 V	LVDS	LVDS0_CH1_TX[0]_P	A89	B89	SCU_GPIO0_[04]	SCU	1.8 V	I/O	BC47
–	–	–	Ground	GND(FIXED)	A90	B90	GND(FIXED)	Ground	–	–	–
BG45	O	1.8 V	LVDS	LVDS0_CH1_CLK_N	A91	B91	SCU_GPIO0_[05]	SCU	1.8 V	I/O	AY44
BH46	O	1.8 V	LVDS	LVDS0_CH1_CLK_P	A92	B92	SCU_GPIO0_[06]	SCU	1.8 V	I/O	BG49
–	–	–	Ground	GND	A93	B93	SCU_GPIO0_[07]	SCU	1.8 V	I/O	BF48
BL41	O	1.8 V	LVDS	LVDS0_CH0_CLK_N	A94	B94	BOOT_MODE[0]	BOOT	1.8 V	I	BB44
BN41	O	1.8 V	LVDS	LVDS0_CH0_CLK_P	A95	B95	BOOT_MODE[1]	BOOT	1.8 V	I	BC45
–	–	–	Ground	GND	A96	B96	BOOT_MODE[2]	BOOT	1.8 V	I	BJ53
BK42	O	1.8 V	LVDS	LVDS0_CH0_TX[0]_N	A97	B97	BOOT_MODE[3]	BOOT	1.8 V	I	BA43
BM42	O	1.8 V	LVDS	LVDS0_CH0_TX[0]_P	A98	B98	BOOT_MODE[4]	BOOT	1.8 V	I	AY42
–	–	–	Ground	GND	A99	B99	BOOT_MODE[5]	BOOT	1.8 V	I	BK52
–	–	–	Ground	GND(FIXED)	A100	B100	GND(FIXED)	Ground	–	–	–
BL43	O	1.8 V	LVDS	LVDS0_CH0_TX[1]_N	A101	B101	I2C1_SDA	I2C	1.8 V	I/O	AV52
BN43	O	1.8 V	LVDS	LVDS0_CH0_TX[1]_P	A102	B102	I2C1_SCL	I2C	1.8 V	O	AY52
–	–	–	Ground	GND	A103	B103	TAMPER_IN[0]	SNVS	1.8 V	I	BE41
BK44	O	1.8 V	LVDS	LVDS0_CH0_TX[2]_N	A104	B104	TAMPER_IN[1]	SNVS	1.8 V	I	BE43
BM44	O	1.8 V	LVDS	LVDS0_CH0_TX[2]_P	A105	B105	TAMPER_OUT[0]	SNVS	1.8 V	O	BD46
–	–	–	Ground	GND	A106	B106	TAMPER_OUT[1]	SNVS	1.8 V	O	BD42
BL45	O	1.8 V	LVDS	LVDS0_CH0_TX[3]_N	A107	B107	UART2_TX	UART	1.8 V	O	BE37
BN45	O	1.8 V	LVDS	LVDS0_CH0_TX[3]_P	A108	B108	UART2_RX	UART	1.8 V	I	BE35
–	–	–	Ground	GND	A109	B109	V_VBAT	Power	3.3 V	P	–
–	–	–	Ground	GND(FIXED)	A110	B110	GND(FIXED)	Ground	–	–	–

3.1.1.2 TQMa8x pinout (continued)

Table 7: Pinout TQMa8x connector X3

i.MX 8 ball	DIR.	Level	Group	Signal	Pin		Signal	Group	Level	DIR.	i.MX 8 ball
–	–	–	Ground	GND	A1	B1	GND	Ground	–	–	–
C17	O	1.8 V	SATA	SATA_TX_N	A2	B2	SATA_RX_N	SATA	1.8 V	I	B20
B16	O	1.8 V	SATA	SATA_TX_P	A3	B3	SATA_RX_P	SATA	1.8 V	I	A19
–	–	–	Ground	GND	A4	B4	GND	Ground	–	–	–
BD6	O	1.8 V	S/PDIF	SPDIF_EXT_CLK	A5	B5	GPIO4_IO[10]	SD / GPIO	1.8 V	I/O	A7
–	–	–	Ground	GND(FIXED)	A6	B6	GND(FIXED)	Ground	–	–	–
BC7	I	1.8 V	S/PDIF	SPDIF_RX	A7	B7	HDMI_RX_CLK_N	HDMI	1.8 V	I	BL11
BC9	O	1.8 V	S/PDIF	SPDIF_TX	A8	B8	HDMI_RX_CLK_P	HDMI	1.8 V	I	BM12
BH10	O	1.8 V	HDMI	HDMI_RX_DDC_SCL	A9	B9	GND	Ground	–	–	–
BE13	I/O	1.8 V	HDMI	HDMI_RX_DDC_SDA	A10	B10	HDMI_RX_ARC_N	HDMI	1.8 V	I	BL13
BN11	I	1.8 V	HDMI	HDMI_RX_MON_5V	A11	B11	HDMI_RX_ARC_P	HDMI	1.8 V	I	BM14
BE33	I/O	1.8 V	LVDS	LVDS1_I2C0_SDA	A12	B12	GND	Ground	–	–	–
BL35	O	1.8 V	LVDS	LVDS1_I2C0_SCL	A13	B13	HDMI_RX_DATA[0]_N	HDMI	1.8 V	I	BL15
BH36	I/O	1.8 V	LVDS	LVDS1_GPIO01	A14	B14	HDMI_RX_DATA[0]_P	HDMI	1.8 V	I	BM16
BD34	O	1.8 V	LVDS	LVDS1_PWM	A15	B15	GND	Ground	–	–	–
–	–	–	Ground	GND(FIXED)	A16	B16	GND(FIXED)	Ground	–	–	–
BK30	O	1.8 V	LVDS	LVDS1_CH1_TX[3]_N	A17	B17	HDMI_RX_DATA[1]_N	HDMI	1.8 V	I	BL17
BM30	O	1.8 V	LVDS	LVDS1_CH1_TX[3]_P	A18	B18	HDMI_RX_DATA[1]_P	HDMI	1.8 V	I	BM18
–	–	–	Ground	GND	A19	B19	GND	Ground	–	–	–
BL31	O	1.8 V	LVDS	LVDS1_CH1_TX[2]_N	A20	B20	HDMI_RX_DATA[2]_N	HDMI	1.8 V	I	BL19
BN31	O	1.8 V	LVDS	LVDS1_CH1_TX[2]_P	A21	B21	HDMI_RX_DATA[2]_P	HDMI	1.8 V	I	BM20
–	–	–	Ground	GND	A22	B22	GND	Ground	–	–	–
BK32	O	1.8 V	LVDS	LVDS1_CH1_TX[1]_N	A23	B23	HDMI_RX_CEC	HDMI	1.8 V	I	BJ9
BM32	O	1.8 V	LVDS	LVDS1_CH1_TX[1]_P	A24	B24	HDMI_RX_HPD	HDMI	1.8 V	I	BF14
–	–	–	Ground	GND	A25	B25	GND	Ground	–	–	–
–	–	–	Ground	GND(FIXED)	A26	B26	GND(FIXED)	Ground	–	–	–
BL33	O	1.8 V	LVDS	LVDS1_CH1_TX[0]_N	A27	B27	ESAI0_TX5_RX0	ESAI	1.8 V	I/O	AU7
BN33	O	1.8 V	LVDS	LVDS1_CH1_TX[0]_P	A28	B28	ESAI0_TX4_RX1	ESAI	1.8 V	I/O	AV8
–	–	–	Ground	GND	A29	B29	ESAI0_TX3_RX2	ESAI	1.8 V	I/O	BC5
BK34	O	1.8 V	LVDS	LVDS1_CH1_CLK_N	A30	B30	ESAI0_TX2_RX3	ESAI	1.8 V	I/O	AU9
BM34	O	1.8 V	LVDS	LVDS1_CH1_CLK_P	A31	B31	GND	Ground	–	–	–
–	–	–	Ground	GND	A32	B32	ESAI0_TX1	ESAI	1.8 V	O	BA7
BK36	O	1.8 V	LVDS	LVDS1_CH0_CLK_N	A33	B33	ESAI0_TX0	ESAI	1.8 V	O	BA9
BM36	O	1.8 V	LVDS	LVDS1_CH0_CLK_P	A34	B34	ESAI0_SCKR	ESAI	1.8 V	O	BB8
–	–	–	Ground	GND(FIXED)	A35	B35	GND(FIXED)	Ground	–	–	–
BL37	O	1.8 V	LVDS	LVDS1_CH0_TX[0]_N	A36	B36	ESAI0_FSR	ESAI	1.8 V	O	AW9
BN37	O	1.8 V	LVDS	LVDS1_CH0_TX[0]_P	A37	B37	ESAI0_SCKT	ESAI	1.8 V	O	AY8
–	–	–	Ground	GND	A38	B38	ESAI0_FST	ESAI	1.8 V	O	BG9
BK38	O	1.8 V	LVDS	LVDS1_CH0_TX[1]_N	A39	B39	NC	DNC	–	–	–
BM38	O	1.8 V	LVDS	LVDS1_CH0_TX[1]_P	A40	B40	GND	Ground	–	–	–
–	–	–	Ground	GND	A41	B41	MIPI_DSI1_SCL	DSI	1.8 V	O	BE27
BL39	O	1.8 V	LVDS	LVDS1_CH0_TX[2]_N	A42	B42	MIPI_DSI1_SDA	DSI	1.8 V	I/O	BG25
BN39	O	1.8 V	LVDS	LVDS1_CH0_TX[2]_P	A43	B43	MIPI_DSI1_PWM	DSI	1.8 V	O	BM24
–	–	–	Ground	GND	A44	B44	MIPI_DSI1_GPIO0_01	DSI	1.8 V	I/O	BK24
–	–	–	Ground	GND(FIXED)	A45	B45	GND(FIXED)	Ground	–	–	–
BK40	O	1.8 V	LVDS	LVDS1_CH0_TX[3]_N	A46	B46	MIPI_DSI1_DATA[3]_N	DSI	1.8 V	O	BH26
BM40	O	1.8 V	LVDS	LVDS1_CH0_TX[3]_P	A47	B47	MIPI_DSI1_DATA[3]_P	DSI	1.8 V	O	BG27
–	–	–	Ground	GND	A48	B48	GND	Ground	–	–	–
F46	I/O	VAR	SD / GPIO	GPIO5_IO[24]	A49	B49	MIPI_DSI1_DATA[2]_N	DSI	1.8 V	O	BH34
–	–	–	Ground	GND	A50	B50	MIPI_DSI1_DATA[2]_P	DSI	1.8 V	O	BG35
B8	I/O	1.8 V	SD / GPIO	GPIO4_IO[12]	A51	B51	GND	Ground	–	–	–
C7	I/O	1.8 V	SD / GPIO	GPIO4_IO[09]	A52	B52	MIPI_DSI1_CLK_N	DSI	1.8 V	O	BH30
D8	I/O	1.8 V	SD / GPIO	GPIO4_IO[11]	A53	B53	MIPI_DSI1_CLK_P	DSI	1.8 V	O	BG31
H44	I/O	VAR	SD / GPIO	GPIO5_IO[25]	A54	B54	GND	Ground	–	–	–
–	–	–	Ground	GND(FIXED)	A55	B55	GND(FIXED)	Ground	–	–	–
H48	I/O	VAR	SD / GPIO	GPIO5_IO[26]	A56	B56	MIPI_DSI1_DATA[1]_N	DSI	1.8 V	O	BH28
G45	I/O	VAR	SD / GPIO	GPIO5_IO[27]	A57	B57	MIPI_DSI1_DATA[1]_P	DSI	1.8 V	O	BG29
L45	I/O	VAR	SD / GPIO	GPIO5_IO[28]	A58	B58	GND	Ground	–	–	–
J45	I/O	VAR	SD / GPIO	GPIO5_IO[29]	A59	B59	MIPI_DSI1_DATA[0]_N	DSI	1.8 V	O	BH32
–	–	–	Ground	GND	A60	B60	MIPI_DSI1_DATA[0]_P	DSI	1.8 V	O	BG33

3.5 Boot-Mode configuration

The Boot-Mode of the i.MX 8 is set with signals BOOT_MODE[5:0], which can be set with DIP switch SW1.
The MBa8x supports the following TQMa8x boot sources.

- eMMC (on TQMa8x)
- QSPI NOR flash (on TQMa8x)
- SD card (on MBa8x)
- Serial downloader via USB OTG

Table 8: Boot-Mode configuration

Boot-Mode	SW1-1 (Boot-Mode0)	SW1-2 (Boot-Mode1)	SW1-3 (Boot-Mode2)	SW1-4 (Boot-Mode3)	SW1-5 (Boot-Mode4)	SW1-6 (Boot-Mode5)
Boot from eFuses	0	0	0	0	0	0
Serial Downloader (USB OTG1)	0	0	1	0	0	0
eMMC	0	0	0	1	0	0
SD card (USDHC1)	0	0	1	1	0	0
Flash / 3-byte read (not supported)	0	0	0	1	1	0
Flash / 4-byte read (not supported)	0	1	1	1	1	0
Hyperflash 1.8 V (not supported)	0	1	0	1	1	0

Note: Boot from NAND	
	Booting from NAND is not supported on the MBa8x.

3.6 Reset and Power Modes

RESET_IN#, IMX_ONOFF and PMIC_PWRON can be pulled to GND by push buttons.
RESET_OUT has a pull-up to V_1V8_ANA. The resulting reset signal is linked to an LED.

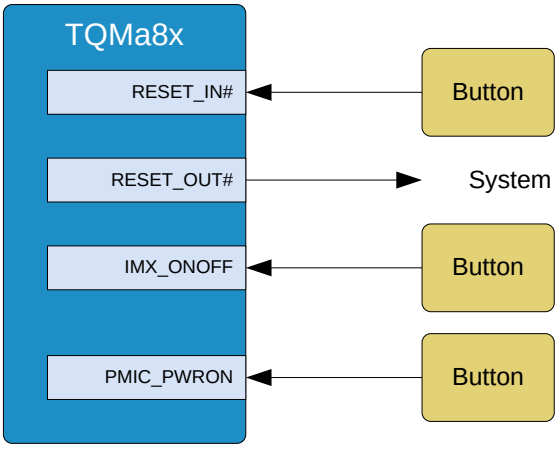

Figure 3: Block diagram Reset

The following TQMa8x signals are used on the MBa8x:

Table 9: Reset and Power Mode signals

Signal	Type	Level	Remark
RESET_IN#	I	1.8 V	• Triggers RESET (POR_B) of the i.MX 8 (low active) • No pull-up on the carrier board required • Low active (pull to GND, push button S7)
RESET_OUT#	O	–	• Open Drain output (low active) • Resets carrier board components • Pull-up on carrier board required (up to 6.5 V)
IMX_ONOFF	I	1.8 V	• ON/OFF function of the i.MX 8 (low active) • No pull-up on the carrier board required • Connect 5 s with GND (push button S9) to switch off the CPU • Low-active (pull to GND)
PMIC_PWRON	I	1.8 V	• Switches PMIC off (Off-Mode, low active) • No pull-up on the carrier board required • Low-active (pull to GND, push button S8)

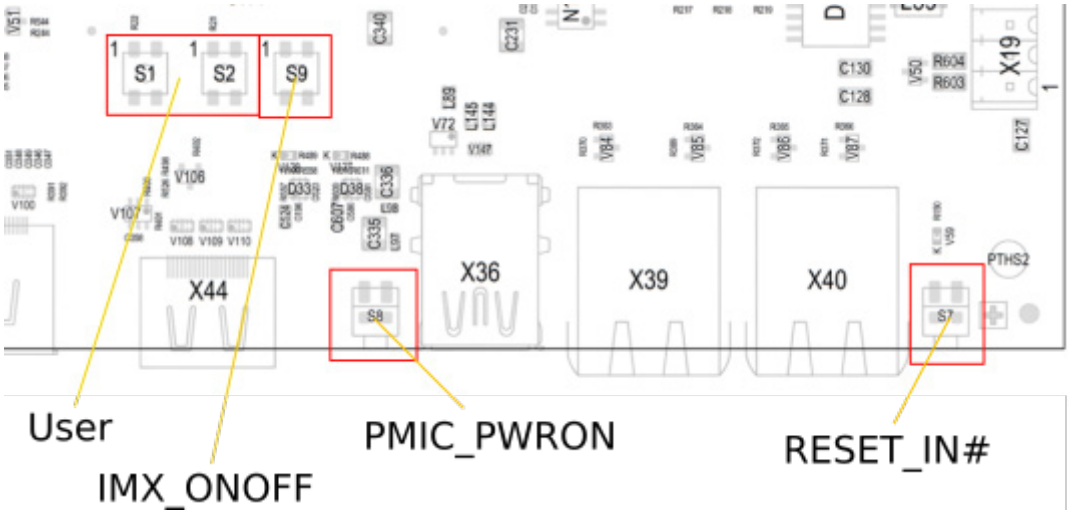

Figure 4: Placement push buttons on MBa8X

3.7 General purpose push buttons

For simple user inputs, the MBa8x offers two short-travel keys that are directly connected to the CPU. The signal lines have a 10 kΩ pull-up to V_1V8 and can be switched to ground by the push buttons.

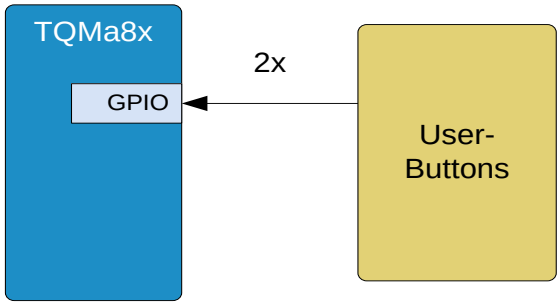

Figure 5: Block diagram GP push buttons

3.8 Battery

To maintain the RTC supply on the TQMa8x module when the mainboard is switched off, a CR2032 coin cell can be used on the mainboard. A battery holder is provided for this purpose. To meet the regulatory requirements for protection of accidental battery charging, a 1 kΩ resistor and a diode are connected in series.

Also, a two-pin header with jumper X23 is provided for additional supply to the V_LICELL level of the PMIC. Furthermore, there is a two-pin header X55 for the connection of an external power supply.

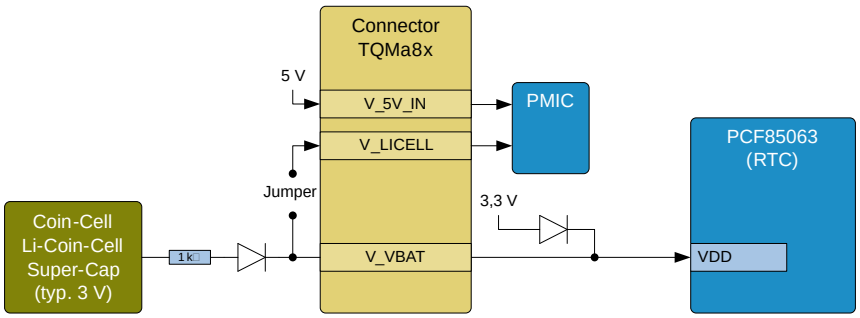

Figure 6: Block diagram battery

3.9 LEDs

The MBa8x has several LEDs. For user outputs two LEDs are available at the signals USER_LED0 and USER_LED1.

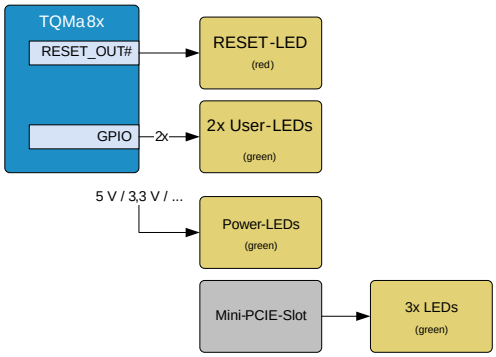

Figure 7: Block diagram LEDs

LEDs are connected to all main voltages (V_24V, V_12V, V_5V0_MOD, V_5V, V_3V3, V_1V8) as well as to the MPCIe voltages (V_3V3_MPCIE, V_1V5_MPCIE). In addition, all USB ports at the VBUS voltages have LEDs. The LEDs for voltages below 3.3 V are connected to V_3V3 and switched by the respective voltage level via a transistor.

The LEDs signal that the voltages have reached their typical end values and facilitate development on the MBa8x, as well as troubleshooting.

Also via a transistor SCU_GPIO0_02 is connected to a LED to switch it independently from the Linux and the bootloader from the SCU firmware. This facilitates the commissioning of the essential basic function of this firmware.

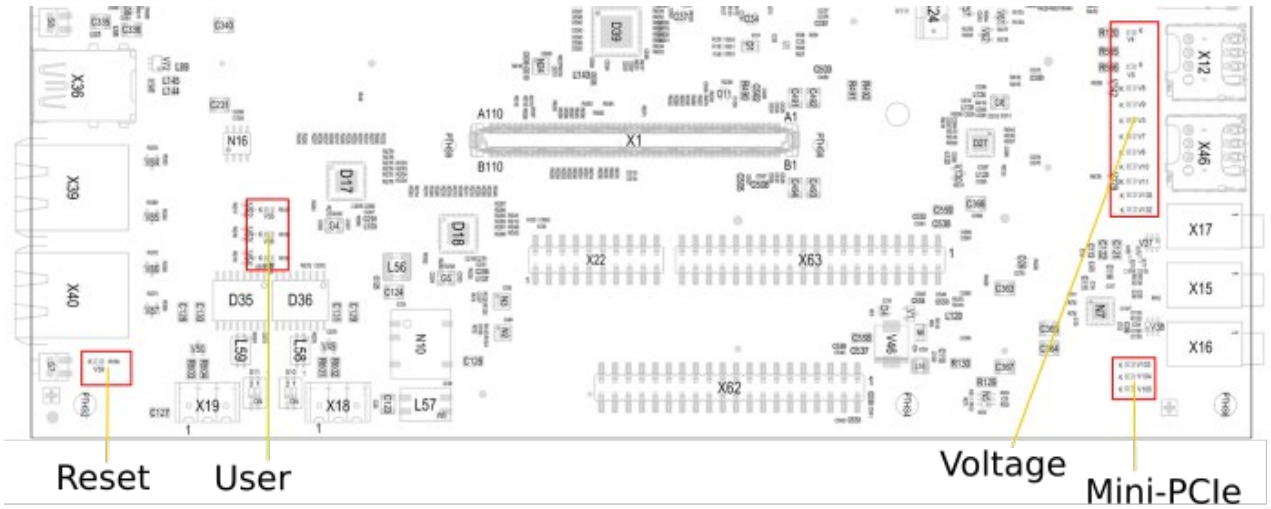

Figure 8: Placement

3.10 I²C devices

Two primary I2C buses are available. I2C1 connects all I2C devices on the module and the MBa8x. The voltage level of both I2C buses is 1.8 V. In order to be able to connect I2C devices with 3.3 V voltage level, there are level converters on the module and the mainboard. However, 3.3 V signals of the module are not available on the mainboard and vice versa.

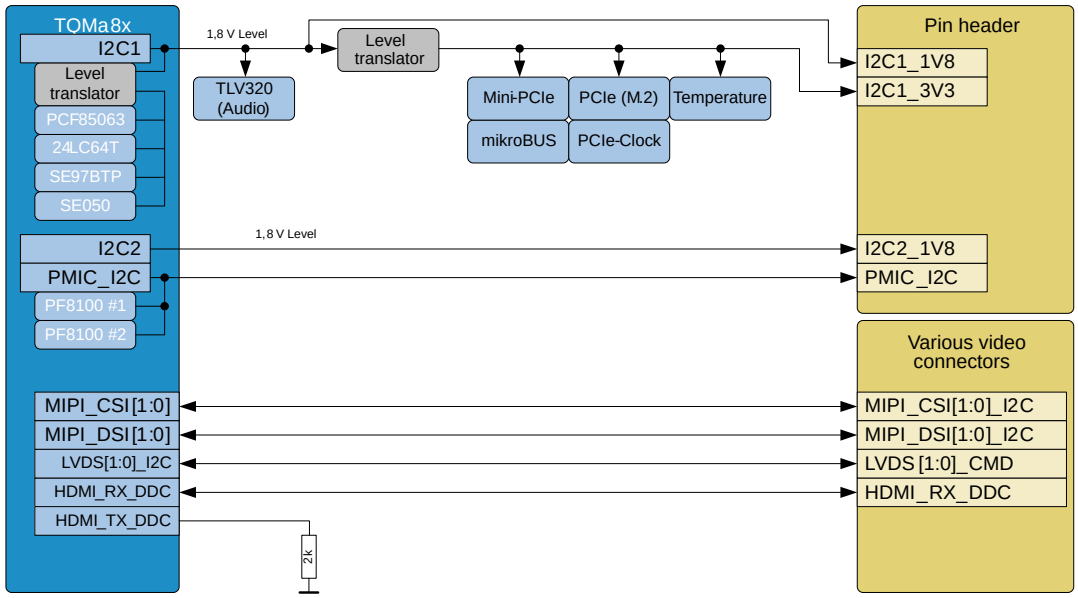

Figure 9: Block diagram I²C bus

Further I2C devices are in use on the TQMa8x, which is why the already occupied I2C addresses must be taken into account. Depending on the application and software load, the data throughput may be limited due to the number of I2C devices used.

The following placement options are available on the MBa8x: For I2C1, unpopulated pull-ups are provided since 2.2 kΩ pull-ups are already populated on the TQMa8x. For I2C2 4.7 kΩ pull-up resistors to 1.8 V are provided, as these are not populated on the module.

Both I2C buses are connected to the pin headers. The following table shows the used addresses of the respective buses:

Table 10: I²C devices, address mapping on TQMa8x and MBa8x

Bus	Device	Component	Address	Note
I2C1	TQMa8x	SE97BTP	0x1B	Temperature sensor
			0x53	EEPROM Read/Write
			0x33	EEPROM Protection Command
		EEPROM 24LC64T	0x57	Optional
		RTC PCF85063ATL	0x51	Optinol
		TSE SE050	0x48	Optional
	MBa8x	Mini-PCIe	NA	3.3 V
		Audio-Codec	0x18	1.8 V
		Clock driver	0x68	3.3 V
		mikroBUS	NA	3.3 V
		PCIe (M.2)	NA	3.3 V
		Temperature sensor	0x1C	3.3 V
		Temperature sensor	0x54	3.3 V
		Temperature sensor	0x34	3.3 V
I2C2	MBa8x	-	-	Available on pin header; 1.8 V
PMIC_I2C	TQMa8x	PMIC PF8x00 #1	0x08	1.8 V
		PMIC PF8x00 #2	0x09	1.8 V

A sensor of type SE97BTP with integrated EEPROM is available on the MBa8x for monitoring the temperature. This sensor is also installed on the TQMa8x. Both sensors are read out via I2C1. The address of the sensor on the MBa8x can be changed by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I2C devices. The placement options are documented in the latest circuit diagram.

I2C is provided at the microBUS interface of the MBa8x. The exact address depends on the used module and must always be checked to avoid address conflicts.

I2C1 is connected to the PCIe M.2 connector with 0 Ω resistors. These also allow this connection to be disconnected if required. The I2C address depends on the card used and must always be checked to avoid address conflicts.

I2C1 is connected to the Mini PCIe connector with 0 Ω resistors. These also allow this connection to be disconnected if required. The I2C address depends on the card used and must always be checked to avoid address conflicts.

The PCIe clock generator is connected I2C1 on 1.8 V level with 0 Ω resistors. These allow this connection to be disconnected if required. The I2C address is fixed and set to 0x68.

If required, the USB 3.0 hub can also be connected to I2C1. The 0 Ω resistors required for this are not equipped! The exact address is not fixed and can be adjusted by placing the bootstrap resistors. With this definition you have to pay attention to possible address conflicts.

3.11 GPIO port expander

An 8-fold port expander PCA9538 is used to control various components on the MBa8x, see Table 11.

The port expander is controlled via I2C1. The address of the port expander can be altered by reassembling resistors.

When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see **Fehler! Verweisquelle konnte nicht gefunden werden.**.

The assembly options are documented in the schematic of the MBa8x.

In the initial state after switching on, all ports are set as input and the respective connected component is thus deactivated.

The I/O level of the signals is 1.8 V.

Table 11: Functions port expander

Port	Signal	Type [1]	Default [2]	Remark
IO_0	Unused	I	Hi-Z	
IO_1	LED_A	O	Low	
IO_2	LED_B	O	Low	
IO_3	Unused	I	Hi-Z	
IO_4	DSI_EN	O	Low	
IO_5	USB_RESET#	O	High	Default: not used (RESET_OUT# is used)
IO_6	V_12V_EN	O	Low	
IO_7	PCIE_DIS#	O	High	

3.12 Temperature sensor

A temperature sensor SE97BTP is populated on the MBa8x to monitor the temperature. The same type of sensor is also used on the TQMa8x. Both sensors are read out via I2C1.

The sensor address on the MBa8x can be changed by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices. The assembly options are documented in the MBa8x schematics.

The SE97BTP has an additional EEPROM. Further specifications of the SE97BTP can be found in the data sheet.

3.13 Further devices

In addition to the port expander and the temperature sensor, more devices are connected to the I2C1.

These are described in the respective sections for the corresponding interfaces.

3.14 Interfaces

3.14.1 Audio

The audio codec used is the TLV320AIC3204 from Texas Instruments. It is connected to the TQMa8x via SAI (configured as I²S) and I²C. The audio codec provides microphone, line in and line out signals. The signals can be accessed via colour coded 3.5 mm jacks (green for line-out/headphone, blue for line-in and pink for microphone). A placement option allows to choose between line out and headphone. Table 12 describes the configuration.

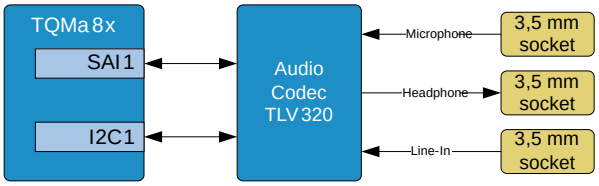

Figure 10: Block diagram Audio

Table 12: Placement option Audio

Mode	R77	R78	R79	R80	Remark
Line-Out	0R0	0R0	NP	NP	Default
Headphone	NP	NP	0R0	0R0	Optional

1: Intended port configuration.

2: Pull-Ups or Pull-Downs on MBa8x.

The MBa8x also provides the Enhanced Serial Audio Interface (ESAI). The ESAI0-Interface (ESAI0) is connected directly to pin header X61. On the other hand, other signals are muxed onto ESAI1. See also chapter 3.2.6 and MBa8x headers.

3.14.2 SPDIF

The SPDIF interface is connected to the starter kit header X64.

3.14.3 CAN-FD

Both CAN interfaces of the MBa8x are directly connected to the CAN ports of the TQMa8x and are available at the two 3-pin connectors X18 and X19. Both interfaces are galvanically isolated up to 1 kV. The CAN interfaces are not galvanically isolated from each other. The CAN signals can be terminated with 120 Ω via DIP switches S10 and S11.

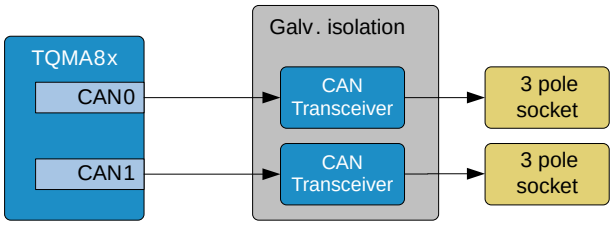

Figure 11: Block diagram CAN-FD

Table 13: CAN termination

DIP switch	Interface	ON	OFF
S10-1 & S10-2	CAN0	CAN0 terminated with 120 Ω	CAN0 not terminated
S11-1 & S11-2	CAN1	CAN1 terminated with 120 Ω	CAN1 not terminated

3.14.4 MLB

A MLB (Media Local Bus or MediaLB) is available on the CPU. This interface serves as an inter-chip bus for the connection of MOST-PHYs (Media Oriented Systems Transport) or other MLB devices.
MLB can be implemented in two transmission modes, both of which are supported by the CPU. For applications with lower bandwidth, the 3-pin implementation (single-ended) is available, for applications with high data rates, the 6-pin implementation (differential). The latter allows a data rate of up to 294.912 MHz, the 3-pin version offers data rates of up to 49.152 MHz.
Only one of the interfaces can be used at a time.

The MLB signals are connected to the 40-pin Hi-Speed connector X21. The wiring is based on Media Local Bus Specification Version 4.2. 3.3 V and 5 V are available at the connector for the optional supply of expansion modules, each of which can supply up to 500 mA. The power drawn must be subtracted from the available power of the starter kit headers.

620 Ω pull-down resistors are fitted to the differential signals MLB_DATA_P and MLB_SIG_P. Further pull-up and pull-down resistors for the differential signals are not populated, as these are usually implemented by the MLB controller.
The differential MLB signals are extended and have a differential impedance of 100 Ω.
Pull-down circuits for single-ended signals are populated.

Table 14: Pinout X21

Pin	Signal	Note
1	V_3V3_MB	-
2	V_5V	-
5	MLB_CLK	47 kΩ PD, 100 Ω + 27 pF PD
9	MLB_DATA	47 kΩ PD, 100 Ω
13	MLB_SIG	47 kΩ PD, 100 Ω
19	MLB_CLK_N	100 Ω nach MLB_CLKP
21	MLB_CLK_P	-
25	MLB_DATA_N	100 Ω nach MLB_DATA_P
27	MLB_DATA_P	-
31	MLB_SIG_N	100 Ω nach MLB_SIG_P
33	MLB_SIG_P	-
All pins not listed are connected to GND		

3.14.5 USB debug

For the output of debug messages of the TQMa8x, one UART of the ARM core, a separate UART of the SCU and two further UARTS of the M4 CPUs are used. These four UARTs are converted to USB by the FTDI FT4232. The FT4232 is a 4-port bridge.

All four COM ports are provided together on one USB port. The interface is supplied from the external USB host and is thus independent of the MBa8x.

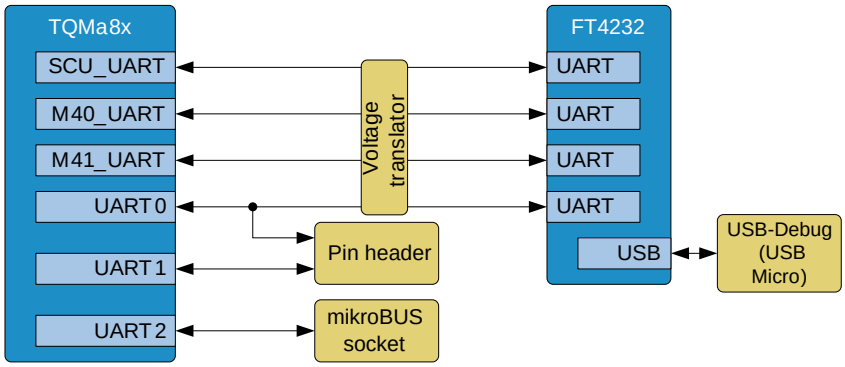

Figure 12: Block diagram USB debug

3.14.6 Ethernet

The i.MX 8 CPU provides two independent RGMII interfaces. On the MBa8x, both interfaces are used to provide two Gigabit Ethernet ports. The PHYs support IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T.

The I/O voltage of the RGMII signals is 1.8 V. Both PHYs are connected with their own PHY reset and interrupt signals. Furthermore, the interrupt signal of the ENET0-PHY is connected to the module.

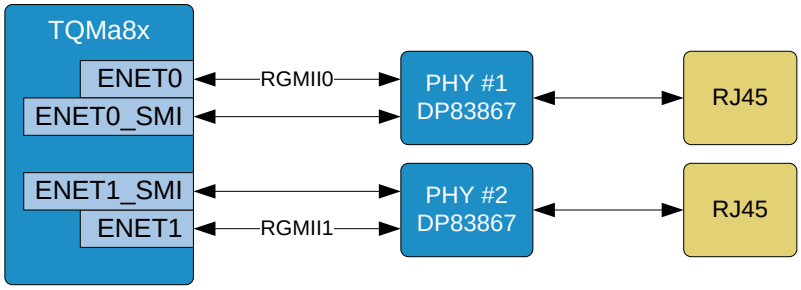

Figure 13: Block diagram Ethernet

Table 15: Ethernet Reset and Interrupt signals

Signal	TQMa8x signal	Pin
ENET0_INT#	ESAI1_TX0	X2-A33
ENET0_RST#	ESAI1_SCKR	X2-A34
ENET1_RST#	ESAI1_FSR	X2-A35

The PHY DP83867 has boot straps to start with configurable default values. All boot straps can be customized by placement options. Further information is available in the MBa8x schematics.

As both Ethernet interfaces have their own MDIO signals, the PHY addresses can be selected as desired. Address 0x00 is assigned to the PHY of Ethernet 0, address 0x03 to that of Ethernet 1.

The possible data throughput is influenced by the system load and the software used. With the standard BSP, the following transfer rates can be achieved on the MBa8x with a Gigabit link:

Table 16: Characteristics Ethernet 0 (X39)

Parameter	Min.	Typ.	Max.	Unit	Remark
Upstream	-	941	1000	Mbit/s	Remote station Full-Duplex 1 Gbit over CAT 5e
Downstream	-	895	1000	Mbit/s	

Table 17: Characteristics Ethernet 1 (X40)

Parameter	Min.	Typ.	Max.	Unit	Remark
Upstream	-	941	1000	Mbit/s	Remote station Full-Duplex 1 Gbit over CAT 5e
Downstream	-	933	1000	Mbit/s	

3.14.7 GPIO

On the MBa8x, some GPIOs are provided by the TQMa8x. A distinction is made between general GPIO pins and those that are dedicated to the integrated auxiliary processors (SCU, ARM M4 CPUs). Some GPIOs are provided via a port expander. The voltage levels of some pins depend on other peripheral modules and may change during operation.

The following GPIOs are used:

Table 18: GPIO signals

Source	Alternative / Note	Signal	Voltage level
SCU_GPIO0_02	SCU_LED0	SCU_LED	1.8 V
SCU_GPIO0_03	GPIO0_IO30	EN_1V5_MPCIE	1.8 V
SCU_GPIO0_04	GPIO1_IO00	SWITCH_B#	1.8 V
SCU_GPIO0_05	GPIO1_IO01	EN_3V3_MPCIE	1.8 V
SCU_GPIO0_06	GPIO1_IO02	EN_12V	1.8 V
SCU_GPIO0_07	GPIO1_IO03	SCU_GPIO0_07	1.8 V
M40_GPIO0_00	GPIO0_IO08	M40_GPIO0_00	1.8 V
M40_GPIO0_01	GPIO0_IO09	M40_GPIO0_01	1.8 V
M41_GPIO0_00	GPIO0_IO12	M41_GPIO0_00	1.8 V
M41_GPIO0_01	GPIO0_IO13	M41_GPIO0_01	1.8 V
GPIO0_IO05	-	GPIO0_IO05	1.8 V / 3.3 V
GPIO2_IO02	-	MBUS_RST#	3.3 V
GPIO2_IO03	-	MBUS_INT	3.3 V
GPIO2_IO17	-	GPIO2_IO17	1.8 V
GPIO2_IO21	-	GPIO2_IO21	1.8 V
GPIO1_IO14	-	GPIO1_IO14	1.8 V
GPIO1_IO15	-	GPIO1_IO15	1.8 V
GPIO4_IO07	-	GPIO4_IO07	1.8 V
GPIO4_IO09	-	GPIO4_IO09	1.8 V
GPIO4_IO10	VSELECT Option	GPIO4_IO10	1.8 V
GPIO4_IO11	-	GPIO4_IO11	1.8 V
GPIO4_IO12	-	GPIO4_IO12	1.8 V
GPIO5_IO19	IO voltage depending on SD card speed	GPIO5_IO19	1.8 V / 3.3 V
GPIO5_IO20	IO voltage depending on SD card speed	GPIO5_IO20	1.8 V / 3.3 V
GPIO5_IO23	USDHC1_STROBE / IO voltage depending on SD card speed	GPIO5_IO23	1.8 V / 3.3 V
GPIO5_IO[29:24]	USDHC2-Interface	GPIO5_IO[29:24]	1.8 V
ESAI1_TX0	GPIO2_IO08	ENET0_INT#	1.8 V
ESAI1_SCKR	GPIO2_IO06	ENET0_RST#	1.8 V
ESAI1_FSR	GPIO2_IO04	ENET1_RST#	1.8 V
ESAI1_SCKT	GPIO2_IO07	USB_RST#	1.8 V
ESAI1_FST	GPIO2_IO05	PCIE_DISABLE#	1.8 V
ESAI1_TX2_RX3	GPIO2_IO10	PCIE_CLK_PD#	1.8 V
ESAI1_TX1	GPIO2_IO09	MIPI_DSI0_BLT_EN	1.8 V
ENET0_REFCLK_125M_25M	GPIO4_IO15	MIPI_DSI1_BLT_EN	1.8 V
ENET1_REFCLK_125M_25M	GPIO4_IO16	MIPI_DSI0_RESET#	1.8 V
ESAI1_TX5_RX0	GPIO2_IO13	MIPI_DSI1_RESET#	1.8 V
ESAI1_TX4_RX1	GPIO2_IO12	FAN_PWR	1.8 V
ESAI1_TX3_RX2	GPIO2_IO11	SWITCH_A#	1.8 V

3.14.8 Display interfaces

3.14.8.1 DisplayPort

In addition to the LVDS and DSI ports, a multifunctional HDMI/DP module is available. The following display specifications can be used with it:

- HDMI 2.0a
- Display port 1.3
- Embedded Display Port 1.4

On the MBa8x, the interface is implemented as DisplayPort as described in the i.MX8 QM/i.MX8 QXP Hardware Developers Guide. The series capacitors of 100 nF on the data lines are placed close to the module connector. ESD protection diodes are placed

close to the DP socket. A self-resetting fuse of 2 A is provided on the DP_PWR pin (DP spec requires a fuse of max. 3 A).

The connection of HDMI to this port is not provided!

Note: NXP explains in the i.MX8 QM/i.MX8 QXP Hardware Developers Guide	
	The Display Port silicon IP natively supports the DisplayPort Dual Mode (DP++). There are no current plans to support this functionality in the BSP or to validate this feature in silicon.

For this reason this functionality is not supported on the MBa8x.

3.14.8.2 HDMI In

The i.MX 8 provides an HDMI input. Thus, for example, image data can be converted to another display interface. HDMI-RX supports a resolution of up to 4K at 30 FPS. HEC (HDMI Ethernet Channel) is not supported.

The differential HDMI signals are extended and have a differential impedance of 100 Ω. HDMI_RX_MON_5V is connected to pin 18 (+5V) of the HDMI socket by means of 100 nF to ground. This 5 V, which is provided by the HDMI source, also supplies the pull-ups on the DDC lines. HDMI_RX_CEC (Consumer Electronics Control) is connected to 3.3 V via 27 kΩ and Schottky diode (pull-up).

ARC (Audio Return Channel): HDMI_RX_ARC_N remains unconnected. The shield of the HDMI socket is connected to GND.

3.14.8.3 LVDS

The i.MX 8 has two LVDS controllers, each with a dual LVDS interface or two channels. Each of the channels uses four differential lanes for transmission.

The mainboard allows a single LVDS or dual LVDS to be connected at a time. For this reason, 2x GPIO (BLT_EN, RESET#), one PWR_EN and one PWM signal are provided per LVDS interface. The GPIOs are multiplexed on the CPU instead of the dedicated I2C signals. The LVDSx_PWM and LVDSx_PWR_EN signals are already dedicated pins of the LVDS bus.

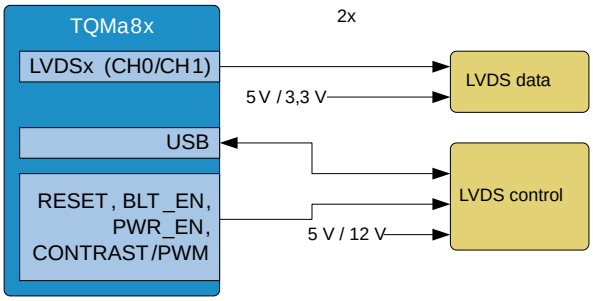

Figure 14: Block diagram LVDS

The differential LVDS signals are extended and have a differential impedance of 100 Ω. Furthermore, all signal lines are provided with ESD protection.

As with all TQ mainboards, there is no redriver and no ground lines between the differential pairs. Experience has shown that this limits the possible cable length to approx. 30 cm.

3.14.8.4 MIPI DSI

The TQMa8x has two MIPI DSI interfaces with four differential lanes each. In addition, the interface offers an I2C master for each of the two DSI ports as well as a dedicated GPIO and PWM pin.

These interfaces are intended for the connection of an adapter board for embedded display modules. This allows easy accessibility and flexibility in the choice of display, but requires the use of an adapter board.

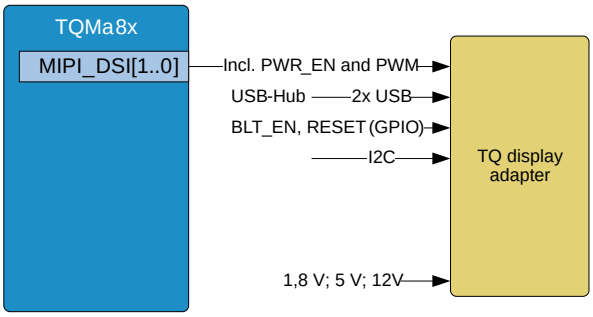

Figure 15: Block diagram MIPI-DSI

The pinout of the connector for the MIPI-DSI adapter was defined based on the existing TQ MIPI-CSI adapter. Control signals that are not included in the corresponding bus are provided via GPIO. The differential DSI signals are extended and have a differential impedance of 100 Ω. Furthermore, all signal lines are provided with ESD protection.
A total of up to 1.5 Gbps can be transmitted. The supported image/video formats can be found in the i.MX 8 specification.
The power drawn from the connectors must be subtracted from the power budget of the pin headers in each case!

Table 19: TQ MIPI-DSI adapter

Description	Signal	Nr.	Nr.	Signal	Description
1,8V	MIPI_DSI0_PWM	1	2	MIPI_DSI1_PWM	1,8V
-	GND	3	4	GND	-
GPIO (1,8V)	MIPI_DSI0_BLT_EN	5	6	MIPI_DSI1_BLT_EN	GPIO (1,8V)
1,8V	MIPI_DIS0_GPIO0_01	7	8	MIPI_DSI1_GPIO0_01	1,8V
GPIO (1,8V)	MIPI_DSI0_RESET#	9	10	MIPI_DSI1_RESET#	GPIO (1,8V)
1,8 V	V_1V8_STBY_DSI	11	12	V_12V_DSI	12 V
-	GND	13	14	GND	-
1,8 V	MIPI_DSI0_D3-	15	16	MIPI_DSI1_D3-	1,8 V
1,8 V	MIPI_DSI0_D3+	17	18	MIPI_DSI1_D3+	1,8 V
-	GND	19	20	GND	-
1,8 V	MIPI_DSI0_D2-	21	22	MIPI_DSI1_D2-	1,8 V
1,8 V	MIPI_DSI0_D2+	23	24	MIPI_DSI1_D2+	1,8 V
-	GND	25	26	GND	-
1,8 V	MIPI_DSI0_D1-	27	28	MIPI_DSI1_D1-	1,8 V
1,8 V	MIPI_DSI0_D1+	29	30	MIPI_DSI1_D1+	1,8 V
-	GND	31	32	GND	-
1,8 V	MIPI_DSI0_D0-	33	34	MIPI_DSI1_D0-	1,8 V
1,8 V	MIPI_DSI0_D0+	35	36	MIPI_DSI1_D0+	1,8 V
-	GND	37	38	GND	-
1,8 V	MIPI_DSI0_CLK-	39	40	MIPI_DSI1_CLK-	1,8 V
1,8 V	MIPI_DSI0_CLK+	41	42	MIPI_DSI1_CLK+	1,8 V
-	GND	43	44	GND	-
1,8 V	MIPI_DSI0_I2C_SDA	45	46	MIPI_DSI1_I2C_SDA	1,8 V
1,8 V	MIPI_DSI0_I2C_SCL	47	48	MIPI_DSI1_I2C_SCL	1,8 V
-	GND	49	50	GND	-
from USB2.0 Hub	USB20_H3_DM	51	52	USB20_H4_DM	from USB2.0 Hub
from USB2.0 Hub	USB20_H3_DP	53	54	USB20_H4_DP	from USB2.0 Hub
-	GND	55	56	GND	-
5 V	V_DSI0_VBUS	57	58	V_DSI1_VBUS	5 V
5 V	V_5V_STBY_DSI	59	60	V_5V_STBY_DSI	5 V

3.14.9 MIPI CSI

The TQMa8x has two MIPI-CSI interfaces with four lanes each. Both CSI interfaces are assigned an I2C, two GPIO signals (reset, power enable) and a master clock output as standard. Trigger and sync signals are also provided with two M4 GPIOs each.

These interfaces are intended for connecting an adapter board for embedded camera modules. This allows easy accessibility and flexibility in camera selection, but requires the use of an adapter board. Up to 1.5 Gbps are transmitted and a maximum image format of 4K with 30 FPS is processed.

The differential CSI signals are elongated and have a differential impedance of 100 Ω.

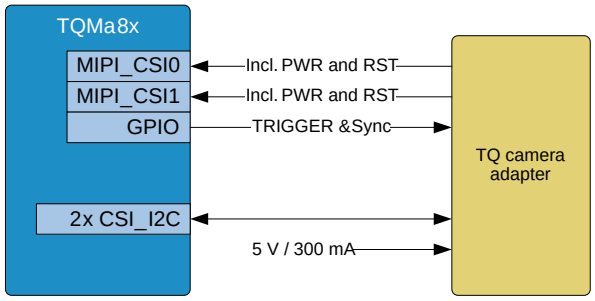

Figure 16: Block diagram MIPI-CSI / TQ Camera Interface

The interface is already used on the MB-SMARC-2 and other TQ boards. Functions have been added to the interface in coordination with TQ EMB.

Table 20: TQ MIPI-CSI adapter

Description	Signal	Nr.	Nr.	Signal	Description
-	GND	1	2	GND	-
GPIO 1,8V	MIPI_CSI0_EN	3	4	CAM1_PWR#	GPIO 1,8V
GPIO 1,8V	MIPI_CSI0_RST#	5	6	MIPI_CSI1_RST#	GPIO 1,8V
GPIO 1,8V	M40_GPIO0_01	7	8	M41_GPIO0_00	GPIO 1,8V
GPIO 1,8V	M40_GPIO0_00	9	10	M41_GPIO0_01	GPIO 1,8V
Reserved	NC	11	12	NC	Reserved
-	GND	13	14	GND	-
-	MIPI_CSI0_DATA3_N	15	16	MIPI_CSI1_DATA3_N	-
-	MIPI_CSI0_DATA3_P	17	18	MIPI_CSI1_DATA3_P	-
-	GND	19	20	GND	-
-	MIPI_CSI0_DATA2_N	21	22	MIPI_CSI1_DATA2_N	-
-	MIPI_CSI0_DATA2_P	23	24	MIPI_CSI1_DATA2_P	-
-	GND	25	26	GND	-
-	MIPI_CSI0_DATA1_N	27	28	MIPI_CSI1_DATA1_N	-
-	MIPI_CSI0_DATA1_P	29	30	MIPI_CSI1_DATA1_P	-
-	GND	31	32	GND	-
-	MIPI_CSI0_DATA0_N	33	34	MIPI_CSI1_DATA0_N	-
-	MIPI_CSI0_DATA0_P	35	36	MIPI_CSI1_DATA0_P	-
-	GND	37	38	GND	-
-	MIPI_CSI0_CLK_N	39	40	MIPI_CSI1_CLK_N	-
-	MIPI_CSI0_CLK_P	41	42	MIPI_CSI1_CLK_P	-
-	GND	43	44	GND	-
-	MIPI_CSI0_SDA	45	46	MIPI_CSI1_SDA[3]	-
-	MIPI_CSI0_SCL	47	48	MIPI_CSI1_SCL[4]	-
-	GND	49	50	GND	-
Master Clock for CSI1	MIPI_CSI0_MCLK_OUT	51	52	MIPI_CSI1_MCLK_OUT	Master Clock for CSI1
-	GND	53	54	GND	-
Reserved for other voltage	NC	55	56	V_5V_STBY	Always on
Reserved for other voltage	NC	57	58	V_5V_STBY	Always on
Reserved for other voltage	NC	59	60	V_5V_STBY	Always on

300 mA (2x150 mA) is budgeted for the TQ camera adapter on the 5 V level. The current consumption has been determined on the basis of the worst-case power consumption of the reference camera "Li-Apollo-adp-IMX185" from Leopard Imaging Inc of 0.63 W. If higher power is required for the connected cameras, this must be subtracted from the power provided at the starter kit headers.

The components under the area for the adapter board must not exceed a height of 2 mm!

[3] Not functional, because connected to the module at X2-A71, where MIPI_CSI1_SCL is located

[4] Not functional, because connected to the module at X2-A72, where MIPI_CSI1_SDA is located.

3.14.10 Mini PCIe

A mini PCIe card slot is realised on the MBa8x. This is connected to the PCIe0 interface. The interface is wired with all signals provided by the standard (e.g. USB, I2C, PCIe). The clock is generated externally from a central location.

Any standard-compliant mini-PCIE card can be used, as long as the necessary software drivers are available.

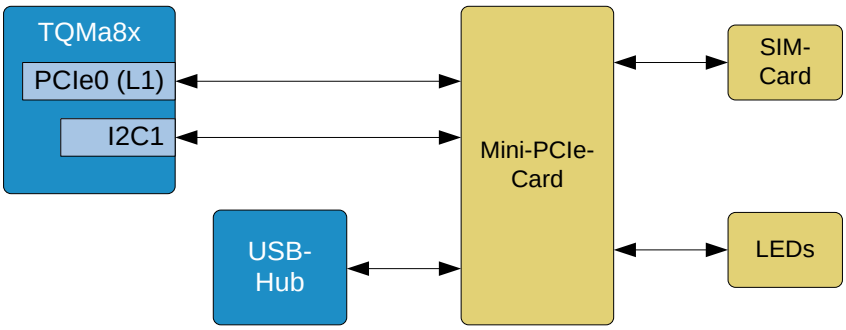

Figure 17: Block diagram Mini-PCIe

The PCIE_PERST#, PCIE_WAKE# and PCIE_CLKREQ# signals have an IO voltage of 3.3 V. These can therefore be connected directly to the Mini PCIe card. The PCIE_DISABLE# signal is connected via GPIO.

The differential PCIe signals are elongated and have a differential impedance of 85 Ω.

3.14.11 PCIe M.2

PCIe1 is made available by using a 2230 form factor M.2 slot with "E" coding. I2C is also connected to this slot, as it is to the Mini PCIe slot.

The connection is the same as for the MB-SMARC-2, with the difference that I2C (pin 58 and 60) is connected with 0 Ω. In addition, a USB 2.0 port of the USB 3.0 hub is connected.

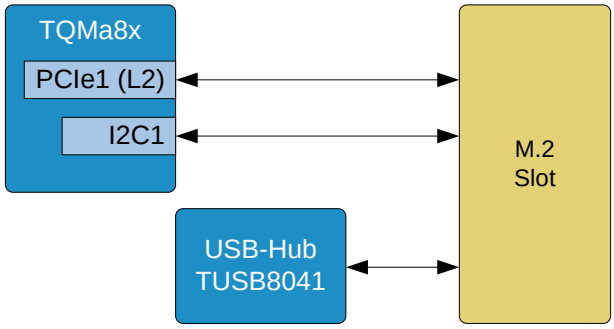

Figure 18: Block diagram PCIe M.2

The differential PCIe signals are elongated and have a differential impedance of 85 Ω. Furthermore, the data lines have the necessary series elements. The signals PCIE_PERST#, PCIE_WAKE# and PCIE_CLKREQ# are connected to the corresponding connector pins.

3.14.12 PCIe-Clock

Based on previous experience with i.MX processors, the internal PCIe reference clock does not meet JEDEC jitter specifications. NXP therefore recommends an additional clock driver to provide i.MX 8 and PCIe endpoints with a stable reference clock. The 9FGV0441 clock generator from IDT is used for this purpose. The external reference clock is not optional, but is the only possible clock source for PCIe modules.

In the circuit diagram of the reference circuit from NXP i.MX8 MEK Platform MCIMX8QM-CPU (EVK) it is noted:

"For simple PCIe Gen1/2 configuration, the CPU's internal REFCLK generator should be used. Peripheral CLKREQ_B should drive the CPU and no external generator is necessary. For most customer Gen1/2 applications, REFCLK should be automatically recovered from within the PCIe lanes and not sent separately."

Furthermore, it is possible to control the clock generator via I2C.

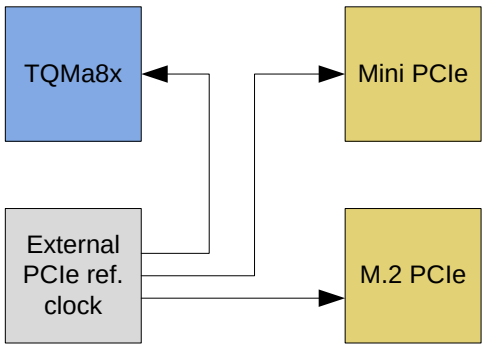

Figure 19: Clock supply PCIe

All PCIe-CLK lines are routed with a differential impedance of 100 Ω. The clock line to the processor is not terminated to ground with 49.9 Ω as required in i.MX8 QM/i.MX8 QXP Hardware Developers Guide. The termination is already included in the clock IC.

A quartz with a load capacitance of 8 pF is used. No capacitors are provided in series in the clock lines. A placement option is provided on all OE pins, which allows the clocks to be switched off.

The reference input of the processor is connected to DIF0. The pull-up for switching off the clock remains unpopulated. The reference input of the Mini PCIe slot is connected to DIF1.

DIF1 is activated by switching on V_3V3_MPCIE. DIF2 is connected to the reference input of the M.2 slot and is continuously active. A placement option to switch off the output is not provided.

DIF3 is not connected.

3.14.13 SATA M.2

An M.2 socket with "B" coding is used for connecting a SATA SSD. In addition, mounting options are available for the 2242 and 2280 form factors.

The differential signals are elongated and have a differential impedance of 85 Ω. 10 nF coupling capacitors are placed in the data lines. According to the M.2 specification, a maximum of 2.5 A is provided.

3.14.14 SIM

A SIM card holder (X12) is provided for the use of a GSM card.

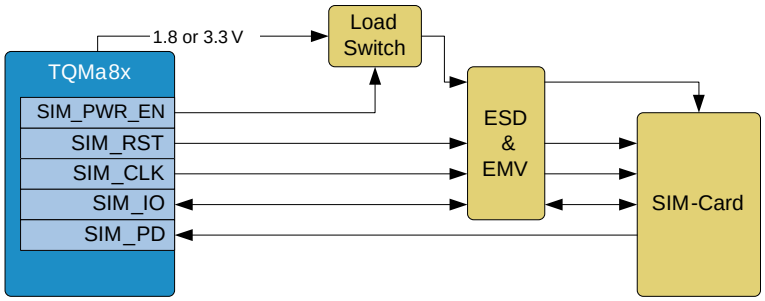

Figure 20: Block diagram SIM card

3.14.15 USB hosts/hubs

The TQMa8x provides two USB OTG interfaces, of which USB OTG2 also supports USB 3.0. Due to specific limitations of the i.MX 8 USB controllers, only USB OTG2 can be used as interface for a USB hub. To provide four host interfaces, the TUSB8041 USB hub is used. The hub has one upstream and four downstream ports.

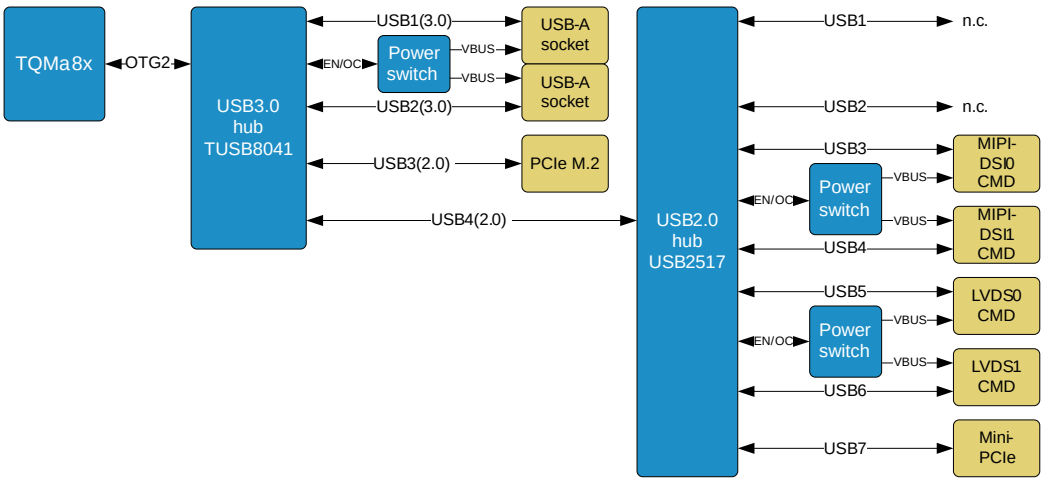

Figure 21: Block diagram USB hub structure of the MBa8x

The USB 3.0 OTG port, consisting of the OTG2 signals and the super speed signals, is used as the upstream port. The reset pin of the hub is connected to USB_RST# via an open-drain buffer and simultaneously brought to 3.3 V level.

USB hosts 1 and 2 are connected as USB 3.0 hosts to a dual USB type A socket (X36). USB host 3 can be tapped at the PCIe M.2 slot (X47). On the contrary, the USB 2.0 hub USB2517 is connected to USB host 4, which serves all internal USB 2.0 hosts. Four ports are used for the LVDS[1:0] CMD and MIPI-DSI[1:0] interfaces. A maximum of 500 mA can be drawn from each of these connectors. The power drawn must be subtracted from the power available at the starter kit headers.

An additional 1.1 V is required for the TUSB8041. These are generated with the DC/DC converter AP7173-FN. Power distribution switches are used to supply the USB hosts with 5 V (VBUS). The following table shows the characteristics of the VBUS supply:

Table 21: Power-Distribution TUSB8041

USB-Hub	Interface	Power-Switch	Features	Max. current	Current-threshold
1	USB-Host	FPF2165R	Thermal-Shutdown; Reverse Current Protection	900 mA	0.970 A …1.186 A
2	USB-Host	FPF2165R		900 mA	0.970 A …1.186 A
3	PCIe-M.2	No VBUS supply	-	-	-
4	USB 2.0 Hub	No VBUS supply	-	-	-

The signals I2C1_SCL/SDA_3V3 are used for the I2C bus. These are already provided for the temperature sensor by a level translator from I2C1_SCL/SDA_1V8.

The USB 3.0 OTG port of the TQMa8x provides a theoretical data rate of 5 Gbps. This is divided among the connected ports of the USB 3.0 hub. Depending on the software and hardware used, the effective read and write rates of the ports can vary.

Table 22: Properties USB host 1 and 2

Parameter	Min.	Typ.	Max.	Unit	Note
Voltage	4.75	5	5.25	V	-
Current	-	-	900	mA	Current limitation to 0,970 A…1,186 A
Voltage dip at load	-	-89	-155	mV	With a load of 500 mA or 950 mA
Read rate	-	121	-	MB/s	Tested only on host 1
Write rate	-	73.2	-	MB/s	Tested only on host 1

3.14.16 USB OTG

USB OTG1 is connected as USB 2.0 OTG to a separate Micro AB USB socket and can be used for the serial downloader. The power supply of the USB OTG port is realized via a power switch.

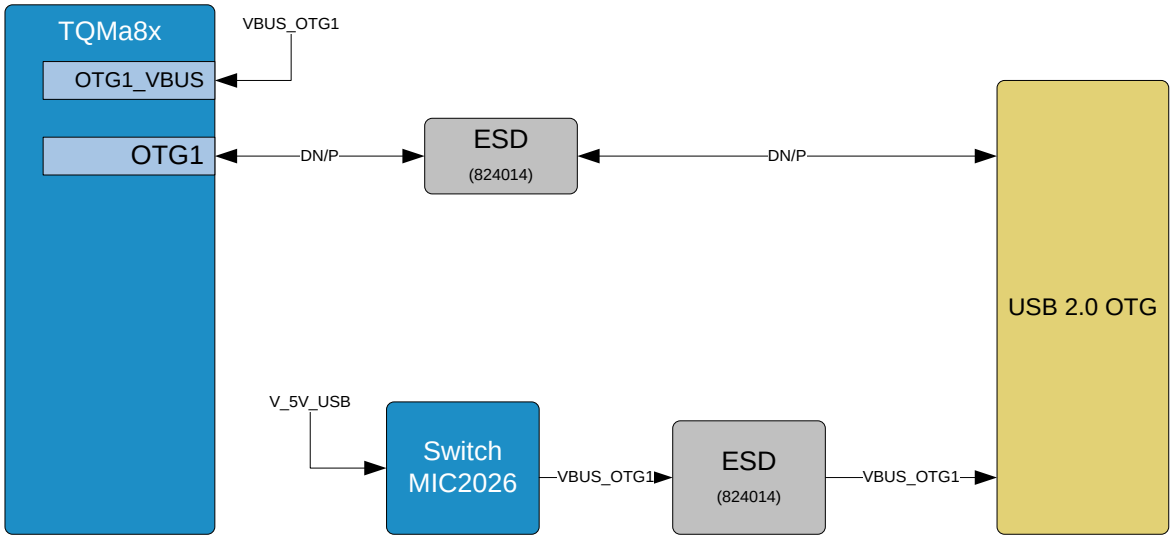

Figure 22: Block diagram USB OTG

The processor supports USB 2.0 with Hi-Speed, Full-Speed and Low-Speed. Depending on the software and hardware used, the effective read and write rates of the ports may vary.

Table 23: Properties of USB-OTG

Parameter	Min.	Typ.	Max.	Unit	Note
Voltage	4,75	5	5,25	V	-
Current	500	1000	1250	mA	-
Voltage dip at load	-	-92	-	mV	With a load of 500 mA
Read rate	-	20,1	-	MB/s	-
Write rate	-	8,8	-	MB/s	-

3.14.17 SD card

The SD card connector is directly connected to the SDHC controller of the TQMa8x module via a 4-bit wide data interface.

The SDHC controller in the TQMa8x basically supports UHS-I SD cards in transfer mode SDR104 according to the SD card standard 3.0. This allows transfer rates of up to 104 Mbyte/s.

The SD card is permanently supplied with 3.3 V, the pull-ups are also connected to this voltage. The signals SW1_WP and SD1_CD# have a fixed I/O voltage of 1.8 V. Their 10 kΩ pull-ups are therefore connected to 1.8 V.

It is possible to boot from SD card (see chapter 3.5). All data lines are provided with ESD protection.

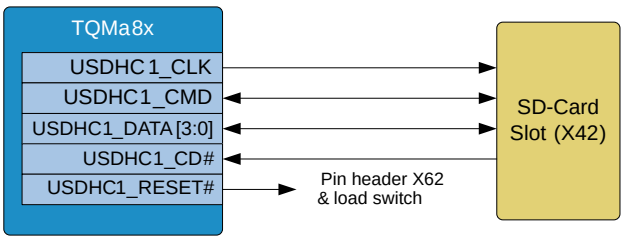

Figure 23: Block diagram SD card

Note: SD card initialisation after reset	
	A load switch is placed on the mainboard to reinitialize the SD card in the event of a system reset from the host. This is controlled with the signal USDHC1_RESET# (multiplexed as GPIO4_IO07) and is available at pin header X62.

The SDHC controller in the TQMa8x supports SD cards with UHS I transfer mode according to the SD card standard 3.1. Transfer rates of 104 Mbyte/s are thus possible.

3.14.18 mikroBUS

A mikroBUS slot is provided for system expansion. mikroBUS is an open standard for which numerous modules or extension boards are available. The specification explicitly stipulates that a microBUS slot must be designed with placement printing.

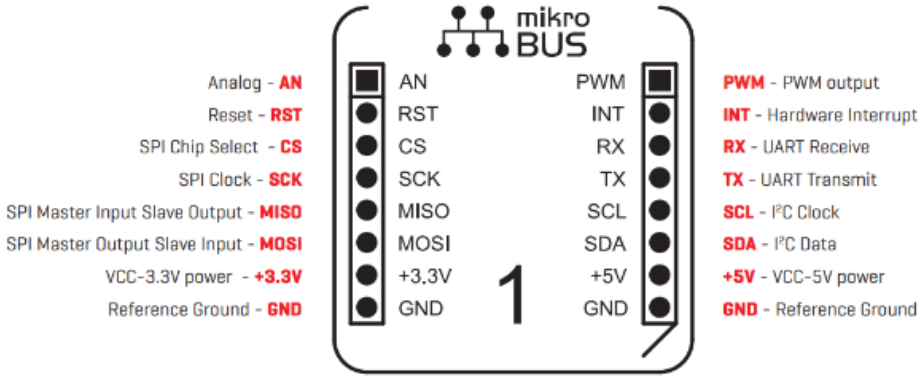

Figure 24: Pinout microbus (source: MikroElektronika)

The mikroBUS modules require 3.3 V and 5 V. These are already available in the system. PTC fuses for 0.75 A are provided for fuse protection.

With regard to the power consumption, there are no max. specified values. Since these are low-power modules, a current consumption of 100 mA per supply voltage is provided for in the calculated current budget - this proved to be sufficient during a random check of microBUS modules. If more power is required, this must be subtracted mathematically from the available power at the starter kit pin headers.

Only modules with 3.3 V IO voltage can be used. Therefore, two level converters are available for the connection to the 1.8 V logic of the TQMa8x.

Excluded from the level conversion is the analog signal (AN) with a maximum input level of 5 V, the I2C bus (I2C1_3V3) and the reset input. The I2C bus can only be operated with 3.3 V level and must be decoupled by removing 0 ohm resistors in case of conflict with the adapter board to be used. The reset input is decoupled via an open drain buffer.

Table 24: mikroBus signals

Pin	Identifier	Connection	Note
1-1	AN	ADC_IN0	0 Ω in series
1-2	RST	GPIO	0 Ω in series
1-3	CS	SPI0	33 Ω in series
1-4	SCK	SPI0	33 Ω in series
1-5	MISO	SPI0	100 Ω in series
1-6	MOSI	SPI0	33 Ω in series
1-7	+3.3V	-	100 mA budgeted, 0,75 A PTC
1-8	GND	GND	-
2-1	PWM	PWM2	Not available for DualMax variants
2-2	INT	GPIO	100 Ω in Serie
2-3	RX	UART2	33 Ω in Serie
2-4	TX	UART2	33 Ω in Serie
2-5	SCL	I2C1_3V3	100 Ω in series
2-6	SDA	I2C1_3V3	0 Ω in series
2-7	+5V	-	0 Ω in series
2-8	GND	GND	100 mA budgeted, 0,75 A PTC

3.14.19 ADC

For the evaluation of the ADC interface different signals and voltages are connected to the ADC inputs. The circuit is intended for test purposes and does not allow high-precision measurements.

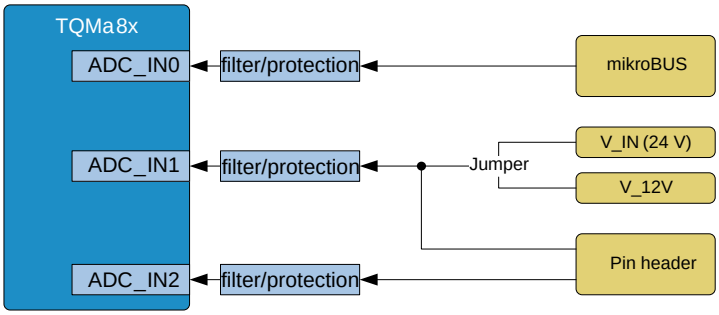

Figure 25: Block diagram ADC

The input voltage and the 12 V level can be connected to ADC_IN1 by using jumpers. Furthermore, the input signal is connected to pin 15 of header X64 and can be supplied with up to 30 V from there.
ADC_IN2, on the other hand, is connected directly to pin 17 of header X64 and can be supplied with up to 5 V.
The scaling factors and cut-off frequencies are shown in the table below.

Table 25: Values ADC circuit

Channel	Identifier	Vin	R1	R2	Scaling factor	Cut-off frequency with 100 nF
ADC_IN0	mikroBUS	5 V	4,32 kΩ	2,4 kΩ	0,3571	368,4 Hz
ADC_IN1	V_IN / V_12V	30 V	21,5 kΩ	1,37 kΩ	0,06	74,0 Hz
ADC_IN2	Pin header	5 V	4,32 kΩ	2,4 kΩ	0,3571	368,4 Hz

3.14.20 MBa8x headers

The MBa8x provides four 100 mil headers. All signals, which are not used on the MBa8x, mainly low-speed signals such as GPIO, SPI and UART, are made available on these headers.

Besides the signals, 1.8 V, 3.3 V, 5 V and 12 V are available on each header. The maximum current load of the individual voltages on the headers depends on the load on other connectors. In total, no more than the specified maximum current may be drawn at the following interfaces:

Table 26: Current consumption headers

Rail	I_{max}	Remark
V_12V	2.5 A	Sum of currents at X4, X7, X60, X61, X62, X63, X64
V_5V	1.5 A	Sum of currents at X4, X7, X8, X11, X21, X24, D29, X57, X60, X61, X62, X63, X64
V_3V3_MB	0.6 A	Sum of currents at X8, X11, X21, D29, X47, X61, X62, X63, X64
V_1V8	0.7 A	Sum of currents at X60, X61, X62, X63, X64

Table 27: Pinout Header X61

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
P	12 V	Power	V_12V	1	2	V_3V3_MB	Power	3.3 V	P
P	5 V	Power	V_5V	3	4	V_1V8	Power	1.8 V	P
P	0 V	Power	GND	5	6	GND	Power	0 V	P
I	1.8 V	SNVS	TAMPER_IN0	7	8	SCU_UART_RX	SCU	1.8 V	I
I	1.8 V	SNVS	TAMPER_IN1	9	10	SCU_UART_TX	SCU	1.8 V	O
O	1.8 V	SNVS	TAMPER_OUT0	11	12	SCU_GPIO0_07	SCU	1.8 V	I/O
O	1.8 V	SNVS	TAMPER_OUT1	13	14	GND	Power	0 V	P
I/O	VAR	GPIO	GPIO5_IO24	15	16	I2C1_SCL	I2C1	1.8 V	O
I/O	VAR	GPIO	GPIO5_IO25	17	18	I2C1_SDA	I2C1	1.8 V	I/O
I/O	VAR	GPIO	GPIO5_IO26	19	20	I2C1_3V3_SDA	I2C1	3.3V	I/O
I/O	VAR	GPIO	GPIO5_IO27	21	22	I2C1_3V3_SCL	I2C1	3.3V	O

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
I/O	VAR	GPIO	GPIO5_IO28	23	24	GPIO4_IO12	GPIO	1.8 V	I/O
I/O	VAR	GPIO	GPIO5_IO29	25	26	GPIO4_IO11	GPIO	1.8 V	I/O
P	0 V	Power	GND	27	28	GPIO4_IO10	GPIO	1.8 V	I/O
I/O	1.8 V	ESAI0	ESAI0_SCKT	29	30	GPIO4_IO09	GPIO	1.8 V	I/O
I/O	1.8 V	ESAI0	ESAI0_SCKR	31	32	GND	Power	0 V	P
I/O	1.8 V	ESAI0	ESAI0_TX0	33	34	ESAI0_FST	ESAI0	1.8 V	O
I/O	1.8 V	ESAI0	ESAI0_TX1	35	36	ESAI0_FSR	ESAI0	1.8 V	O
I/O	1.8 V	ESAI0	ESAI0_TX3_RX2	37	38	ESAI0_TX2_RX3	ESAI0	1.8 V	I/O
I/O	1.8 V	ESAI0	ESAI0_TX5_RX0	39	40	ESAI0_TX4_RX1	ESAI0	1.8 V	I/O

Table 28: Pinout Header X62

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
P	12 V	Power	V_12V	1	2	V_3V3_MB	Power	3.3 V	P
P	5 V	Power	V_5V	3	4	V_1V8	Power	1.8 V	P
P	0 V	Power	GND	5	6	GND	Power	0 V	P
P	0 V	Power	GND	7	8	GND	Power	0 V	P
P	0 V	Power	GND	9	10	GND	Power	0 V	P
I/O	1.8 V	M4 GPIO	M40_GPIO0_00	11	12	QSPI0B_DQS	QSIOPI	1.8 V	I/O
I/O	1.8 V	M4 GPIO	M40_GPIO0_01	13	14	GND	Power	0 V	P
I/O	1.8 V	M4 GPIO	M41_GPIO0_00	15	16	QSPI0A_SS1#	QSPI	1.8 V	I/O
I/O	1.8 V	M4 GPIO	M41_GPIO0_01	17	18	QSPI0B_SS1#	QSPI	1.8V	I/O
P	0 V	Power	GND	19	20	GND	Power	0 V	P
I/O	1.8 V	M4_UART	M41_UART_TX	21	22	GPIO4_IO07	GPIO	1.8 V	I/O
O	1.8 V	M4_UART	M41_UART_RX	23	24	GPIO5_IO23	GPIO	VAR	I/O
P	0 V	Power	GND	25	26	GPIO0_IO05	SIM	VAR	I/O
O	1.8 V	M4_UART	M40_UART_RX	27	28	GND	Power	0 V	P
I/O	1.8 V	M4_UART	M40_UART_TX	29	30	UART1_RX	UART0	1.8 V	I
P	0 V	Power	GND	31	32	UART1_TX	UART0	1.8 V	O
I	1.8 V	UART0	UART0_RX	33	34	UART1_CTS#	UART0	1.8 V	I
O	1.8 V	UART0	UART0_TX	35	36	UART1_RTS#	UART0	1.8 V	O
I	1.8 V	UART0	UART0_CTS#	37	38	GND	Power	0 V	P
O	1.8 V	UART0	UART0_RTS#	39	40	RTC_EVENT#	SYSTEM	VAR	O

Table 29: Pinout Header X63

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
P	12 V	Power	V_12V	1	2	V_3V3_MB	Power	3.3 V	P
P	5 V	Power	V_5V	3	4	V_1V8	Power	1.8 V	P
P	0 V	Power	GND	5	6	GND	Power	0 V	P
O	1.8 V	MCLK	MCLK_OUT	7	8	MCLK_IN	MCLK	1.8 V	I
P	0 V	Power	GND	9	10	GND	Power	0 V	P
O	1.8 V	PWM	PWM3_OUT	11	12	QSPI1A_SCLK	QSPI	1.8 V	O
O	1.8 V	PWM	PWM2_OUT	13	14	GND	Power	0 V	P
P	0 V	Power	GND	15	16	QSPI1A_SS[0]#	QSPI	1.8 V	O
O	1.8 V	I2C	PMIC_I2C_SCL	17	18	QSPI1A_SS[1]#	QSPI	1.8 V	O
I/O	1.8 V	I2C	PMIC_I2C_SDA	19	20	QSPI1A_DQS	QSPI	1.8 V	I
P	0 V	Power	GND	21	22	QSPI1A_DATA3	QSPI	1.8 V	I/O
O	1.8 V	SYSTEM	IMX_MEMC_ON	23	24	QSPI1A_DATA2	QSPI	1.8 V	I/O
I	1.8 V	SYSTEM	IMX_ONOFF	25	26	QSPI1A_DATA1	QSPI	1.8 V	I/O
I	1.8 V	SYSTEM	RESET_IN#	27	28	QSPI1A_DATA0	QSPI	1.8 V	I/O

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
O	VAR	SYSTEM	RESET_OUT#	29	30	GND	Power	0 V	P
I/O	1.8 V	FTM	FTM_CH0	31	32	USB_HSIC_STROBE	HSIC	1.8 V	I/O
I/O	1.8 V	FTM	FTM_CH1	33	34	USB_HSIC_DATA	HSIC	1.8 V	I/O
I/O	1.8 V	FTM	FTM_CH2	35	36	GND	Power	0 V	P
I/O	1.8 V	GPIO	GPIO2_IO17	37	38	CAN2_RX	CAN2	1.8 V	I
I/O	1.8 V	GPIO	GPIO2_IO21	39	40	CAN2_TX	CAN2	1.8 V	O

Table 30: Pinout Header X64

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
P	12 V	Power	V_12V	1	2	V_3V3_MB	Power	3.3 V	P
P	5 V	Power	V_5V	3	4	V_1V8	Power	1.8 V	P
P	0 V	Power	GND	5	6	GND	Power	0 V	P
P	0 V	Power	GND	7	8	GND	Power	0 V	P
O	1.8 V	SYSTEM	PMIC2_FSOB	9	10	SPI0_CS1	SPI0	1.8 V	O
O	1.8 V	SYSTEM	PMIC1_FSOB	11	12	TEMP_EVENT#	SYSTEM	VAR	O
P	0 V	Power	GND	13	14	SPI1_CS0	SPI1	1.8 V	O
I/O	VAR	ADC	ADC_IN1	15	16	SPI1_CS1	SPI1	1.8 V	O
I/O	VAR	ADC	ADC_IN2	17	18	SPI1_SDI	SPI1	1.8 V	I
P	0 V	Power	GND	19	20	SPI1_SDO	SPI1	1.8 V	O
I/O	1.8 V	GPIO	GPIO1_IO14	21	22	SPI1_SCK	SPI1	1.8 V	O
I/O	1.8 V	GPIO	GPIO1_IO15	23	24	GND	Power	0 V	P
P	0 V	Power	GND	25	26	SPI2_CS0	SPI2	1.8 V	O
I	1.8 V	SAI1	SAI1_RXFS	27	28	SPI2_CS1	SPI2	1.8 V	O
I	1.8 V	SAI1	SAI1_RXC	29	30	SPI2_SDI	SPI2	1.8 V	I
P	0 V	Power	GND	31	32	SPI2_SDO	SPI2	1.8 V	O
O	1.8 V	SPDIF	SPDIF_EXT_CLK	33	34	SPI2_SCK	SPI2	1.8 V	O
P	0 V	Power	GND	35	36	GND	Power	0 V	P
I/O	1.8 V	I2C2	I2C2_SDA	37	38	SPDIF_RX	SPDIF	1.8 V	I
O	1.8 V	I2C2	I2C2_SCL	39	40	SPDIF_TX	SPDIF	1.8 V	O

3.14.21 JTAG

The JTAG interface is routed to a 20-pin header (X22). The required pull-ups of the lines TDI, TMS, TRST# and SRST# are available on the MBa8x. All signal lines use 1.8 V as reference voltage.

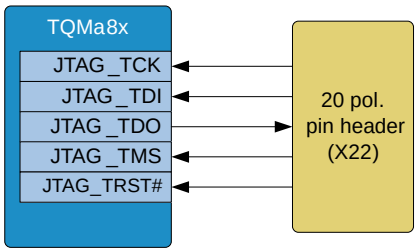

Figure 26: Block diagram JTAG

The supply voltage at the connector can be set to V_1V8 or V_3V3_MB by means of an assembly option.
The JTAG interface is not ESD protected.

3.15 Power supply

The MBa8x requires a supply voltage between 16 and 26.7 volts, nominal 24 volts. The following protective circuits are provided for the input voltage V_24V of the MBa8x:

- Fuse 7 A, slow blow
- Overvoltage protection (26.7 V … 29.5 V)
- Filter circuit for RF interference
- Reverse polarity protection

The voltages (rails) on the mainboard can be divided into three main paths, consisting of two LM25119s and a TPS45335. These supply the largest loads (TQMa8x, USB supply, display supply with 12 V).

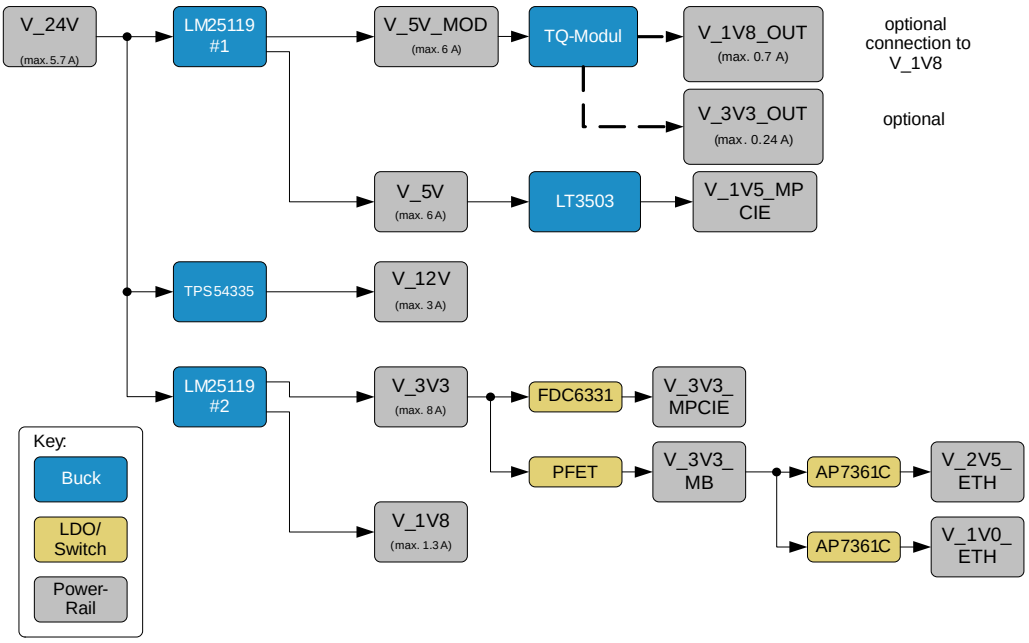

Figure 27: Block diagram supply

The design also allows power sequencing of all voltage levels used. With the exception of V_3V3 and V_V5_MOD, all voltages are switched on after the TQMa8x boots. The PMICx_PGOOD signals of the module are linked together on the mainboard by means of AND gate and together enable the other controllers in sequence step B. This release automatically activates all linear regulators (V_2V5_ETH, V_1V0_ETH, V_1V1_USB, V_3V3_MPCIE and V_1V5_MPCIE) as well as the DC/DC regulator for V_5V_CAN.

Attention: Voltages at headers	
	The internal voltages (1.8 V, 12 V, etc.) provided at the MBa8x headers are not additionally protected. Technically an overload of the fuse is therefore possible. The resulting total current consumption of the MBa8x should be kept below 7 A in total.

3.16 Cooling concept

The biggest power loss on the motherboard is caused by the voltage regulators. In addition, the module is a heat source that indirectly affects the mainboard. Depending on the application, further power losses can occur, mainly on additional external consumers on the starter kit headers, the Mini PCIe slot, etc.

The use of an optional heat sink or heat spreader is provided for evaluating the TQMa8x under high load cases. Three holes are available on the MBa8x for this purpose. The metallization of the hole has GND potential.

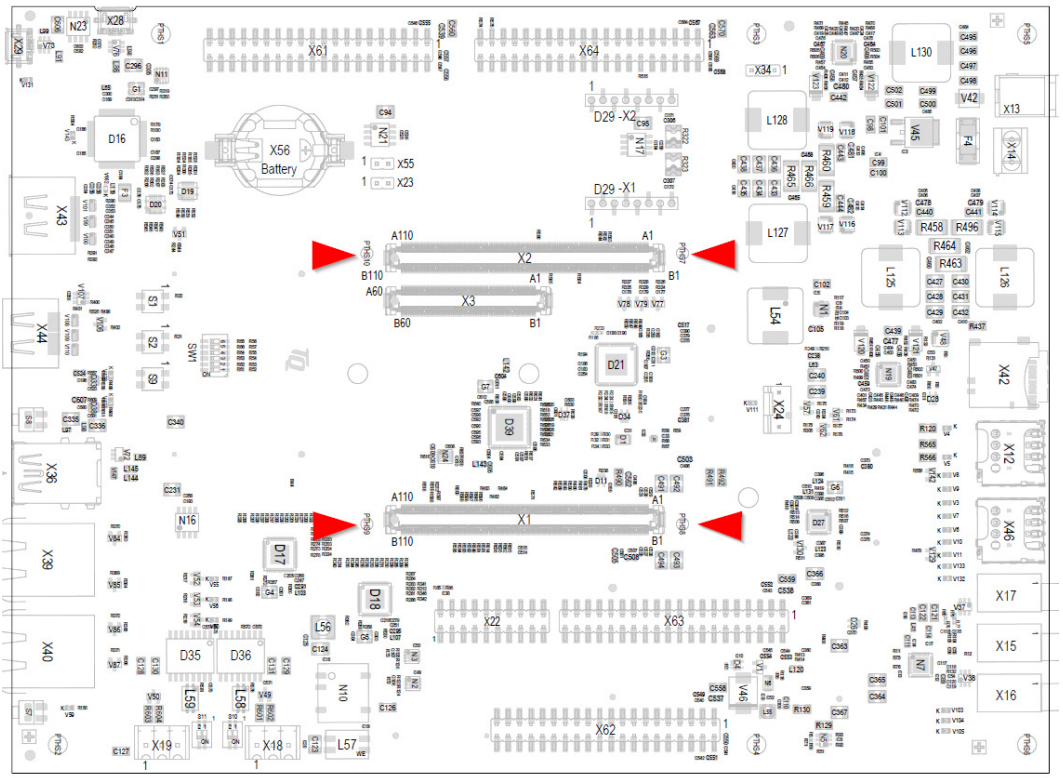

Figure 28: Position of heat sink mounting holes

Attention: TQMa8x heat dissipation	
	The i.MX 8 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8x must be taken into consideration when connecting the heat sink. The TQMa8x is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8x and thus malfunction, deterioration or destruction.

3.17 Fan

The CPU's power consumption requires a heat sink and fan for temperature management. The fan is controlled directly by the CPU. A four-pin header X24 with a 2.54 mm pitch is used for this.

FTM_CH2 is provided for the connection of a tachometer signal, PWM3_OUT for speed control and FAN_PWR for switching off the fan. Due to the good availability of compatible devices, 12 V is chosen as supply voltage for the fan, 5 V is optionally possible. In case the FTM module is not supported by the software, the pin can be multiplexed as GPIO.

4. SOFTWARE

No software is required for the MBa8x.
Suitable software is only required on the TQMa8x and is not a part of this User's Manual.
More information can be found in the TQ-Support Wiki for the TQMa8x.

5. MECHANICS

5.1 MBa8x dimensions

The MBa8x has overall dimensions (length × width) of 170 × 230 mm².
The MBa8x has a maximum height of approximately 26,4 mm.
The MBa8x has six 4.2 mm mounting holes for the housing, and four 2.7 mm mounting holes for a heat sink.
The MBa8x weighs approximately 294 g without TQMa8x.

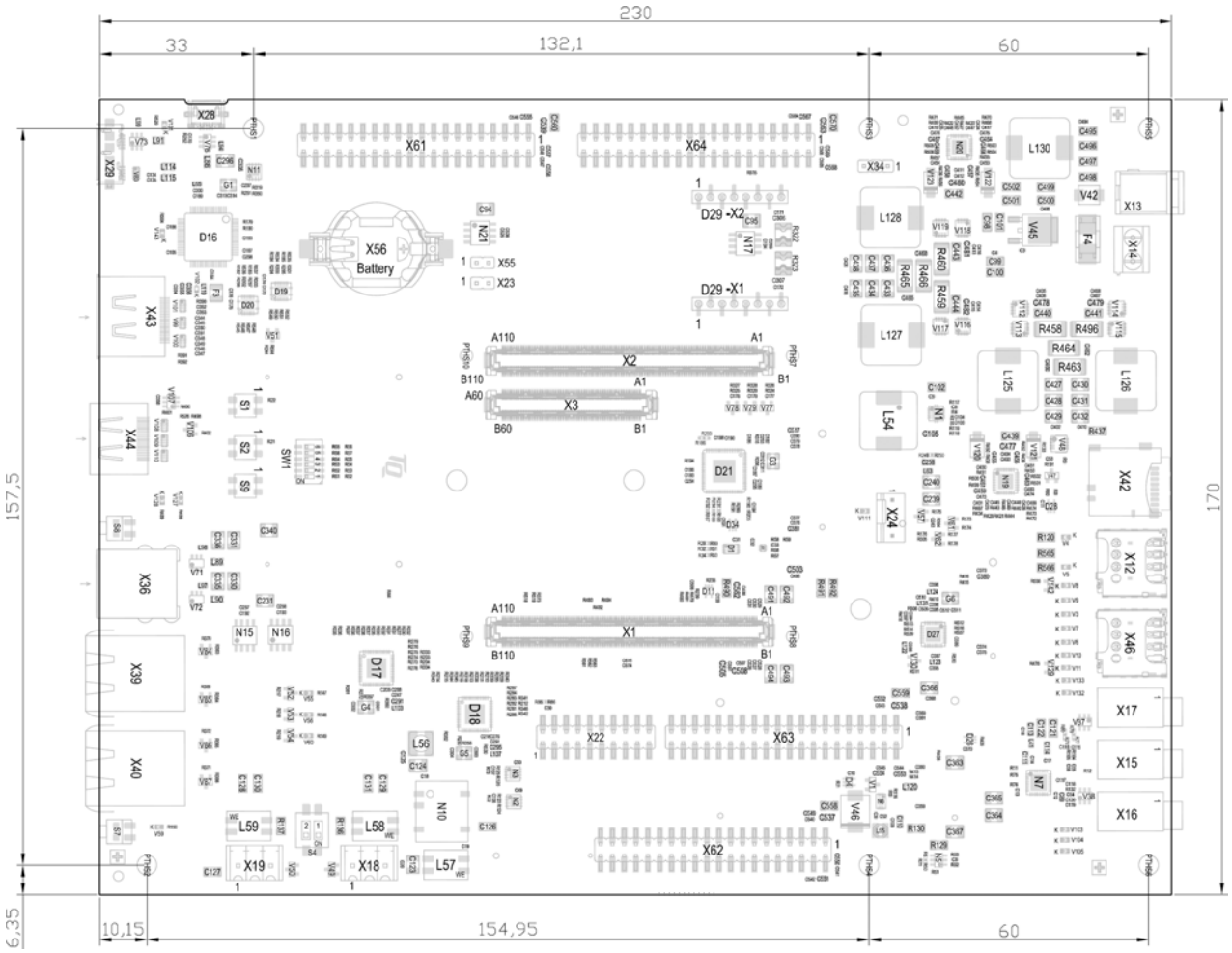

Figure 29: MBa8x dimensions

5.2 Notes of treatment

The TQMa8x is held in the mating connectors with a considerable retention force.
To avoid damaging the TQMa8x connectors as well as the carrier board connectors while removing the TQMa8x the use of the extraction tool MOZIA8X is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa8x for the extraction tool MOZIA8X.

5.3 Embedding in the target system

The MBa8x serves as a design base for customer products, as well as a reference platform during development.

5.4 Thermal management

MBa8x plus TQMa8x have a maximum peak power consumption of approx. 206 W.
Further power loss occurs mainly at externally connected devices.

Attention: TQMa8x heat dissipation	
	The i.MX 8 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8x must be taken into consideration when connecting the heat sink. The TQMa8x is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8x or the MBa8x and thus malfunction, deterioration or destruction.

5.5 Assembly

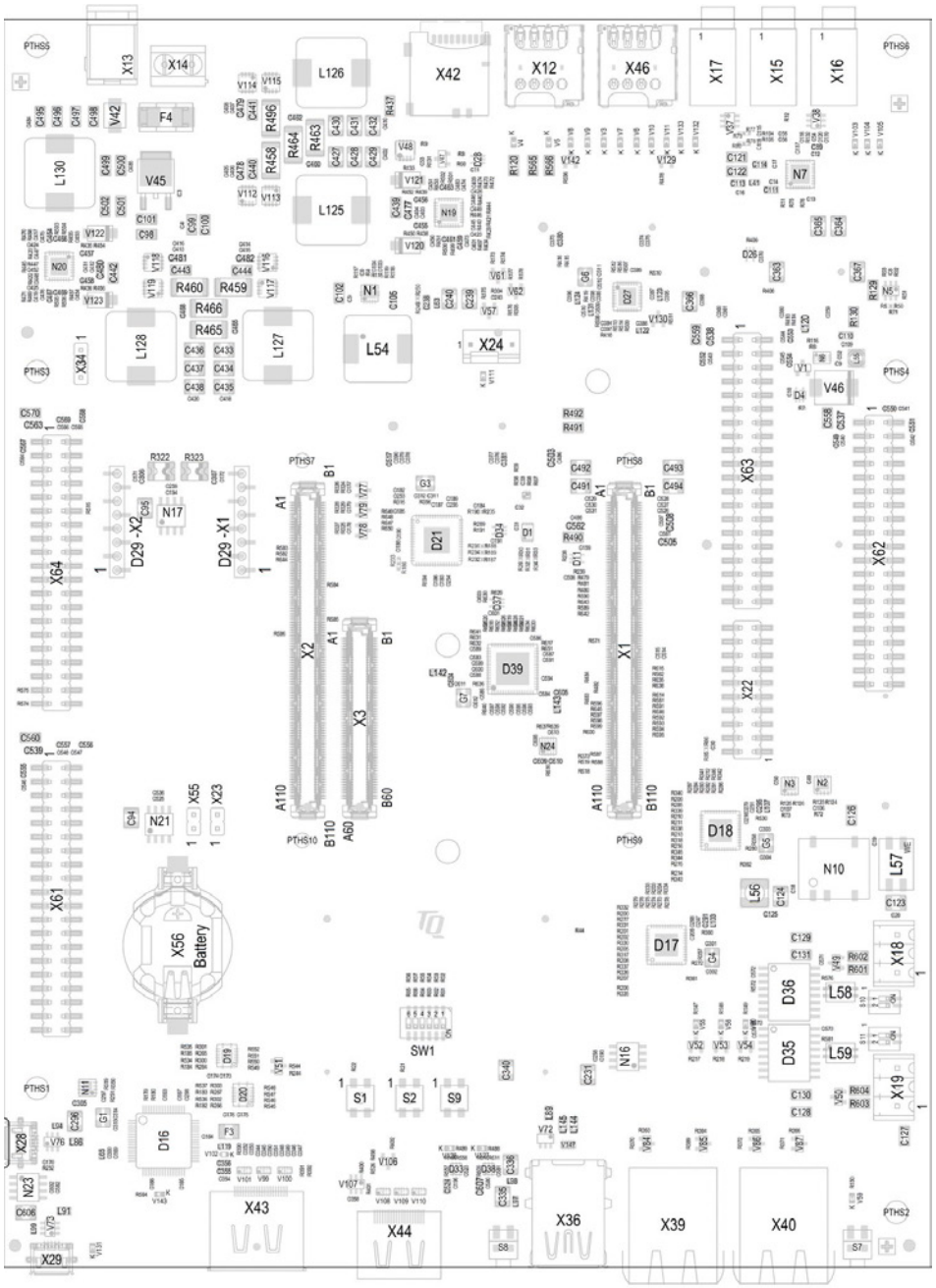

Figure 30: MBa8x, component placement top

5.5 Assembly (continued)

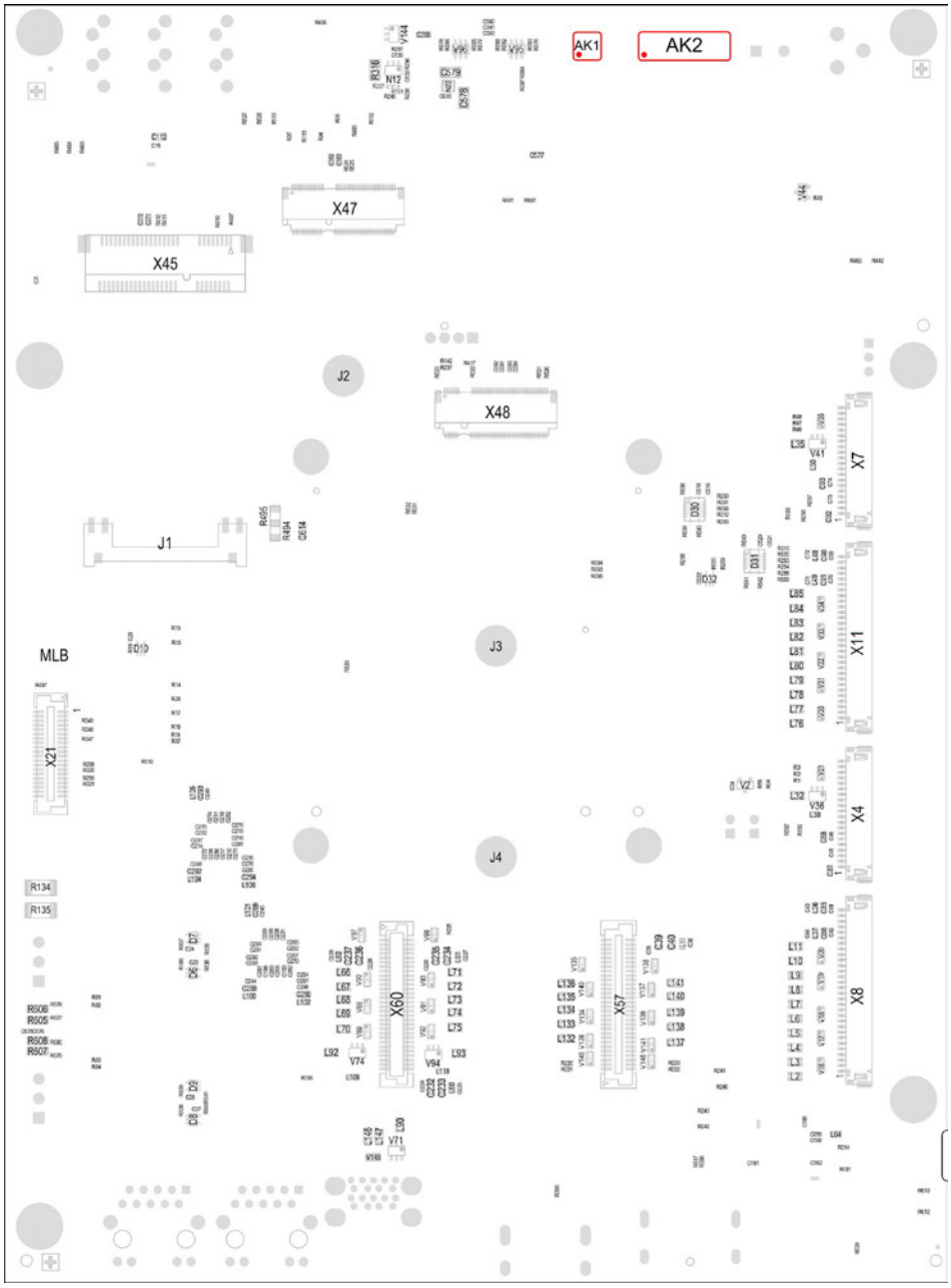

Figure 31: MBa8x, component placement bottom

The labels on the MBa8x revision 02xx show the following information:

Table 31: Labels on MBa8x

Label	Content
AK1	Serial number
AK2	MBa8x version and revision, tests performed

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

As the MBa8x is a development platform, no explicit EMC tests were performed.
During the development of the MBa8x the standard DIN EN 55022:2010 limit class A was taken into account.

6.2 ESD

ESD protection is provided on most interfaces of the MBa8x.
The MBa8x schematics show, which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤48 V DC.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 32: Climatic and operational conditions MBa8x

Parameter	Range	Remark
Ambient temperature	-20 °C to +65 °C	Without TQMa8x module
Ambient temperature	-20 °C to +59 °C	With TQMa8x module (passively cooled)
Storage temperature	–40 °C to +70 °C	With CR2032 battery

Attention: TQMa8x heat dissipation	
	The i.MX 8 CPU belongs to a performance category in which a cooling system could be essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8x must be taken into consideration when connecting the heat sink. The TQMa8x is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8x and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa8x. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa8x.
The MBa8x is designed to be insensitive to vibration and impact.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa8x is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa8x was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP) directive, is applicable to products for the end user with an annual quantity >200,000. The MBa8x must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa8x enable compliance with EuP requirements for the MBa8x.

8.5 Packaging

The MBa8x is delivered in reusable packaging.

8.6 Batteries

8.7 General notes

For technical reasons a battery is necessary for the MBa8x. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets, except technical requirements such as vibration resistance require direct soldering.

8.8 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.9 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa8x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa8x is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 33: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures
NAND	Not-And (flash memory)
NC	Not Connected
NOR	Not-Or
NP	Not Placed

9.1 Acronyms and definitions (continued)

Table 26: Acronyms (continued)

Acronym	Meaning
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (Interface)
PU	Pull-Up
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 34: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8DualX Industrial Applications Processors - Data Sheet	15 May 2020	NXP
(2)	i.MX 8QuadXPlus and 8DualXPlus Applications Processors - Data Sheet	15 May 2020	NXP
(3)	i.MX 8DualXPlus/8QuadXPlus Applications Processor Reference Manual	14 May 2020	NXP
(4)	Mask Set Errata i.MX 8	01 May 2020	NXP
(5)	i.MX8 MEK Platform MCIMX8QM-CPU (EVK), SPF-29420_C2.pdf	Rev. C / 17.09.2018	NXP
(6)	i.MX8 QM/i.MX8 QXP Hardware Developers Guide, IMX8HWDG_Rev2.5p.pdf	Rev. 2.5p / 26 Jan 2022	NXP
(7)	i.MX 8QuadMax Applications Processor Reference Manual, IMX8QMRM_Rev0.pdf	Rev. 0 / 09/2021	NXP
(8)	TQMa8x User's Manual	– current –	TQ-Systems
(9)	TQMa8x Support Wiki	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

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