MBa8Xx
User's Manual

MBa8Xx UM 0102
14.03.2024

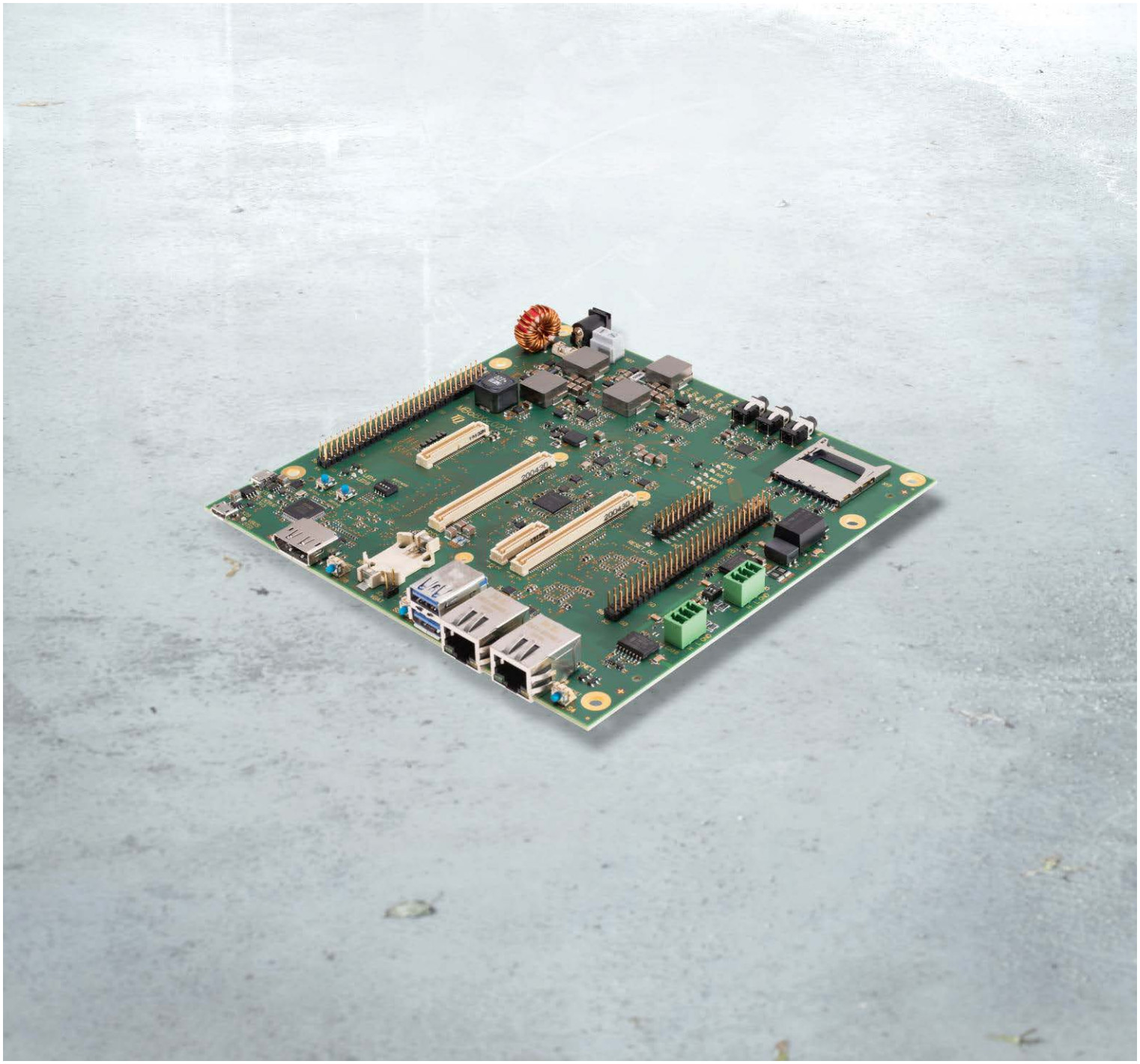

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	21.12.2020	Petz		First edition
0101	31.01.2022	Petz Kreuzer	All Table 8, Table 43 Footnote 2, Table 44 3.8.3 Figure 26, Figure 27 Figure 28 Figure 29 Figure 11 3.8.10 3.8.12	Non-functional changes, phrases, expressions Signal names TAMPER_IN3 / TAMPER_IN4 swapped Typo corrected (i.MX 8 ⇨ i.MX 8X) Information about available SCU-UARTs removed, Note added Updated Renamed “Component placement bottom” removed SCU_UART / UART1 swapped Chapter renamed and rewriten Signal name SD1_WP corrected
0102	14.03.2024	Kreuzer	Figure 1	UART1 note added

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa8Xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8Xx schematics
- TQMa8Xx User's Manual
- i.MX 8X Data Sheet
- i.MX 8X Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8Xx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa8Xx as of revision 02xx. The MBa8Xx is designed as a carrier board for the TQ-Minimodules TQMa8Xx and TQMa8Xx4. If not described differently, all descriptions apply to both TQMa8Xx and TQMa8Xx4.

For better readability, the TQMa8Xx is therefore named for both, the TQMa8Xx and the TQMa8Xx4.

Core of the MBa8Xx is the TQMa8Xx with an NXP i.MX 8X CPU.

The TQMa8Xx connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, etc., all other available signals of the TQMa8Xx are routed on 100 mil standard pin headers on the MBa8Xx.

CPU features and interfaces can be evaluated, software development for a TQMa8Xx based project can start immediately.

Currently three i.MX 8X derivatives are supported:

1. i.MX 8DualX (Dual Cortex®-A35)
2. i.MX 8DualXPlus (Dual Cortex®-A35)
3. i.MX 8QuadXPlus (Quad Cortex®-A35)

Note: i.MX 8DualX, reduced functionality	
	The information in this document primarily refers to the i.MX 8DualXPlus and i.MX 8QuadXPlus. The i.MX 8DualX is not considered in this document because some interfaces are not available or have limitations. Details can be found in the TQMa8Xx User's Manual.

2.1 MBa8Xx block diagram

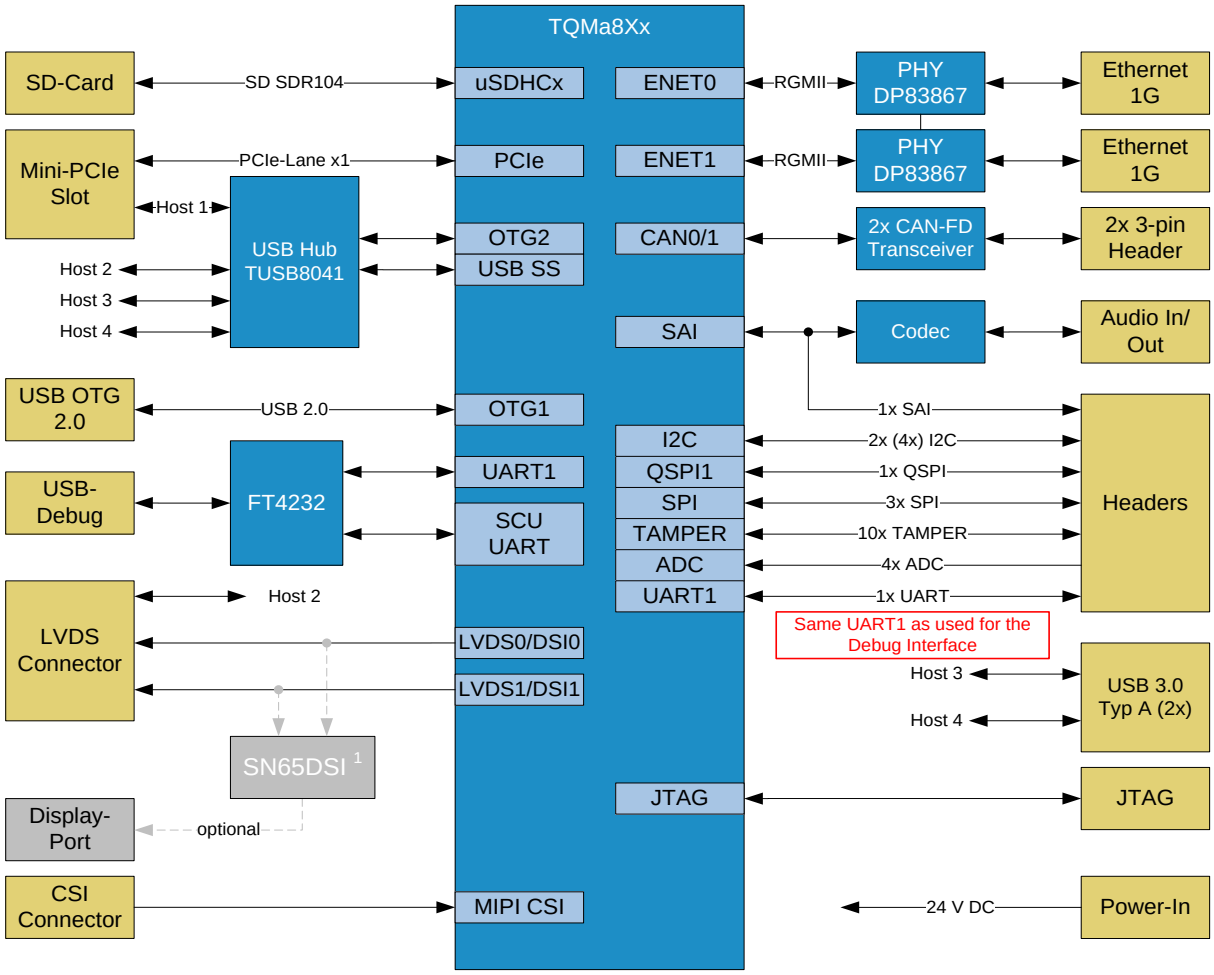


Figure 1: Block diagram MBa8Xx

[1]: This circuit part is no longer present on the MBa8Xx as of revision 0203.

2.2 MBa8Xx data interfaces

The following interfaces/functions and user interfaces are available on the MBa8Xx:

Table 2: Data interfaces

Interface	Connector	Type
Audio	X8 X9 X10	3.5 mm jack • MIC • Line-in • Line-out
CAN-FD	X11, X12	3-pin Phoenix
Coin cell	X6	CR2032 holder
eDP / DisplayPort [1]	X23	20-pin, 90°
Ethernet, 1000 Base-T	X18, X19	RJ-45, integrated magnetics
Headers	X4, X5	100 mil header, 2 × 60-pin
LVDS (Dual)	X14	30-pin, DF19G
LVDS CMD	X22	20-pin, DF19G
MIPI CSI	X28	60-pin, Board-to-Board
Mini PCIe	X24	Mini PCIe socket
	X25	SIM card holder
Power In	X26	DC jack (2.5 mm / 5.5 mm)
	X27	2-pin screw terminal block
SD card, UHS-I	X17	Push-Pull
USB 2.0 Hi-Speed Host	X22, X24	20-pin, DF19G, Mini PCIe socket
USB 2.0 Hi-Speed OTG	X29	USB, Micro AB
USB 3.0 SS Host	X20	USB, stacked Type A
USB debug	X13	USB, Micro AB

The MBa8Xx provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	9 × Green LED	Power LEDs
	4 × Green LED	3 × USB Host, 1 × USB OTG
	1 × Green LED	Debug LED for USB debug interface
	2 × Green LED	GP LEDs at port expander
	3 × Green LED	Mini PCIe: WWAN, WLAN, WPAN
	1 × Red LED	Reset LED
	2 × Green / Yellow LED	Ethernet LEDs (Activity / Speed)
Temperature sensor	1 × SE97BTP	Digital I²C temperature sensor
Power / Reset button	3 × Push button	RESET-IN, PMIC_PWRON, IMX_ONOFF
General Purpose button	2 × Push button	GP push button at port expander
Boot Mode configuration	1 × 4-fold DIP switch	Boot Mode configuration
CAN termination	2 × 2-fold DIP switch	–
JTAG	1 × 20-pin, 100 mil header	–

[1]: This circuit part is no longer present on the MBa8Xx as of revision 0203.

3. ELECTRONICS

The following chapters describe the interfaces of the MBa8Xx as of revision 02xx in connection with a TQMa8Xx or TQMa8Xx4 with maximum configuration. If not described differently, all descriptions apply to both TQMa8Xx and TQMa8Xx4.

For better readability, the TQMa8Xx is therefore named for both, the TQMa8Xx and the TQMa8Xx4.

In any case the TQMa8Xx User's Manual must be complied with.

3.1 TQMa8Xx

The TQMa8Xx is the central system on the MBa8Xx. It provides DDR3L SDRAM (TQMa8Xx), or LPDDR4 SDRAM (TQMa8Xx4), eMMC, NOR flash, RTC, an EEPROM, power supply and power management functionality.

All TQMa8Xx internal voltages are derived from the 3.3 V supply voltage. All functionally relevant pins of the CPU are routed to the TQMa8Xx connectors. This enables the user to use the TQMa8Xx with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa8Xx User's Manual.

On the MBa8Xx the standard interfaces like USB, Ethernet, etc., provided by the TQMa8Xx are routed to industry standard connectors. All other signals and buses provided by the TQMa8Xx are routed to 100 mil headers.

The boot behaviour of the TQMa8Xx can be configured.

The Boot Mode configuration is set by a DIP switch on the MBa8Xx, see chapter 3.2.

Furthermore the MBa8Xx provides all power supplies and configurations required for the operation of the TQMa8Xx.

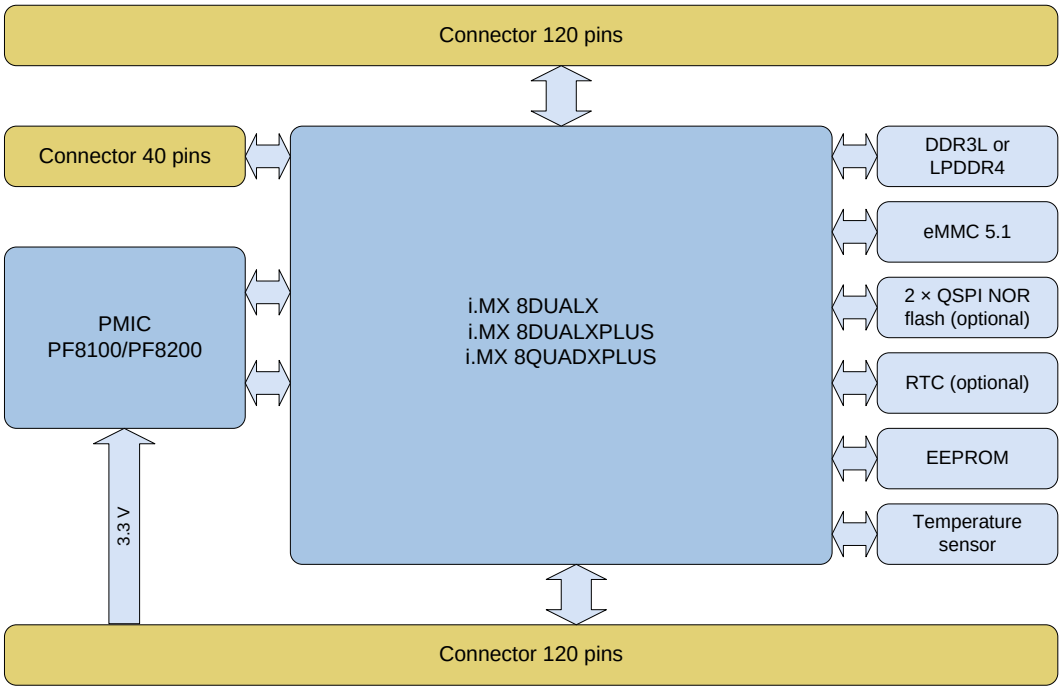


Figure 2: Block diagram TQMa8Xx

3.1.1 TQMa8Xx connectors on MBa8Xx

The TQMa8Xx is connected to the MBa8Xx with 280 pins on three connectors.
The following table shows details of the connectors assembled on the MBa8Xx:

Table 4: Connectors assembled on MBa8Xx

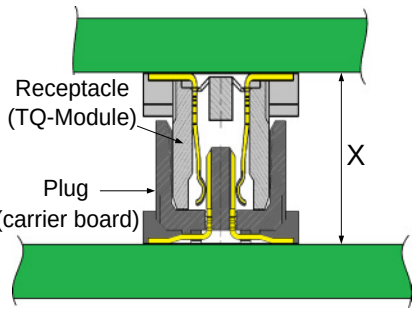
Manufacturer	Pin count / part number	Qty.	Remark
TE connectivity	120-pin / 5177986-5	2	0.2 µm gold plating
	40-pin / 5177986-1	1	0.2 µm gold plating

The TQMa8Xx is held in the mating connectors on the MBa8Xx by 280 pins with a retention force of approximately 28 N.
To avoid damaging the connectors of the MBa8Xx or the TQMa8Xx while removing the TQMa8Xx, the use of the extraction tool MOZI8XX is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa8Xx for the extraction tool MOZI8XX.

The following table shows some suitable mating connectors for the carrier board:

Table 5: Carrier board mating connectors

Manufacturer	Pin count part number	Remark	Stack height (X)	
TE connectivity	120-pin: 5177986-5 40-pin: 5177986-1	On MBa8Xx	5 mm	
	120-pin: 1-5177986-5 40-pin: 1-5177986-1	–	6 mm	
	120-pin: 2-5177986-5 40-pin: 2-5177986-1	–	7 mm	
	120-pin: 3-5177986-5 40-pin: 3-5177986-1	–	8 mm	

The pins assignment listed in Table 6 to Table 8 refer to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in Table 6 to Table 8 refer to the i.MX 8X documentation, see Table 57.

3.1.2 TQMa8Xx pinout

All available TQMa8Xx signals are available at three connectors on the MBa8Xx.
The direction of the signals in Table 6 to Table 8 is shown from the perspective of the TQMa8Xx.
Further information like pull-ups or pull-downs on the TQMa8Xx can be taken from the TQMa8Xx User's Manual (7).

Note: Available interfaces	
	Depending on the TQMa8Xx derivative not all interfaces are available. More information about available interfaces can be found in the TQMa8Xx User's Manual.

3.1.2 TQMa8Xx pinout (continued)

Table 6: Pinout TQMa8Xx connector X1

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
–	0 V	Ground	GND	1	2	GND	Ground	0 V	–
O	1.8 V (1)	ENET	ENET1_REFCLK_OUT (2)	3	4	TEMP_EVENT#	CONFIG	–	O
–	0 V	Ground	GND	5	6	GND	Ground	0 V	–
I	1.8 V (1)	ENET	ENET1_RXC (2)	7	8	ENET1_TXC (2)	ENET	1.8 V (1)	O
–	0 V	Ground	GND	9	10	GND	Ground	0 V	–
I	1.8 V (1)	ENET	ENET1_RX_CTL (2)	11	12	ENET1_TX_CTL (2)	ENET	1.8 V (1)	O
I	1.8 V (1)	ENET	ENET1_RXD0 (2)	13	14	ENET1_TXD0 (2)	ENET	1.8 V (1)	O
I	1.8 V (1)	ENET	ENET1_RXD1 (2)	15	16	ENET1_TXD1 (2)	ENET	1.8 V (1)	O
I	1.8 V (1)	ENET	ENET1_RXD2 (2)	17	18	ENET1_TXD2 (2)	ENET	1.8 V (1)	O
I	1.8 V (1)	ENET	ENET1_RXD3 (2)	19	20	ENET1_TXD3 (2)	ENET	1.8 V (1)	O
–	0 V	Ground	GND	21	22	GND	Ground	0 V	–
I/O	1.8 V (3)	M4 GPIO	M4_GPIO0_IO02	23	24	V_1V5_MPCIE_EN	PCIe	1.8 V (3)	O
I/O	1.8 V (3)	M4 GPIO	M4_GPIO0_IO03	25	26	V_3V3_MPCIE_EN	PCIe	1.8 V (3)	O
I/O	1.8 V (3)	M4 I2C	M4_I2C_SDA	27	28	LCD_CONTRAST	DSI / LVDS	1.8 V (3)	O
I/O	1.8 V (3)	M4 I2C	M4_I2C_SCL	29	30	PMIC_PGOOD	CONFIG	1.8 V	O
I	1.8 V	CONFIG	PMIC_WDI	31	32	GND	Ground	0 V	–
O	1.8 V (3)	UART	UART1_TX	33	34	SPI2_SCK	SPI	1.8 V (3)	O
I	1.8 V (3)	UART	UART1_RX	35	36	SPI2_SDO	SPI	1.8 V (3)	O
O	1.8 V (3)	UART	UART1_RTS#	37	38	SPI2_SDI	SPI	1.8 V (3)	I
I	1.8 V (3)	UART	UART1_CTS#	39	40	SPI2_CS0	SPI	1.8 V (3)	O
–	0 V	Ground	GND	41	42	SPI1_CS0	SPI	1.8 V (3)	O
O	1.8 V (1)	ENET	ENET0_MDC (2)	43	44	SPI1_CS1	SPI	1.8 V (3)	O
I/O	1.8 V (1)	ENET	ENET0_MDIO (2)	45	46	SPI1_SDO	SPI	1.8 V (3)	O
–	0 V	Ground	GND	47	48	SPI1_SDI	SPI	1.8 V (3)	I
O	1.8 V (1)	ENET	ENET0_REFCLK_OUT (2)	49	50	SPI1_SCK	SPI	1.8 V (3)	O
–	0 V	Ground	GND	51	52	GND	Ground	0 V	–
I	1.8 V (1)	ENET	ENET0_RXC (2)	53	54	ENET0_TXC (2)	ENET	1.8 V (1)	O
–	0 V	Ground	GND	55	56	GND	Ground	0 V	–
I	1.8 V (1)	ENET	ENET0_RX_CTL (2)	57	58	ENET0_TX_CTL (2)	ENET	1.8 V (1)	O
–	0 V	Ground	GND	59	60	GND	Ground	0 V	–
I	1.8 V (1)	ENET	ENET0_RXD0 (2)	61	62	ENET0_TXD0 (2)	ENET	1.8 V (1)	O
I	1.8 V (1)	ENET	ENET0_RXD1 (2)	63	64	ENET0_TXD1 (2)	ENET	1.8 V (1)	O
I	1.8 V (1)	ENET	ENET0_RXD2 (2)	65	66	ENET0_TXD2 (2)	ENET	1.8 V (1)	O
I	1.8 V (1)	ENET	ENET0_RXD3 (2)	67	68	ENET0_TXD3 (2)	ENET	1.8 V (1)	O
–	0 V	Ground	GND	69	70	GND	Ground	0 V	–
I	3.3 V	USB	USB_OTG1_ID	71	72	USB_OTG2_ID	USB	3.3 V	I
P	5 V	USB	USB_OTG1_VBUS	73	74	USB_OTG2_VBUS	USB	3.3 V	P
O	3.3 V	USB	USB_OTG1_PWR	75	76	USB_OTG2_PWR	USB	3.3 V	O
I	3.3 V	USB	USB_OTG1_OC#	77	78	USB_OTG2_OC#	USB	3.3 V	I
–	0 V	Ground	GND	79	80	GND	Ground	0 V	–
I/O	3.3 V	USB	USB_OTG1_D–	81	82	USB_OTG2_D–	USB	3.3 V	I/O
I/O	3.3 V	USB	USB_OTG1_D+	83	84	USB_OTG2_D+	USB	3.3 V	I/O
–	0 V	Ground	GND	85	86	GND	Ground	0 V	–
I/O	1.8 / 3.3 V	SD	SD1_CMD	87	88	USB_SS_TX+	USB	1.0 V	O
–	0 V	Ground	GND	89	90	USB_SS_TX–	USB	1.0 V	O
O	1.8 / 3.3 V	SD	SD1_CLK	91	92	GND	Ground	0 V	–
–	0 V	Ground	GND	93	94	USB_SS_RX+	USB	1.0 V	I
I/O	1.8 / 3.3 V	SD	SD1_DATA0	95	96	USB_SS_RX–	USB	1.0 V	I
I/O	1.8 / 3.3 V	SD	SD1_DATA1	97	98	GND	Ground	0 V	–
I/O	1.8 / 3.3 V	SD	SD1_DATA2	99	100	PCIE_TX–	PCIe	0.7 V	O
I/O	1.8 / 3.3 V	SD	SD1_DATA3	101	102	PCIE_TX+	PCIe	0.7 V	O
–	0 V	Ground	GND	103	104	GND	Ground	0 V	–
I	1.8 V	SD	SD1_WP	105	106	PCIE_RX–	PCIe	0.7 V	I
P	1.8 V	Power	V_1V8 (4)	107	108	PCIE_RX+	PCIe	0.7 V	I
I	1.8 V	SD	SD1_CD#	109	110	GND	Ground	0 V	–
I	1.8 V	CONFIG	PE1_INT#	111	112	PCIE_REFCLK–	PCIe	0.7 V	I
–	0 V	Ground	GND	113	114	PCIE_REFCLK+	PCIe	0.7 V	I
I	3.3 V	PCIe	PCIE_CLKREQ#	115	116	GND	Ground	0 V	–
O	3.3 V	PCIe	PCIE_PERST#	117	118	IMX_ONOFF	CONFIG	1.8 V	I
I	3.3 V	PCIe	PCIE_WAKE#	119	120	GND	Ground	0 V	–

1: Depends on X1-107 (V_ENET_IN on TQMa8Xx). V_ENET_IN is hard-wired to 1.8 V on the MBa8Xx, see also chapter 3.10.
2: RGMII is not available with the i.MX 8DualX. RMII or an alternate multiplexing function can be used.
3: Depends on X2-11 (V_IO_IN on TQMa8Xx). V_IO_IN is hard-wired to 1.8 V on the MBa8Xx, see also chapter 3.10.
4: Signal V_ENET_IN on TQMa8Xx. V_ENET_IN is hard-wired to 1.8 V on the MBa8Xx, see also chapter 3.10.

3.1.2 TQMa8Xx pinout (continued)

Table 7: Pinout TQMa8Xx connector X2

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
P	3.3 V	Power	V_3V3_TQM	1	2	V_3V3_TQM	Power	3.3 V	P
P	3.3 V	Power	V_3V3_TQM	3	4	V_3V3_TQM	Power	3.3 V	P
P	3.3 V	Power	V_3V3_TQM	5	6	V_3V3_TQM	Power	3.3 V	P
–	0 V	Ground	GND	7	8	GND	Ground	0 V	–
–	0 V	Ground	GND	9	10	GND	Ground	0 V	–
P	1.8 V	Power	V_1V8_OUT (1)	11	12	V_1V8_OUT (1)	Power	1.8 V	P
I	1.8 V	CONFIG	BOOT_MODE0	13	14	GND	Ground	0 V	–
I	1.8 V	CONFIG	BOOT_MODE1	15	16	MCLK_OUT0	CLK	1.8 V (2)	O
I	1.8 V	CONFIG	BOOT_MODE2	17	18	MCLK_IN1	CLK	1.8 V (2)	I
I	1.8 V	CONFIG	BOOT_MODE3	19	20	MCLK_IN0	CLK	1.8 V (2)	I
P	1.8 V	Power	V_1V8_ANA	21	22	GND	Ground	0 V	–
P	3 V	Power	V_LICELL	23	24	MIPI_CSI_SCL	CSI	1.8 V	O
O	1.8 V	CONFIG	PMIC_FSOB_EWARN	25	26	MIPI_CSI_SDA	CSI	1.8 V	I/O
I	1.8 V	CONFIG	PMIC_PWRON	27	28	SCU_UART_RX	SCU UART	1.8 V	I
–	0 V	Ground	GND	29	30	SCU_UART_TX	SCU UART	1.8 V	O
I	1.8 V	CSI	MIPI_CSI_D0–	31	32	RESET_IN#	CONFIG	3.0 V	I
I	1.8 V	CSI	MIPI_CSI_D0+	33	34	RESET_OUT#	CONFIG	3.0 V	O
–	0 V	Ground	GND	35	36	GND	Ground	0 V	–
I	1.8 V	CSI	MIPI_CSI_D1–	37	38	I2C2_SCL	I2C	1.8 V (2)	I/O
I	1.8 V	CSI	MIPI_CSI_D1+	39	40	I2C2_SDA	I2C	1.8 V (2)	I/O
–	0 V	Ground	GND	41	42	GND	Ground	0 V	–
I	1.8 V	CSI	MIPI_CSI_D2–	43	44	SPI3_SCK	SPI	1.8 V (2)	O
I	1.8 V	CSI	MIPI_CSI_D2+	45	46	SPI3_SDO	SPI	1.8 V (2)	O
–	0 V	Ground	GND	47	48	SPI3_SDI	SPI	1.8 V (2)	I
I	1.8 V	CSI	MIPI_CSI_D3–	49	50	SPI3_CS0	SPI	1.8 V (2)	O
I	1.8 V	CSI	MIPI_CSI_D3+	51	52	SPI3_CS1	SPI	1.8 V (2)	O
–	0 V	Ground	GND	53	54	PMIC_AMUX_VSD	DNC	–	O
I	1.8 V	CSI	MIPI_CSI_CLK–	55	56	GND	Ground	0 V	–
I	1.8 V	CSI	MIPI_CSI_CLK+	57	58	MIPI_CSI_MCLK	CSI	1.8 V	O
–	0 V	Ground	GND	59	60	GND	Ground	0 V	–
O	1.8 V	DSI / LVDS	MIPI_DSI1_D0–	61	62	MIPI_DSI0_D0–	DSI / LVDS	1.8 V	O
O	1.8 V	DSI / LVDS	MIPI_DSI1_D0+	63	64	MIPI_DSI0_D0+	DSI / LVDS	1.8 V	O
–	0 V	Ground	GND	65	66	GND	Ground	0 V	–
O	1.8 V	DSI / LVDS	MIPI_DSI1_D1–	67	68	MIPI_DSI0_D1–	DSI / LVDS	1.8 V	O
O	1.8 V	DSI / LVDS	MIPI_DSI1_D1+	69	70	MIPI_DSI0_D1+	DSI / LVDS	1.8 V	O
–	0 V	Ground	GND	71	72	GND	Ground	0 V	–
O	1.8 V	DSI / LVDS	MIPI_DSI1_D2–	73	74	MIPI_DSI0_D2–	DSI / LVDS	1.8 V	O
O	1.8 V	DSI / LVDS	MIPI_DSI1_D2+	75	76	MIPI_DSI0_D2+	DSI / LVDS	1.8 V	O
–	0 V	Ground	GND	77	78	GND	Ground	0 V	–
O	1.8 V	DSI / LVDS	MIPI_DSI1_D3–	79	80	MIPI_DSI0_D3–	DSI / LVDS	1.8 V	O
O	1.8 V	DSI / LVDS	MIPI_DSI1_D3+	81	82	MIPI_DSI0_D3+	DSI / LVDS	1.8 V	O
–	0 V	Ground	GND	83	84	GND	Ground	0 V	–
O	1.8 V	DSI / LVDS	MIPI_DSI1_CLK–	85	86	MIPI_DSI0_CLK–	DSI / LVDS	1.8 V	O
O	1.8 V	DSI / LVDS	MIPI_DSI1_CLK+	87	88	MIPI_DSI0_CLK+	DSI / LVDS	1.8 V	O
–	0 V	Ground	GND	89	90	GND	Ground	0 V	–
I	1.8 V (2)	ENET	ENET0_INT#	91	92	ENET0_RESET#	ENET	1.8 V (2)	O
I	1.8 V (2)	ENET	ENET1_INT#	93	94	ENET1_RESET#	ENET	1.8 V (2)	O
–	0 V	Ground	GND	95	96	GND	Ground	0 V	–
I	1.8 V	QSPI	QSPIB_DQS	97	98	SAI1_TXC	SAI	1.8 V (2)	O
–	0 V	Ground	GND	99	100	SAI1_TXFS	SAI	1.8 V (2)	O
O	1.8 V	QSPI	QSPIB_SCLK	101	102	SAI1_TXD	SAI	1.8 V (2)	O
–	0 V	Ground	GND	103	104	GND	Ground	0 V	–
I/O	1.8 V	QSPI	QSPIB_DATA0	105	106	SAI1_RXC	SAI	1.8 V (2)	I
I/O	1.8 V	QSPI	QSPIB_DATA1	107	108	SAI1_RXFS	SAI	1.8 V (2)	I
I/O	1.8 V	QSPI	QSPIB_DATA2	109	110	SAI1_RXD	SAI	1.8 V (2)	I
I/O	1.8 V	QSPI	QSPIB_DATA3	111	112	MIPI_CSI_EN	CSI	1.8 V	O
O	1.8 V	QSPI	QSPIB_SS0#	113	114	MIPI_CSI_RST#	CSI	1.8 V	O
O	1.8 V	QSPI	QSPIB_SS1#	115	116	I2C1_SDA	I2C	1.8 V (2)	I/O
I/O	1.8 V	GPIO	GPIO3_IO15	117	118	I2C1_SCL	I2C	1.8 V (2)	I/O
–	0 V	Ground	GND	119	120	GND	Ground	0 V	–

1: Signal V_IO_IN on TQMa8Xx. V_IO_IN is hard-wired to 1.8 V on the MBa8Xx, see also chapter 3.10. Maximum load on pins 11 and 12 is 0.5 A each.
2: Depends on X2-11 (V_IO_IN on TQMa8Xx). V_IO_IN is hard-wired to 1.8 V on the MBa8Xx, see also chapter 3.10.

3.1.2 TQMa8Xx pinout (continued)

Table 8: Pinout TQMa8Xx connector X3

Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.
–	0 V	Ground	GND	1	2	GND	Ground	0 V	–
I	1.8 V	GPIO	SWITCH_B#	3	4	JTAG_TCK	JTAG	1.8 V	I
I	1.8 V	GPIO	SWITCH_A#	5	6	JTAG_TDI	JTAG	1.8 V	I
–	0 V	Ground	GND	7	8	JTAG_TDO	JTAG	1.8 V	O
O	1.8 V (1)	DSI / LVDS	LCD_RESET#	9	10	JTAG_TMS	JTAG	1.8 V	I
O	1.8 V (1)	DSI / LVDS	LCD_BLT_EN	11	12	SCU_WDOG_OUT (2)	CONFIG	1.8 V	O_{PU}
O	1.8 V (1)	DSI / LVDS	LCD_PWR_EN	13	14	GND	Ground	0 V	–
I/O	1.8 V (1)	DSI / LVDS	GPIO1_IO26	15	16	CAN0_RX	CAN	1.8 V (1)	I
–	0 V	Ground	GND	17	18	CAN0_TX	CAN	1.8 V (1)	O
O	1.8 V (1)	TAMPER	TAMPER_OUT0	19	20	CAN1_RX	CAN	1.8 V (1)	I
O	1.8 V (1)	TAMPER	TAMPER_OUT1	21	22	CAN1_TX	CAN	1.8 V (1)	O
O	1.8 V (1)	TAMPER	TAMPER_OUT2	23	24	GND	Ground	0 V	–
O	1.8 V (1)	TAMPER	TAMPER_OUT3	25	26	ADC_IN0	ADC	1.8 V	I
O	1.8 V (1)	TAMPER	TAMPER_OUT4	27	28	ADC_IN1	ADC	1.8 V	I
I	1.8 V (1)	TAMPER	TAMPER_IN0	29	30	ADC_IN2	ADC	1.8 V	I
I	1.8 V (1)	TAMPER	TAMPER_IN1	31	32	ADC_IN3	ADC	1.8 V	I
I	1.8 V (1)	TAMPER	TAMPER_IN2	33	34	V_ADC_IN (3)	ADC	1.8 V	I
I	1.8 V (1)	TAMPER	TAMPER_IN4	35	36	PMIC_I2C_SDA	DNC	1.8 V	I/O
I	1.8 V (1)	TAMPER	TAMPER_IN3	37	38	PMIC_I2C_SCL	DNC	1.8 V	I/O
–	0 V	Ground	GND	39	40	GND	Ground	0 V	–

1: Depends on X2-11 (V_IO_IN on TQMa8Xx). V_IO_IN is hard-wired to 1.8 V on the MBa8Xx, see also chapter 3.10.
2: Changed from JTAG_TRST# to SCU_WDOG_OUT. Signal JTAG_TRST# is not supported anymore by the i.MX 8X.
3: ADC reference voltage of the TQMa8Xx is hard-wired to 1.8 V on the MBa8Xx via V_1V8_OUT.

3.2 Boot Mode configuration

The MBa8Xx supports the following TQMa8Xx boot sources:

- eMMC (on TQMa8Xx)
- QSPI NOR flash (on TQMa8Xx)
- SD card (X17 on MBa8Xx)
- Serial downloader via USB OTG (X29)

The Boot Mode of the i.MX 8X is set with signals BOOT_MODE[3:0], which can be set with the 4-fold DIP switch S1.
The following table shows the possible settings of the boot configurations:

Table 9: Boot Mode configuration

Boot-Mode	S1-1 (BM3)		S1-2 (BM2)		S1-3 (BM1)		S1-4 (BM0)		Remark
	Pos.	Level	Pos.	Level	Pos.	Level	Pos.	Level	
Boot from eFuses	OFF	0	OFF	0	OFF	0	OFF	0	–
Serial Downloader (USB OTG1)	OFF	0	OFF	0	OFF	0	ON	1	As of i.MX 8X stepping B0
eMMC (USDCH0)	OFF	0	OFF	0	ON	1	OFF	0	–
SD card (USDHC1)	OFF	0	OFF	0	ON	1	ON	1	–
Reserved	OFF	0	ON	1	OFF	0	OFF	0	–
Reserved	OFF	0	ON	1	OFF	0	ON	1	–
QSPI (QSPI0A/B)	OFF	0	ON	1	ON	1	OFF	0	3-byte read
QSPI (QSPI0A/B)	OFF	0	ON	1	ON	1	ON	1	Only for Hyperflash
Reserved	ON	1	X	X	X	X	X	X	–

Note: Boot from NAND	
	Booting from NAND is not supported on the MBa8Xx.

3.3 I²C devices

3.3.1 Default I²C interface

The TQMa8Xx provides several I²C buses, of which only I2C1 is used on the MBa8Xx.

Due to the multiple I2C devices on the TQMa8Xx, the already used I2C addresses have to be taken into account. Depending on the application and software load, the number of I²C devices used can limit the data throughput or block the bus. For this reason, the devices used on the MBa8Xx can be optionally connected to the I2C2. This assembly option is described in the MBa8Xx schematics.

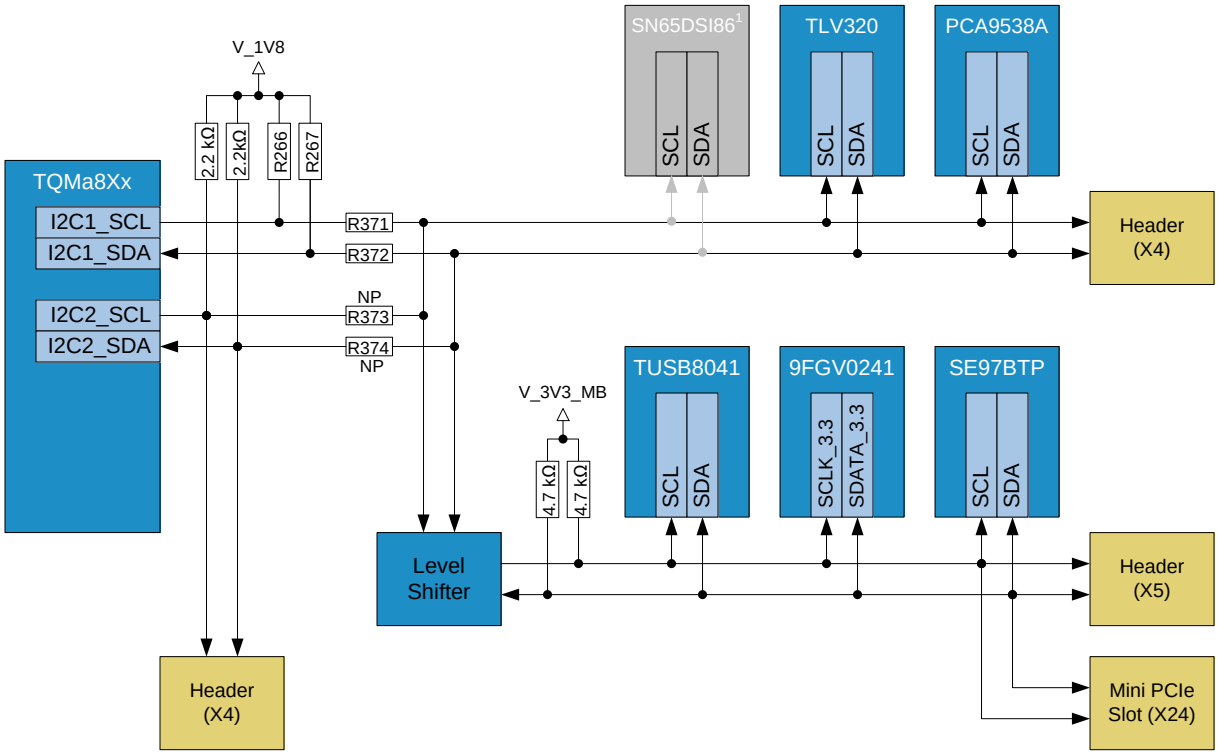


Figure 3: Block diagram I²C bus

Note: I²C address conflicts	
	When changing the address due to assembly options or when connecting further I²C components, it must be ensured that no address conflicts occur. Otherwise malfunctions may occur. The addresses preassigned by the TQMa8Xx must also be observed (depending on the TQMa8Xx variant used).

[1]: This circuit part is no longer present on the MBa8Xx as of revision 0203.

3.3.1 Default I2C interface (continued)

The following table shows the default I²C device addresses on the MBa8Xx and the TQMa8Xx.
For some devices the address can be changed by assembly options. The options are described in detail in the given chapter.

Table 10: I²C devices, address mapping on TQMa8Xx and MBa8Xx

Location	Device	Function	7-bit address	Remark
TQMa8Xx	SE050	Trusted Secure Element	0x48 / 100 1000b	
	24LC64	EEPROM	0x57 / 101 0111b	
	SE97BTP	Temperature sensor	0x1B / 001 1011b	
		EEPROM	0x53 / 101 0011b	R/W access in Normal Mode
		EEPROM	0x33 / 011 0011b	R/W access in Protected Mode
	PCF85063	RTC	0x51 / 101 0001b	
MBa8Xx	TUSB8041	USB hub (optional)	0x44 / 100 0100b	Optional
	TLV320	Audio Codec	0x18 / 001 1000b	
	SN65DSI86	DisplayPort Bridge	0x2C / 010 1100b	Optional [1]
	9FGV0241	PCIE clock generator	0x6A / 110 1010b	Optional [2]
	PCA9306DQE	Temperature sensor	0x1C / 001 1100b	Discrete
	SE97BTP	EEPROM	0x54 / 101 0100b	R/W access in Normal Mode
		EEPROM	0x34 / 011 0100b	R/W access in Protected Mode
	PCA9538A	Port expander	0x70 / 111 0000b	

Note: I²C address conflicts

When changing the address due to assembly options or when connecting further I²C components, it must be ensured that no address conflicts occur. Otherwise malfunctions may occur. The addresses preassigned by the TQMa8Xx must also be observed (depending on the TQMa8Xx variant used).

1: This circuit part is no longer present on the MBa8Xx as of revision 0203.
2: Only when using certain variants of the TQMa8Xx4.

3.3.2 M4 I²C interface

In addition to the I²C interfaces I2C1 and I2C2, the interface of the i.MX 8X system controller is also available on the MBa8Xx.
The M4_I2C bus is connected to header X5. There are no other devices on this bus on the MBa8Xx.
Both I²C lines M4_I2C_SCL and M4_I2C_SDA are provided with 2.2-kΩ pull-up resistors to 1.8 V on the MBa8Xx.
To reduce the bus load on I2C1, the I²C devices on the MBa8Xx can be connected to the I2C2 bus. As shown in the following table, the configuration of the used I²C bus is determined by the resistors R371 to R374.

Table 11: Assembly option I2C1 / I2C2 bus for I²C devices on MBa8Xx

I²C bus	R371	R372	R373	R374	Remark
I2C1	0 Ω	0 Ω	NP	NP	Default
I2C2	NP	NP	0 Ω	0 Ω	–

In addition to the pull-up resistors on the I2C1 bus on the TQMa8Xx, the bus load can be adapted on the MBa8Xx by assembling further pull-up resistors (R266 on SCL, R267 on SDA).

3.3.3 Further I²C devices

In addition to the port expander and the temperature sensor, more I²C devices are connected to the I2C1, see Table 10.
These devices are described in the respective chapter for the corresponding interface.

3.4 GPIO port expander

An 8-fold port expander PCA9538A is used to control various components on the MBa8Xx, see Table 12.
The port expander is controlled via I2C1. The address of the port expander can be altered by reassembling resistors.
When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 10.
The assembly options are documented in the schematic of the MBa8Xx.
In the initial state after switching on, all ports are set as input and the respective connected component is thus deactivated.
The I/O level of the signals is 1.8 V.

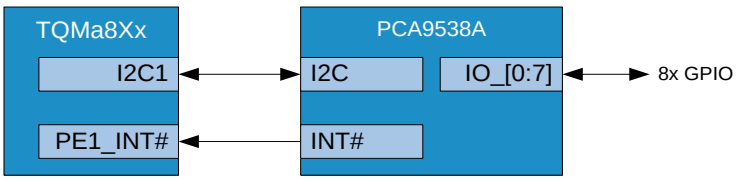


Figure 4: Block diagram GPIO expander

Table 12: Port expander functions

Port	Signal	Dir.	Remark
IO_0	(NC)	I	Not connected / reserved
IO_1	LED_A	O_{PD}	User-LED (see chapter 3.9.5, Status LEDs)
IO_2	LED_B	O_{PD}	User-LED (see chapter 3.9.5, Status LEDs)
IO_3	(NC)	I	Not connected / reserved
IO_4	DSI_EN	O	Enable signal eDP bridge[1], high-active
IO_5	USB_RESET#	O	Not used. Optional as Reset for the USB hub (see Table 18), low-active
IO_6	V_12V_EN	O	Enable signal for 12 V supply (V_12V), high-active

[1]: This circuit part is no longer present on the MBa8Xx as of revision 0203.

Port	Signal	Dir.	Remark
IO_7	PCIE_DIS#	O	Disable signal for Mini PCIe, low-active

The I²C address of the GPIO port expander is determined, among other things, by the input level of pins A0 and A1.
By changing the resistor, the I²C address can be changed according to the following table.
Details can be taken from the MBa8Xx schematics.

Table 13: Assembly option I²C address GPIO port expander

7-bit-address	R22	R146	R23	R147	Remark
0x70	NP	0 Ω	NP	0 Ω	Default
0x71	0 Ω	NP	NP	0 Ω	–
0x72	NP	0 Ω	0 Ω	NP	–
0x73	0 Ω	NP	0 Ω	NP	–

3.5 Temperature sensor and EEPROM

A temperature sensor SE97BTP is populated on the MBa8Xx to monitor the temperature. The same type of sensor is also used on the TQMa8Xx. Both sensors are read out via I2C1, see Table 10.
The sensor address on the MBa8Xx can be changed by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 10. The assembly options are documented in the MBa8Xx schematics.
The SE97BTP has an additional EEPROM. Further specifications of the SE97BTP can be found in the data sheet.

The alarm output EVENT# of the SE97BTP is not connected and is not available on the MBa8Xx.

Figure 5: Block diagram temperature sensor

The I²C addresses of the temperature sensor and the EEPROM are determined by the input level of pins A0, A1 and A2, among other things. The I²C addresses can be changed according to the following table by a resistor reassembly.
Details can be taken from the MBa8Xx schematics.

Table 14: Assembly option I²C address temperature sensor / EEPROM

7-bit address			R43	R42	R44	R45	R46	R47	Remark
Temperature sensor	EEPROM (read/write)	EEPROM (Software protection)							
0x18	0x50	0x30	NP	10 kΩ	NP	10 kΩ	NP	10 kΩ	–
0x19	0x51	0x31	10 kΩ	NP	NP	10 kΩ	NP	10 kΩ	–
0x1A	0x52	0x32	NP	10 kΩ	10 kΩ	NP	NP	10 kΩ	–
0x1B	0x53	0x33	10 kΩ	NP	10 kΩ	NP	NP	10 kΩ	–
0x1C	0x54	0x34	NP	10 kΩ	NP	10 kΩ	10 kΩ	NP	Default
0x1D	0x55	0x35	10 kΩ	NP	NP	10 kΩ	10 kΩ	NP	–
0x1E	0x56	0x36	NP	10 kΩ	10 kΩ	NP	10 kΩ	NP	–
0x1F	0x57	0x37	10 kΩ	NP	10 kΩ	NP	10 kΩ	NP	–

3.6 RTC backup

The TQMa8Xx has an optional RTC and a voltage rail for standby functions. This is supplied via pin LICELL.
On the MBa8Xx there are two possibilities to supply the LICELL input [1]:

- CR2032-Battery holder
- 2-pin header for alternative connection of an external voltage or batteries

The maximum input voltage at X7 is described in the TQMa8Xx User's Manual.

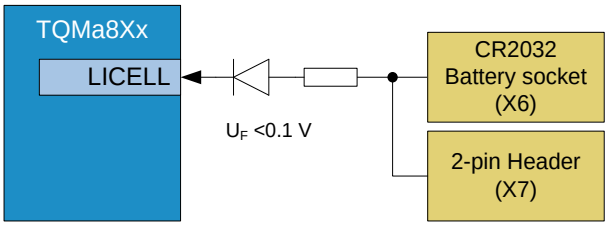


Figure 6: Block diagram RTC backup

Table 15: Pinout RTC backup (X7)

Pin	Signal	Level	Remark
1	V_LICELL	3 V	Supply voltage for RTC on TQMa8Xx
2	GND	0 V	Ground

To meet regulatory requirements for protection against accidental battery charging, a 1 kΩ resistor and diode is connected in series between X6/X7 and the LICELL input of the TQMa8Xx.
The diode has a very low forward voltage (<0.1 V) in order not to unnecessarily reduce the battery runtime.
If it is necessary to reduce the forward voltage to 0 V for test purposes, the protective diode can be removed according to Table 16 and a corresponding resistor can be fitted.

Table 16: Assembly option RTC-Backup

Reverse current protection	V2106	R2110	Remark
Active	BAT54	NP	Default
Not active	NP	0 Ω	Note: 1 kΩ in series is still present in this case

Attention: Loss of reverse current protection	
	The reverse current protection is lost when the protective diode is replaced with a resistor! This is especially critical for TQMa8Xx with external RTC, since here the 3.3 V supply of the TQMa8Xx in ON mode [2] drives directly into the RTC backup battery!

1: Only one of the two options may be used at a time!
2: TQMa8Xx is supplied at V_3V3_IN.

3.7 USB hub

Four USB host interfaces are provided via the TUSB8041 USB hub. The hub has one upstream port and four downstream ports. The upstream port is the USB 3.0 OTG port, consisting of the OTG2 signals as well as the SuperSpeed signals.

USB host 1 and 2 of the hub are used internally for the Mini PCIe (see also chapter 3.8.8) or LVDS / MIPI DSI (see also chapter 3.8.6.2) interfaces. The other two USB hosts 3 and 4 are externally accessible as USB 3.0 hosts, see also chapter 3.8.10.

Table 17 shows the power management configured on the MBa8Xx with pull-up or pull-down resistors.
Alternatively, all settings can be changed by assembly options.

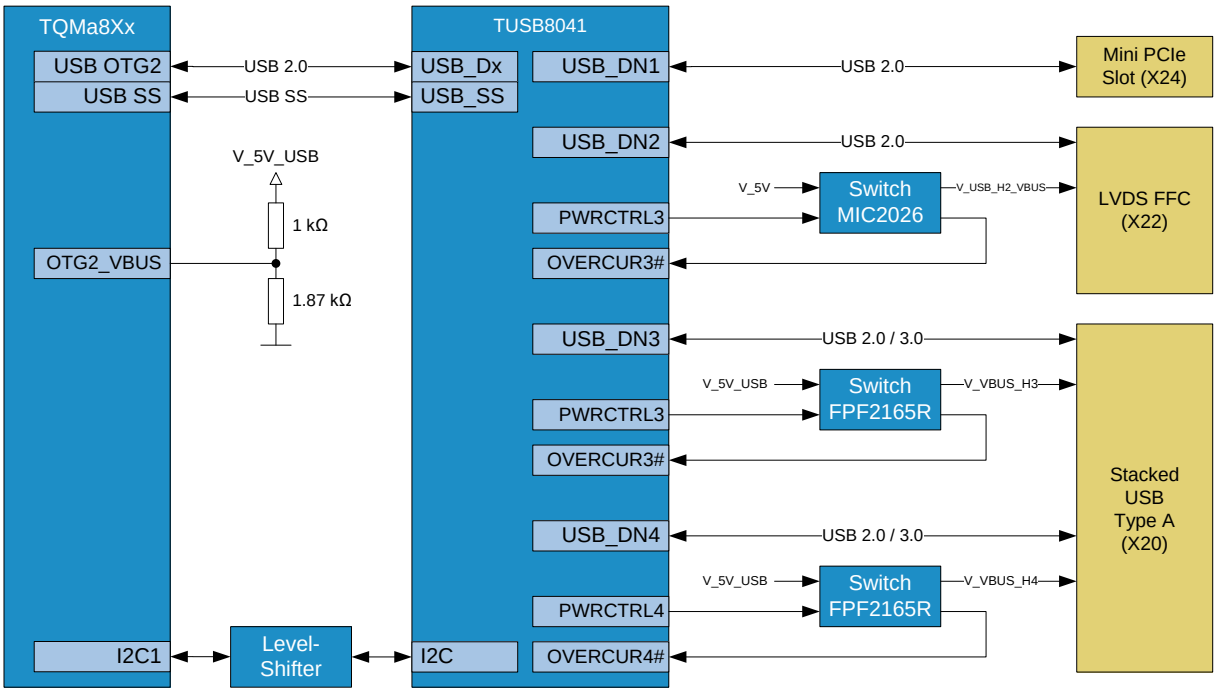


Figure 7: Block diagram USB hub

Table 17: USB hub Power Management

Config pin on USB hub	Default value MBa8Xx	Description
FULLPWRMGMT#	0	Power Management and Overcurrent inputs active
PWRCTRL_POL	1	PWRCTLx signals are high-active
GANGED	0	Power Management is done individually for each downstream port
AUTOEN#	1	Automatic Charge Mode is deactivated
SMBUS#	1	I^2C mode

The VBUS supply and overcurrent monitoring of the respective USB hosts (except Mini PCIe) is done by power distribution switches. The Mini PCIe interface does not require VBUS voltage.

The USB hub can be configured via the I2C1 bus (optional, see Table 19).

By default the Global Power Reset of the USB hub is connected to the RESET_OUT# signal of the TQMa8Xx. If necessary, the reset source can be changed via resistor assembly option, so that the reset is triggered by a signal from the GPIO port expander (see also chapter 3.4).

Table 18: Assembly option Reset USB hub

Reset source / signal	R383	R384	R385	Remark
TQMa8Xx (RESET_OUT#)	NP	NP	0 Ω	Default
GPIO Port Expander (USB_RESET#)	10 kΩ	0 Ω	NP	–

By default the I2C1 bus is not connected to the USB hub. This can be done by assembling two resistors, as shown in the table below.

Table 19: Assembly option I2C1 bus am USB hub

I2C1 bus	R201	R202	Remark
Not connected	NP	NP	Default
Connected	0 Ω	0 Ω	–

3.8 Data interfaces

3.8.1 Audio

The MBa8Xx provides one microphone, line-in and line-out interface each. The signals can be tapped via 3.5 mm jacks. The TLV320AIC3204 from Texas Instruments is used as the audio codec. It is connected to the processor module via SAI (configured as I^2S) and I^2C interfaces.

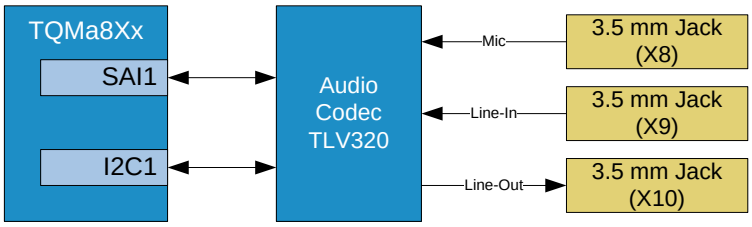


Figure 8: Block diagram Audio

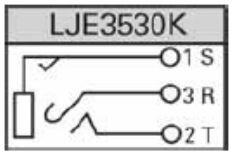


Figure 9: Pinout 3.5 mm jack

Table 20: Pinout Audio (X8, X9, X10)

Channel	Pin	Signal	Dir.	Level	Remark
MIC (X8)	1	AGND_AUD	P	0 V	Ground (filtered from GND)
	2	MIC_IN_L	A_I	0.9 V	Mic left (Mono)
	3	MIC_IN_R	A_I	0.9 V	Mic right (not used ⇨ pull-down to AGND_AUD)
Line-In (X9)	1	AGND_AUD	P	0 V	Ground (filtered from GND)
	2	LINE_IN_L	A_I	1.65 V	Line-In left
	3	LINE_IN_R	A_I	1.65 V	Line-In right
Line-Out (X10)	1	AGND_AUD	P	0 V	Ground (filtered from GND)
	2	LINE_OUT_L	A_O	1.65 V	Line-Out left
	3	LINE_OUT_R	A_O	1.65 V	Line-Out right

3.8.1 Audio (continued)

Table 21: Mic (X8), Line-In (X9), Line-Out or Headphone (X10)

Channel	Parameter	Min.	Typ.	Max.	Remark
MIC, Line-In	Sampling rate ADC	8 kHz		192 kHz	–
	Input voltage			0.9 V	Depends on configured common mode voltage
	Mic bias			3.3 V	Programmable, depends on common mode voltage
	Gain / volume control Analog Digital	 0 dB –12 dB		 47.5 dB 20 dB	Programmable (in 0.5 dB steps)
Line-Out	Sampling rate ADC	8 kHz		192 kHz	–
	Output voltage			1.65 V	Depends on configured common mode voltage
	Load Line-Out (Stereo) Headphone (Stereo) Headphone (Mono)	 0.6 kΩ 14.4 Ω 24.4 Ω	 10 kΩ 16 Ω 32 Ω		 Single-ended Differential
	Output power headphone Normal mode Maximum mode			 15 mW 40 mW	Per channel, single-ended Common-Mode voltage 0.9 V Common-Mode voltage 1.65 V
	Gain / volume control Analog Digital	 –6 dB –63.5 dB		 29 dB 24 dB	Programmable (in 1 dB steps)
	Signal to Noise Ratio		100 dB		Stereo, single-ended, depends on common mode voltage

A placement option allows to choose between Line-Out and Headphone. The following table describes the configuration.

Table 22: Assembly option Line-Out / Headphone

Mode	R136	R137	R138	R139	Remark
Line-Out	0 Ω	0 Ω	NP	NP	Default
Headphone	NP	NP	0 Ω	0 Ω	–

3.8.2 CAN

Both CAN interfaces of the MBa8Xx are directly connected to the CAN ports of the TQMa8Xx and are available at the two 3-pin connectors X11 and X12. Both interfaces are galvanically isolated with 1 kV. The CAN interfaces are not electrically isolated from each other.

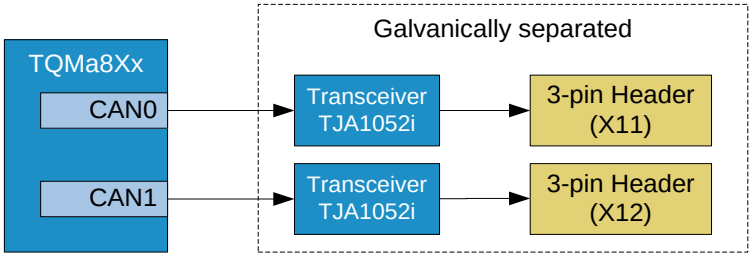


Figure 10: Block diagram CAN

The CAN signals can be terminated with 120 Ω via DIP switches SW1 (CAN0) and SW2 (CAN1).

Table 23: CAN termination

SWx-1	SWx-2	Modus
OFF	OFF	No termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Termination with 120 Ω

Table 24: Pinout CAN0 / 1 (X11, X12)

CAN	Pin	Signal	Dir.	Level	Remark
CAN0	1	CAN0_H	I/O	Spec. (1)	CAN High-Level I/O from CAN0 / galvanically isolated
	2	CAN0_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN0 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated
CAN1	1	CAN1_H	I/O	Spec. (1)	CAN High-Level I/O from CAN1 / galvanically isolated
	2	CAN1_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN1 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated

3.8.3 Debug USB

To display debug messages of the TQMa8Xx, the MBa8Xx can be connected as USB 2.0 device to a host via X13.
Four UART interfaces can be connected, which are converted to USB with the 4-port bridge FT4232.
Available UART interfaces:

- UART1 for the Cortex-A35-Core
- SCU_UART for the SCU
- 2 × UART at pin header X4 (can be used freely, e.g. for additionally multiplexed UARTs)

The interface is powered by the external USB host, independent of the MBa8Xx supply.

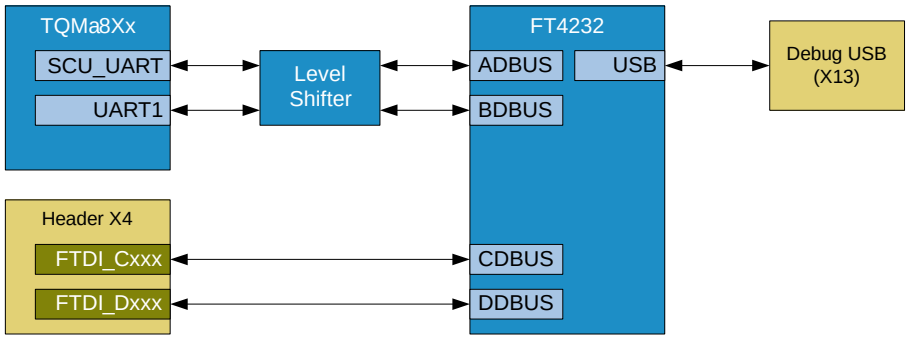


Figure 11: Block diagram USB debug

Note: Connection to the host cannot be established	
	If no connection to the host can be established, the host may require drivers: https://ftdichip.com/Drivers/vcp-drivers/

1: According to CAN standard.

3.8.4 Ethernet

The i.MX 8X CPU and thus the TQMa8Xx provides two independent RGMII interfaces. On the MBa8Xx, both interfaces are configured as Gigabit Ethernet ports. The PHYs support IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T.
The I/O voltage of the RGMII signals is 1.8 V.

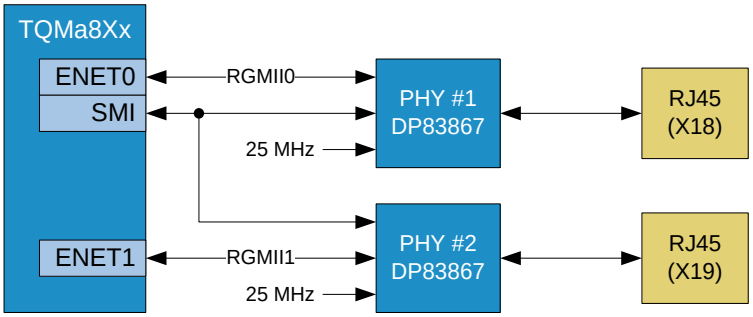


Figure 12: Block diagram Ethernet

Both transceivers are each connected with their own reset and interrupt signals, for which four GPIO signals of the TQMa8Xx are used. The following table shows the signals used.

Table 25: Reset and interrupt signals

Ethernet port	Transceiver function	MBa8Xx signal	TQMa8Xx signal	TQMa8Xx pin	Remark
Ethernet 1	Interrupt input (Pin: INT)	ENET0_INT#	GPIO3_IO00	X2-91	Low-active / pulled-up to V_1V8
	Reset output (Pin: RESET#)	ENET0_RESET#	GPIO3_IO02	X2-92	Low-active / pulled-up to V_1V8
Ethernet 2	Interrupt input (Pin: INT)	ENET1_INT#	GPIO3_IO01	X2-93	Low-active / pulled-up to V_1V8
	Reset output (Pin: RESET#)	ENET1_RESET#	GPIO3_IO03	X2-94	Low-active / pulled-up to V_1V8

3.8.4 Ethernet (continued)

The Transceiver DP83867 has boot straps to start with configurable default values.

The standard configuration on the MBa8Xx is shown in the following table, alternatively, these can be changed via register settings or via placement options.

Table 26: Standard configuration of Ethernet transceivers (boot straps)

Config-Pin on Ethernet-Transceiver [1]	Default MBa8Xx Mode [2]	Description
RX_D0 (Transceiver #1)	1	Addresses for Management Interface (SMI): Transceiver #1 - `0b0000` Transceiver #2 - `0b0011`
RX_D0 (Transceiver #2)	4	
RX_D2	1	
RX_CTRL	3	Not applicable
GPIO_0	1	RGMII RX CLOCK SKEW = 2.0 ns
GPIO_1	1	
LED_2	1	RGMII TX CLOCK SKEW = 2.0 ns
LED_1	1	
		Mode 10/100/1000 Mbit/s available (ANEG_SEL = 0)
LED_0	1	Port Mirroring disabled, SGMII Mode disabled

The activity status of the respective Ethernet port is indicated by the LEDs in the RJ45 sockets. The table shows the default configuration. This can be adapted via register settings in the transceivers. The status messages are identical for both Ethernet ports.

Table 27: Ethernet-LEDs

LED	Colour	Function / Indication
LED left	Green	Connection is established
LED right	Yellow	Send and receive activity

The possible data throughput is influenced by the system load and the software used. With the standard BSP, the following transfer rates can be achieved on the MBa8Xx with a Gigabit link.

Table 28: Characteristics Ethernet 1 / 2 (X18, X19)

Ethernet	Parameter	Min.	Typ.	Max. [3]	Remark
Ethernet 1	Upstream	–	941 Mbit/s	1000 Mbit/s	Remote station Full-Duplex 1 Gbit over CAT 5e
	Downstream	–	895 Mbit/s	1000 Mbit/s	
Ethernet 2	Upstream	–	941 Mbit/s	1000 Mbit/s	Remote station Full-Duplex 1 Gbit over CAT 5e
	Downstream	–	933 Mbit/s	1000 Mbit/s	

1: Identical for both transceivers unless explicitly stated.
2: A detailed description of the modes and their configuration can be found in data sheet (6).
3: Theoretical maximal value.

3.8.5 GPIO

Some GPIOs are used on the MBa8Xx, which are provided by the TQMa8Xx. Some GPIOs are provided via a port expander. The port expander is described in chapter 3.4. The following TQMa8Xx GPIOs are used:

Table 29: GPIO TQMa8Xx

Source	Signal	Target	CPU config / connection on MBa8Xx
GPIO0_IO30	V_1V5_MPCIE_EN	LT3503	Output / 10 kΩ pull-down
GPIO0_IO31	V_3V3_MPCIE_EN	FDC6331	Output / 10 kΩ pull-down
GPIO1_IO07	LCD_CONTRAST	LVDS connector	Output, Mux: LCD_PWM0 / –
GPIO1_IO29	LCD_RESET#		Output / 10 kΩ pull-down
GPIO1_IO30	LCD_BLT_EN		Output / 10 kΩ pull-down
GPIO1_IO25	LCD_PWR_EN		Output / 10 kΩ pull-down
GPIO1_IO13	SWITCH_A#	User button	Input / 10 kΩ pull-up
GPIO1_IO14	SWITCH_B#		
GPIO3_IO00	ENET0_INT#	DP83867	Input / 2.2 kΩ pull-up
GPIO3_IO01	ENET1_INT#		Input / 2.2 kΩ pull-up
GPIO3_IO02	ENET0_RESET#		Output / 10 kΩ pull-up
GPIO3_IO03	ENET1_RESET#		Output / 10 kΩ pull-up
GPIO3_IO07	MIPI_CSI_EN	CSI interface	Output, Mux: MIPI_CSI_EN / 10 kΩ pull-down
GPIO3_IO08	MIPI_CSI_RST#		Output, Mux: MIPI_RST# / 10 kΩ pull-down
M4_GPIO0_IO03	M4_GPIO0_IO03		Input/Output / –
M4_GPIO0_IO02	M4_GPIO0_IO02	Header	Input/Output / –
GPIO1_IO26	GPIO1_IO26	Header and CSI interface	Input/Output / –

3.8.6 Display interfaces

3.8.6.1 eDP / DisplayPort

Attention: Availability DisplayPort interface	
	Since MBa8Xx revision 0203 this circuit part is no longer provided due to insufficient software support of the SN65DSI86. The MBa8Xx Rev.0300 will therefore use the alternative eDP bridge TC9595XBG from Toshiba in the future, which offers better Linux support.

In addition to the standard LVDS interface (X14), an eDP or DisplayPort connection is also available on the MBa8Xx to connect monitors. This is implemented with the DSI-Bridge SN65DSI86, which converts both LVDS/DSI ports of the TQMa8Xx to an embedded DisplayPort. Thus the port supports 4K and Full HD.

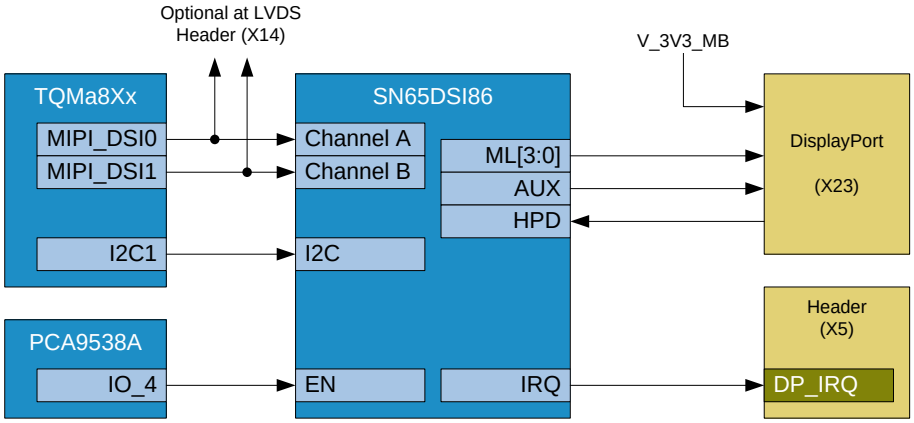


Figure 13: Block diagram DisplayPort / eDP

Note: Specification differences between eDP and DisplayPort	
	Due to different electrical specifications of eDP and DisplayPort, it may be necessary to adapt the voltage swing or pre-emphasis level via software. For details see data sheet of SN65DSI86.

Note: Parallel usage of LVDS and DisplayPort interfaces	
	The information on limited use of the LVDS interface with simultaneous use of the DisplayPort interface in chapter 3.8.6.2 must be observed.

3.8.6.1 eDP / DisplayPort (continued)

Media type: eDP / DisplayPort
Interface TQMa8Xx: MIPI-DSI0 und MIPI-DSI1 (via eDP-Bridge); I2C1
Compatibility: eDP 1.4 / DisplayPort 1.2a
Transfer rate: Up to 5.4 Gbps (max. theoretical value according to Spec.)
ESD protection: ±12 kV Contact Discharge according to IEC 61000-4-2 (all signals)

Table 30: Supply voltage (V_3V3_MB) at eDP / DisplayPort (X23)

Parameter	Min.	Typ.	Max.
Output voltage	3.25 V	3.3 V	3.35 V
Output current	–	–	500 mA

The I²C address of the eDP bridge is determined by the input level of the ADDR pin, among other things. By resistor reassembly, the I²C address can be changed according to Table 31.

Table 31: Assembly option I²C address eDP bridge

7-bit address	R103	R104	Remark
0x2C	NP	10 kΩ	Default
0x2D	10 kΩ	NP	–

3.8.6.2 Dual channel LVDS / MIPI_DSI

Two separate LVDS interfaces are available on the MBa8Xx. The interfaces are provided by a combined transceiver from the i.MX 8X, which outputs either MIPI-DSI or LVDS. The maximum possible resolutions depend on the type of transceiver. MIPI-DSI supports 1920x1200 (WUXGA) at 60 fps, LVDS supports 1920x1080 (Full HD) at 60 fps. The LVDS signals are provided as Dual Channel interface on connector X14.

On a second connector X22, various supply voltages (12 V, 5 V) as well as USB and configuration signals are available.

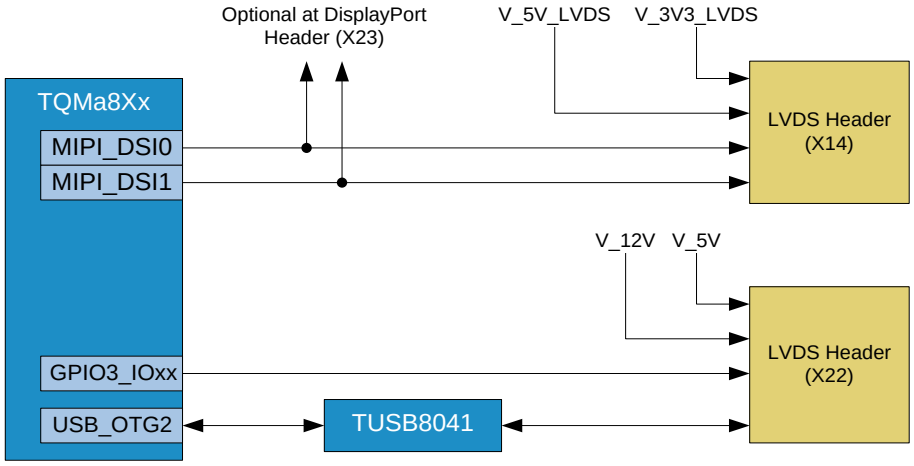


Figure 14: Block diagram Dual-Channel LVDS

Note: Limited use of the DisplayPort interface	
	For MBa8Xx revisions older than revision 0203: • LVDS (X14) and the eDP / DisplayPort interface (X23) use the same LVDS lanes of the TQMa8Xx. • Due to the associated automatic signal termination in the eDP bridge, only one of the two interfaces can be used at a time. • If the eDP / DisplayPort is not used, the eDP bridge must be deactivated by EN signal (by port expander PCA9538A). This automatically deactivates the low impedance termination in the SN65DSI86 and the LVDS interface (X14) can be used. Since MBa8Xx revision 0203 this circuit part is no longer offered

3.8.6.2 Dual channel LVDS / MIPI_DSI (continued)

Table 32: Pinout LVDS (X14)

Pin	Signal	Dir.	Level	Remark
1	MIPI_DSI0_DATA0–	O	1.8 V	DSI interface 1 (Lane 0)
2	MIPI_DSI0_DATA0+	O	1.8 V	
3	MIPI_DSI0_DATA1–	O	1.8 V	DSI interface 1 (Lane 1)
4	MIPI_DSI0_DATA1+	O	1.8 V	
5	MIPI_DSI0_DATA2–	O	1.8 V	DSI interface 1 (Lane 2)
6	MIPI_DSI0_DATA2+	O	1.8 V	
7	GND	P	0 V	Ground
8	MIPI_DSI0_CLOCK–	O	1.8 V	DSI interface 1 (Clock)
9	MIPI_DSI0_CLOCK+	O	1.8 V	
10	MIPI_DSI0_DATA3–	O	1.8 V	DSI interface 1 (Lane 3)
11	MIPI_DSI0_DATA3+	O	1.8 V	
12	MIPI_DSI1_DATA0–	O	1.8 V	DSI interface 2 (Lane 0)
13	MIPI_DSI1_DATA0+	O	1.8 V	
14	GND	P	0 V	Ground
15	MIPI_DSI1_DATA1–	O	1.8 V	DSI interface 2 (Lane 1)
16	MIPI_DSI1_DATA1+	O	1.8 V	
17	GND	P	0 V	Ground
18	MIPI_DSI1_DATA2–	O	1.8 V	DSI interface 2 (Lane 2)
19	MIPI_DSI1_DATA2+	O	1.8 V	
20	MIPI_DSI1_CLOCK–	O	1.8 V	DSI interface 2 (Clock)
21	MIPI_DSI1_CLOCK+	O	1.8 V	
22	MIPI_DSI1_DATA3–	O	1.8 V	DSI interface 2 (Lane 3)
23	MIPI_DSI1_DATA3+	O	1.8 V	
24	GND	P	0 V	Ground
25	V_5V_LVDS	P	5 V	5 V supply voltage (filtered from V_5V)
26	V_5V_LVDS	P	5 V	
27	V_5V_LVDS	P	5 V	
28	V_3V3_LVDS	P	3.3 V	3.3 V supply voltage (filtered from V_3V3_MB)
29	V_3V3_LVDS	P	3.3 V	
30	V_3V3_LVDS	P	3.3 V	
M1, M2	GND	P	0 V	Ground

3.8.6.2 Dual channel LVDS / MIPI_DSI (continued)

Table 33: Pinout LVDS (X22)

Pin	Signal	Dir.	Level	Remark
1	V_12V	P	12 V	12 V supply voltage
2	V_12V	P	12 V	
3	V_12V	P	12 V	
4	GND	P	0 V	Ground
5	GND	P	0 V	
6	GND	P	0 V	
7	V_5V	P	5 V	5 V supply voltage
8	V_5V	P	5 V	
9	GND	P	0 V	Ground
10	GND	P	0 V	
11	V_USB_H2_VBUS	P	5 V	VBUS USB Host 2
12	GND	P	0 V	Ground
13	USBH2_D–	I/O	3.3 V	Data USB Host 2
14	USBH2_D+	I/O	3.3 V	
15	GND	P	0 V	Ground
16	LCD_RESET#	O_{PD}	1.8 V	Reset (TQMa8Xx: GPIO1_IO29)
17	LCD_BLT_EN	O_{PD}	1.8 V	Backlight-Enable (TQMa8Xx: GPIO1_IO30)
18	LCD_PWR_EN	O_{PD}	1.8 V	Power-Enable (TQMa8Xx: GPIO1_IO25)
19	LCD_CONTRAST	O	1.8 V	PWM Contrast-/ Brightness (TQMa8Xx: GPIO1_IO07)
20	GND	P	0 V	Ground
M1, M2	GND	P	0 V	Ground

3.8.7 MIPI CSI

The Camera Serial Interface (CSI) of the TQMa8Xx is available on the MBa8Xx on a dedicated connector. Camera data can be processed with max. 4K@30 fps.

Connectors and pin assignment correspond to a TQ internal standard, which enables the connection of the TQ camera adapter MBaxCA. The camera adapter is designed for Basler camera modules.

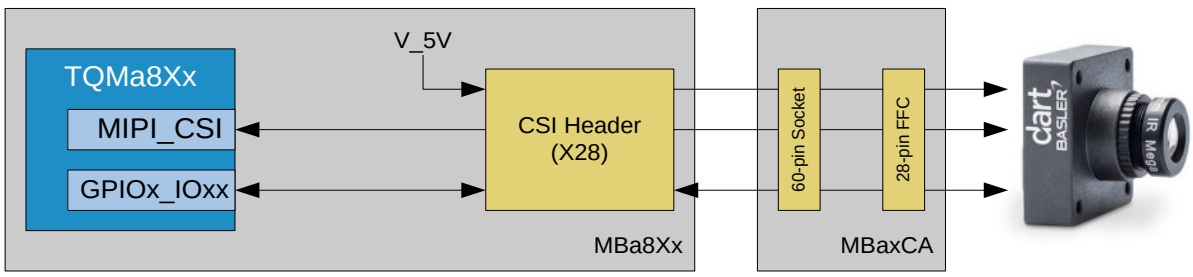


Figure 15: Block diagram MIPI CSI

3.8.7 MIPI CSI (continued)

Table 34: Pinout MIPI-CSI (X28)

Pin	Signal	Dir.	Level	Remark
1	GND	P	0 V	Ground
2	GND	P	0 V	
3	MIPI_CSI_EN	O_{PD}	1.8 V	CSI-Enable (TQMa8Xx: GPIO3_IO07)
4	(NC)	–	–	Not connected / reserved
5	MIPI_CSI_RST#	O_{PD}	1.8 V	Reset (TQMa8Xx: GPIO3_IO08)
6	(NC)	–	–	Not connected / reserved
7	GPIO1_IO26	I	1.8 V	General Purpose Input (e.g. Trigger input)
8	(NC)	–	–	Not connected / reserved
9	M4_GPIO0_IO03	I	1.8 V	General Purpose Input (e.g. Sync input)
10	(NC)	–	–	Not connected / reserved
11	(NC)	–	–	
12	(NC)	–	–	
13	GND	P	0 V	Ground
14	GND	P	0 V	
15	MIPI_CSI_D3–	I	1.8 V	CSI interface (Lane 3)
16	(NC)	–	–	Not connected / reserved
17	MIPI_CSI_D3+	I	1.8 V	CSI interface (Lane 3)
18	(NC)	–	–	Not connected / reserved
19	GND	P	0 V	Ground
20	GND	P	0 V	
21	MIPI_CSI_D2–	I	1.8 V	CSI interface (Lane 2)
22	(NC)	–	–	Not connected / reserved
23	MIPI_CSI_D2+	I	1.8 V	CSI interface (Lane 2)
24	(NC)	–	–	Not connected / reserved
25	GND	P	0 V	Ground
26	GND	P	0 V	
27	MIPI_CSI_D1–	I	1.8 V	CSI interface (Lane 1)
28	(NC)	–	–	Not connected / reserved
29	MIPI_CSI_D1+	I	1.8 V	CSI interface (Lane 1)
30	(NC)	–	–	Not connected / reserved
31	GND	P	0 V	Ground
32	GND	P	0 V	
33	MIPI_CSI_D0–	I	1.8 V	CSI interface (Lane 0)
34	(NC)	–	–	Not connected / reserved
35	MIPI_CSI_D0+	I	1.8 V	CSI interface (Lane 0)
36	(NC)	–	–	Not connected / reserved
37	GND	P	0 V	Ground
38	GND	P	0 V	
39	MIPI_CSI_CLK–	I	1.8 V	CSI interface (Clock)
40	(NC)	–	–	Not connected / reserved
41	MIPI_CSI_CLK+	I	1.8 V	CSI interface (Clock)
42	(NC)	–	–	Not connected / reserved
43	GND	P	0 V	Ground
44	GND	P	0 V	
45	MIPI_CSI_SDA	I/O	1.8 V	Data for I^2C configuration interface (TQMa8Xx: GPIO3_IO06 (1))
46	(NC)	–	–	Not connected / reserved
47	MIPI_CSI_SCL	O	1.8 V	Clock for I^2C configuration interface (TQMa8Xx: GPIO3_IO05 (1))
48	(NC)	–	–	Not connected / reserved
49	GND	P	0 V	Ground
50	(NC)	–	–	Not connected / reserved
51	MIPI_CSI_MCLK	O	1.8 V	Master clock
52	(NC)	–	–	Not connected / reserved
53	GND	P	0 V	Ground
54	GND	P	0 V	
55	(NC)	–	–	Not connected / reserved
56	V_5V_CSI	P	5 V	5 V supply (filtered from V_5V), max 0.5 A in total at pins 56, 58, 60
57	(NC)	–	–	Not connected / reserved
58	V_5V_CSI	P	5 V	5 V supply (filtered from V_5V), max 0.5 A in total at pins 56, 58, 60
59	(NC)	–	–	Not connected / reserved
60	V_5V_CSI	P	5 V	5 V supply (filtered from V_5V), max 0.5 A in total at pins 56, 58, 60

1: There are no pull-up resistors on the TQMa8Xx and the MBa8Xx. Additional external pull-ups must be implemented on the CSI adapter if required.

3.8.8 Mini PCIe

On the MBa8Xx a Mini PCIe card slot is available.
The interface is wired with all signals, which the standard provides (e.g. USB, I²C, and PCIe).
The hardware thus supports any standard-compliant Mini-PCIE card.

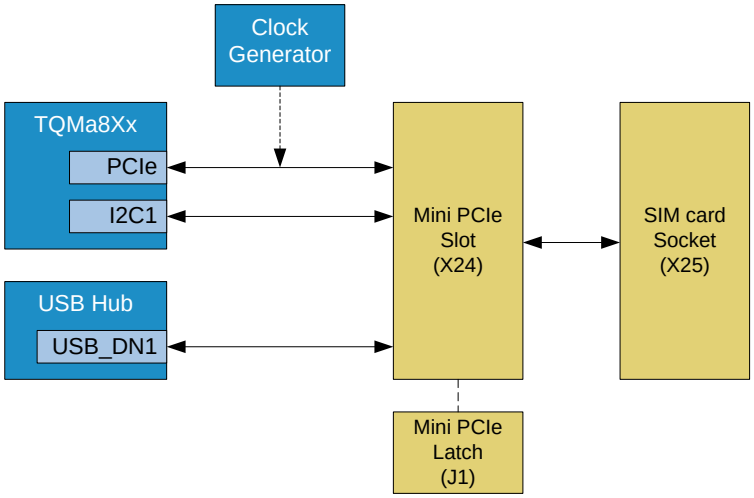


Figure 16: Block diagram Mini PCIe

To use the Mini PCIe interface, the two voltage regulators for the voltages V_1V5_MPCIE and V_3V3_MPCIE must be activated first. Thus, the power sequencing requirements of the Mini PCIe standard can be met. Two GPIO signals of the TQMa8Xx are used for this. The following table shows the used signals.

Table 35: Reset- and Interrupt signals of Ethernet-Transceiver

Voltage	MBa8Xx signal	TQMa8Xx signal	TQMa8Xx pin	Remark
V_1V5_MPCIE	V_1V5_MPCIE_EN	GPIO0_IO30	X1-24	High-active / pulled-down to GND
V_3V3_MPCIE	V_3V3_MPCIE_EN	GPIO0_IO31	X1-26	High-active / pulled-down to GND

An additional SIM card holder for GSM cards is provided (for further information see chapter 3.8.9).

Media type: Mini-PCI Express (cards with size 50.95 mm x 30 mm)
Interface TQMa8Xx: PCIe
Compatibility: PCI Express Base Specification, Revision 4.0, Version 0.7
PCI Express® Mini Card Electromechanical Specification Revision 2.1
Transfer rate: Up to 8 Gbps (max. theoretical value according to spec.)
ESD protection: Not available on the MBa8Xx

Table 36: V_1V5_MPCIE, V_3V3_MPCIE at Mini PCIe (X24)

Voltage	Parameter	Min.	Typ.	Max.	Remark
V_3V3_MPCIE	Output voltage	3.2 V	3.3 V	3.35 V	–
	Output current	–	–	1.1 A	Max. 0.5 A per pin at X24
V_1V5_MPCIE	Output voltage	1.44 V	1.5 V	1.53 V	–
	Output current	–	–	375 mA	–

3.8.8 Mini PCIe (continued)

Table 37: Pinout Mini PCIe (X24)

Pin	Signal	Dir.	Level	Remark
1	PCIE_WAKE#	I	3.3 V	Wake-Up-Signal of Mini PCIe card
2	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
3	(NC)	–	–	Not connected / reserved
4	GND	P	0 V	Ground
5	(NC)	–	–	Not connected / reserved
6	V_1V5_MPCIE	P	1.5 V	1.5 V supply voltage
7	PCIE_CLKREQ#	I	3.3 V	Clock-Request of Mini PCIe card
8	UIM_PWR	O	– (1)	Supply voltage for SIM card
9	GND	P	0 V	Ground
10	UIM_DATA	I/O	– (1)	Bidirectional data line for SIM card
11	PCIE_REFCLK–	O	0.7 V	PCIe reference clock
12	UIM_CLK	O	– (1)	Clock output for SIM card
13	PCIE_REFCLK+	O	0.7 V	PCIe reference clock
14	UIM_RST	O	– (1)	Reset output for SIM card
15	GND	P	0 V	Ground
16	UIM_VPP	O	– (1)	Programming voltage for SIM card
17	(NC)	–	–	Not connected / reserved
18	GND	P	0 V	Ground
19	(NC)	–	–	Not connected / reserved
20	PCIE_DISABLE#	O	3.3 V	Disable signal for Mini PCIe card (PCIE_DIS# level converted by GPIO port expander)
21	GND	P	0 V	Ground
22	PCIE_PERST#	O	3.3 V	Power-Good of Mini PCIe card
23	PCIE_RX–	I	0.7 V	PCIe receive
24	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
25	PCIE_RX+	I	0.7 V	PCIe receive
26	GND	P	0 V	Ground
27	GND	P	0 V	Ground
28	V_1V5_MPCIE	P	1.5 V	1.5 V supply voltage
29	GND	P	0 V	Ground
30	I2C1_SCL_3V3	O_{PU}	3.3 V	I^2C clock (I2C1_SCL level shifted)
31	PCIE_TX–	O	0.7 V	PCIe transmit
32	I2C1_SDA_3V3	I/O_{PU}	3.3 V	I^2C data (I2C1_SDA level shifted)
33	PCIE_TX+	O	0.7 V	PCIe transmit
34	GND	P	0 V	Ground
35	GND	P	0 V	Ground
36	USBH1_D–	I/O	3.3 V	Data USB Host 1
37	GND	P	0 V	Ground
38	USBH1_D+	I/O	3.3 V	Data USB Host 1
39	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
40	GND	P	0 V	Ground
41	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
42	LED_WWAN#	I	3.3 V	Status input WWAN# (see chapter 3.9.5)
43	GND	P	0 V	Ground
44	LED_WLAN#	I	3.3 V	Status input WLAN# (see chapter 3.9.5)
45	(NC)	–	–	Not connected / reserved
46	LED_WPAN#	I	3.3 V	Status input WPAN# (see chapter 3.9.5)
47	(NC)	–	–	Not connected / reserved
48	V_1V5_MPCIE	P	1.5 V	1.5 V supply voltage
49	(NC)	–	–	Not connected / reserved
50	GND	P	0 V	Ground
51	(NC)	–	–	Not connected / reserved
52	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage

1: Depending on the Mini PCIe card used.

3.8.8 Mini PCIe (continued)

By default, the Mini PCIe reference clock for the i.MX 8X processor and the Mini PCIe card is generated by a clock generator (Renesas 9FGV0241). This implementation is based on a recommendation from NXP and the experience of other i.MX processors, that the CPU internal PCIe reference clock usually does not meet the JEDEC jitter specifications.

For test purposes the reference clock of the TQMa8Xx4 can also be used directly. The required assembly options are described in the following table.

Table 38: Assembly option Mini PCIe reference clock

Mode	R318	R319	C23	C24	R157	R158	R471	R472	Remark
Discrete clock generator	NP	NP	NP	NP	0 Ω	0 Ω	0 Ω	0 Ω	Default
Clock from TQMa8Xx4	49.9 Ω	49.9 Ω	100 nF	100 nF	NP	NP	NP	NP	–

Attention: PCIe clock generator on TQMa8Xx4 present	
	When using a TQMa8Xx4 with assembled PCIe clock generator, the above assembly option (TQMa8Xx4 as reference clock) is compulsory to be implemented. This prevents the two clock generators from the TQMa8Xx4 and the MBa8Xx driving against each other.

The separate clock generator 9FGV0241 offers the possibility to vary the spread spectrum at the clock outputs.
By default the spread option is disabled.

Table 39: Assembly option Spread Spectrum of the Mini PCIe reference clock

Spread-Option	R1	R2	Remark
Spread off	NP	1 kΩ	Default
Spread = –0.25 %	NP	NP	–
Spread = –0.5 %	1 kΩ	NP	–

By default the I2C1 bus is not connected to the Mini PCIe clock generator. This can be done, as shown in the following table, by assembling two resistors.

Table 40: Assembly option I2C1 bus at Mini PCIe clock generator

I2C1 bus	R155	R156	Remark
Not connected	NP	NP	Default
Connected	0 Ω	0 Ω	–

3.8.9 SIM card

A SIM card holder (X25) is available on the MBa8Xx for the use of a SIM card, which is directly connected to the Mini PCIe interface.

Media type: GSM (SIM cards with form factor 2FF/UICC)
Interface TQMa8Xx: –
Compatibility: Specification of the Subscriber Identity Module - Mobile Equipment Interface (GSM 11.11)
Transfer rate: –
ESD protection: Not available on the MBa8Xx

3.8.10 USB 3.0 Host

Two USB 3.0 host interfaces are provided on X20 (Top: USB Host 3; Bottom: USB Host 4). The maximum output current of each Host is 900 mA (per port). Since the TQMa8Xx only provides two USB interfaces and one of them is used as a debug interface on the MBa8Xx, the second USB interface of the TQMa8Xx is connected to a hub, which provides two additional, internally used USB 2.0 hosts in addition to the two USB 3.0 hosts described here. Further details can be found in chapter 3.7.

The USB 3.0 OTG port of the TQMa8Xx provides a theoretical data rate of 5 Gbps. This is divided among the connected ports of the USB 3.0 hub. Depending on the software and hardware used, the effective read and write rates of the ports can vary.

3.8.11 USB 2.0 OTG

USB OTG1 is connected as USB 2.0 OTG to a separate USB socket (type Micro AB) and can be used for the serial downloader.

The maximum output current of USB OTG1 is 500 mA (as Host) and the theoretical data rate is 480 Mbps. Depending on the software and hardware used, the effective read and write rates of the ports may vary.

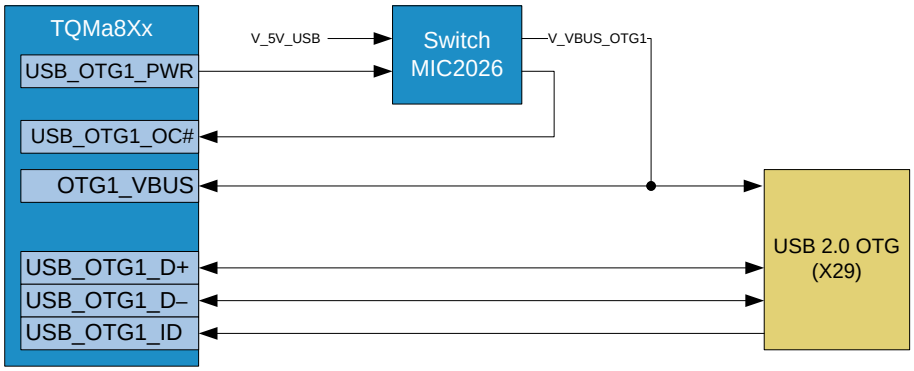


Figure 17: Block diagram USB OTG

3.8.12 SD card

The SD card connector is directly connected to the SDHC controller of the TQMa8Xx via a 4-bit wide data interface.

The SDHC controller in the TQMa8Xx basically supports UHS-I SD cards in transfer mode SDR104 according to the SD card standard 3.0. This allows transfer rates of up to 104 Mbyte/s.

The SD card is permanently supplied with 3.3 V, the pull-ups are also connected to this voltage. But the signals SD1_WP and SD1_CD# have a fixed I/O voltage of 1.8 V. Their 10 kΩ pull-ups are connected to 1.8 V.

It is possible to boot from SD card, see chapter 3.2. All data lines are provided with ESD protection.

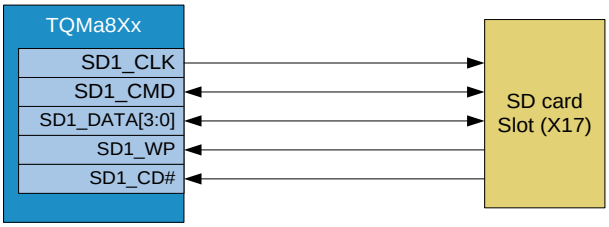


Figure 18: Block diagram SD card

Note: SD card initialisation after reset	
	During a system reset, the host reinitializes the SD card, but the SD card remains in the SDR104 transfer mode and thus also at an I/O voltage of 1.8 V since the supply voltage of the SD card is not power-cycled after a system reset on the MBa8Xx revision 02xx. This will be corrected on the MBa8Xx revision 03xx. Because of this behaviour, the host cannot reinitialize the SD card in SDR104 mode at boot time and communication problems may occur. To avoid this, a power cycle must be performed e.g. by pushing Power Button S5.

3.8.13 MBa8Xx headers (X4, X5)

The MBa8Xx provides two 100 mil headers. All unused signals are made available on these.

Besides the signals, 1.8 V, 3.3 V, 5 V and 12 V are available on each header. The maximum current load of the individual voltages on the headers depends on the load on other connectors. In total, no more than the specified maximum current may be drawn at the following interfaces:

Table 41: Power consumption headers

Rail	I_{max}	Remark
V_12V	3 A	Sum of currents at X4, X5 and X22 [1]
V_5V	2 A	Sum of currents at X4, X5, X14 and X22 [2]
V_3V3_MB	2 A	Sum of currents at X4, X5 and X14 [3]
V_1V8	50 mA	Sum of currents at X4 and X5 if V_1V8 supplied by TQMa8Xx
	1 A	Sum of currents at X4 and X5 if V_1V8 supplied by regulator on MBa8Xx [4]

Note: Observe power consumption with regard to the overall system	
	The supply voltages (1.8 V, 12 V, etc.) provided at the MBa8Xx headers are not individually fused. Technically, an overload of the fuse at the 24 V supply input is therefore possible, see also chapter 3.10. Please note the resulting total current consumption of the MBa8Xx, which must be less than 4 A!

1: The sum of the current consumptions of all 12 V supply voltages at LVDS (X14, X22) and X4 and X5 must not exceed 3 A.
2: The sum of the current consumptions of all 5 V supply voltages at LVDS (X14, X22) and X4, X5 must not exceed 2 A.
3: The sum of the current consumption of all 3.3 V supply voltages at DisplayPort (X23), LVDS (X14, X22) and X4, X5 must not exceed 2 A.
4: Available per assembly option, see Table 51.

3.8.13 MBa8Xx headers (continued)

Table 42: Pinout Header X4

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
P	12 V	Power	V_12V	1	2	V_3V3_MB	Power	5 V	P
P	5 V	Power	V_5V	3	4	V_1V8	Power	1.8 V	P
P	0 V	Power	GND	5	6	GND	Power	0 V	P
O	1.8 V	QSPI	QSPIB_SCLK (1)	7	8	QSPIB_DATA0 (1)	QSPI	1.8 V	I/O
P	0 V	Power	GND	9	10	QSPIB_DATA1 (1)	QSPI	1.8 V	I/O
O	1.8 V	QSPI	QSPIB_SS0# (1)	11	12	QSPIB_DATA2 (1)	QSPI	1.8 V	I/O
O	1.8 V	QSPI	QSPIB_SS1# (1)	13	14	QSPIB_DATA3 (1)	QSPI	1.8 V	I/O
I/O	1.8 V	GPIO	GPIO3_IO15	15	16	GND	Power	0 V	P
P	0 V	Power	GND	17	18	MCLK_IN1	CLK	1.8 V	I
I	1.8 V	QSPI	QSPIB_DQS (1)	19	20	GND	Power	0 V	P
P	0 V	Power	GND	21	22	MCLK_IN0	CLK	1.8 V	I
-	-	-	(NC) (2)	23	24	GND	Power	0 V	P
P	0 V	Power	GND	25	26	FTDI_CTXD	Debug	3.3 V	O_{PD}
O_{PU}	1.8 V	I2C	I2C2_SCL	27	28	FTDI_CRXD	Debug	3.3 V	I
I/O_{PU}	1.8 V	I2C	I2C2_SDA	29	30	GND	Power	0 V	P
P	0 V	Power	GND	31	32	FTDI_DTXD	Debug	3.3 V	O_{PD}
O	1.8 V	SPI	SPI3_SCK	33	34	FTDI_DRXD	Debug	3.3 V	I
I	1.8 V	SPI	SPI3_SDI	35	36	GND	Power	0 V	P
O	1.8 V	SPI	SPI3_SDO	37	38	(NC) (2)	-	-	-
O	1.8 V	SPI	SPI3_CS0	39	40	(NC) (2)	-	-	-
O	1.8 V	SPI	SPI3_CS1	41	42	GND	Power	0 V	P
P	0 V	Power	GND	43	44	(NC) (2)	-	-	-
I	1.8 V	SAI	SAI1_RXFS	45	46	(NC) (2)	-	-	-
I	1.8 V	SAI	SAI1_RXC	47	48	GND	Power	0 V	P
P	0 V	Power	GND	49	50	(NC) (2)	-	-	-
AI	1.8 V (3)	ADC	ADC_IN0	51	52	(NC) (2)	-	-	-
AI	1.8 V (3)	ADC	ADC_IN1	53	54	GND	Power	0 V	P
AI	1.8 V (3)	ADC	ADC_IN2	55	56	I2C1_SDA	I2C	1.8 V	I/O
AI	1.8 V (3)	ADC	ADC_IN3	57	58	I2C1_SCL	I2C	1.8 V	O
P	0 V	Power	GND	59	60	GND	Power	0 V	P

1: No restrictions for TQMa8Xx without SPI flash. For TQMa8Xx with SPI flash the usability/availability may be limited. Details are available on request.
2: Reserved for future use.
3: The reference voltage is determined by the voltage at X3-34.

3.8.13 MBa8Xx headers (continued)

Table 43: Pinout Header X5

I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O
P	12 V	Power	V_12V	1	2	V_3V3_MB	Power	3.3 V	P
P	5 V	Power	V_5V	3	4	V_1V8	Power	1.8 V	P
P	0 V	Power	GND	5	6	GND	Power	0 V	P
O	1.8 V	SPI	SPI1_SCK	7	8	PMIC_PGOOD	Config	1.8 V	O
O	1.8 V	SPI	SPI1_SDO	9	10	PMIC_FSOB_EWARN (1)	Config	1.8 V	O
I	1.8 V	SPI	SPI1_SDI	11	12	PMIC_AMUX_VSD (2)	Config	1.8 / 3.3 V	O
O	1.8 V	SPI	SPI1_CS0	13	14	M4_GPIO0_IO02	M4 GPIO	1.8 V	I/O
O	1.8 V	SPI	SPI1_CS1	15	16	PMIC_WDI	Config	1.8 V	I
P	0 V	Power	GND	17	18	PE1_INT#	Config	1.8 V	O
O	1.8 V	SPI	SPI2_SCK	19	20	SCU_WDOG_OUT (3)	Config	1.8 V	O
O	1.8 V	SPI	SPI2_SDO	21	22	DP_IRQ	Config	–	O_{OD} (4)
I	1.8 V	SPI	SPI2_SDI	23	24	GND	Power	0 V	P
O	1.8 V	SPI	SPI2_CS0	25	26	UART1_RX	UART	1.8 V	I
P	0 V	Power	GND	27	28	UART1_TX	UART	1.8 V	O
I/O	1.8 V	I2C	PMIC_I2C_SDA	29	30	UART1_RTS#	UART	1.8 V	O
O	1.8 V	I2C	PMIC_I2C_SCL	31	32	UART1_CTS#	UART	1.8 V	I
P	0 V	Power	GND	33	34	GND	Power	0 V	P
I/O	3.3 V	I2C	I2C1_SDA_3V3	35	36	M4_I2C_SDA	M4 I2C	1.8 V	I/O_{PU}
O	3.3 V	I2C	I2C1_SCL_3V3	37	38	M4_I2C_SCL	M4 I2C	1.8 V	O_{PU}
P	0 V	Power	GND	39	40	GND	Power	0 V	P
I	1.8 V	TAMPER	TAMPER_IN3	41	42	TAMPER_OUT4	TAMPER	1.8 V	O
I	1.8 V	TAMPER	TAMPER_IN4	43	44	TAMPER_OUT3	TAMPER	1.8 V	O
I	1.8 V	TAMPER	TAMPER_IN2	45	46	TAMPER_OUT2	TAMPER	1.8 V	O
I	1.8 V	TAMPER	TAMPER_IN1	47	48	TAMPER_OUT1	TAMPER	1.8 V	O
I	1.8 V	TAMPER	TAMPER_IN0	49	50	TAMPER_OUT0	TAMPER	1.8 V	O
P	0 V	Power	GND	51	52	GND	Power	0 V	P
O	1.8 V	ENET	ENET0_REFCLK_OUT	53	54	RESET_OUT#	Config	1.8 V	O_{PU}
P	0 V	Power	GND	55	56	TEMP_EVENT#	Config	–	O_{OD} (4)
O	1.8 V	ENET	ENET1_REFCLK_OUT	57	58	(NC) (5)	-	-	-
P	0 V	Power	GND	59	60	GND	Power	0 V	P

1: This signal has different functions depending on the TQMa8Xx variant. See TQMa8Xx User's Manual for details.
2: For factory use only, do not contact.
3: If the i.MX 8X internal watchdog of the SCU is to be used as PMIC watchdog interrupt (PMIC_WDI), pins X5-16 (PMIC_WDI) and X5-20 (SCU_WDOG_OUT) must be connected.
4: Open-Drain Output. Requires external pull-up to supply voltage if used.
5: Reserved for future use.

3.8.14 JTAG

The JTAG interface is routed to a 20-pin header (X15). The required pull-ups of the lines TDI, TMS, and SRST# are available on the MBa8Xx. All signal lines use 1.8 V as reference voltage. The JTAG interface is not ESD protected.

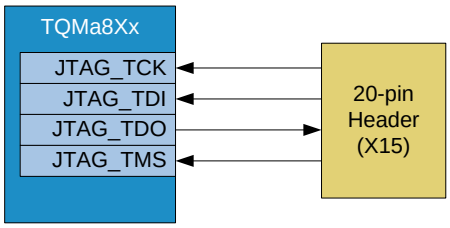


Figure 19: Block diagram JTAG

Table 44: Pinout JTAG (X15)

Pin	Signal	Dir.	Level	Remark
1	JTAG_VREF	P	1.8 V	1.8 V reference voltage for debugger (via series resistor 100 Ω at V_1V8)
2	V_1V8	P	1.8 V (1)	1.8 V supply voltage for debugger
3	SCU_WDOG_OUT	O_{PU}	1.8 V	Watchdog output of i.MX 8X
4	GND	P	0 V	Ground
5	JTAG_TDI	I_{PU}	1.8 V	Test Data In
6	GND	P	0 V	Ground
7	JTAG_TMS	I_{PU}	1.8 V	Test Mode Select
8	GND	P	0 V	Ground
9	JTAG_TCK	I_{PD}	1.8 V	Test Clock
10	GND	P	0 V	Ground
11	(NC)	I_{PD}	1.8 V	Not used (pulled to GND)
12	GND	P	0 V	Ground
13	JTAG_TDO	O	1.8 V	Test Data Out
14	GND	P	0 V	Ground
15	JTAG_SRST#	I/O_{PU}	1.8 V	System Reset (see also chapter 3.11)
16	GND	P	0 V	Ground
17	(NC)	I_{PU}	1.8 V	Not used (pulled to V_1V8)
18	GND	P	0 V	Ground
19	(NC)	I_{PD}	1.8 V	Not used (pulled to GND)
20	GND	P	0 V	Ground

By default the debugger is supplied with 1.8 V at X15-2. Alternatively, the supply voltage can be changed to 3.3 V using the placement option. The maximum output current is 10 mA. The following table shows the corresponding changes.

Table 45: Assembly option supply voltage JTAG

Voltage	R141	R142	Remark
1.8 V (V_1V8)	0 Ω	NP	Default
3.3 V (V_3V3_MB)	NP	0 Ω	–

1: Can be changed by assembly option, see Table 45.

3.9 User interfaces

3.9.1 Reset button

Reset button S4 resets the CPU and PMIC on the TQMa8Xx. The generated reset signal simultaneously activates the RESET_OUT# signal, which also resets various components on the MBa8Xx.

3.9.2 Power button

Button S5 is directly connected to pin PMIC_PWRON of the TQMa8Xx. By pressing the button the PMIC is switched off (Off-Mode; low-active).

3.9.3 On/Off button

Button S6 is directly connected to pin IMX_ONOFF of the TQMa8Xx. Pressing the button triggers the ON/OFF function of the i.MX 8X.

3.9.4 GPI buttons

Two buttons (S2, S3) are available on the MBa8Xx for user-specific use. These buttons are connected to two GPIO pins of the TQMa8Xx.

Table 46: General Purpose buttons

Button	Signal	GPIO at TQMa8Xx	TQMa8Xx pin	Remark
S2	SWITCH_A#	GPIO1_IO13	X3-5	Low-active / pulled-up to V_1V8
S3	SWITCH_B#	GPIO1_IO14	X3-3	Low-active / pulled-up to V_1V8

3.9.5 Status LEDs

In addition to the status LEDs of the two Ethernet sockets, the MBa8Xx provides more indicator LEDs:

Table 47: Status-LEDs

Function group	LED	Colour	Indication
Reset	V1	Red	Indicates the reset status of the des TQMa8Xx (at signal RESET_OUT#)
USB	V3	Green	Indicates the presence of VBUS for USB Host 2
	V4	Green	Indicates the presence of VBUS for USB Host 3
	V5	Green	Indicates the presence of VBUS for USB Host 4
	V88	Green	Indicates the presence of VBUS for USB OTG
Mini PCIe	V7	Green	Shows the status of the WWAN# signal on the Mini-PCIe interface
	V8	Green	Shows the status of the WLAN# signal on the Mini-PCIe interface
	V9	Green	Shows the status of the WPAN# signal on the Mini-PCIe interface
User LEDs	V12	Green	Programmable LED (LED_A) on I^2C GPIO Expander [1]
	V13	Green	Programmable LED (LED_B) on I^2C GPIO Expander [1]
Power [2]	V14	Green	Indicates the presence of the external 24 V supply voltage (V_24V)
	V15	Green	Indicates the presence of the internal 12 V supply voltage (V_12V)
	V16	Green	Indicates the presence of the internal 5 V supply voltage (V_5V)
	V17	Green	Indicates the presence of the internal 3.3 V supply voltage (V_3V3)
	V18	Green	Indicates the presence of the internal 3.3 V supply voltage (V_3V3_MB)
	V19	Green	Indicates the presence of the internal 3.3 V supply voltage (V_1V8)
	V20	Green	Indicates the presence of the internal 3.3 V supply voltage (V_5V_USB)
	V21	Green	Indicates the presence of the internal 3.3 V supply voltage (V_3V3_MPCIE)
	V22	Green	Indicates the presence of the internal 3.3 V supply voltage (V_1V5_MPCIE)
Debug	V72	Green	Indicates the presence of an external USB supply voltage an X13

1: For further information, see chapter 3.4.
2: For details on the supply concept and the distribution of the internal supply voltages, refer to chapter 3.10.

3.10 Power supply

The MBa8Xx must be supplied with 24 V DC (typ.) via one of the two connections X26 and X27, which can be used alternatively.

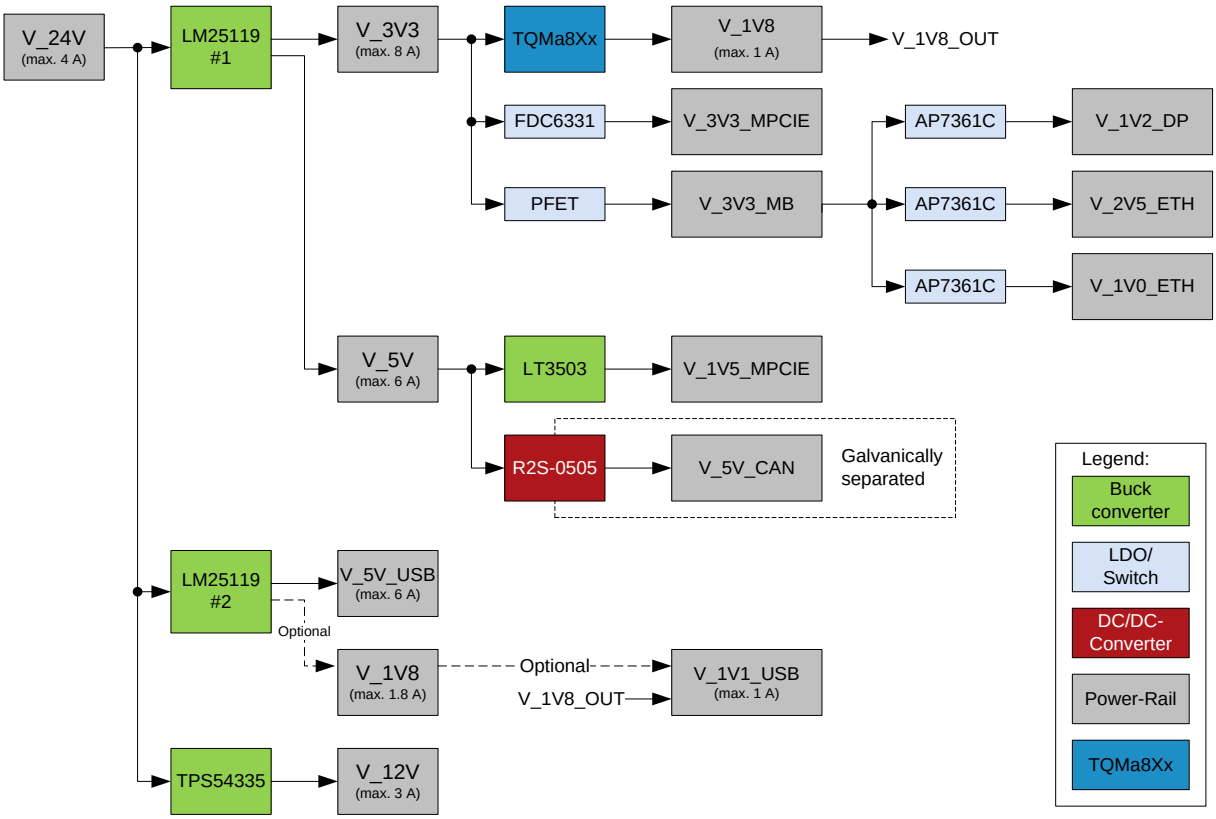


Figure 20: Block diagram MBa8Xx power supply

Figure 20 shows all voltages (rails) on the MBa8Xx, which are divided into three main paths consisting of two LM25119 and one TPS45335. These supply the largest loads. (TQMa8Xx, USB supply, 12 V display supply.)

The design also allows power sequencing of all voltage levels used. With the exception of V_3V3, all voltages are switched on after the TQMa8Xx boots. A 1.8 V supply is already provided by the TQMa8Xx and delivers up to 1000 mA.

The 1.8 V supply is provided by default directly from the TQMa8Xx via pin X2-12 (V_1V8_OUT). The second part of the LM25119 (#2) is optional and can be used if the 1.8 V rail requires more power. The assembly option is described in Table 51.

3.10.1 Input protection

The following protective circuits are provided for the input voltage V_24V of the MBa8Xx:

- Fuse 4 A, slow blow
- Overvoltage protection
- PI Filter (CLC element)
- Reverse polarity protection
- Voltage stabilization

Attention: Voltages at headers	
	The internal voltages (1.8 V, 12 V, etc.) provided at the MBa8Xx headers are not separately fused. Technically an overload of the fuse is therefore possible. The resulting total current consumption of the MBa8Xx should be kept below 4 A in total.

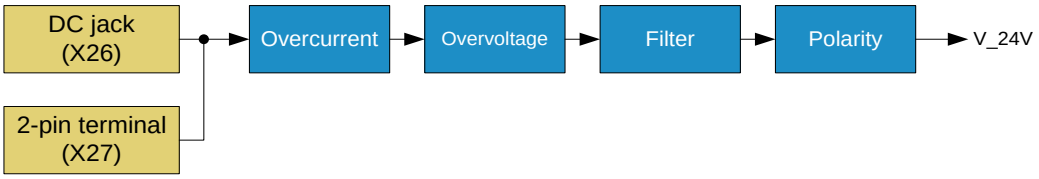


Figure 21: Block diagram Power-In

Table 48: Supply voltage V_24V_IN at Power-In (X26, X27)

Parameter	Min.	Typ.	Max.	Remark
Input voltage	16 V	24 V	26.7 V	–
Power consumption	–	TBD (1)	95 W (2)	–
Rated current of the fuse	–	4 A	–	–
Voltage limitation in case of overvoltage	26.7 V	–	29.5 V	Note: The MBa8Xx may be damaged in case of permanent overvoltage!

Table 49: Pinout Power-In (X26, X27)

Pin	Pin	Signal	Type	Level	Remark
X26	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground
	3	(NC)	–	–	Not connected
X27	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground

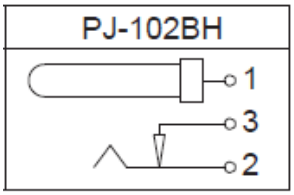


Figure 22: Pinout DC socket 2.5 mm/5.5 mm

1: Typical scenario is not defined.
2: Theoretical full load. All supply voltages are loaded with maximum current, e.g. by connecting additional load to the pin headers, and all system components have maximum power consumption.

3.10.2 Power sequencing

The MBa8Xx allows power sequencing of the voltage levels used. Except for V_3V3 and V_5V_USB all voltages are switched on after the boot process of the TQMa8Xx.

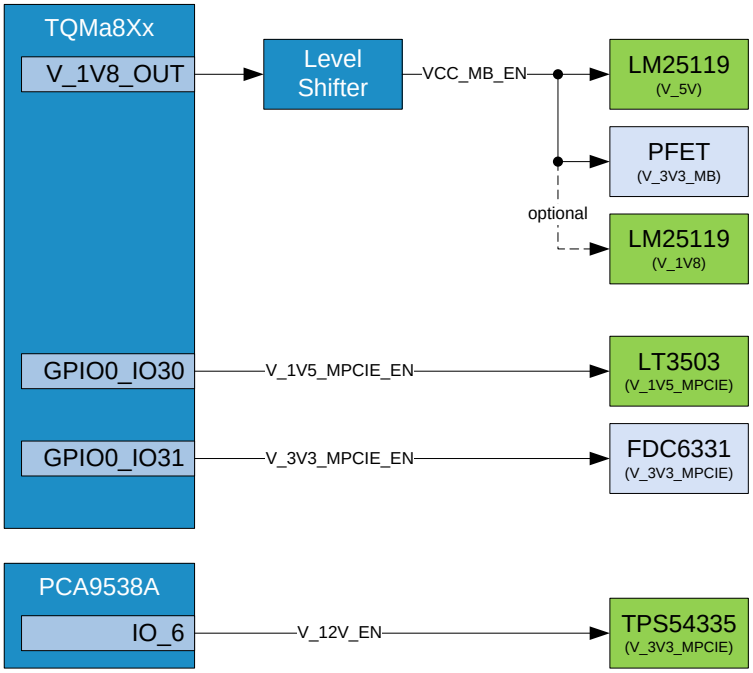


Figure 23: Block diagram Enable signals for Power Sequencing

From Figure 23, the following sequencing of the various voltage levels on the MBa8Xx is given, not considering the rise times of the voltages:

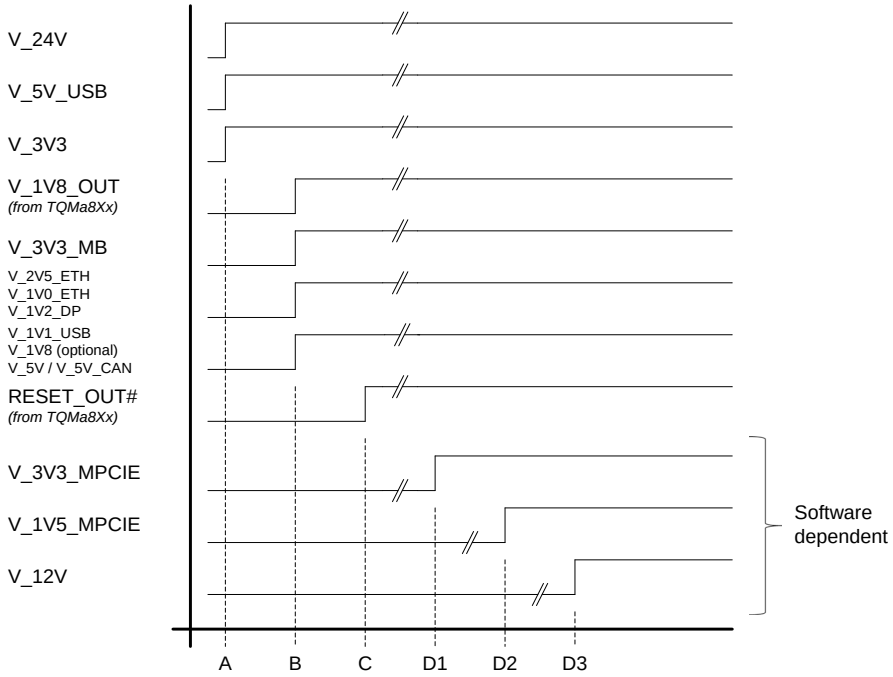


Figure 24: Power sequencing

The following table shows the sequence steps from Figure 24:

Table 50: Power sequencing

Sequence	Description
A	Start point: Power-up MBa8Xx supplies.
B	Release MBa8Xx supplies by V_1V8_OUT.
C	Release RESET_OUT# after completion of TQMa8Xx power sequencing plus preconfigured delay.
D1, D2, D3	Switching on of additional supply by software driver with signals V_3V3_MPCIE_EN, V_1V5_MPCIE_EN and V_12V_EN.

V_1V8_OUT controls the regulators for V_5V and V_1V8, as well as the power FET for V_3V3_MB. Thus the linear regulators for V_2V5_ETH, V_1V0_ETH, V_1V2_DP and V_1V1_USB as well as the DC/DC regulator for V_5V_CAN are activated automatically. Determined by the internal power sequence of the TQMa8Xx, RESET_OUT# is only released with a corresponding time offset after the last voltage level V_1V8_OUT (TQMa8Xx internal V_1V8) is switched on. Thus all necessary voltages on the TQMa8Xx and the carrier board are stable when the system starts.

The 1.8 V supply for the components on the MBa8Xx is provided by default via pin X2-12 (V_1V8_OUT) of the TQMa8Xx. Alternatively, a 1.8 V voltage regulator can be used on the MBa8Xx via a mounting option. The following table shows the corresponding options.

Table 51: Assembly option 1.8 V regulator

1.8 V supply	R182	R364	Remark
TQMa8Xx (V_1V8_OUT)	NP	0 Ω	Default
Voltage regulator on the MBa8Xx (LM25119)	0 Ω	NP	–

3.11 Reset structure

Figure 25 shows the reset structure on the MBa8Xx.

In addition to the reset signals of the TQMa8Xx, the MBa8Xx also provides further software-controlled reset signals for individual function blocks, e.g. ENET reset for the Ethernet transceivers. These are implemented by GPIO signals and named accordingly in the respective chapters when applicable.

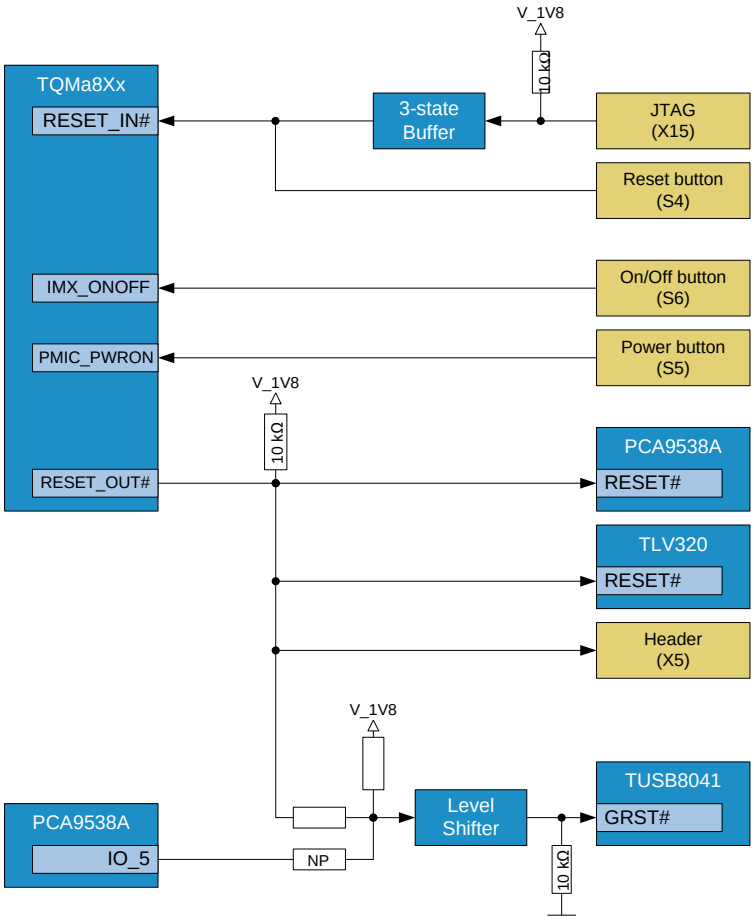


Figure 25: Block diagram Reset

Table 52: RESET_IN# (affects JTAG_SRST# at X15)

Parameter	Min.	Typ.	Max.	Remark
Input voltage				Low-active
High level	1.2 V	1.8 V	5.5 V	
Low level	–	–	0.6 V	

Table 53: RESET_OUT# (at X5)

Parameter	Min.	Typ.	Max.	Remark
Output voltage				Low-active
High level	1.2 V	–	1.84 V	
Low level	–	–	0.5 V	

4. SOFTWARE

No software is required for the MBa8Xx.
Suitable software is only required on the TQMa8Xx and is not a part of this User's Manual.
More information can be found in the TQ-Support Wiki for the TQMa8Xx.

5. MECHANICS

5.1 MBa8Xx dimensions

The MBa8Xx has overall dimensions (length × width × height) of 170 mm × 170 mm × 27.1 mm.
The MBa8Xx has six 4.2 mm mounting holes for the housing, and three 2.7 mm mounting holes for a heat sink.
The MBa8Xx weighs approximately 220 grams without TQMa8Xx.

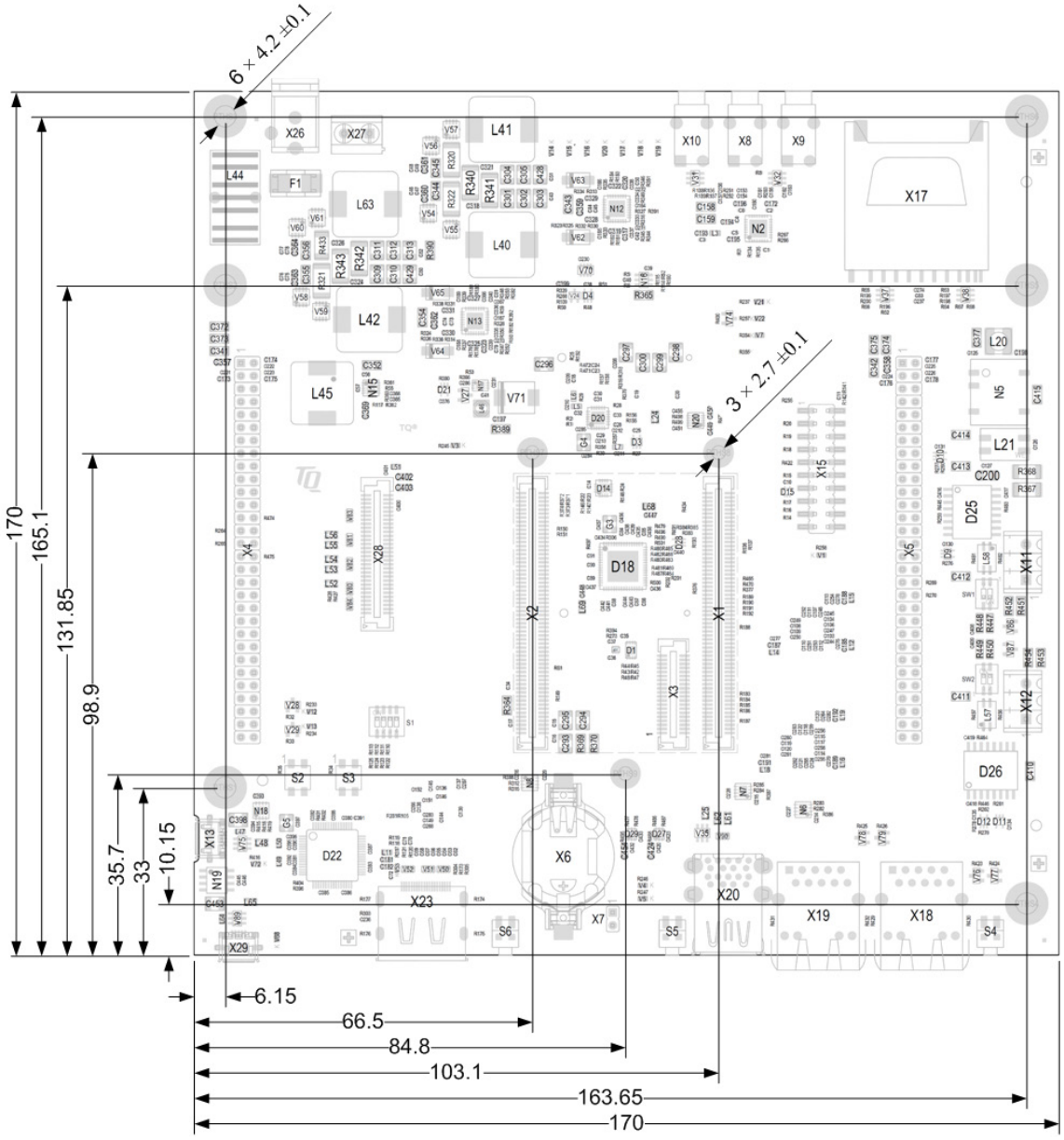


Figure 26: MBa8Xx dimensions

5.2 Notes of treatment

The TQMa8Xx is held in the mating connectors with a retention force of approximately 28 N.

To avoid damaging the TQMa8Xx connectors as well as the carrier board connectors while removing the TQMa8Xx the use of the extraction tool MOZI8XX is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa8Xx for the extraction tool MOZI8XX.

5.3 Embedding in the target system

The MBa8Xx serves as a design base for customer products, as well as a reference platform during development.

5.4 Housing

The form factor and the mounting holes of the MBa8Xx are designed for installation in a standard EURO housing.

5.5 Thermal management

The greatest power dissipation on the MBa8Xx is caused by the voltage regulators. In addition, the TQMa8Xx is a heat source that acts indirectly on the MBa8Xx. Depending on the application, further power dissipation can occur, mainly at additional external loads on the pin headers on the MBa8Xx, the Mini PCIe slot, etc.

For evaluation of the TQMa8Xx under high load conditions an optional heat sink or heat spreader is provided. Three holes are provided on the MBa8Xx for this purpose. The metallization of the mounting hole has GND potential.

5.5 Thermal management (continued)

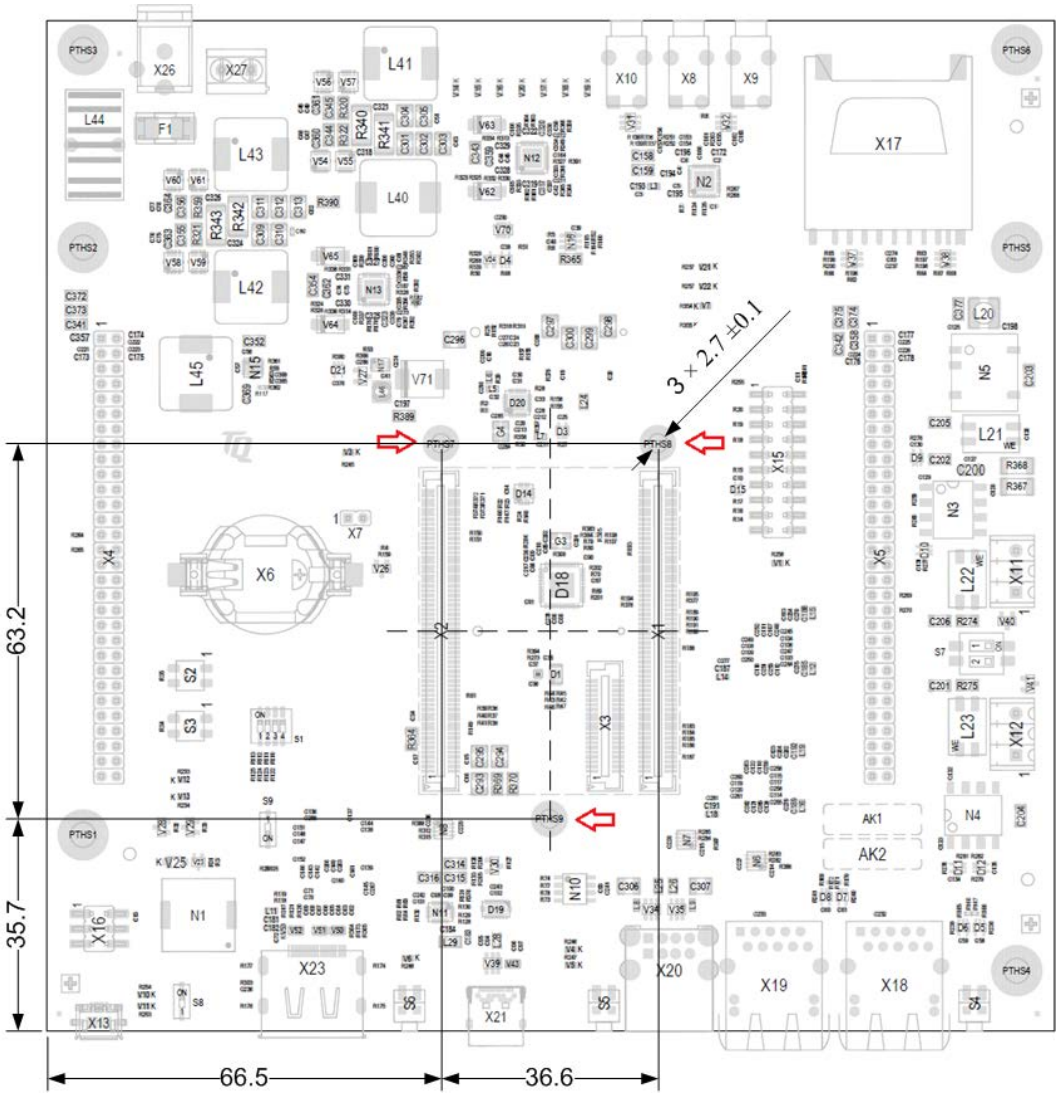


Figure 27: TQMa8Xx heat sink mounting holes

Attention: TQMa8Xx heat dissipation	
	The i.MX 8X CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8Xx must be taken into consideration when connecting the heat sink. The TQMa8Xx is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Xx or the MBa8Xx and thus malfunction, deterioration or destruction.

5.6 Assembly

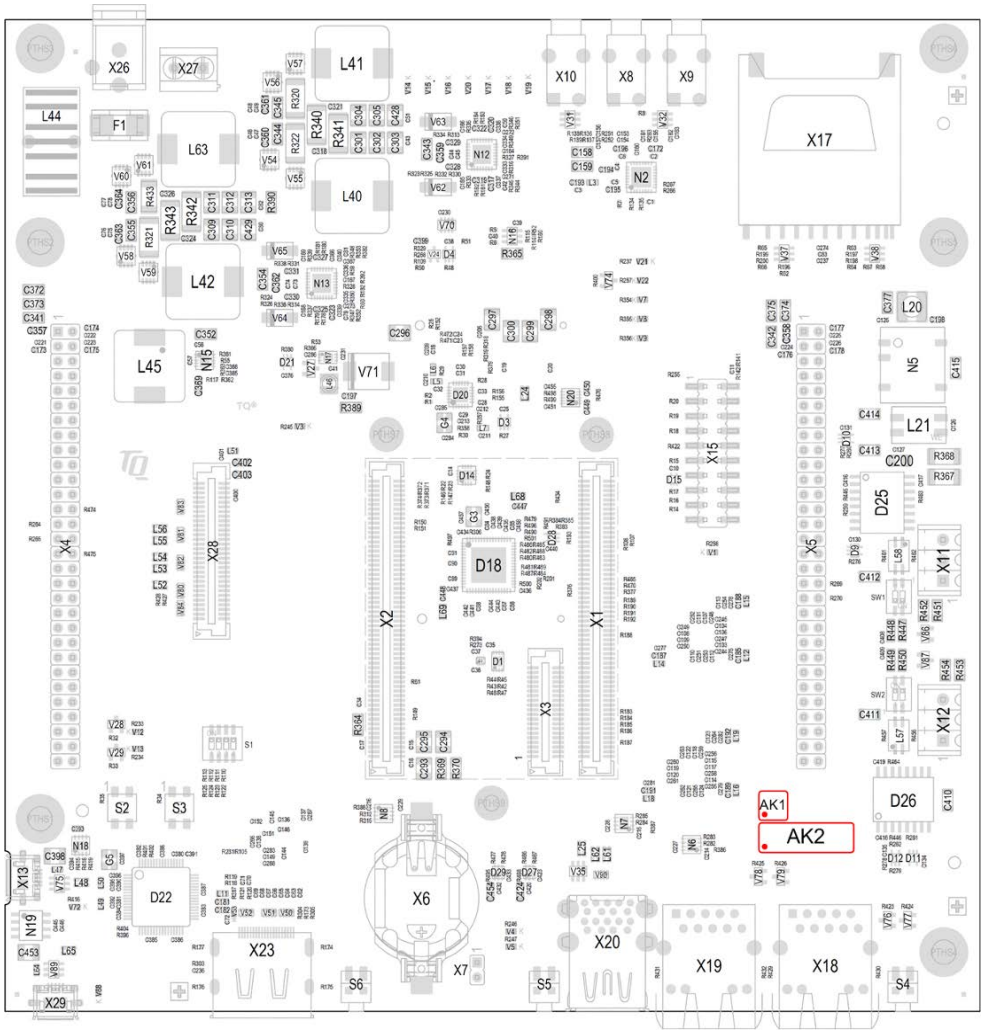


Figure 28: MBa8Xx label position

The labels on the MBa8Xx revision 02xx show the following information:

Table 54: Labels on MBa8Xx

Label	Content
AK1	Serial number
AK2	MBa8Xx version and revision, tests performed

5.7 Position of interfaces

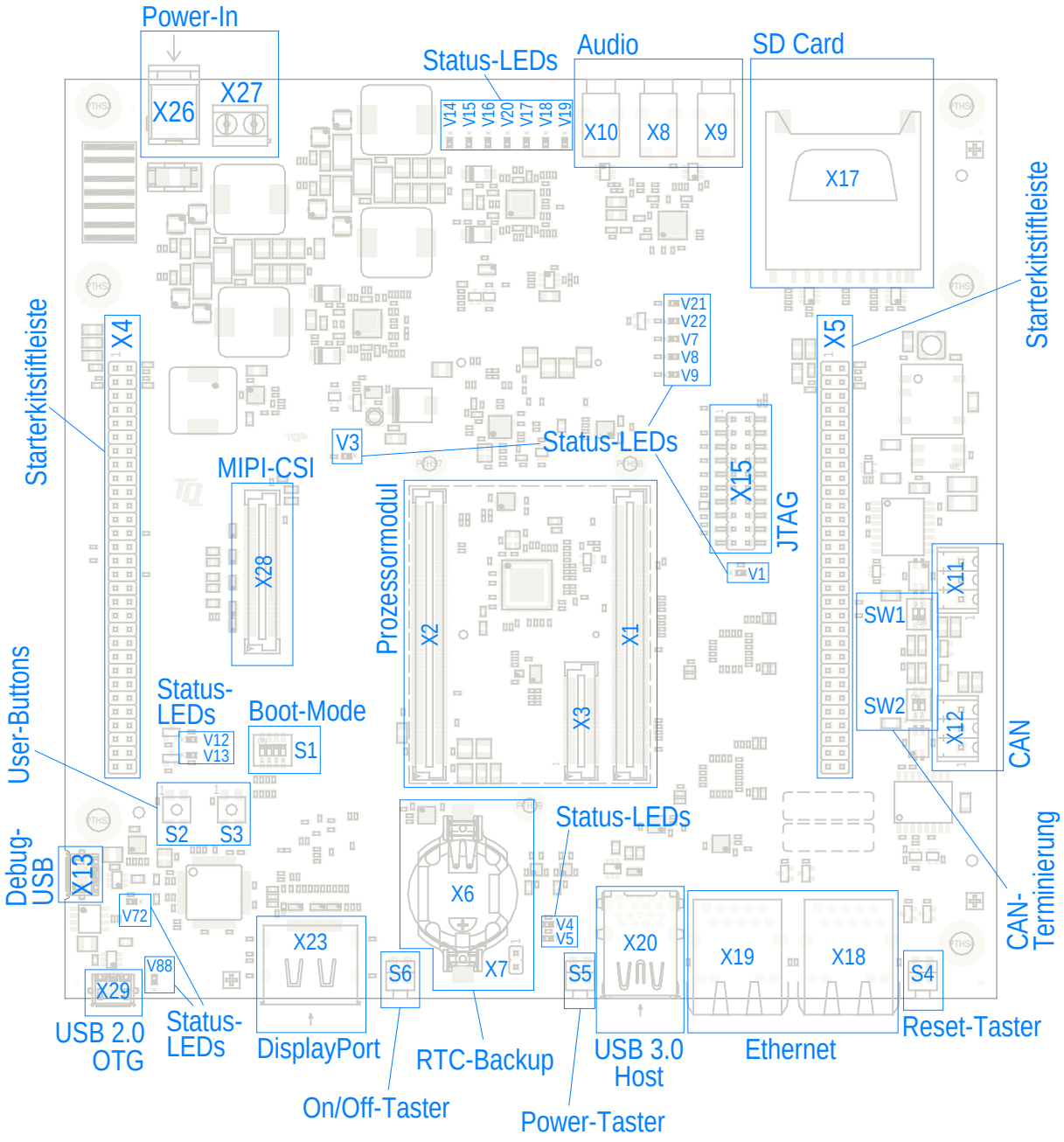


Figure 29: MBa8Xx interfaces top

5.7 Position of interfaces (continued)

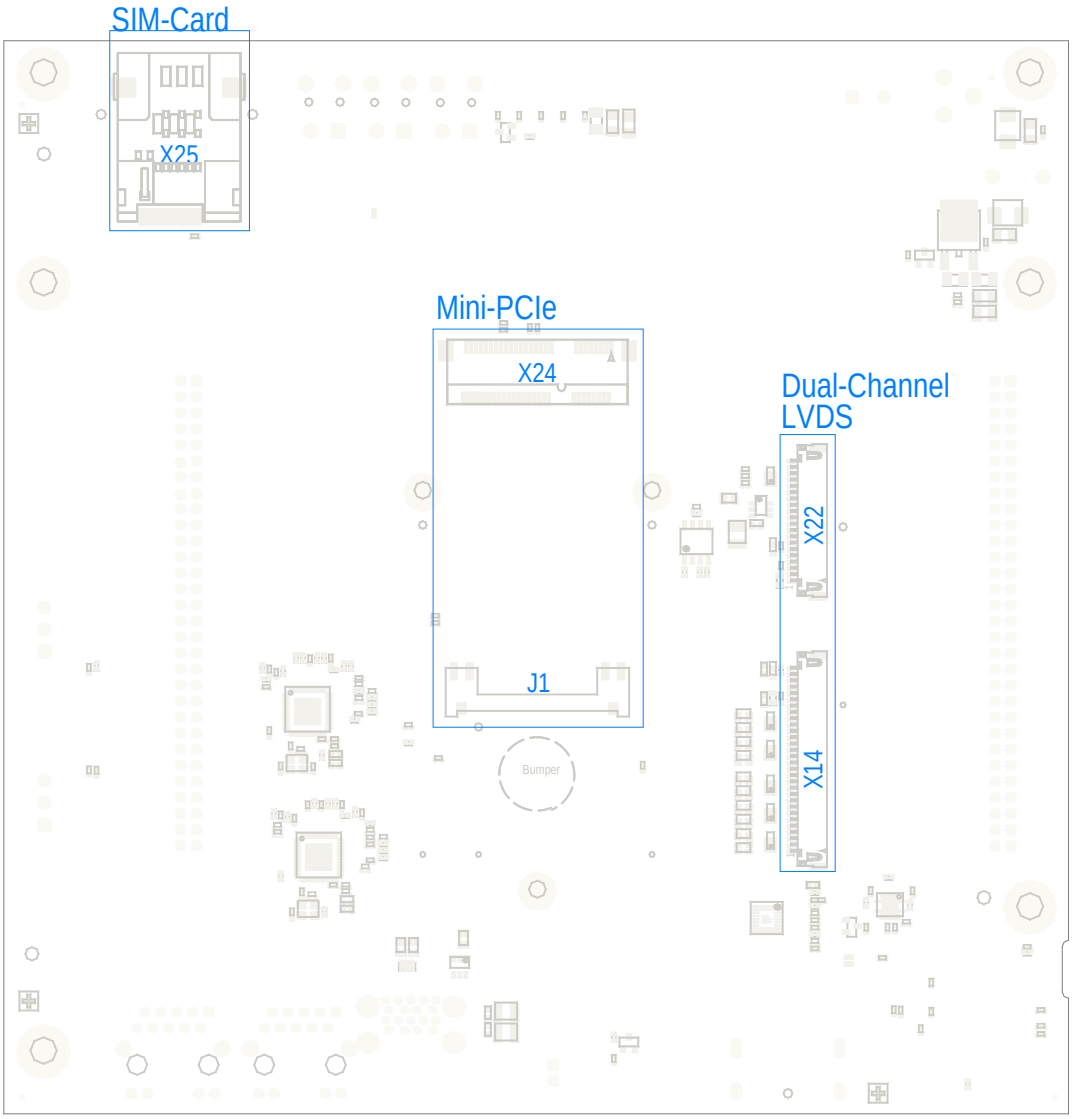


Figure 30: MBa8Xx interfaces bottom

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBa8Xx is a development platform, no EMC tests have been performed.
During the development of the MBa8Xx the standard DIN EN 55022:2010 limit class A was taken into account.

6.2 ESD

ESD protection is provided on most interfaces of the MBa8Xx.
The MBa8Xx schematics show, which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 55: Climatic and operational conditions MBa8Xx

Parameter	Range	Remark
Ambient temperature	–20 °C to +70 °C	With Lithium battery
	–20 °C to +85 °C	Without Lithium battery
Storage temperature	–40 °C to +70 °C	With Lithium battery
	–40 °C to +100 °C	Without Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa8Xx heat dissipation	
	The i.MX 8X CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa8Xx must be taken into consideration when connecting the heat sink. The TQMa8Xx is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Xx and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa8Xx. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa8Xx.
The MBa8Xx is designed to be insensitive to vibration and impact.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa8Xx is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa8Xx was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa8Xx must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa8Xx enable compliance with EuP requirements for the MBa8Xx.

8.5 Packaging

The MBa8Xx is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

For technical reasons a battery is necessary for the MBa8Xx. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa8Xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa8Xx is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 56: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AI	Analog Input
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CLC	Capacitor-Inductor-Capacitor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communication
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
I_{PD}	Input with Pull-Down
I_{PU}	Input with Pull-Up
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures

9.1 Acronyms and definitions (continued)

Table 56: Acronyms (continued)

Acronym	Meaning
NAND	Not-And (flash memory)
(NC)	Not Connected
NOR	Not-Or
NP	Not Placed
O_{OD}	Open-Drain Output
O_{PD}	Output with Pull-Down
O_{PU}	Output with Pull-Up
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media-Independent Interface
SIM	Subscriber Identification Module
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 57: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8DualX Industrial Applications Processors – Data Sheet	15 May 2020	NXP
(2)	i.MX 8DualXPlus / i.MX 8QuadXPlus Applications Processors – Data Sheet	15 May 2020	NXP
(3)	i.MX 8DualXPlus / i.MX 8QuadXPlus Applications Processor – Reference Manual	14 May 2020	NXP
(4)	i.MX 8X – Mask Set Errata	01 May 2020	NXP
(5)	eDP Bridge SN65DSI86 – Data Sheet	October 2020	TI
(6)	Ethernet Transceiver DP83867 – Data Sheet	December 2019	TI
(7)	TQMa8Xx User's Manual	– current –	TQ-Systems
(8)	TQMa8Xx Support Wiki	– current –	TQ-Systems

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