MBa65xx
Preliminary User's Manual

MBa65xx UM 0001
13.07.2022

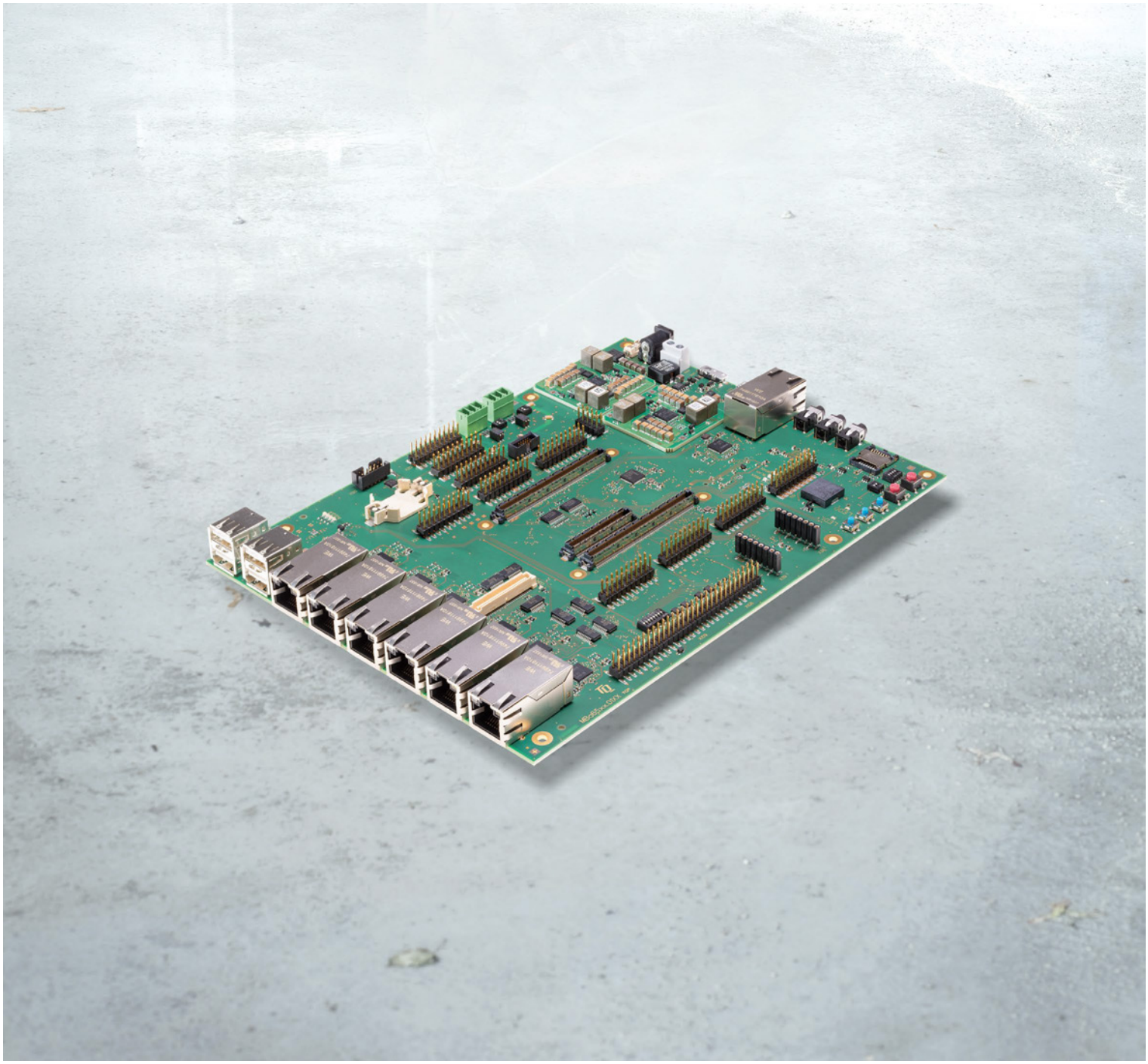

TABLE OF CONTENTS

TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	13.07.2022	Kreuzer		First edition

1. ABOUT THIS MANUAL

1.1 Copyright and license expenses

This Preliminary User's Manual may not be copied, reproduced, translated, changed or distributed, completely or partially in electronic, machine readable, or in any other form without the written consent of TQ-Systems GmbH.

The drivers and utilities for the components used as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Bootloader-licence expenses are paid by TQ-Systems GmbH and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be calculated / declared separately.

1.2 Registered trademarks

TQ-Systems GmbH aims to adhere to copyrights of all graphics and texts used in all publications, and strives to use original or license-free graphics and texts.

All brand names and trademarks mentioned in this Preliminary User's Manual, including those protected by a third party, unless specified otherwise in writing, are subjected to the specifications of the current copyright laws and the proprietary laws of the present registered proprietor without any limitation. One should conclude that brand and trademarks are rightly protected by a third party.

1.3 Disclaimer

TQ-Systems GmbH does not guarantee that the information in this Preliminary User's Manual is up-to-date, correct, complete or of good quality. Nor does TQ-Systems GmbH assume guarantee for further usage of the information. Liability claims against TQ-Systems GmbH, referring to material or non-material related damages caused, due to usage or non-usage of the information given in this Preliminary User's Manual, or due to usage of erroneous or incomplete information, are exempted, as long as there is no proven intentional or negligent fault of TQ-Systems GmbH.

TQ-Systems GmbH explicitly reserves the rights to change or add to the contents of this Preliminary User's Manual or parts of it without special notification.

Important Notice:

Before using the MBa65xx or parts of the MBa65xx schematics, you must evaluate it and determine if it is suitable for your intended application. You assume all risks and liability associated with such use. TQ-Systems GmbH makes no other warranties including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose. Except where prohibited by law, TQ-Systems GmbH will not be liable for any indirect, special, incidental or consequential loss or damage arising from the usage of the MBa65xx or schematics used, regardless of the legal theory asserted.

1.4 Imprint

TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: info@tq-group.com
Web: www.tq-group.com

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa65xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa65xx schematics
- TQMa65xx User's Manual
- AM65xx Data Sheet
- AM65xx Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa65Xx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa65xx as of revision 02xx. The MBa65xx is designed as a carrier board for the TQ-Modules TQMa65xx.

Core of the MBa65xx is the TQMa65xx with a Texas Instruments AM65xx CPU.

The TQMa65xx connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, etc., all other available signals of the TQMa65xx are routed on 100 mil standard pin headers on the MBa65xx.

CPU features and interfaces can be evaluated, software development for a TQMa65xx based project can start immediately.

Currently five Am65xx derivatives are supported:

- AM6526
- AM6527
- AM6528
- AM6546
- AM6548

2.1 MBa65xx block diagram

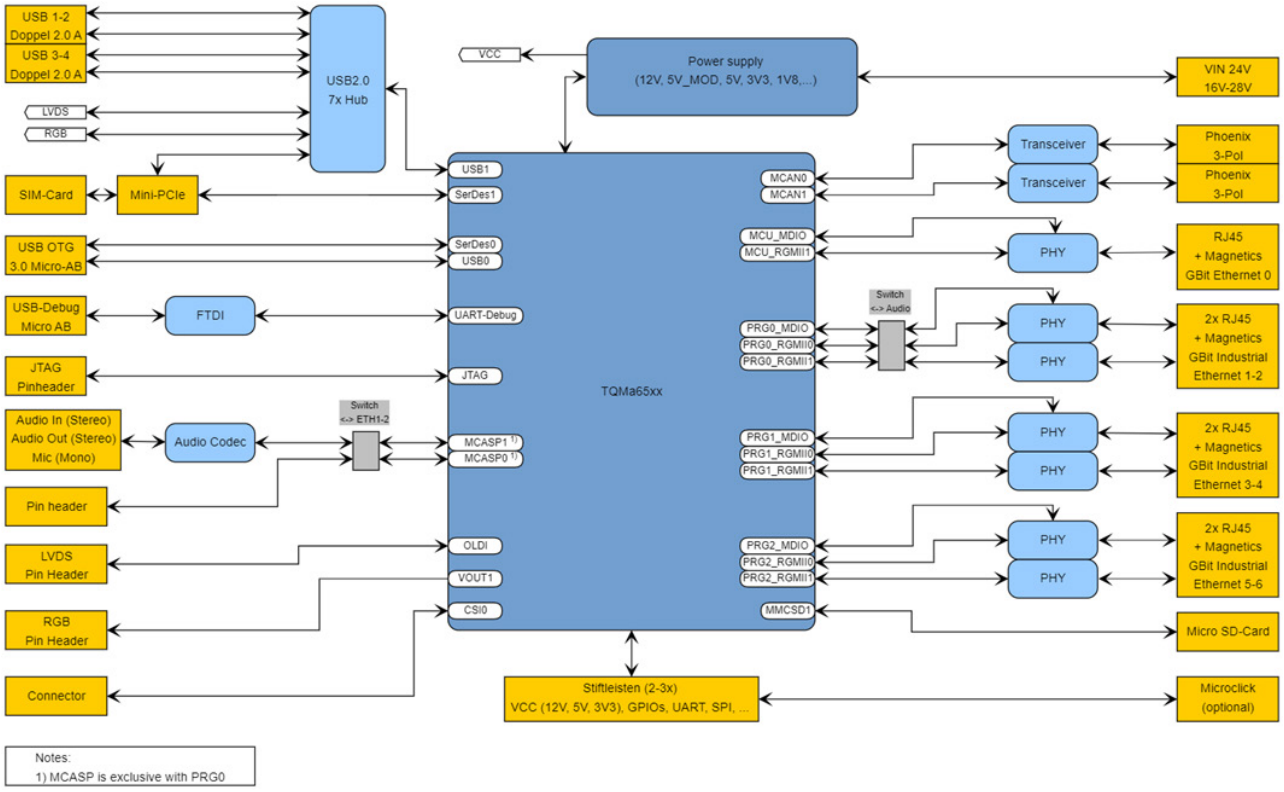

Figure 1: Block diagram MBa65xx

2.2 MBa65xx data interfaces

The following interfaces/functions and user interfaces are available on the MBa65xx:

Table 2: Data interfaces

Interface	Connector	Type
Audio	X18 X17 X16	3.5 mm jack • MIC (mono) • Line-in (stereo) • Line-out (stereo)
CAN	X31 X32	3-pin Phoenix
Coin cell	X42	CR2032 holder
Ethernet, 1000 Base-T	X28	RJ-45, integrated magnetics
Ethernet, 1000 Base-T (TSN and SyncE capable)	X4 X5 X6 X7 X15 X16	RJ-45
Headers	X20 X21 X23 X25 X26 X27 X111	100 mil header • Power-Out (12 V, 5 V, 3.3 V, 1.8V) • 5x I²C • MikroBus • 4x UART • 32+ GPIOs • 16x ADC • JTAG • Secure Element • Programming-/Debugging interfaces • Statussignals
LVDS	X33 X34	DF19 • LCD data • CMD • USB 2.0
Micro SD card	X17	Push-Pull
MIPI CSI-2	X108	100 mil header
Mini PCIe	X29	Mini PCIe socket
	X25	SIM card holder
Power In (24 V±5 %)	X45	DC jack (2.5 mm / 5.5 mm)
	X44	2-pin screw terminal block
PRU-ICSSG	X11	PRG1 wih • 2 real-time capable Gbit Ethernet MACs • 2 synchron clocks • I²C, UART and GPIOs
RGB display (24 bit RGB with touch controller)	X108 X109 X110	100 mil header
USB 2.0 Hi-Speed Host	X34	DF19
USB 2.0 Hi-Speed Host	X109	100 mil header
USB 2.0 Hi-Speed Host	X29	Mini PCIe
USB 2.0 Hi-Speed Host (4 x)	X113 X114	USB, Micro A stacked
USB 3.0 SS OTG	X115	USB, Micro AB
USB debug	X37	USB, Micro B

2.3 MBa65xx diagnostic and user interfaces

The MBa65xx provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	4 × Green LED	Power Good 5V, 3.3V, 1.8V, 12V
	4 × Red LED	Power Fault 5V, 3.3V, 1.8V, 12V
	2 × Red LED	Cold Reset, Warm Reset
	8 × Green LED	5x VBUS USB2.0 1x VBUS USB3.0
	3 × Green LED	Mini PCIe: WWAN, WLAN, WPAN
	2 × Blue LED	Software controlled LEDs
	3 × Blue LED	MCASP/ PRG0/PRG1 interface activ
	7 x Green / Yellow / Orange LED	Ethernet-LEDs (Activity / Speed / Error)
Power / Reset button	2 × Push button	Power Reset, CPU-/PMIC-Reset
Navigation button	3 × Push button	GPIO push button at port expander
Boot Mode configuration	29 x DIP switch / Pin straps	Boot Mode configuration DIP switch for easier boot source selection
CAN- / RS485 termination	4 x DIP switch	–
Buzzer	1 x	–
JTAG	1 × 20-pin, 100 mil header	–
Interface and debug switch	6 x DIP switch	–

3. ELECTRONICS

The following chapters describe the interfaces of the MBa65xx as of revision 02xx in connection with a TQMa65xx with maximum configuration.

In any case the TQMa65xx User's Manual must be complied with.

3.1 TQMa65xx

The TQMa65xx is the central system on the MBa65xx. It provides DDR4 RAM (TQMa65xx), eMMC, NOR flash, RTC, an EEPROM, power supply and power management functionality.

On the MBa65xx the standard interfaces like USB, Ethernet, etc., provided by the TQMa65xx are routed to industry standard connectors. All other signals and buses provided by the TQMa65xx are routed to 100 mil headers.

The boot behaviour of the TQMa65xx can be configured.

The Boot Mode configuration is set by a DIP switch on the MBa65xx, see chapter 3.2.

Furthermore the MBa65xx provides all power supplies and configurations required for the operation of the TQMa65xx.

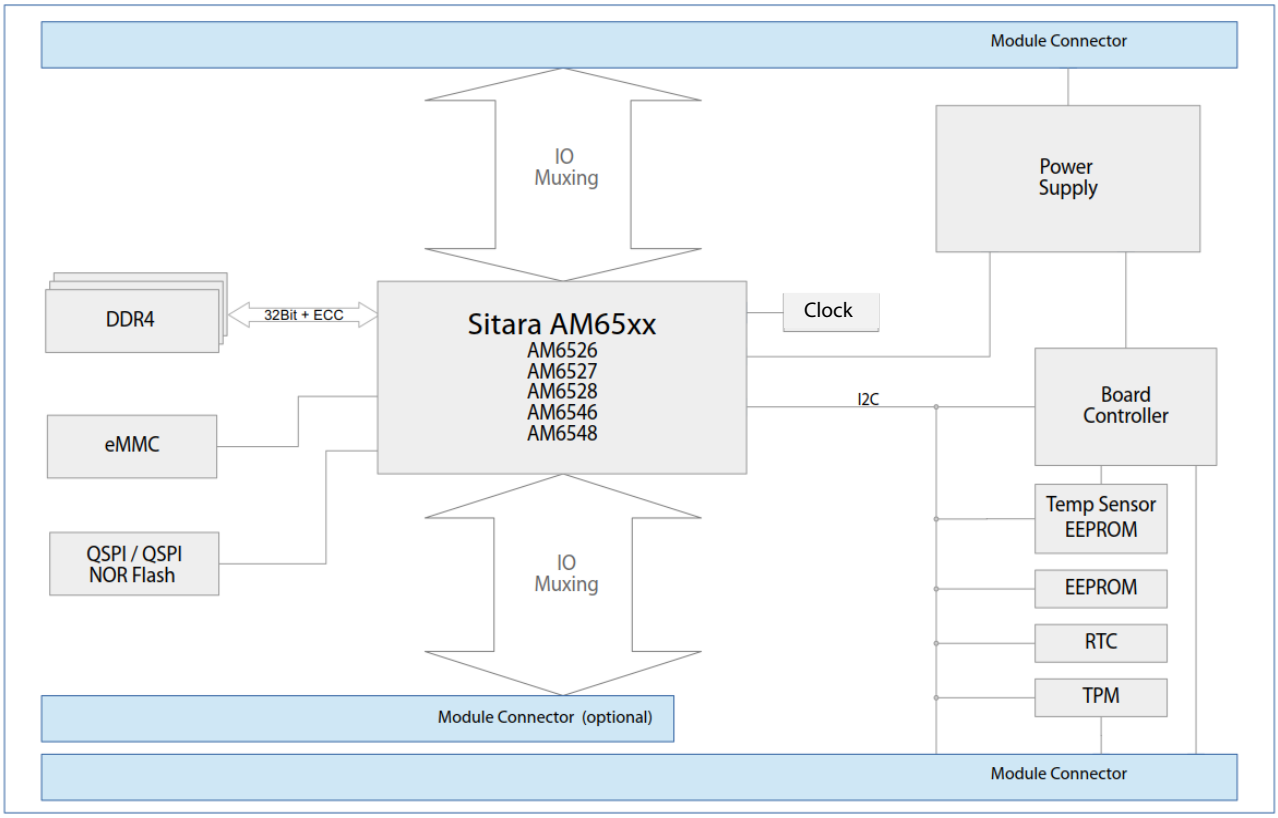

Figure 2: Block diagram TQMa65xx

3.1.1 TQMa65xx connectors on MBa65xx

The TQMa65xx is connected to the MBa65xx with 560 pins on three connectors.
The following table shows details of the connectors assembled on the MBa65xx:

Table 4: Connectors assembled on MBa65xx

Manufacturer	Pin count / part number	Qty.	Remark
EPT	220-pin / 401-51101-51	2	SMD220
	120-pin / 401-51401-51	1	SMD120

The TQMa65xx is held in the mating connectors on the MBa65xx by 560 pins. To avoid damaging the connectors of the MBa65xx or the TQMa65xx while removing the TQMa65xx, the use of an extraction tool is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa65xx for the extraction tool.

The pins assignment listed in Table 5 to Table 7 refer to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in Table 5 to Table 7 refer to the AM65xx documentation, see Table 56.

3.1.2 TQMa65xx pinout

All available TQMa65xx signals are available at three connectors on the MBa65xx. When using the processor signals, it is essential to observe the multiple assignment of the pins by different processor-internal function units (multiplexing).
The direction of the signals in Table 5 to Table 7 is shown from the perspective of the TQMa65xx.
Further information like pull-ups or pull-downs on the TQMa65xx can be taken from the TQMa65xx User's Manual (7).

Note: Available interfaces	
	Depending on the TQMa65xx derivative not all interfaces are available. More information about available interfaces can be found in the TQMa65xx User's Manual.

3.1.2 TQMa65xx pinout (continued)

Table 5: Pinout TQMa65xx connector X1

Dir.	Level	Group	Signal	Module pin		Signal	Group	Level	Dir.
P	0 V	Ground	VCC5V_IN	A1	B1	DGND	Ground	0 V	P
P	5V	Power	VIN	A2	B2	VIN	Power	5V	P
P	5V	Power	VIN	A3	B3	VIN	Power	5V	P
P	5V	Power	VIN	A4	B4	VIN	Power	5V	P
P	5V	Power	VIN	A5	B5	VIN	Power	5V	P
P	5V	Power	VIN	A6	B6	VIN	Power	5V	P
P	5V	Power	VIN	A7	B7	VIN	Power	5V	P
P	5V	Power	VIN	A8	B8	VIN	Power	5V	P
P	5V	Power	VIN	A9	B9	VIN	Power	5V	P
P	0 V	Ground	DGND	A10	B10	VIN	Power	5V	P
P	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A12	B12	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A13	B13	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A14	B14	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A15	B15	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A16	B16	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A17	B17	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A18	B18	VDD_SD	Power	3.3 V	P
P	0 V	Ground	DGND	A19	B19	VBAT	Power	3.3 V	P
P	1.8 V	Power	VCC1V8L1	A20	B20	VCC3V3S	Power	1.8 V/3.3 V	P
P	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	P
P	1.8 V	Power	VCC1V8	A22	B22	VCC3V3	Power	3.3 V	P
P	1.8 V	Power	VCC1V8	A23	B23	VCC3V3	Power	3.3 V	P
P	0 V	Ground	DGND	A24	B24	DGND	Ground	0 V	P
I	3.3 V	JTAG	nSRST_JTAG#	A25	B25	IO1_RES	Factory Test	3.3 V	I/O
I	1.8 V	SYSTEM	POR#_MB	A26	B26	IO2_RES	Factory Test	3.3 V	I/O
O	1.8 V/3.3 V	SYSTEM	POR#_OUT	A27	B27	IO3_RES	Factory Test	3.3 V	I/O
P	0 V	Ground	DGND	A28	B28	RES_BC#	Factory Test	3.3 V	I
I	1.8 V	SERDES	SERDES1_RXP	A29	B29	SWD_CLK	Factory Test	3.3 V	I
I	1.8 V	SERDES	SERDES1_RXN	A30	B30	SWD_DIO	Factory Test	3.3 V	I/O
P	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	P
O	1.8 V	SERDES	SERDES1_TXN_C	A32	B32	DGND	Ground	0 V	P
O	1.8 V	SERDES	SERDES1_TXP_C	A33	B33	SERDES0_PCIe_REFCLK0P	SERDES	1.8 V	O
P	0 V	Ground	DGND	A34	B34	SERDES0_PCIe_REFCLK0N	SERDES	1.8 V	O
O	1.8 V	SERDES	SERDES1_PCIe_REFCLK1P	A35	B35	DGND	Ground	0 V	P
O	1.8 V	SERDES	SERDES1_PCIe_REFCLK1N	A36	B36	SERDES0_RXN	SERDES	1.8 V	I
P	0 V	Ground	DGND	A37	B37	SERDES0_RXP	SERDES	1.8 V	I
O	1.8 V	SERDES	SERDES1_REFCLKP	A38	B38	DGND	Ground	0 V	P
O	1.8 V	SERDES	SERDES1_REFCLKN	A39	B39	SERDES0_TXP_C	SERDES	1.8 V	O
P	0 V	Ground	DGND	A40	B40	SERDES0_TXN_C	SERDES	1.8 V	O
P	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	SPI0_D1	A42	B42	SERDES0_REFCLKP	SERDES	1.8 V	O

I/O	1.8 V/3.3 V	SPI	SPI0_D0	A43	B43	SERDES0_REFCLKN	SERDES	1.8 V	O
P	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	SPI1_CS1	A45	B45	UART0_CTS#	UART	1.8 V/3.3 V	I
I/O	1.8 V/3.3 V	SPI	SPI1_CS0	A46	B46	UART0_RXD	UART	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A47	B47	UART0_TXD	UART	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	SPI	SPI0_CLK	A48	B48	UART0_RST#	UART	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A49	B49	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	SPI1_CLK	A50	B50	USB0_VBUS_R	USB	VDDA_3P3_USB	
P	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	SPI0_CS0	A52	B52	USB0_ID	USB	3.3 V	
I/O	1.8 V/3.3 V	SPI	SPI0_CS1	A53	B53	USB0_DRVVBUS	USB	1.8 V/3.3 V	
P	0 V	Ground	DGND	A54	B54	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	SPI1_D0	A55	B55	USB0_DM	USB	3.3 V	
I/O	1.8 V/3.3 V	SPI	SPI1_D1	A56	B56	USB0_DP	USB	3.3 V	
P	0 V	Ground	DGND	A57	B57	DGND	Ground	0 V	P
O	1.8 V/3.3 V	CAN	MCU_MCAN1_TX_AC3	A58	B58	USB1_VBUS_R	USB	VDDA_3P3_USB	
I	1.8 V/3.3 V	CAN	MCU_MCAN1_RX_AD3	A59	B59	USB1_ID	USB	3.3 V	
P	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A61	B61	USB1_DRVVBUS	USB	1.8 V/3.3 V	
I	1.8 V/3.3 V	CAN	MCU_MCAN0_RX	A62	B62	DGND	Ground	0 V	P
O	1.8 V/3.3 V	CAN	MCU_MCAN0_TX	A63	B63	USB1_DP	USB	3.3 V	
P	0 V	Ground	DGND	A64	B64	USB1_DM	USB	3.3 V	
I/O/D	1.8 V/3.3 V	I2C	WKUP_I2C_SDA	A65	B65	DGND	Ground	0 V	P
I/O/D	1.8 V/3.3 V	I2C	WKUP_I2C_SCL	A66	B66	WKUP_GPIO0_11	GPIO	1.8 V/3.3 V	
P	0 V	Ground	DGND	A67	B67	WKUP_GPIO0_10	GPIO	1.8 V/3.3 V	
I/O/D	1.8 V/3.3 V	I2C	MCU_I2C0_SDA	A68	B68	WKUP_GPIO0_9	GPIO	1.8 V/3.3 V	
I/O/D	1.8 V/3.3 V	I2C	MCU_I2C0_SCL	A69	B69	WKUP_GPIO0_8	GPIO	1.8 V/3.3 V	
P	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	P
O	1.8 V/3.3 V	UART	WKUP_UART0_RTSn_AC1	A71	B71	WKUP_GPIO0_3	GPIO	1.8 V/3.3 V	
I	1.8 V/3.3 V	UART	WKUP_UART0_CTSn_AC2	A72	B72	WKUP_GPIO0_2	GPIO	1.8 V/3.3 V	
O	1.8 V/3.3 V	UART	WKUP_UART0_TXD	A73	B73	WKUP_GPIO0_1	GPIO	1.8 V/3.3 V	
I	1.8 V/3.3 V	UART	WKUP_UART0_RXD	A74	B74	WKUP_GPIO0_0	GPIO	1.8 V/3.3 V	
P	0 V	Ground	DGND	A75	B75	WKUP_GPIO0_33_N3	GPIO	1.8 V/3.3 V	
I/O	1.8 V/3.3 V	SPI	MCU_SPI0_D1	A76	B76	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	MCU_SPI0_D0	A77	B77	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	MCU_SPI0_CS0	A78	B78	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	SPI	MCU_SPI0_CLK	A79	B79	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	WKUP_GPIO0_32_N2	A81	B81	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	WKUP_GPIO0_31_P1	A82	B82	MCU_POR#_OUT	SYSTEM	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	WKUP_GPIO0_28_P3	A83	B83	MCU_WARM_RESET#_OUT	SYSTEM	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	WKUP_GPIO0_27_P2	A84	B84	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	WKUP_GPIO0_26_R1	A85	B85	MCU_RESET#_MB	SYSTEM	1.8 V/3.3 V	I
I/O	1.8 V/3.3 V	GPIO	WKUP_GPIO0_25_T1	A86	B86	MCU_SAFETY_ERROR#	SYSTEM	1.8 V/3.3 V	I/O
P	0 V	Ground	DGND	A87	B87	DGND	Ground	0 V	P

O	1.8 V	SYSTEM	WARM_RESET#_OUT	A88	B88	MCU_UART0_TXD_P5	UART	1.8 V/3.3 V	O
I	1.8 V/3.3 V	SYSTEM	WARM_RESET#_MB	A89	B89	MCU_UART0_RXD_P4	UART	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	RGMII	MCU_RGMII1_TXC	A91	B91	MCU_RGMII1_RXC	RGMII	1.8 V/3.3 V	I
O	1.8 V/3.3 V	RGMII	MCU_RGMII1_TX_CTL	A92	B92	MCU_RGMII1_RX_CTL	RGMII	1.8 V/3.3 V	I
O	1.8 V/3.3 V	RGMII	MCU_RGMII1_TD3	A93	B93	MCU_RGMII1_RD0	RGMII	1.8 V/3.3 V	I
O	1.8 V/3.3 V	RGMII	MCU_RGMII1_TD2	A94	B94	MCU_RGMII1_RD1	RGMII	1.8 V/3.3 V	I
O	1.8 V/3.3 V	RGMII	MCU_RGMII1_TD1	A95	B95	MCU_RGMII1_RD2	RGMII	1.8 V/3.3 V	I
O	1.8 V/3.3 V	RGMII	MCU_RGMII1_TD0	A96	B96	MCU_RGMII1_RD3	RGMII	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A97	B97	DGND	Ground	0 V	P
O	1.8 V/3.3 V	RGMII	MCU_RGMII1_MDC	A98	B98	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	RGMII	MCU_RGMII1_MDIO	A99	B99	SOC_SAFETY_ERROR#	SYSTEM	1.8 V	I/O
P	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A101	B101	DGND	Ground	0 V	P
A	1.8 V	ADC	MCU_ADC1_AIN7	A102	B102	MCU_ADC0_AIN7	ADC	1.8 V	A
A	1.8 V	ADC	MCU_ADC1_AIN6	A103	B103	MCU_ADC0_AIN6	ADC	1.8 V	A
A	1.8 V	ADC	MCU_ADC1_AIN5	A104	B104	MCU_ADC0_AIN5	ADC	1.8 V	A
A	1.8 V	ADC	MCU_ADC1_AIN4	A105	B105	MCU_ADC0_AIN4	ADC	1.8 V	A
A	1.8 V	ADC	MCU_ADC1_AIN3	A106	B106	MCU_ADC0_AIN3	ADC	1.8 V	A
A	1.8 V	ADC	MCU_ADC1_AIN2	A107	B107	MCU_ADC0_AIN2	ADC	1.8 V	A
A	1.8 V	ADC	MCU_ADC1_AIN1	A108	B108	MCU_ADC0_AIN1	ADC	1.8 V	A
A	1.8 V	ADC	MCU_ADC1_AIN0	A109	B109	MCU_ADC0_AIN0	ADC	1.8 V	A
P	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	P

3.1.2 TQMa65xx pinout (continued)

Table 6: Pinout TQMa65xx connector X2

Dir.	Level	Group	Signal	Module pin		Signal	Group	Level	Dir.
P	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	P
O	1.8 V/3.3 V	RGMII	PRG2_RGMII1_TD3 _AE16	A2	B2	PRG2_RGMII2_TD3 _AD14	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG2_RGMII1_TD2 _AF16	A3	B3	PRG2_RGMII2_TD2 _AC15	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG2_RGMII1_TD1 _AG16	A4	B4	PRG2_RGMII2_TD1 _AF14	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG2_RGMII1_TD0 _AH16	A5	B5	PRG2_RGMII2_TD0 _AD15	RGMII	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A6	B6	DGND	Ground	0 V	P
I	1.8 V/3.3 V	RGMII	PRG2_RGMII1_RD3 _AG18	A7	B7	PRG2_RGMII2_RD3 _AH14	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG2_RGMII1_RD2 _AH17	A8	B8	PRG2_RGMII2_RD2 _AD17	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG2_RGMII1_RD1 _AE18	A9	B9	PRG2_RGMII2_RD1 _AC16	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG2_RGMII1_RD0 _AF18	A10	B10	PRG2_RGMII2_RD0 _AH15	RGMII	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	P
I	1.8 V/3.3 V	RGMII	PRG2_RGMII1_RX_ CTL_AG17	A12	B12	PRG2_RGMII2_RX_ CTL_AG14	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG2_RGMII1_RXC _AF17	A13	B13	PRG2_RGMII2_RXC _AG15	RGMII	1.8 V/3.3 V	I
I/O	1.8 V/3.3 V	RGMII	PRG2_RGMII1_TXC _AD16	A14	B14	PRG2_RGMII2_TXC _AE14	RGMII	1.8 V/3.3 V	I/O
O	1.8 V/3.3 V	RGMII	PRG2_RGMII1_TX_ CTL_AE17	A15	B15	PRG2_RGMII2_TX_ CTL_AC17	RGMII	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A16	B16	DGND	Ground	0 V	P
O	1.8 V/3.3 V	RGMII	PRG1_RGMII2_TD3 _AG19	A17	B17	PRG1_RGMII1_TD3 _AD19	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG1_RGMII2_TD2 _AH19	A18	B18	PRG1_RGMII1_TD2 _AG20	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG1_RGMII2_TD1 _AF19	A19	B19	PRG1_RGMII1_TD1 _AH21	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG1_RGMII2_TD0 _AE20	A20	B20	PRG1_RGMII1_TD0 _AH20	RGMII	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	P
I	1.8 V/3.3 V	RGMII	PRG1_RGMII2_RD3 _AH22	A22	B22	PRG1_RGMII1_RD3 _AD21	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG1_RGMII2_RD2 _AG21	A23	B23	PRG1_RGMII1_RD2 _AF23	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG1_RGMII2_RD1 _AH23	A24	B24	PRG1_RGMII1_RD1 _AG24	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG1_RGMII2_RD0 _AH24	A25	B25	PRG1_RGMII1_RD0 _AE22	RGMII	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A26	B26	DGND	Ground	0 V	P
I	1.8 V/3.3 V	RGMII	PRG1_RGMII2_RX_ CTL_AE21	A27	B27	PRG1_RGMII1_RX_ CTL_AG23	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG1_RGMII2_RXC _AG22	A28	B28	PRG1_RGMII1_RXC _AF22	RGMII	1.8 V/3.3 V	I
I/O	1.8 V/3.3 V	RGMII	PRG1_RGMII2_TXC _AE19	A29	B29	PRG1_RGMII1_TXC _AD20	RGMII	1.8 V/3.3 V	I/O
O	1.8 V/3.3 V	RGMII	PRG1_RGMII2_TX_ CTL_AC20	A30	B30	PRG1_RGMII1_TX_ CTL_AF21	RGMII	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	P

O	1.8 V/3.3 V	RGMII	PRG0_RGMII2_TD3_AE27	A32	B32	PRG0_RGMII1_TD3_AA24	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG0_RGMII2_TD2_AD24	A33	B33	PRG0_RGMII1_TD2_AD26	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG0_RGMII2_TD1_AD25	A34	B34	PRG0_RGMII1_TD1_AC26	RGMII	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG0_RGMII2_TD0_AC25	A35	B35	PRG0_RGMII1_TD0_AD27	RGMII	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A36	B36	DGND	Ground	0 V	P
I	1.8 V/3.3 V	RGMII	PRG0_RGMII2_RD3_AB26	A37	B37	PRG0_RGMII1_RD3_AA27	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG0_RGMII2_RD2_AC27	A38	B38	PRG0_RGMII1_RD2_W24	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG0_RGMII2_RD1_AC28	A39	B39	PRG0_RGMII1_RD1_W25	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG0_RGMII2_RD0_AB28	A40	B40	PRG0_RGMII1_RD0_V24	RGMII	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	P
I	1.8 V/3.3 V	RGMII	PRG0_RGMII2_RX_CTL_AA25	A42	B42	PRG0_RGMII1_RX_CTL_Y24	RGMII	1.8 V/3.3 V	I
I	1.8 V/3.3 V	RGMII	PRG0_RGMII2_RXC_AB27	A43	B43	PRG0_RGMII1_RXC_Y25	RGMII	1.8 V/3.3 V	I
I/O	1.8 V/3.3 V	RGMII	PRG0_RGMII2_TXC_AC24	A44	B44	PRG0_RGMII1_TXC_AD28	RGMII	1.8 V/3.3 V	I/O
O	1.8 V/3.3 V	RGMII	PRG0_RGMII2_TX_CTL_AB24	A45	B45	PRG0_RGMII1_TX_CTL_AB25	RGMII	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A46	B46	DGND	Ground	0 V	P
O	1.8 V/3.3 V	RGMII	PRG1_MDIO0_MDC_AH18	A47	B47	GPIO1_37_V27	GPIO	1.8 V/3.3 V	I/O
I/O	1.8 V/3.3 V	RGMII	PRG1_MDIO0_MDIO_AD18	A48	B48	PRG0_PRU0_GPO5_V28	GPIO	1.8 V/3.3 V	I/O
P	0 V	Ground	DGND	A49	B49	VOUT_DE_T23	GPMC	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG2_MDIO0_MDC_AE15	A50	B50	VOUT_PCLK_R24	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	RGMII	PRG2_MDIO0_MDIO_AC19	A52	B52	VOUT_HSYNC_T24	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A53	B53	VOUT_VSYNC_T25	GPMC	1.8 V/3.3 V	O
O	1.8 V/3.3 V	RGMII	PRG0_MDIO0_MDC_AE28	A54	B54	VOUT_DATA23_R23	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	RGMII	PRG0_MDIO0_MDIO_AE26	A55	B55	VOUT_DATA22_R26	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A56	B56	VOUT_DATA21_P23	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	RGMII	PRG1_PRU0_GPO5_AF27	A57	B57	VOUT_DATA20_T28	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_64_AF28	A58	B58	VOUT_DATA19_U28	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_74_AG25	A59	B59	VOUT_DATA18_P26	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	GPIO0_73_AH26	A61	B61	VOUT_DATA17_P25	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_66_AH25	A62	B62	VOUT_DATA16_R28	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_75_AG26	A63	B63	VOUT_DATA15_R27	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_63_AG27	A64	B64	VOUT_DATA14_P24	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_85_AF25	A65	B65	VOUT_DATA13_N25	GPMC	1.8 V/3.3 V	O

I/O	1.8 V/3.3 V	GPIO	GPIO0_65_AF26	A66	B66	VOUT_DATA12_N26	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_86_AF24	A67	B67	VOUT_DATA11_P27	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_84_AE24	A68	B68	VOUT_DATA10_P28	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_93_AE23	A69	B69	VOUT_DATA9_M26	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	GPIO0_94_AD22	A71	B71	VOUT_DATA8_N23	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_83_AD23	A72	B72	VOUT_DATA7_M25	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO0_95_AC21	A73	B73	VOUT_DATA6_N28	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A74	B74	VOUT_DATA5_N27	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A75	B75	VOUT_DATA4_N24	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO1_67_Y26	A76	B76	VOUT_DATA3_M24	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO1_59_AA28	A77	B77	VOUT_DATA2_M28	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO1_66_Y27	A78	B78	VOUT_DATA1_M23	GPMC	1.8 V/3.3 V	O
I/O	1.8 V/3.3 V	GPIO	GPIO1_58_Y28	A79	B79	VOUT_DATA0_M27	GPMC	1.8 V/3.3 V	O
P	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	GPIO1_68_W26	A81	B81	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	GPIO1_56_W28	A82	B82	I2C2_SCL_T27	I2C	1.8 V/3.3 V	I/O/D
I/O	1.8 V/3.3 V	GPIO	GPIO1_57_W27	A83	B83	I2C2_SDA_R25	I2C	1.8 V/3.3 V	I/O/D
I/O	1.8 V/3.3 V	GPIO	GPIO1_38_V26	A84	B84	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	GPIO1_36_U27	A85	B85	OLDI0_A0P	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	GPIO	GPIO1_47_V25	A86	B86	OLDI0_A0N	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	GPIO	GPIO1_46_U26	A87	B87	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	GPIO1_39_U25	A88	B88	OLDI0_A1P	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	GPIO	GPIO1_48_U24	A89	B89	OLDI0_A1N	LCD	1.8 V	I/O
P	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	PRG0_PRU1_GPO5_U23	A91	B91	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	GPIO	PRG1_PRU1_GPO5_AC22	A92	B92	OLDI0_A2P	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	GPIO	GPIO1_13_A23	A93	B93	OLDI0_A2N	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	GPIO	GPIO1_14_B23	A94	B94	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A95	B95	OLDI0_A3P	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	MMC/SD	SD_DAT0	A96	B96	OLDI0_A3N	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	MMC/SD	SD_DAT1	A97	B97	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	MMC/SD	SD_DAT2	A98	B98	OLDI0_CLKN	LCD	1.8 V	I/O
I/O	1.8 V/3.3 V	MMC/SD	SD_DAT3	A99	B99	OLDI0_CLKP	LCD	1.8 V	I/O
P	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	MMC/SD	SD_CMD	A101	B101	NMI#	SYSTEM	1.8 V/3.3 V	I
I	1.8 V/3.3 V	MMC/SD	SD_SDWP	A102	B102	ECAP0_IN_APWM_OUT	PWM	1.8 V/3.3 V	I/O
I	1.8 V/3.3 V	MMC/SD	SD_SDCD	A103	B103	TIMER_IO1	TIMER	1.8 V/3.3 V	I/O
O	1.8 V/3.3 V	MMC/SD	SD_CLK_R	A104	B104	TIMER_IO0	TIMER	1.8 V/3.3 V	I/O
P	0 V	Ground	DGND	A105	B105	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A106	B106	I2C0_SDA	I2C	1.8 V/3.3 V	I/O/D
I	1.8 V/3.3 V	SYSTEM	EXT_REFCLK1	A107	B107	I2C0_SCL	I2C	1.8 V/3.3 V	I/O/D
P	0 V	Ground	DGND	A108	B108	I2C1_SDA	I2C	1.8 V/3.3 V	I/O/D
O	1.8 V	SYSTEM	OSC1	A109	B109	I2C1_SCL	I2C	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	P

3.1.2 TQMa65xx pinout (continued)

Table 7: Pinout TQMa65xx connector X3

Dir.	Level	Group	Signal	Module pin		Signal	Group	Level	Dir.
P	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	P
O	1.8 V/3.3 V	XSPI	XSPI_CLK_X3	A2	B2	NC	NC	-	-
P	0 V	Ground	DGND	A3	B3	NC	NC	-	-
O	1.8 V/3.3 V	XSPI	XSPI_CS0_X3	A4	B4	NC	NC	-	-
I	1.8 V/3.3 V	XSPI	XSPI_DQS_X3	A5	B5	NC	NC	-	-
P	0 V	Ground	DGND	A6	B6	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ0_X3	A7	B7	NC	NC	-	-
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ1_X3	A8	B8	NC	NC	-	-
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ2_X3	A9	B9	NC	NC	-	-
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ3_X3	A10	B10	NC	NC	-	-
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ4_X3	A11	B11	NC	NC	-	-
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ5_X3	A12	B12	NC	NC	-	-
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ6_X3	A13	B13	NC	NC	-	-
I/O	1.8 V/3.3 V	XSPI	XSPI_DQ7_X3	A14	B14	NC	NC	-	-
O	1.8 V/3.3 V	XSPI	XSPI_CS1_X3	A15	B15	NC	NC	-	-
P	0 V	Ground	DGND	A16	B16	DGND	Ground	0 V	P
O	1.8 V/3.3 V	XSPI	XSPI_LBCLKO_X3	A17	B17	JTAG_EMU1	JTAG	1.8 V/3.3 V	I/O
P	0 V	Ground	DGND	A18	B18	JTAG_EMU0	JTAG	1.8 V/3.3 V	I/O
-	-	NC	NC	A19	B19	JTAG_TRST#	JTAG	1.8 V/3.3 V	I
-	-	NC	NC	A20	B20	DGND	Ground	0 V	P
-	-	NC	NC	A21	B21	JTAG_TCK	JTAG	1.8 V/3.3 V	I
-	-	NC	NC	A22	B22	DGND	Ground	0 V	P
-	-	NC	NC	A23	B23	JTAG_TDO	JTAG	1.8 V/3.3 V	O/Z
-	-	NC	NC	A24	B24	JTAG_TMS	JTAG	1.8 V/3.3 V	I
-	-	NC	NC	A25	B25	JTAG_TDI	JTAG	1.8 V/3.3 V	I
P	0 V	Ground	DGND	A26	B26	DGND	Ground	0 V	P
-	-	NC	NC	A27	B27	SE_ISO_7816_IO1	SECURITY	3.3 V	I/O
-	-	NC	NC	A28	B28	SE_ISO_7816_IO2	SECURITY	3.3 V	I/O
-	-	NC	NC	A29	B29	SE_ISO_14443_LA	SECURITY	-	I/O
-	-	NC	NC	A30	B30	SE_ISO_14443_LB	SECURITY	-	I/O
-	-	NC	NC	A31	B31	SE_ISO_7816_RST#	SECURITY	3.3 V	I
-	-	NC	NC	A32	B32	DGND	Ground	0 V	P
-	-	NC	NC	A33	B33	SE_ISO_7816_CLK	SECURITY	3.3 V	I
-	-	NC	NC	A34	B34	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A35	B35	DGND	Ground	0 V	P
O	1.8 V/3.3 V	MMC/SD	eMMC_CLK_X3	A36	B36	NC	NC	-	-
P	0 V	Ground	DGND	A37	B37	NC	NC	-	-
O	1.8 V/3.3 V	MMC/SD	eMMC_CMD_X3	A38	B38	NC	NC	-	-
	1.8 V/3.3 V	MMC/SD	eMMC_DS_X3	A39	B39	NC	NC	-	-
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT0_X3	A40	B40	NC	NC	-	-
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT1_X3	A41	B41	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT2_X3	A42	B42	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT3_X3	A43	B43	CSI0_RXN4	CSI	1.8 V	I
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT4_X3	A44	B44	CSI0_RXP4	CSI	1.8 V	I
P	0 V	Ground	DGND	A45	B45	DGND	Ground	0 V	P
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT5_X3	A46	B46	CSI0_RXN3	CSI	1.8 V	I
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT6_X3	A47	B47	CSI0_RXP3	CSI	1.8 V	I
I/O	1.8 V/3.3 V	MMC/SD	eMMC_DAT7_X3	A48	B48	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A49	B49	CSI0_RXN2	CSI	1.8 V	I
-	-	NC	NC	A50	B50	CSI0_RXP2	CSI	1.8 V	I

-	-	NC	NC	A51	B51	DGND	CSI	0 V	P
-	-	NC	NC	A52	B52	CSI0_RXN1	CSI	1.8 V	I
-	-	NC	NC	A53	B53	CSI0_RXP1	CSI	1.8 V	I
-	-	NC	NC	A54	B54	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A55	B55	DGND	Ground	0 V	P
-	-	NC	NC	A56	B56	CSI0_RXN0	CSI	1.8 V	I
-	-	NC	NC	A57	B57	CSI0_RXP0	CSI	1.8 V	I
-	-	NC	NC	A58	B58	DGND	Ground	0 V	P
-	-	NC	NC	A59	B59	DGND	Ground	0 V	P
P	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	P

3.2 Boot Mode configuration

The MBa65xx supports the following TQMa65xx boot sources:

- SD Card
- eMMC
- NOR Flash
- I^2C
- SPI
- Ethernet
- USB (since silicon rev. 2.0)
- PCIe
- UART

The boot configuration interface is implemented with DIP switches and resistors as shown in the figure:

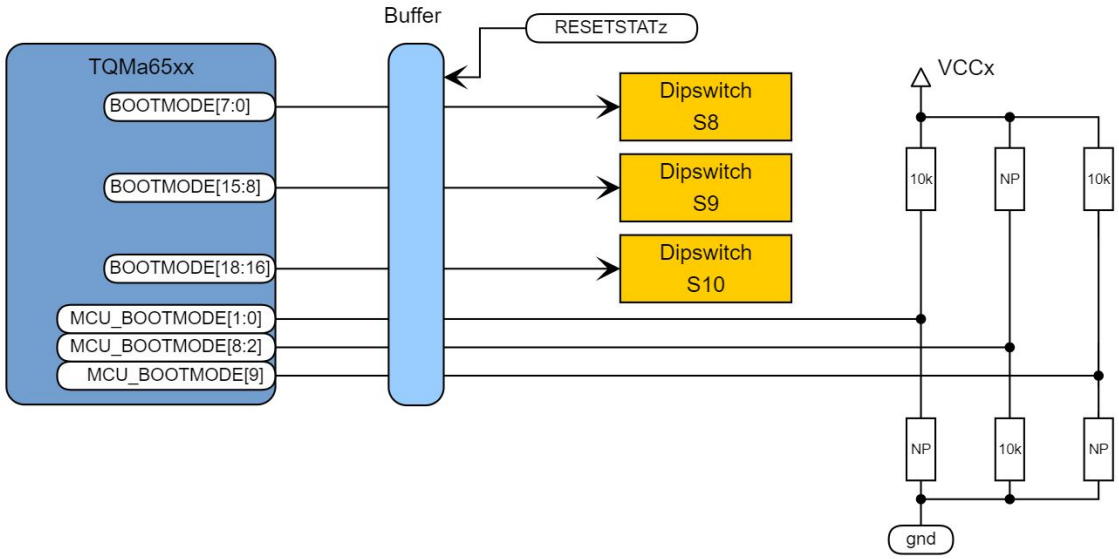

Figure 3: Block diagram Boot Mode

The boot source is selected via the S8, S9 and S10 switches. Detailed information on the boot configurations of the AM65 can be found in the User's Manual of the TQMa65xx.

The following table describes the settings of the DIP switches for possible boot media. The settings for Backup and Primary boot medium can be set independently of each other. Further settings such as transfer modes and CPU clock can be found in the User's Manual TQMa65xx. Switch position 1 means ON here, whereas 0 corresponds to the OFF position.

Table 8: Boot Mode configuration

SYSBOOT[6:0]							Boot-Mode
Backup			Primary				
6	5	4	3	2	1	0	
0	0	0	0	0	0	0	No boot
1	0	1	0	1	0	0	SPI
1	1	1	0	1	0	1	I2C
1	0	0	0	1	1	0	MMC/SD card, eMMC
0	1	1	0	1	1	1	Ethernet
0	0	1	1	0	0	0	USB
0	0	0	1	0	0	1	PCIe
0	1	0	1	0	1	0	UART

3.3 I²C devices

The TQMa65xx has five I²C interfaces which are available on the module connectors as primary function. The followingfigure shows the structure of the MCU_I2C on the mainboard. The bus switch is not relevant for general operation and only serves to separate individual components.

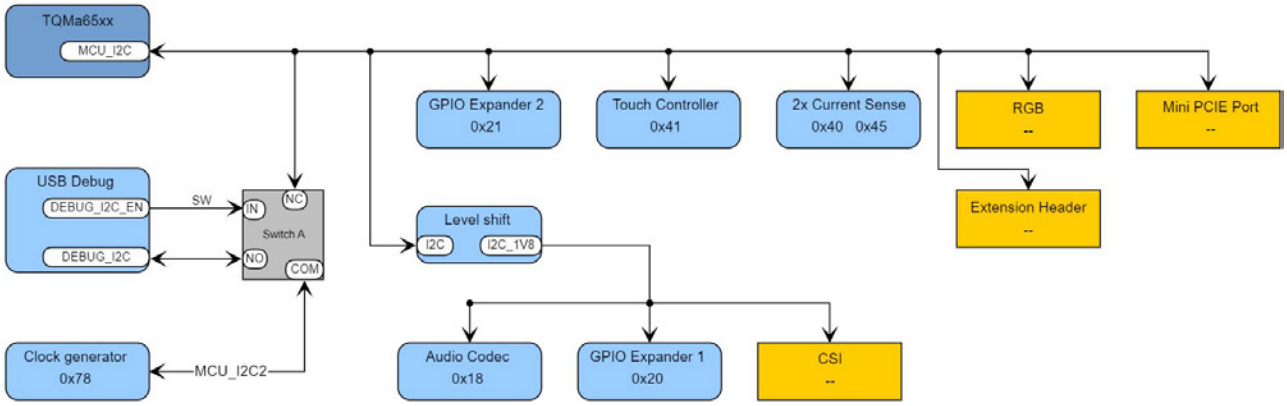

Figure 4: Block diagram I²C bus

The following table lists the used signals of the I2C interfaces:

Table 9: I²C signals

Signal	Dir.
I2C0_SDA	I/O
I2C0_SCL	O
I2C1_SDA	I/O
I2C1_SCL	O
I2C2_SDA	I/O
I2C2_SCL	O
WKUP_I2C_SDA	I/O
WKUP_I2C_SCL	O
MCU_I2C_SDA	I/O
MCU_I2C_SCL	O

The following devices are connected to the WKUP_I2C bus on the TQMa65xx:

Table 10: WKUP_I2C address allocation

Device	Address
Board controller (MKL04Z16VFM4)	0x11 / 001.0001
DC/DC converter (TPS62363YZH)	0x60 / 110.0000
EEPROM (M24C64-RDW6TP)	0x50 / 101.0000
Temperature sensor (SE97BTP)	0x1F / 001.1111
Temp. sensor EEPROM	0x57 / 101.0111
Temp. sensor EEPROM (WP)	0x37 / 011.0111
RTC (PCF85063ATL)	0x51 / 101.0001
TPM (SE050C2HQ1)	0x48 / 100.1000

On the MBa65xx the following devices are connected to the MCU_I2C bus:

Table 11: MCU I2C address allocation

Device	Address	Note
Clock (LMK05318RGZ)	0x78 / 111.1000	
GPIO expander I (PCA9555APW)	0x20 / 010.0000	
GPIO expander II (PCA9555APW)	0x21 / 010.0001	
Touch controller (USB2517I-JZX)	0x41 / 100.0001	
Audio codec (TLV320AIC3204RHBT)	0x18 / 001.1000	
Current sense (INA226AIDGS)	0x45 / 100.0101	5 V module supply
Current sense (INA226AIDGS)	0x40 / 100.0000	24 V input voltage

The clock can be disconnected from the main line via a switch and can be controlled by the USB debug interface.
I2C0, I2C1 and I2C2 are available on pin headers on the MBa65xx and have no use on the mainboard.

Note: I^2C address conflicts	
	When changing the address due to assembly options or when connecting further I^2C components, it must be ensured that no address conflicts occur. Otherwise malfunctions may occur. The addresses preassigned by the TQMa65xx must also be observed (depending on the TQMa65xx variant used).

3.4 GPIO port expander

Two port expanders PCA9555A with 16 ports each are used to control various components on the MBa65xx.
The port expanders are configured via MCU_I2C. The addresses of the expanders can be changed by resistor reassembly.
In the initial state after power-on, all ports are set as input and the respective connected component is thus disabled. All enable and reset signals are Lo by default via pulldowns.

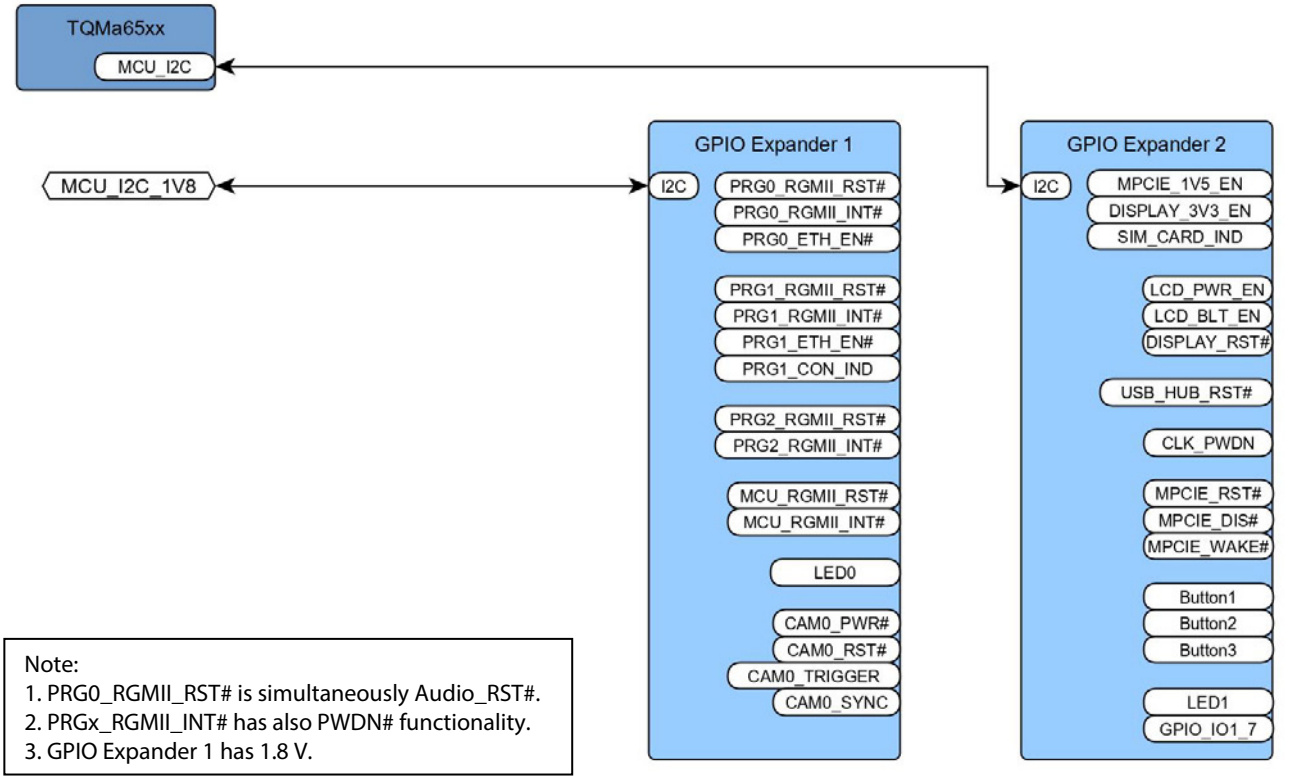

Figure 5: Block diagram port expander

The following tables explain the functions of the port expander pins.

Table 12: Port expander I functions, (0x20), 1.8 V

Port	Signal	Dir.	Remark
IO0_0	PRG0_RGMII_RST#	O	PRG0 Ethernet Reset (alternative Audio Reset), signal with pulldown to GND
IO0_1	PRG0_RGMII_INT#	I	PRG0 Ethernet Interrupt, has also PWDN# functionality, signal with pullup to 1.8 V
IO0_2	PRG0_ETH_EN#	IO	PRG0 Enable Detect, General Purpose Output, signal with pullup to 1.8 V
IO0_3	PRG1_RGMII_RST#	O	PRG1 Ethernet Reset, signal with pulldown to GND
IO0_4	PRG1_RGMII_INT#	I	PRG1 Ethernet Interrupt, has also PWDN# functionality, signal with pullup to 1.8 V
IO0_5	PRG1_ETH_EN#	IO	PRG1 Enable Detect, General Purpose Output, signal with pulldown to GND
IO0_6	PRG1_CON_IND	IO	PRG1 Connector Detect, General Purpose Output, signal with pulldown to GND
IO1_7	PRG2_RGMII_RST#	O	PRG2 Ethernet Reset, signal with pulldown to GND
IO1_0	PRG2_RGMII_INT#	I	PRG2 Ethernet Interrupt, has also PWDN# functionality, signal with pullup to 1.8 V
IO1_1	MCU_RGMII0_RST#	O	MCU Ethernet Reset, signal with pulldown to GND
IO1_2	MCU_RGMII0_INT#	I	MCU Ethernet Interrupt, signal with pullup to 1.8 V
IO1_3	LED0	O	Software controlled LED, signal with pulldown to GND
IO1_4	CAM0_PWR#	O	CSI Interface Power Enable
IO1_5	CAM0_RST#	O	CSI Interface Reset, signal with pulldown to GND
IO1_6	CAM0_TRIGGER	O	CSI Interface Trigger
IO1_7	CAM0_SYNC	O	CSI Interface Synchronisation

Table 13: Port expander II functions, (0x21), 3.3 V

Port	Signal	Dir.	Remark
IO0_0	MPCIE_1V5_EN	O	Mini PCIe 1.5 V supply enable, signal with pulldown to GND
IO0_1	DISPLAY_3V3_EN	O	LVDS connector 3.3 V supply enable, signal with pulldown to GND
IO0_2	SIM_CARD_IND	I	Indicator for inserted sim card, signal with pullup to 3.3 V
IO0_3	LCD_PWR_EN	O	Power enable for LVDS/RGB Display, signal with pulldown to GND
IO0_4	LCD_BLT_EN	O	Backlight enable for LVDS/RGB Display
IO0_5	DISPLAY_RST#	O	Reset for LVDS/RGB Display (optional), signal with pulldown to GND
IO0_6	USB_HUB_RST#	O	Reset for USB Hub, signal with pulldown to GND
IO1_7	CLK_PDN#	O	Power Down signal for Ethernet/PCIe Clock, signal with pulldown to GND
IO1_0	MPCIE_RST#	O	Mini PCIe Reset, signal with pulldown to GND
IO1_1	MPCIE_DIS#	O	Mini PCIe Disable
IO1_2	MPCIE_WAKE#	O	Mini PCIe Wakeup
IO1_3	BUTTON_NAV0	I	Navigation button 0
IO1_4	BUTTON_NAV1	I	Navigation button 1
IO1_5	BUTTON_NAV2	I	Navigation button 2
IO1_6	LED1	O	Software controlled LED
IO1_7	MKBUS_RST#	O	Reset for MikroBus pin strip

3.5 Clock and network synchronization

An LMK05318 is used as clock generator. This serves as clock source for the Ethernet interfaces of the six PRUs, mini PCIe and SerDes. Depending on the application, any frequencies can be set and mini PCIe can be operated in synchronous or asynchronous mode. The LMK05318 can also get its reference from the Ethernet PHYs of PRG1 and optionally PRG2. This allows frequency synchronization of all real-time Ethernet interfaces as well as the mini PCIe interface (SyncE).

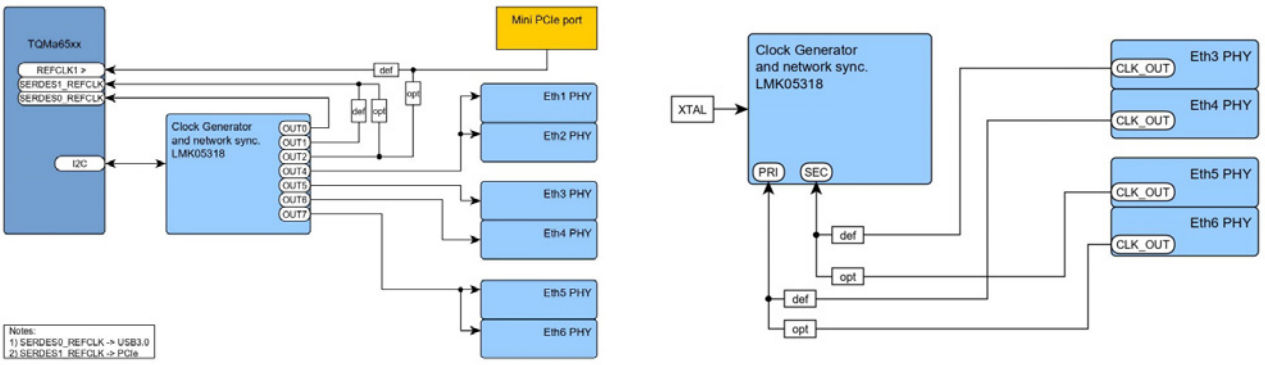

Figure 6: Block diagram clock

The clock generator is connected to the MCU_I2C bus and can be programmed via this bus (optionally also via the USB debug interface).

3.6 Multiplexing

On the MBa65xx two buses are provided with switches.
Firstly the MAC interface of the PRG0 subsystem contains switches, because there is an internal multiplexing with the MCASP interface, i.e. audio, in the CPU. So that one or the other interface can be used as required, the lines are multiplexed on the mainboard and the respective disconnected interface is deactivated.
Secondly, the PHYs of the PRG1 can be disconnected from the MAC. This allows the MAC to be used on a customer-designed plug-on board, which can be plugged onto the standard board-to-board connector X11.

3.6.1 PRG0 – MCASP Switch

The PRG0-MCASP switch switches between the Ethernet interfaces Eth1/Eth2 and audio. In audio mode the unused GPIOs of the PRUs as well as the clock are executed on pin headers.
Switching is possible manually via a dipswitch (Fn switch).

Table 14: PRG0 GPIO assignment

Module side		Interface side			
		Multiplexing 1		Multiplexing 2	
Source	Signal	Target	Signal	Target	Signal
X2-B37	PRG0_PRU0_GPIO3	Eth1	PRG0_RGMII1_TR_RXD3	X26-3	GPIO1_32_SW
X2-B38	PRG0_PRU0_GPIO2	Eth1	PRG0_RGMII1_TR_RXD2	X26-5	GPIO1_31_SW
X2-B39	PRG0_PRU0_GPIO1	Eth1	PRG0_RGMII1_TR_RXD1	Audio	MCASP0_FSX
X2-B40	PRG0_PRU0_GPIO0	Eth1	PRG0_RGMII1_TR_RXD0	Audio	MCASP0_ACLKX
X2-B42	PRG0_PRU0_GPIO4	Eth1	PRG0_RGMII1_TR_RXCTRL	Audio	MCASP0_AXR0
X2-B43	PRG0_PRU0_GPIO6	Eth1	PRG0_RGMII1_TR_RXCLK	Audio	MCASP0_AXR2
X2-B32	PRG0_PRU0_GPIO15	Eth1	PRG0_RGMII1_TR_TX3	X26-17	GPIO1_44_SW
X2-B33	PRG0_PRU0_GPIO14	Eth1	PRG0_RGMII1_TR_TX2	X26-15	GPIO1_43_SW
X2-B34	PRG0_PRU0_GPIO13	Eth1	PRG0_RGMII1_TR_TX1	X26-13	GPIO1_42_SW
X2-B35	PRG0_PRU0_GPIO12	Eth1	PRG0_RGMII1_TR_TX0	X26-11	GPIO1_41_SW
X2-B45	PRG0_PRU0_GPIO11	Eth1	PRG0_RGMII1_TR_TXCTRL	X26-9	GPIO1_40_SW
X2-B44	PRG0_PRU0_GPIO16	Eth1	PRG0_RGMII1_TR_GTXCLK	X26-4	GPIO1_45_SW
X2-A37	PRG0_PRU1_GPIO3	Eth2	PRG0_RGMII2_TR_RXD3	X26-12	GPIO1_52_SW
X2-A38	PRG0_PRU1_GPIO2	Eth2	PRG0_RGMII2_TR_RXD2	X26-10	GPIO1_51_SW
X2-A39	PRG0_PRU1_GPIO1	Eth2	PRG0_RGMII2_TR_RXD1	X26-8	GPIO1_50_SW
X2-A40	PRG0_PRU1_GPIO0	Eth2	PRG0_RGMII2_TR_RXD0	X26-6	GPIO1_49_SW
X2-A42	PRG0_PRU1_GPIO4	Eth2	PRG0_RGMII2_TR_RXCTRL	X26-14	GPIO1_53_SW
X2-A43	PRG0_PRU1_GPIO6	Eth2	PRG0_RGMII2_TR_RXCLK	X26-16	GPIO1_55_SW
X2-A32	PRG0_PRU1_GPIO15	Eth2	PRG0_RGMII2_TR_TX3	X27-9	GPIO1_64_SW
X2-A33	PRG0_PRU1_GPIO14	Eth2	PRG0_RGMII2_TR_TX2	X27-7	GPIO1_63_SW
X2-A34	PRG0_PRU1_GPIO13	Eth2	PRG0_RGMII2_TR_TX1	X27-5	GPIO1_62_SW
X2-A35	PRG0_PRU1_GPIO12	Eth2	PRG0_RGMII2_TR_TX0	X27-3	GPIO1_61_SW
X2-A45	PRG0_PRU1_GPIO11	Eth2	PRG0_RGMII2_TR_TXCTRL	X26-18	GPIO1_60_SW
X2-A44	PRG0_PRU1_GPIO16	Eth2	PRG0_RGMII2_TR_GTXCLK	X27-11	GPIO1_65_SW
X2-A55	PRG0_MDIO_MDIO	Eth1/2	PRG0_MDIO_MDIO_SW	-	NC
X2-A54	PRG0_MDIO_MDC	Eth1/2	PRG0_MDIO_MDC_SW	-	NC
Clock Out4	PRG0_ETH_CLK	Eth1/2	PRG0_ETH_CLK_SW	X27-13	CLK_OUT4_SW
X2-B48	PRG0_PRU0_GPIO5	Eth1	PRG0_RGMII1_GPIO0_SW	X26-7	GPIO1_34_SW
X2-A91	PRG0_PRU1_GPIO5	Eth2	PRG0_RGMII2_GPIO0_SW	Audio	MCASP0_AHCLKX

3.6.2 PRG1 Switch

In the case of the PRG1, there is no actual multiplexing. Instead, the MAC is additionally implemented via a high-speed board-to-board connector. If a plug-on card is attached, the on-board interface is deactivated and disconnected from the bus.
The interface can also be deactivated manually via a dipswitch (Fn switch).

Table 15: PRG1 GPIO assignment

Module side		Interface side			
		Multiplexing 1		Multiplexing 2	
Source	Signal	Source	Signal	Source	Signal
X2-B37	PRG1_RGMII1_TR_RXD3	Eth3	PRG1_RGMII1_TR_RXD_SW3	-	-
X2-B38	PRG1_RGMII1_TR_RXD2	Eth3	PRG1_RGMII1_TR_RXD_SW2	-	-
X2-B39	PRG1_RGMII1_TR_RXD1	Eth3	PRG1_RGMII1_TR_RXD_SW1	-	-
X2-B40	PRG1_RGMII1_TR_RXD0	Eth3	PRG1_RGMII1_TR_RXD_SW0	-	-
X2-B42	PRG1_RGMII1_TR_RXCTRL	Eth3	PRG1_RGMII1_TR_RXCTRL_SW	-	-
X2-B43	PRG1_RGMII1_TR_RXCLK	Eth3	PRG1_RGMII1_TR_RXCLK_SW	-	-
X2-B32	PRG1_RGMII1_TR_TX3	Eth3	PRG1_RGMII1_TR_TX_SW3	-	-
X2-B33	PRG1_RGMII1_TR_TX2	Eth3	PRG1_RGMII1_TR_TX_SW2	-	-
X2-B34	PRG1_RGMII1_TR_TX1	Eth3	PRG1_RGMII1_TR_TX_SW1	-	-
X2-B35	PRG1_RGMII1_TR_TX0	Eth3	PRG1_RGMII1_TR_TX_SW0	-	-
X2-B45	PRG1_RGMII1_TR_TXCTRL	Eth3	PRG1_RGMII1_TR_TXCTRL_SW	-	-
X2-B44	PRG1_RGMII1_TR_GTXCLK	Eth3	PRG1_RGMII1_TR_GTXCLK_SW	-	-
X2-A37	PRG1_RGMII2_TR_RXD3	Eth4	PRG1_RGMII2_TR_RXD_SW3	-	-
X2-A38	PRG1_RGMII2_TR_RXD2	Eth4	PRG1_RGMII2_TR_RXD_SW2	-	-
X2-A39	PRG1_RGMII2_TR_RXD1	Eth4	PRG1_RGMII2_TR_RXD_SW1	-	-
X2-A40	PRG1_RGMII2_TR_RXD0	Eth4	PRG1_RGMII2_TR_RXD_SW0	-	-
X2-A42	PRG1_RGMII2_TR_RXCTRL	Eth4	PRG1_RGMII2_TR_RXCTRL_SW	-	-
X2-A43	PRG1_RGMII2_TR_RXCLK	Eth4	PRG1_RGMII2_TR_RXCLK_SW	-	-
X2-A32	PRG1_RGMII2_TR_TX3	Eth4	PRG1_RGMII2_TR_TX_SW3	-	-
X2-A33	PRG1_RGMII2_TR_TX2	Eth4	PRG1_RGMII2_TR_TX_SW2	-	-
X2-A34	PRG1_RGMII2_TR_TX1	Eth4	PRG1_RGMII2_TR_TX_SW1	-	-
X2-A35	PRG1_RGMII2_TR_TX0	Eth4	PRG1_RGMII2_TR_TX_SW0	-	-
X2-A45	PRG1_RGMII2_TR_TXCTRL	Eth4	PRG1_RGMII2_TR_TXCTRL	-	-
X2-A44	PRG1_RGMII2_TR_GTXCLK	Eth4	PRG1_RGMII2_TR_GTXCLK_SW	-	-
X2-A55	PRG1_MDIO_MDIO	Eth3/4	PRG1_MDIO_SW_MDIO	-	-
X2-A54	PRG1_MDIO_MDC	Eth3/4	PRG1_MDIO_SW_MDC	-	-
Clock Out5	PRG1_ETH3_CLK	Eth3	PRG1_ETH3_CLK_SW	-	-
Clock Out6	PRG1_ETH4_CLK	Eth4	PRG1_ETH4_CLK_SW	-	-
Clock Priref	PRG1_RECOV_CLK_PRI	Eth3	PRG1_RECOV_CLK_PRI_SW	-	-
Clock Secref	PRG1_RECOV_CLK_SEC	Eth4	PRG1_RECOV_CLK_SEC_SW	-	-
X2-B48	PRG0_PRU0_GPIO5	Eth1	PRG1_RGMII1_GPIO0_SW	-	-
X2-A91	PRG0_PRU1_GPIO5	Eth2	PRG1_RGMII2_GPIO0_SW	-	-

3.7 PRG1 Connector

The PRU-ICSSG1 is additionally designed with a high-speed board-to-board connector (Tyco 5177986-2) installed as standard. The pinout is described in the following table:

Table 16: PRG1 connector

Note	Ref.	Dir.	Type	Name	#	#	Name	Type	Dir.	Ref.	Note
			PWR	**VCC5V**	**1**	**2**	**PRG1_MDIO_MDC**	OCL	OUT	VCC1V8	
			PWR	**GND**	**3**	**4**	**PRG1_MDIO_MDIO**	OCL	BI	VCC1V8	
			PWR	**VCC3V3**	**5**	**6**	**GND**				
			PWR	**VCC3V3**	**7**	**8**	**PRG1_RGMII1_TR_TXD[3]**	CMOS	OUT	VCC1V8	
Plug on card indicator	VCC3V3	IN	ANALOG	**CON_IND**	**9**	**10**	**PRG1_RGMII1_TR_TXD[2]**	CMOS	OUT	VCC1V8	
			PWR	**GND**	**11**	**12**	**PRG1_RGMII1_TR_TXD[1]**	CMOS	OUT	VCC1V8	
			PWR	**GND**	**13**	**14**	**PRG1_RGMII1_TR_TXD[0]**	CMOS	OUT	VCC1V8	
			PWR	**VCC1V8**	**15**	**16**	**PRG1_RGMII1_TR_TXCLK**	CMOS	OUT	VCC1V8	
			PWR	**VCC1V8**	**17**	**18**	**PRG1_RGMII1_TR_TXCTRL**	CMOS	OUT	VCC1V8	
			PWR	**GND**	**19**	**20**	**GND**				
			PWR	**GND**	**21**	**22**	**PRG1_RGMII1_TR_RXCLK**	CMOS	IN	VCC1V8	
	VCC1V8	BI	CMOS	**PRG1_PRU0_GPIO7**	**23**	**24**	**PRG1_RGMII1_TR_RXD[0]**	CMOS	IN	VCC1V8	
	VCC1V8	BI	CMOS	**PRG1_PRU0_GPIO17**	**25**	**26**	**PRG1_RGMII1_TR_RXD[1]**	CMOS	IN	VCC1V8	
	VCC1V8	BI	CMOS	**PRG1_PRU0_GPIO18**	**27**	**28**	**PRG1_RGMII1_TR_RXD[2]**	CMOS	IN	VCC1V8	
	VCC1V8	BI	CMOS	**PRG1_PRU0_GPIO19**	**29**	**30**	**PRG1_RGMII1_TR_RXD[3]**	CMOS	IN	VCC1V8	
	VCC1V8	BI	CMOS	**PRG1_PRU0_GPIO5**	**31**	**32**	**PRG1_RGMII1_TR_RXCTL**	CMOS	IN	VCC1V8	
	VCC1V8	BI	CMOS	**PRG1_PRU1_GPIO5**	**33**	**34**	**GND**				
			PWR	**GND**	**35**	**36**	**PRG1_RGMI2_TR_TXD[3]**	CMOS	OUT	VCC1V8	
Sync. Ref. (primary)	VCC1V8	IN	LVCMOS	**PRG1_RECOV_CLK_PRI**	**37**	**38**	**PRG1_RGMI2_TR_TXD[2]**	CMOS	OUT	VCC1V8	
	VCC1V8	OUT	LVCMOS	**PRG1_ETH3_CLK**	**39**	**40**	**PRG1_RGMI2_TR_TXD[1]**	CMOS	OUT	VCC1V8	
			PWR	**GND**	**41**	**42**	**PRG1_RGMI2_TR_TXD[0]**	CMOS	OUT	VCC1V8	
Sync. Ref. (secundary)	VCC1V8	IN	LVCMOS	**PRG1_RECOV_CLK_SEC**	**43**	**44**	**PRG1_RGMI2_TR_TXCLK**	CMOS	OUT	VCC1V8	
	VCC1V8	OUT	LVCMOS	**PRG1_ETH4_CLK**	**45**	**46**	**PRG1_RGMI2_TR_TXCTRL**	CMOS	OUT	VCC1V8	
			PWR	**GND**	**47**	**48**	**GND**				
UART_TXD of PRU	VCC1V8	BI	CMOS	**PRG1_PRU1_GPIO9**	**49**	**50**	**PRG1_RGMI2_TR_RXCLK**	CMOS	IN	VCC1V8	
UART_TXD of PRU	VCC1V8	BI	CMOS	**PRG1_PRU1_GPIO10**	**51**	**52**	**PRG1_RGMI2_TR_RXD[0]**	CMOS	IN	VCC1V8	
	VCC1V8	OUT	OCL	**PRG1_RGMII_RST#**	**53**	**54**	**PRG1_RGMI2_TR_RXD[1]**	CMOS	IN	VCC1V8	
	VCC1V8	IN	OCL	**PRG1_RGMII_INT#**	**55**	**56**	**PRG1_RGMI2_TR_RXD[2]**	CMOS	IN	VCC1V8	
	VCC3V3	BI	OCL	**I2C1_SDA**	**57**	**58**	**PRG1_RGMI2_TR_RXD[3]**	CMOS	IN	VCC1V8	
	VCC3V3	OUT	OCL	**I2C1_SCL**	**59**	**60**	**PRG1_RGMI2_TR_RXCTL**	CMOS	IN	VCC1V8	

The signal CON_IND serves as an indicator for an attached card. This pin should be connected directly to the VCC3V3 supply on plug-on cards and should be able to drive at least 1mA. Plugging in a card then drives the signal Hi and disables the interface on the mainboard.

The two signals PRG1_ETH3_CLK and PRG1_ETH4_CLK are available as synchronous clock supply. For SyncE functionality PRG1_RECOV_CLK_PRI/SEC can also be used as references for the Network Synchronizer of the MBa65xx.

3.8 Temperature sensor and EEPROM

A SE97BTP with integrated EEPROM is mounted on the top of the TQMa65xx to monitor the temperature. The MBa65xx itself does not have any temperature sensors.

3.9 RTC backup

A Real Time Clock (RTC) with a separate (backup) power supply is used to maintain the current time in the event of an interrupted power supply. For the backup supply of the RTC on the TQMa65xx a lithium battery type CR2032 with very low self-discharge is used on the bottom side of the MBa65xx.

3.10 USB hub

To provide multiple USB 2.0 ports, the USB1 interface of the TQMa65xx is connected to a 7 x USB hub, the USB2517I. Four of the seven ports are directly provided for external devices via two double sockets. The remaining three are used for Mini PCIe and for the two display interfaces. A reset of the hub is possible via a GPIO of Port Expander 2.

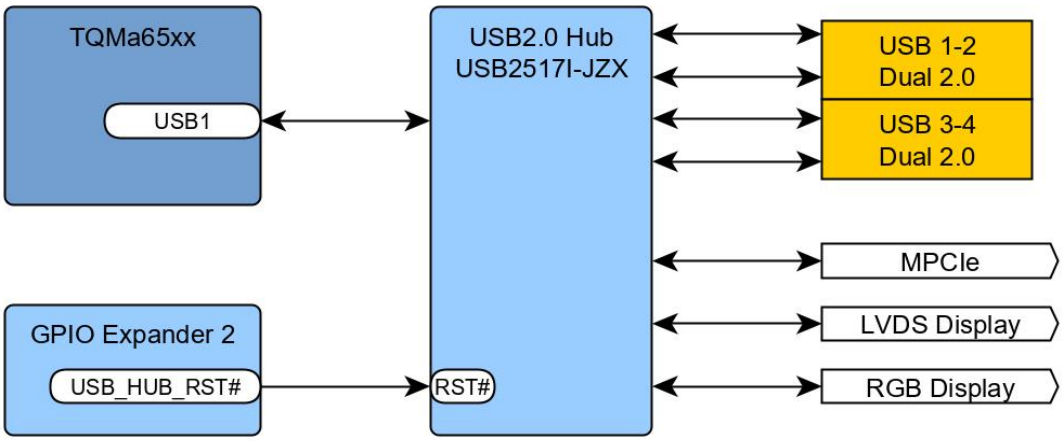

Figure 7: Block diagram USB hub

The USB sockets and the display interfaces have their own USB power supply (VBUS). The supply can be switched via a switch and is turned off in case of an overload (from Iout > 500 mA). In case of Mini PCIe the supply is done via the main supply of the plug-in card.

The wiring of all four sockets is as described in the table:

Table 17: Pinout USB 2.0 sockets (USB Micro Type A, double) with x = (1, 2, 3, 4)

Pin	Pin name	Signal	I/O	Note
1	VBUS	USB20_Hx_VBUS	P	110 µF decoupling + EMI filter
2	D-	USB20_Hx_DM	I/O	Common mode choke in series
3	D+	USB20_Hx_DP	I/O	Common mode choke in series
4	DGND	DGND	P	

The following tables show the pin assignment of the connectors used:

Table 18: USB Host 5 assignment for Mini PCIe (connector X29)

Pin	Pin name	Signal	I/O	Note
36	D-	USB20_H5_DM	I/O	Common mode choke in series
38	D+	USB20_H5_DP	I/O	Common mode choke in series

Table 19: Pin assignment USB Host 6 for LVDS display interface (pin header X34)

Pin	Pin name	Signal	I/O	Note
13	D-	USB20_H6_DM	I/O	Common mode choke in series
14	D+	USB20_H6_DP	I/O	Common mode choke in series

Table 20: Pin assignment USB Host 7 for RGB display interface (connector X109)

Pin	Pin name	Signal	I/O	Note
16	D-	USB20_H7_DM	I/O	Common mode choke in series
18	D+	USB20_H7_DP	I/O	Common mode choke in series

3.11 Data interfaces

3.11.1 Audio

The TLV320 from Texas Instruments is used as audio codec. This is connected to the module via SAI (configured as I2S) and I2C. The audio codec provides microphone, line in and line out signals. The signals are ESD protected and can be tapped via 3.5 mm jack sockets.

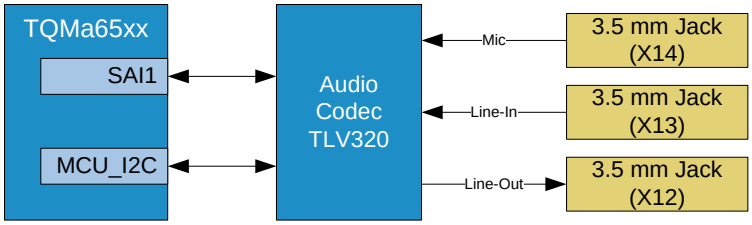

Figure 8: Block diagram Audio

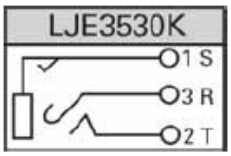

Figure 9: Pinout 3.5 mm jack

By using a placement option, it is possible to choose between line-out or headphone:

Table 21: Assembly option Line-Out / Headphone

Mode	R359	R360	R357	R358	Remark
Line-Out	0 Ω	0 Ω	NP	NP	Default
Headphone	NP	NP	0 Ω	0 Ω	–

Table 22: Pinout Audio (X14, X13, X12)

Channel	Pin	Signal	Remark
MIC (X14)	1	GND_AUDIO	
	2	MIC_IN	2.2 kΩ in series to MIC_BIAS + ESD protection
	3	GND_AUDIO	Mic right (not used ⇨ pull-down to AGND_AUD)
Line-In (X13)	1	GND_AUDIO	
	2	LINE_IN_L	470 nF in series + ESD protection
	3	LINE_IN_R	470 nF in series + ESD protection
Line-Out (X12)	1	GND_AUDIO	
	2	AUDIO_OUT_L	1 µF and 100 Ω in series + 47 nF against GND_AUDIO, optional connection to HP_L possible + ESD protection
	3	AUDIO_OUT_R	1 µF and 100 Ω in series + 47 nF against GND_AUDIO, optional connection to HP_R possible + ESD protection

3.11.2 CAN

The two CAN interfaces of the MBa65xx are operated directly from the CAN ports of the TQMa65xx and are available at the three-pin connectors X31 and X32. Both interfaces are galvanically isolated up to 2 kVAC (the CAN interfaces are not galvanically isolated from each other).

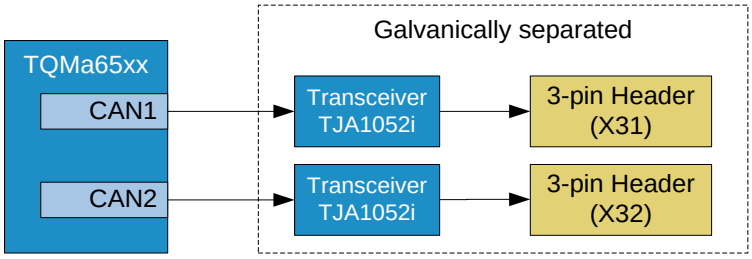

Figure 10: Block diagram CAN

The two CAN interfaces are designed identically. Regardless of the processor variant, CAN-FD can be transmitted with a data transfer rate of max. 5 Mbit/s.
With the switches S3 or S7 a 120 Ohm termination can be switched on at the bus 1 or 2.

Table 23: Pinout CAN0 / 1 (X31, X32)

CAN	Pin	Pin name	Dir.	Signal	Remark
CAN1 (X31)	1	CAN_H	I/O	DCAN1_H	galvanically isolated
	2	CAN_L	I/O	DCAN1_L	galvanically isolated
	3	DGND	P	GND_CAN	galvanically isolated
CAN2 (X32)	1	CAN_H	I/O	DCAN2_H	galvanically isolated
	2	CAN_L	I/O	DCAN2_L	galvanically isolated
	3	DGND	P	GND_CAN	galvanically isolated

3.11.3 Debug USB

On the MBa65xx the debug interface is implemented with the MCP2221A as USB-UART/I2C bridge. Due to the additional I2C functionality of the MCP2221A the USB interface can also be used for programming the clock. For this the corresponding components are separated from the main line with a switch.

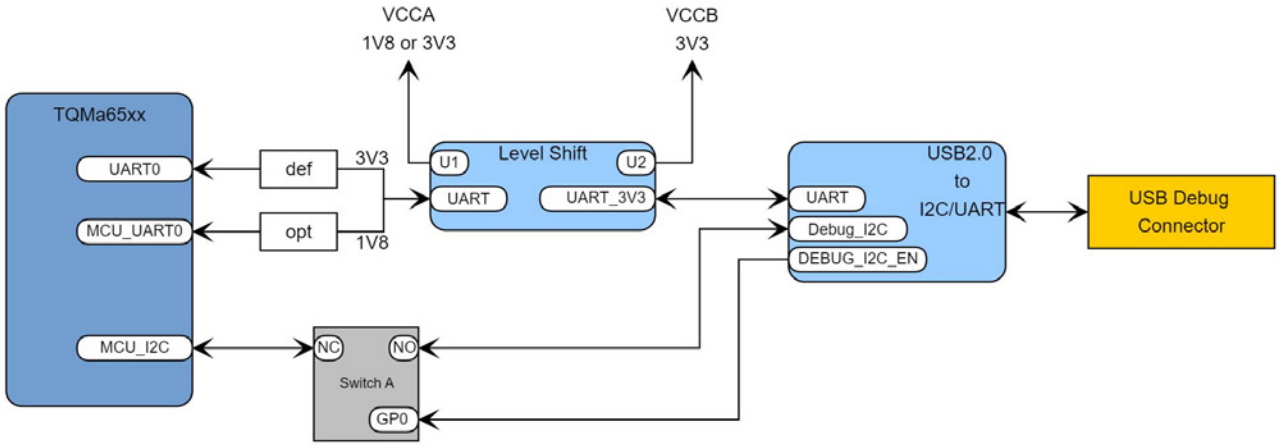

Figure 11: Block diagram USB debug

As usual the UART functionality provides a debugging interface for the CPU.

Table 24: Pin assignment Debug USB (X37)

Pin	Signal
1	USB_DBG_VBUS
2	USB_DBG_DM
3	USB_DBG_DP
4	NC
5	DGND
M1…M4	DGND

3.11.4 GBit Ethernet (PRU-ICSSG)

The AM65xx has a total of 6 PRUs with real-time Ethernet ports. These are basically designed in the same way. One DP83867ISR PHY each is connected to the MACs and one RJ45 socket each with integrated transformer. The reset/interrupt signals are shared by two PHYs of each PRG subsystem, as well as one clock output of the clock generator. For further functionality, one GPIO of each PHY is connected to one GPIO of the corresponding PRU at PRG0 and PRG1.

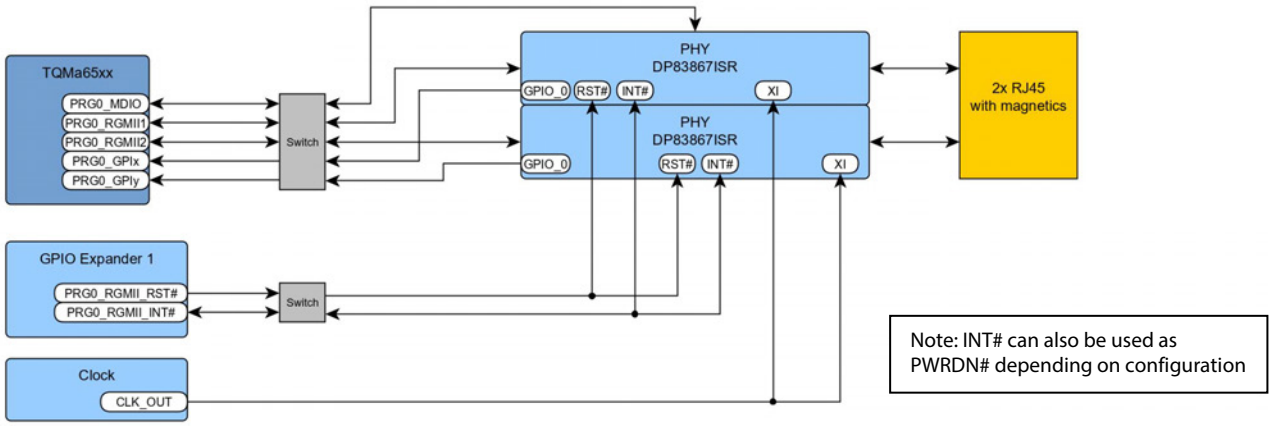

Figure 12: Block diagram Ethernet for PRG0

The upper figure shows the interface for PRG0 (PRU 1 and PRU 2). Since CPU internally the PRG0 is exclusive with MCASP (audio), the lines can be separated via switches depending on which interface is used.

In PRG1 (figure below) there is no CPU-internal multiplexing, but the interface is alternatively implemented via a slot, which is why the on-board interface can also be separated via switches. In addition, the PHYs here have separate clock signals and also serve as sources for a primary and secondary reference clock. The MBa65xx is thus not only real-time capable, but also supports SyncE.

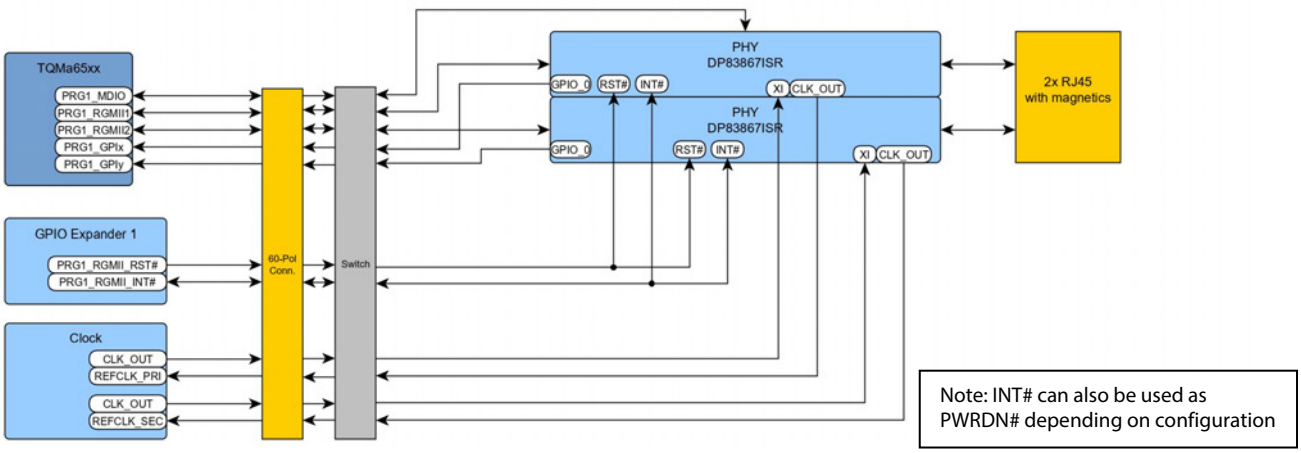

Figure 13: Block diagram Ethernet for PRG1

PRG2 is structurally similar to PRG0, but has no special features. So there are no bus switches installed and also the additional GPIOs are not present.

Table 25: Contact assignment RJ45 sockets X4, X5, X6, X7, X15, X16

Pin	Pin name	Signal	I/O	Note
11	J1	PRGx_RGMIIy_TD_P_A	I/O	–
10	J2	PRGx_RGMIIy_TD_M_A	I/O	–
4	J3	PRGx_RGMIIy_TD_P_B	I/O	–
5	J6	PRGx_RGMIIy_TD_M_B	I/O	–
3	J4	PRGx_RGMIIy_TD_P_C	I/O	–
2	J5	PRGx_RGMIIy_TD_M_C	I/O	–
8	J7	PRGx_RGMIIy_TD_P_D	I/O	–
9	J8	PRGx_RGMIIy_TD_M_D	I/O	–

3.11.5 Display interfaces

The AM65x CPU has a display subsystem (DSS) which provides a 24-bit RGB interface and LVDS.

3.11.5.1 RGB

The AM65x CPU has a 24-bit parallel LCD interface VOUT1. On the MBa65xx this interface provides a 24-/18-bit RGB interface. Beside the RGB interface further auxiliary signals of the CPU for e.g. a touch controller and the control of the display are led to a pin header.

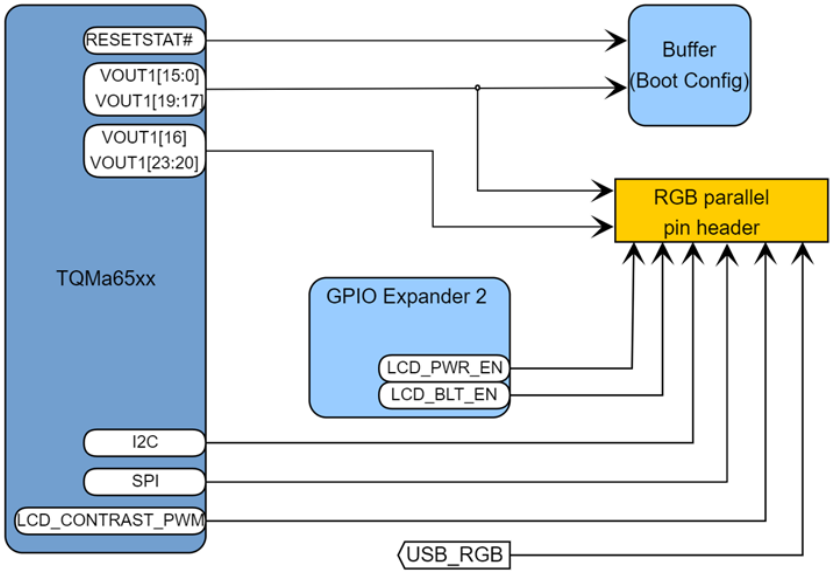

Figure 14: Block diagram RGB

Pinout 24 Bit RGB parallel Interface:

Table 26: Pin assignment pin headers X108, X109, X110

Group	Signal	Pin (X108)		Signal	Group
Power	VCC12V	1	2	VCC3V3	Power
Power	VCC5V	3	4	VCC3V3	Power
Power	DGND	5	6	DGND	Power
LCD	VOUT1_PCLK	7	8	VOUT1_DE	LCD
LCD	VOUT1_HSYNC	9	10	VOUT1_ DATA[1]	LCD
LCD	VOUT1_VSYNC	11	12	VOUT1_ DATA[3]	LCD
LCD	VOUT1_DATA[0]	13	14	VOUT1_ DATA[5]	LCD
LCD	VOUT1_ DATA[2]	15	16	VOUT1_ DATA[7]	LCD
LCD	VOUT1_ DATA[4]	17	18	VOUT1_ DATA[9]	LCD
LCD	VOUT1_ DATA[6]	19	20	VOUT1_ DATA[11]	LCD
Group	Signal	Pin (X109)		Signal	Group
LCD	VOUT1_ DATA[8]	1	2	VOUT1_ DATA[13]	LCD
LCD	VOUT1_ DATA[10]	3	4	VOUT1_ DATA[15]	LCD
LCD	VOUT1_ DATA[12]	5	6	VOUT1_ DATA[17]	LCD
LCD	VOUT1_ DATA[14]	7	8	VOUT1_ DATA[19]	LCD
LCD	VOUT1_ DATA[16]	9	10	VOUT1_ DATA[21]	LCD
LCD	VOUT1_ DATA[18]	11	12	VOUT1_ DATA[23]	LCD
LCD	VOUT1_ DATA[20]	13	14	USB_H7_VBUS	Power
LCD	VOUT1_ DATA[22]	15	16	USB_H7_DM	USB4
Power	DGND	17	18	USB_H7_DP	USB4
I2C2	MCU_I2C_SCL	19	20	DGND	Power
Group	Signal	Pin (X110)		Signal	Group
I2C2	MCU_I2C_SDA	1	2	NC	-
SPI1	SPI0_D1[1]	3	4	SPI0_D0	SPI16
SPI1	SPI0_CS0	5	6	SPI0_SCLK	SPI1
SPI1	SPI0_CS1	7	8	DGND	Power
LCD	LCD_PWR_EN	9	10	LCD_BLT_EN	LCD
LCD	MBA65_RST#[2]	11	12	GPIO_46_3V3[3]	LCD
Power	DGND	13	14	DGND	Power
Touch	TOUCH_Y+	15	16	TOUCH_X+	Touch
Touch	TOUCH_Y-	17	18	TOUCH_X-	Touch
Power	DGND	19	20	DGND	Power

3.11.5.2 LVDS

The LVDS interface is implemented via two DF19 connectors on the bottom side of the mainboard. The LVDS data signals (4x TX and 1x clock pairs) as well as 3.3 V and 5 V are connected to the first connector (30 pin, X33). To operate the display, command signals are routed to another connector (20 pin, X34).

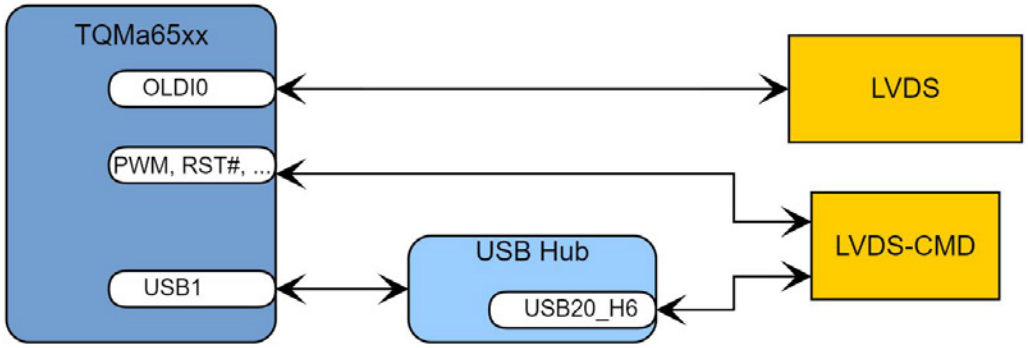

Figure 15: Block diagram LVDS

[1] SPI1_D0 and SPI1_D1 are configurable as MISO or MOSI
[2] Optional DISPLAY_RST# from GPIO Expander
[3] CD_CONTRAST_PWM. Level shifted GPIO1_46

The LVDS transceiver is configured for 8-bit FORMAT-1 mode and operates at 65 MHz clock frequency. For the pin assignment of the connectors (Hirose DF19G-30P-1H and DF19G-20P-1H) see the following tables.

Table 27: Pin assignment LVDS connector (X33)

Pin	Signal	Note
1	OLDI0_A0N	ESD protection
2	OLDI0_ A0P	ESD protection
3	OLDI0_ A1N	ESD protection
4	OLDI0_ A1P	ESD protection
5	OLDI0_ A2N	ESD protection
6	OLDI0_ A2P	ESD protection
7	DGND	
8	OLDI0_ CLKN	ESD protection
9	OLDI0_ CLKP	ESD protection
10	OLDI0_ A3N	ESD protection
11	OLDI0_ A3P	ESD protection
12…13	NC	
14	DGND	
15…16	NC	
17	DGND	
18…23	NC	
24	DGND	
25…27	5 V	
28…30	3,3 V	Switched by GPIO
M1, M2	DGND	

Table 28: Pin assignment LVDS_CTRL connector (X34)

Pin	Signal	Note
1..3	12 V	
4…6	DGND	
7…8	5 V	
9…10	DGND	
11	USB20_H6_VBUS	ESD protection
12	DGND	
13	USB20_H6 _DM	ESD protection + Common mode choke in series
14	USB20_H6 _DP	ESD protection + Common mode choke in series
15	DGND	
16	DISPLAY_OLDI_RST#	ESD protection
17	LCD_BLT_EN	ESD protection
18	LCD_PWR_EN	ESD protection
19	GPIO_46_3V3 (LCD_CONTRAST_PWM)	ESD protection, GPIO1_46 - level converted
20	DGND	
M1	DGND	
M2	DGND	

3.11.6 MIPI CSI-2

The AM65x CPU has a Camera Sensor Interface-2 (CSI-2) receiver module. One interface has four lanes.

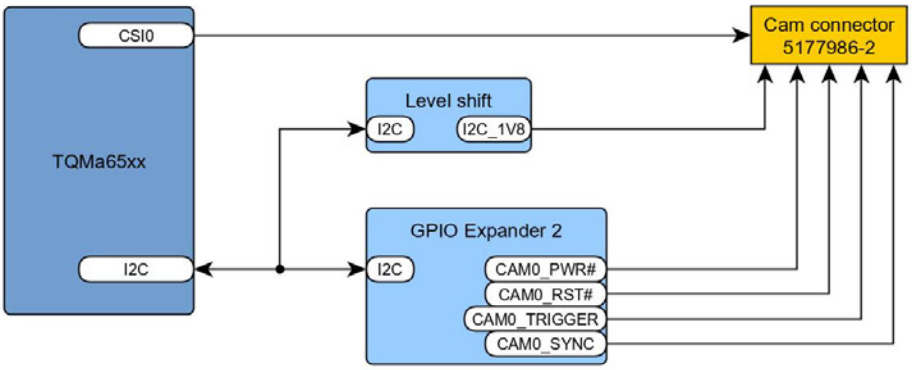

Figure 16: Block diagram MIPI CSI-2

Table 29: Pin assignment MIPI CSI-2 (X10)

Groupe	Signal	Pin X10		Signal	Groupe
Power	DGND	1	2	DGND	Power
Power	CAM0_PWR#	3	4	VCC1V8	Power
Reset	CAM0_RST#	5	6	DGND	Power
Control	CAM0_TRIGGER	7	8	NC	-
Control	CAM0_SYNC	9	10	NC	-
-	NC	11	12	NC	-
Power	DGND	13	14	DGND	Power
CSI0	CSI0_RXN4	15	16	NC	-
CSI0	CSI0_RXP4	17	18	NC	-
Power	DGND	19	20	DGND	Power
CSI0	CSI0_RXN3	21	22	NC	-
CSI0	CSI0_RXP3	23	24	NC	-
Power	DGND	25	26	DGND	Power
CSI0	CSI0_RXN2	27	28	NC	-
CSI0	CSI0_RXP2	29	30	NC	-
Power	DGND	31	32	DGND	Power
CSI0	CSI0_RXN1	33	34	NC	-
CSI0	CSI0_RXP1	35	36	NC	-
Power	DGND	37	38	DGND	Power
CSI0	CSI0_RXN0	39	40	NC	-
CSI0	CSI0_RXP0	41	42	NC	-
Power	DGND	43	44	DGND	Power
I2C	MCU_I2C_1V8_SDA	45	46	NC	-
I2C	MCU_I2C_1V8_SCL	47	48	NC	-
Power	DGND	49	50	DGND	Power
GPIO1	GPIO1_57	51	52	NC	-
Power	DGND	53	54	DGND	Power
-	NC	55	56	VCC5V	Power
-	NC	57	58	VCC5V	Power
-	NC	59	60	VCC5V	Power

3.11.7 Mini PCIe

A mini PCIe slot for full-size cards with an additional slot for SIM cards is implemented on the MBa65xx. For the pin assignment see the following table. According to the standard, the interface has a slot for cards with 50.95 mm x 30 mm dimensions and a PCIe lane (PCIe x1). The interface is supplied by the central clock with a freely configurable clock (and optionally synchronized with Ethernet).

Any standard-compliant mini PCIe card can be used, if necessary software drivers are available. A SIM card holder is also installed for the use of a GSM card.

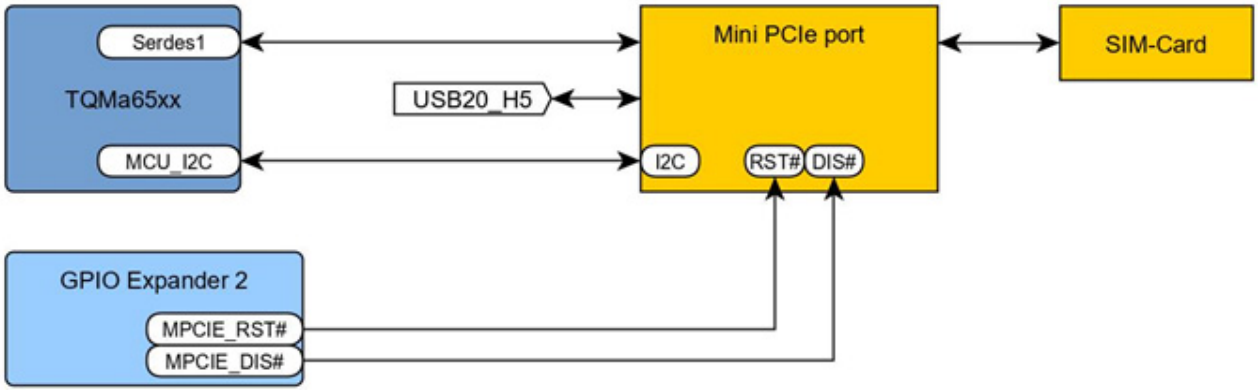

Figure 17: Block diagram Mini PCIe

Attention	
	When selecting a PCIe card to be used, the distance between the board and the card must be taken into account. The receptacle of the connector for the card is located 3.7 mm above the board. With heat sink screw connection with a protrusion of max. 2 mm, the space permitted according to PCIe specification is available.

The voltages provided for the Mini PCIe card may be loaded with the maximum currents specified in the following table.

Table 30: Maximum permitted currents Mini-PCIe

Voltage	Nominal value	Imax
VCC3V3_MPCIE	3.3 V	1100 mA
VCC1V5_MPCIE	1.5 V	375 mA

Table 31: Pin assignment SIM card connector (X30)

Pin	Signal	Remark
C1	SIM_V_PWR	-
C2	SIM_RST	-
C3	SIM_CLK	-
C5	DGND	-
C6	SIM_VPP	-
C7	SIM_DATA	-
SW1	NC	-
SW2	NC	-

Table 32: Pin assignment Mini PCIe (X29)

Pin	Signal	Remark
1	PCIE_WAKE#	Wake-Up-Signal of Mini PCIe card
2	VCC3V3_MPCIE	3.3 V supply voltage
3	NC	Not connected / reserved
4	DGND	Ground
5	NC	Not connected / reserved
6	VCC1V5_MPCIE	1.5 V supply voltage
7	NC	Clock-Request of Mini PCIe card
8	SIM_V_PWR	Supply voltage for SIM card
9	DGND	Ground
10	SIM_DATA	Bidirectional data line for SIM card
11	MPCIE_CLK_N	PCIE Clock from Clock Generator (alternatively from the CPU)
12	SIM_CLK	Clock output for SIM card
13	MPCIE_CLK_P	PCIE Clock from Clock Generator (alternatively from the CPU)
14	SIM_RST	Reset output for SIM card
15	DGND	Ground
16	SIM_VPP	Programming voltage for SIM card
17	NC	Not connected / reserved
18	DGND	Ground
19	NC	Not connected / reserved
20	PCIE_DIS#	Disable signal for Mini PCIe card (PCIE_DIS# level converted by GPIO port expander)
21	DGND	Ground
22	MBA65_RST#	Optional MPCIE_RST# from GPIO Expander
23	PCIE_RX_N	PCIe receive, 100 nF in series
24	VCC3V3_MPCIE	3.3 V supply voltage
25	PCIE_RX_P	PCIe receive, 100 nF in series
26	DGND	Ground
27	DGND	Ground
28	VCC1V5_MPCIE	1.5 V supply voltage
29	DGND	Ground
30	MCU_I2C_SCL	I^2C clock
31	PCIE_TX_N	PCIe transmit, 100 nF in series (on TQMa65xx)
32	MCU_I2C_SDA	I^2C data (I2C4)
33	PCIE_TX_P	PCIe transmit, 100 nF in series (on TQMa65xx)
34	DGND	Ground
35	DGND	Ground
36	USB20_H5_DM	Data USB Host 1, common mode choke in series
37	DGND	Ground
38	USB20_H5_DP	Data USB Host 1, common mode choke in series
39	VCC3V3_MPCIE	3.3 V supply voltage
40	DGND	Ground
41	VCC3V3_MPCIE	3.3 V supply voltage
42	LED_WWAN#	Status input WWAN#, in series with 270 Ω and green LED on VCC3V3_MPCIE
43	DGND	Ground
44	LED_WLAN#	Status input WLAN#, in series with 270 Ω and green LED on VCC3V3_MPCIE
45	NC	Not connected / reserved
46	LED_WPAN#	Status input WPAN#, in series with 270 Ω and green LED on VCC3V3_MPCIE
47	NC	Not connected / reserved
48	VCC1V5_MPCIE	1.5 V supply voltage
49	NC	Not connected / reserved
50	DGND	Ground
51	NC	Not connected / reserved
52	VCC3V3_MPCIE	3.3 V supply voltage

3.11.8 MikroBus

To be able to quickly verify serial interfaces, such as UART, I2C, SPI, a MicroBus socket strip for MikroBus modules is provided on the MBa65xx. MikroBus is a fixed standard with numerous expansion boards for evaluation purposes. Two connectors BL-15-SMD-043-08-B-SM from Fischer Elektronik are used.

Table 33: Pin assignment X38, X39

Group	Signal	Pin		Signal	Group
		X38	X39		
Analogue In	MCU_ADC1_AIN[7]	1	1	GPIO_36_3V3 (PWM)	GPIO1
GPIO	MKBUS_RST#	2	2	GPIO_47_3V3 (INT#)	GPIO1
SPI1	SPI1_CS0	3	3	GPIO1_66 (UART2_RXD)	GPIO1
SPI1	SPI1_CLK	4	4	GPIO1_56 (UART2_TXD)	GPIO1
SPI1	SPI1_D0	5	5	I2C1_SCL	I2C1
SPI1	SPI1_D1	6	6	I2C1_SDA	I2C1
Power	VCC3V3	7	7	VCC5V	Power
Power	GND	8	8	GND	Power

3.11.9 USB 3.0 Super-Speed OTG

The USB OTG interface of the TQMa65xx is realized on the MBa65xx with the USB3.0 Micro AB socket (X115).

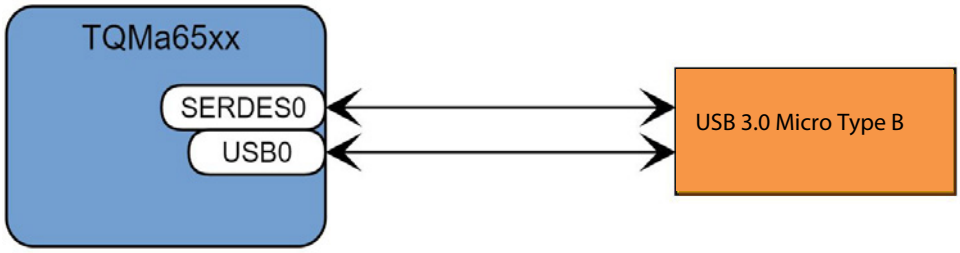

Figure 18: Block diagram USB OTG

The following table shows the pin assignment:

Table 34: Pinout USB OTG (USB Micro AB)

Pin	Pin name	Signal	I/O	Note
1	VBUS	USB0_30_VBUS	P	100 µF against DGND + EMI filter, Imax = 100 mA
2	D-	USB0_30_DM	I/O	Common mode choke in series
3	D+	USB0_30_DP	I/O	Common mode choke in series
4	ID	USB0_30_ID	I	
5	DGND	DGND	P	
6	SSTX-	USB0_30_TXDM	O	Common mode choke in series
7	SSTX+	USB0_30_TXDP	O	Common mode choke in series
8	GND_DRAIN		P	
9	SSRX-	USB0_30_RXDM	I	Common mode choke in series
10	SSRX+	USB0_30_RXDP	I	Common mode choke in series
M1-6	DGND	DGND	P	

The USB OTG ports of the TQMa65xx provide a theoretical data rate of 300 MB/s. Depending on the software and hardware used, the effective read and write rates of the ports can vary further.

3.11.10 SD card

The SD card connector X17 is directly connected to the SDHC controller of the TQMa65xx module. A 4-bit wide data interface is used.

The SDHC controller in the TQMa65xx module basically supports the UHS-I mode (not Silicon Rev. 1.0).

It is possible to boot from the SD card. All data lines are provided with ESD protection.

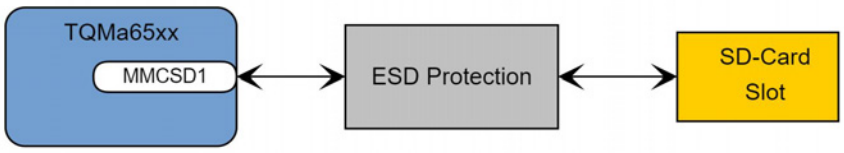

Figure 19: Block diagram SD card

Table 35: Pinout SD Card

Pin	Signal	Note
1	MMCSD1_DAT2	10 kΩ pull-up to VCC3V3 + ESD protection
2	MMCSD1_DAT3	10 kΩ pull-up to VCC3V3 + ESD protection
3	MMCSD1_CMD	10 kΩ pull-up to VCC3V3 + ESD protection
4	VCC3V3_SDCARD	3.3 V
5	MMCSD1_CLK	ESD protection
6	DGND	–
7	MMC1_DATA0	10 kΩ pull-up to VCC3V3 + ESD protection
8	MMC1_DATA1	10 kΩ pull-up to VCC3V3 + ESD protection
M1 - M4	DGND	Shield

3.11.11 Pin headers

The MBa65xx has several additional pin headers. All unused and some used signals are made available on these.
In addition to the signals, 1.8 V, 3.3 V, 5 V and 12 V are also available on some of them.

Note: Observe power consumption with regard to the overall system	
	The supply voltages (1.8 V, 12 V, etc.) provided at the MBa65xx headers are not individually fused. Technically, an overload of the fuse at the 24 V supply input is therefore possible. Please note the resulting total current consumption of the MBa65xx, which must be less than 4 A!

3.11.11.1 X23 – Communication

Table 36: Pinout X23

Group	Signal	Pin	Pin	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
UART0	UART0_RXD	3	4	MCU_SPI0_CLK	MCU_SPI0
UART0	UART0_TXD	5	6	MCU_SPI0_CS0	MCU_SPI0
UART0	UART0_CTS#	7	8	MCU_SPI0_D0	MCU_SPI0
UART0	UART0_RTS#	9	10	MCU_SPI0_D1	MCU_SPI0
I2C0	I2C0_SDA	11	12	I2C2_SDA	I2C2
I2C0	I2C0_SCL	13	14	I2C2_SCL	I2C2
MCU_I2C	MCU_I2C_SDA	15	16	GPIO1_37	GPIO1
MCU_I2C	MCU_I2C_SCL	17	18	MCU_UART0_3V3_TXD	MCU_UART0
GPIO1	MCU_I2C_INT#	19	20	MCU_UART0_3V3_RXD	MCU_UART0

3.11.11.2 X111 - Communication and security

Table 37: Pinout X111

Group	Signal	Pin	Pin	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
Sec. Element	SE_ISO_7816_RST#	3	4	SE_ISO_14443_LA	Sec. Element
–	NC	5	6	SE_ISO_14443_LB	Sec. Element
Sec. Element	SE_ISO_7816_IO2	7	8	DGND	Power
Sec. Element	SE_ISO_7816_IO1	9	10	DGND	Power
Sec. Element	SE_ISO_7816_CLK	11	12	WKUP_UART0_TXD	WKUP_UART0
Power	DGND	13	14	WKUP_UART0_CTS#	WKUP_UART0
WKUP_I2C	WKUP_I2C_SCL	15	16	WKUP_UART0_RXD	WKUP_UART0
WKUP_I2C	WKUP_I2C_SDA	17	18	WKUP_UART0_RTS#	WKUP_UART0
Power	DGND	19	20	DGND	Power

3.11.11.3 X20, X21 - GPIOs

Table 38: Pinout X20, X21

Group	Signal	Pin X20	Pin X20	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
GPIO0	GPIO0_64	3	4	GPIO1_13	GPIO1
GPIO0	GPIO0_83	5	6	GPIO1_14	GPIO1
GPIO0	GPIO0_84 (USB30_FAULT)	7	8	GPIO1_39	GPIO1
GPIO0	GPIO0_93	9	10	GPIO1_56 (UART2_TXD)	GPIO1
GPIO0	GPIO0_94	11	12	GPIO1_57 (CSI0_MCLK)	GPIO1
GPIO0	GPIO0_95	13	14	GPIO1_58	GPIO1
GPIO1	GPIO1_67	15	16	GPIO1_59	GPIO1
GPIO1	GPIO1_68	17	18	GPIO1_66 (UART2_RXD)	GPIO1
Power	DGND	19	20	GPIO1_38	GPIO1
Group	Signal	Pin X21	Pin X21	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
WKUP_GPIO0	WKUP_GPIO0_0	3	4	WKUP_GPIO0_25	WKUP_GPIO0
WKUP_GPIO0	WKUP_GPIO0_1	5	6	WKUP_GPIO0_26	WKUP_GPIO0
WKUP_GPIO0	WKUP_GPIO0_2	7	8	WKUP_GPIO0_27	WKUP_GPIO0
WKUP_GPIO0	WKUP_GPIO0_3	9	10	WKUP_GPIO0_28	WKUP_GPIO0
WKUP_GPIO0	WKUP_GPIO0_8	11	12	WKUP_GPIO0_31	WKUP_GPIO0
WKUP_GPIO0	WKUP_GPIO0_9	13	14	WKUP_GPIO0_32	WKUP_GPIO0
WKUP_GPIO0	WKUP_GPIO0_10	15	16	WKUP_GPIO0_33	WKUP_GPIO0
WKUP_GPIO0	WKUP_GPIO0_11	17	18	DGND	Power
Power	DGND	19	20	DGND	Power

3.11.11.4 X25 - Reset and board controller

Table 39: Pinout X25

Group	Signal	Pin	Pin	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
Reset	TQMA65_RESET#	3	4	SWD_DIO	TQMa65 µC
Reset	TQMA65_RESETSTAT#	5	6	SWD_CLK	TQMa65 µC
Reset	TQMA65_POR_OUT#	7	8	RST_BC#	TQMa65 µC
–	NC	9	10	IO1_RES (opt: RUN# 3V3, 1V8)	TQMa65 µC
Reset	MCU_PORz_OUT	11	12	IO2_RES (opt: BootCfg EN#)	TQMa65 µC
Reset	MCU_WARM_RESET_OUT	13	14	IO3_RES	TQMa65 µC
Safety	SOC_SAFETY_ERROR#	15	16	NC	–
Safety	MCU_SAFETY_ERROR#	17	18	DGND	Power
Power	DGND	19	20	DGND	Power

3.11.11.5 X22 - ADC Input

All ADC input signals with 10 kOhm pulldown

Table 40: X22 – ADC Input

Group	Signal	Pin	Pin	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
Analog In	MCU_ADC1_AIN[0]	3	4	MCU_ADC0_AIN[0]	Analog In
Analog In	MCU_ADC1_AIN[1]	5	6	MCU_ADC0_AIN[1]	Analog In
Analog In	MCU_ADC1_AIN[2]	7	8	MCU_ADC0_AIN[2]	Analog In
Analog In	MCU_ADC1_AIN[3]	9	10	MCU_ADC0_AIN[3]	Analog In
Analog In	MCU_ADC1_AIN[4]	11	12	MCU_ADC0_AIN[4]	Analog In
Analog In	MCU_ADC1_AIN[5]	13	14	MCU_ADC0_AIN[5]	Analog In
Analog In	MCU_ADC1_AIN[6]	15	16	MCU_ADC0_AIN[6]	Analog In
Analog In	MCU_ADC1_AIN[7]	17	18	MCU_ADC0_AIN[7]	Analog In
Power	DGND	19	20	DGND	Power

3.11.11.6 X26, X27 - GPIOs (PRG0) and miscellaneous

Table 41: Pinout X26, X27

Group	Signal	Pin X26	Pin X26	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
GPIO1	GPIO1_60_SW	3	4	GPIO1_44_SW	GPIO1
GPIO1	GPIO1_55_SW	5	6	GPIO1_43_SW	GPIO1
GPIO1	GPIO1_53_SW	7	8	GPIO1_42_SW	GPIO1
GPIO1	GPIO1_52_SW	9	10	GPIO1_41_SW	GPIO1
GPIO1	GPIO1_51_SW	11	12	GPIO1_40_SW	GPIO1
GPIO1	GPIO1_50_SW	13	14	GPIO1_34_SW	GPIO1
GPIO1	GPIO1_49_SW	15	16	GPIO1_32_SW	GPIO1
GPIO1	GPIO1_45_SW	17	18	GPIO1_31_SW	GPIO1
Power	DGND	19	20	DGND	Power
Group	Signal	Pin X27	Pin X27	Signal	Group
Power	VCC3V3	1	2	VCC1V8	Power
GPIO Exp.	GPIOEXP0_IO0_6/PRG1_CON_IND	3	4	EXT_REFCLK1	CPU Clk
GPIO Exp.	GPIOEXP0_IO0_5/PRG1_ETH_EN#	5	6	OSC1_EXT	CPU Clk
GPIO Exp.	GPIOEXP0_IO0_3/PRG0_ETH_EN#	7	8	CLK_OUT_4_SW	Clock
GPIO Exp.	MKBUS_RST#/GPIOEXP1_IO1_7_3V3	9	10	GPIO1_65_SW	GPIO1
Timer	TIMER_IO1	11	12	GPIO1_64_SW	GPIO1
Timer	TIMER_IO0	13	14	GPIO1_63_SW	GPIO1
Interrupt	NMI#	15	16	GPIO1_62_SW	GPIO1
PWM	ECAP0_IN_APWM_OUT	17	18	GPIO1_61_SW	GPIO1
Power	DGND	19	20	DGND	Power

3.11.11.7 X24 - Mainboard and module voltages

Table 42: Pinout X24

Group	Signal	Pin	Pin	Signal	Group
Power	VCC5V	1	2	VCC12V	Power
Power	VCC3V3	3	4	VCC1V8	Power
Power	DGND	5	6	DGND	Power
Power	VCC1V8_TQMA65	7	8	VCC3V3S_TQMA65	Power
Power	VCC1V8L1_TQMA65	9	10	VCC3V3_TQMA65	Power
Power	DGND	11	12	DGND	Power
Power	DGND	13	14	V_BAT	Power
Power	DGND	15	16	VCC3V3_SDCARD	Power
Power	DGND	17	18	DGND	Power
Power	DGND	19	20	DGND	Power

3.11.12 JTAG

The JTAG interface is implemented as a 20-pin header (X19). The necessary 10k pull-ups of the lines TDI, TDO, TMS, TRST# and SRST# as well as the 10k pull-down at TCK and RTCK are implemented on the MBa65xx. All signal lines use 3.3 V as reference. The JTAG interface is not ESD protected.

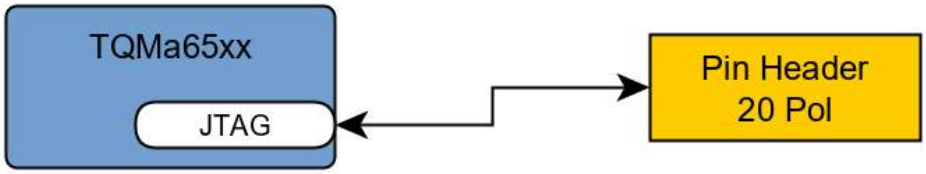

Figure 20: Block diagram JTAG

Table 43: Pinout JTAG (X19)

Group	Signal	Pin	Pin	Signal	Group
Power	JTAG_VREF	1	2	VCC3V3	Power
Reset	JTAG_TRST#	3	4	DGND	Power
JTAG Data	JTAG_TDI	5	6	DGND	Power
JTAG Mode	JTAG_TMS	7	8	DGND	Power
Clock	JTAG_TCK	9	10	DGND	Power
-	NC	11	12	DGND	Power
JTAG Data	JTAG_TDO	13	14	DGND	Power
Reset	JTAG_SRST#	15	16	DGND	Power
Emulation	JTAG_EMU0	17	18	DGND	Power
Emulation	JTAG_EMU1	19	20	DGND	Power

3.11.13 Debug Board Controller

A board controller is provided on the TQMa65xx, for which a separate debug / programming interface with a 10-pin header (X112) is available on the main board. This debug interface is for development purposes only.

Table 44: Module controller programming interface (X112)

Group	Signal	Pin	Pin	Signal	Group
Power	VCC3V3S_TQMA65	1	2	SWD_DIO	Module µC
Power	DGND	3	4	SWD_CLK	Module µC
Power	DGND	5	6	NC	–
–	NC	7	8	NC	–
–	NC	9	10	NC	–

The Segger J-Link with the following adapter is intended for programming:

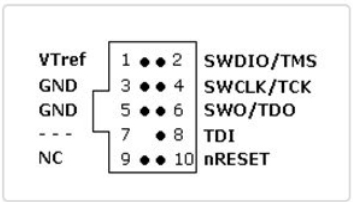

Figure 21: J-Link adapter (Source: Segger)

3.12 User interfaces

3.12.1 Power-/Reset buttons

A power button (S1) for hard resets and a reset button (S2) for soft resets are installed.

3.12.2 Navigation buttons

For development purposes three navigation buttons are connected to the port expander on the MBa65xx. By using the signal GPIO1_48 this is interrupt capable.

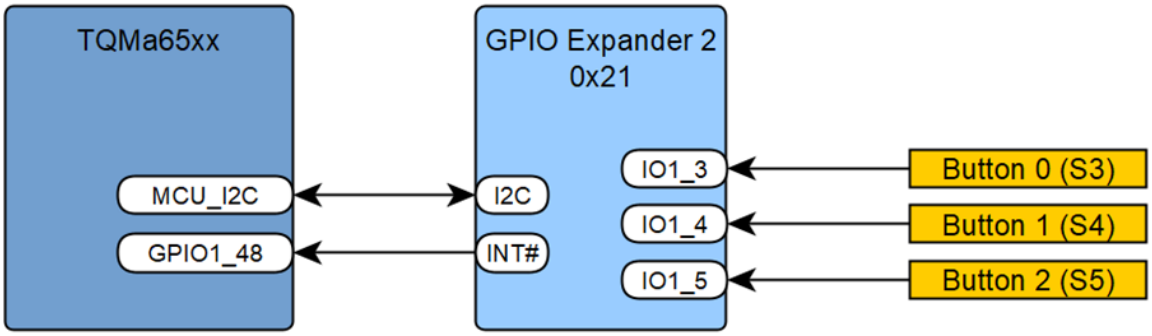

Figure 22: Block diagram navigation buttons

3.12.3 Buzzer

For acoustic signaling a buzzer is provided on the MBa65xx. The buzzer is controlled directly via a PWM-capable GPIO (GPIO1_39) of the AM65xx.

3.12.4 Status LEDs

The MBa65xx has 32 diagnostics and status LEDs to signal the system status. The following table shows the meaning of all LEDs.

Table 45: Status-LEDs

Function group	LED	Colour	Indication
Power	V146	Green	VCC3V3
	V147	Green	VCC24V
	V148	Green	VCC12V
	V149	Green	VCC5V
	V150	Green	VCC1V8
	V151	Green	VCC1V5_MPCIE
	V152	Green	VCC5V_MOD
	V156	Green	VCC3V3S_TQMA65
Reset	V103	Red	Hard Reset (Power Button)
	V7	Red	Warm Reset (Reset Button)
USB	V85	Green	USB30_OTG_VBUS
	V112	Green	USB20_H1_VBUS (light up when VBUS of USB2.0 Host 1 active)
	V113	Green	USB20_H2_VBUS (light up when VBUS of USB2.0 Host 2 active)
	V114	Green	USB20_H3_VBUS (light up when VBUS of USB2.0 Host 3 active)
	V115	Green	USB20_H4_VBUS (light up when VBUS of USB2.0 Host 4 active)
	V89	Green	USB_DEBUG_VBUS (light up when VBUS of USB-Debug active)
Mini PCIe	V86	Green	Mini-PCIe WWAN
	V87	Green	Mini-PCIe WLAN
	V88	Green	Mini-PCIe WPAN
GPIO	V1	Blue	LED of port expander (MCU_I2C:0x20) port IO1_3 (hi-active)
	V2	Blue	LED of port expander (MCU_I2C:0x21) port IO1_6 (hi-active)
Ethernet	X1-X7	Green	Link established
		Yellow	Activity indicator
		Orange	GPIO programmable (designated: Error)
Multiplexing	V5	Blue	Audio Interface active (exclusive PRG0)
	V6	Blue	Ethernet 1, 2 (PRG0) active (exclusive Audio)
	V3	Blue	PRG1 Plug-on card detected (exclusive on-Board Ethernet)
	V4	Blue	Ethernet 3, 4 (PRG1) active (exclusive Plug-on card)

3.12.5 Fn-switch S7

There are some additional switches on the MBa65xx, with which the interface multiplexing on the mainboard can be set and debugging/testing can be done.
The special feature of the Fn-switch is that the position of the switches is latched on reset (the input is not adjustable during operation).

Table 46: Fn-switch S7

		Function	
Interface	Reference	Off (0)	On (1)
Muxing Switch[1]	S7.1	Ethernet 1, 2 (PRG0) active	Audio (MCASP0) active
	S7.2	On-Board Ethernet 2, 3 (PRG1) active	Plug-on card can be used[2]

[1] S7 is latched. Changes are only applied with a complete hard reset.

[2] If the PRG1_CON_IND signal is correctly connected to VCC3V3 on the plug-on board, the on-board interface is automatically deactivated when the board is plugged on.

3.13 Power supply

The MBa65xx is usually supplied with 24 V. Switching regulators are used to generate the main voltage levels 5 V, 3.3 V, 1.8 V and 12 V. A dual output switching regulator generates 5V_MOD for the supply of the TQMa65xx module as well as another 5 V voltage for use on the mainboard, e.g. for USB and CAN.

The voltages 3.3 V and 1.8 V are used for the peripherals on the mainboard. Some of the voltages generated from them are individually switchable:

- VCC3V3_DISPLAY: Via a GPIO
- VCC1V5_MPCIE: Via a GPIO
- VCCxVx_ETHn: Disabled for n = (1, 2) when audio (MCASP) is used and disabled for n = (3, 4) when a plug-on card is used for PRG1
- VCCxVx_AUDIO: Disabled when Ethernet ports 1/2 (PRG0) are used

12 V supply is available on headers/plugs and is not used on the mainboard.

3.13.1 Input protection

The input supply of the MBa65xx is used to supply the switching regulators for 5V_MOD, 5 V, 12 V as well as 3.3V. The protection circuit has the following properties:

- Fuse 4 A, slow blow
- Overvoltage protection
- PI Filter
- Reverse polarity protection
- Voltage stabilization
- Capacitors for voltage smoothing

Figure 23: Block diagram Power-In

Table 47: Supply voltage V_24V_IN at Power-In (X44, X45)

Parameter	Min.	Typ.	Max.	Remark
Input voltage	16 V	24 V	32 V	–
Power consumption	–	TBD (1)	90 W (2)	–
Rated current of the fuse	–	4 A	–	–
Voltage limitation in case of overvoltage	40 V	–	44.2 V	Note: The MBa65xx may be damaged in case of permanent overvoltage!

1: Typical scenario is not defined.
2: Theoretical full load. All supply voltages are loaded with maximum current, e.g. by connecting additional load to the pin headers, and all system components have maximum power consumption.

Table 48: Pinout Power-In (X44, X45)

Pin	Pin	Signal	Type	Level	Remark
X45	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground
	3	(NC)	–	–	Not connected
X44	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground

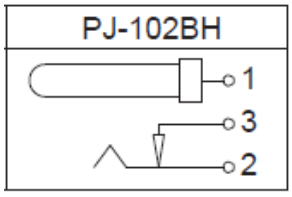

Figure 24: Pinout DC socket 2.5 mm/5.5 mm

3.14 Reset structure

Figure 25 shows the reset structure on the MBa65xx.

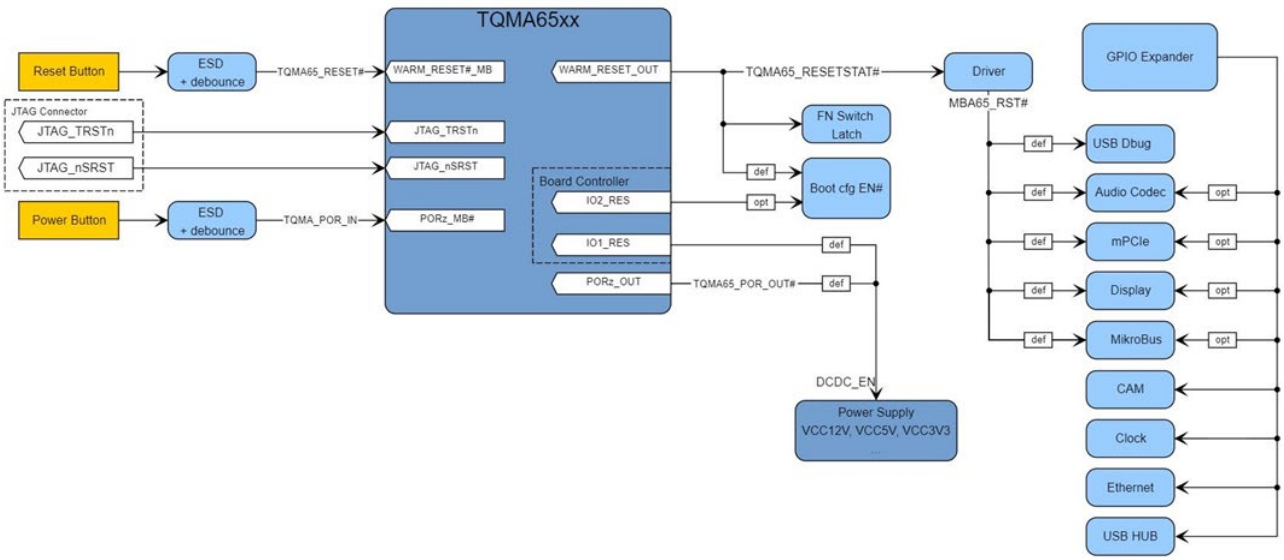

Figure 25: Block diagram Reset

For the MBa65xx different possibilities are available for a complete or partial reset of the module. The following table describes the signals used:

Table 49: Reset signals

Signal	Source	Type	Default	Note
TQMA65_POR_OUT#	TQMa65xx	O	Hi	Activated by the module during power sequencing and turns on the mainboard regulators for 3.3 V and 1.8 V.
CAM0_PWR#	GPIO expander	O	Lo	Enable for camera supply (1.8 V)
MPCIE_1V5_EN		O	Lo	Enable for 1.5 V supply for Mini PCIe
DISPLAY_3V3_EN		O	Lo	Enable for 3.3V supply for LVDS display
LCD_PWR_EN		O	Lo	Power Enable for external display
TQMA65_POR_IN#	Button	I	Hi	Hard Reset for the TQMa65xx. Triggers the power up sequencing
TQMA65_RESET#	Button	I	Hi	CPU Reset
TQMA65_RESETSTAT	TQMa65xx	O	Hi	The signal becomes Hi when the CPU is completely out of reset.
JTAG_TRSTn/JTAG_nSRST	JTAG connector	I		JTAG Reset signals
other	Port expander	O	Lo	See chapter 3.4

4. SOFTWARE

The TQMa65xx is supplied with a specially adapted bootloader, which is configured for use on an MBa65xx.
This bootloader includes module specific as well as board specific adaptations like e.g.

- CPU configuration
- RAM configuration
- RAM timing
- e-MMC configuration
- Muxing
- Clocks
- Pin configuration
- Driver strengths

When using a different bootloader, these data have to be adapted. More information can be found in the TQ-Support Wiki for the TQMa65xx.

5. MECHANICS

5.1 MBa65xx dimensions

The MBa65xx has overall dimensions (length × width) of 230 mm × 170 mm.
The MBa65xx has six 3.2 mm mounting holes for the housing, and four 3.7 mm mounting holes for a heat sink.
The MBa65xx mass is approximately 318 g without TQMa65xx.

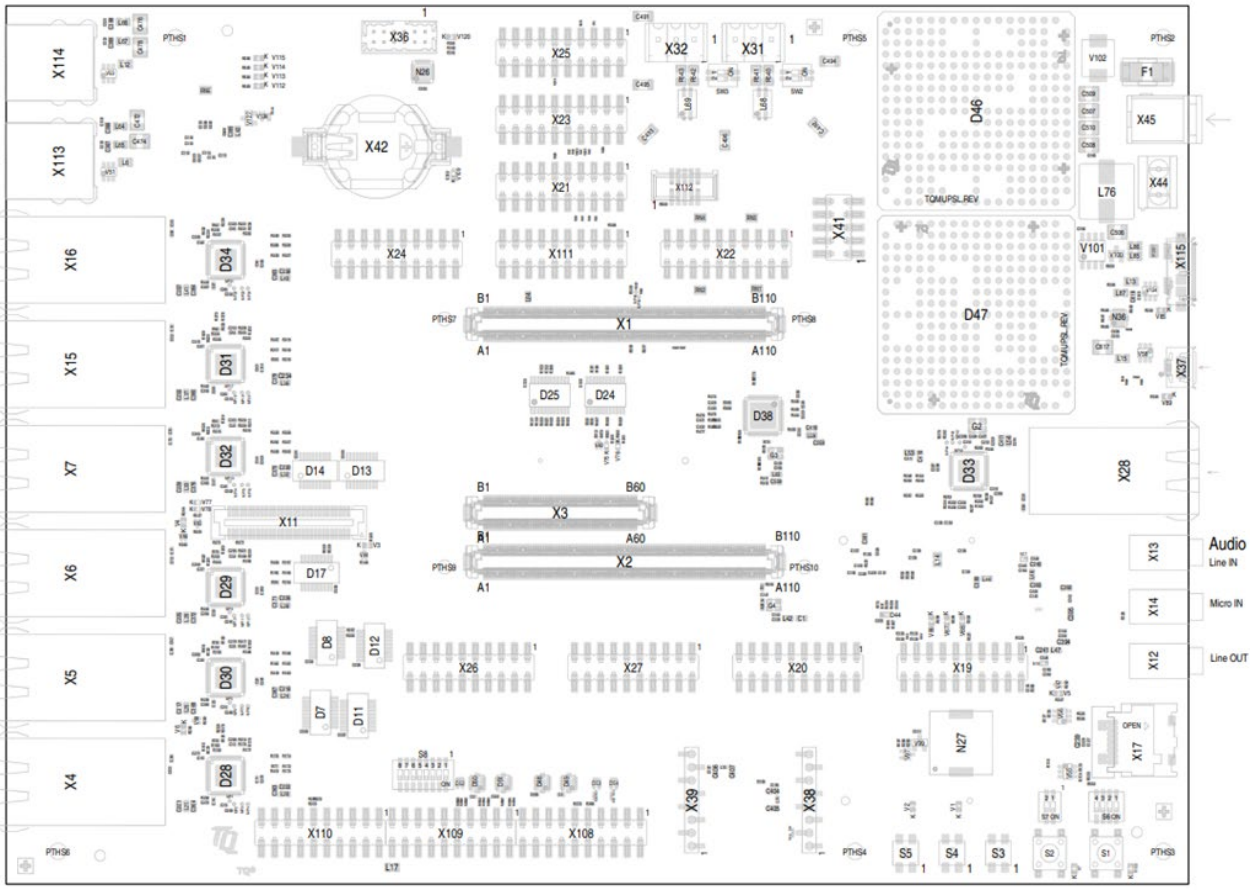

Figure 26: Assembly plan top side

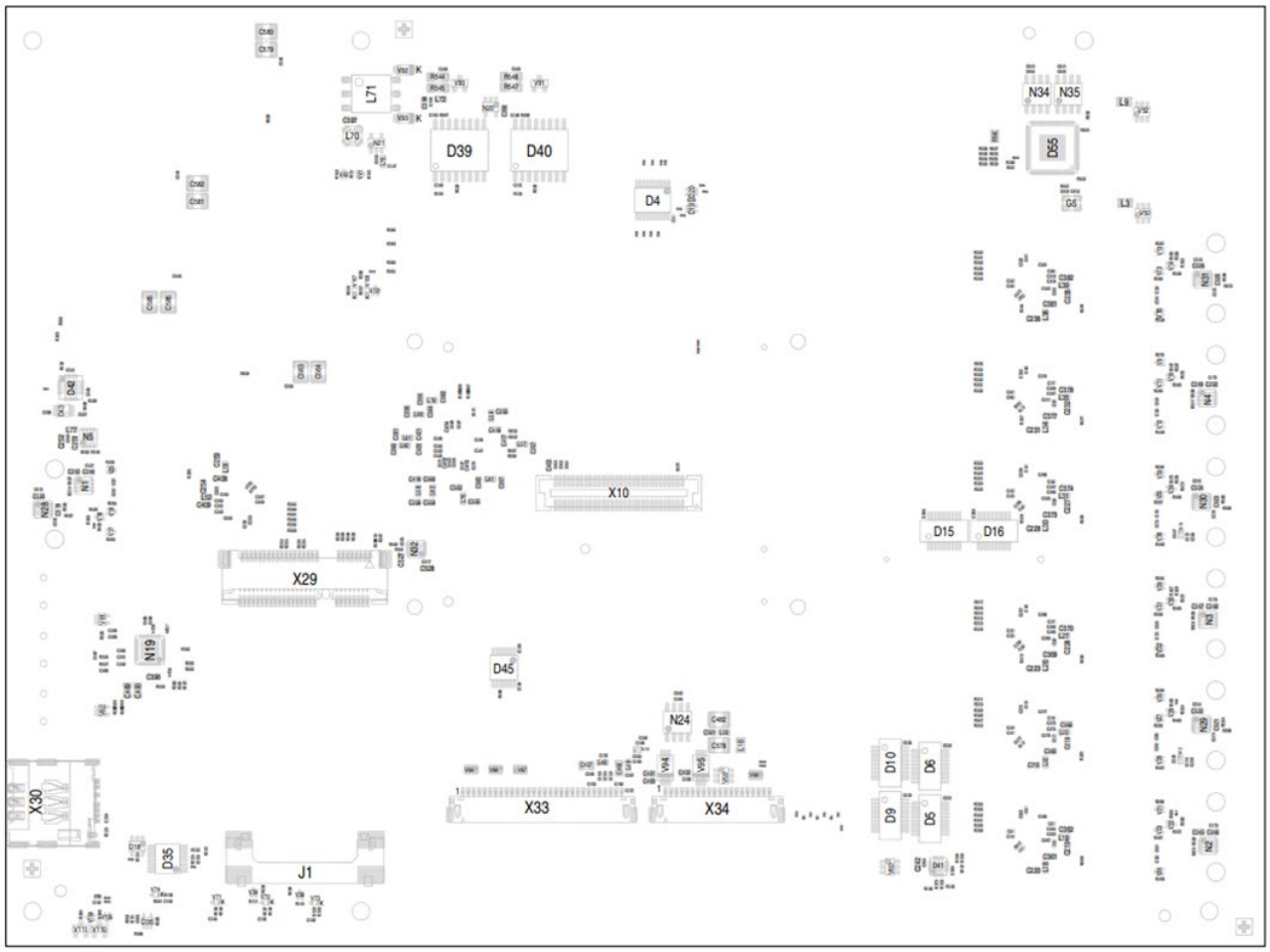

Figure 27: Assembly plan bottom side

5.2 Notes of treatment

To avoid damaging the TQMa65xx connectors as well as the carrier board connectors while removing the TQMa65xx the use of the extraction tool MOZI is strongly recommended. This extraction tool can be purchased separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBa65xx for the extraction tool MOZI.

5.3 Embedding in the target system

The MBa65xx serves as a design base for customer products, as well as a reference platform during development.

5.4 Protection against external influences

Protection class IP00 has been defined for the starter kit. This means that there is no protection against foreign objects, contact and moisture or water.

5.5 Thermal management

Up to 8.4 W are dissipated for the heat dissipation of the MBa65xx including the module when no other loads are operated. Further power dissipation mainly occurs at any additional externally connected loads (starter kit headers, PCIe slot, etc.).

The customer is responsible for dissipating this power loss in his application.

Attention: TQMa65xx heat dissipation	
	The AM65xx CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa65xx must be taken into consideration when connecting the heat sink. The TQMa65xx is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa65xx or the MBa65xx and thus malfunction, deterioration or destruction.

5.6 Labelling

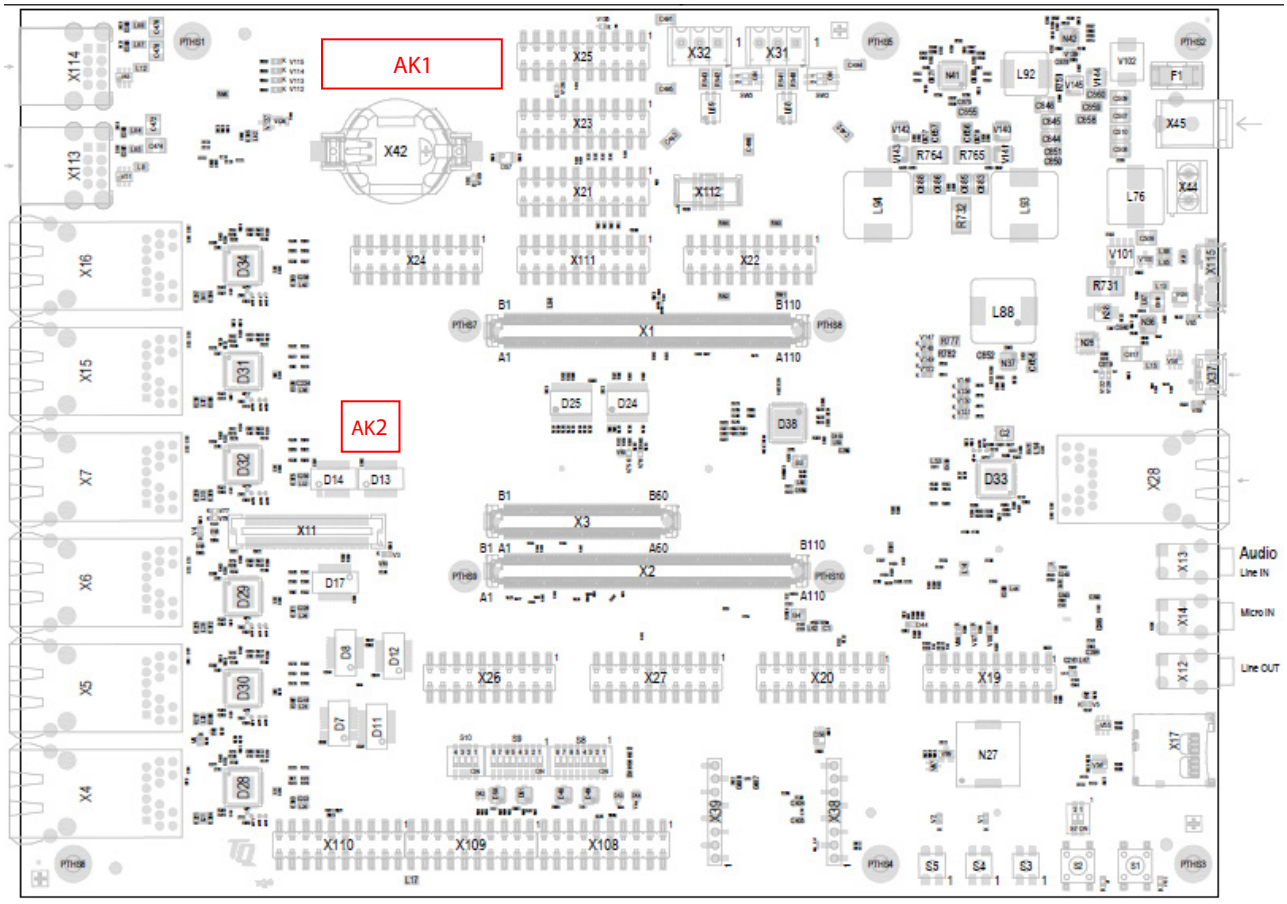

Figure 28: MBa65xx label position

The labels on the MBa65xx show the following information:

Table 50: Labels on MBa65xx

Label	Content
AK1	MBa65xx version and revision, tests performed
AK2	Serial number

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBa65xx is a development platform, no EMC tests have been performed.
During the development of the MBa65xx the standard DIN EN 55022:2010 limit class A was taken into account.

6.2 ESD

ESD protection is provided on most interfaces of the MBa65xx.
The MBa65xx schematics show, which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 51: Climatic and operational conditions MBa65xx

Parameter	Range	Remark
Ambient temperature	0 °C to +60 °C	With Lithium battery
	–40 °C to +85 °C	Without Lithium battery
Storage temperature	–40 °C to +100 °C	Without Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa65xx heat dissipation	
	The AM65xx CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa65xx must be taken into consideration when connecting the heat sink. The TQMa65xx is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa65xx and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa65xx. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa65xx.
The MBa65xx is designed to be insensitive to vibration and impact.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa65xx is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa65xx was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa65xx must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa65xx enable compliance with EuP requirements for the MBa65xx.

8.5 Packaging

The MBa65xx is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

For technical reasons a battery is necessary for the MBa65xx. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa65xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa65xx is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 52: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AI	Analog Input
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CLC	Capacitor-Inductor-Capacitor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communication
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
I_{PD}	Input with Pull-Down
I_{PU}	Input with Pull-Up
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures

9.1 Acronyms and definitions (continued)

Table 56: Acronyms (continued)

Acronym	Meaning
NAND	Not-And (flash memory)
(NC)	Not Connected
NOR	Not-Or
NP	Not Placed
O_{OD}	Open-Drain Output
O_{PD}	Output with Pull-Down
O_{PU}	Output with Pull-Up
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media-Independent Interface
SIM	Subscriber Identification Module
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 53: Further applicable documents

No.	Name	Rev., Date	Company
(1)	AM654x, AM652x Sitara™ Processors Silicon Revision 1.0 datasheet	26 July 2019	TI
(2)	AM65x/DRA80xM Processors Technical Reference Manual (Rev. E)	12 December 2019	TI
(3)	AM65x/DRA80xM Processors Silicon Revision 1.0 Errata (Rev. D)	23 December 2019	TI
(4)	TQMa65xx User's Manual	– current –	TQ-Systems
(5)	TQMa65xx Support Wiki	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

Technology in Quality