TQMLS10xxA
User's Manual

TQMLS10xxA UM 0108
24.09.2024

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	12.08.2019	Petz		First issue
0101	07.10.2019	Petz	All 1.9 Table 2 Table 4 4.7.2 4.9.1 4.12 10, 21 7.5 (5)	Hyperlinks updated, Links to TQMLS10xxA-specific BSPs added Link to PTXdist documentation removed, Link to Yocto documentation added Clarified and corrected Values added Reworked, Figure 9 added Information added Chapter added Footnotes added Updated Link to LS1043A Errata added
0102	29.11.2019	Petz	All Table 5 4.14.2	Links updated Clarified Chapters 4.14.2 to 4.14.5 merged
0103	02.11.2020	Petz	All 2 Table 17	Non-functional changes, links updated Cortex®-core naming corrected and description extended Link to LS1043A Errata removed
0104	18.11.2021	Kreuzer	Table 3 4.14.2	eMMC boot with all TQMLS10xxA variants possible Added references to CPU variants
0105	21.03.2022	Kreuzer	Table 2	Max. frequency corrected for LS1046A
0106	07.12.2023	Kreuzer	4.9.3	Resistor value corrected
0107	19.06.2024	Kreuzer	4.6 7.4, 7.5, 7.6, 7.7, 8.5	Chapter streamlined Chapter added
0108	24.09.2024	Kreuzer	1.4 2 4.9.4	Chapter moved Revision updated Internal Pull Up corrected

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMLS10xxA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.

The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLS10xxA circuit diagram
- MBLS10xxA User's Manual
- LS10xxA Data Sheets
- LS10xxA Reference Manuals
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMLS10xxA

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMLS10xxA, **Rev. 03xx** and refers to some software settings. A certain TQMLS10xxA derivative does not necessarily provide all features described in this User's Manual. This User's Manual does also not replace the NXP CPU Reference Manuals. The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMLS10xxA, and the BSP provided by TQ-Systems GmbH. See also chapter 6.

The TQMLS10xxA is a universal Minimodule based on the NXP Layerscape CPUs LS1043A / LS1046A / LS1088A. These Layerscape CPUs feature Dual Cortex®-A53 or Cortex®-A72 cores, Quad Cortex®-A53 or Cortex®-A72 cores, or octal Cortex®-A53 cores, with QorIQ technology. The TQMLS10xxA extends the TQ-Systems GmbH product range and offers an outstanding computing performance. A suitable CPU derivative (LS1043A / LS1046A / LS1088A) can be selected for each requirement. All essential CPU pins are routed to the TQMLS10xxA connectors. There are therefore no restrictions for customers using the TQMLS10xxA with respect to an integrated customised design. Furthermore all components required for the CPU to function like DDR4 SDRAM, eMMC, power supply and power management are integrated on the TQMLS10xxA. The main TQMLS10xxA characteristics are:

- CPU derivatives LS1043A (LS1023A), LS1046A (LS1026A), LS1088A
- DDR4 SDRAM with ECC
- eMMC and QSPI NOR flash
- Single supply voltage 5 V
- On-board RTC / EEPROM / temperature sensor

The MBLS10xxA also serves as carrier board and reference platform for the TQMLS10xxA.

3. OVERVIEW

3.1 Block diagram

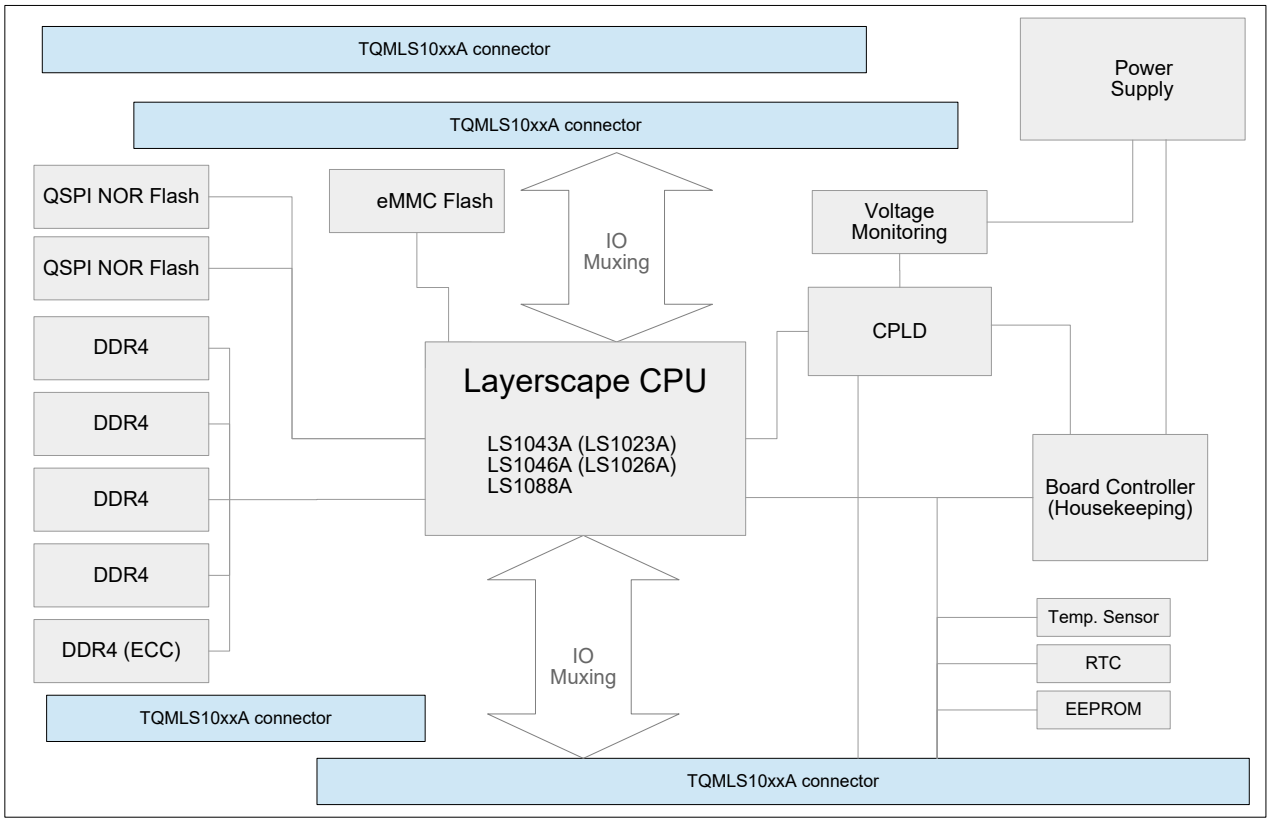


Figure 1: Block diagram TQMLS10xxA (simplified)

3.2 System components

The TQMLS10xxA provides the following key functions and characteristics:

- Layerscape CPUs LS1043A (LS1023A), LS1046A (LS1026A), LS1088A
- Oscillators
- Reset structure
- Power supply and power-sequencing
- Voltage supervision
- Housekeeping µController
- Temperature sensor
- RTC
- EEPROM
- DDR4 SDRAM with ECC
- QSPI NOR flash
- eMMC
- Four connectors (420 pins)

All essential CPU pins are routed to the TQMLS10xxA connectors. There are therefore no restrictions for customers using the TQMLS10xxA with respect to an integrated customised design.

All TQMLS10xxA versions are fully pin-compatible and therefore interchangeable. The functionality of the different TQMLS10xxA is mainly determined by the features provided by the respective CPU.

4. ELECTRONICS

4.1 LS10xxA

4.1.1 LS10xxA variants, block diagrams

The LS10xxA module family is available with three variants of the LS10xxA CPUs from NXP.

The following block diagrams illustrate the differences between the CPUs:

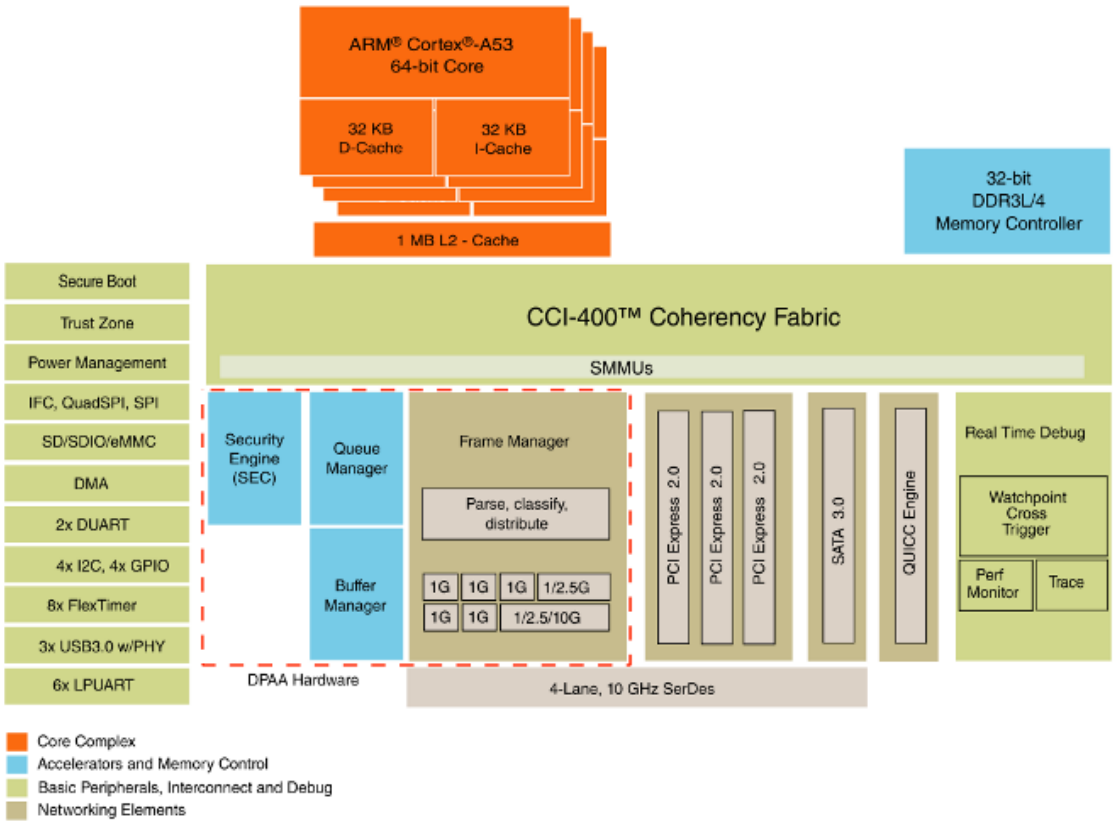


Figure 2: Block diagram LS1043A (Quad Cortex®-A53)
(Source: NXP)

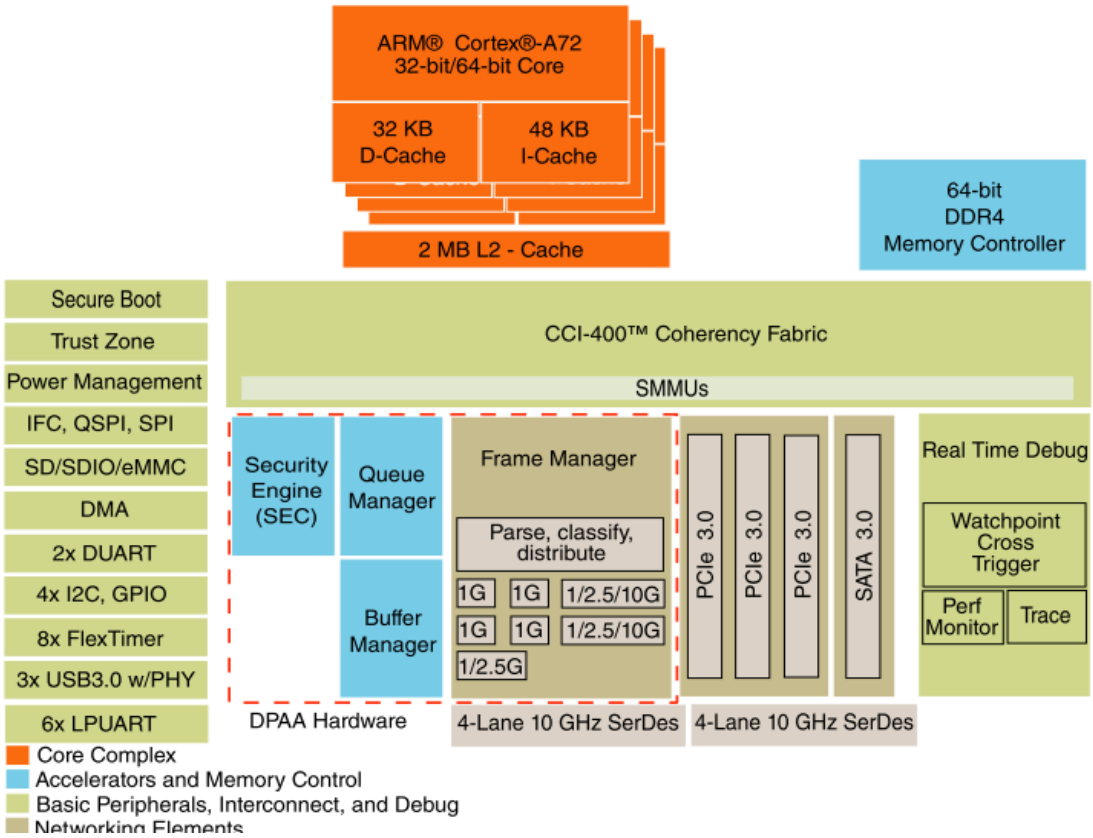


Figure 3: Block diagram LS1046A (Quad Cortex®-A72)
(Source: NXP)

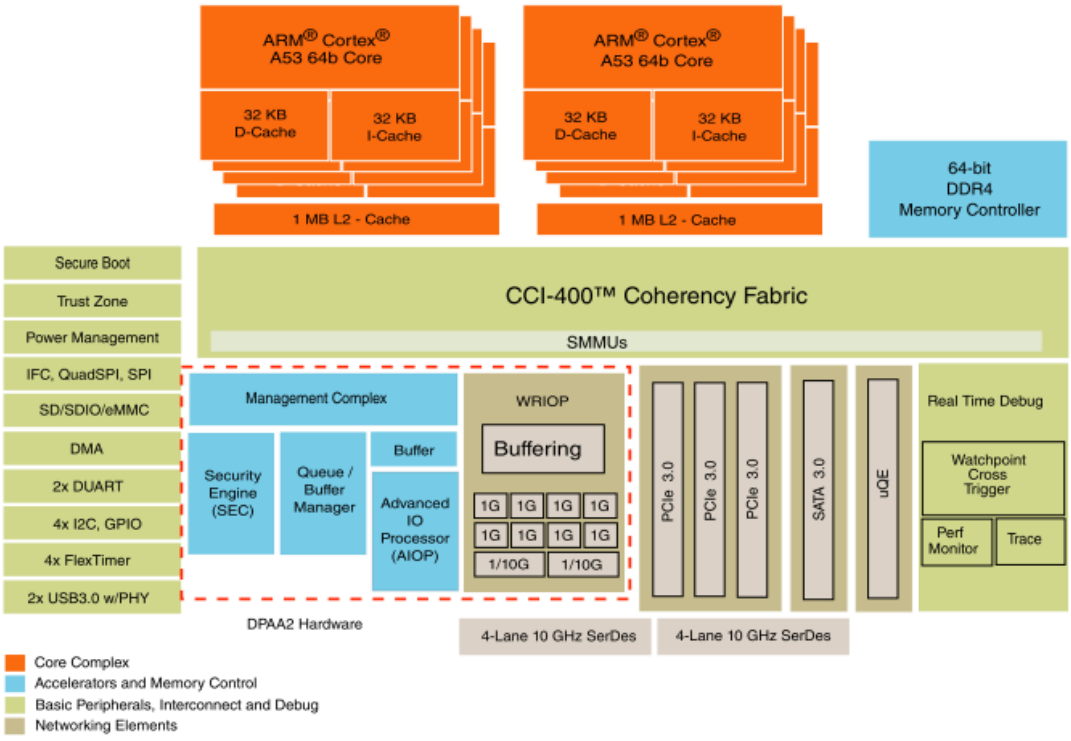


Figure 4: Block diagram LS1088A (Octal Cortex®-A53)
(Source: NXP)

4.1.2 LS10xxA variants, details

The following table shows the features provided by the different variants.
Fields with a red background indicate differences; fields with a green background indicate compatibility.

Table 2: LS10xxA variants

Feature	LS1043A	LS1046A	LS1088A
Cores			
Number of cores	4 × A53 Cortex® v8	4 × A72 Cortex® v8	8 × A53 Cortex® v8
Bus width	64-bit	64-bit	64-bit
Max. frequency (MHz)	up to 1600	up to 1800	up to 1600
Memory Size			
L1 cache	32 kB I/D	32 kB D cache/ 48 kB I Cache	32 kB I/D
L2 cache	Shared 1 MB	Shared 2 MB	Shared 2 × 1 MB
Main memory type	1 × DDR3L/4, 1600 MT/s	1 × DDR4, 2100 MT/s	1 × DDR4, 2100 MT/s
Max. memory size	1 TB (40-bit address)	1 TB (40-bit address)	1 TB (40-bit address)
Interconnect			
CCI 400	400 MHz	600 MHz	700 MHz
I/O			
Ethernet controllers	1 × 10 Gbit/s XFI; 1 × QSGMII; 4 × 1 Gbit/s SGMII; 2 × 2.5 Gbit/s SGMII 2 × RGMII	2 × 10 Gbit/s XFI; 1 × QSGMII; 5 × 1 Gbit/s SGMII; 3 × 2.5 Gbit/s SGMII 2 × RGMII	2 × 10 Gbit/s XFI; 2 × QSGMII; 4 × 1 Gbit/s SGMII; 2 × 2.5 Gbit/s SGMII 2 × RGMII
SerDes lanes	4 lanes at up to 10 GHz	8 lanes at up to 10 GHz	8 lanes at up to 10 GHz
PCI Express controllers	3 × Gen 2.0 controllers; 5 Gbit/s Root complex supported, ×4, ×2, and ×1 link widths	3 × Gen 3.0 controllers; 8 Gbit/s Root complex or end point supported, ×4, ×2, and ×1 link widths	3 × Gen 3.0 controllers; 8 Gbit/s Root complex or end point supported, ×4, ×2, and ×1 link widths
SATA	1 × SATA controller up to 6.0 Gbit/s	1 × SATA controller up to 6.0 Gbit/s	1 × SATA controller up to 6.0 Gbit/s
USB	3 × USB 3.0 controllers; 5 Gbit/s	3 × USB 3.0 controllers; 5 Gbit/s	2 × USB 3.0 controllers; 5 Gbit/s
QE	HDLC, Transparent UART, TDM/SI	Not supported	HDLC, Transparent UART, TDM/SI
Integrated Flash Controller (IFC)	8-/16-bit data width, 28-bit address width	8-/16-bit data width, 28-bit address width	8-/16-bit data width, 28-bit address width
Other peripherals	1 × eSDHC; 1 × QSPI; 1 × SPI; 4 × I²C; 2 × DUART; 6 × LPUART; 8 × FlexTimer	1 × eSDHC; 1 × QSPI; 1 × SPI; 4 × I²C; 2 × DUART; 6 × LPUART; 8 × FlexTimer	1 × eSDHC; 1 × QSPI; 1 × SPI; 4 × I²C; 2 × DUART; 4 × FlexTimer
Clocking			
Single source clocking	DIFF_SYSCLK/ DIFF_SYSCLK_B with LVDS receiver	DIFF_SYSCLK/ DIFF_SYSCLK_B with LVDS receiver	DIFF_SYSCLK/ DIFF_SYSCLK_B with HCSL receiver
Package			
Package	23 mm × 23 mm, 0.8 mm pitch, 780-pin FC-PBGA Unlidded	23 mm × 23 mm, 0.8 mm pitch, 780-pin FC-PBGA Unlidded	23 mm × 23 mm, 0.8 mm pitch, 780-pin FC-PBGA Lidded

4.2 Reset Configuration Word RCW

The Reset Configuration Word RCW can be taken from the LS1043A / LS1046A / LS1088A Reference Manuals (1).

4.3 RCW source selection

On the TQMLS10xxA the RCW source selection is controlled by a CPLD. An external pin strapping is not required.

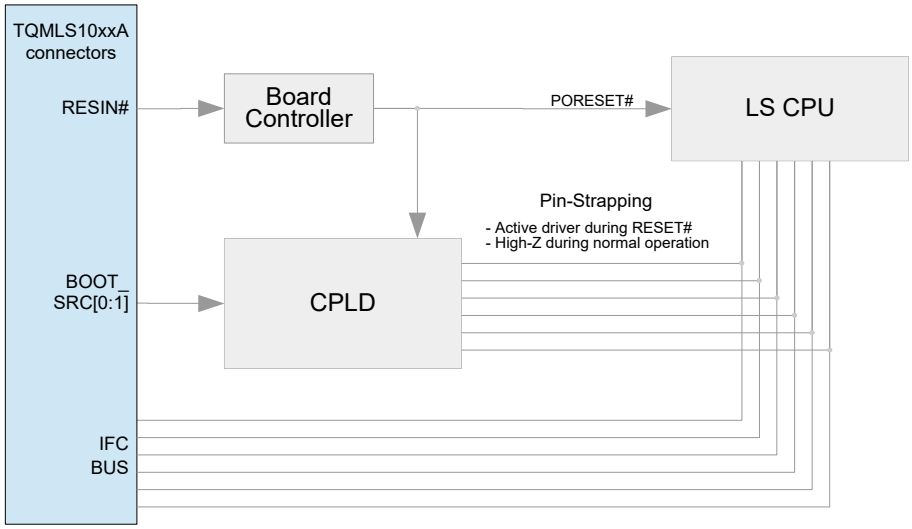


Figure 5: Block diagram RCW source selection

The boot source is selected with signals BOOT_CFG[1:0].

Table 3: RCW source selection

BOOT_CFG1	BOOT_CFG0	RCW Source
Low	Low	QSPI NOR Flash
Low	High	I^2C (LS1088A only)
High	Low	SDHC
High	High	eMMC

BOOT_CFG[1:0] is initialized with a Pull-Up to 3.3V on the TQMLS10xxA.
After the TQMLS10xxA is powered-up, the CPLD applies the pin strapping.

4.4 Clock supply

The clock supply on the TQMLS10xxA corresponds to the structure „Multiple Reference clocking“, described in (1).

- SYSCLK = 100 MHz
- DDRCLK = 100 MHz (LS1043A, LS1046A), 133.33 MHz (LS1088A)
- ECx_GTX_CLK125 is not generated on the TQMLS10xxA, has to be generated externally.
- Differential SERDES clocks are not generated on the TQMLS10xxA, have to be generated externally.

4.5 Power Modes

Currently no power modes are implemented.

4.6 JTAG

The JTAG interface is routed to the connectors. Signals TMS, and TRST# have 10 kΩ Pull-Ups to 1.8 V on the TQMLS10xxA.

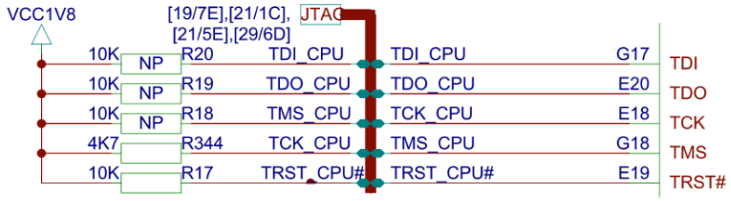


Figure 6: Block diagram JTAG interface

Signal TRST_CPU# is connected with PORESET# by resistors. TRST# is pulled at the same time as PORESET#, but can also be pulled Low using an external debugger, while PORESET# remains unchanged.

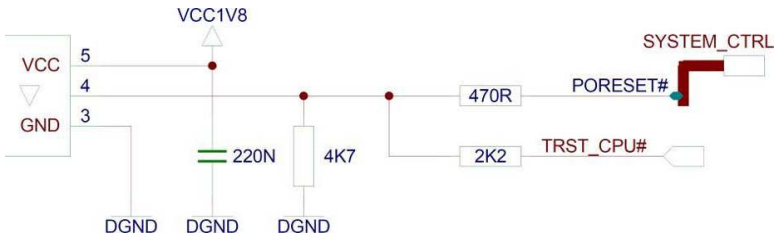


Figure 7: Wiring of JTAG_TRST# and PORESET#

4.7 Power supply

4.7.1 Input voltage

The TQMLS10xxA requires a 5 V supply with a maximum tolerance of ±5 %.

4.7.2 Feedback voltages

The voltages DVDD, LVDD, TVDD, and VCCGPIIN can be fed back according to customer requirements:

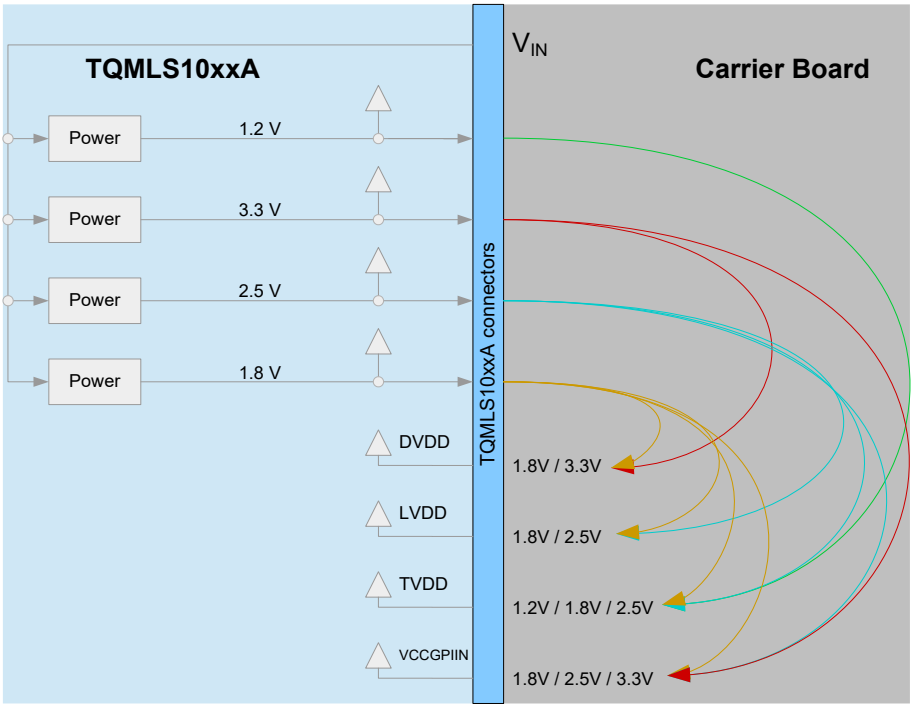


Figure 8: Block diagram feedback voltages

The TQMLS10xxA provides the respective voltages in order to enable a simple connection according to customer requirements on the carrier board. The voltages generated on the TQMLS10xxA may only be used for the TQMLS10xxA itself. Further loads by external circuitry on a carrier board are not permitted and may lead to supply and monitoring errors.

Voltage EVDD is switched on the TQMLS10xxA:

- EVDD = 3.3V if SDHC_EXT_SEL = 1 (SD card)
- EVDD = 1.8V if SDHC_EXT_SEL = 0 (eMMC)

4.7.3 Power-up sequencing

The power-up sequencing is executed and monitored by the TQMLS10xxA.PORESET# is kept Low during power-up.

4.7.4 Voltage monitoring

All voltages generated on the TQMLS10xxA are monitored.

4.7.5 Power consumption

The given power consumptions have to be seen as typical values. The power consumption of the TQMLS10xxA strongly depends on the application, the mode of operation, the environmental temperature, and the operating system.

The power supply of the carrier board should be designed for an output power of 18 to 20 watts.

The following table shows typical power consumption of the TQMLS10xxA under various operating conditions.

Table 4: TQMLS10xxA power consumption @ 5 V

Mode of operation	TQMLS1043A	TQMLS1046A	TQMLS1088A	$T_{environment}$
U-Boot, idle	4.08 W	7 W	8.64 W	+25 °C
U-Boot, memory test	4.24 W	8.4 W	9.44 W	
Linux, idle	3.92 W	7.1 W	8 W	
Linux, 100 % CPU load	6 W (1)	11.9 W (2)	12.32 W (3)	
U-Boot, idle	5.76 W	11.6 W	12.76 W	+85 °C
U-Boot, memory test	6.72 W	14.2 W	15.72 W	
Linux, 100 % CPU load	8.05 W (1)	15.6 W (2)	18.9 W (3)	

Attention: Destruction or malfunction, TQMLS10xxA heat dissipation	
	The TQMLS10xxA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LS10xxA must be taken into consideration when connecting the heat sink, see (2). The LS10xxA is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMLS10xxA and thus malfunction, deterioration or destruction.

1: `stressapptest -s 3600 -M 700 -m 4 -C 4 -i 4`
2: `stressapptest -s 3600 -M 1024 -m 4 -C 4 -i 4`
3: `stressapptest -s 3600 -M 512 -m 4 -C 4 -i 4`

4.8 Reset structure

If RESIN# is disabled, the Board Controller starts the initialization of the TQMLS10xxA.
If no errors occur during initialization and when power supplies are OK, the CPU is started via PORESET#.
RESET# is provided at the TQMLS10xxA connector via signal RESET_OUT#.
PORESET# should not be connected at the TQMLS10xxA connector.
A red LED (V26) signals the RESET# state.
HRESET# of the CPU is directly available at the TQMLS10xxA connector (4.7 kΩ Pull-Up to 1.8 V).
CPU signal RESET_REQ# is processed by the Board Controller and routed to the TQMLS10xxA connectors.

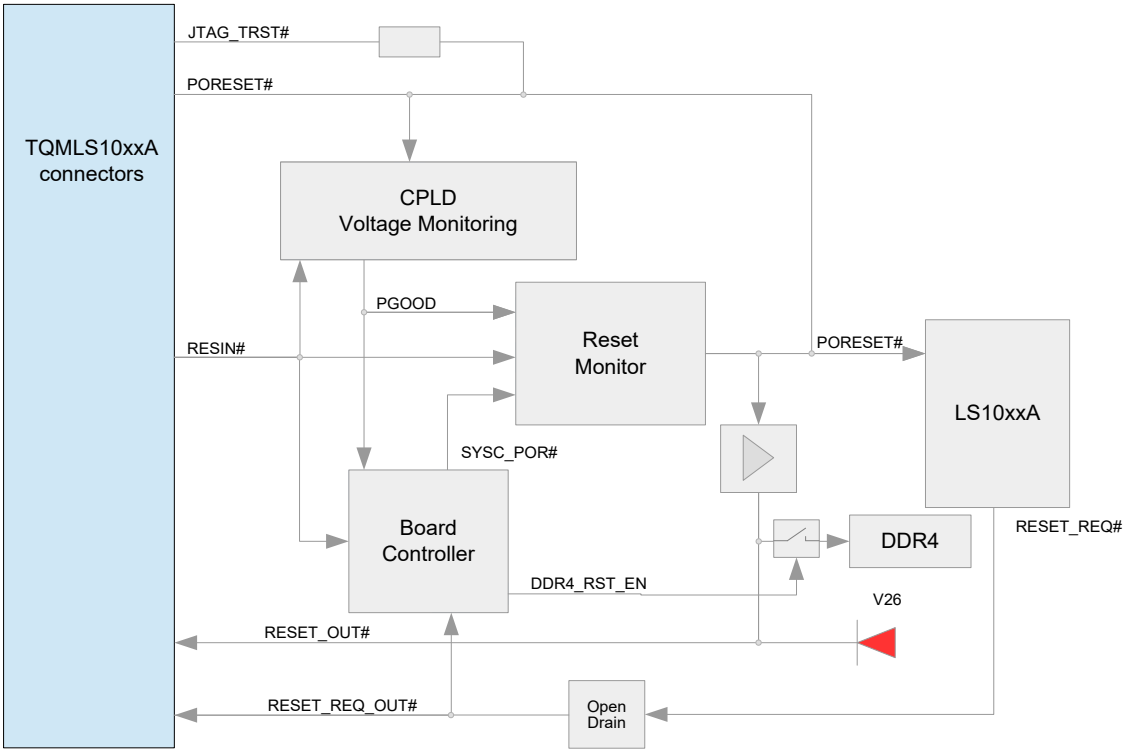


Figure 9: Block diagram Reset structure

- RESIN# keeps the TQMLS10xxA in RESET#
- Further RESET# sources are:
  - By software via Board Controller
  - By software via CPU RESET_REQ
  - V_{IN} Power Fail

Table 5: RESET options

Wiring at RESIN#	Reset function
Open Drain	Self-reset possible Logic Low at RESIN# triggers RESET
Open, or Pull-Up ≥47 kΩ to VCC3V3	Self-reset possible RESET_REQ_OUT# can trigger RESIN# on TQMLS10xxA
Pull-Up <10 kΩ to VCC3V3	**No** self-reset possible RESET_REQ_OUT# cannot trigger RESIN# on TQMLS10xxA
Push/Pull driver	**No** self-reset, but external RESET possible Logic High at RESIN# overrides RESET_REQ_OUT# on TQMLS10xxA

4.9 Memory

4.9.1 DDR4 SDRAM

Depending on the CPU derivative, the TQMLS10xxA supports up to 8 Gbyte DDR4 SDRAM.
ECC is optionally available and is assembled as an additional DDR4 SDRAM component.

4.9.2 SPI NOR flash

Up to two QSPI NOR flash devices can be assembled on the TQMLS10xxA.

4.9.3 EEPROM, 24LC256

A 24LC256 series EEPROM with 256 Kbit (32 kB × 8 bit) is assembled on the TQMLS10xxA.
Write Protection can be controlled by

- CPLD
- Board Controller
- USRGPIO pin

A 100 kΩ Pull-Down is assembled on the TQMLS10xxA, thus write access is permitted.
Write protection is controlled by the CPLD. Write_Protect# of the EEPROM is not connected directly to the TQMLS10xxA connectors, but can be controlled indirectly via USR_GPIO_1.

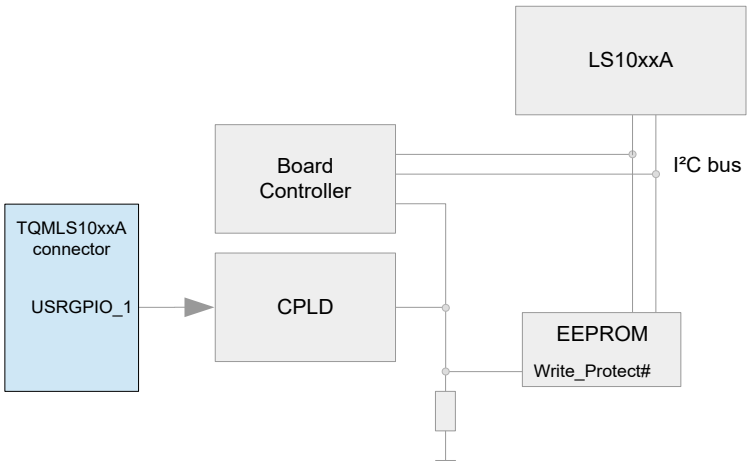


Figure 10: Block diagram 24LC256 EEPROM interface

4.9.4 eMMC

The LS10xxA derivatives provide only one SDHC controller. Therefore the SD card interface cannot be used when an eMMC is assembled on the TQMLS10xxA. Hence the SDHC interface is routed to the TQMLS10xxA connectors and can be enabled with the SDHC_EXT_SEL control signal. A Pull- Up (FPGA internal Pull Up) on the TQMLS10xxA activates the eMMC on the TQMLS10xxA by default.

Table 6: SDHC_EXT_SEL options

SDHC_EXT_SEL	Configuration
High	External SDHC
Low	On-board eMMC

4.10 Temperature sensor with EEPROM, SE97B

4.10.1 Temperature sensor, SE97B

A temperature sensor SE97B is assembled on the TQMLS10xxA, which measures the environmental temperature.

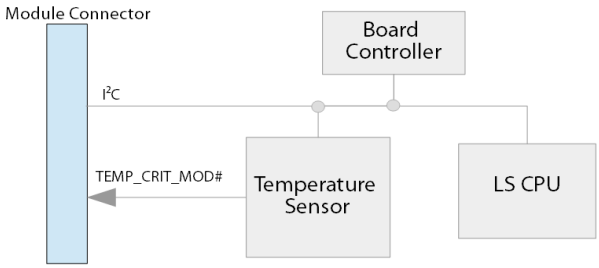


Figure 11: Block diagram SE97B temperature sensor

➢ The temperature sensor has I²C address `0x18 / 001 1000b`

The accuracy of the temperature sensor is as follows:

- Max. ±1 °C between +75 °C and +95 °C
- Max. ±2 °C between +40 °C and +125 °C
- Max. ±3 °C between –40 °C and +125 °C

Signal TEMP_CRIT_MOD# of the temperatures sensor is routed to the TQMLS10xxA connector. It provides a warning at a programmed trigger level. During power-up the sensor is configured to T_CRIT_LOKAL = +95 °C by the Board Controller. This value can be overwritten by the boot loader, the operating system, or the application.
The signal has an Open Drain output, a Pull-Up to 3.3 V is provided on the TQMLS10xxA.

4.10.2 EEPROM, SE97B

The SE97B also contains a 2 Kbit (256 × 8 Bit) EEPROM. The EEPROM is divided into two parts.
The lower 128 bytes (00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software.
The upper 128 bytes (80h to FFh) are not write protected and can be used for general purpose data storage.

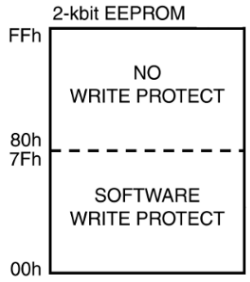


Figure 12: Memory Map SE97B EEPROM

The EEPROM can be accessed with the following two I²C addresses.

- EEPROM (Normal Mode): `0x50 / 101 0000b`
- EEPROM (Protected Mode): `0x30 / 011 0000b`

4.11 RTC

An RTC type PCF85063A is assembled. RTC signal CLKOUT (32 kHz) is routed to the TQMLS10xxA connector (X2-118).

RTC signal INT# can be used in several ways:

- External use: Signal is accessible at the TQMLS10xxA connector, Pull-Up to 3.3 V on the TQMLS10xxA.
- The signal is also available on the Board Controller for wake-up.

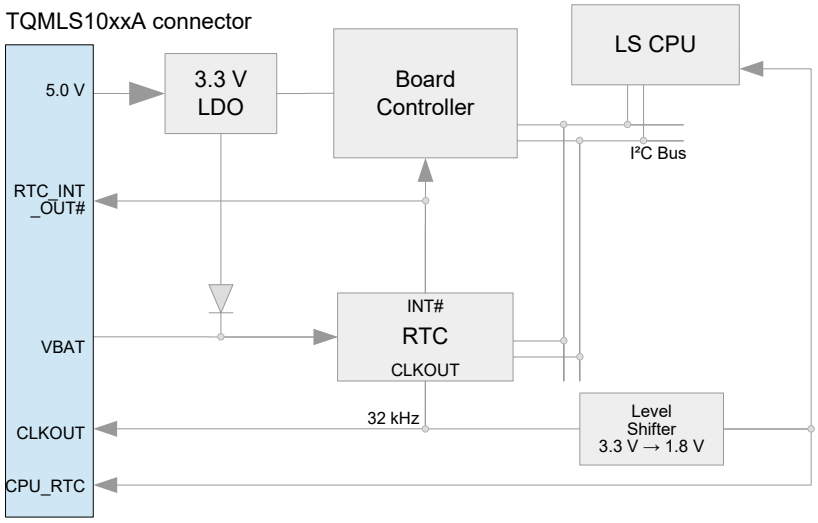


Figure 13: Block diagram RTC interface

➢ The RTC has I²C address `0x51 / 101 0001b`

The RTC is clocked with a 32.768 kHz crystal with an accuracy of ±20 ppm at +25 °C. This equals to a maximum deviation of 1.7 seconds per day. The accuracy at +85 °C is ±30 ppm. This equals to a maximum deviation of 2.6 seconds per day. The RTC is supplied by VBAT. A GoldCap® or a battery is required.

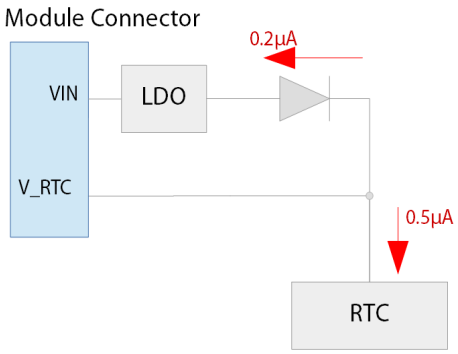


Figure 14: Block diagram RTC buffering interface

4.12 UART

It is recommended to assemble 4.7 kΩ Pull-Ups at the UART_SOUT signals on the carrier board.
For details contact TQ-Support.

4.13 I²C bus

The I²C devices on the TQMLS10xxA are connected to the I2C1 bus.

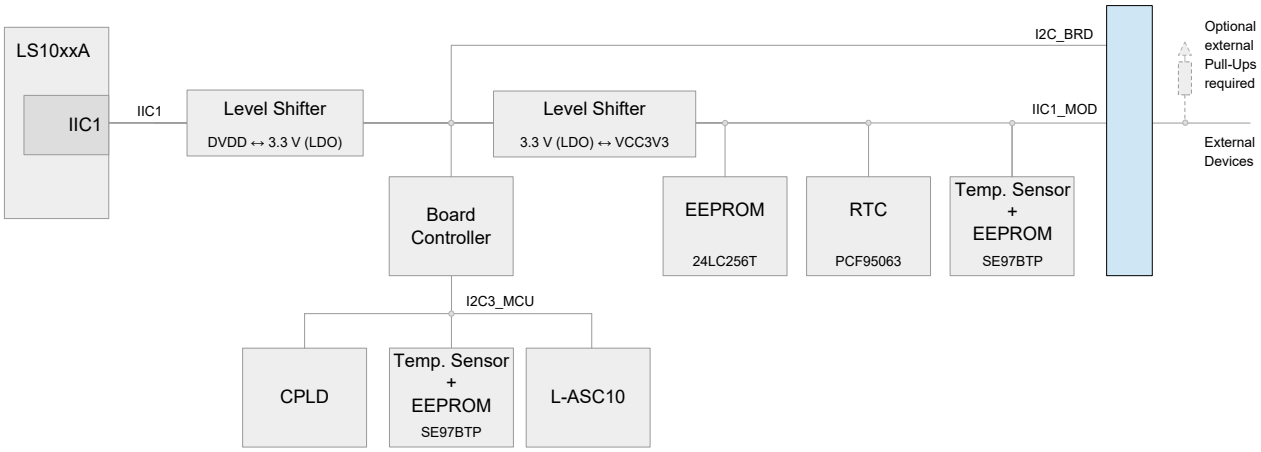


Figure 15: Block diagram I²C bus 1 structure on TQMLS10xxA

4.7 kΩ Pull-Ups at the I²C bus are assembled on the TQMLS10xxA. More devices can be connected to the bus but then additional external Pull-Ups may be required on account of the higher capacitive load.

Table 7: I²C addresses

Device	Function	7-bit address	Remark
Connected to Board Controller, not accessible			
L-ASC10	Voltage Monitoring	0x60 / 110 0000b	–
MachX03	CPLD	(n.a.)	–
SE97B	Temperature sensor	0x1B / 001 1011b	Access to temperature registers
	EEPROM	0x53 / 101 0011b	R/W access in Normal Mode
	EEPROM	0x33 / 011 0011b	R/W access in Protected Mode
Connected to LS10xxA, accessible			
24LC256	EEPROM	0x57 / 101 0111b	–
STM32	Board Controller	0x11 / 001 0001b	Should not be altered
PCF85063A	RTC	0x51 / 101 0001b	–
SE97B	Temperature sensor	0x18 / 001 1000b	Access to temperature registers
	EEPROM	0x50 / 101 0000b	R/W access in Normal Mode
	EEPROM	0x30 / 011 0000b	R/W access in Protected Mode

4.14 TQMLS10xxA interfaces

4.14.1 Pin multiplexing

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The pin assignment listed in Table 8 to Table 11 refer to the corresponding standard BSPs of TQ-Systems GmbH in combination with the Starterkit MBLS10xxA. For standard BSPs, see 1.9.

Attention: Destruction or malfunction	
	Depending on the configuration many CPU pins can provide several different functions. Please take note of the information concerning the configuration of these pins in (1), before integration or start-up of your carrier board / Starterkit.

4.14.2 Pinout TQMLS10xxA connectors

The following Table 8 describes the TQMLS10xxA connectors pinout for the CPU variant LS1046A. The partly differing pinouts with the CPU variants LS1043A and LS1088A are described in the TQMLS10xxA Design Checklist, which is available on request from the TQ-Support.

Table 8: Pinout connector X1

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
		5 V	Power	VIN	1	2	VIN	Power	5 V		
		5 V	Power	VIN	3	4	VIN	Power	5 V		
		5 V	Power	VIN	5	6	VIN	Power	5 V		
		5 V	Power	VIN	7	8	VIN	Power	5 V		
		5 V	Power	VIN	9	10	VIN	Power	5 V		
		5 V	Power	VIN	11	12	VIN	Power	5 V		
		5 V	Power	VIN	13	14	VIN	Power	5 V		
		5 V	Power	VIN	15	16	VIN	Power	5 V		
		5 V	Power	VIN	17	18	VIN	Power	5 V		
		5 V	Power	VIN	19	20	VIN	Power	5 V		
		5 V	Power	VIN	21	22	VIN	Power	5 V		
		0 V	Ground	DGND	23	24	DGND	Ground	0 V		
		0 V	Ground	DGND	25	26	DGND	Ground	0 V		
		0 V	Ground	DGND	27	28	DGND	Ground	0 V		
		0 V	Ground	DGND	29	30	DGND	Ground	0 V		
		0 V	Ground	DGND	31	32	DGND	Ground	0 V		
		0 V	Ground	DGND	33	34	DGND	Ground	0 V		
		0 V	Ground	DGND	35	36	DGND	Ground	0 V		
		3.0 V	Power	VBAT	37	38	VCC1V8	Power	1.8 V		
		1.8 V	Power	VCC1V8	39	40	VCC3V3	Power	3.3 V		
		1.8 V	Power	VCC1V8	41	42	VCC3V3	Power	3.3 V		
		1.8 V	Power	VCC1V8	43	44	VCC1V2_MOD	Power	1.2 V		
		1.2 V	Power	VCC1V2_MOD	45	46	NC	NC	–		
		1.2 V	Power	VCC1V2_MOD	47	48	NC	NC	–		
		2.5 V	Power	VCC2V5	49	50	LVDDIN	Power	1.8 / 2.5 / 3.3 V		
		2.5 V	Power	VCC2V5	51	52	LVDDIN	Power	1.8 / 2.5 / 3.3 V		
		1.8 / 2.5 / 3.3 V	Power	VCCGPIIN	53	54	LVDDIN	Power	1.8 / 2.5 / 3.3 V		
		1.8 / 2.5 / 3.3 V	Power	VCCGPIIN	55	56	DVDD	Power	1.8 / 2.5 / 3.3 V		
		1.2 / 1.8 / 2.5 V	Power	TVDD	57	58	DVDD	Power	1.8 / 2.5 / 3.3 V		
		1.2 / 1.8 / 2.5 V	Power	TVDD	59	60	DGND	Ground	0 V		
		0 V	Ground	DGND	61	62	USR_GPIO_6	SYSTEM	1.8 / 2.5 / 3.3 V (4)	I	–
–	I	1.8 / 2.5 / 3.3 V (4)	SYSTEM	USR_GPIO_7	63	64	DGND	Ground	0 V		
–	–	3.3 V	Factory Test	I2C_BRD_SDA	65	66	BCTL_UARTx_TX	Factory Test	–	O	–
–	–	3.3 V	Factory Test	I2C_BRD_SCL	67	68	BCTL_UARTx_RX	Factory Test	–	I	–
		0 V	Ground	DGND	69	70	DGND	Ground	0 V		
B8	I/O	1.8 V (5)	IFC	IFC_AD00	71	72	USR_GPIO_1	SYSTEM	1.8 / 2.5 / 3.3 V (4)	I	–
A8	I/O	1.8 V (5)	IFC	IFC_AD01	73	74	USR_GPIO_2	SYSTEM	1.8 / 2.5 / 3.3 V (4)	I	–
B9	I/O	1.8 V (5)	IFC	IFC_AD02	75	76	USR_GPIO_3	SYSTEM	1.8 / 2.5 / 3.3 V (4)	I	–
A9	I/O	1.8 V (5)	IFC	IFC_AD03	77	78	USR_GPIO_4	SYSTEM	1.8 / 2.5 / 3.3 V (4)	I	–
A10	I/O	1.8 V (5)	IFC	IFC_AD04	79	80	USR_GPIO_5	SYSTEM	1.8 / 2.5 / 3.3 V (4)	I	–
B11	I/O	1.8 V (5)	IFC	IFC_AD05	81	82	DGND	Ground	0 V		
A11	I/O	1.8 V (5)	IFC	IFC_AD06	83	84	IFC_PERR#	IFC	1.8 V (5)	I/O	E17
B12	I/O	1.8 V (5)	IFC	IFC_AD07	85	86	IFC_PAR0	IFC	1.8 V (5)	I/O	B18
		0 V	Ground	DGND	87	88	IFC_PAR1	IFC	1.8 V (5)	I/O	D17
A12	I/O	1.8 V (5)	IFC	IFC_AD08	89	90	IFC_NDDQS	IFC	1.8 V (5)	I/O	B17
A13	I/O	1.8 V (5)	IFC	IFC_AD09	91	92	DGND	Ground	0 V		
B14	I/O	1.8 V (5)	IFC	IFC_AD10	93	94	IFC_AVD	IFC	1.8 V (5)	O	A18
A14	I/O	1.8 V (5)	IFC	IFC_AD11	95	96	IFC_BCTL	IFC	1.8 V (5)	O	E15
B15	I/O	1.8 V (5)	IFC	IFC_AD12	97	98	IFC_CLE	IFC	1.8 V (5)	I/O	C19
A15	I/O	1.8 V (5)	IFC	IFC_AD13	99	100	DGND	Ground	0 V		
A16	I/O	1.8 V (5)	IFC	IFC_AD14	101	102	IFC_CLK0	IFC	1.8 V (5)	O	A20
A17	I/O	1.8 V (5)	IFC	IFC_AD15	103	104	DGND	Ground	0 V		
		0 V	Ground	DGND	105	106	IFC_CLK1	IFC	1.8 V (5)	O	B20
C16	I	1.8 V (5)	IFC	IFC_RB0#	107	108	DGND	Ground	0 V		
D16	I	1.8 V (5)	IFC	IFC_RB1#	109	110	IFC_CS0#	IFC	1.8 V (5)	O	C17
E14	O	1.8 V (5)	IFC	IFC_TE	111	112	IFC_CS1#	IFC	1.8 V (5)	I/O	A19
C15	O	1.8 V (5)	IFC	IFC_WE0#	113	114	IFC_CS2#	IFC	1.8 V (5)	I/O	D20
D19	O	1.8 V (5)	IFC	IFC_WP0#	115	116	IFC_CS3#	IFC	1.8 V (5)	I/O	C20
E16	O	1.8 V (5)	IFC	IFC_NDDDR_CLK	117	118	IFC_OE#	IFC	1.8 V (5)	I/O	C18
		0 V	Ground	DGND	119	120	DGND	Ground	0 V		

4: VCCGPIIN (X1-53, 55)
5: OVDD

4.14.2 Pinout TQMLS10xxA connectors (continued)

Table 9: Pinout connector X2

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
		0 V	Ground	DGND	1	2	DGND	Ground	0 V		
F11	I	1.8 V (6)	IRQ	IRQ0	3	4	IRQ2	IRQ	1.8 V (6)	I	H7
F15	I	1.8 V (6)	IRQ	IRQ1	5	6	IRQ11	IRQ	1.8 / 2.5 V (7)	I/O	W3
		0 V	Ground	DGND	7	8	DGND	Ground	0 V		
M5	I/O	1.8 / 3.3 V (8)	IRQ	FTM3_CH4	9	10	FTM3_CH0	IRQ	1.8 / 3.3 V (8)	I/O	J4
N5	I/O	1.8 / 3.3 V (8)	IRQ	FTM3_CH5	11	12	FTM3_CH1	IRQ	1.8 / 3.3 V (8)	I/O	J5
P4	I/O	1.8 / 3.3 V (8)	IRQ	FTM3_CH6	13	14	FTM3_CH2	IRQ	1.8 / 3.3 V (8)	I/O	K5
J3	I/O	1.8 / 3.3 V (8)	IRQ	FTM3_CH7	15	16	FTM3_CH3	IRQ	1.8 / 3.3 V (8)	I/O	L5
F5	I	–	USB	USB1_ID	17	18	DGND	Ground	0 V		
E7	I	–	USB	USB1_VBUS	19	20	DGND	Ground	0 V		
		0 V	Ground	DGND	21	22	USB1_TX_P	USB	–	O	F1
		0 V	Ground	DGND	23	24	USB1_TX_M	USB	–	O	F2
F6	I/O	–	USB	USB1_D_P	25	26	DGND	Ground	0 V		
E6	I/O	–	USB	USB1_D_M	27	28	DGND	Ground	0 V		
		0 V	Ground	DGND	29	30	USB1_RX_P	USB	–	I	E3
		0 V	Ground	DGND	31	32	USB1_RX_M	USB	–	I	E4
G6	I/O	1.8 / 3.3 V (8)	USB	USB_PWRFAULT	33	34	DGND	Ground	0 V		
H6	I/O	1.8 / 3.3 V (8)	USB	USB_DRVBUS	35	36	DGND	Ground	0 V		
		0 V	Ground	DGND	37	38	USB2_TX_P	USB	–	O	D1
		0 V	Ground	DGND	39	40	USB2_TX_M	USB	–	O	D2
D5	I/O	–	USB	USB2_ID	41	42	DGND	Ground	0 V		
C7	I/O	–	USB	USB2_VBUS	43	44	DGND	Ground	0 V		
		0 V	Ground	DGND	45	46	USB2_RX_P	USB	–	I	C3
		0 V	Ground	DGND	47	48	USB2_RX_M	USB	–	I	C4
D6	I/O	–	USB	USB2_D_P	49	50	DGND	Ground	0 V		
C6	I/O	–	USB	USB2_D_M	51	52	DGND	Ground	0 V		
		0 V	Ground	DGND	53	54	USB3_TX_P	USB	–	O	B1
		0 V	Ground	DGND	55	56	USB3_TX_M	USB	–	O	B2
B6	I/O	–	USB	USB3_D_P	57	58	DGND	Ground	0 V		
A6	I/O	–	USB	USB3_D_M	59	60	DGND	Ground	0 V		
		0 V	Ground	DGND	61	62	USB3_RX_P	USB	–	I	A3
		0 V	Ground	DGND	63	64	USB3_RX_M	USB	–	I	A4
M4	I/O	1.8 / 3.3 V (8)	USB	USB2_PWRFAULT	65	66	DGND	Ground	0 V		
		0 V	Ground	DGND	67	68	DGND	Ground	0 V		
P3	I/O	1.8 / 3.3 V (9)	SDHC	SDHC_CLK_MOD	69	70	USB2_DRVVBUS	USB	1.8 / 3.3 V (8)	I/O	L4
		0 V	Ground	DGND	71	72	USB3_VBUS	USB	–	I	A7
U3	I/O	1.8 V (6)	SDHC	SDHC_CLK_SYNC_IN	73	74	USB3_ID	USB	–	I	B5
		0 V	Ground	DGND	75	76	DGND	Ground	0 V		
V3	I/O	1.8 V (6)	SDHC	SDHC_CLK_SYNC_OUT	77	78	SPI_SCK	SPI	1.8 V (6)	O	U2
		0 V	Ground	DGND	79	80	DGND	Ground	0 V		
P1	I/O	1.8 / 3.3 V (9)	SDHC	SDHC_DAT0_MOD	81	82	SPI_PCS0	SPI	1.8 V (6)	I/O	U1
R2	I/O	1.8 / 3.3 V (9)	SDHC	SDHC_DAT1_MOD	83	84	SPI_PCS1	SPI	1.8 V (6)	I/O	R3
R1	I/O	1.8 / 3.3 V (9)	SDHC	SDHC_DAT2_MOD	85	86	SPI_PCS2	SPI	1.8 V (6)	I/O	T3
T1	I/O	1.8 / 3.3 V (9)	SDHC	SDHC_DAT3_MOD	87	88	SPI_PCS3	SPI	1.8 V (6)	I/O	V1
		0 V	Ground	DGND	89	90	DGND	Ground	0 V		
P2	I/O	1.8 / 3.3 V (9)	SDHC	SDHC_CMD_MOD	91	92	SPI_SIN	SPI	1.8 V (6)	I/O	U3
K3	I/O	1.8 / 3.3 V (8)	SDHC	SDHC_CD#	93	94	SPI_SOUT	SPI	1.8 V (6)	I/O	V3
L3	I/O	1.8 / 3.3 V (8)	SDHC	SDHC_WP	95	96	DGND	Ground	0 V		
		0 V	Ground	DGND	97	98	IIC1_SCL_MOD	I2C	3.3 V	O	N1
J1	I/O	1.8 / 3.3 V (8)	UART	UART1_CTS#	99	100	IIC1_SDA_MOD	I2C	3.3 V	I/O	M1
J2	I/O	1.8 / 3.3 V (8)	UART	UART1_RTS	101	102	IIC4_SCL	I2C	1.8 / 3.3 V (8)	I/O	M3
H2	I	1.8 / 3.3 V (8)	UART	UART1_SIN	103	104	IIC4_SDA	I2C	1.8 / 3.3 V (8)	I/O	N3
H1	O	1.8 / 3.3 V (8)	UART	UART1_SOUT (10)	105	106	DGND	Ground	0 V		
		0 V	Ground	DGND	107	108	EVT9#	SYSTEM	1.8 V (6)	I/O	G7
K1	I/O	1.8 / 3.3 V (8)	UART	UART2_SIN	109	110	CPU_ASLEEP	SYSTEM	1.8 V (6)	I/O	E9
L2	I/O	1.8 / 3.3 V (8)	UART	UART2_SOUT (10)	111	112	DGND	Ground	0 V		
		0 V	Ground	DGND	113	114	CLK_OUT	SYSTEM	1.8 V (6)	O	G16
–	O	3.3 V	SYSTEM	TEMP_CRIT_MOD#	115	116	DGND	Ground	0 V		
–	I	3.3 V	SYSTEM	RESIN#	117	118	CPU_RTC	SYSTEM	1.8 V (6)	I/O	F17
–	O	3.3 V	SYSTEM	RESET_OUT#	119	120	CLKOE	Factory Test	3.3 V	I	–

6: OVDD
7: LVDDIN (X1-50, 52, 54)
8. DVDD
9: EVDD
10: 4.7 kΩ Pull-Up on carrier board is recommended.

4.14.2 Pinout TQMLS10xxA connectors (continued)

Table 10: Pinout connector X3

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
		0 V	Ground	DGND	1	2	DGND	Ground	0 V		
AG2	I/O	1.8 / 2.5 V (11)	EC1	EMI1_MDC	3	4	EMI1_MDIO	EC1	1.8 / 2.5 V (11)	I/O	AF2
		0 V	Ground	DGND	5	6	DGND	Ground	0 V		
AC3	I/O	1.8 / 2.5 V (11)	EC1	EC1_GTX_CLK125	7	8	DGND	Ground	0 V		
		0 V	Ground	DGND	9	10	EC1_GTX_CLK	EC1	1.8 / 2.5 V (11)	I/O	W4
W1	I/O	1.8 / 2.5 V (11)	EC1	EC1_RX_CLK	11	12	DGND	Ground	0 V		
		0 V	Ground	DGND	13	14	EC1_TX_EN	EC1	1.8 / 2.5 V (11)	I/O	AB4
AB1	I/O	1.8 / 2.5 V (11)	EC1	EC1_RX_DV	15	16	EC1_TXD0	EC1	1.8 / 2.5 V (11)	I/O	AB3
AA2	I/O	1.8 / 2.5 V (11)	EC1	EC1_RXD0	17	18	EC1_TXD1	EC1	1.8 / 2.5 V (11)	I/O	AA3
AA1	I/O	1.8 / 2.5 V (11)	EC1	EC1_RXD1	19	20	EC1_TXD2	EC1	1.8 / 2.5 V (11)	I/O	Y4
Y1	I/O	1.8 / 2.5 V (11)	EC1	EC1_RXD2	21	22	EC1_TXD3	EC1	1.8 / 2.5 V (11)	I/O	Y3
W2	I/O	1.8 / 2.5 V (11)	EC1	EC1_RXD3	23	24	DGND	Ground	0 V		
		0 V	Ground	DGND	25	26	SWDIO	Factory Test	3.3 V	I/O	–
–	I	1.8 / 3.3 V (12)	SYSTEM	SDHC_EXT_SEL	27	28	SWCLK	Factory Test	3.3 V	I/O	–
–	O	3.3 V	SYSTEM	RTC_INT_OUT	29	30	DGND	Ground	0 V		
		0 V	Ground	DGND	31	32	JTAG_TDI	JTAG	3.3 V	I	–
E10	I/O	1.8 V (13)	EVENT	EVT0#	33	34	JTAG_TDO	JTAG	3.3 V	O	–
E13	I/O	1.8 V (13)	EVENT	EVT1#	35	36	JTAG_TMS	JTAG	3.3 V	I	–
E8	I/O	1.8 V (13)	EVENT	EVT2#	37	38	JTAG_TRST#	JTAG	3.3 V	I	–
E12	I/O	1.8 V (13)	EVENT	EVT3#	39	40	JTAG_TCK	JTAG	3.3 V	I	–
E11	I/O	1.8 V (13)	EVENT	EVT4#	41	42	DGND	Ground	0 V		
		0 V	Ground	DGND	43	44	CKSTP_OUT#	SYSTEM	1.8 V (13)	O	G15
–	I	3.3 V	SYSTEM	BOOT_SRC1	45	46	PROG_SFP	SYSTEM	1.8 V (14)	I	
–	I	3.3 V	SYSTEM	BOOT_SRC0	47	48	TA_BB_TMP_DETECT#	SYSTEM	0.9 / 1.0 V (15)	I	H12
–	I/O	3.3 V	SYSTEM	GPIO_EXP_01	49	50	TA_TMP_DETECT#	SYSTEM	1.8 V (13)	I	H20
F8	I	1.8 V (13)	SYSTEM	HRESET#	51	52	TBSCAN_EN#	SYSTEM	1.8 V (13)	I	F19
F9	O	1.8 V (13)	SYSTEM	PORESET#	53	54	NC	NC	–	–	–
–	O	3.3 V	SYSTEM	RESET_REQ_OUT#	55	56	POWER_GOOD	SYSTEM	3.3 V	O	–
–	I	3.3 V	SYSTEM	POWER_FAIL	57	58	SLEEP	SYSTEM	3.3 V	I	–
		0 V	Ground	DGND	59	60	DGND	Ground	0 V		

11: LVDDIN (X1-50, 52, 54)
12: EVDD
13: OVDD
14: TA_PROG_SFP
15: TA_BB_VDD

4.14.2 Pinout TQMLS10xxA connectors (continued)

Table 11: Pinout connector X4

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
		0 V	Ground	DGND	1	2	DGND	Ground	0 V		
AH4	I/O	1.2 / 1.8 / 2.5 V (16)	EC2	EMI2_MDC	3	4	DGND	Ground	0 V		
		0 V	Ground	DGND	5	6	EMI2_MDIO	EC2	1.2 / 1.8 / 2.5 V (16)	I/O	AH3
AG4	I/O	1.8 / 2.5 V (17)	EC2	EC2_GTX_CLK125	7	8	DGND	Ground	0 V		
		0 V	Ground	DGND	9	10	DGND	Ground	0 V		
AC1	I/O	1.8 / 2.5 V (17)	EC2	EC2_RX_CLK	11	12	EC2_GTX_CLK	EC2	1.8 / 2.5 V (17)	I/O	AC4
		0 V	Ground	DGND	13	14	DGND	Ground	0 V		
AF1	I/O	1.8 / 2.5 V (17)	EC2	EC2_RX_DV	15	16	EC2_TX_EN	EC2	1.8 / 2.5 V (17)	I/O	AG3
AE2	I/O	1.8 / 2.5 V (17)	EC2	EC2_RXD0	17	18	EC2_TXD0	EC2	1.8 / 2.5 V (17)	I/O	AF3
AE1	I/O	1.8 / 2.5 V (17)	EC2	EC2_RXD1	19	20	EC2_TXD1	EC2	1.8 / 2.5 V (17)	I/O	AE4
AD1	I/O	1.8 / 2.5 V (17)	EC2	EC2_RXD2	21	22	EC2_TXD2	EC2	1.8 / 2.5 V (17)	I/O	AE3
AC2	I/O	1.8 / 2.5 V (17)	EC2	EC2_RXD3	23	24	EC2_TXD3	EC2	1.8 / 2.5 V (17)	I/O	AD3
		0 V	Ground	DGND	25	26	DGND	Ground	0 V		
		0 V	Ground	DGND	27	28	DGND	Ground	0 V		
		0 V	Ground	DGND	29	30	SD1_TX0_N	SERDES	1.35 V (18)	O	AE6
		0 V	Ground	DGND	31	32	SD1_TX0_P	SERDES	1.35 V (18)	O	AD6
AH6	I	0.9 / 1.0 V (19)	SERDES	SD1_RX0_N	33	34	DGND	Ground	0 V		
AG6	I	0.9 / 1.0 V (19)	SERDES	SD1_RX0_P	35	36	DGND	Ground	0 V		
		0 V	Ground	DGND	37	38	SD1_TX1_N	SERDES	1.35 V (18)	O	AE8
		0 V	Ground	DGND	39	40	SD1_TX1_P	SERDES	1.35 V (18)	O	AD8
AH8	I	0.9 / 1.0 V (19)	SERDES	SD1_RX1_N	41	42	DGND	Ground	0 V		
AG8	I	0.9 / 1.0 V (19)	SERDES	SD1_RX1_P	43	44	DGND	Ground	0 V		
		0 V	Ground	DGND	45	46	SD1_TX2_N	SERDES	1.35 V (18)	O	AE10
		0 V	Ground	DGND	47	48	SD1_TX2_P	SERDES	1.35 V (18)	O	AD10
AH10	I	0.9 / 1.0 V (19)	SERDES	SD1_RX2_N	49	50	DGND	Ground	0 V		
AG10	I	0.9 / 1.0 V (19)	SERDES	SD1_RX2_P	51	52	DGND	Ground	0 V		
		0 V	Ground	DGND	53	54	SD1_TX3_N	SERDES	1.35 V (18)	O	AE11
		0 V	Ground	DGND	55	56	SD1_TX3_P	SERDES	1.35 V (18)	O	AD11
AH11	I	0.9 / 1.0 V (19)	SERDES	SD1_RX3_N	57	58	DGND	Ground	0 V		
AG11	I	0.9 / 1.0 V (19)	SERDES	SD1_RX3_P	59	60	DGND	Ground	0 V		
		0 V	Ground	DGND	61	62	SD2_TX0_N	SERDES	1.35 V (18)	O	AE15
		0 V	Ground	DGND	63	64	SD2_TX0_P	SERDES	1.35 V (18)	O	AD15
AH15	I	0.9 / 1.0 V (19)	SERDES	SD2_RX0_N	65	66	DGND	Ground	0 V		
AG15	I	0.9 / 1.0 V (19)	SERDES	SD2_RX0_P	67	68	DGND	Ground	0 V		
		0 V	Ground	DGND	69	70	SD2_TX1_N	SERDES	1.35 V (18)	O	AE16
		0 V	Ground	DGND	71	72	SD2_TX1_P	SERDES	1.35 V (18)	O	AD16
AH16	I	0.9 / 1.0 V (19)	SERDES	SD2_RX1_N	73	74	DGND	Ground	0 V		
AG16	I	0.9 / 1.0 V (19)	SERDES	SD2_RX1_P	75	76	DGND	Ground	0 V		
		0 V	Ground	DGND	77	78	SD2_TX2_N	SERDES	1.35 V (18)	O	AE18
		0 V	Ground	DGND	79	80	SD2_TX2_P	SERDES	1.35 V (18)	O	AD18
AH18	I	0.9 / 1.0 V (19)	SERDES	SD2_RX2_N	81	82	DGND	Ground	0 V		
AG18	I	0.9 / 1.0 V (19)	SERDES	SD2_RX2_P	83	84	DGND	Ground	0 V		
		0 V	Ground	DGND	85	86	SD2_TX3_N	SERDES	1.35 V (18)	O	AE19
		0 V	Ground	DGND	87	88	SD2_TX3_P	SERDES	1.35 V (18)	O	AD19
AH19	I	0.9 / 1.0 V (19)	SERDES	SD2_RX3_N	89	90	DGND	Ground	0 V		
AG19	I	0.9 / 1.0 V (19)	SERDES	SD2_RX3_P	91	92	DGND	Ground	0 V		
		0 V	Ground	DGND	93	94	DGND	Ground	0 V		
		0 V	Ground	DGND	95	96	SD1_REF_CLK1_N	SERDES	0.9 / 1.0 V (19)	I	AH13
		0 V	Ground	DGND	97	98	SD1_REF_CLK1_P	SERDES	0.9 / 1.0 V (19)	I	AG13
AE13	I	0.9 / 1.0 V (19)	SERDES	SD2_REF_CLK1_N	99	100	DGND	Ground	0 V		
AD13	I	0.9 / 1.0 V (19)	SERDES	SD2_REF_CLK1_P	101	102	DGND	Ground	0 V		
		0 V	Ground	DGND	103	104	SD1_REF_CLK2_N	SERDES	0.9 / 1.0 V (19)	I	AB8
		0 V	Ground	DGND	105	106	SD1_REF_CLK2_P	SERDES	0.9 / 1.0 V (19)	I	AA8
AB19	I	0.9 / 1.0 V (19)	SERDES	SD2_REF_CLK2_N	107	108	DGND	Ground	0 V		
AB18	I	0.9 / 1.0 V (19)	SERDES	SD2_REF_CLK2_P	109	110	DGND	Ground	0 V		
		0 V	Ground	DGND	111	112	DGND	Ground	0 V		
		0 V	Ground	DGND	113	114	DGND	Ground	0 V		
M2	I	1.8 / 3.3 V (20)	UART	UART4_SIN	115	116	UART4_SOUT (21)	UART	1.8 / 3.3 V (20)	O	L1
		0 V	Ground	DGND	117	118	DGND	Ground	0 V		
		0 V	Ground	DGND	119	120	DGND	Ground	0 V		

16: TVDD (X1-57, 59)
17: LVDDIN (X1-50, 52, 54)
18: XVDD
19: SVDD
20. DVDD
21: 4.7 kΩ Pull-Up on carrier board is recommended.

4.14.3 Assembly

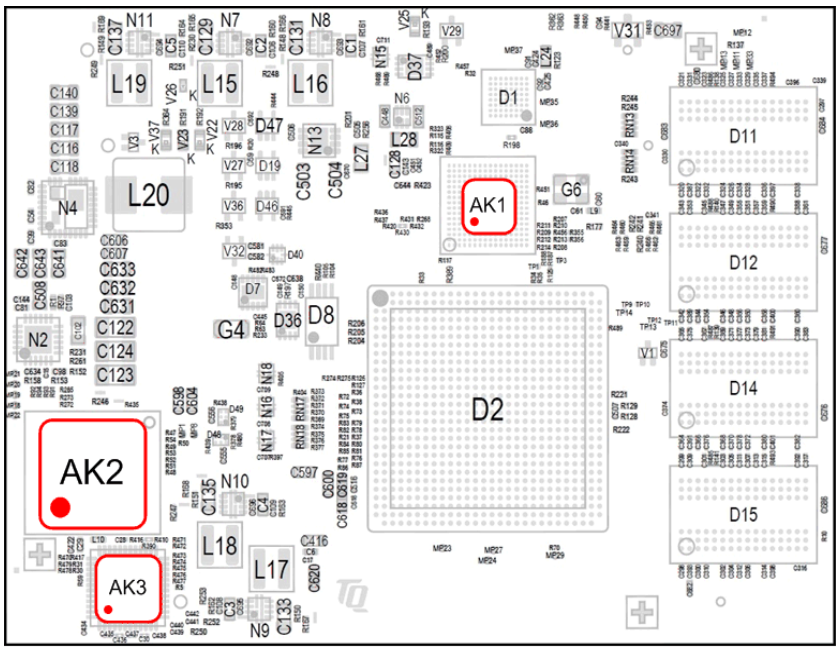


Figure 16: TQMLS10xxA assembly, top

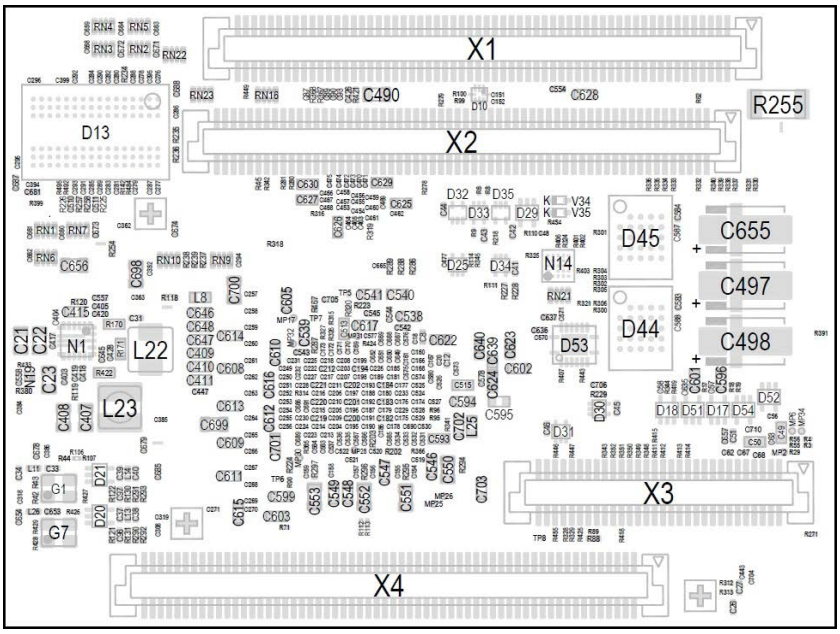


Figure 17: TQMLS10xxA assembly, bottom

The labels on the TQMLS10xxA show the following information:

Table 12: Labels on TQMLS10xxA

Label	Text
AK1	Serial number
AK2	First MAC address (+ additional reserved MAC addresses), tests performed
AK3	TQMLS10xxA version and revision

5. MECHANICS

5.1 Dimensions TQMLS1043A

Figure 18: TQMLS1043A dimensions, side view

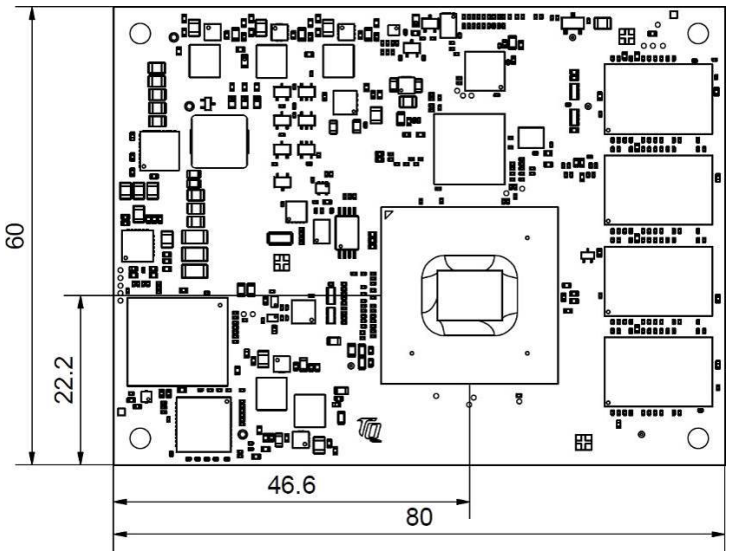


Figure 19: TQMLS1043A dimensions, top view

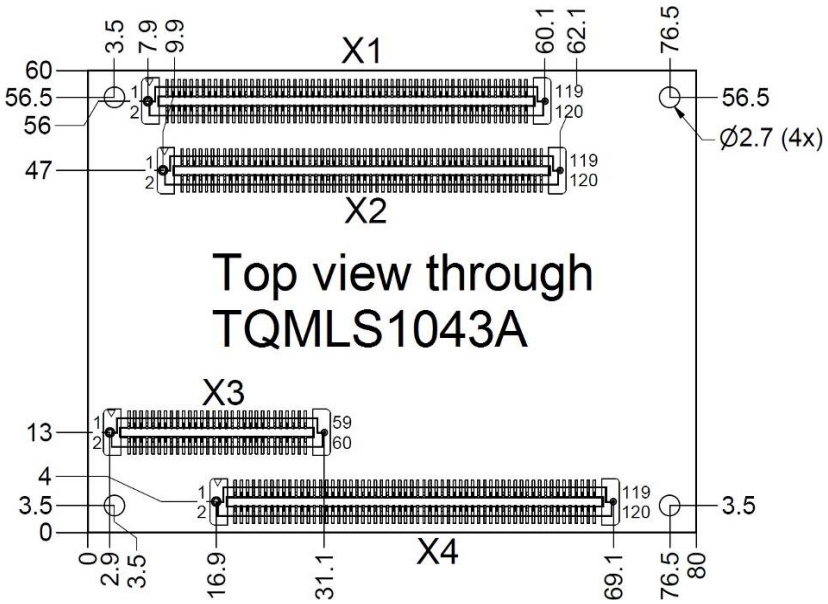


Figure 20: TQMLS1043A dimensions, top view **through** TQMLS1043A

5.2 Dimensions TQMLS1046A / TQMLS1088A

Figure 21: TQMLS1046A / TQMLS1088A dimensions, side view

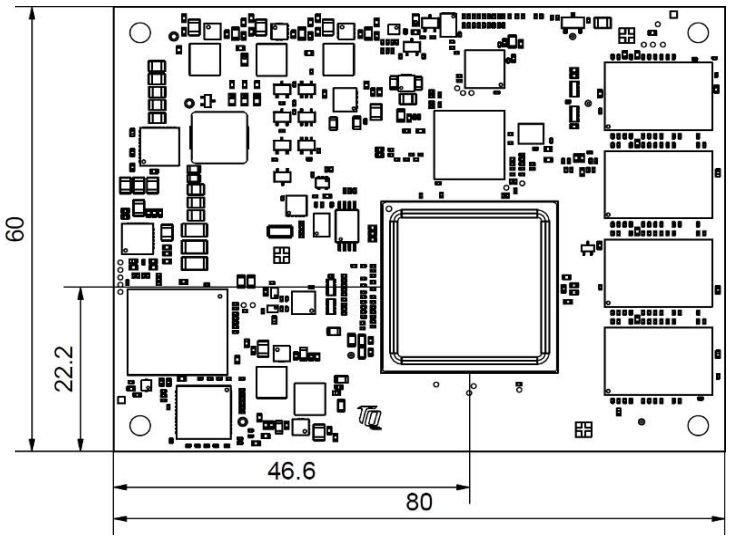


Figure 22: TQMLS1046A / TQMLS1088A dimensions, top view

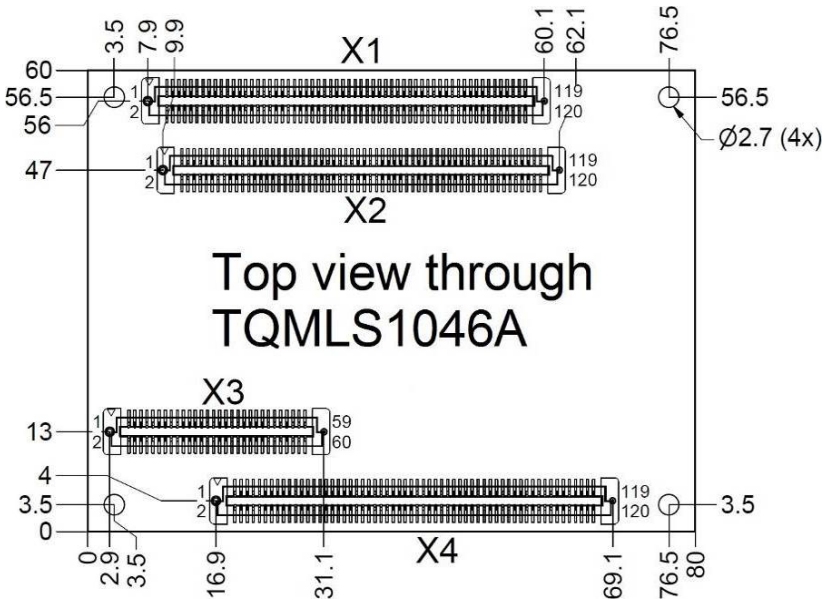


Figure 23: TQMLS1046A / TQMLS1088A dimensions, top view **through** TQMLS1046A / TQMLS1088A

5.3 TQMLS10xxA connectors

The TQMLS10xxA is connected to the carrier board with 420 pins on four connectors.

The following table shows details of the connector assembled on the TQMLS10xxA.

Table 13: Connector assembled on TQMLS10xxA

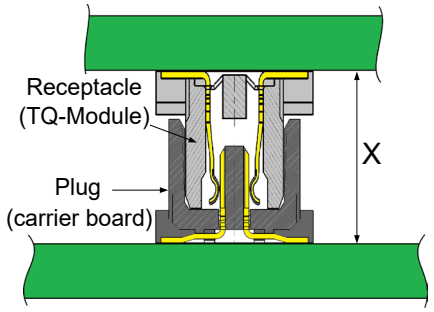
Manufacturer	Part number	Remark
TE connectivity	60-pin: 5177985-2 120-pin: 5177985-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMLS10xxA is held in the mating connectors with a retention force of approximately 42 N.
To avoid damaging the TQMLS10xxA connectors as well as the carrier board connectors while removing the TQMLS10xxA the use of the extraction tool MOZI52XX is strongly recommended. See chapter 5.8 for further information.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMLS10xxA for the extraction tool MOZI52XX.

The following table shows some suitable mating connectors for the carrier board.

Table 14: Carrier board mating connectors

Manufacturer	Pin count / part number	Remark	Stack height (X)	
TE connectivity	60-pin: 5177986-2 120-pin: 5177986-5	On MBLS10xxA	5 mm	
	60-pin: 1-5177986-2 120-pin: 1-5177986-5	–	6 mm	
	60-pin: 2-5177986-2 120-pin: 2-5177986-5	–	7 mm	
	60-pin: 3-5177986-2 120-pin: 3-5177986-5	–	8 mm	

5.4 Adaptation to the environment

The TQMLS10xxA overall dimensions (length × width) are 80 × 60 mm².
The CPU on the TQMLS10xxA has a maximum height of approximately 8.6 mm above the MBLS10xxA.
The TQMLS10xxA weighs approximately 33 grams.

5.5 Protection against external effects

As an embedded module, the TQMLS10xxA is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.6 Thermal management

The cooling system for the TQMLS1088A should be designed to dissipate a maximum of approximately 20 watts.
The power consumption of TQMLS1043A and TQMLS1046A are significantly lower, see Table 4.
The power dissipation originates primarily in the CPU and the DDR4 SDRAM.
The power dissipation also depends on the software used and can vary according to the application.

Attention: Destruction or malfunction, TQMLS10xxA heat dissipation	
	The TQMLS10xxA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LS10xxA must be taken into consideration when connecting the heat sink, see (2). The LS10xxA is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMLS10xxA and thus malfunction, deterioration or destruction.

5.7 Structural requirements

The TQMLS10xxA is held in the mating connectors by the retention force of the pins (420). If high requirements are set for vibration and shock resistance, additional fastening via the mounting holes is possible in the final application.

5.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMLS10xxA may only be extracted from the carrier board by using the extraction tool MOZI52XX that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMLS10xxA for the extraction tool MOZI52XX.

6. SOFTWARE

The TQMLS10xxA is delivered with a preinstalled boot loader and a BSP, which is configured for the Starterkit MBLS10xxA.
Documentation and BSPs can be found in the respective TQ-Support Wiki, see (1.9).
The boot loader provides TQMLS10xxA-specific as well as board-specific settings, e.g.:

- CPU configuration
- PMIC configuration
- DDR4 SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMLS10xxA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
The following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board.
- A sufficient number of blocking capacitors in all supply voltages.
- Fast or permanently clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and / or shielding besides,
  take note of not only the frequency, but also the signal rise times.
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly).

Since the TQMLS10xxA is plugged on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMLS10xxA.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa95xxSA is only a sub-component of an overall system.

7.5 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

7.6 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.
The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

7.7 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.
In general, a reliable operation is given when following conditions are met:

Table 15: Climate and operational conditions

Parameter	Range	Remark
Ambient temperature	–40 °C to +85 °C	–
Storage temperature	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the CPUs' thermal characteristics is to be taken from the NXP Reference Manuals (1).

7.8 Reliability and service life

No MTBF was calculated for the TQMLS10xxA. The TQMLS10xxA is designed to be insensitive to vibration and impact.
High quality industrial grade connectors are assembled on the TQMLS10xxA.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The TQMLS10xxA is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMLS10xxA was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMLS10xxA must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the TQMLS10xxA enable compliance with EuP requirements for the TQMLS10xxA.

8.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

8.6 Battery

No batteries are assembled on the TQMLS10xxA.

8.7 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMLS10xxA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMLS10xxA is delivered in reusable packaging.

8.8 Other entries

The energy consumption of this subassembly is minimised by suitable measures.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 16: Acronyms

Acronym	Meaning
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DC	Direct Current
DDR	Double Data Rate
DUART	Debug UART
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multi-Media Card
ESD	Electrostatic Discharge
eSDHC	enhanced Secure Digital High Capacity
EU	European Union
EuP	Energy using Products
FC-PBGA	Flip-Chip Plastic Ball Grid Array
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
HCSL	Host Clock Signal Level
HDLC	High-level Data Link Control
I/D	Instruction / Data
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IFC	Integrated Flash-Controller
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LED	Light Emitting Diode
LPUART	Low Power UART
LVDS	Low Voltage Differential Signal
MAC	Media Access Control
MOZI	Module extractor (Modulzieher)
MTBF	Mean operating Time Between Failures

9.1 Acronyms and definitions (continued)

Table 16: Acronyms (continued)

Acronym	Meaning
n.a.	Not Applicable
NC	Not Connected
NOR	Not-Or
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCMCIA	People Can't Memorize Computer Industry Acronyms
PMIC	Power Management Integrated Circuit
PWP	Permanent Write Protected
PWR	Power
QSGMII	Quad Serial Gigabit Media-Independent Interface
QSPI	Quad Serial Peripheral Interface
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGMII	Reduced Gigabit Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
RWP	Reversible Write Protected
SATA	Serial ATA
SD card	Secure Digital Card
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random-Access Memory
SERDES	Serialiser/Deserialiser
SGMII	Serial Gigabit Media-Independent Interface
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TB	Terabyte
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
XFI	10 Gigabit Small Form-factor Interface

9.2 References

Table 17: Further applicable documents

No.:	Name	Rev., Date	Company
(1)	Reference Manuals: LS1043A LS1046A LS1088A	Rev. 3, 02/2017 Rev. 1, 10/2017 Rev. 0, 02/2018	NXP NXP NXP
(2)	Data Sheets: LS1043A LS1046A LS1088A	Rev. 3, 03/2018 Rev. 1, 03/2018 Rev. 0, 01/2018	NXP NXP NXP
(3)	MBLS10xxA User's Manual	– current –	TQ-Systems
(4)	TQMLS10xxA Support Wiki	– current –	TQ-Systems

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