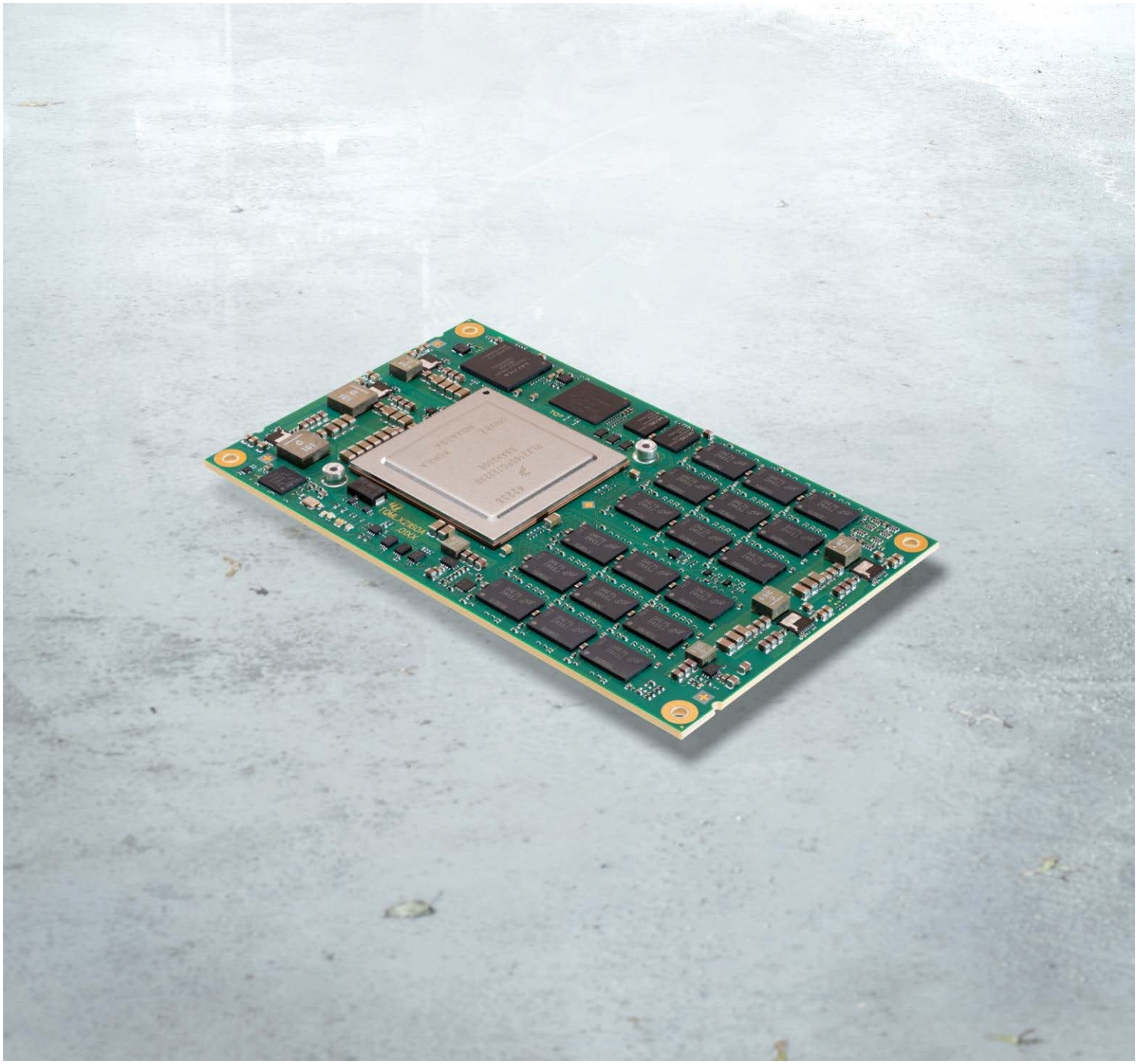
TQMLX2160A
User's Manual

TQMLX2160A UM 0102
11.12.2024



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	28.02.2022	Kreuzer		First edition
0101	22.05.2024	Kreuzer		Typo, formating
0102	11.12.2024	Kreuzer	1.4, 7.4, 7.5, 7.6, 8.4 Table 10 4.11.3	Chapter added Table enhanced Connector source added

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMLX2160A and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.

The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLX2160A circuit diagram
- MBLX2160A User's Manual
- LX2160A documentation
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMLX2160A

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMLX2160A, **Rev. 01xx** and refers to some software settings.

A certain TQMLX2160A derivative does not necessarily provide all features described in this User's Manual.

This User's Manual does also not replace the LX2160A documentation (1), (2). The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMLX2160A, and the BSP provided by TQ-Systems. See also chapter 6.

The TQMLX2160A is a universal Minimodule based on the ARM® NXP CPUs LX2080A, LX2120A or LX2160A.

These CPUs have up to 16 Cortex®-A72 cores with QorIQ technology. The TQMLX2160A extends the TQ-Systems GmbH product range and offers an outstanding computing performance. A suitable CPU derivative can be selected for each requirement.

All essential CPU pins are routed to the TQMLX2160A connectors. There are therefore no restrictions using the TQMLX2160A with respect to an integrated design. Furthermore all components required for the CPU to function like DDR4 SDRAM, eMMC, power supply and power management are integrated on the TQMLX2160A.

The main TQMLX2160A characteristics are:

- LX CPUs with 8 / 12 / 16 cores
- Size 126 mm x 78 mm
- Up to 64 Gbyte DDR4 SDRAM with ECC
- Up to 64 Gbyte eMMC NAND flash
- Up to 512 Mbyte QSPI / Octal-NOR flash
- 64 Kbit EEPROM
- Voltage supervision
- Real-Time-Clock
- Secure Element
- Temperature sensor
- All essential CPU pins are routed to the TQMLX2160A connectors
- Single 5 V power supply

The MBLX2160A serves as carrier board and reference platform for the TQMLX2160A.

3. OVERVIEW

3.1 Block diagram

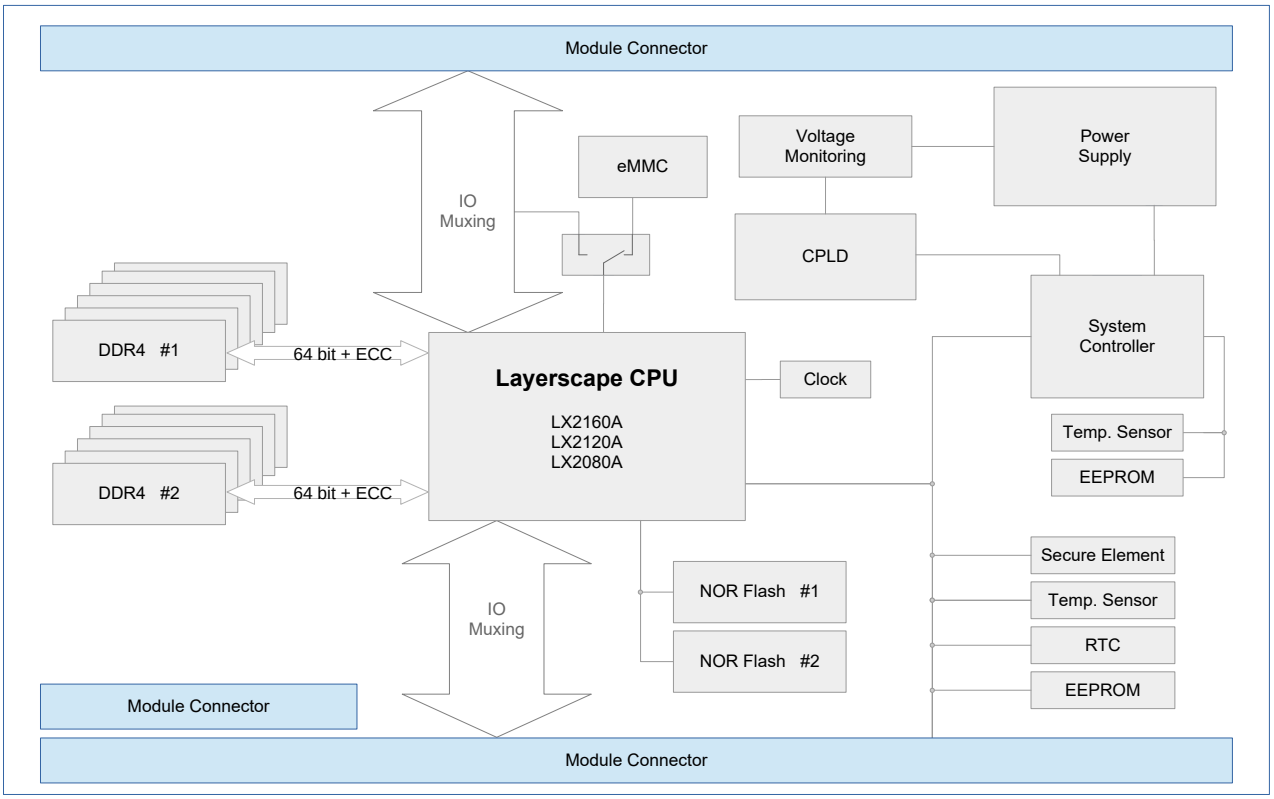

Figure 1: Block diagram TQMLX2160A (simplified)

3.2 System components

The TQMLX2160A provides the following key functions and characteristics:

- LX2160A / LX2120A / LX2080A CPU with up to 16 cores
- DDR4 SDRAM at two controllers
- eMMC NAND flash 5.1
- 2x QSPI NOR flash
- EEPROM (optional)
- Real-Time clock (optional)
- Secure Element chip (optional)
- Oscillators
- Temperature sensor
- Housekeeping via system controller / CPLD
  - Voltage supervision
  - Power sequencing
  - Temperature supervision
  - Error log

All essential CPU pins are routed to the TQMLX2160A connectors. There are therefore no restrictions for customers using the TQMLX2160A with respect to an integrated customised design.

All TQMLX2160A versions are fully pin-compatible and therefore interchangeable.

The functionality of the different TQMLX2160A is mainly determined by the features provided by the respective CPU.

4. ELECTRONICS

4.1 Processor variants

Three different LX CPU derivatives can be assembled on the TQMLX2160A.

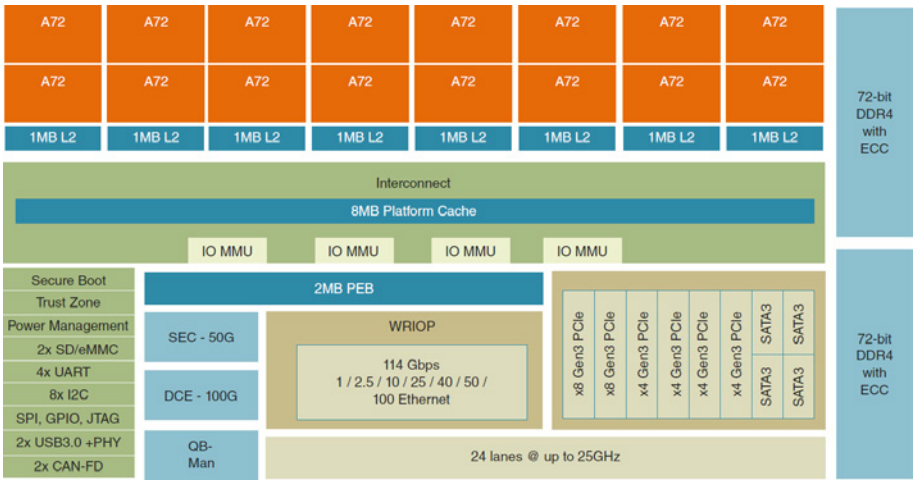

Figure 2: Block diagram LX2160A
(Source: NXP)

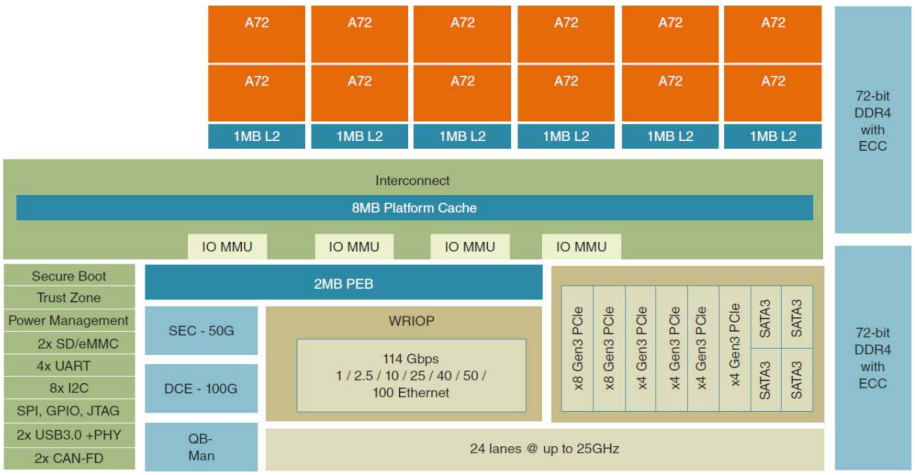

Figure 3: Block diagram LX2120A
(Source: NXP)

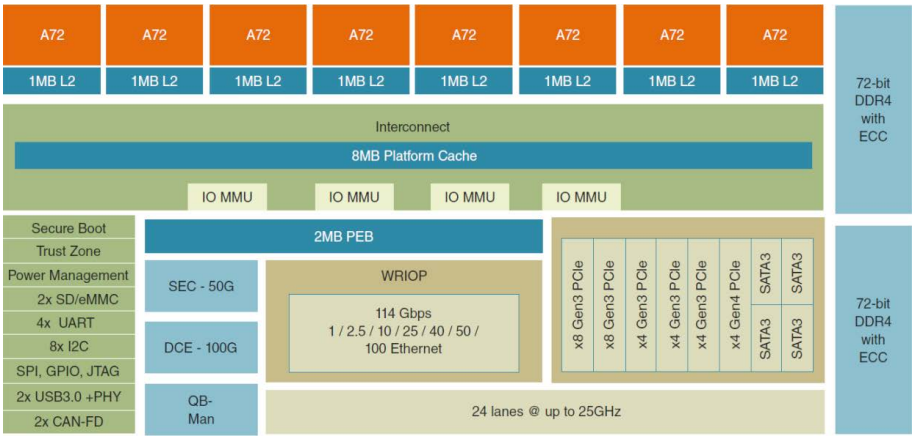

Figure 4: Block diagram LX2080A
(Source: NXP)

4.2 Reset structure

The following block diagram illustrates the Reset circuitry on the TQMLX2160A.

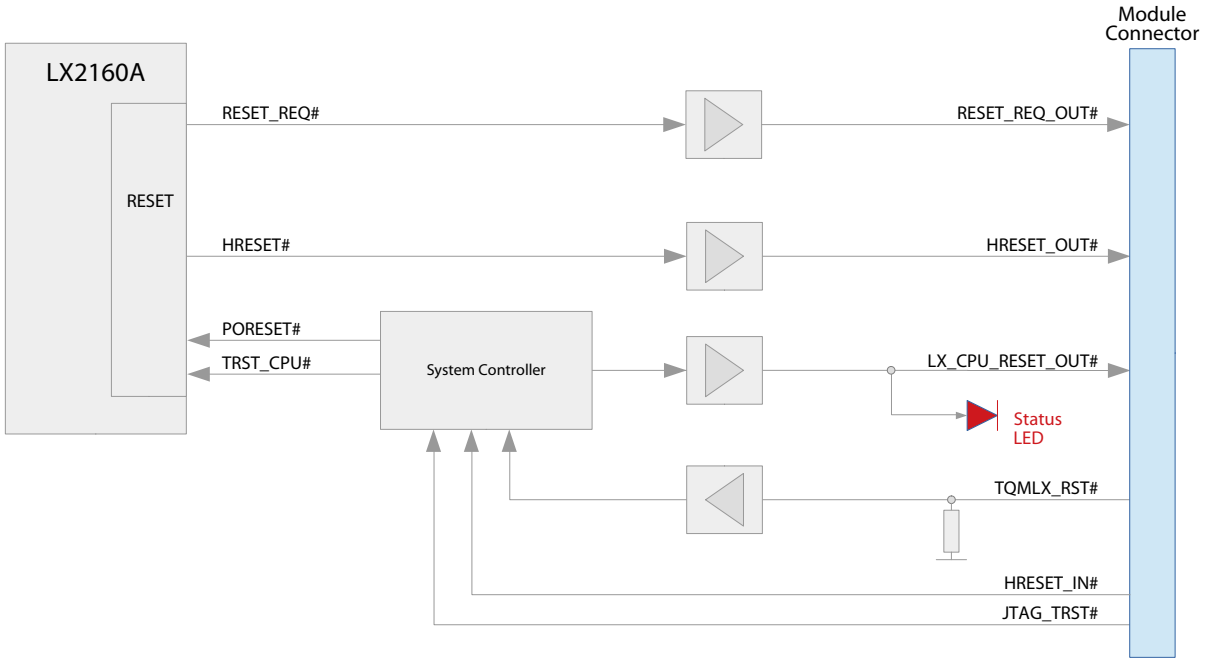

Figure 5: Block diagram Reset structure

4.2.1 TQMLX_RST#

TQMLX_RST# is the reset signal to control the whole TQMLX2160A module. Coming from the module connector, it will be able to hold system controller in reset. If the signal TQMLX_RST# is set to high by the base board, the system controller will start the module.

By default TQMLX_RST# is connected with a pulldown (47-100K), so that the module does not start by itself as soon as the supply voltage is applied. Furthermore a small RC filter is provided at TQMLX_RST#.

A 5 V tolerant buffer is provided. Thus the module can be activated from the base board also with the 5V VIN voltage (e.g. via pullup or directly) and no further voltage is needed for starting.

4.2.2 HRESET#

HRESET# (1.8V) has a pullup and is connected to the system controller and with DDR4_RST#.

A second, downstream driver is used to provide the signal at the TQMLX2160A connector. A level conversion from 1.8 V to 3.3 V is done.

4.2.3 RESET_REQ#

The reset request signal of the LX2160A has a pullup (1.8 V) and after the level conversion to 3.3 V it is made available to the system controller as well as to the TQMLX2160A connector. To avoid faulty circuits on the base board, buffers are interconnected.

4.2.4 LX_CPU_RESET_OUT#

LX_CPU_RESET_OUT# serves as status signal to the base board that the LX CPU is still held in reset. The signal is controlled from the system controller. The state of the signal is indicated by a red LED.

4.2.5 JTAG_TRST#

The TRST# from the JTAG debugger is not connected directly to the CPU, but to the system controller. The reason for this is that TRST# must be controlled together with PORESET# at startup. For the JTAG access it is necessary to separate PORESET# and TRST# depending on the debugger and for the boundary scan test TRST# must be controlled independently of PORESET#.

4.3 Boot source

The boot source of the TQMLX2160A is selected with signals BOOT_SRC[2:0]. Pull-Ups to 3.3 V are provided on the TQMLX2160A.

Table 2: Boot source selection

BOOT_SRC2 (X2-A34)	BOOT_SRC1 (X2-A33)	BOOT_SRC0 (X2-A32)	Boot source
1	1	1	NOR flash
1	1	0	SD card
1	0	1	eMMC
1	0	0	I^2C
0	1	1	XSPI – NAND 2 KB
0	1	0	XSPI – NAND 4 KB
0	0	1	Hard Coded Option
0	0	0	TBD

4.4 DDR4 SDRAM

The LX2160A features two DDR4 controllers. Both controllers have a 72 bit interface (64 bit + 8 bit ECC) each.
ECC is an assembly option and is assembled as an additional DDR4 SDRAM device.
Up to 64 Gbyte of DDR4 SDRAM with a transfer rate of 2800 MT/s can be assembled on the TQMLX2160A.

4.5 NOR flash, eMMC / SD card

The LX2160A provides two SPI interfaces XSPI1_A and XSPI1_B. XSPI1_B is multiplexed with SDHC2. A NOR Flash Swap function (NOR_SWAP#) is implemented: XSPI1_A CS0# and CS1# can be swapped without the CPU registering this.

The SDHC2 / eMMC interface is configured with the eMMC_SEL0/1 signals. These signals are preconfigured on the TQMLX2160A with a pullup to 3.3V. The eMMC_SEL configuration cannot be changed during runtime.

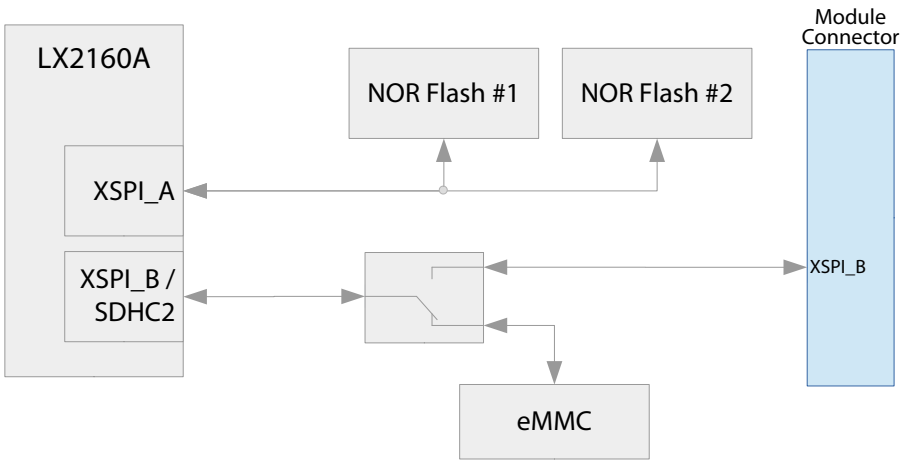

Figure 6: Block diagram NOR flash interface

Table 3: eMMC_SEL0/1 signals

eMMC_SEL1	eMMC_SEL0	Configuration
0	0	SDHC2 entirely at the module connector
0	1	eMMC on TQMLX2160A connected with 4 bit data + 2 × I^2C (I2C_7 and I2C_8)
1	0	(Undefined)
1	1	eMMC on TQMLX2160A connected with 8 bit data (default)

The TQMLX2160A supports the following eMMC transfer modes:

Table 4: eMMC Modes

Mode	1-bit support		4-bit support		8-bit support	
	LX2160A	eMMC 5.1	LX2160A	eMMC 5.1	LX2160A	eMMC 5.1
DS (Default Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS (High Speed)	Yes	Yes	Yes	Yes	Yes	Yes
HS200	No	No	Yes	Yes	Yes	Yes
HS400	No	No	No	No	Yes	Yes
DDR	No	No	Yes	Yes	Yes	Yes

4.6 EEPROMs

The TQMLX2160A provides two EEPROMS:

- A 64 Kbit serial EEPROM type 24LC64
- A 2 Kbit (256 × 8 Bit) serial EEPROM type SE97B, combined with a temperature sensor

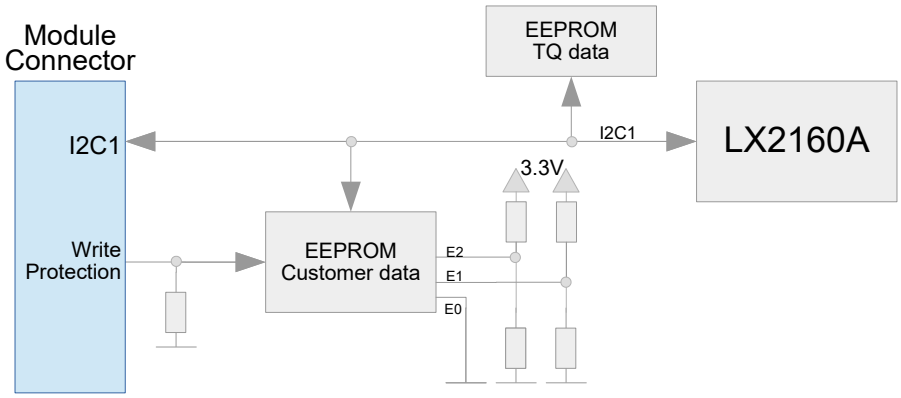

Figure 7: Block diagram I2C1 EEPROM interface

4.6.1 EEPROM, 24LC64

The TQMLX2160A provides a 64 Kbit serial EEPROM type 24LC64. The EEPROM is connected to I2C1 of the LX2160A. WP of the M24LC64 is pulled low on the TQMLX2160A, thus write access is permitted. See also Figure 7.

➢ The I²C address of the EEPROM is `0x50 / 101 0000b`

Other I²C addresses see chapter 4.9.2.

4.6.2 Temperature sensor with EEPROM, SE97B

4.6.2.1 Temperature sensor, SE97B

A temperature sensor SE97B is assembled on the TQMLX2160A, which measures the environmental temperature.

➢ The temperature sensor is connected to I2C1 and has I²C address `0x1F / 001 1111b`

Other I²C addresses see chapter 4.9.2.

The accuracy of the temperature sensor is as follows:

- Max. ±1 °C between +75 °C and +95 °C
- Max. ±2 °C between +40 °C and +125 °C
- Max. ±3 °C between –40 °C and +125 °C

Signal EVENT_TEMPSENSOR# of the temperatures sensor is routed to the TQMLX2160A connector X3-B99.
The signal has an Open Drain output, an optional Pull-Up to 3.3 V can be assembled on the TQMLX2160A.

4.6.2.2 EEPROM, SE97B

The SE97B is connected to the I2C1 bus of the LX2160A and contains a 2 Kbit (256 × 8 Bit) EEPROM.
In this EEPROM TQMLX2160A-specific data is stored, see Table 4. The user can also store own data in this EEPROM.
The EEPROM is divided into two parts. The lower 128 bytes (00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. The upper 128 bytes (80h to FFh) are not write protected and can be used for general purpose data storage. The EEPROM can be accessed with the following two I²C addresses.

- EEPROM (Normal Mode): `0x57 / 101 0111b`
- EEPROM (Protected Mode): `0x37 / 011 0111b`

Other I²C addresses see chapter 4.9.2.

In the EEPROM, TQMLX2160A-specific data is stored. It is, however, not essential for the correct operation of the TQMLX2160A. The user can delete or change the data, but this is not recommended.

In the following table, the parameters stored in the EEPROM are shown.

Table 5: TQMLX2160A-specific data in the EEPROM

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
`0x00`	Variable	Variable	$32_{(10)}$	Binary	Hard Reset Configuration Word (HRCW), (optional)
`0x20`	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
`0x30`	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
`0x40`	Variable	Variable	$64_{(10)}$	ASCII	Order code
`0x80`	–	–	$8{,}064_{(10)}$	–	(Unused)

4.7 RTC

An optional RTC type PCF85063A can be assembled on the TQMLX2160A.
RTC signal CLKOUT (32 kHz) is routed to the TQMLX2160A connector (X3-B97).
The RTC can be supplied via VBAT_RTC from the base board. VBAT_RTC = 0.9 V to 5.5 V.
CLKOUT is deactivated when the TQMLX2160A is not supplied with V_{IN}.

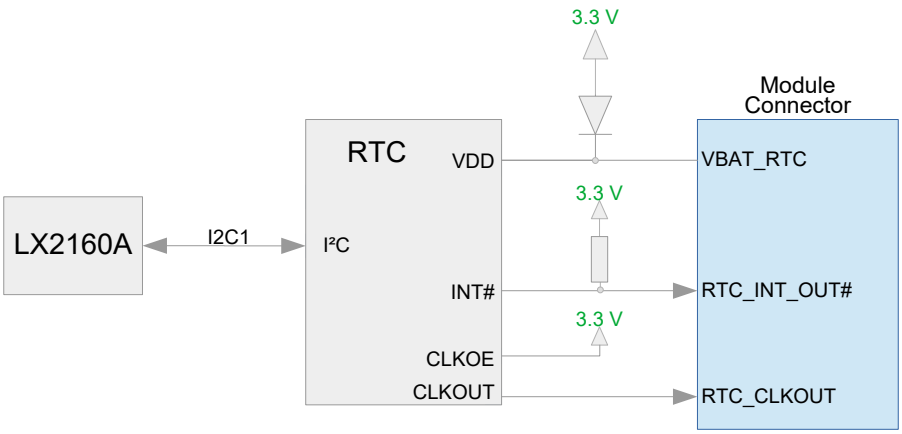

Figure 8: Block diagram RTC interface

➢ The RTC has I²C address `0x51 / 101 0001b`

Other I²C addresses see chapter 4.9.2.

4.8 Secure Element

An optional Secure Element type SE050C2HQ1 can be assembled on the TQMLX2160A.
The device is connected to the CPU as shown in the following Figure.

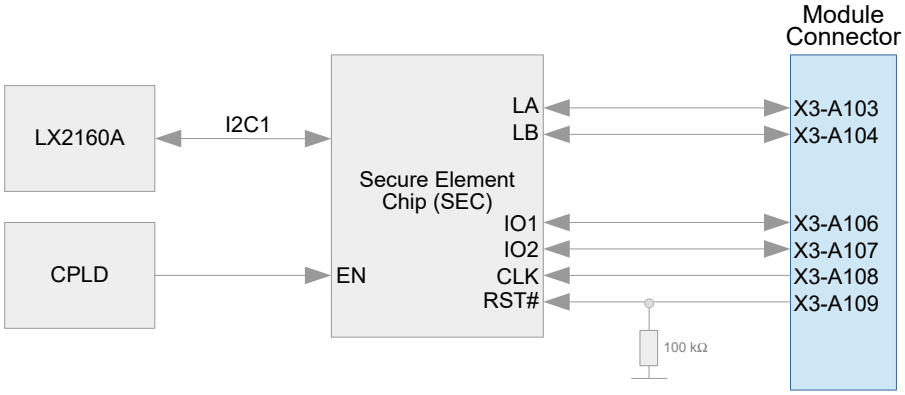

Figure 9: Block diagram SEC interface

- The SEC has I²C address `0x48 / 100 1000b`

Other I²C addresses see chapter 4.9.2.

4.9 Interfaces

4.9.1 SerDes

The LX2160A provides three SerDes blocks with eight lanes each.
No AC coupling capacitors are assembled on the TQMLX2160A. These have to be populated on the carrier board.
The following tables show the SerDes muxing options.

Table 6: SerDes Block 1 muxing options

	Front Side Left SERDES1 (×8)							
	0	1	2	3	4	5	6	7
	H	G	F	E	D	C	B	A
1	PCIe.1 ×4				PCIe.2 ×4			
2	SGMII.3	SGMII.4	SGMII.5	SGMII.6	PCIe.2 ×4			
3	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 ×4			
4	SGMII.3	SGMII.4	SGMII.5	SGMII.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10
5	PCIe.1 ×4				USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
6	USXGMII / XFI.3	USXGMII / XFI.4	SGMII.3	SGMII.3	SGMII.7	SGMII.8	SGMII.9	SGMII.10
7	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10
8	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
9	PCIe.1 ×1	SGMII.4	SGMII.5	SGMII.6	PCIe.2 ×1	SGMII.8	SGMII.9	SGMII.10
10	PCIe.2 ×1 (gen 1,2)	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 ×1 (gen 1,2)	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
11	PCIe.1 ×2		SGMII.5	SGMII.6	PCIe.2 ×2		SGMII.9	SGMII.10
12	PCIe.1 ×4				PCIe.2 ×2		SGMII.9	SGMII.10
13	100GE.1				100GE.2			
14	100GE.1				PCIe.2 ×4			
15	50GE.1		50GE.2		PCIe.2 ×4			
16	50GE.1		25GE.5	25GE.6	PCIe.2 ×4			
17	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 ×4			
18	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
19	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	40GE.2			
20	40GE.1				40GE.2			
21	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 ×2		25GE.9	25GE.10
22	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 ×2		USXGMII / XFI.9	USXGMII / XFI.10

Table 7: SerDes Block 2 muxing options

	Front Side Right SERDES2 (×8)							
	0	1	2	3	4	5	6	7
	A	B	C	D	E	F	G	H
1	PCIe.3 ×2 (gen 1,2)		SATA.1	SATA.2	PCIe.4 ×4 (gen 1,2)			
2	PCIe.3 ×8							
3	PCIe.3 ×4				PCIe.4 ×4			
4	PCIe.3 ×4 (gen 1,2)				PCIe.4 ×2 (gen 1,2)		SATA.1	SATA.2
5	PCIe.3 ×4				SATA.3	SATA.4	SATA.1	SATA.2
6	PCIe.3 ×4 (gen 1,2)				SGMII.15	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14
7	PCIe.3 ×1 (gen 1,2)	SGMII.12	SGMII.17	SGMII.18	PCIe.4 ×1 (gen 1,2)	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14
8	X	X	SATA.1	SATA.2	SATA.3	SATA.4	USXGMII / XFI.13	USXGMII / XFI.14
9	SGMII.11	SGMII.12	SGMII.17	SGMII.18	SGMII.15	SGMII.16	SGMII.13	SGMII.14
10	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.2 ×4			
11	PCIe.3 ×1	SGMII.12	SGMII.17	SGMII.18	PCIe.4 ×1	SGMII.16	SGMII.13	SGMII.14
12	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.4 ×2 (gen 1,2)		SATA.1	SATA.2
13	PCIe.3 ×4				PCIe.4 ×2		SGMII.13	SGMII.14
14	PCIe.3 ×2		SGMII.17	SGMII.18	PCIe.4 ×2		SGMII.13	SGMII.14

Table 8: SerDes Block 3 muxing options

	Back Side SERDES3 (×8)							
	0	1	2	3	4	5	6	7
	A	B	C	D	E	F	G	H
1	PCIe.5 ×8							
2	PCIe.5 ×4				PCIe.6 ×4			

4.9.2 I²C bus

The LX2160A provides up to six I²C buses. All I²C devices on the TQMLX2160A are connected to the I2C1 bus. Therefore the I2C1 bus cannot be multiplexed to any other function.

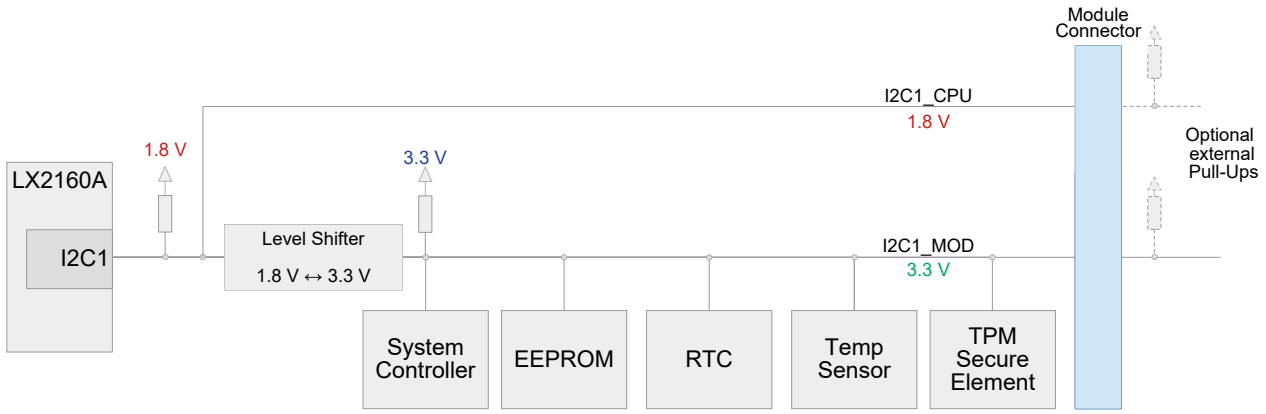

Figure 10: Block diagram I²C bus 1 structure on TQMLX2160A

4.7 kΩ Pull-Ups at the I²C bus are assembled on the TQMLX2160A. More devices can be connected to the bus but then additional external Pull-Ups may be required on account of the higher capacitive load.

Table 9: I²C addresses

Device	Function	7-bit address	Remark
24LC64	EEPROM	0x50 / 101 0000b	–
STM32	System Controller	0x11 / 001 0001b	Should not be altered
PCF85063A	RTC	0x51 / 101 0001b	–
SE050	Secure Element	0x48 / 100 1000b	–
SE97B	Temperature sensor	0x1F / 001 1111b	Access to temperature registers
	EEPROM	0x57 / 101 0111b	R/W access in Normal Mode
	EEPROM	0x37 / 011 0111b	R/W access in Protected Mode

Note: I²C erratum A-010650	
	Please take note of NXP's I²C erratum A-010650 when using I²C buses. A workaround is available for the I2C_1 bus, to which all devices on the module are connected. GPIO3_DAT11 / IRQ11 is used for this. Therefore this GPIO is not available for general purpose. Due to the numerous multiplexing options for the other five possible I²C buses, this workaround is not used for these five I²C busses. If these I²C buses are to be used on the baseboard, the workaround must be implemented.

4.9.3 UART

(TBD)

4.9.4 USB

The LX2160A features two USB 3.0 controllers with integrated PHYs. All signals are routed directly to the TQMLX2160A connectors. For the signals USB1_TX_P/N and USB_2_TX_P/N 100 nF AC coupling capacitors are populated on the TQMLX2160A. Therefore only AC coupling capacitors are required on the carrier board at the corresponding RX lines. These should be placed as close as possible to the device.

4.9.5 RGMII

Both RGMII interfaces EC1 and EC2 are directly routed to the TQMLX2160A connectors. The I/O signals have 1.8 V level.
The signals EC1_TX_EN (GPIO4_DAT4) and EC2_TX_EN (GPIO4_DAT16) are equipped with 1 kΩ Pull-Downs on the TQMLX2160A.

4.9.6 JTAG

The JTAG interface is routed to the connectors. Signals TCK, and TRST# have Pull-Ups to 1.8 V on the TQMLX2160A.

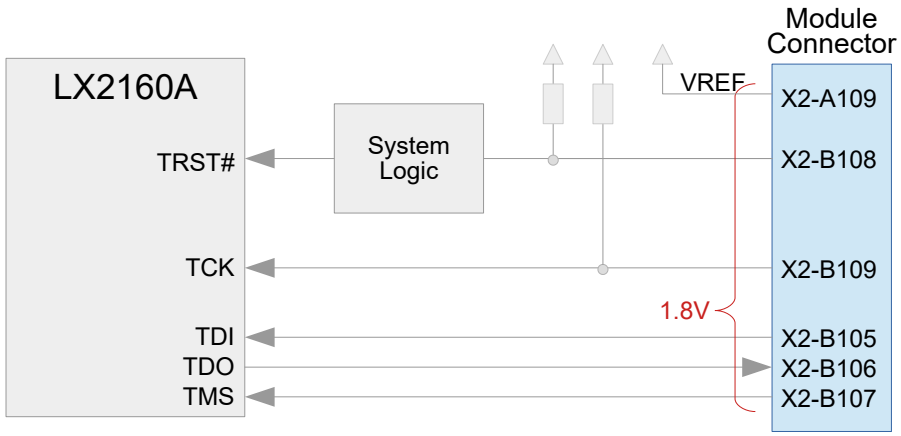

Figure 11: Block diagram JTAG interface

4.10 Power supply

4.10.1 Input voltage

The TQMLX2160A requires a 5 V supply with a maximum tolerance of ±5 %.

4.10.2 Voltage monitoring

All voltages generated on the TQMLX2160A are monitored.

4.10.3 Power consumption

The given power consumptions have to be seen as typical values. The power consumption of the TQMLX2160A strongly depends on the application, the mode of operation, the environmental temperature, and the operating system.

The power supply of the carrier board should be designed for an output power of up to 60 watts.

The following table shows typical power consumption of the TQMLX2160A under various operating conditions. with TQ cooling solution.

Table 10: TQMLX2160A power consumption @ 5 V

Mode of operation	TQMLX2080A	TQMLX2120A	TQMLX2160A	T_{amb}
Number of Cores	8	12	16	
U-Boot, idle	30 W	32 W	36 W	+25 °C
U-Boot, memory test	31 W	34 W	38 W	
Linux, idle	22 W	22 W	22 W	
Linux, 100 % CPU load	38 W	43 W	48 W	
U-Boot, idle	35 W	37 W	38 W	+85 °C
Linux, idle	23 W	24 W	24 W	
Linux, 100 % CPU load	45 W	48 W	50 W	

Attention: Destruction or malfunction, TQMLX2160A heat dissipation	
	The TQMLX2160A belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LX2160A must be taken into consideration when connecting the heat sink. The LX2160A is the highest component on the TQMLX2160A. Inadequate cooling connections can lead to overheating of the TQMLX2160A and thus malfunction, deterioration or destruction.

4.11 TQMLX2160A connectivity

4.11.1 Interface impedances

Usually all signals have a single-ended impedance of nominal 50 Ω with a tolerance of ±10 %. Depending on the signal, the following impedances are used on the TQMLX2160A and recommended for the carrier board:

Table 11: TQMLX2160A interface impedances

Interface	Impedance TQMLX2160A	Recommendation for carrier board
USB 3.0	90 Ω, differential	90 Ω ±15 %, differential
SerDes 1	100 Ω, differential	100 Ω ±10 %, differential
SerDes 2	100 Ω, differential	100 Ω ±10 %, differential
SerDes 3	90 Ω, differential	90 Ω ±10 %, differential

The layout guidelines of the corresponding standards are to be taken note of for the mainboard design.

4.11.2 SerDes track length

The following table shows the SerDes interface track lengths on the TQMLX2160A from the CPU ball to the connector pin, and the insertion loss of each lane in dB assuming the following conditions:

- PCIe Gen 3 with 4 GHz: 0.44dB/Inch + 2 x 0.04 dB for Vias
- XFI with 5.17 GHz: 0.5dB/Inch + 2 x 0.05 dB for Vias
- CAUI with 12.9 GHz: 0.84dB/Inch + 2x 0.15 dB für Vias

Table 12: SerDes track length and estimated insertion loss

SerDes	Lane	Signal	Length (mm)	PCIe Gen 3 (dB)	XFI (dB)	CAUI (dB)
SerDes 1	Lane 0	RX	19.7	0.42	0.49	0.95
		TX	19.1	0.41	0.48	0.93
	Lane 1	RX	21.5	0.45	0.52	1.01
		TX	20.9	0.44	0.51	0.99
	Lane 2	RX	19.5	0.42	0.48	0.94
		TX	18.8	0.41	0.47	0.92
	Lane 3	RX	21.4	0.45	0.52	1.01
		TX	20.8	0.44	0.51	0.99
	Lane 4	RX	21.4	0.45	0.52	1.01
		TX	20.8	0.44	0.51	0.99
	Lane 5	RX	19.2	0.41	0.48	0.93
		TX	18.9	0.41	0.47	0.93
	Lane 6	RX	21.6	0.45	0.53	1.01
		TX	20.6	0.44	0.51	0.98
	Lane 7	RX	19.5	0.42	0.48	0.94
		TX	18.6	0.40	0.47	0.92
	–	PLLF	30.1	–	–	–
		PLLS	23.5	–	–	–
SerDes 2	Lane 0	RX	19.9	0.42	–	–
		TX	19.1	0.41	–	–
	Lane 1	RX	22.0	0.46	–	–
		TX	21.3	0.45	–	–
	Lane 2	RX	19.9	0.42	–	–
		TX	19.9	0.42	–	–
	Lane 3	RX	22.4	0.47	–	–
		TX	21.9	0.46	–	–
	Lane 4	RX	22.2	0.46	–	–
		TX	21.7	0.46	–	–
	Lane 5	RX	19.9	0.42	–	–
		TX	19.5	0.42	–	–
	Lane 6	RX	22.2	0.46	0.54	–
		TX	21.8	0.46	0.53	–
	Lane 7	RX	20.0	0.43	0.49	–
		TX	20.0	0.43	0.49	–
	–	PLLF	25.7	–	–	–
		PLLS	16.9	–	–	–
SerDes 3	Lane 0	RX	27.2	0.47	–	–
		TX	25.5	0.52	–	–
	Lane 1	RX	27.8	0.56	–	–
		TX	26.6	0.54	–	–
	Lane 2	RX	26.0	0.53	–	–
		TX	25.1	0.51	–	–
	Lane 3	RX	28.3	0.57	–	–
		TX	28.0	0.57	–	–
	Lane 4	RX	27.6	0.56	–	–
		TX	27.1	0.55	–	–
	Lane 5	RX	25.9	0.53	–	–
		TX	26.7	0.54	–	–
	Lane 6	RX	28.2	0.57	–	–
		TX	28.3	0.57	–	–
	Lane 7	RX	26.1	0.53	–	–
		TX	26.8	0.54	–	–
	–	PLLF	25.2	–	–	–
		PLLS	26.0	–	–	–

4.11.3 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of.
The pin assignment of the connectors in Table 13 to Table 15 refers to the corresponding BSP provided by TQ-Systems in combination with the MBLX2160A. The electrical and pin characteristics are to be taken from the LX2160A documentation (1), (2).

Connector samples are available from: https://www.ept.de/index.php?tq-colibri-lp

Attention: Destruction or malfunction	
	Depending on the configuration, many LX2160A balls can provide several different functions. Please take note of the information in the LX2160A documentation (1), (2) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMLX2160A. The meanings given in the following tables must be observed: RFU: Reserved pins without function. To support future TQMLX2160A versions, these pins must not be connected. DNC: These pins must never be wired and must be left open.

4.11.4 Pinout TQMLX2160A connectors

Table 13: Pinout connector X1

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	I	5 V	Power	V_{IN}	A1	B1	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A2	B2	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A3	B3	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A4	B4	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A5	B5	V_{IN}	Power	5 V	I	–
–	–	0 V	Power	DGND	A6	B6	DGND	Power	0 V	–	–
–	I	5 V	Power	V_{IN}	A7	B7	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A8	B8	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A9	B9	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A10	B10	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A11	B11	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A12	B12	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A13	B13	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A14	B14	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A15	B15	V_{IN}	Power	5 V	I	–
–	–	0 V	Power	DGND	A16	B16	DGND	Power	0 V	–	–
–	I	5 V	Power	V_{IN}	A17	B17	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A18	B18	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A19	B19	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A20	B20	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A21	B21	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A22	B22	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A23	B23	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A24	B24	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A25	B25	V_{IN}	Power	5 V	I	–
–	–	0 V	Power	DGND	A26	B26	DGND	Power	0 V	–	–
–	I	5 V	Power	V_{IN}	A27	B27	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A28	B28	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A29	B29	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A30	B30	V_{IN}	Power	5 V	I	–
–	I	5 V	Power	V_{IN}	A31	B31	V_{IN}	Power	5 V	I	–
–	–	0 V	Power	DGND	A32	B32	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A33	B33	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A34	B34	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A35	B35	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A36	B36	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A37	B37	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A38	B38	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A39	B39	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A40	B40	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A41	B41	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A42	B42	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A43	B43	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A44	B44	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A45	B45	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A46	B46	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A47	B47	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A48	B48	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A49	B49	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A50	B50	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A51	B51	DGND	Power	0 V	–	–
–	O	1.8 V	Power	1V8_OUT	A52	B52	1V8_OUT	Power	1.8 V	O	–
–	O	1.8 V	Power	1V8_OUT	A53	B53	1V8_OUT	Power	1.8 V	O	–
–	–	0 V	Power	DGND	A54	B54	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A55	B55	DGND	Power	0 V	–	–
–	O	3.3 V	Power	3V3_OUT	A56	B56	3V3_OUT	Power	3.3 V	O	–
–	O	3.3 V	Power	3V3_OUT	A57	B57	3V3_OUT	Power	3.3 V	O	–
–	I	3.3 V	Power	TA_BB_VDD_IN	A58	B58	(NC)	DNC	–	–	–
–	I	1.8 V	Power	TA_PROG_SFP_IN	A59	B59	(NC)	DNC	–	–	–
–	–	0 V	Power	DGND	A60	B60	DGND	Power	0 V	–	–

4.11.4 Pinout TQMLX2160A connectors (continued)

Table 14: Pinout connector X2

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	–	0 V	Power	DGND	A1	B1	DGND	Power	0 V	–	–
–	O	3.3 V	Reset	LX_CPU_RESET_OUT#	A2	B2	TQMLX_RST_IN#	Reset	3.3 V	I	–
M9	O	3.3 V	Reset	RESET_REQ_OUT	A3	B3	SYSC_MON_UART_RX	SYSC	3.3 V	I	–
F6	O	3.3 V	Reset	HRESET_OUT#	A4	B4	SYSC_MON_UART_TX	SYSC	3.3 V	O	–
–	–	0 V	Power	DGND	A5	B5	DGND	Power	0 V	–	–
F5	I/O	1.8 V	I2C	I2C1_CPU_SCL	A6	B6	SYSC_UART_MUX_RX	SYSC	3.3 V	I	–
G5	I/O	1.8 V	I2C	I2C2_CPU_SDA	A7	B7	SYSC_UART_MUX_TX	SYSC	3.3 V	O	–
–	–	0 V	Power	DGND	A8	B8	DGND	Power	0 V	–	–
–	I	3.3 V	JTAG_CPLD	JTAG_CPLD_TCK	A9	B9	I2C5_CPU_SCL	I2C	1.8 V	I/O	C4
–	I	3.3 V	JTAG_CPLD	JTAG_CPLD_TMS	A10	B10	I2C5_CPU_SDA	I2C	1.8 V	I/O	D3
–	–	0 V	Power	DGND	A11	B11	DGND	Power	0 V	–	–
–	O	3.3 V	JTAG_CPLD	JTAG_CPLD_TDO	A12	B12	UART1_SOUT	UART	1.8 V	I/O	B6
–	I	3.3 V	JTAG_CPLD	JTAG_CPLD_TDI	A13	B13	UART1_SIN	UART	1.8 V	I/O	B5
–	–	0 V	Power	DGND	A14	B14	UART2_SOUT	UART	1.8 V	I/O	D6
–	I	3.3 V	SYSC	SYSC_SWCLK	A15	B15	UART2_SIN	UART	1.8 V	I/O	D5
–	I/O	3.3 V	SYSC	SYSC_SWDIO	A16	B16	UART3_SOUT	UART	1.8 V	I/O	A5
–	–	0 V	Power	DGND	A17	B17	UART3_SIN	UART	1.8 V	I/O	A6
–	–	0 V	Power	DGND	A18	B18	UART4_SOUT	UART	1.8 V	I/O	C5
E3	I/O	1.8 V	SDHC1	SDHC1_CD#	A19	B19	UART4_SIN	UART	1.8 V	I/O	C6
E4	I/O	1.8 V	SDHC1	SDHC1_WP	A20	B20	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A21	B21	DGND	Power	0 V	–	–
D1	I/O	EVDD	SDHC1	SDHC1_CLK	A22	B22	SDHC1_DAT0	SDHC1	EVDD	I/O	F1
–	–	0 V	Power	DGND	A23	B23	SDHC1_DAT1	SDHC1	EVDD	I/O	E2
B2	I/O	1.8 V	SDHC1	SDHC1_DS	A24	B24	SDHC1_DAT2	SDHC1	EVDD	I/O	C1
–	–	0 V	Power	DGND	A25	B25	SDHC1_DAT3	SDHC1	EVDD	I/O	C2
E1	I/O	EVDD	SDHC1	SDHC1_CMD	A26	B26	SDHC1_DAT4	SDHC1	1.8 V	I/O	A3
–	–	0 V	Power	DGND	A27	B27	SDHC1_DAT5	SDHC1	1.8 V	I/O	A4
–	I	3.3 V	CONFIG	eMMC_SEL0	A28	B28	SDHC1_DAT6	SDHC1	1.8 V	I/O	B3
–	I	3.3 V	CONFIG	eMMC_SEL1	A29	B29	SDHC1_DAT7	SDHC1	1.8 V	I/O	C3
–	–	0 V	Power	DGND	A30	B30	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A31	B31	DGND	Power	0 V	–	–
–	I	3.3 V	CONFIG	BOOT_SRC0	A32	B32	DGND	Power	0 V	–	–
–	I	3.3 V	CONFIG	BOOT_SRC1	A33	B33	DGND	Power	0 V	–	–
–	I	3.3 V	CONFIG	BOOT_SRC2	A34	B34	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A35	B35	TA_BB_TMP_DETECT#	TRUST	TA_BB_VDD	I	J27
–	I	3.3 V	CONFIG	NOR_SWAP#	A36	B36	TA_TMP_DETECT#	TRUST	1.8 V	I	N9
–	–	0 V	Power	DGND	A37	B37	TQMLX_WAKE	CONFIG	3.3 V	I	–
–	I	1.8 V	CONFIG	EVDD_SEL	A38	B38	TQMLX_SLEEP#	CONFIG	3.3 V	I	–
–	O	3.3 V	SYSC	SYSC_I2C2_SCL	A39	B39	EXT_POWER_FAIL_IN#	CONFIG	3.3 V	I	–
–	I/O	3.3 V	SYSC	SYSC_I2C2_SDA	A40	B40	TQMLX_PGOOD	CONFIG	3.3 V	O	–
–	–	0 V	Power	DGND	A41	B41	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A42	B42	DGND	Power	0 V	–	–
A9	O	–	USB1	USB1_TX_P	A43	B43	DGND	Power	0 V	–	–
B9	O	–	USB1	USB1_TX_N	A44	B44	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A45	B45	USB1_ID	USB1	3.3 V	I/O	E9
C8	I	–	USB1	USB1_RX_P	A46	B46	DGND	Power	0 V	–	–
D8	I	–	USB1	USB1_RX_N	A47	B47	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A48	B48	USB1_PWRFAULT	USB1	1.8 V	I/O	B7
F8	I/O	–	USB1	USB1_DP	A49	B49	USB1_DRVBUS	USB1	1.8 V	I/O	A7
F9	I/O	–	USB1	USB1_DN	A50	B50	USB1_VBUS	USB1	5 V	I	G8
–	–	0 V	Power	DGND	A51	B51	DGND	Power	0 V	–	–
A11	O	–	USB2	USB2_TX_P	A52	B52	DGND	Power	0 V	–	–
B11	O	–	USB2	USB2_TX_N	A53	B53	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A54	B54	USB2_ID	USB2	3.3 V	IO	E11
C10	I	–	USB2	USB2_RX_P	A55	B55	DGND	Power	0 V	–	–

4.11.4 Pinout TQMLX2160A connectors (continued)

Table 14: Pinout connector X2 (continued)

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
D10	I	–	USB2	USB2_RX_N	A56	B56	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A57	B57	USB2_PWRFAULT	USB2	1.8 V	I/O	G7
F10	I/O	–	USB2	USB2_DP	A58	B58	USB2_DRVBUS	USB2	1.8 V	I/O	E7
F11	I/O	–	USB2	USB2_DN	A59	B59	USB2_VBUS	USB2	5 V	I	G10
–	–	0 V	Power	DGND	A60	B60	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A61	B61	DGND	Power	0 V	–	–
F17	I	–	SERDES3	SD3_PLLF_REFCLK_P	A62	B62	SD3_PLLS_REFCLK_P	SERDES3	–	I	B17
E17	I	–	SERDES3	SD3_PLLF_REFCLK_N	A63	B63	SD3_PLLS_REFCLK_N	SERDES3	–	I	A17
–	–	0 V	Power	DGND	A64	B64	DGND	Power	0 V	–	–
F13	O	–	SERDES3	SD3_TX0_P	A65	B65	SD3_RX0_P	SERDES3	–	I	A13
G13	O	–	SERDES3	SD3_TX0_N	A66	B66	SD3_RX0_N	SERDES3	–	I	B13
–	–	0 V	Power	DGND	A67	B67	DGND	Power	0 V	–	–
H14	O	–	SERDES3	SD3_TX1_P	A68	B68	SD3_RX1_P	SERDES3	–	I	C14
J14	O	–	SERDES3	SD3_TX1_N	A69	B69	SD3_RX1_N	SERDES3	–	I	D14
–	–	0 V	Power	DGND	A70	B70	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A71	B71	DGND	Power	0 V	–	–
F15	O	–	SERDES3	SD3_TX2_P	A72	B72	SD3_RX2_P	SERDES3	–	I	A15
G15	O	–	SERDES3	SD3_TX2_N	A73	B73	SD3_RX2_N	SERDES3	–	I	B15
–	–	0 V	Power	DGND	A74	B74	DGND	Power	0 V	–	–
H16	O	–	SERDES3	SD3_TX3_P	A75	B75	SD3_RX3_P	SERDES3	–	I	C16
J16	O	–	SERDES3	SD3_TX3_N	A76	B76	SD3_RX3_N	SERDES3	–	I	D16
–	–	0 V	Power	DGND	A77	B77	DGND	Power	0 V	–	–
H18	O	–	SERDES3	SD3_TX4_P	A78	B78	SD3_RX4_P	SERDES3	–	I	C18
J18	O	–	SERDES3	SD3_TX4_N	A79	B79	SD3_RX4_N	SERDES3	–	I	D18
–	–	0 V	Power	DGND	A80	B80	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A81	B81	DGND	Power	0 V	–	–
F19	O	–	SERDES3	SD3_TX5_P	A82	B82	SD3_RX5_P	SERDES3	–	I	A19
G19	O	–	SERDES3	SD3_TX5_N	A83	B83	SD3_RX5_N	SERDES3	–	I	B19
–	–	0 V	Power	DGND	A84	B84	DGND	Power	0 V	–	–
H20	O	–	SERDES3	SD3_TX6_P	A85	B85	SD3_RX6_P	SERDES3	–	I	C20
J20	O	–	SERDES3	SD3_TX6_N	A86	B86	SD3_RX6_N	SERDES3	–	I	D20
–	–	0 V	Power	DGND	A87	B87	DGND	Power	0 V	–	–
F21	O	–	SERDES3	SD3_TX7_P	A88	B88	SD3_RX7_P	SERDES3	–	I	A21
G21	O	–	SERDES3	SD3_TX7_N	A89	B89	SD3_RX7_N	SERDES3	–	I	B21
–	–	0 V	Power	DGND	A90	B90	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A91	B91	DGND	Power	0 V	–	–
A25	I/O	1.8 V	SDHC2	SDHC2_MOD_CLK	A92	B92	SDHC2_MOD_DAT0	SDHC2	1.8 V	I/O	A23
–	–	0 V	Power	DGND	A93	B93	SDHC2_MOD_DAT1	SDHC2	1.8 V	I/O	C24
C25	I/O	1.8 V	SDHC2	SDHC2_MOD_DS	A94	B94	SDHC2_MOD_DAT2	SDHC2	1.8 V	I/O	B23
–	–	0 V	Power	DGND	A95	B95	SDHC2_MOD_DAT3	SDHC2	1.8 V	I/O	A24
B25	I/O	1.8 V	SDHC2	SDHC2_MOD_CMD	A96	B96	SDHC2_MOD_DAT4	SDHC2	1.8 V	I/O	C26
–	–	0 V	Power	DGND	A97	B97	SDHC2_MOD_DAT5	SDHC2	1.8 V	I/O	B27
–	–	0 V	Power	DGND	A98	B98	SDHC2_MOD_DAT6	SDHC2	1.8 V	I/O	A26
–	–	0 V	Power	DGND	A99	B99	SDHC2_MOD_DAT7	SDHC2	1.8 V	I/O	A27
–	–	0 V	Power	DGND	A100	B100	DGND	Power	0 V	–	–
–	I	3.3 V	CONFIG	LX_CONFIG_RFU1	A101	B101	DGND	Power	0 V	–	–
–	I	3.3 V	CONFIG	LX_CONFIG_RFU2	A102	B102	TBSCAN_EN#	TEST	1.8 V	I	F23
–	I	3.3 V	CONFIG	LX_CONFIG_RFU3	A103	B103	DGND	Power	0 V	–	–
–	I	3.3 V	CONFIG	LX_CONFIG_RFU4	A104	B104	JTAG_LX_HRESET	JTAG_CPU	1.8 V	I	–
–	I	3.3 V	CONFIG	LX_CONFIG_RFU5	A105	B105	JTAG_LX_TDI	JTAG_CPU	1.8 V	I	H27
–	–	0 V	Power	DGND	A106	B106	JTAG_LX_TDO	JTAG_CPU	1.8 V	O	G27
D27	I/O	1.8 V	I2C	I2C6_CPU_SCL	A107	B107	JTAG_LX_TMS	JTAG_CPU	1.8 V	I	G25
C27	I/O	1.8 V	I2C	I2C5_CPU_SDA	A108	B108	JTAG_LX_TRST#	JTAG_CPU	1.8 V	I	H26
–	O	1.8 V	JTAG_CPU	JTAG_LX_VREF	A109	B109	JTAG_LX_TCK	JTAG_CPU	1.8 V	I	G26
–	–	0 V	Power	DGND	A110	B110	DGND	Power	0 V	–	–

4.11.4 Pinout TQMLX2160A connectors (continued)

Table 15: Pinout connector X3

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	–	0 V	Power	DGND	A1	B1	DGND	Power	0 V	–	–
J4	I/O	1.8 V	EC1	EC1_TX_EN	A2	B2	EC1_RX_CLK	EC1	1.8 V	I/O	G1
–	–	0 V	Power	DGND	A3	B3	DGND	Power	0 V	–	–
J3	I/O	1.8 V	EC1	EC1_TXD0	A4	B4	EC1_RXD0	EC1	1.8 V	I/O	J2
H3	I/O	1.8 V	EC1	EC1_TXD1	A5	B5	EC1_RXD1	EC1	1.8 V	I/O	J1
G4	I/O	1.8 V	EC1	EC1_TXD2	A6	B6	EC1_RXD2	EC1	1.8 V	I/O	H1
G3	I/O	1.8 V	EC1	EC1_TXD3	A7	B7	EC1_RXD3	EC1	1.8 V	I/O	G2
–	–	0 V	Power	DGND	A8	B8	EC1_RX_DV	EC1	1.8 V	I/O	K1
F3	I/O	1.8 V	EC1	EC1_GTX_CLK	A9	B9	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A10	B10	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A11	B11	DGND	Power	0 V	–	–
N4	I/O	1.8 V	EC2	EC2_TX_EN	A12	B12	EC2_RX_CLK	EC2	1.8 V	I/O	L1
–	–	0 V	Power	DGND	A13	B13	DGND	Power	0 V	–	–
N3	I/O	1.8 V	EC2	EC2_TXD0	A14	B14	EC2_RXD0	EC2	1.8 V	I/O	N2
M3	I/O	1.8 V	EC2	EC2_TXD1	A15	B15	EC2_RXD1	EC2	1.8 V	I/O	N1
L4	I/O	1.8 V	EC2	EC2_TXD2	A16	B16	EC2_RXD2	EC2	1.8 V	I/O	M1
L3	I/O	1.8 V	EC2	EC2_TXD3	A17	B17	EC2_RXD3	EC2	1.8 V	I/O	L2
–	–	0 V	Power	DGND	A18	B18	EC2_RX_DV	EC2	1.8 V	I/O	P1
K3	I/O	1.8 V	EC2	EC2_GTX_CLK	A19	B19	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A20	B20	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A21	B21	DGND	Power	0 V	–	–
R2	O	1.8 V	EMI	EMI1_MDC	A22	B22	EC_GTX_CLK125_IN_P	EC1	–	I	–
R1	I/O	1.8 V	EMI	EMI1_MDIO	A23	B23	EC_GTX_CLK125_IN_N	EC1	–	I	–
–	–	0 V	Power	DGND	A24	B24	DGND	Power	0 V	–	–
P4	O	1.8 V	EMI	EMI2_MDC	A25	B25	CLK_OUT	CLKOUT	1.8 V	I/O	L6
R3	I/O	1.8 V	EMI	EMI2_MDIO	A26	B26	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A27	B27	CAN1_TX	CAN	1.8 V	I/O	H5
K9	I/O	1.8 V	EVT	EVT0#	A28	B28	CAN1_RX	CAN	1.8 V	I/O	J5
L11	I/O	1.8 V	EVT	EVT1#	A29	B29	CAN2_TX	CAN	1.8 V	I/O	K5
G6	I/O	1.8 V	EVT	EVT2#	A30	B30	CAN2_RX	CAN	1.8 V	I/O	L5
–	–	0 V	Power	DGND	A31	B31	DGND	Power	0 V	–	–
L10	I/O	1.8 V	EVT	EVT3#	A32	B32	EVT4#	EVT	1.8 V	I/O	M10
–	–	0 V	Power	DGND	A33	B33	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A34	B34	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A35	B35	DGND	Power	0 V	–	–
AW13	I	–	SERDES1	SD1_PLLF_REFCLK_P	A36	B36	SD1_PLLS_REFCLK_P	SERDES1	–	I	AR13
AV13	I	–	SERDES1	SD1_PLLF_REFCLK_N	A37	B37	SD1_PLLS_REFCLK_N	SERDES1	–	I	AP13
–	–	0 V	Power	DGND	A38	B38	DGND	Power	0 V	–	–
AW9	I	–	SERDES1	SD1_RX0_P	A39	B39	SD1_TX0_P	SERDES1	–	O	AP9
AV9	I	–	SERDES1	SD1_RX0_N	A40	B40	SD1_TX0_N	SERDES1	–	O	AN9
–	–	0 V	Power	DGND	A41	B41	DGND	Power	0 V	–	–
AU10	I	–	SERDES1	SD1_RX1_P	A42	B42	SD1_TX1_P	SERDES1	–	O	AM10
AT10	I	–	SERDES1	SD1_RX1_N	A43	B43	SD1_TX1_N	SERDES1	–	O	AL10
–	–	0 V	Power	DGND	A44	B44	DGND	Power	0 V	–	–
AW11	I	–	SERDES1	SD1_RX2_P	A45	B45	SD1_TX2_P	SERDES1	–	O	AP11
AV11	I	–	SERDES1	SD1_RX2_N	A46	B46	SD1_TX2_N	SERDES1	–	O	AN11
–	–	0 V	Power	DGND	A47	B47	DGND	Power	0 V	–	–
AU12	I	–	SERDES1	SD1_RX3_P	A48	B48	SD1_TX3_P	SERDES1	–	O	AM12
AT12	I	–	SERDES1	SD1_RX3_N	A49	B49	SD1_TX3_N	SERDES1	–	O	AL12
–	–	0 V	Power	DGND	A50	B50	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A51	B51	DGND	Power	0 V	–	–
AU14	I	–	SERDES1	SD1_RX4_P	A52	B52	SD1_TX4_P	SERDES1	–	O	AM14
AT14	I	–	SERDES1	SD1_RX4_N	A53	B53	SD1_TX4_N	SERDES1	–	O	AL14
–	–	0 V	Power	DGND	A54	B54	DGND	Power	0 V	–	–
AW15	I	–	SERDES1	SD1_RX5_P	A55	B55	SD1_TX5_P	SERDES1	–	O	AP15

4.11.4 Pinout TQMLX2160A connectors (continued)

Table 15: Pinout connector X3 (continued)

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
AV15	I	–	SERDES1	SD1_RX5_N	A56	B56	SD1_TX5_N	SERDES1	–	O	AN15
–	–	0 V	Power	DGND	A57	B57	DGND	Power	0 V	–	–
AU16	I	–	SERDES1	SD1_RX6_P	A58	B58	SD1_TX6_P	SERDES1	–	O	AM16
AT16	I	–	SERDES1	SD1_RX6_N	A59	B59	SD1_TX6_N	SERDES1	–	O	AL16
–	–	0 V	Power	DGND	A60	B60	DGND	Power	0 V	–	–
AW17	I	–	SERDES1	SD1_RX7_P	A61	B61	SD1_TX7_P	SERDES1	–	O	AP17
AV17	I	–	SERDES1	SD1_RX7_N	A62	B62	SD1_TX7_N	SERDES1	–	O	AN17
–	–	0 V	Power	DGND	A63	B63	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A64	B64	DGND	Power	0 V	–	–
AP23	I	–	SERDES2	SD2_PLLF_REFCLK_P	A65	B65	SD2_PLLS_REFCLK_P	SERDES2	–	I	AV23
AR23	I	–	SERDES2	SD2_PLLF_REFCLK_N	A66	B66	SD2_PLLS_REFCLK_N	SERDES2	–	I	AW23
–	–	0 V	Power	DGND	A67	B67	DGND	Power	0 V	–	–
AW19	I	–	SERDES2	SD2_RX0_P	A68	B68	SD2_TX0_P	SERDES2	–	O	AP19
AV19	I	–	SERDES2	SD2_RX0_N	A69	B69	SD2_TX0_N	SERDES2	–	O	AN19
–	–	0 V	Power	DGND	A70	B70	DGND	Power	0 V	–	–
AU20	I	–	SERDES2	SD2_RX1_P	A71	B71	SD2_TX1_P	SERDES2	–	O	AM20
AT20	I	–	SERDES2	SD2_RX1_N	A72	B72	SD2_TX1_N	SERDES2	–	O	AL20
–	–	0 V	Power	DGND	A73	B73	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A74	B74	DGND	Power	0 V	–	–
AW21	I	–	SERDES2	SD2_RX2_P	A75	B75	SD2_TX2_P	SERDES2	–	O	AP21
AV21	I	–	SERDES2	SD2_RX2_N	A76	B76	SD2_TX2_N	SERDES2	–	O	AN21
–	–	0 V	Power	DGND	A77	B77	DGND	Power	0 V	–	–
AU22	I	–	SERDES2	SD2_RX3_P	A78	B78	SD2_TX3_P	SERDES2	–	O	AM22
AT22	I	–	SERDES2	SD2_RX3_N	A79	B79	SD2_TX3_N	SERDES2	–	O	AL22
–	–	0 V	Power	DGND	A80	B80	DGND	Power	0 V	–	–
AU24	I	–	SERDES2	SD2_RX4_P	A81	B81	SD2_TX4_P	SERDES2	–	O	AM24
AT24	I	–	SERDES2	SD2_RX4_N	A82	B82	SD2_TX4_N	SERDES2	–	O	AL24
–	–	0 V	Power	DGND	A83	B83	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A84	B84	DGND	Power	0 V	–	–
AW25	I	–	SERDES2	SD2_RX5_P	A85	B85	SD2_TX5_P	SERDES2	–	O	AP25
AV25	I	–	SERDES2	SD2_RX5_N	A86	B86	SD2_TX5_N	SERDES2	–	O	AN25
–	–	0 V	Power	DGND	A87	B87	DGND	Power	0 V	–	–
AU26	I	–	SERDES2	SD2_RX6_P	A88	B88	SD2_TX6_P	SERDES2	–	O	AM26
AT26	I	–	SERDES2	SD2_RX6_N	A89	B89	SD2_TX6_N	SERDES2	–	O	AL26
–	–	0 V	Power	DGND	A90	B90	DGND	Power	0 V	–	–
AW27	I	–	SERDES2	SD2_RX7_P	A91	B91	SD2_TX7_P	SERDES2	–	O	AP27
AV27	I	–	SERDES2	SD2_RX7_N	A92	B92	SD2_TX7_N	SERDES2	–	O	AN27
–	–	0 V	Power	DGND	A93	B93	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A94	B94	DGND	Power	0 V	–	–
H7	I/O	1.8 V	GPIO	GPIO3_DAT08	A95	B95	VBAT_RTC	RTC	3.3 V	I	–
K7	I/O	1.8 V	GPIO	GPIO3_DAT09	A96	B96	RTC_INT_OUT#	RTC	3.3 V	O	–
H8	I/O	1.8 V	GPIO	GPIO3_DAT10	A97	B97	RTC_CLKOUT	RTC	3.3 V	O	–
G5	I/O	3.3 V	I2C	I2C1_MOD_SDA	A98	B98	EEPROM_WP	EEPROM	3.3 V	I	–
F5	O	3.3 V	I2C	I2C1_MOD_SCL	A99	B99	EVENT_TEMPSENSOR	TEMP	3.3 V	O	–
–	–	0 V	Power	DGND	A100	B100	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A101	B101	IRQ0	IRQ	1.8 V	I/O	H9
–	–	0 V	Power	DGND	A102	B102	IRQ1	IRQ	1.8 V	I/O	H10
–	I/O	–	SECURE	SE14443_LA	A103	B103	IRQ2	IRQ	1.8 V	I/O	11
–	I/O	–	SECURE	SE14443_LB	A104	B104	IRQ3	IRQ	1.8 V	I/O	J7
–	–	0 V	Power	DGND	A105	B105	IRQ4	IRQ	1.8 V	I/O	J11
–	I/O	3.3 V	SECURE	SE_7816_IO1	A106	B106	IRQ5	IRQ	1.8 V	I/O	J9
–	I/O	3.3 V	SECURE	SE_7816_IO2	A107	B107	IRQ6	IRQ	1.8 V	I/O	H6
–	O	3.3 V	SECURE	SE_7816_CLK	A108	B108	IRQ7	IRQ	1.8 V	I/O	K6
–	I	3.3 V	SECURE	SE_7816_RST#	A109	B109	DGND	Power	0 V	–	–
–	–	0 V	Power	DGND	A110	B110	DGND	Power	0 V	–	–

5. MECHANICS

5.1 TQMLX2160A assembly

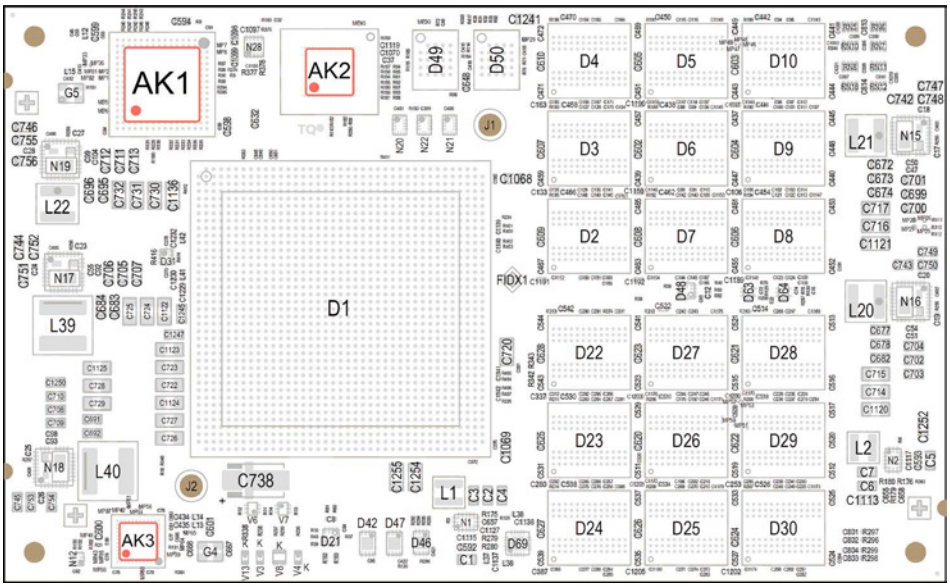

Figure 12: TQMLX2160A assembly, top

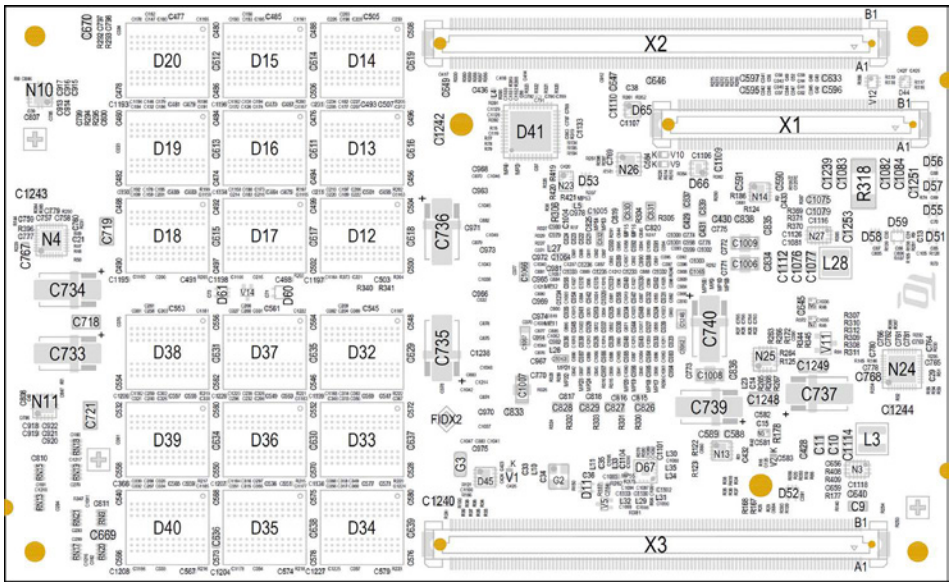

Figure 13: TQMLX2160A assembly, bottom

The labels on the TQMLX2160A show the following information:

Table 16: Labels on TQMLX2160A

Label	Content
AK1	TQMLX2160A version and revision, tests performed
AK2	MAC address
AK3	Serial number

5.2 TQMLX2160A weight, dimensions

The TQMLX2160A overall dimensions (length × width) are 126.0 mm × 78.0 mm (± 0,1 mm).
The CPU on the TQMLX2160A has a maximum height of approximately 10.5 mm above the MBLX2160A.
The TQMLX2160A provides four 2.7 mm Ø mounting holes and two M2 steel spacers to mount a heat sink.
The TQMLX2160A weighs approximately 101 g (± 2 g).

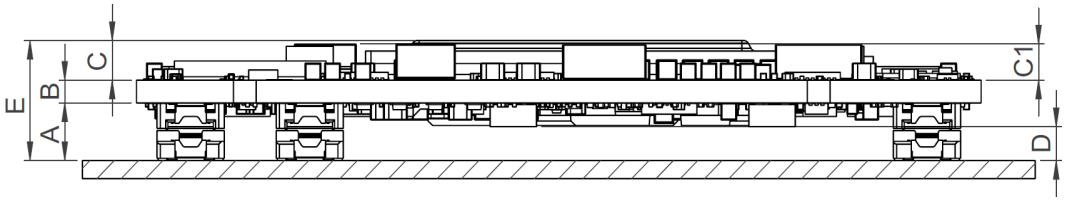

Figure 14: TQMLX2160A dimensions, side view

Table 17: TQMLX2160A side view dimensions

Dimension	Value (mm)	Remark
A	5.10 ±0.07	Board-to-Board distance
B	2.10 ±0.21	PCB thickness
C	3.30 ±0.15	CPU height
C1	3.10 ±0.10	Inductors
D	3.00 ±0.07	Space below TQMLX2160A
E	10.46 ±0.27	Overall height to CPU surface

5.2 TQMLX2160A weight, dimensions (continued)

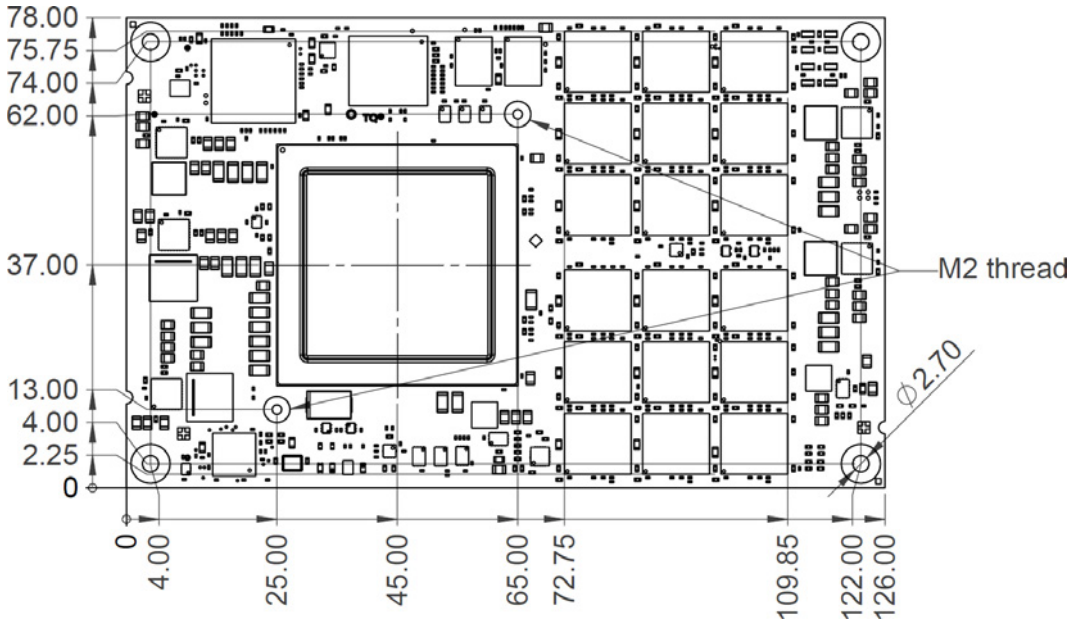

Figure 15: TQMLX2160A dimensions, top view

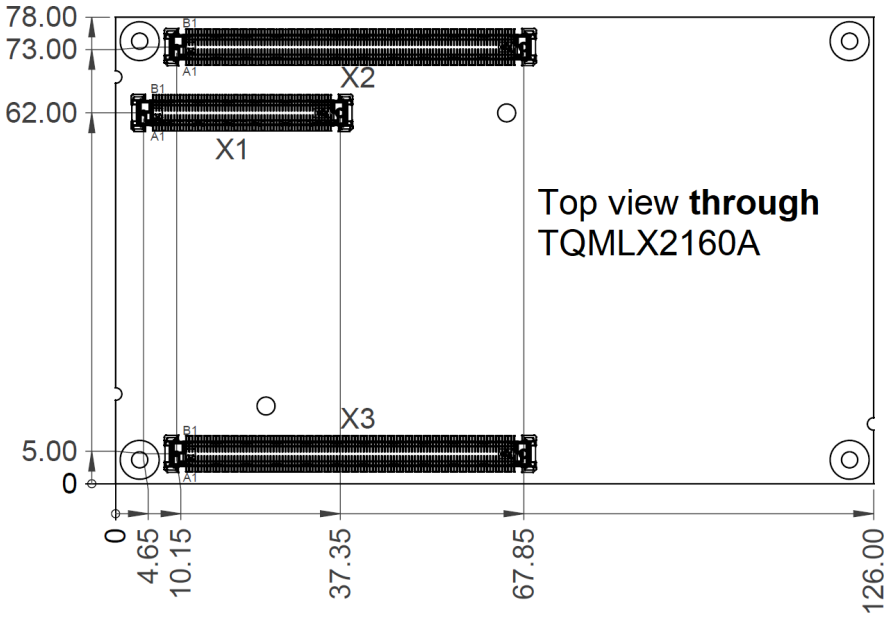

Figure 16: TQMLX2160A dimensions, top view through TQMLX2160A

5.3 TQMLX2160A connectors

The TQMLX2160A is connected to the carrier board with 560 pins on three connectors.

The following table shows details of the connector assembled on the TQMLX2160A.

Table 18: Connector assembled on TQMLX2160A

Manufacturer	Part number	Type
EPT	402-51401-51	120-pin, 0.5 mm pitch
	402-51101-51	220-pin, 0.5 mm pitch

The following table shows suitable carrier board mating connectors.

Table 19: Carrier board mating connectors

Manufacturer	Part number	Type	Remark
EPT	401-51401-51	• 120 pin, 0.5 mm pitch • Data transfer rate 10+ Gbit/s	5 mm board-to-board distance
	401-51103-51	• 220 pin, 0.5 mm pitch • Data transfer rate 16+ Gbit/s	
	401-55401-51	• 120 pin, 0.5 mm pitch • Data transfer rate 10+ Gbit/s	8 mm board-to-board distance
	401-55103-51	• 220 pin, 0.5 mm pitch • Data transfer rate 16+ Gbit/s	

To avoid damaging the connectors of the TQMLX2160A during extraction, the use of the extraction tool MOZILX2160A is strongly recommended.

Note: 16 Gbit+ specification	
	It is strongly recommended to use the 220-pin module connectors with 16 Gbit+ specification for carrier boards. For the 120-pin module connectors the 10Gbit+ specification is sufficient. Carrier board mating connectors with 5 mm height can also be used.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMLX2160A for the extraction tool MOZILX2160A.

5.4 Protection against external effects

As an embedded module, the TQMLX2160A is not protected against dust, external impact and contact (IP00). Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

The cooling system for the TQMLX2160A should be designed to dissipate a maximum of approximately 60 watts.
The power consumption of TQMLX2080A and TQMLX2120A are significantly lower.
The power dissipation originates primarily in the CPU the buck regulators and the DDR4 SDRAM.
The power dissipation also depends on the software used and can vary according to the application.

Attention: Destruction or malfunction, TQMLX2160A heat dissipation	
	The TQMLX2160A belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the LX2160A must be taken into consideration when connecting the heat sink. The LX2160A is the highest component on the TQMLX2160A. Inadequate cooling connections can lead to overheating of the TQMLX2160A and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMLX2160A should be fastened to the carrier board with spacer bolts or spacer sleeves at the four mounting holes.

5.7 Notes of treatment

To avoid damage caused by mechanical stress, the TQMLX2160A may only be extracted from the carrier board by using the extraction tool MOZILX2160A that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMLX2160A for the extraction tool MOZILX2160A.

6. SOFTWARE

The TQMLX2160A is delivered with a preinstalled boot loader and a BSP, which is configured for the Starterkit carrier board MBLX2160A. Documentation and more information about the BSP can be found in the TQ-Support Wiki, see 1.9.
The boot loader provides TQMLX2160A-specific as well as board-specific settings, e.g.:

- CPU configuration
- DDR4 SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMLX2160A was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
The following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board.
- A sufficient number of blocking capacitors in all supply voltages.
- Fast or permanently clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and / or shielding besides,
  take note of not only the frequency, but also the signal rise times.
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly).

Since the TQMLX2160A is plugged on an application-specific carrier board, EMC or ESD tests only make sense for the whole device.

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMLX2160A.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMLX2160A is only a sub-component of an overall system.

7.5 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

7.6 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

7.7 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 20: Climate and operational conditions

Parameter	Range	Remark
Ambient temperature	–40 °C to +85 °C	with suitable cooling (tested with water cooling)
	–40 °C to +60 °C	tested with cooling solution developed by TQ
T_J LX2160A	–40 °C to +105 °C	–
Case temperature DDR4 SDRAM	–40 °C to +95 °C	–
Storage temperature	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the CPUs' thermal characteristics is to be taken from the LX2160A documentation (1), (2).

7.8 Reliability and service life

The calculated MTBF of the TQMLX2160A is 240,000 h @ +40 °C ambient temperature, Ground, Benign.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The TQMLX2160A is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMLX2160A was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

8.5 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMLX2160A must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMLX2160A enable compliance with EuP requirements for the TQMLX2160A.

8.6 Battery

No batteries are assembled on the TQMLX2160A.

8.7 Packaging

The TQMLX2160A is delivered in reusable packaging.

8.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMLX2160A, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMLX2160A is minimised by suitable measures.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))

- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 21: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DDR	Double Data Rate
DNC	Do Not Connect
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multi-Media Card
ESD	Electrostatic Discharge
EU	European Union
EuP	Energy using Products
GPIO	General Purpose Input/Output
HRCW	Hard Reset Configuration Word
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LED	Light Emitting Diode
MAC	Media Access Control
MOZI	Modulzieher (Module extractor)
MTBF	Mean (operating) Time Between Failures
NAND	Not-And (Flash memory)
NC	Not Connected
NOR	Not-Or (Flash memory)
PCB	Printed Circuit Board
PCIe	PCI Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (device)
PWP	Permanent Write Protected

9.1 Acronyms and definitions (continued)

Table 20: Acronyms (continued)

Acronym	Meaning
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGMII	Reduced Gigabit Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
RWP	Reversible Write Protected
SD card	Secure Digital Card
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random-Access Memory
SERDES	Serializer/Deserializer
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protect
XFI	10 Gigabit Small Form-factor Interface
XSPI	Expanded Serial Peripheral Interface

9.2 References

Table 22: Further applicable documents

No.:	Name	Rev., Date	Company
(1)	LX2160A Reference Manual	Rev 1, 6 Oct. 2021	NXP
(2)	LX2160A Data Sheet	Rev 3, 23 Sep. 2021	NXP
(3)	LX2160A Fact Sheet	Rev. 0, 05. Oct. 2017	NXP
(4)	MBLX2160A User's Manual	– current –	TQ-Systems
(5)	TQMLX2160A Support Wiki	– current –	TQ-Systems

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