TQMP2020
User's Manual

TQMP2020 UM 0104
21.11.2019

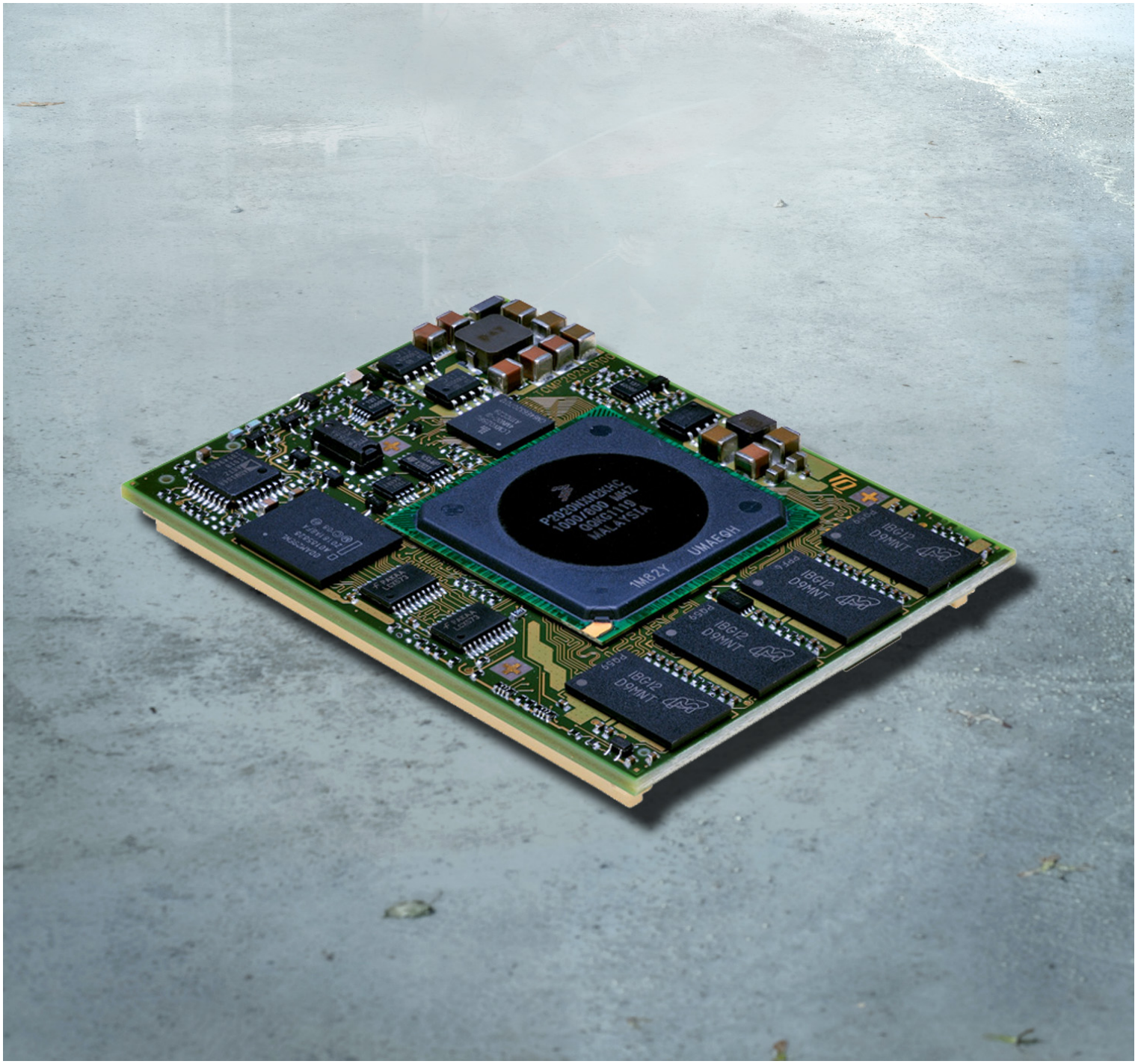

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TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
100	17.10.2011	Petz		Document created
101	03.01.2012	Petz	3.2.3 Table 7 3.2.3.6 Illustration 6 3.2.4.6 Table 17	CPU configuration legend updated "Meaning P2020" of signal PORDEVSR[20:21] for "10" and "11" corrected Warning added Added "100 MHz" for TQMP1xxx removed Type of signal HRESET# specified more precisely
102	24.05.2012	Petz	3.2.3.2 3.7	Typo Link to Wiki added
0103	04.10.2019	Petz	All 1.3, 1.4, 1.9, 3.2.7, 5.1, 5.6, 7.6, 7.7, Table 47 3.2.2.1 ~ 3.2.2.7 Table 10 Table 39, Table 40, Table 43, 5.3, 7.3 3.2.4.6 3.3.3.1 ~ 3.3.3.3 Table 13 3.2.8, 3.2.8.1, 3.2.8.2 3.2.8.4 Table 17 6, Illustration 9 7.1	Freescale replaced with NXP, hyperlinks updated, formatting, typo Updated Merged in 3.2.2 Restructured and clarified Added Typo corrected: LCKL LCLK Merged in 3.3.3 Simplified, column "Device" added, Footnote 1 added Completely reworked Typo corrected: SA560004EDP SA56004EDP, content clarified, Full I2C addresses added Split into Table 21 to Table 38 Information added Removed
0104	21.11.2019	Petz	3.2.2.2, Table 4, Table 5 3.4.3.2	Clarified Chapters 3.4.3.2 to 3.4.3.5 merged

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TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMP2020 and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- STKP2020 circuit diagram
- STKP2020 User's Manual
- P2020RM Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- ELDK documentation: www.denx.de/wiki/DULG/ELDK
- TQ-Support Wiki: Support-Wiki TQMP2020

2. BRIEF DESCRIPTION

The TQMP2020 is a universal Minimodule based on the NXP QorIQ processor P2020.
It extends the range of Power-Architecture based modules towards High-End, with reduced size.
The P2020 computing performance (dual core CPU) is approximately double in comparison to the MPC8548, at significantly lower power dissipation. Alternatively, a P2010 (single core) can be assembled on the TQMP2020.
In this case, the computing performance is equal to the MPC8548. The power dissipation is reduced further.
The dual core CPUs P1020 or P1021, or the single core CPUs P1011 or P1012 can be assembled on the same PCP alternatively.

The TQMP2020 characteristic features are:

- Dual or Single Core, max. 1.2 GHz
- DDR3, 32 or 64 bit with ECC
- 4 × SERDES, configurable as PCI Express, SGMII or Serial Rapid I/O
- 3 × Gbit-Ethernet

The Starterkit STKP2020 is designed to be an Eval-Board for the TQMP2020.
All relevant CPU pins are routed to the TQMP2020 connectors.
When using the TQMP2020, the user has complete freedom, like with a design-in solution.

3. ELECTRONICS

3.1 Overview

3.1.1 TQMP2020 block diagram

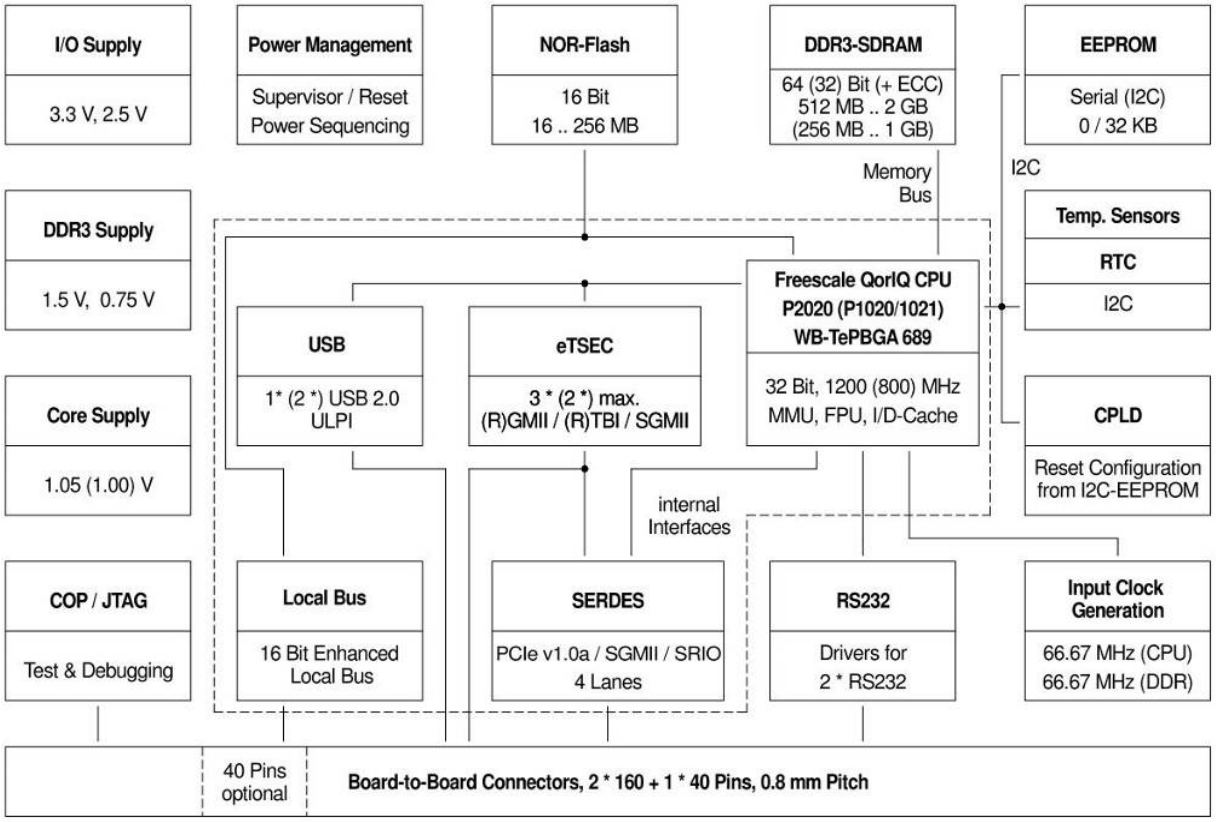


Illustration 1: TQMP2020 block diagram

3.1.2 TQMP2020 System components

- QorIQ processor P2020 or P2010, optional P1020/11 and P1021/12
- Oscillator for CPU clocks
- Reset generator and power fail logic
- CPLD for reset configuration
- Voltage regulator for 2.5 V, 1.8 V, 1.5 V, core voltage VDD, VTT, VREF
- Switch for 3.3 V
- DDR3 SDRAM
- NOR Flash
- Serial EEPROM (data + configuration)
- RTC
- Temperature sensors
- RS232 driver for two serial interfaces
- Board-to-board connector system

3.2 Function groups

3.2.1 CPU

As an alternative to the P2020, (dual core) a P2010 (single core) can be assembled on the same TQMP2020.
Unless otherwise noted, the name P2020 also stands for the P2010 in the following, and equally for derivatives with and without encryption engine.
The P2020 offers a large number of interfaces. On account of high data rates, special care has to be taken concerning the interfaces mentioned in the following.

3.2.1.1 eTSEC Parallel Modes

Three TQMP2020 Gigabit Ethernet interfaces are implemented via eTSECs. All relevant pins are routed to the TQMP2020 connectors, to enable the usage of all possible interface modes supported by the CPU.
PHY and magnetics have to be integrated on the carrier board for RF-technical reasons.

- **MII mode**
  - Highest frequency to be transmitted: 25 MHz (Tx- and Rx clock 100 Mbit/s)
- **RMII mode**
  - Highest frequency to be transmitted: 50 MHz (Tx- and Rx clock @ 100 Mbit/s)
  - Lower number of signals than with MII
  - Timing is tighter than with MII, because both clock edges are used
- **GMII-and TBI mode**
  - Highest frequency to be transmitted: 125 MHz (Tx- and Rx clock @ 1 Gbit/s)
  - Transmit clock changes signal of GTX_CLK to TX_CLK as well as direction with fallback to 10/100 Mbit/s (MII)
- **RGMII-and RTBI mode**
  - Highest frequency to be transmitted: 125 MHz (Tx- and Rx clock @ 1 Gbit/s)
  - Lower number of signals than with (G)MII or TBI
  - Timing tighter than with (G)MII and TBI, because both clock edges are used
  - Source clocking

The interface mode configuration is carried out via the CPLD, which reads the configuration from the configuration EEPROM. See also 3.2.3. The above-described interfaces, except RGMII, are supported by the P2020 as well as the P2010.
With all other CPUs, (P1020/11 as well as P1021/12) only two eTSECs (eTSEC1 / 3) can be used in “Parallel Mode” with RGMII.
The following table shows the possible eTSEC configurations.

Table 2: eTSEC configuration P2020/P2010 (P1020/P1011, P1021/P1012)

eTSEC1	eTSEC2	eTSEC3
Standard interface Inactive	Standard interface SGMII Inactive	 SGMII Inactive
Reduced interface Inactive	Reduced interface SGMII Inactive	 SGMII Inactive
 Inactive	SGMII Inactive	SGMII Inactive
<u>Reduced interface</u> <u>Inactive</u>	<u>Reduced interface</u> <u>SGMII</u> <u>Inactive</u>	<u>Reduced interface</u> <u>SGMII</u> <u>Inactive</u>

<u>Underlined</u>: also P1020/1011 and P1021/1012

Standard interfaces: GMII, TBI, MII
Reduced interfaces: RGMII, RTBI, RMII

Attention: I/O voltages in “Parallel Mode”	
	If the “Parallel Mode” is used, the I/O voltages at the CPU (= LVDD) and at the PHYs must be the same. See also 3.3.2.3.

3.2.1.2 Serializer/Deserializer (SerDes)

The SerDes controller can be operated as a SGMII, PCI Express or Serial Rapid I/O:

- SGMII Highest frequency to be transmitted: 625 MHz (1.25 Gbit/s)
- PCI Express Highest frequency to be transmitted: 1.25 GHz (2.5 Gbit/s)
- Serial Rapid I/O Highest frequency to be transmitted: 1.563 GHz (3.125 Gbit/s)

Serial Rapid I/O (SRIO) is only supported by the P2020 and the P2010.
The following table shows the possible SerDes controller configurations.

Table 3: SerDes configuration P2020/P2010 (P1020/P1011, P1021/P1012)

SerDes lanes				Gbaud	
0	1	2	3	0 & 1	2 & 3
PEX1: × 1	Off	Off	Off	2.5	–
PEX1: × 1	PEX2: × 1	PEX3: × 2		2.5	2.5
PEX1: × 2		PEX3: × 2		2.5	2.5
PEX1: × 4				2.5	
SRIO2: × 1	SRIO1: × 1	Off	Off	3.125	–
SRIO2: × 4				1.25 / 2.5 / 3.125	
SRIO2: × 1	SRIO1: × 1	SGMII2	SGMII3	1.25 / 2.5	1.25
PEX1: × 1	SRIO1: × 1	SGMII2	SGMII3	2.5	1.25
PEX1: × 1	PEX2: × 1	SGMII2	SGMII3	2.5	1.25
PEX1: × 2		SGMII2	SGMII3	2.5	1.25
Off	Off	Off	Off	–	–

Underlined: also P1020/11 and P1021/12

The SerDes controller configuration is carried out via the CPLD, which reads the configuration from the EEPROM SE97B.
See also 3.2.3, and Table 2.

3.2.1.3 USB

In contrast to P2020/10 and the P1021/12, the P1020/11 possesses two USB controllers.
Because Local Bus and USB2 are multiplexed with the P1020/11, the second USB-PHY (ULPI) must be connected at the Local Bus. This means that the second USB-PHY is very limited in its function, or the NOR flash can only be partly used.

3.2.2 Reset logic and voltage supervision

The reset logic contains the following functions:

- The following voltages on the TQMP2020 are supervised:
  - 3.3 V, 2.5 V, 1.8 V, 1.5 V
  - VDD (core voltage)
  - VREF (reference voltage for DDR3 SDRAM)
  - VTT (termination voltage for DDR3 SDRAM)

- External reset input (debounced with 200 ms delay)
- PGOOD output (e.g., for power sequencing of an external PHY)
- Reset state indication by a LED (HRESET# low ⇨ LED lights up)

The supply voltage tolerance range is:
VCC3V3ID = 3.201 V to 3.465 V = 3.3 V –3% / +5%

Permitted voltage range for CPU and 3.3 V logic:
VCC3V3 = 3.135 V to 3.465 V

The voltage supervision tolerance and the voltage drop in VCC3V3 is taken into account:
V_{Reset} = 3.135 V to 3.201 V

The required core voltage depends on the CPU (P2 or P1). It is set by component placement, and by supervisor configuration. This setting cannot be changed.

3.2.2.1 Reset LED

- LED is controlled via the HRESET#-Signal; HRESET# low ⇨ LED lights up
- The supervisor extends the HRESET# pulse for at least 200 ms.
  Thereby the reset is visible even if the reset pulse at RESIN# is very short.

3.2.2.2 Self-Reset

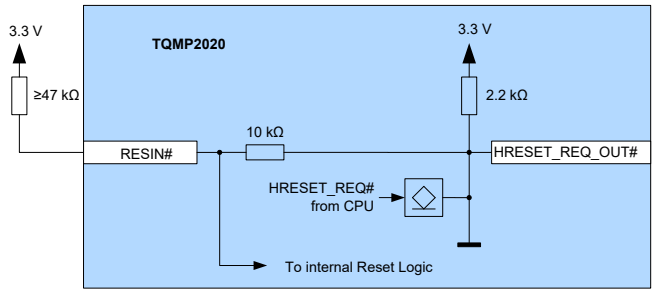
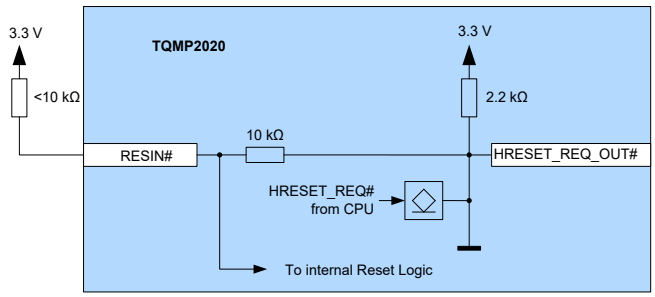
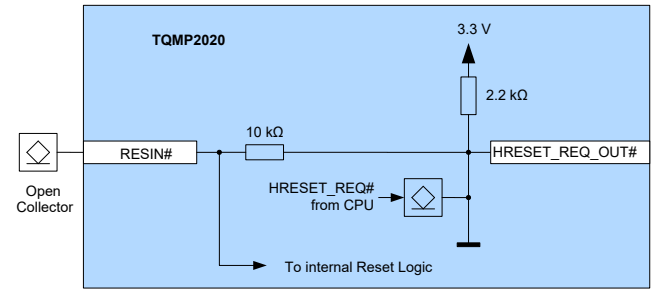
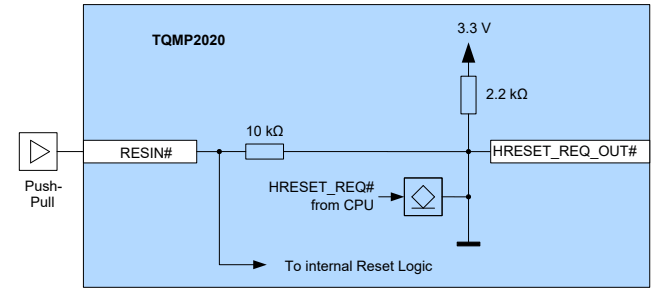
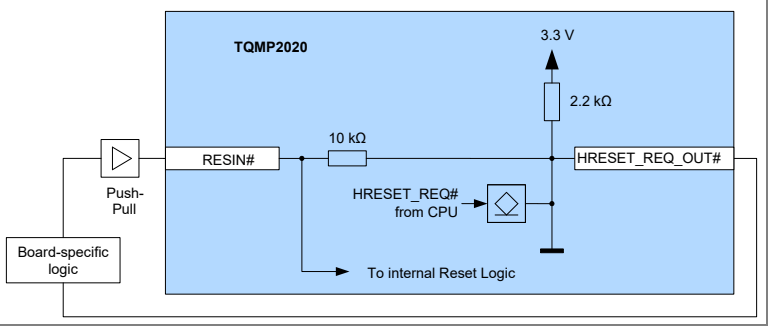
The P2020 can request a hardware reset by software. The signal HRESET_REQ# signals the reset requirement.
A hardware reset can be triggered by writing to register bit RSTCR[HRESET_REQ].
The following participants can also trigger HRESET_REQ#:

- Boot sequencer error (Preamble, CRC)
- eSDHC boot loader error (e.g., boot signature)
- eSPI boot loader error (e.g., boot signature)
- Uncorrectable eLBC ECC Error during boot phase of NAND flash
- Rapid I/O
- e500 watchdog

3.2.2.2 Self-Reset (continued)

The following RESIN# wirings show different possibilities to connect RESIN #.

Table 4: RESIN# connection

Self-Reset performed when HRESET_REQ# asserted.	
No Self-Reset performed when HRESET_REQ# asserted.	
Self-Reset performed when HRESET_REQ# asserted, external reset signal connected to RESIN#.	
No Self-Reset performed when HRESET_REQ# asserted, external reset signal connected to RESIN#.	
Self-Reset via external reset signal using additional logic.	

3.2.2.2 Self-Reset (continued)

The following table shows the reset options, depending on the RESIN# signal wiring.

Table 5: Reset options

Wiring at RESIN#	Reset function
Open-Drain	Self-Reset possible Logic Low at RESIN# triggers RESET
Open, or Pull-up ≥47 kΩ to 3.3 V	Self-Reset possible HRESET_REQ# can trigger RESIN# on TQMP2020
Pull-up <10 kΩ to 3.3 V	**No** Self-Reset possible HRESET_REQ# cannot trigger RESIN# on TQMP2020
Push/Pull driver	**No** Self-Reset, but external RESET possible Logic High at RESIN# overrides HRESET_REQ# on TQMP2020

3.2.2.3 JTAG reset TRST#

TRST# will be pulled low by HRESET#, it can still however be triggered separately (COP/JTAG-Debugging).
This is achieved with the following circuit on the TQMP2020.

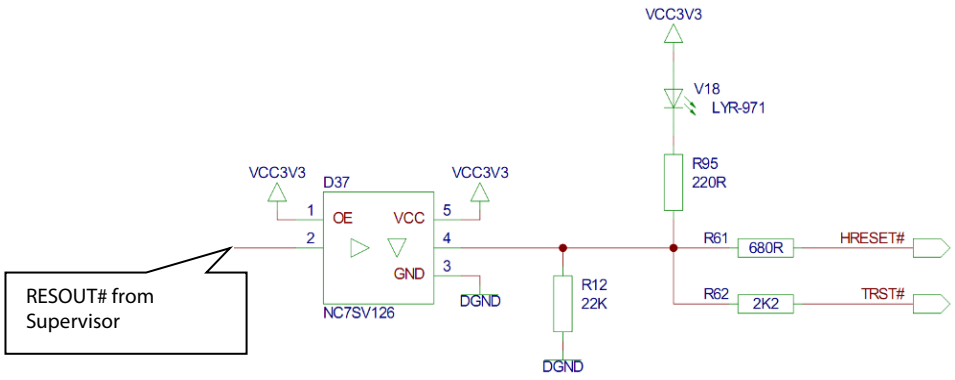


Illustration 2: Wiring of TRST#

3.2.3 CPU configuration

Table 6: Legend for Table 7, Table 8 and Table 9

Binary value in bold	"Default" (NXP) ⇨ internal value if nothing is connected (internal pull-up)
Binary value greyed out	"Reserved" ⇨ do not use
Light green highlighted	Value is fixed in the design (not alterable)
Dark green highlighted	Value is set in the design by comparators (not by CPLD / EEPROM)
Blue highlighted	Default values of CPLD

3.2.3.1 Hardware Reset configuration

The signals listed in column 2 (I/O signal at P2020) define the CPU reset configuration on the TQMP2020.

Table 7: Reset configuration

Config signal	I/O signal at P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_boot_seq[0:1]	LGPL3/LFWP#, LGPL5	PORBMSR[10:11]	00	Reserved	Reserved
			01	Boot sequencer is enabled on I2C1 with normal I²C addressing mode.	Boot sequencer is enabled on I2C1 with normal I²C addressing mode.
			10	Boot sequencer is enabled on I2C1 with extended I²C addressing mode.	Boot sequencer is enabled on I2C1 with extended I²C addressing mode.
			11	**Boot sequencer is disabled. No I²C ROM is accessed.**	**Boot sequencer is disabled. No I²C ROM is accessed.**
cfg_sys_pll[0:2]	LA[29:31]	PORPLLSR[26:30]	000	4:1	4:1
			001	5:1	5:1
			010	6:1	6:1
			011	8:1	Reserved
			others	Reserved	Reserved
cfg_core0_pll[0:2]	LBCTL, LALE, LGPL2/LOE#/LFRE#	PORPLLSR[10:15]	000	4:1	Reserved
			001	9:2 (4.5:1)	Reserved
			010	1:1	1:1
			011	3:2 (1.5:1)	3:2 (1.5:1)
			100	2:1	2:1
			101	5:2 (2.5:1)	5:2 (2.5:1)
			110	3:1	3:1
			111	7:2 (3.5:1)	Reserved
cfg_core1_pll[0:2]	LWE0#, UART_SOUT1, READY_P1	PORPLLSR[2:7]	000	4:1	Reserved
			001	9:2 (4.5:1)	Reserved
			010	1:1	1:1
			011	3:2 (1.5:1)	3:2 (1.5:1)
			100	2:1	2:1
			101	5:2 (2.5:1)	5:2 (2.5:1)
			110	3:1	3:1
			111	7:2 (3.5:1)	Reserved

Config signal	I/O signal at P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_ddr_pll[0:2]	TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT[1:2]	PORPLLSR[18:22]	000	Reserved	3:1
			001	4:1	4:1
			010	6:1	6:1
			011	8:1	8:1
			100	10:1	10:1
			101	12:1	Reserved
			110	Reserved	Reserved
			111	Synchronous mode	Synchronous mode
cfg_srds_pll_toe	TRIG_OUT/READY_P0	PORDEVSR2[10]	0	Enable PLL lock time-out counter, POR-sequence waits for SerDes PLL to lock while time-out counter has not expired	Not used
			1	**Disable PLL lock time-out counter, POR-sequence waits for SerDes PLL to lock**	Not used
cfg_plat_speed	LA23	PORDEVSR2[14]	0	Platform clock <333 MHz	Platform clock <300 MHz and >267 MHz
			1	**Platform clock ≥333 MHz**	**Platform clock ≥300 MHz**
cfg_core0_speed	LA24	PORDEVSR2[12]	0	Core 0 clock ≤1 GHz	Core 0 clock ≤450 MHz
			1	**Core 0 clock >1 GHz**	**Core 0 clock >450 MHz**
cfg_core1_speed	LA25	PORDEVSR2[13]	0	Core 1 clock ≤1 GHz	Core 1 clock ≤450 MHz
			1	**Core 1 clock >1 GHz**	**Core 1 clock >450 MHz**
cfg_ddr_speed	LA26	PORDEVSR2[15]	0	DDR clock <500 MHz	DDR clock <450 MHz
			1	**DDR clock ≥500 MHz**	**DDR clock ≥450 MHz**
cfg_sys_speed	LA28	PORDEVSR2[21]	0	System clock <66 MHz	Reserved
			1	**System clock ≥66 MHz**	**System clock ≥66 MHz**
cfg_cpu[0:1]_boot	LA27, LA16	PORBMSR[0:1]	00	CPU boot holdoff mode for both cores. The e500 cores are prevented from booting until configured by an external master.	CPU boot holdoff mode for both cores. The e500 cores are prevented from booting until configured by an external master.
			01	e500 core 1 is allowed to boot without waiting for configuration by an external master, while e500 core 0 is prevented from booting until configured by an external master or the other core.	e500 core 1 is allowed to boot without waiting for configuration by an external master, while e500 core 0 is prevented from booting until configured by an external master or the other core.
			10	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core.	e500 core 0 is allowed to boot without waiting for configuration by an external master, while e500 core 1 is prevented from booting until configured by an external master or the other core.
			11	Both e500 cores are allowed to boot without waiting for configuration by an external master.	**Both e500 cores are allowed to boot without waiting for configuration by an external master.**
cfg_ddr_debug	DMA2_DDONE0#	PORDBGMSR[7]	0	ECC pins driven Debug info instead of normal ECC I/O. (disconnect memory devices)	ECC pins driven Debug info instead of normal ECC I/O. (disconnect memory devices)
			1	**ECC pins in normal mode**	**ECC pins in normal mode**
cfg_device_ID[7:5]	TSEC2_TXD[4:2]	PORDEVSR[29:31]	xxx-----	Device ID LSBs for Rapid I/O hosts	Not used

Config signal	I/O signal at P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_dram_type	TSEC2_TXD1	PORDEVSR[25]	0	DDR2 1.8 V, CKE low @ reset	DDR2 1.8 V, CKE low @ reset
			1	**DDR3 1.5 V, CKE low @ reset**	**DDR3 1.5 V, CKE low @ reset**
cfg_elbc_ecc	MSRCID0	PORDEVSR[15]	0	eLBC ECC checking disabled	eLBC ECC checking disabled
			1	**eLBC ECC checking enabled**	**eLBC ECC checking enabled**
cfg_eng_use[0:7]	LA[20:22], UART_SOUT0, *TRIG_OUT/READY_P0*, MSRCID1, MSRCID4, DMA1_DDONE#	PORDEVSR2	000x0000	Reserved for engineering use	Not used
			...	Reserved for engineering use	Not used
			111x1110	Reserved for engineering use	Not used
			111x1111	**Default (see cfg_srds_pll_toe)**	Not used
cfg_host_agt[0:2]	LWE1#/LBS1, LA[18:19]	PORBMSR[13:15]	000	Agent on all PCIe and SRIO	Agent on all PCIe
			001	Agent on PCIe 1 or host SRIO 2, Host on PCIe 2 / SRIO 1, Host on PCIe 3	Agent on PCIe 1, Host on PCIe 2
			010	Host on PCIe 1 or agent SRIO 2, Agent on PCIe 2 / SRIO 1, Host on PCIe 3	Host on PCIe 1, Agent on PCIe 2
			011	Host on PCIe 1 / SRIO 2, Host on PCIe 2 / SRIO 1, Agent on PCIe 3	Reserved
			100	Agent on PCIe 1 / SRIO 2, Agent on PCIe 2 / SRIO 1, Host on PCIe 3	Reserved
			101	Agent on PCIe 1 or host SRIO 2, Host on PCIe 2 / SRIO 1, Agent on PCIe 3	Reserved
			110	Host on PCIe 1 or agent SRIO 2, Agent on PCIe 2 / SRIO 1, Agent on PCIe 3	Reserved
			111	**Host processor / root complex for all PCIe / SRIO**	**Host processor / root complex for all PCIe**

Config signal	I/O signal at P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_io_ports[0:3]	TSEC1_TXD[3:1], TSEC2_TX_ER	PORDEVSR[9:12]	0000	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, SerDes lanes 1-3 powered down	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, SerDes lanes 1-3 powered down
			0001	SerDes lanes 0-3 powered down	SerDes lanes 0-3 powered down
			0010	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, PCIe 2 (x1) (2.5 Gbps) → SerDes lane 1, PCIe 3 (x2) (2.5 Gbps) → SerDes lane 2-3	Reserved
			0011	Reserved	Reserved
			0100	PCIe 1 (x2) (2.5 Gbps) → SerDes lane 0-1, PCIe 3 (x2) (2.5 Gbps) → SerDes lane 2-3	Reserved
			0101	Reserved	Reserved
			0110	PCIe 1 (x4) (2.5 Gbps) → SerDes lane 0-3	PCIe 1 (x4) (2.5 Gbps) → SerDes lane 0-3
			0111	SRIO 2 (1x) (3.125 Gbps) → SerDes lane 0, SRIO 1 (1x) (3.125 Gbps) → SerDes lane 1, SerDes lanes 2-3 powered down	Reserved
			1000	SRIO 2 (4x) (1.25 Gbps) → SerDes lane 0-3	Reserved
			1001	SRIO 2 (4x) (2.5 Gbps) → SerDes lane 0-3	Reserved
			1010	SRIO 2 (4x) (3.125 Gbps) → SerDes lane 0-3	Reserved
			1011	SRIO 2 (1x) (1.25 Gbps) → SerDes lane 0, SRIO 1 (1x) (1.25 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	Reserved
			1100	SRIO 2 (1x) (2.5 Gbps) → SerDes lane 0, SRIO 1 (1x) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	Reserved
			1101	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, SRIO 1 (1x) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	Reserved
			1110	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, PCIe 2 (x1) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3	PCIe 1 (x1) (2.5 Gbps) → SerDes lane 0, PCIe 2 (x1) (2.5 Gbps) → SerDes lane 1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3
			1111	**PCIe 1 (x2) (2.5 Gbps) → SerDes lane 0-1 SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2 SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3**	**PCIe 1 (x2) (2.5 Gbps) → SerDes lane 0-1, SGMII 2 (x1) (1.25 Gbps) → SerDes lane 2, SGMII 3 (x1) (1.25 Gbps) → SerDes lane 3**
cfg_mem_debug	DMA2_DACK0#	PORDBGMSR[5]	0	Debug info from eLBC is driven on MSRCID and MDVAL	Debug info from eLBC is driven on MSRCID and MDVAL
			1	**Debug info from DDR is driven on MSRCID and MDVAL**	**Debug info from DDR is driven on MSRCID and MDVAL**
cfg_rio_sys_size	LGPL0/LFCLE	PORDEVSR[28]	0	Large system size (up to 65536 devices)	Not used
			1	**Small system size (up to 256 devices)**	Not used

Config signal	I/O signal at P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_rom_loc[0:3]	TSEC1_TXD[6:4], TSEC1_TX_ER	PORBMSR[4:7]	0000	PCIe 1	PCIe 1
			0001	PCIe 2	PCIe 2
			0010	SRIO 1	Reserved
			0011	SRIO 2	Reserved
			0100	DDR	DDR
			0101	PCIe 3	Reserved
			0110	On-Chip boot ROM - SPI config	On-Chip boot ROM - SPI config
			0111	On-Chip boot ROM - eSDHC config	On-Chip boot ROM - eSDHC config
			1000	eLBC FCM - 8-bit NAND small page	eLBC FCM - 8-bit NAND small page
			1001	Reserved	Reserved
			1010	eLBC FCM - 8-bit NAND large page	eLBC FCM - 8-bit NAND large page
			1011	Reserved	Reserved
			1100	Reserved	Reserved
			1101	eLBC GPCM - 8-bit ROM	eLBC GPCM - 8-bit ROM
			1110	eLBC GPCM - 16-bit ROM	eLBC GPCM - 16-bit ROM
			1111	**eLBC GPCM - 16-bit ROM (formerly probably GPCM - 32-bit)**	**eLBC GPCM - 16-bit ROM (formerly probably GPCM - 32-bit)**
cfg_sgmii2	LGPL1/LFALE	PORDEVSR[3]	0	eTSEC2 (SGMII) → SGMII SerDes lane 2 pins	Not used
			1	**eTSEC2 (Std.) → TSEC2_* pins**	Not used
cfg_sgmii3	TSEC_1588_ALARM_OUT2	PORDEVSR[4]	0	eTSEC3 (SGMII) → SGMII SerDes lane 3 pins	eTSEC3 → SGMII
			1	**eTSEC3 (Std.) → TSEC3_* pins**	**eTSEC3 → RGMII**
cfg_srds_refclk	TSEC_1588_ALARM_OUT1	PORDEVSR2[18]	0	SerDes Ref Clock = 125 MHz	SerDes Ref Clock = 125 MHz
			1	**SerDes Ref Clock = 100 MHz**	**SerDes Ref Clock = 100 MHz**
cfg_tsec_reduce	EC_MDC	PORDEVSR[0]	0	eTSEC1 & eTSEC2 in reduced pin mode (RTBI, RGMII, RMII)	eTSEC1 in reduced mode (RGMII)
			1	**eTSEC1 & eTSEC2 in std. width (TBI, GMII, MII)**	**Reserved**
cfg_tsec1_prtcl[0:1]	TSEC1_TXD0, TSEC1_TXD7	PORDEVSR[6:7]	00	Reserved	Reserved / eTSEC1 → SGMII
			01	ETSEC1 → MII / RMII	Reserved / eTSEC1 → SGMII
			10	ETSEC1 → GMII / RGMII	eTSEC1 → RGMII
			11	**ETSEC1 → TBI / RTBI**	**Reserved /** eTSEC1 → SGMII
cfg_tsec2_prtcl[0:1]	TSEC2_TXD0, TSEC2_TXD7	PORDEVSR[18:19]	00	Reserved	Not used
			01	ETSEC2 → MII / RMII (if not configured to SGMII)	Not used
			10	ETSEC2 → GMII / RGMII (if not configured to SGMII)	Not used
			11	**eTSEC2 → TBI / RTBI (if not configured to SGMII)**	Not used
cfg_tsec3_prtcl[0:1]	UART_RTS[0:1]#	PORDEVSR[20:21]	00	Reserved	Reserved / eTSEC3 → SGMII
			01	eTSEC3 → RMII (if not configured to SGMII)	Reserved / eTSEC3 → SGMII
			10	eTSEC3 → RGMII (if not configured to SGMII)	eTSEC3 → RGMII
			11	**eTSEC3 → RTBI (if not configured to SGMII)**	**Reserved / eTSEC3 → SGMII**
cfg_sdhc_cd_pol_sel	TSEC2_TXD5/TSEC3_TX_EN	PORDEVSR[23]	0	eSDHC Card-detect polarity is not inverted	Not used
			1	**eSDHC Card-detect polarity is not inverted**	**Not used**

3.2.3.2 Additional available reset configuration signals

The signals listed in the following table are not used on the TQMP2020. The carrier board can pass additional configuration data to the CPU using these signals, if desired. These do not influence the CPU configuration by hardware after a reset, but can merely be utilised by software.

Table 8: Free reset configuration (general purpose)

Config signal	I/O-Signal at P2020	Register	Value	Meaning P2020	Meaning P1020 / P1021
cfg_gpinput[0:15]	LAD[0:15]	GPPORCR[0:15]	0xnnnn_0000	General-purpose POR config → not used	General-purpose POR config → not used

3.2.3.3 Other configuration signals

The TQMP2020 generates the signals listed in the following table. They are not read during reset, but must be applied permanently.

Table 9: Static configuration signals

Config signal	I/O-Signal at the P2020	Register	Value	Function P2020	Function P1020 / P1021
LVDD_VSEL	LVDD_VSEL	IOVSELSR[30:31]	0	3.3 V: eTSEC[1:3], Eth. Management, 1588	3.3 V: eTSEC[1:3], Eth. Management, 1588
			1	2.5 V: eTSEC[1:3], Eth. Management, 1588	2.5 V: eTSEC[1:3], Eth. Management, 1588
BVDD_VSEL[0:1]	BVDD_VSEL[0:1]	IOVSELSR[26:27]	00	3.3 V: Local Bus, GPIO[8:15]	3.3 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
			01	2.5 V: Local Bus, GPIO[8:15]	2.5 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
			10	1.8 V: Local Bus, GPIO[8:15]	1.8 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
			11	3.3 V: Local Bus, GPIO[8:15]	3.3 V: Local Bus, GPIO[8:15] / CE_PB*, CE_PC0
CVDD_VSEL[0:1]	CVDD_VSEL[0:1]	IOVSELSR[22:23]	00	3.3 V: USB, eSDHC, SPI	3.3 V: USB, eSDHC, SPI
			01	2.5 V: USB, eSDHC, SPI	2.5 V: USB, eSDHC, SPI
			10	1.8 V: USB, eSDHC, SPI	1.8 V: USB, eSDHC, SPI
			11	3.3 V: USB, eSDHC, SPI	3.3 V: USB, eSDHC, SPI

3.2.3.4 EEPROM SE97B, Reset-configuration

The following table shows the configuration data in the EEPROM of the SE97B at address `0x57 / 101 0111b`.
The single fields with configuration data consist in each case of an Enable bit plus the actual data field:

Enable 0 = Tri-State 1 = Actively driven during Reset	Configuration data see Table 7

Table 10: EEPROM SE97B, Hard Reset Configuration Word

Byte	Content							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Fixed Configuration ID							
	0	0	1	0	1	0	1	0
1	Enable	cfg_boot_seq[0:1]		Enable	cfg_sys_pll[0:2]			Enable
2	cfg_core0_pll[0:2]			Enable	cfg_core1_pll[0:2]			Enable
3	cfg_ddr_pll[0:2]			Enable	cfg_srds_pll_toe	Enable	cfg_plat_speed	Enable
4	cfg_core0_speed	Enable	cfg_core1_speed	Enable	cfg_ddr_speed	Enable	cfg_sys_speed	Enable
5	cfg_cpu[0:1]_boot		Enable	cfg_ddr_debug	Enable	cfg_device_ID[7:5]		
6	Enable	cfg_dram_type	Enable	cfg_elbc_ecc	Enable	cfg_eng_use[0:2]		
7	cfg_eng_use[3:7]					Enable	cfg_host_agt[0:1]	
8	cfg_host_agt[2]	Enable	cfg_io_ports[0:3]				Enable	cfg_mem_debug
9	Enable	cfg_rio_sys_size	Enable	cfg_rom_loc[0:3]				Enable
10	cfg_sgmii2	Enable	cfg_sgmii3	Enable	cfg_srds_refclk	Enable	cfg_tsec_reduce	Enable
11	cfg_tsec1_prtcl[0:1]		Enable	cfg_tsec2_prtcl[0:1]		Enable	cfg_tsec3_prtcl[0:1]	
12	Enable	cfg_sdhc_cd_pol_sel	(Unused)	(Unused)	(Unused)	(Unused)	(Unused)	(Unused)
13	CRC checksum							

Note: Invalid Hard Reset Configuration Word in SE97B EEPROM

An altered reset configuration can lead to an unbootable system.
In this case there are two options to return to a functioning reset configuration:

1: Connect an external master (Programmer) at the I²C bus 1.
TQ-Support can recommend a suitable tool.

2: Recovery by TQMP2020 software:
The software in the NOR flash on the TQMP2020 has to run with the default reset configuration, and the I²C bus has to be accessible. For a “how to” see chapter 3.2.3.5, Tip 1.

3.2.3.5 Error handling and default configuration

The CPLD transmits a reset sequence on the I2C bus (IIC1) before the actual access.
This ensures that accesses still running during reset, are completed and the EEPROM is ready to be read.
To ensure the system integrity, the configuration mechanism handles the following errors:

- I²C protocol error
- Configuration ID missing
- CRC incorrect

In these cases, the CPLD starts another attempt. If this also fails, the default configuration will be passed to the CPU (highlighted in blue in Table 7). This guarantees that the system boots, but with certain functional limitations (lower clock, interfaces partly not available).
The CRC uses the polynomial x8 + x2 + x + 1 and the start value 0xFF. A tool, which calculates the CRC, can be provided.

Tip 1
Altered or erased configuration data generates a CRC error, which causes the default configuration to be loaded. When the system has booted with default configuration, the EEPROM can be rewritten. Another possibility is, to pull IIC1_SDA "low". This leads to a protocol error (NACK) and therefore the default configuration to be used. In this manner a system can operate with two different boot configurations: e.g., a normal operation (SE97B EEPROM) with boot process via PCIe or eSDHC and a service or emergency operation (default-config) with boot loader in the NOR flash.

Tip 2
The enable-bits enable the configuration of single fields not via the TQMP2020, but via the carrier board without reprogramming the EEPROM. Thus, e.g., the field "cfg_device_ID" can be configured with different Device-IDs depending on the carrier board. Pull-ups / pull-downs or active drivers (driver conflicts possible) must be provided on the carrier board for this. During Reset and Power-Up the corresponding signals are driven by the CPLD. Since these signals are outputs of the CPU or the TQMP2020, possible driver's conflicts must be taken into account in the carrier board design. The signals UART_SOUT0# (cfg_eng_use3), UART_SOUT1# (cfg_core1_pll1) and TSEC2_TXD5/TSEC3_TX_EN (cfg_sdhc_cd_pol_sel) are an exception. During Reset these signals are separated from the TQMP2020-connector to maintain system integrity.

3.2.3.6 Settings via boot sequencer

The CPU configuration with CPU specific boot sequencer cannot replace the configuration via the CPU pins, but only complement. Because it runs before the software starts, it can carry out additional settings, which cannot or should not be set by software. The standard software delivered with the TQMP2020 (U-Boot) does not depend on the boot sequencer.

The standard software (U-Boot) delivered with the TQMP2020 does not rely on the boot sequencer.

The configuration with the boot sequencer starts after reset.

In certain cases, the configuration via the boot sequencer is indispensable:

- Multiprocessor environments
- Preconfiguration to boot from other systems or interfaces (e.g., PCIe, Rapid I/O, SDRAM...)
- Fixing of incompatibilities with reset values (e.g., bus driver control preset functionality LBCTL)

Note: Invalid data in SE97B EEPROM	
	Invalid data can lead to an unbootable system! This condition can be avoided by temporary activating the default configuration, since the boot sequencer is deactivated in case of invalid data. See also chapter 3.2.3.5, Tip 2.

Attention: Maximum I2C bus clock	
	The CPU clocks the I²C bus with 160 kHz when the boot sequencer is used. Devices, which can only work at a maximum of 100 kHz, may not be connected to IIC1, when the boot sequencer is enabled. This only affects the carrier board as all I²C bus devices on the TQMP2020 can operate at 400 kHz.

3.2.4 Clock

3.2.4.1 P2020/2010 internal clock structure

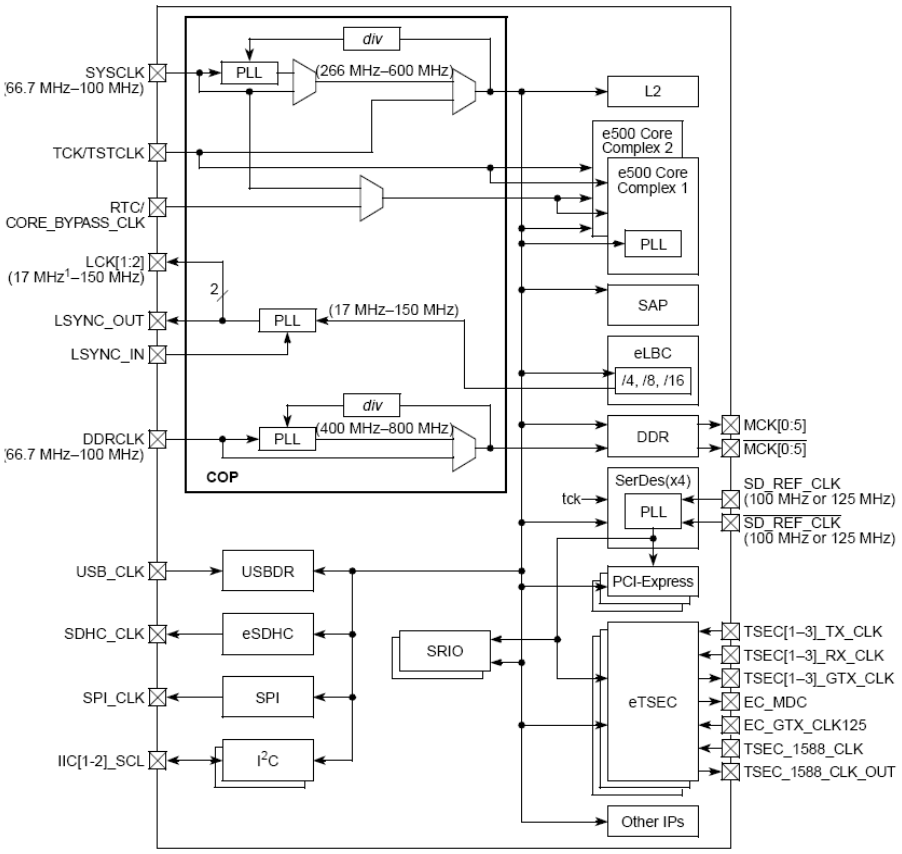


Illustration 3: P2020/2010 clock subsystem, block diagram

(Source: NXP)

3.2.4.2 P1020/1011 and P1021/1012 internal clock structure

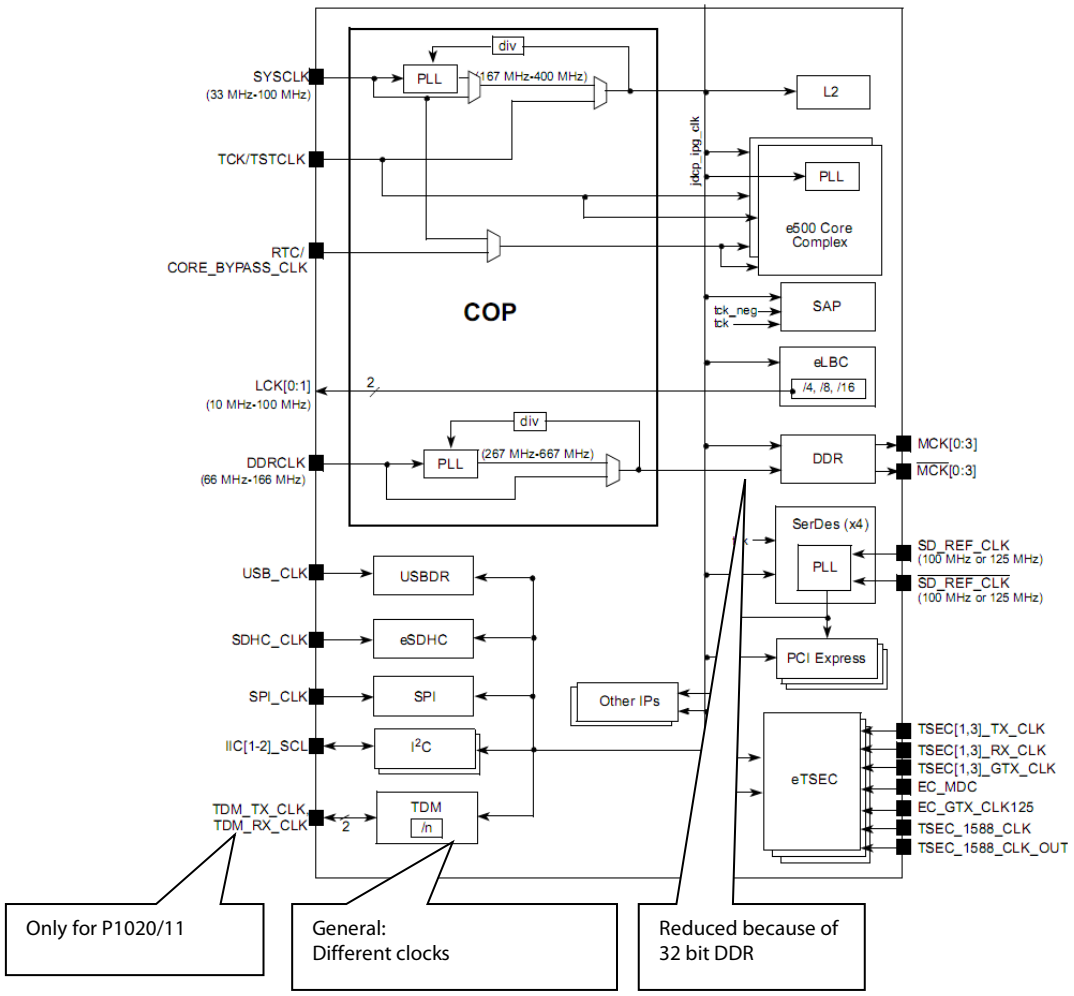


Illustration 4: P1020/1011 and P1021/1012 clock subsystem, block diagram

(Source: NXP)

3.2.4.3 System clock SYSCLK

In normal operation, SYSCLK is generated on the TQMP2020.

The Platform- or Core-Complex-Bus clock (see 3.2.4.4) is generated by multiplication from this.

The Memory bus clock (see 0) can also be generated.

The frequency is 66.666 MHz.

Spread spectrum clocking is possible on request, but not standard.

3.2.4.4 Core-Complex-Bus clock CCB_CLK

The Platform- or Core-Complex-Bus clock CCB_CLK is generated from the system clock signal SYSCLK by multiplication. The multiplication factor is fixed by the reset configuration. The signal merely exists CPU internally. It is used for the L2 cache (internal) as well as for the Local Bus and other interfaces.

The frequency is set to 400 MHz by default.

Core frequencies of 600, 800, 1000 and 1200 MHz are possible with it, see 3.2.4.5.

TQMP1xxx: 266 / 333 / 400 / 533 MHz = 0.5 × frequency CORE_CLK or constant 266 MHz.

3.2.4.5 Processor Core clock CORE_CLK

The core clock CORE_CLK is generated by multiplication from CCB_CLK.
The multiplication factor is fixed by the reset configuration.
The signal merely exists CPU internally and is used for the e500v2 core(s).
Possible frequencies are 600, 800, 1000 or 1200 MHz.

TQMP1020, TQMP1021: 333 to 800 MHz, gradation depending on CCB_CLK and multiplication factors.

3.2.4.6 Local Bus clock LCLK

The Local Bus clock LCLK is generated from CCB_CLK divided by LCRR[CLKDIV] (values 4, 8 or 16). The division factor LCRR[CLKDIV] is configurable at run time.
The signal is used for the Local Bus.
Possible frequencies with CCB_CLK = 400 MHz are 25, 50, 100 MHz.
The maximum possible frequency LCLK for the P2020 is 150 MHz.

TQMP1xxx:

- *with CCB_CLK = 400 MHz: 25, 50 MHz*
- *with CCB_CLK = 267 MHz: 17, 33, 66 MHz*

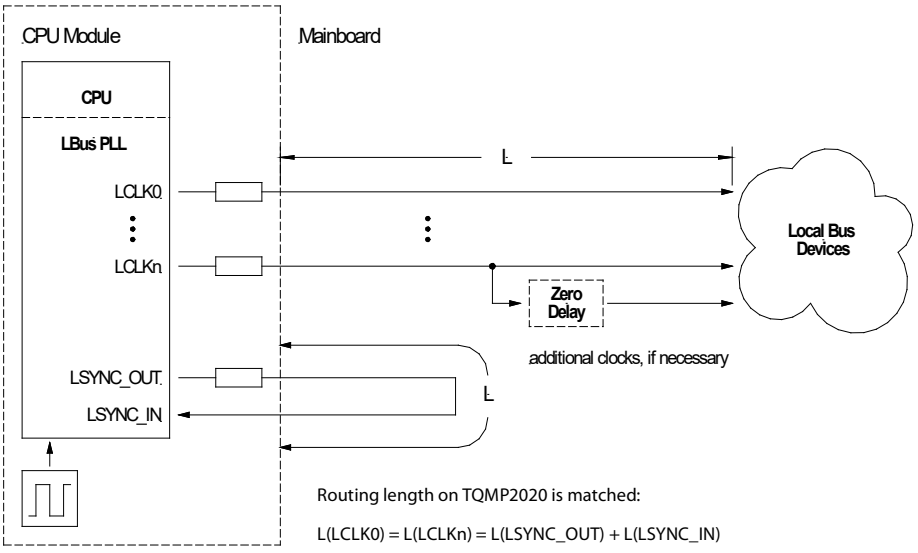


Illustration 5: Length alignment Local Bus

Two clock outputs LCLK[0:1] are routed to the connectors. A zero-delay buffer has to be provided on the carrier board, if more participants have to be supplied as clock outputs are available.
The following applies for the feedback:

- A feedback is only required if the Local Bus is used in PLL Enable mode.
- No feedback is required, however, if the PLL Bypass mode is used (it may be present).
- The track length adjustment is only required if participants, which use the clock, are connected to the Local Bus on the carrier board. If this is not the case, the feedback track length is insignificant.
  There are no bus participants on the TQMP2020 requiring the clock.

3.2.4.7 Memory bus clocks: DDRCLK, DDR_CLK, MCKx, MCK#

The Platform clock CCB_CLK can be used as an alternative to the Memory Bus clock DDR_CLK, or be generated by an own PLL from DDRCLK (= SYSCLK).
The Memory Bus clock DDR_CLK corresponds to the DDR data rate, which is twice as high as MCKx and MCK#.
Favourite frequency: DDR_CLK = 800 MHz, which is DDRCLK (66.666 MHz) × 12.

TQMP1xxx: 666 MHz from DDRCLK (66.666 MHz) × 10.

3.2.4.8 Real-Time clock RTC

The signal RTC is a clock input, through which a time base can be created, independent of the system clock.
The signal RTC is available at the connector but not connected on the TQMP2020.
More detailed information can be found in the CPU hardware specification (1).

3.2.4.9 USB clock USB_CLK

The signal USB_CLK is required for the interface to the external USB-PHY. (The USB controller runs synchronically to CCB_CLK).
If USB is used, a 60-MHz clock must be fed at this signal.
More detailed information can be found in the CPU hardware specification (1).

3.2.4.10 SERDES clock SD_REF_CLK/SD_REF_CLK#

The signal pair SD_REF_CLK/SD_REF_CLK# is required for the SERDES interface.
(The system side runs synchronically to CCB_CLK).
If the SERDES interface is used, depending on protocol and data rate, a clock of 100 or 125 MHz must be supplied here.
If no SERDES clock is supplied, the reset configuration has to prevent that the CPU waits for the SERDES-PLL to lock after a reset.
See also cfg_srds_pll_toe, chapter 3.2.3.1.
More detailed information can be found in the CPU hardware specification (1).

3.2.4.11 Standard clock frequencies

Table 11: Standard clock frequencies (with P2020)

Clock	Frequency [MHz]	Remark
SYSCLK	66.666	Input clock system-PLL
CCB_CLK	400	Platform clock
CORE_CLK	1,200	Core clock
LCLK	25 / 50 / 100	Standard frequency underlined
DDRCLK	66.666	Input clock DDR-PLL, frequency identical with SYSCLK
DDR_CLK	800	= Data rate
MCKx/MCKx#	400	= Half data rate = physical clock
RTC	Freely selectable	Not connected on TQMP2020
USB_CLK	60	When required externally
SD_REF_CLK/SD_REF_CLK#	100 / 125	When required externally, frequency depending on protocol and data rate

3.2.5 Local Bus

The available chip selects are assigned as follows:

Table 12: Assignment chip selects at the Local Bus

Chip select	Usage on TQMP2020
LCS0#/CS_NOR#	NOR flash (boot)
LCS1#	Available
LCS2#	Available
LCS3#	Available
LCS4#	Available
LCS5#/DMA2_DREQ1#	Available, if not used for DMA
LCS6#/DMA2_DACK1#	Available, if not used for DMA
LCS7#/DMA2_DDONE1#	Available, if not used for DMA

3.2.6 NOR flash

- 3.3-V flashes Micron PC28FxxxM29EW, alternatively EON EN29GL, 16 bit
- Connected at the Local Bus because of multiplexed addresses and data ⇨ addresses via a latch
- One bank with 16-bit bus
- 16 to 256 Mbyte
- Access time 100 ns
- Chip-select LCS0#

The status signal RY/BY# of the flash is not used by the CPU.
The event of write and erasure cycles must be monitored by polling.

3.2.7 DDR3 SDRAM

- P20xx: 64 bit, with or without ECC
  P10xx: 32 bit, with or without ECC
- P20xx: 512 Mbyte to 2 Gbyte
  P10xx: 256 Mbyte to 1 Gbyte
- P20xx: DDR3-800 (400 MHz clock)
  P10xx: DDR3-667 (333 MHz clock)
- Chip select MCS0#, with stacked DDR also MCS1#

3.2.8 I²C bus

All I²C bus devices on the TQMP2020 are connected to the I²C bus IIC1 of the CPU. Table 13 shows the addresses used.
All devices can operate with a maximum I²C clock of 400 kHz.
The pull-ups available on the TQMP2020 are sufficient for the bus loads on the TQMP2020. If more devices are connected to the bus on the carrier board, additional pull-ups must be assembled on the carrier board, to meet the I²C specification.

Table 13: IIC1 device addresses

Device	Function	7-bit address
M24256	EEPROM	0x50 / 101 0000b
SE97B	EEPROM (Normal Mode)	0x57 / 101 0111b
	EEPROM (Write Protect Mode)	0x37 / 011 0111b
	Temperature Sensor	0x1F / 001 1111b
SA56004EDP [1]	Temperature Sensor [1]	0x4C / 100 1100b
DS1337	RTC	0x68 / 110 1000b
ADM1068	Power Manager	0x44 / 100 0100b

3.2.8.1 EEPROM M24256

The EEPROM M24256 has a capacity of 32 Kbyte (256 Kbit). It can store device-specific data. The EEPROM is an assembly option. It is erased at delivery und fully available for device-specific data. It can i.e., be used for a boot sequencer.
It is connected to I²C controller IIC1 address 0x50 / 101 0000b, see Table 13.

3.2.8.2 Temperature sensor / EEPROM SE97B

A 256 byte EEPROM including temperature sensor is connected to I²C bus 1. The SE97B I²C addresses are listed in Table 13.
At delivery the EEPROM contains a Hard Reset Configuration Word (see 3.2.3.4) and other TQMP2020-specific data, see Table 14.
The EEPROM is one of several possibilities to store the Reset Configuration. A correctly configured system can be restored by setting the Default Reset Configuration in the EEPROM as the Reset Configuration source.
The lower 128 bytes (00h to 7Fh) containing the TQMP2020-specific data, can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. The upper 128 bytes (80h to FFh) are not write protected and can be used for general purpose data storage. The SE97B also provides a temperature sensor to monitor the temperature of the TQMP2020.

The following table shows the TQMP2020-specific data in the SE97B EEPROM.

Table 14: EEPROM SE97B, TQMP2020-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	(Variable)	(Variable)	$48_{(10)}$	Binary	Hard Reset Configuration Word
0x30	(Variable)	(Variable)	$32_{(10)}$	Binary	Copy of Hard Reset Configuration Word
0x50	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	First MAC address
0x60	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x70	(Variable)	(Variable)	$16_{(10)}$	ASCII	Order code
0x80	(Unused)		$128_{(10)}$	–	–

Note: Invalid Hard Reset Configuration Word in SE97B EEPROM

An altered reset configuration can lead to an unbootable system.
In this case there are two options to return to a functioning reset configuration:

3: Connect an external master (Programmer) at the I²C bus 1.
TQ-Support can recommend a suitable tool.

4: Recovery by TQMP2020 software:
The software in the NOR flash on the TQMP2020 has to run with the default reset configuration, and the I²C bus 1 has to be accessible. For a "how to" see chapter 3.2.3.5, Tip 1.

1: Address is compatible to ADT7461, LM86, MAX6657/8 and ADM1032.

3.2.8.3 RTC DS1337U

Since the CPU does not contain a bufferable RTC, a discrete RTC DS1337U is assembled on the TQMP2020.

- RTC DS1337U, controlled via I²C bus
- Battery buffering possible (battery on carrier board at VBAT)
- Alarm outputs INTA# and SQW/INTB# (Open Drain) are routed to a common pin
- Controlled via I²C controller IIC1, address `0x68 / 110 1000b`
- 30 ppm oscillator tolerance over the whole temperature range

3.2.8.4 Temperature supervision

- Control of all sensors via I²C bus IIC1, device addresses see Table 13
- Measuring point 1: CPU die temperature by CPU-internal measuring diode
  Can be read by remote channel of SA56004EDP, address `0x4C / 100 1100b`
- Measuring point 1a (assembly option):
  External sensor between CPU and switching regulator, as an alternative to CPU-internal measuring diode
  Can be read by remote channel of SA56004EDP, address `0x4C / 100 1100b`
- Measuring point 2: PCB bottom side next to DDR3
  Can be read by local channel of SA56004EDP, address `0x4C / 100 1100b`
- Measuring point 3: PCB top side between DDR3 devices
  Can be read by combined device SE97B, address `0x1F / 001 1111b`

3.2.9 General-Purpose I/O

- 16 GPIOs, 9 of it multiplexed with other interface signals
  - P1020: 16 GPIOs
  - P1021: no GPIOs
- Configured as input after power-on reset
- Open drain capable
- Interrupt capable

3.3 Supply

3.3.1 Power sequencing

The TQMP2020 has to be supplied with 3.3 V. All other voltages are generated on the TQMP2020.
The integrated power manager ensures valid power sequencing.
LVDD and CVDD may not be supplied by an external voltage to guarantee a correct power sequencing.
LVDD and CVDD must be fed via the provided pins VCC3V3OUT, VCC2V5OUT or VCC1V8OUT instead (see Illustration 6).

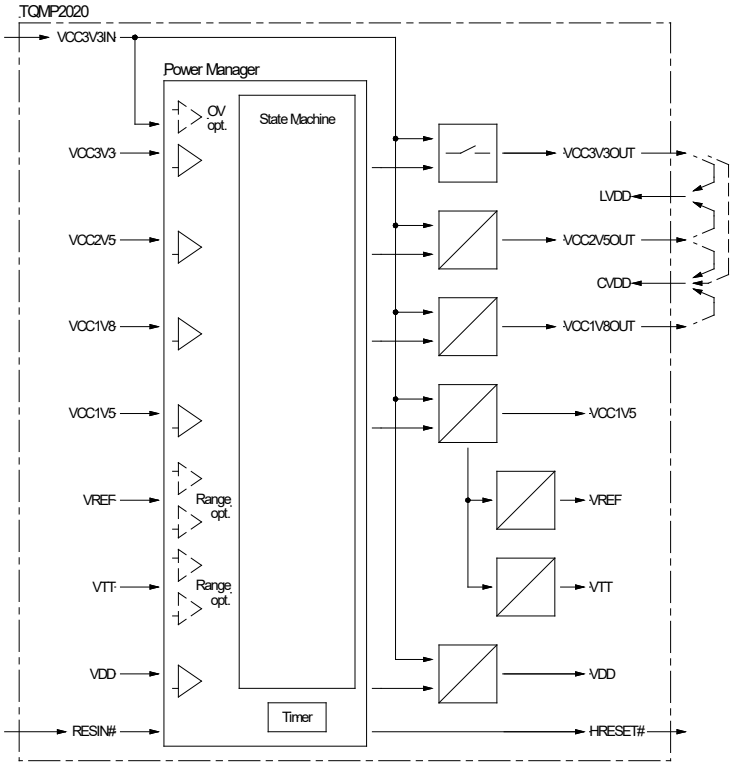


Illustration 6: Supply structure (simplified)

3.3.2 Supply inputs

For the supply voltages to be fed the following limits apply:

3.3.2.1 VCC3V3IN / main supply

Table 15: Requirements for 3.3 V supply voltage

Parameter	Value	Remark
VCC3V3IN	3.201 V to 3.465 V (3.3 V, –3 % / +5 %)	Determined by voltage range of components and supervisor threshold (see 3.3.2)
Ripple max.	30 mV	Peak to peak
Current consumption	5 A	TQMP2020 @ 400 / 1200 / 800 MHz (CCB / Core / DDR3)

3.3.2.2 VBAT / RTC supply

- RTC supply
- Current consumption only, if VBAT >VCC3V3
  (Connection via Schottky diode to VCC3V3 is present on TQMP2020.)

Table 16: Requirements for VBAT

Parameter	Value	Remark
Voltage VBAT	1.8 V to 5.5 V	Determined by voltage range of RTC (see 3.2.8.3)
Max. ripple	1 %	Peak to peak
Timekeeping current	2 µA	VCC3V3IN = 0 V, Oscillator running

3.3.2.3 LVDD / Ethernet-I/O supply

LVDD is generated by feedback of voltages VCC3V3OUT or VCC2V5OUT, which are monitored and generated on the TQMP2020. In this way all specifications are met automatically.
The driver's configuration LVDD_VSEL is done on the TQMP2020, based on the supplied voltage, see 3.2.3.3.

3.3.2.4 BVDD / Local Bus supply

BVDD always operates at 3.3 V. BVDD cannot be altered.
The driver's configuration BVDD_VSEL[0:1] is done on the TQMP2020, see 3.2.3.3.

3.3.2.5 CVDD / supply USB, SDHC and SPI

CVDD is generated by feedback of voltages VCC3V3OUT, VCC2V5OUT or VCC1V8OUT, which are monitored and generated on the TQMP2020. In this way all specifications are met automatically.
The driver's configuration CVDD_VSEL[0:1] is done on the TQMP2020, based on the supplied voltage, see 3.2.3.3.

3.3.3 Supply outputs

VCC2V5OUT and VCC3V3OUT exclusively supply the I/O voltages LVDD or CVDD.
VCC1V8OUT exclusively supplies the I/O voltage CVDD.
An additional load is not permitted.

3.4 Interfaces to other systems and devices

3.4.1 Serial interfaces

- Two internal UARTs: UART1 and UART2
- Max. 115,200 baud (limited by driver / level shifter)
- Transceiver for TxD and RxD with RS232compatible levels
- Additionally all signals are also available unbuffered at the TQMP2020 connectors
- Default assembly: driver for 2 × RxD and 2 × TxD; the control signals RTS and CTS are only available unbuffered

3.4.2 COP/JTAG interface

All NXP COP/JTAG interface signals (debugging interface) are made available externally.
The COP/JTAG interface encloses the following signals. (Signal direction seen from the TQMP2020 or Starterkit):

Table 17: Signals COP/JTAG interface

X230 *	Signal name	Type	Function
1	TDO	O	Test Data Output
2	NC	–	–
3	TDI	I	Test Data Input
4	TRST#	I	Test Reset
5	NC	–	–
6	VDD_SENSE	O	Voltage Sense of Debugger (3.3 V, 10 mA max.)
7	TCK	I	Test Clock
8	CKSTP_IN# **	I	Checkstop In
9	TMS	I	Test Mode Select
10	NC	–	–
11	SRESET#	I	Soft Reset
12	NC	–	(Optional Ground)
13	RESIN#	I	Reset In, connects to HRESET# on TQMP2020
14	(Key pin)	–	–
15	CKSTP_OUT# **		Checkstop Out
16	GND	–	Ground

* On Starterkit STKP2020

** Or'ed on the STKP2020, see (1)

The wiring on the carrier board can be taken from the STKP2020 circuit diagram.

Note: COP/JTAG configuration	
	The COP/JTAG interface uses the same signals as the JTAG interface. A CPLD type LCMXO256C is behind the CPU in the JTAG chain on the TQMP2020. This information must be passed on to the debugger. ***Lauterbach Trace32:*** SYStem.CONFIG IRPRE 8 SYStem.CONFIG DRPRE 1 ***Abatron BDI2000:*** SCANSUCC 1 8 ; 1 device with instruction register length 8 for MachXO device

A corresponding setting should also exist at all other usable debuggers.

3.4.3 External bus / other interfaces

The interfaces described here are routed to the connectors leading to the carrier board:

2 × 160 pins + 1 × 40 pins

3.4.3.1 Treatment of unused pins

The TQMP2020 is designed in such a way, that only a minimum number of signals are required to run the TQMP2020.
Therefore many signals do not need external wiring if their function is not required.

- Pure outputs (type = O):
  no wiring required
- Inputs and I/Os with pull-up / pull-down (type = O, I/O, with pull-ups or pull-downs):
  no wiring required
- I/Os which can be configured as an output (e.g., GPIO_5):
  it is generally sufficient to configure unused pins as an output during initialisation
- Continuing notes are found in (1)

3.4.3.2 TQMP2020 connector pinout X1, X2, X3

The following table shows the pinout of connector X1.

Table 18: TQMP2020 connector X1

Group	Signal [2]	Pin		Signal [2]	Group
Power	VCC3V3	1	2	VCC3V3	Power
	VCC3V3	3	4	VCC3V3	
	VCC3V3	5	6	VCC3V3	
	VCC3V3	7	8	VCC3V3	
	VCC3V3	9	10	VBAT	
	VCC3V3	11	12	TSEC2_RXD0	Ethernet
Ethernet	TSEC1_RXD0	13	14	TSEC2_RXD1	
	TSEC1_RXD1	15	16	TSEC2_RXD2	
	TSEC1_RXD2	17	18	TSEC2_RXD3	
	TSEC1_RXD3	19	20	GND	Power
	TSEC1_RXD4/ TSEC3_RXD0	21	22	TSEC2_RXD4	Ethernet
	TSEC1_RXD5/ TSEC3_RXD1	23	24	TSEC2_RXD5	
	TSEC1_RXD6/ TSEC3_RXD2	25	26	TSEC2_RXD6	
Power	GND	27	28	TSEC2_RXD7	
Ethernet	TSEC1_RXD7/ TSEC3_RXD3	29	30	TSEC2_RX_DV	
	TSEC1_RX_DV	31	32	TSEC2_RX_ER	
	TSEC1_RX_ER	33	34	TSEC2_RX_CLK	
Ethernet	TSEC1_RX_CLK	35	36	GND	Power
	TSEC1_TXD0	37	38	TSEC2_TXD0	Ethernet
	TSEC1_TXD1	39	40	TSEC2_TXD1	
	TSEC1_TXD2	41	42	TSEC2_TXD2	
Power	GND	43	44	TSEC2_TXD3	
Ethernet	TSEC1_TXD3	45	46	TSEC2_TXD4/ TSEC3_GTX_CLK	
	TSEC1_TXD4/ TSEC3_TXD0	47	48	TSEC2_TXD5/ TSEC3_TX_EN	
	TSEC1_TXD5/ TSEC3_TXD1	49	50	TSEC2_TXD6	
	TSEC1_TXD6/ TSEC3_TXD2	51	52	GND	Power
	TSEC1_TXD7/ TSEC3_TXD3	53	54	TSEC2_TXD7	Ethernet
	TSEC1_TX_EN	55	56	TSEC2_TX_EN	
	TSEC1_TX_ER	57	58	TSEC2_TX_ER	
Power	GND	59	60	TSEC2_TX_CLK	
Ethernet	TSEC1_TX_CLK	61	62	TSEC2_GTX_CLK	
	TSEC1_GTX_CLK	63	64	TSEC2_CRS/TSEC3_RX_ER	
	TSEC1_CRS/ TSEC3_RX_DV	65	66	TSEC2_COL/TSEC3_TX_CLK	
	TSEC1_COL TSEC3_RX_CLK	67	68	GND	Power
	TSEC_1588_CLK_IN	69	70	TSEC_1588_CLK_OUT	Ethernet
	TSEC_1588_TRIG_IN1	71	72	TSEC_1588_PULSE_OUT1	
	TSEC_1588_TRIG_IN2	73	74	TSEC_1588_PULSE_OUT2	
Power	GND	75	76	EC_MDC	
Ethernet	TSEC_1588_ALARM_OUT1	77	78	EC_MDIO	
	TSEC_1588_ALARM_OUT2	79	80	EC_GTX_CLK125	

2: Signals in parentheses are not connected with the TQMP2020 and STKP2020 but, however, give the configuration for future TQMP2020 versions.

3.4.3.2 TQMP2020 connector pinout X1, X2, X3 (continued)

Table 18: TQMP2020 connector X1 (continued)

Group	Signal [3]	Pin		Signal [3]	Group
NC	NC (RSVD4080/EMI2_MDC)	81	82	ASLEEP	Control
	NC (RSVD4080/EMI2_MDIO)	83	84	GND	Power
Power	GND	85	86	SD_REF_CLK	SerDes
	GND	87	88	SD_REF_CLK#	
NC	NC (SD_TX3)	89	90	GND	Power
	NC (SD_TX3#)	91	92	GND	
Power	GND	93	94	NC (SD_RX3)	NC
	GND	95	96	NC (SD_RX3#)	
SGMII	SD_TX2	97	98	GND	Power
	SD_TX2#	99	100	GND	
Power	GND	101	102	SD_RX2	SGMII
	GND	103	104	SD_RX2#	
PCIe Slot 2	SD_TX1	105	106	GND	Power
	SD_TX1#	107	108	GND	
Power	GND	109	110	SD_RX1	PCIe Slot 2
	GND	111	112	SD_RX1#	
PCIe Slot 1	SD_TX0	113	114	GND	Power
	SD_TX0#	115	116	GND	
Power	GND	117	118	SD_RX0	PCIe Slot 1
	GND	119	120	SD_RX0#	
NC	NC (RSVD1022/SD2_REF_CLK)	121	122	GND	Power
	NC (RSVD1022/SD2_REF_CLK#)	123	124	GND	
Power	GND	125	126	NC (RSVD1022/SD2_RX1)	NC
	GND	127	128	NC (RSVD1022/SD2_RX1#)	
NC	NC (RSVD1022/SD2_TX1)	129	130	GND	Power
	NC (RSVD1022/SD2_TX1#)	131	132	GND	
Power	GND	133	134	NC (RSVD1022/SD2_RX0)	NC
	GND	135	136	NC (RSVD1022/SD2_RX0#)	
NC	NC (RSVD1022/SD2_TX0)	137	138	GND	Power
	NC (RSVD1022/SD2_TX0#)	139	140	GND	
Power	GND	141	142	NC (RSVD4080/SD_2)	NC
	GND	143	144	NC (RSVD4080/SD_2#)	
NC	NC (RSVD4080/SD_0)	145	146	GND	Power
	NC (RSVD4080/SD_0#)	147	148	GND	
Power	GND	149	150	NC (RSVD4080/SD_3)	NC
	GND	151	152	NC (RSVD4080/SD_3#)	
NC	NC (RSVD4080/SD_1)	153	154	GND	Power
	NC (RSVD4080/SD_1#)	155	156	GND	
Power	GND	157	158	PGOOD	Control
NC	NC (RSVD1022/POWER_OK/GPIO3_19)	159	160	NC (RSVD1022/POWER_EN)	NC

3: Signals in parentheses are not connected with the TQMP2020 and STKP2020 but, however, give the configuration for future TQMP2020 versions.

3.4.3.2 TQMP2020 connector pinout X1, X2, X3 (continued)

The following table shows the pinout of connector X2.

Table 19: TQMP2020 connector X2

Group	Signal [4]	Pin		Signal [4]	Group
Power	3V3 [5]	1	2	GPIO_0/IRQ7	GPIO
	CVDD	3	4	GPIO_1/IRQ8	
	LVDD	5	6	GPIO_2/IRQ9	
	2V5 [5]	7	8	GND	Power
	1V8 [5]	9	10	GPIO_3/IRQ10	GPIO
GPIO	GPIO_5	11	12	GPIO_4/IRQ11	
	GPIO_7	13	14	GPIO_6	
Power	GND	15	16	GPIO_8/SDHC_CD#	
GPIO	GPIO_9/SDHC_WP	17	18	GPIO_10/USB_PCTL0	
	GPIO_11/USB_PCTL1	19	20	GPIO_12	
	GPIO_13	21	22	GPIO_14	
	GPIO_15	23	24	GND	Power
SPI	SPI_MISO	25	26	SPI_CS0#/SDHC_DATA4	SPI
	SPI_MOSI	27	28	SPI_CS1#/SDHC_DATA5	
	SPI_CLK	29	30	SPI_CS2#/SDHC_DATA6	
Power	GND	31	32	SPI_CS3#/SDHC_DATA7	
SDHC	SDHC_DATA0	33	34	NC (RSVD1022/SDHC_CD)	NC
	SDHC_DATA1	35	36	SDHC_CMD	SDHC
	SDHC_DATA2	37	38	SDHC_CLK	
	SDHC_DATA3	39	40	GND	Power
USB	USB_NXT	41	42	NC (RSVD1022/SDHC_WP)	NC
	USB_DIR	43	44	USB_STP	USB
	USB_CLK	45	46	USB_PWRFAULT	
Power	GND	47	48	USB_D0	
USB	USB_D1	49	50	USB_D2	
	USB_D3	51	52	USB_D4	
	USB_D5	53	54	USB_D6	
	USB_D7	55	56	GND	Power
Local bus	LWE0#/LFWE#/LBS#	57	58	LCLK0	Local bus
	LCS7#/DMA2_DDONE1#	59	60	LAD0	
	LGPL4/LGTA#/LFRB/LUPWAIT/LPBSE	61	62	LAD1	
Power	GND	63	64	LAD2	
Local bus	LALE	65	66	LAD3	
	LBCTL	67	68	LAD4	
	LAD6	69	70	LAD5	
	LAD7	71	72	GND	Power
	LA24	73	74	LA25	Local bus
Control	DDRCLK_CPU	75	76	LA26	
Power	GND	77	78	LA27	
Control	SYSCLK_CPU	79	80	LA28	

4: Signals in parentheses are not connected with the TQMP2020 and STKP2020 but, however, give the configuration for future TQMP2020 versions.
5: The three voltages at pins 1, 7 and 9 are outputs on the TQMP2020. They are connected with CVDD and LVDD in such a way that the interfaces USB, SPI, SD card and Ethernet each run with the correct voltage. The circuitry on the STKP2020 should not be altered.

3.4.3.2 TQMP2020 connector pinout X1, X2, X3 (continued)

Table 19: TQMP2020 connector X2 (continued)

Group	Signal [6]	Pin		Signal [6]	Group
Control	CLK_OUT	81	82	LA29	Local bus
Power	GND	83	84	LA30	
Control	RTC	85	86	LA31	
	MSRID0	87	88	MDVAL	Control
	MSRID1	89	90	GND	Power
	MSRID2	91	92	SCAN_MODE#	Control
	MSRID3	93	94	TEST_SEL#	
	MSRID4	95	96	TQM_TDI	JTAG
Power	GND	97	98	TQM_TDO	
Control	TRIG_IN	99	100	TQM_TMS	
	TRIG_OUT/READY_P0/QUIESCE#	101	102	TQM_TCK	
	READY_P1	103	104	TQM_TRST#	
Control	MCP0#	105	106	GND	Power
	MCP1#	107	108	DMA1_DREQ#	Control
	UDE0#	109	110	DMA1_DACK#	
	UDE1#	111	112	DMA1_DDONE#	
Power	GND	113	114	DMA2_DREQ0#	
Control	IRQ0	115	116	DMA2_DACK0#	
	IRQ1	117	118	DMA2_DDONE0#	
	IRQ2	119	120	IRQ_OUT#	
	IRQ3	121	122	GND	Power
	IRQ4	123	124	NC (RSVD1022/IRQ7)	NC
	IRQ5	125	126	NC (RSVD1022/IRQ8)	
	IRQ6	127	128	NC (RSVD1022/IRQ9)	
Power	GND	129	130	NC (RSVD1022/IRQ10)	
I²C	IIC1_SCL	131	132	IIC2_SCL	I²C
	IIC1_SDA	133	134	IIC2_SDA	
JTAG	TQM_CKSTP_IN0#	135	136	TQM_CHKSTP_IN1#	JTAG
Control	HRESET#	137	138	GND	Power
	HRESET_REQ#	139	140	TQM_CHKSTP_OUT1#	JTAG
	SRESET#	141	142	TQM_CHKSTP_OUT0#	
	RESIN#	143	144	CLKOE	Control
Power	GND	145	146	TEMP_OS#	
UART	SIN0	147	148	RTC_INT#	
	SOUT0	149	150	SIN1	UART
	UART_SIN0#	151	152	SOUT1	
	UART_SOUT0#	153	154	GND	Power
	UART_RTS0#	155	156	UART_CTS1#	UART
	UART_CTS0#	157	158	UART_RTS1#	
	UART_SIN1#	159	160	UART_SOUT1#	

6: Signals in parentheses are not connected with the TQMP2020 and STKP2020 but, however, give the configuration for future TQMP2020 versions.

3.4.3.2 TQMP2020 connector pinout X1, X2, X3 (continued)

The following table shows the pinout of connector X3.

Table 20: TQMP2020 connector X3

Group	Signal [7]	Pin		Signal [7]	Group
NC	NC (RSVD1022/IRQ11)	1	2	LWE1#/LBS1#	Local bus
Power	GND	3	4	LCS5#/DMA2_DREQ1#	
Local bus	LGPL0/LFCLE	5	6	LCS6#/DMA2_DACK1#	
	LGPL1/LFALE	7	8	LDP0	
	LGPL2/LFRE#/LOE#	9	10	LDP1	
	LGPL3/LFWP#	11	12	GND	Power
	LGPL5	13	14	LAD8	Local bus
	LCS0#/CS_NOR#	15	16	LAD9	
	LCS1#	17	18	LAD10	
Power	GND	19	20	LAD11	
Local bus	LCS2#	21	22	LAD12	
	LCS3#	23	24	LAD13	
	LCS4#	25	26	LAD14	
	LA23	27	28	GND	Power
	LA22	29	30	LAD15	Local bus
	LA21	31	32	LA16	
	LCLK1	33	34	LA17	
Power	GND	35	36	LA18	
Local bus	LSYNC_IN	37	38	LA19	
	LSYNC_OUT	39	40	LA20	

7: Signals in parentheses are not connected with the TQMP2020 and STKP2020 but, however, give the configuration for future TQMP2020 versions.

3.4.3.3 TQMP2020 pinout according to functional groups

The TQMP2020 pinout is referred to in column "Description".
Notes of treatment on the carrier board are provided, if required.

Table 21: Pinout GPIO / DMA / Timer

GPIO / DMA / Timer				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
GPIO_0/IRQ7	R28	I/O	General Purpose I/O 0 / External Interrupt 7	X2-2
GPIO_1/IRQ8	R26	I/O	General Purpose I/O 1 / External Interrupt 8	X2-4
GPIO_2/IRQ9	P29	I/O	General Purpose I/O 2 / External Interrupt 9	X2-6
GPIO_3/IRQ10	N24	I/O	General Purpose I/O 3 / External Interrupt 10	X2-10
GPIO_4/IRQ11	U29	I/O	General Purpose I/O 4 / External Interrupt 11	X2-12
GPIO_5	R24	I/O	General Purpose I/O 5	X2-11
GPIO_6	R29	I/O	General Purpose I/O 6	X2-14
GPIO_7	R25	I/O	General Purpose I/O 7	X2-13
GPIO_8/SDHC_CD#	F22	I/O	General Purpose I/O 8 / eSDHC card detection	X2-16
GPIO_9/SDHC_WP	A24	I/O	General Purpose I/O 9 / eSDHC card write protect	X2-17
GPIO_10/USB_PCTL0	A25	I/O	General Purpose I/O 10 / USB Port control 0	X2-18
GPIO_11/USB_PCTL1	D24	I/O	General Purpose I/O 11 / USB Port control 1	X2-19
GPIO_12	F23	I/O	General Purpose I/O 12	X2-20
GPIO_13	E23	I/O	General Purpose I/O 13	X2-21
GPIO_14	F24	I/O	General Purpose I/O 14	X2-22
GPIO_15	E24	I/O	General Purpose I/O 15	X2-23

Table 22: Pinout USB

USB				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
USB_NXT	B26	I	USB Next data	X2-41
USB_DIR	A28	I	USB Direction	X2-43
USB_STP	B29	O	USB Stop	X2-44
USB_PWRFAULT	C29	I	USB VBUS power fault	X2-46
USB_CLK	D27	I	USB PHY clock	X2-45
USB_D7	C28	I/O	USB Data 7	X2-55
USB_D6	C25	I/O	USB Data 6	X2-54
USB_D5	B28	I/O	USB Data 5	X2-53
USB_D4	B25	I/O	USB Data 4	X2-52
USB_D3	D26	I/O	USB Data 3	X2-51
USB_D2	A27	I/O	USB Data 2	X2-50
USB_D1	A26	I/O	USB Data 1	X2-49
USB_D0	C26	I/O	USB Data 0	X2-48

Table 23: Pinout Power Management

Power Management				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
ASLEEP	U25	O	Sleep State, ↑ 4k7 to VCC3V3 on TQMP2020	X1-82

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

3.4.3.3 TQMP2020 pinout according to functional groups (continued)

Table 24: Pinout Debug / Test

Debug / Test				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
TCK	V29	I	Test Clock, ↑ 4k7 to VCC3V3 on TQMP2020	X2-102
TDI	T25	I	Test Data In	X2-96
TDO	(V28)	O	CPU Test Data Out via CPLD, see 3.4.2	X2-98
TMS	U26	I	Test Mode Select, ↑ 10k to VCC3V3 on TQMP2020	X2-100
TRST#	V26	I	Test Reset	X2-104
TRIG_IN	AB28	I	Watchpoint Trigger in, ↓ 4k7 to DGND on TQMP2020	X2-99
TRIG_OUT/READY_P0/QUIESCE#	U28	O	Watchpoint Trigger Out / Processor 0 ready / quiescent state	X2-101
READY_P1	W26	O	Processor 1 ready	X2-103
MSRCID0	P28	O	Memory Debug Source ID 0	X2-87
MSRCID1	R27	O	Memory Debug Source ID 1	X2-89
MSRCID2	P27	O	Memory Debug Source ID 2	X2-91
MSRCID3	P26	O	Memory Debug Source ID 3	X2-93
MSRCID4	N26	O	Memory Debug Source ID 4	X2-95
MDVAL	M24	O	Memory Debug data valid	X2-88
SCAN_MODE#	W27	I	Scan Mode, ↑ 1k to VCC3V3 on TQMP2020	X2-92
TEST_SEL#	AA28	I	Test Select P2020, P1020, P1021: ↑ 4k7 to VCC3V3 on TQMP2020 P2010, P1011, P1012: ↓ 1k to DGND on TQMP2020	X2-94

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 25: Pinout Interrupt Controller / DMA

Interrupt Controller / DMA				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
DMA1_DREQ#	Y28	I	DMA1 request, ↑ 4k7 to VCC3V3 on TQMP2020	X2-108
DMA2_DREQ0#	W28	I	DMA2 request 0, ↑ 4k7 to VCC3V3 on TQMP2020	X2-114
DMA1_DACK#	T28	O	DMA1 acknowledge	X2-110
DMA2_DACK0#	T29	O	DMA2 acknowledge 0	X2-116
DMA1_DDONE#	T26	O	DMA1 done	X2-112
DMA2_DDONE0#	Y29	O	DMA2 done 0	X2-118
UDE0#	J27	I	Unconditional debug event 0, ↑ 4k7 to VCC3V3 on TQMP2020	X2-109
UDE1#	K28	I	Unconditional debug event 1, ↑ 4k7 to VCC3V3 on TQMP2020	X2-111
MCP0#	AA27	I	Machine check processor 0, ↑ 4k7 to VCC3V3 on TQMP2020	X2-105
MCP1#	M25	I	Machine check processor 1, ↑ 4k7 to VCC3V3 on TQMP2020	X2-107
IRQ0#	L24	I	External interrupt 0, ↑ 4k7 to VCC3V3 on TQMP2020	X2-115
IRQ1#	K26	I	External interrupt 1, ↑ 4k7 to VCC3V3 on TQMP2020	X2-117
IRQ2#	K29	I	External interrupt 2, ↑ 4k7 to VCC3V3 on TQMP2020	X2-119
IRQ3#	N25	I	External interrupt 3, ↑ 4k7 to VCC3V3 on TQMP2020	X2-121
IRQ4#	L26	I	External interrupt 4, ↑ 4k7 to VCC3V3 on TQMP2020	X2-123
IRQ5#	L29	I	External interrupt 5, ↑ 4k7 to VCC3V3 on TQMP2020	X2-125
IRQ6#	K27	I	External interrupt 6, ↑ 4k7 to VCC3V3 on TQMP2020	X2-127
IRQ_OUT#	N29	O	Interrupt output, ↑ 4k7 to VCC3V3 on TQMP2020	X2-120

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 26: Pinout Clocks

Clocks				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
CLK_OUT	T24	O	Clock Out, → 22 Ω on TQMP2020	X2-81
RTC	K24	I	Real-Time clock	X2-85
DDRCLK	AC9	O	DDR clock, driven on TQMP2020, do not connect, for test use only	X2-75
SYSCLK	W29	O	System clock, driven on TQMP2020, do not connect, for test use only	X2-79

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

3.4.3.3 TQMP2020 pinout according to functional groups (continued)

Table 27: Pinout I2C

I²C				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
IIC1_SDA	H28	I/O	I2C1 Serial data, ↑ 2k4 to VCC3V3 on TQMP2020	X2-133
IIC1_SCL	G27	I/O	I2C1 Serial clock, ↑ 2k4 to VCC3V3 on TQMP2020	X2-131
IIC2_SDA	H26	I/O	I2C2 Serial data, ↑ 4k7 to VCC3V3 on TQMP2020	X2-134
IIC2_SCL	H25	I/O	I2C2 Serial clock, ↑ 4k7 to VCC3V3 on TQMP2020	X2-132

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 28: Pinout Reset

Reset				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
HRESET#	W25	I	Hard reset, driven on TQMP2020 (P2020: input; TQMP2020: output; see Illustration 6)	X2-137
HRESET_REQ#	U24	O	Hard reset request, ↑ 2k2 to VCC3V3 on TQMP2020, connected to RESIN# via 10k on TQMP2020	X2-139
SRESET#	W24	I	Soft reset, ↑ 4k7 to VCC3V3 on TQMP2020	X2-141
CKSTP_IN0#	AA29	I	Checkstop in 0, ↑ 4k7 to VCC3V3 on TQMP2020	X2-135
CKSTP_IN1#	AB29	I	Checkstop in 1, ↑ 4k7 to VCC3V3 on TQMP2020	X2-136
CKSTP_OUT0#	V25	O	Checkstop Out 0, ↑ 4k7 to VCC3V3 on TQMP2020	X2-142
CKSTP_OUT1#	Y27	O	Checkstop Out 1, ↑ 4k7 to VCC3V3 on TQMP2020	X2-140

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 29: Pinout Non-CPU Signals

Non-CPU Signals				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
RTC_INT#	–	O	Real-Time clock interrupt outputs INTA# and SQW/INTB# (DS1337) connected together, ↑ 10k via Schottky diode to VCC3V3 on TQMP2020	X2-148
TEMP_OS#	–	O	Temperature sensor alarm outputs EVENT# (SE97B), ALERT# and T_CRIT# (SA56004E) connected together, ↑ 10k to VCC3V3	X2-146
RESIN#	–	I	Reset Input (Reset input of voltage supervisor), ↑ and connection to HRESET_REQ# on TQMP2020	X2-143
CLKOE	–	I	Internal 66.666 MHz driver enable, ↑ 4k7 to VCC3V3 on TQMP2020	X2-144
PGOOD	–	O	Power good output, ↓ 22k to DGND on TQMP2020, use for carrier board power sequencing	X1-158

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 30: Pinout SPI

SPI				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
SPI_MISO	F28	I	SPI Master-in slave-out, ↑, 2 to 10k to CVDD on carrier board if not used	X2-25
SPI_MOSI	F25	I/O	SPI Master-out slave-in, ↑, 2 to 10k to CVDD on carrier board if not used	X2-27
SPI_CS0#/ SDHC_DATA4	D28	I/O	SPI slave select 0 / SDHC data line 4, ↑, 2 to 10k to CVDD on carrier board if not used	X2-26
SPI_CS1#/ SDHC_DATA5	E26	I/O	SPI slave select 1 / SDHC data line 5	X2-28
SPI_CS2#/ SDHC_DATA6	F29	I/O	SPI slave select 2 / SDHC data line 6	X2-30
SPI_CS3#/ SDHC_DATA7	E29	I/O	SPI slave select 3 / SDHC data line 7	X2-32
SPI_CLK	D29	O	SPI clock, ↓, 1k to DGND on carrier board if not used	X2-29

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

3.4.3.3 TQMP2020 pinout according to functional groups (continued)

Table 31: Pinout ESDHC

ESDHC				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
SDHC_DATA0	G28	I/O	SDHC data line 0	X2-33
SDHC_DATA1	F27	I/O	SDHC data line 1	X2-35
SDHC_DATA2	G25	I/O	SDHC data line 2	X2-37
SDHC_DATA3	G26	I/O	SDHC data line 3	X2-39
SDHC_CMD	F26	I/O	SDHC CMD line	X2-36
SDHC_CLK	G29	O	SDHC clock	X2-38

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 32: Pinout RS232

RS232 (via transceiver)				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
RS232_SIN0	–	I	UART0 serial in data, RS232 level	X2-147
RS232_SOUT0	–	O	UART0 serial out data, RS232 level	X2-149
RS232_SIN1	–	I	UART1 serial in data, RS232 level	X2-150
RS232_SOUT1	–	O	UART1 serial out data, RS232 level	X2-152

Table 33: Pinout UARTs

UARTs				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
UART_SIN0	H29	I	UART0 serial in data, LVTTL level, ↑ 10k to VCC3V3 on TQMP2020 if RS232 transceiver is not assembled Do not connect if RS232 transceiver on TQMP2020 is used	X2-151
UART_SOUT0	J26	O	UART0 serial out data, LVTTL level	X2-153
UART_CTS0#	J28	I	UART0 clear to send, LVTTL level, ↑ 10k to VCC3V3 on TQMP2020	X2-157
UART_RTS0#	J29	O	UART0 request to send, LVTTL level	X2-155
UART_SIN1	G24	I	UART1 serial in data, LVTTL level, ↑ 10k to VCC3V3 on TQMP2020 if RS232 transceiver is not assembled Do not connect if RS232 transceiver on TQMP2020 is used	X2-159
UART_SOUT1	J25	O	UART1 serial out data, LVTTL level	X2-160
UART_CTS1#	H24	I	UART1 clear to send, LVTTL level, ↑ 10k to VCC3V3 on TQMP2020	X2-156
UART_RTS1#	J24	O	UART1 request to send, LVTTL level	X2-158

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

3.4.3.3 TQMP2020 pinout according to functional groups (continued)

Table 34: Pinout Local Bus

Local Bus				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
LAD0	B18	I/O	Local Bus address / data 0	X2-60
LAD1	E20	I/O	Local Bus address / data 1	X2-62
LAD2	A19	I/O	Local Bus address / data 2	X2-64
LAD3	B20	I/O	Local Bus address / data 3	X2-66
LAD4	D19	I/O	Local Bus address / data 4	X2-68
LAD5	A18	I/O	Local Bus address / data 5	X2-70
LAD6	B17	I/O	Local Bus address / data 6	X2-69
LAD7	C20	I/O	Local Bus address / data 7	X2-71
LAD8	F19	I/O	Local Bus address / data 8	X3-14
LAD9	E10	I/O	Local Bus address / data 9	X3-16
LAD10	B16	I/O	Local Bus address / data 10	X3-18
LAD11	D14	I/O	Local Bus address / data 11	X3-20
LAD12	D17	I/O	Local Bus address / data 12	X3-22
LAD13	E11	I/O	Local Bus address / data 13	X3-24
LAD14	A16	I/O	Local Bus address / data 14	X3-26
LAD15	C15	I/O	Local Bus address / data 15	X3-30
LDP0	E18	I/O	Local Bus data parity 0, ↑ 4k7 to VCC3V3 on TQMP2020	X3-8
LDP1	B19	I/O	Local Bus data parity 1, ↑ 4k7 to VCC3V3 on TQMP2020	X3-10
LA16	B21	O	Local Bus burst address 16	X3-32
LA17	A22	O	Local Bus burst address 17	X3-34
LA18	C21	O	Local Bus burst address 18	X3-36
LA19	F21	O	Local Bus burst address 19	X3-38
LA20	E12	O	Local Bus burst address 20	X3-40
LA21	A21	O	Local Bus burst address 21	X3-31
LA22	D11	O	Local Bus burst address 22	X3-29
LA23	E22	O	Local Bus burst address 23	X3-27
LA24	F20	O	Local Bus burst address 24	X2-73
LA25	E21	O	Local Bus burst address 25	X2-74
LA26	B22	O	Local Bus burst address 26	X2-76
LA27	F18	O	Local Bus burst address 27	X2-78
LA28	A23	O	Local Bus burst address 28	X2-80
LA29	B23	O	Local Bus burst address 29	X2-82
LA30	C23	O	Local Bus burst address 30	X2-84
LA31	D23	O	Local Bus burst address 31	X2-86
LCS0#/CS_NOR#	D20	O	Local Bus chip select 0, Used internally for NOR flash, ↑ 4k7 to VCC3V3 on TQMP2020	X3-15
LCS1#	A12	O	Local Bus chip select 1, ↑ 4k7 to VCC3V3 on TQMP2020	X3-17
LCS2#	E19	O	Local Bus chip select 2, ↑ 4k7 to VCC3V3 on TQMP2020	X3-21
LCS3#	D21	O	Local Bus chip select 3, ↑ 4k7 to VCC3V3 on TQMP2020	X3-23
LCS4#	F11	O	Local Bus chip select 4, ↑ 4k7 to VCC3V3 on TQMP2020	X3-25
LCS5#/DMA2_DREQ1#	D15	I/O	Local Bus chip select 5 / DMA2 request 1, ↑ 4k7 to VCC3V3 on TQMP2020	X3-4
LCS6#/DMA2_DACK1#	D13	O	Local Bus chip select 6 / DMA2 acknowledge 1, ↑ 4k7 to VCC3V3 on TQMP2020	X3-6
LCS7#/DMA2_DDONE1#	A17	O	Local Bus chip select 7 / DMA2 done 1, ↑ 4k7 to VCC3V3 on TQMP2020	X2-59
LWE0#/LFWE#/LBS0#	F12	O	Local Bus write enable 0 / NAND flash write enable / byte (lane) select 0	X2-57
LWE1#/LBS1#	D12	O	Local Bus write enable 1 / byte (lane) select 1	X3-2
LBCTL	E17	O	Local Bus data buffer control	X2-67
LALE	C17	O	Local Bus address latch enable Signal integrity and timing is critical. Do not connect if not used on carrier board. If used, keep as short as possible and observe length constraints with respect to LAD[0:15]	X2-65
LGPL0/LFCLE	B12	O	Local Bus UPM general purpose line 0 / NAND flash command latch enable	X3-5
LGPL1/LFALE	C13	O	Local Bus GP line 1 / NAND flash address latch enable	X3-7
LGPL2/LFRE#/LOE#	A20	O	Local Bus GP line 2 / NAND flash read enable / output enable	X3-9
LGPL3/LFWP#	D10	O	Local Bus GP line 3 / NAND flash write protect	X3-11
LGPL4/LGTA#/LFRB/ LUPWAIT/LPBSE	B13	I/O	Local Bus GP line 4 / transaction termination / NAND flash ready-busy / wait / parity byte select, ↑ 4k7 to VCC3V3 on TQMP2020	X2-61
LGPL5	C19	O	Local Bus GP line 5	X3-13
LCLK0	B15	O	Local Bus clock 0, → 22 Ω on TQMP2020	X2-58
LCLK1	A15	O	Local Bus clock 1, → 22 Ω on TQMP2020	X3-33
LSYNC_IN	A13	I	Local Bus PLL synchronization in, → 22 Ω and ↑ 4k7 to VCC3V3 on TQMP2020	X3-37
LSYNC_OUT	A14	O	Local Bus PLL synchronization out, → 22 Ω on TQMP2020	X3-39

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

3.4.3.3 TQMP2020 pinout according to functional groups (continued)

Table 35: Pinout eTSEC1 / eTSEC2

(e)TSECs / IEEE1588				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
TSEC_1588_CLK_IN	AG21	I	IEEE1588 clock in, ↑ 10k to LVDD on TQMP2020	X1-69
TSEC_1588_TRIG_IN1	AH20	I	IEEE1588 trigger in 1, ↑ 10k to LVDD on TQMP2020	X1-71
TSEC_1588_TRIG_IN2	AG20	I	IEEE1588 trigger in 2, ↑ 10k to LVDD on TQMP2020	X1-73
TSEC_1588_ALARM_OUT1	AE20	O	IEEE1588 alarm out 1	X1-77
TSEC_1588_ALARM_OUT2	AJ20	O	IEEE1588 alarm out 2	X1-79
TSEC_1588_CLK_OUT	AG22	O	IEEE1588 clock out	X1-70
TSEC_1588_PULSE_OUT1	AH21	O	IEEE1588 pulse out 1	X1-72
TSEC_1588_PULSE_OUT2	AJ22	O	IEEE1588 pulse out 2	X1-74
EC_MDC	AD20	O	Ethernet management data clock	X1-76
EC_MDIO	AJ21	I/O	Ethernet management data in / out, ↑ 10k to LVDD on TQMP2020	X1-78
EC_GTX_CLK125	AF24	I	eTSEC Gigabit reference clock, ↓ 10k to DGND on TQMP2020	X1-80
TSEC1_TXD7/TSEC3_TXD3	AF22	O	eTSEC1 transmit data 7 / eTSEC3 transmit data 3	X1-53
TSEC1_TXD6/TSEC3_TXD2	AD22	O	eTSEC1 transmit data 6 / eTSEC3 transmit data 2	X1-51
TSEC1_TXD5/TSEC3_TXD1	AD23	O	eTSEC1 transmit data 5 / eTSEC3 transmit data 1	X1-49
TSEC1_TXD4/TSEC3_TXD0	AE21	O	eTSEC1 transmit data 4 / eTSEC3 transmit data 0	X1-47
TSEC1_TXD3	AJ25	O	eTSEC1 transmit data 3	X1-45
TSEC1_TXD2	AH28	O	eTSEC1 transmit data 2	X1-41
TSEC1_TXD1	AE25	O	eTSEC1 transmit data 1	X1-39
TSEC1_TXD0	AD24	O	eTSEC1 transmit data 0	X1-37
TSEC1_TX_EN	AH24	O	eTSEC1 transmit enable, ↓ 10k to DGND on TQMP2020	X1-55
TSEC1_TX_ER	AF23	O	eTSEC1 transmit error	X1-57
TSEC1_TX_CLK	AJ24	I	eTSEC1 transmit clock in, ↑ 10k to LVDD on TQMP2020	X1-61
TSEC1_GTX_CLK	AG25	O	eTSEC1 transmit clock out	X1-63
TSEC1_CRS/TSEC3_RX_DV	AJ27	I/O	eTSEC1 carrier sense / eTSEC3 receive data valid, ↑ 10k to LVDD on TQMP2020	X1-65
TSEC1_COL/TSEC3_RX_CLK	AH26	I	eTSEC1 collision detect / eTSEC3 receive clock, ↑ 10k to LVDD on TQMP2020	X1-67
TSEC1_RXD7/TSEC3_RXD3	AG23	I	eTSEC1 receive data 7 / eTSEC3 receive data 3, ↑ 10k to LVDD on TQMP2020	X1-29
TSEC1_RXD6/TSEC3_RXD2	AH22	I	eTSEC1 receive data 6 / eTSEC3 receive data 2, ↑ 10k to LVDD on TQMP2020	X1-25
TSEC1_RXD5/TSEC3_RXD1	AJ23	I	eTSEC1 receive data 5 / eTSEC3 receive data 1, ↑ 10k to LVDD on TQMP2020	X1-23
TSEC1_RXD4/TSEC3_RXD0	AE24	I	eTSEC1 receive data 4 / eTSEC3 receive data 0, ↑ 10k to LVDD on TQMP2020	X1-21
TSEC1_RXD3	AJ28	I	eTSEC1 receive data 3, ↑ 10k to LVDD on TQMP2020	X1-19
TSEC1_RXD2	AE22	I	eTSEC1 receive data 2, ↑ 10k to LVDD on TQMP2020	X1-17
TSEC1_RXD1	AD21	I	eTSEC1 receive data 1, ↑ 10k to LVDD on TQMP2020	X1-15
TSEC1_RXD0	AH25	I	eTSEC1 receive data 0, ↑ 10k to LVDD on TQMP2020	X1-13
TSEC1_RX_DV	AJ26	I	eTSEC1 receive data valid, ↑ 10k to LVDD on TQMP2020	X1-31
TSEC1_RX_ER	AH23	I	eTSEC1 receive error, ↑ 10k to LVDD on TQMP2020	X1-33
TSEC1_RX_CLK	AG26	I	eTSEC1 receive clock, ↑ 10k to LVDD on TQMP2020	X1-35
TSEC2_TXD7	AE26	O	eTSEC2 transmit data 7	X1-54
TSEC2_TXD6	AF26	O	eTSEC2 transmit data 6	X1-50
TSEC2_TXD5/TSEC3_TX_EN	AB24	O	eTSEC2 transmit data 5 / eTSEC3 transmit enable, ↓ 10k to DGND on TQMP2020	X1-48
TSEC2_TXD4/ TSEC3_GTX_CLK	AB25	O	eTSEC2 transmit data 4 / eTSEC3 transmit clock out	X1-46
TSEC2_TXD3	AG29	O	eTSEC2 transmit data 3	X1-44
TSEC2_TXD2	AA25	O	eTSEC2 transmit data 2	X1-42
TSEC2_TXD1	AF27	O	eTSEC2 transmit data 1	X1-40
TSEC2_TXD0	Y24	O	eTSEC2 transmit data 0	X1-38
TSEC2_TX_EN	AA26	O	eTSEC2 transmit enable, ↓ 10k to DGND on TQMP2020	X1-56
TSEC2_TX_ER	AE29	O	eTSEC2 transmit error	X1-58
TSEC2_TX_CLK	AA24	I	eTSEC2 transmit clock in, ↑ 10k to LVDD on TQMP2020	X1-60
TSEC2_GTX_CLK	AG28	O	eTSEC2 transmit clock out	X1-62
TSEC2_CRS/TSEC3_RX_ER	AD25	I/O	eTSEC2 carrier sense / eTSEC3 receive error, ↑ 10k to LVDD on TQMP2020	X1-64
TSEC2_COL/TSEC3_TX_CLK	AE27	I	eTSEC2 collision detect / eTSEC3 transmit clock in, ↑ 10k to LVDD on TQMP2020	X1-66
TSEC2_RXD7	AD27	I	eTSEC2 receive data 7, ↑ 10k to LVDD on TQMP2020	X1-28
TSEC2_RXD6	AB26	I	eTSEC2 receive data 6, ↑ 10k to LVDD on TQMP2020	X1-26
TSEC2_RXD5	AC26	I	eTSEC2 receive data 5, ↑ 10k to LVDD on TQMP2020	X1-24
TSEC2_RXD4	AD26	I	eTSEC2 receive data 4, ↑ 10k to LVDD on TQMP2020	X1-22
TSEC2_RXD3	AB27	I	eTSEC2 receive data 3, ↑ 10k to LVDD on TQMP2020	X1-18
TSEC2_RXD2	AD28	I	eTSEC2 receive data 2, ↑ 10k to LVDD on TQMP2020	X1-16
TSEC2_RXD1	AF29	I	eTSEC2 receive data 1, ↑ 10k to LVDD on TQMP2020	X1-14
TSEC2_RXD0	AF28	I	eTSEC2 receive data 0, ↑ 10k to LVDD on TQMP2020	X1-12
TSEC2_RX_DV	AD29	I	eTSEC2 receive data valid, ↑ 10k to LVDD on TQMP2020	X1-30
TSEC2_RX_ER	AE28	I	eTSEC2 receive error, ↑ 10k to LVDD on TQMP2020	X1-32
TSEC2_RX_CLK	AC29	I	eTSEC2 receive clock, ↑ 10k to LVDD on TQMP2020	X1-34

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

3.4.3.3 TQMP2020 pinout according to functional groups (continued)

Table 36: Pinout SERDES

SERDES				
Signal	CPU Pin	Type	Description	TQMP2020 Pin
SD_TX3	AD18	O	SERDES transmit data 3	X1-89
SD_TX3#	AE18	O	SERDES transmit data 3 complement	X1-91
SD_TX2	AE17	O	SERDES transmit data 2	X1-97
SD_TX2#	AF17	O	SERDES transmit data 2 complement	X1-99
SD_TX1	AE13	O	SERDES transmit data 1	X1-105
SD_TX1#	AF13	O	SERDES transmit data 1 complement	X1-107
SD_TX0	AD12	O	SERDES transmit data 0	X1-113
SD_TX0#	AE12	O	SERDES transmit data 0 complement	X1-115
SD_RX3	AH18	I	SERDES receive data 3	X1-94
SD_RX3#	AJ18	I	SERDES receive data 3 complement	X1-96
SD_RX2	AH16	I	SERDES receive data 2	X1-102
SD_RX2#	AJ16	I	SERDES receive data 2 complement	X1-104
SD_RX1	AH14	I	SERDES receive data 1	X1-110
SD_RX1#	AJ14	I	SERDES receive data 1 complement	X1-112
SD_RX0	AH12	I	SERDES receive data 0	X1-118
SD_RX0#	AJ12	I	SERDES receive data 0 complement	X1-120
SD_REF_CLK	AG15	I	SERDES PLL reference clock	X1-86
SD_REF_CLK#	AF15	I	SERDES PLL reference clock complement	X1-88

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

Table 37: Pinout TQMP2020 supply

TQMP2020 supply				
Signal	Pin Count	Type	Description	TQMP2020 Pin
VCC3V3IN	2	Supply	3.3 V supply input	See below
	X1-6, X1-8			
VCC3V3IN	8	Supply	3.3 V supply input	See below
	X1-1, X1-2, X1-3, X1-4, X1-5, X1-7, X1-9, X1-11			
VBAT	1	Supply	Battery Voltage, connected directly to RTC supply pin and or'ed with VCC3V3 via Schottky diode.	X1-10
LVDD	1	Supply	eTSEC, IEEE1588 and Ethernet Management I/O supply voltage Connect to either VCC3V3OUT or VCC2V5OUT, depending on Physical Interface Mode; LVDD_VSEL will be set automatically depending on LVDD voltage.	X2-5
CVDD	1	Supply	USB, eSDHC and eSPI I/O supply voltage Connect to VCC3V3OUT, VCC2V5OUT or VCC1V8OUT, depending on desired I/O voltage; CVDD_VSEL[0:1] will be set automatically depending on CVDD voltage.	X2-3
VCC3V3OUT	1	Supply	3.3 V supply output after power sequencing switch Use for LVDD and/or CVDD supply only!	X2-1
VCC2V5OUT	1	Supply	2.5 V supply output Use for LVDD and/or CVDD supply only!	X2-7
VCC1V8OUT	1	Supply	1.8 V supply output Use for CVDD supply only!	X2-9
DGND	71	Supply	(Digital) Ground Connect all pins to Ground for best signal integrity of high-speed lanes.	See below
	X1-20, X1-27, X1-36, X1-43, X1-52, X1-59, X1-68, X1-75, X1-84, X1-85, X1-87, X1-90, X1-92, X1-93, X1-95, X1-98, X1-100, X1-101, X1-103, X1-106, X1-108, X1-109, X1-111, X1-114, X1-116, X1-117, X1-119, X1-122, X1-124, X1-125, X1-127, X1-130, X1-132, X1-133, X1-135, X1-138, X1-140, X1-141, X1-143, X1-146, X1-148, X1-149, X1-151, X1-154, X1-156, X1-157			
	X2-8, X2-15, X2-24, X2-31, X2-40, X2-47, X2-56, X2-63, X2-72, X2-77, X2-83, X2-90, X2-97, X2-106, X2-113, X2-122, X2-129, X2-138, X2-145, X2-154			
	X3-3, X3-12, X3-19, X3-28, X3-35			

3.4.3.3 TQMP2020 pinout according to functional groups (continued)

Table 38: Reserved Pins

Reserved			
Signal	Type	Description	TQMP2020 Pin
RSVD4080 / SD_3	I	Reserved input 3, connect to ground	X1-150
RSVD4080 / SD_3#	I	Reserved input 3 complement, connect to ground	X1-152
RSVD4080 / SD_2	I	Reserved input 2, connect to ground	X1-142
RSVD4080 / SD_2#	I	Reserved input 2 complement, connect to ground	X1-144
RSVD4080 / SD_1	O	Reserved output 1, do not connect	X1-153
RSVD4080 / SD_1#	O	Reserved output 1 complement, do not connect	X1-155
RSVD4080 / SD_0	O	Reserved output 0, do not connect	X1-145
RSVD4080 / SD_0#	O	Reserved output 0 complement, do not connect	X1-147
RSVD1022 / SD2_TX1	O	Reserved SERDES2 transmit data 1, do not connect	X1-129
RSVD1022 / SD2_TX1#	O	Reserved SERDES2 transmit data 1 complement, do not connect	X1-131
RSVD1022 / SD2_TX0	O	Reserved SERDES2 transmit data 0, do not connect	X1-137
RSVD1022 / SD2_TX0#	O	Reserved SERDES2 transmit data 0 complement, do not connect	X1-139
RSVD1022 / SD2_RX1	I	Reserved SERDES2 receive data 1, connect to ground	X1-126
RSVD1022 / SD2_RX1#	I	Reserved SERDES2 receive data 1 complement, connect to ground	X1-128
RSVD1022 / SD2_RX0	I	Reserved SERDES2 receive data 0, connect to ground	X1-134
RSVD1022 / SD2_RX0#	I	Reserved SERDES2 receive data 0 complement, connect to ground	X1-136
RSVD1022 / SD2_REF_CLK	I	Reserved SERDES PLL reference clock, connect to ground	X1-121
RSVD1022 / SD2_REF_CLK#	I	Reserved SERDES PLL reference clock complement, connect to ground	X1-123
RSVD4080 / EMI2_MDC	O	Reserved Ethernet management clock 2, do not connect	X1-81
RSVD4080 / EMI2_MDIO	I/O	Reserved Ethernet management data in / out 2, do not connect	X1-83
RSVD1022 / POWER_OK / GPIO3_19	I/O	Reserved power ok, do not connect	X1-159
RSVD1022 / POWER_EN	O	Reserved power enable, do not connect	X1-160
RSVD1022 / SDHC_CD / GPIO1_28	I/O	Reserved eSDHC card detection, do not connect	X2-34
RSVD1022 / SDHC_WP / GPIO1_29	I/O	Reserved eSDHC card write protect, do not connect	X2-42
RSVD1022 / IRQ7	I	Reserved external interrupt 7, do not connect	X2-124
RSVD1022 / IRQ8	I	Reserved external interrupt 8, do not connect	X2-126
RSVD1022 / IRQ9	I	Reserved external interrupt 9, do not connect	X2-128
RSVD1022 / IRQ10	I	Reserved external interrupt 10, do not connect	X2-130
RSVD1022 / IRQ11	I	Reserved external interrupt 11, do not connect	X3-1

- low active signal, ↑ - (pull up), ↓ - (pull down), → - (element in series)

4. SOFTWARE

The TQMP2020 is delivered with a preinstalled boot loader U-Boot and a TQ-BSP, which is tailored for the STKP2020.
The boot loader U-Boot provides module-specific as well as board-specific settings, e.g.:

- Clocks
- CPU configuration
- Driver strengths
- Multiplexing
- Pin configuration
- PMIC configuration
- RAM configuration and timing

More information can be found in the TQMP1020 Support Wiki and the TQMP2020 Support Wiki.

5. MECHANICS

5.1 TQMP2020 connectors

The TQMP2020 is connected to the carrier board with three connectors (360 pins).
The following table shows details of the connector assembled on the TQMP2020.

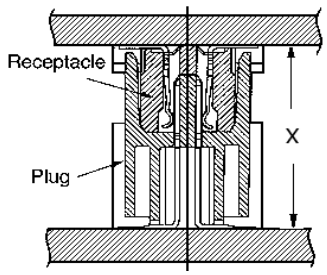
Table 39: TQMP2020 connectors

Manufacturer	Part number	Description	Package
TE connectivity	5177985-1	1 × 40-pin connector (receptacle)	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C
	5177985-8	2 × 160-pin connector (receptacle)	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMP2020 is held in the connectors with a considerable retention force.
To avoid damaging the TQMP2020 connectors as well as the carrier board connectors while removing the TQMP2020, it is strongly recommended to use an extraction tool. See chapter 5.8 for further information.

The following table shows suitable mating connectors for the carrier board.

Table 40: Carrier board mating connectors

Manufacturer	Part number	Remark	Stack height (X)	
TE connectivity	40-pin: 5177986-1 160-pin: 5177986-8	On STKP2020	5 mm	
	40-pin: 1-5177986-1 160-pin: 2-5179230-8	–	6 mm	
	40-pin: 2-5177986-1 160-pin: 5179030-8	–	7 mm	
	40-pin: 3-5177986-1 160-pin: 3-5177986-8	–	8 mm	

Note: RF suitability of TQMP2020-connectors	
	The RF suitability of the TQMP2020-connectors was verified with the stack height 5 mm. The results indicate however, that there are sufficient reserves to use higher connectors for the given data rates of up to 3.125 Gbit/s (6 mm, possibly even 7 mm).

5.2 TQMP2020 dimensions

Table 41: TQMP2020 stack heights, overview

Expansion stage DDR SDRAM	Stack height without heat sink, max. a + b + c	Free stack height under TQMP2020, min. a – d
All	10.3 mm	3.0 mm

Table 42: TQMP2020 stack heights

Dim.	Value [mm]	Remark
a	5.0 ±0.2	Combination of TQMP2020-connector with mating connector; 6, 7 and 8 mm are also possible with different connectors on carrier board
b	2.0 ±0.1	PC-board
c	3.0 +0	Coil L2 (highest stack height top side)
d	1.6 ±0.2	Ferrite L8 (highest stack height bottom side)
e2 / e3	–	(not applicable)
f	2.46 +0 / –0.46	CPU (top side, not shown in Illustration 7)

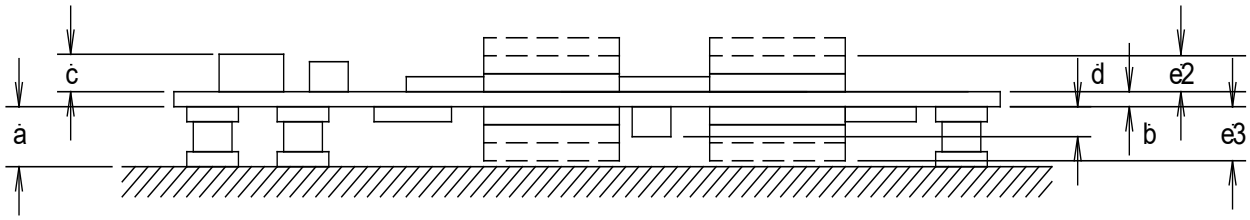


Illustration 7: TQMP2020 side view

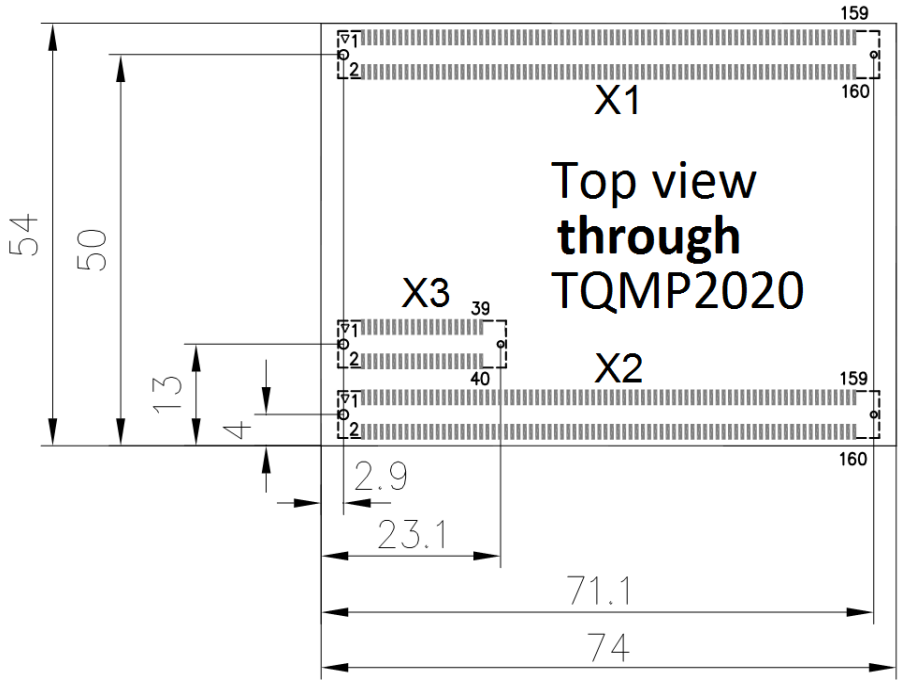


Illustration 8: TQMP2020 dimensions, top view **through** TQMP2020

5.3 TQMP2020 component placement

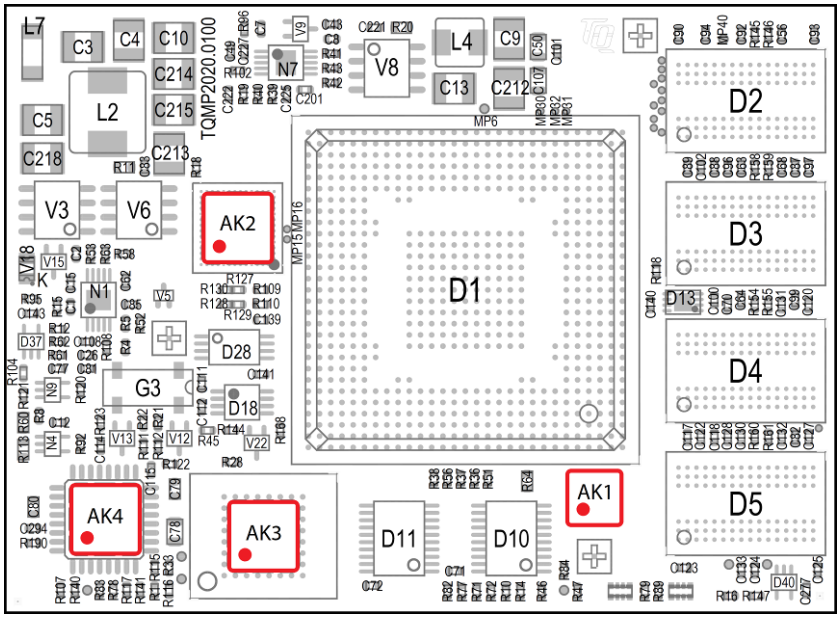


Illustration 9: TQMP2020, component placement top

The labels on the TQMP2020 show the following information:

Table 43: Labels on TQMP2020

Label	Text
AK1	Serial number
AK2	First MAC address (+ additional reserved MAC addresses)
AK3	TQMP2020 version and revision
AK4	Tests performed

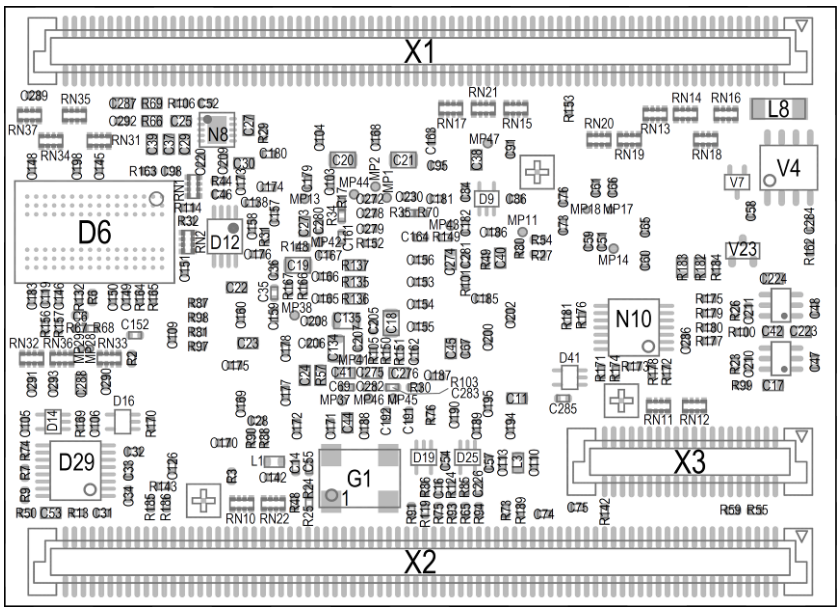


Illustration 10: TQMP2020, component placement bottom

5.4 Adaptation to the environment

The TQMP2020 has overall dimensions (length × width × height) of 74 × 54 × 8.0 mm³.
The TQMP2020 has a maximum height of approximately 10 mm above the carrier board.

5.5 Protection against external effects

As an embedded module the TQMP2020 is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.6 Thermal management

The thermal design power TDP at 400 / 1200 / 800 MHz CCB / Core / DDR clock is approximately 12 W.
The cooling has to be designed according to this value.
Because of the systems thermal inertia, the power loss will however be lower in average.

Attention: Destruction or malfunction, TQMP2020 heat dissipation	
	The TQMP2020 belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8 must be taken into consideration when connecting the heat sink. The P2020 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMP2020 and thus malfunction, deterioration or destruction.

5.7 Structural requirements

The TQMP2020 is held in its mating connectors by the pins (a total of 360) with a retention force of approximately 36 N.
For high requirements with respect to vibration and shock firmness an additional holder has to be provided in the final product to hold the TQMP2020 in its position. For this purpose TQ-Systems GmbH can provide a suitable solution. As no heavy and big components are used, no further requirements are given.

5.8 Notes of treatment

In order to avoid damage to the TQMP2020 itself or the connectors on the carrier board caused by mechanical stress during removal of the TQMP2020, the use of the extraction tool MOZIP2020 is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMP2020 for the extraction tool MOZIP2020.

6. OPERATIONAL CONDITIONS

6.1 Climatic conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection), hence, no fixed value can be given for the whole assembly.
In general, a reliable operation is given when following conditions are met:

Table 44: Conditions for standard temperature range 0 to +70 °C

Parameter	Range	Remark
T_j temperature CPU	0 °C to +125 °C	–
Case temperature DDR3 SDRAM	0 °C to +95 °C	–
Case temperature other ICs	0 °C to +70 °C	–
Storage temperature TQMP2020	0 °C to +70 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 45: Conditions for industrial temperature range –40 to +85 °C

Parameter	Range	Remark
T_j temperature CPU	–40 °C to +125 °C	–
Case temperature DDR3 SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Storage temperature TQMP2020	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information about the thermal characteristics of the CPU are to be taken from (1).
The TQMP2020 is not protected against dust, external impact and contact (IP00). Adequate protection has to be guaranteed by the surrounding system.

6.2 Reliability and service life

No detailed MTBF calculation has been done for the TQMP2020.
The theoretical MTBF of the TQMP2020 is approximately 1 / FIT = 1 / (800×10^{-9} / h) = 1,250,000 h at +40 °C, ground benign.
The TQMP2020 is designed to be insensitive to vibration and impact.
High quality industrial grade connectors are assembled on the TQMP2020.

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMP2020 was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system. Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board; connect all TQMP2020 DGND pins.
- A good connection between PCB ground and housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and/or shielding; do not route tracks over separating trenches
- Filtering of all signals which can be connected externally (also "slow" and DC can radiate RF indirectly)

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMP2020. According to the data sheets, the devices used already have some protection; however, this is generally not sufficient to meet the legal requirements without any further measures. The following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering, in certain circumstances Zener diode
- Fast signals: Integrated protective devices (suppressor diode arrays)

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material. Due to the fact that at present there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications regarding this were not carried out.

7.5 RoHS

The TQMP2020 is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

7.6 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMP2020 was designed to be recyclable and easy to repair.

7.7 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as TQ-Systems GmbH is informed by suppliers accordingly.

7.8 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMP2020 must therefore always be seen in conjunction with the complete device.

7.9 Batteries

No batteries are assembled on the TQMP2020.

7.10 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMP2020, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMP2020 is delivered in reusable packaging.

7.11 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of this subassembly is minimised by suitable measures.
Printed PC-boards are delivered in reusable packaging.
Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 46: Acronyms

Acronym	Meaning
BGA	Ball Grid Array
COP	Common On-chip Processor
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DDR	Double Data Rate
DMA	Direct Memory Access
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
eTSEC	enhanced Three-Speed Ethernet Controller
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GP	General Purpose
I2C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP	Ingress Protection
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LSB	Least Significant Bit
LVTTL	Low Voltage Transistor Transistor Logic
MII	Media-Independent Interface
MSB	Most Significant Bit
n.a.	Not Applicable
NAND	Not-and
NC	Not Connected
NOR	Not-or
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (Interface)
PLL	Phase Locked Loop
POR	Power-On Reset
PWP	Permanent Write Protect
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTBI	Reduced Ten-Bit Interface
RTC	Real-Time Clock
RWP	Reversible Write Protect
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SMD	Surface-Mounted Device
SPI	Serial Peripheral Interface
TBI	Ten-Bit Interface
TSEC	Three-Speed Ethernet Controller
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin count Interface
UPM	User Programmable Machine
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface
UTMI+	UTMI extension supporting USB host and On-The-Go
WEEE®	Waste Electrical and Electronic Equipment

8.2 References

Table 47: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	P2020 QorIQ Integrated Processor Hardware Specifications	Rev. 0 / 04/2011	NXP
(2)	P1020 QorIQ Integrated Processor Hardware Specifications Product Preview / Preliminary, NXP Confidential Proprietary P1020EC	Rev. H Draft / 05/2010	NXP
(3)	P1021 QorIQ Integrated Processor Hardware Specifications Product Preview / Preliminary, NXP Confidential Proprietary P1021EC	Rev. H Draft / 05/2010	NXP
(4)	P1022/13 QorIQ Integrated Processor Hardware Specifications Preliminary, NXP Confidential Proprietary	Rev. D / 12/2009	NXP
(5)	P2020 QorIQ Integrated Processor Reference Manual P2020RM	Rev. 1 / 03/2011	NXP
(6)	STKP2020 User's Manual	– current –	TQ-Systems
(7)	Support-Wiki for the TQMP2020	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

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