STKP2020
User's Manual

STKP2020 UM 100
17.10.2011

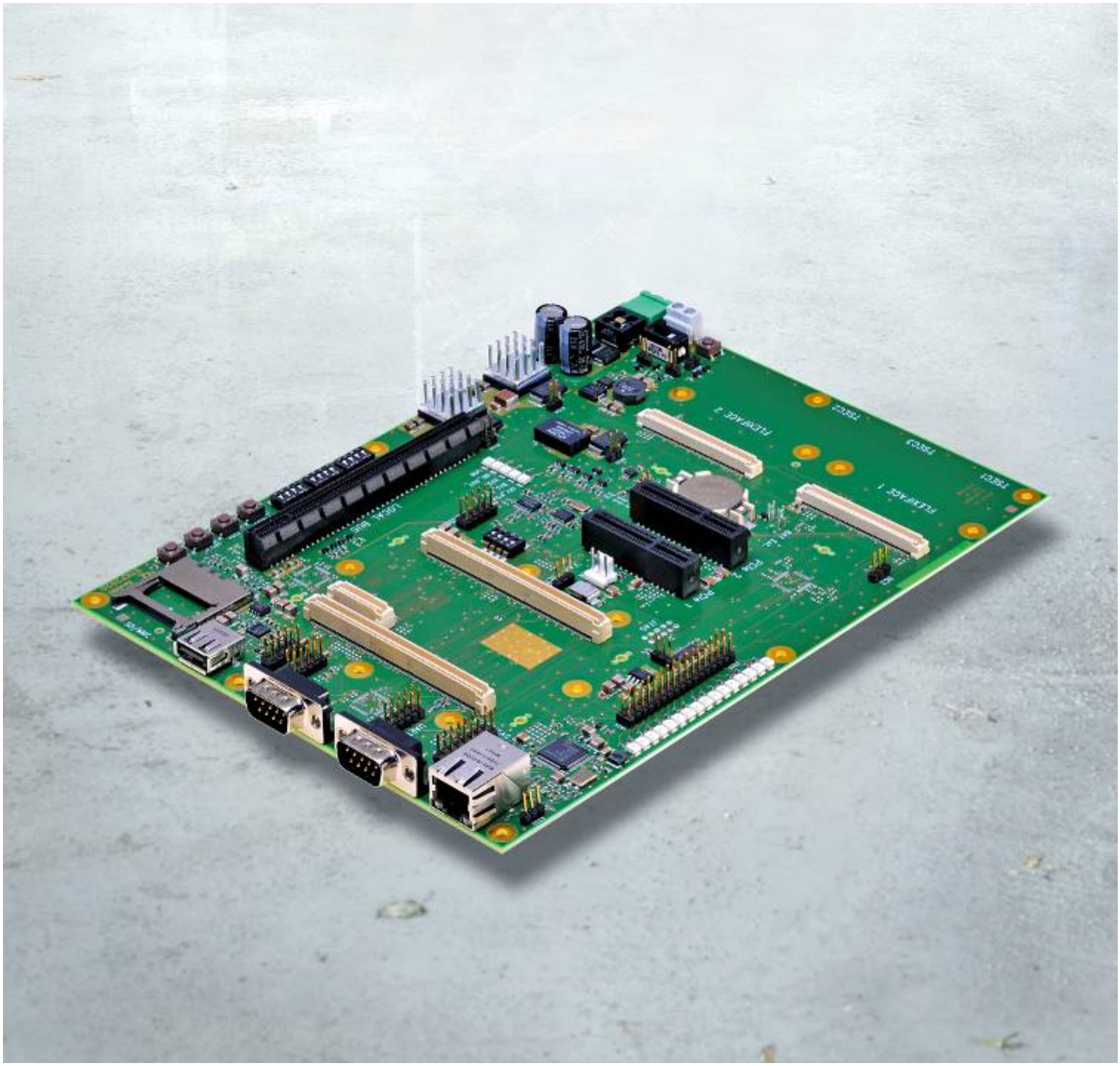

TABLE OF CONTENTS

1. ABOUT THIS MANUAL 1
1.1 Copyright and licence expenses 1
1.2 Registered trademarks 1
1.3 Disclaimer 1
1.4 Imprint 1
1.5 Tips on safety 2
1.6 Symbols and typographic conventions 2
1.7 Handling and ESD tips 2
1.8 Naming of signals 3
1.9 Further applicable documents / presumed knowledge 3
1.10 Acronyms and definitions 4
2. BRIEF DESCRIPTION 5
3. TECHNICAL DATA 6
3.1 Functionality and system architecture overview 6
3.2 Technical data overview 7
3.2.1 Technical data electronics 7
3.2.2 Technical data mechanics 8
3.2.3 Component placement 8
3.3 Electronics specification 9
3.3.1 External interfaces 9
3.3.1.1 Power supply 9
3.3.1.2 COM1 (RS232) 11
3.3.1.3 COM2 (RS232) 12
3.3.1.4 On-board gigabit Ethernet 13
3.3.1.5 USB 15
3.3.1.6 SD card slot 17
3.3.1.7 COP/JTAG P2020 19
3.3.1.8 JTAG chain 20
3.3.1.9 UART 21
3.3.1.10 SPI 23
3.3.1.11 GPIO 24
3.3.1.12 IEEE® 1588 25
3.3.1.13 I^2C 26
3.3.2 Internal interfaces 27
3.3.2.1 PCIe slots 27
3.3.2.2 FlexiFace® 1 (2 × gigabit Ethernet) 30
3.3.2.3 FlexiFace® 2 (1 × gigabit Ethernet) 32
3.3.2.4 Local bus slot 34
3.3.2.5 Fan connector 37
3.3.3 System components 38
3.3.3.1 Processor board TQMP2020 38
3.3.3.2 SERDES clock generation 43
3.3.3.3 Ethernet clock generation 45
3.3.3.4 I^2C-bus 46
3.3.3.5 I^2C I/O expander 1 (DIP switches, push-buttons) 47
3.3.3.6 I^2C I/O expander 2 (LEDs) 48
3.3.3.7 JTAG chain 51
3.3.3.8 Battery socket 53
3.3.3.9 Power supply 54
3.3.3.9.1 Power supply block diagram 54
3.3.3.9.2 Input power supply 54
3.3.3.9.3 Voltage generation 5 V 54
3.3.3.9.4 Voltage generation 3.3 V and 3.3 V PCIe 54
3.3.3.9.5 Voltage generation 2.5 V 56
3.3.3.9.6 Voltage generation 12 V PCIe 56
3.3.3.9.7 LED V810: 12 V PCIE ERR 57
3.3.3.9.8 Current measurement 57
3.3.3.9.9 Power consumption 58
3.3.3.10 Voltage supervision and reset generation 59

TABLE OF CONTENTS (continued)

3.3.4 User's interfaces 59
3.3.4.1 On-off switch 59
3.3.4.2 Reset push-button 59
3.3.4.3 User DIP switches 60
3.3.4.4 User push-buttons 60
3.3.4.5 User LEDs 60
3.3.4.6 Status / Error LEDs 60
3.3.4.7 Ethernet LEDs 60
3.3.4.8 SERDES clock DIP switch 60
4. SOFTWARE SPECIFICATION 61
5. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS 61
5.1 EMC characteristics 61
5.2 Operational safety and personal security 61
6. CLIMATIC AND OPERATIONAL CONDITIONS 61
6.1 Reliability and product life 61
6.2 Environment protection 61
6.2.1 RoHS compliance 61
6.2.2 Other entries 61

TABLE DIRECTORY

Table 1: Terms and Conventions 2
Table 2: Acronyms 4
Table 3: Pinout of power supply connector (X601) 9
Table 4: Suitable mating plug (power supply connector) for X601 9
Table 5: Pinout of power supply terminal (X600) 9
Table 6: Pinout of header for external power-on (X630) 10
Table 7: Used type of connector (header for external power-on) 10
Table 8: Pinout of COM1 (X210, D-sub connector) 11
Table 9: Pinout of COM2 (X210, D-sub connector) 12
Table 10: Pinout of Ethernet jack (X380) 14
Table 11: Pinout of USB jack 16
Table 12: Pinout of SD card slot (X200) 17
Table 13: Pinout of COP/JTAG (X230) 19
Table 14: Used type of connector (COP/JTAG) 19
Table 15: Pinout of JTAG chain header (X240) 20
Table 16: Used type of connector (JTAG chain header) 20
Table 17: Pinout of UART header (X130) 22
Table 18: Used type of connector (UART header) 22
Table 19: Pinout of SPI header (X140) 23
Table 20: Used type of connector (SPI header) 23
Table 21: Pinout of GPIO header (X150) 24
Table 22: Used type of connector (GPIO header) 24
Table 23: Pinout of IEEE® 1588 header (X410) 25
Table 24: Used type of connector (IEEE® 1588 header) 25
Table 25: Pinout of I²C 1 header (X160) 26
Table 26: Pinout of I²C 2 header (X170) 26
Table 27: Used type of connector (I²C 1 header) 26
Table 28: Used type of connector (I²C 2 header) 26
Table 29: Pinout of PCIe-slot 1 (X450) 28
Table 30: Pinout of PCIe-Slot 2 (X470) 29
Table 31: Pinout of FlexiFace® 1 (X400) 31
Table 32: Pinout of FlexiFace® 2 (X900) 33
Table 33: Pinout of local bus slot (X550) 35
Table 34: Pinout of fan connector (X621) 37
Table 35: Pinout of jumper fan voltage (X620) 37
Table 36: Used type of connector (fan connector) 37
Table 37: Used type of connector (Jumper fan voltage header) 37
Table 38: Pinout of TQMP2020 module connector (X100) 39
Table 39: Pinout of TQMP2020 module connector (X120) 40
Table 40: Pinout of TQMP2020 module connector (X110) 42
Table 41: Used parts (connectors to the processor board) 42
Table 42: SERDES reference frequency per protocol 43
Table 43: Configuration of SERDES clock frequency 44
Table 44: Configuration of SERDES clock spread spectrum 44
Table 45: Assignment of I²C I/O expander 1 to DIP switches and push-buttons 47
Table 46: Assignment of I²C I/O expander 2 to LEDs 48
Table 47: Pinout of LED jumper header (X260) 50
Table 48: Pinout of additional header for extension board (X261) 50
Table 49: Used type of connector (LED jumper header) 50
Table 50: Used type of connector (additional header for extension board) 50
Table 51: Pinout of JTAG test connector (X240) 52
Table 52: Used type of connector (JTAG test connector) 52
Table 53: Pinout of RTC battery external supply / measurement (X610, X611) 53
Table 54: Current measurement on the STKP2020 57
Table 55: Current consumption STKP2020 in different load scenarios 58
Table 56: Voltages and currents on the STKP2020 58
Table 57: Pinout of HRESET_REQ# jumper (X871) 59
Table 58: Used type of connector (HRESET_REQ# jumper) 59

ILLUSTRATION DIRECTORY

Illustration 1: STKP2020 image 5
Illustration 2: STKP2020 block diagram 6
Illustration 3: Top view STKP2020 8
Illustration 4: Position of power supply connectors 9
Illustration 5: Position of on-off switch and header for external power-on 10
Illustration 6: Position of COM1 interface 11
Illustration 7: Position of COM2 interface 12
Illustration 8: On-board gigabit Ethernet interface, schematic illustration 13
Illustration 9: Position of on-board gigabit Ethernet interface 13
Illustration 10: Position of SGMII configuration-EEPROM and header 14
Illustration 11: Position of USB jack 15
Illustration 12: Position of USB_PWR_OK LED 15
Illustration 13: Position of USB_PWR ERR LED 16
Illustration 14: Position of SD card slot 17
Illustration 15: Position of COP/JTAG connector 19
Illustration 16: Position of JTAG chain header 20
Illustration 17: UART interfaces, schematic illustration 21
Illustration 18: Position of UART header 21
Illustration 19: Position of SPI header 23
Illustration 20: Position of GPIO header 24
Illustration 21: Position of IEEE® 1588 header 25
Illustration 22: Position of I²C headers 26
Illustration 23: Position of PCIe slots 27
Illustration 24: FlexiFace® 1, schematic illustration 30
Illustration 25: Position of FlexiFace® 1 - slot 30
Illustration 26: FlexiFace® 2, schematic illustration 32
Illustration 27: Position of FlexiFace® 2 slot 32
Illustration 28: Position of local bus slot 34
Illustration 29: Position of fan connector and jumper 37
Illustration 30: Position of plug connectors for TQMP2020 38
Illustration 31: Position of DIP switch for SERDES clock parametrisation 43
Illustration 32: Position of jumper for Ethernet clock selection 45
Illustration 33: Wiring of I²C buses 46
Illustration 34: Position of DIP switches and push-buttons 47
Illustration 35: Position of user LEDs and jumpers 48
Illustration 36: Position of X621 for extension board GPIO 49
Illustration 37: Architecture of JTAG chain 51
Illustration 38: Position of JTAG test connector 52
Illustration 39: Position of battery socket 53
Illustration 40: Power supply block diagram 54
Illustration 41: Position of headers “3.3 V measuring resistors” 55
Illustration 42: Position of Error-LEDs VCC3V3, VCC3V3_PCIE 55
Illustration 43: Position of header “12 V PCIe measuring resistor” 56
Illustration 44: Position of Error-LED VCC12V_PCIE 57
Illustration 45: Position of HRESET_REQ# jumper 59

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1. ABOUT THIS MANUAL

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the module and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the used modules:**
  These documents describe the service, functionality and special characteristics of the used module (incl. BIOS).
- **Specifications of the used components:**
  The manufacturer's specifications of the used components, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram STKP2020.SP.0100.pdf
- CPU Manual P2020: P2020RM.pdf, P2020EEC_RevF.pdf
- User's Manual TQMP2020.UM.100
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of ELDK (http://www.denx.de/wiki/DULG/ELDK)

1.10 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 2: Acronyms

Acronym	Meaning
CPU	Central Processing Unit
COP	Common On-chip Processor
DIN	Deutsche Industrie Norm
DC	Direct Current
DC/DC	Direct Current/Direct Current
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electro-Magnetic Compatibility
ESD	Electro-Static Discharge
eSDHC	Enhanced Secure Digital High Capacity
eTSEC	Enhanced Three-Speed Ethernet Controller
GPIO	General Purpose Input/Output
Gbps	Gigabit per second
IP	Ingress Protection
I/O	Input/Output
IEEE®	Institute of Electrical and Electronics Engineers
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LDO	Low Drop-Out
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect express
Phy	Physical (interface)
PCB	Printed Circuit Board
PLD	Programmable Logic Device
PD	Pull-Down (resistor)
PQ	Product Qualification
PU	Pull-Up (resistor)
RTC	Real-Time Clock
RS232	Recommended Standard (serial interface)
RGMII	Reduced Gigabit Media Independent Interface
RJ45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
SD-Card	Secure Digital Card
SDHC	Secure Digital High Capacity
SD/MMC	Secure Digital Multimedia Card
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface
SERDES	Serializer/Deserializer
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WEEE	Waste Electrical and Electronic Equipment

2. BRIEF DESCRIPTION

Illustration 1: STKP2020 image

The Starterkit STKP2020 serves as a baseboard for the module TQMP2020.
It is a reference platform with which the functions of the TQMP2020 can be shown and evaluated.
The module TQMP2020 is based on the Freescale QorIQ-CPU P2020.
Models with pin-compatible processors (P2010, P1020, P1011, P1021, and P1012) are also possible.
The Starterkit STKP2020 also serves as a baseboard for these models.
The following features mark the advantage of the Starterkit:

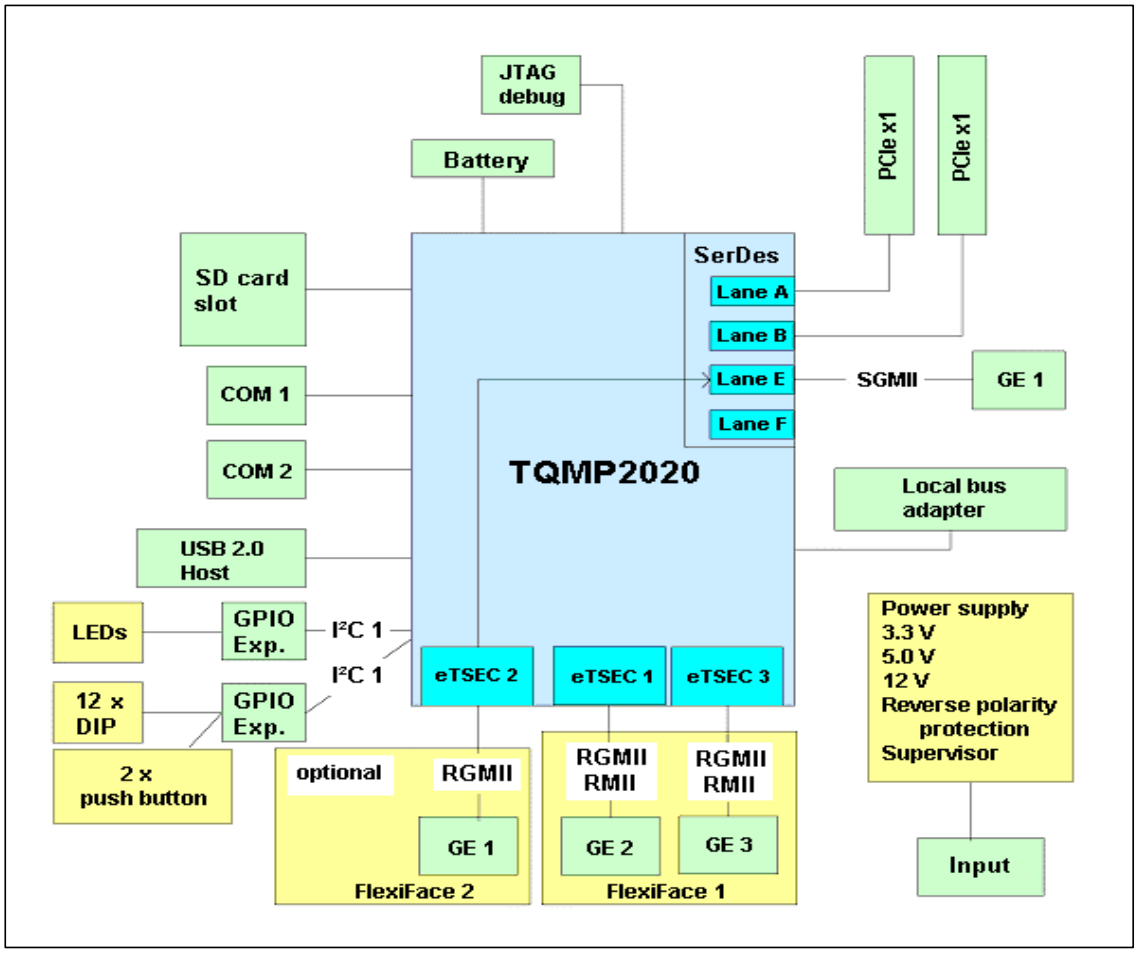
- Saving in time by early adaptation of software components on the target system.
- Users who design their own mainboard receive the circuit diagrams of the starter kit from TQ-Systems.
  The user saves time, because frequently required parts of the circuit can be taken over from the schematic.
- Risk minimisation by being able to evaluate single system requirements before completion of the whole system, e.g., test of response times, transfer speeds, CPU performance, thermal behaviour etc.
- Minimisation of risk and time saving by being able to test customised functions, e.g., for PCI or PCIe or similar extension interfaces and to customise the software if necessary.
- Saving in time during start-up of the customised mainboard by reference measurements on the Starterkit.
- Time saving with troubleshooting on the customer's system by referencing to an examined, certified Starterkit platform.
- Comfortable start-up, because all necessary components like power supply, cable, module extractor, documentation, heat sink and software are already included in the delivery.

3. TECHNICAL DATA

3.1 Functionality and system architecture overview

The following block diagram shows the interfaces and system components of the STKP2020:

Illustration 2: STKP2020 block diagram



3.2 Technical data overview

3.2.1 Technical data electronics

System components:

- Processor board: TQMP2020
- SGMII PHY and transformer for gigabit Ethernet
- USB 2.0 Phy and USB power switch
- I^2C I/O expander for user's switches and user's push-buttons
- I^2C I/O expander for user LEDs
- Clock buffer for selection of Ethernet clock source
- Clock generator and clock buffer for selection of SERDES clock source
- Battery socket for clock (RTC) on the module
- Inverse-polarity protection for input voltage
- Generation of internal supply voltages: 2.5 V, 3.3 V, 5 V, 3V3_PCIE and 12V_PCIE
- Voltage supervision and reset generation
- JTAG chain and test PLDs

Internal interfaces:

- PCIe slot 1
- PCIe slot 2
- FlexiFace® 1
- FlexiFace® 2
- Local bus slot
- Fan connector

External interfaces to other systems and devices:

- Supply voltage: 18 V to 28 V DC
- COM1 as RS232
- COM2 as RS232
- On-board gigabit Ethernet
- USB 2.0 host interfaces with supply of the devices (500 mA @ 5 V)
- SD card slot
- COP/JTAG connector for the processor P2020
- JTAG chain for production test
- 2 × UART via header
- SPI with four CS via header
- 8 × GPIO via header
- IEEE® 1588 signals via header
- 2 × I^2C-bus via header

User's interfaces:

- On-off switch
- Reset push-button
- Three 4-fold user DIP switches (function freely programmable)
- Four user push-buttons (function freely programmable)
- 16 user LEDs (function freely programmable)
- Five power LEDs (12V_PCIE ERR, 3V3 PCIE ERR, 3V3 ERR, USB_PWR ERR, USB_PWR_OK)
- Ethernet-LEDs (Link/Activity or Speed) integrated in the RJ45 jack
- A 4-fold DIP switch to select SERDES clock and spread spectrum

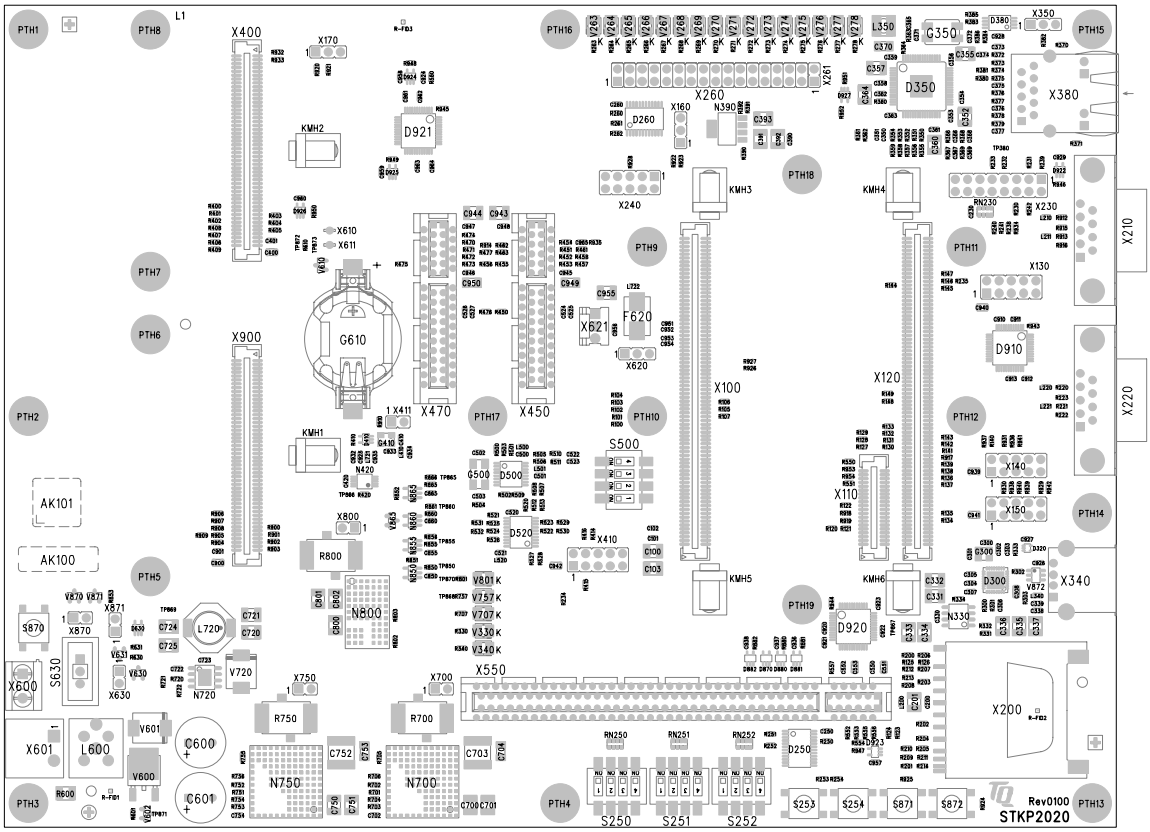
3.2.2 Technical data mechanics

The overall dimensions of the 12-layer PCB of the STKP2020 are 230 × 170 mm².
Hexagonal bolts M3 × 12 are mounted at the STKP2020 PCB as spacers.
M3 bolts are already premounted on the STKP2020 to securely screw the FlexiFace® boards.
With the provided screws M3 × 5 the FlexiFace® boards can be mounted on the M3 bolts.

3.2.3 Component placement

The following component placement view of the top side of the STKP2020 serves as orientation in order to search for interfaces and other components. With all following enlarged details this view serves as a reference.

Illustration 3: Top view STKP2020



	All detailed illustrations shown in this document have the same orientation as this top view. This illustration is also available in pdf-format as a single file.

3.3 Electronics specification

3.3.1 External interfaces

In the following section the interfaces to other systems and devices of the STKP2020 are described.

3.3.1.1 Power supply

The supply voltage range of the STKP2020 is 18 V to 28 V DC.
A suitable table top power supply (TR70A18-01A03 IPC, 18 V; 3.9 A) is included in the delivery of the STKP2020.
This or a comparable CE-certified, protective-isolated DC power supply can be connected via a 2-pin Phoenix connector (X601).

The following illustration shows the position of the power supply connectors on the STKP2020:

Illustration 4: Position of power supply connectors

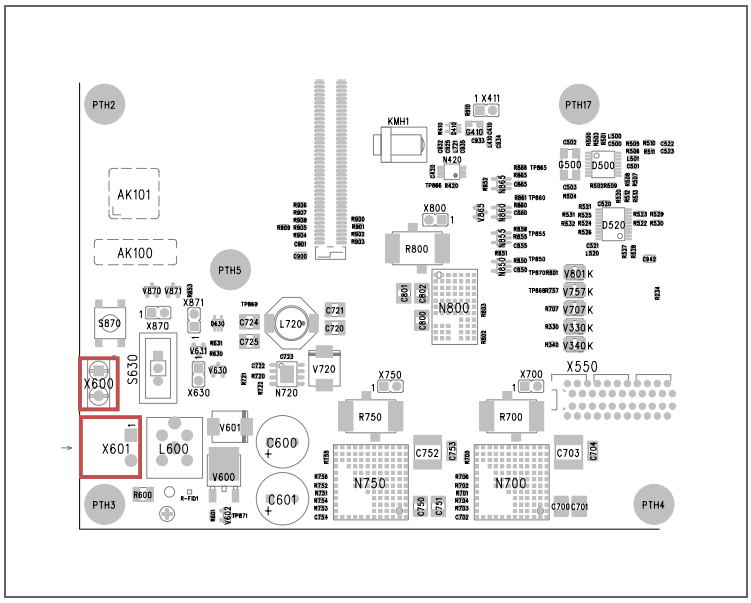


Table 3: Pinout of power supply connector (X601)

Pin	Signal name	Remark
1	VIN	18 V to 28 V DC
2	GND	Ground

Table 4: Suitable mating plug (power supply connector) for X601

Manufacturer / type	Description
Phoenix /, MSTB 2,5/ 2-ST-5,08	2-pin, 5.08 mm pitch, maximum 250 V, 12 A

Alternatively the power supply can also be connected to screw terminal (X600).

Table 5: Pinout of power supply terminal (X600)

Pin	Signal name	Remark
1	VIN	18 V to 28 V DC
2	GND	Ground

An external power supply (laboratory power supply, alternative table top power supply) should be able to supply min. 3.9 A, as the provided table top power supply TR70A18.
Details about the current consumption can be taken from section 3.3.3.9.9.

The following protection circuits exist at the supply input:

- Input filter
- Protection against reversing polarity of the supply voltage

Several DC/DC converters and LDOs generate the voltages required on the STKP2020 from the input voltage (cf. section 3.3.3.9). To switch these converters on, the on-off switch (S630) must be pressed. It is marked with "On-off" in the silk screen.

The board can also be switched on externally. A header (X630) is available on the STKP2020 for this purpose.
If both pins of the header are connected, the board is switched off.
If the connection is opened, the DC/DC converters are switched on and the board starts.

The following illustration shows the position of the on-off switch as well as the header on the STKP2020:

Illustration 5: Position of on-off switch and header for external power-on

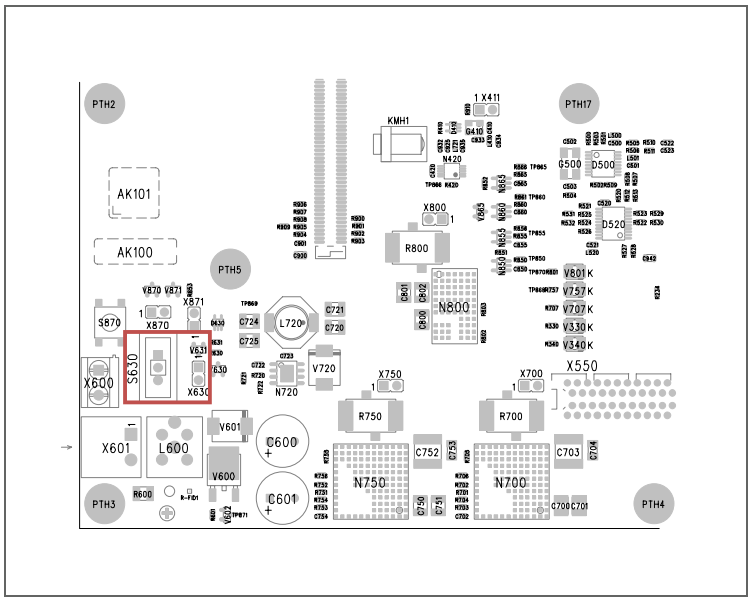


Table 6: Pinout of header for external power-on (X630)

Pin	Signal	Description
1	MR#	MR# of the supervisor device D630
2	GND	Digital ground

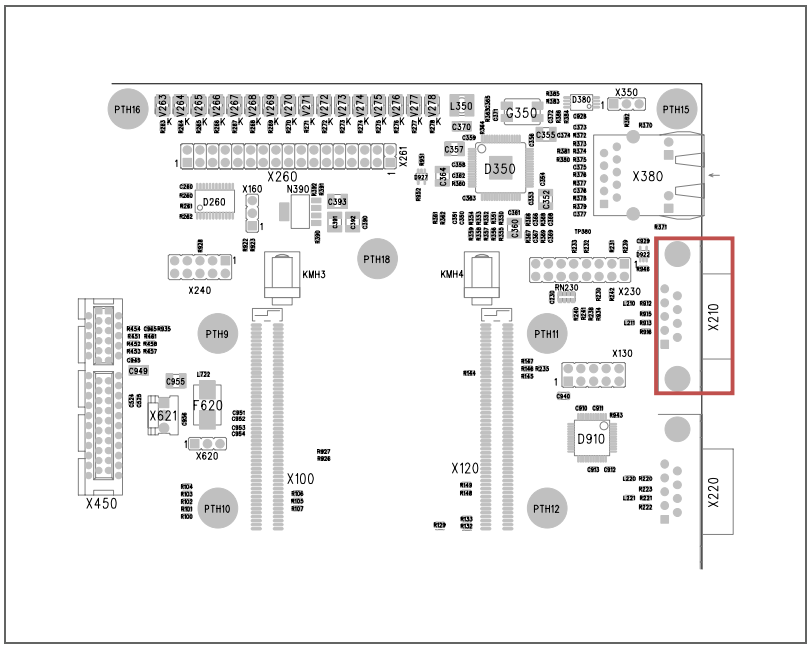
Table 7: Used type of connector (header for external power-on)

Manufacturer / type	Description
Pin header	Single row, 2.54 mm pitch, 2-pin

3.3.1.2 COM1 (RS232)

The RS232 interface COM1 is directly routed from the module TQMP2020 and brought out to D-sub connector (X210).

Illustration 6: Position of COM1 interface



An optional voltage (5 V or 12 V) can be conducted over two of the unused pins of the D-sub connector in an alternative assembly in order to supply, for example, optocouplers for an external galvanic separation.

Data rate: 4.8 kbaud to 115.2 kbaud (cable length ≤3 m)
Type of connector: 9-pin D-sub (male)
Protection circuit: TVS diodes (bidirectional)

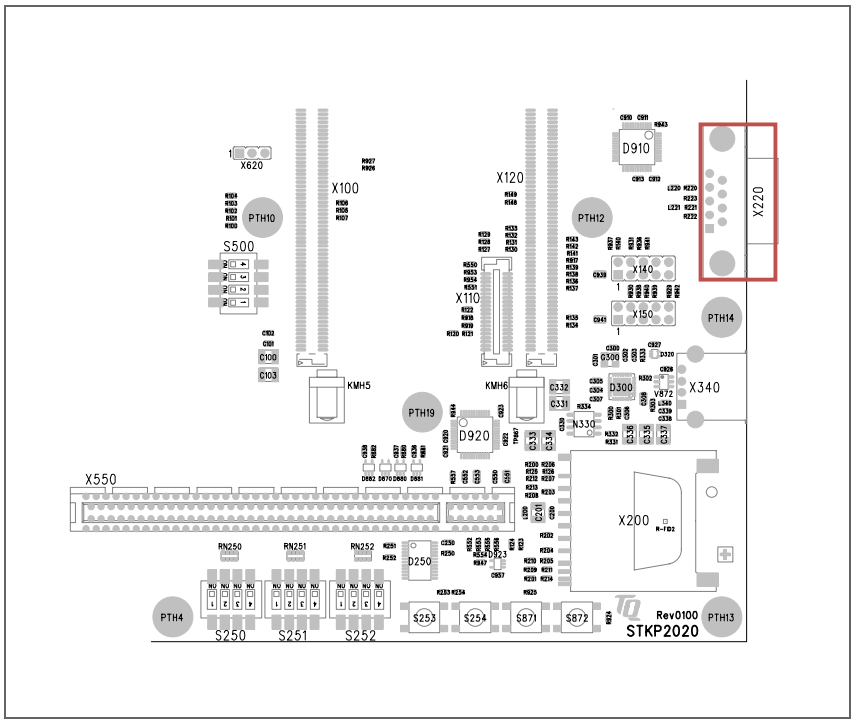
Table 8: Pinout of COM1 (X210, D-sub connector)

Pin	Signal name	Remark
1	NC	Not connected
2	RxD	Receive Data
3	TxD	Transmit Data
4	NC	Not connected, optionally 5V or 12V
5	GND	Ground
6	NC	Not connected
7	NC	Not connected, optionally 5V or 12V
8	NC	Not connected
9	NC	Not connected

3.3.1.3 COM2 (RS232)

The RS232 interface COM2 is directly routed from the module TQMP2020 and brought out to D-sub connector (X220).

Illustration 7: Position of COM2 interface



An optional voltage (5 V or 12 V) can be conducted over two of the unused pins of the D-sub connector in an alternative assembly in order to supply, for example, optocouplers for an external galvanic separation.

Data rate: 4.8 kbaud to 115.2 kbaud (cable length ≤3 m)
Type of connector: 9-pin D-sub (male)
Protection circuit: TVS diodes (bidirectional)

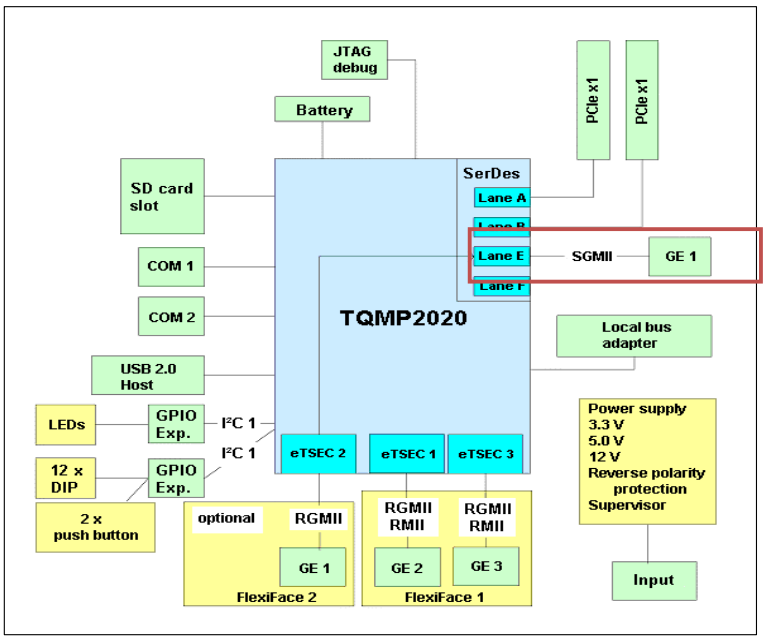
Table 9: Pinout of COM2 (X220, D-sub connector)

Pin	Signal name	Remark
1	NC	Not connected
2	RxD	Receive Data
3	TxD	Transmit Data
4	NC	Not connected, optionally 5V or 12V
5	GND	Ground
6	NC	Not connected
7	NC	Not connected, optionally 5V or 12V
8	NC	Not connected
9	NC	Not connected

3.3.1.4 On-board gigabit Ethernet

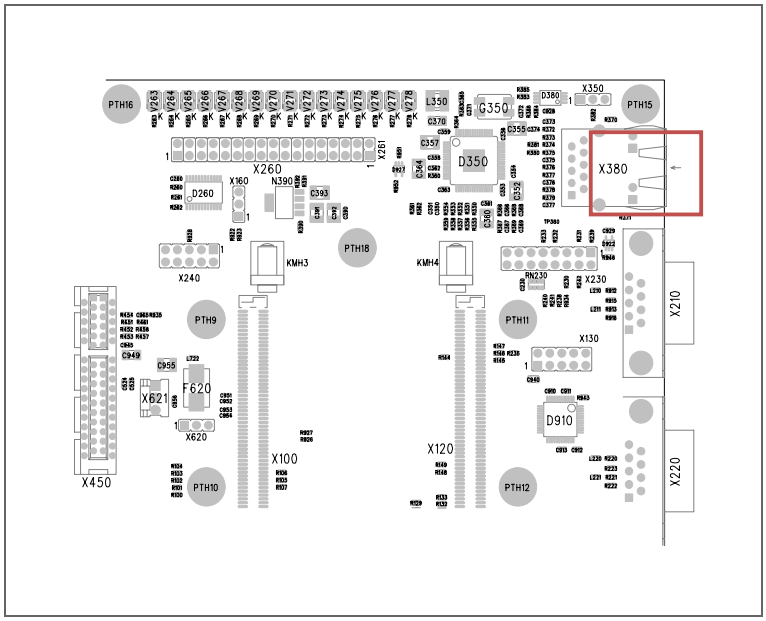
The on-board gigabit Ethernet interface is made available through eTSEC2 and the SerDes-Lane "E" of the module.
The Media Independent Interface is implemented as SGMII. Alternatively eTSEC2 can also be brought out through FlexiFace® 2.
The reset configuration of the module must therefore be updated. The necessary information is to be taken from the User's Manual of the TQMP2020. Both variations exclude one another (see also section 3.3.2.3, FlexiFace® 2 (1 × gigabit Ethernet).

Illustration 8: On-board gigabit Ethernet interface, schematic illustration



The on-board gigabit Ethernet interface is provided at a shielded RJ45 jack with integrated transformers and LEDs.
The Ethernet-MAC integrated in the P2020 is therefore connected with the Phy (D350) on the STKP2020.

Illustration 9: Position of on-board gigabit Ethernet interface



	The Phy used on the STKP2020 cannot operate with transformers with common center tap on the PHY-side.

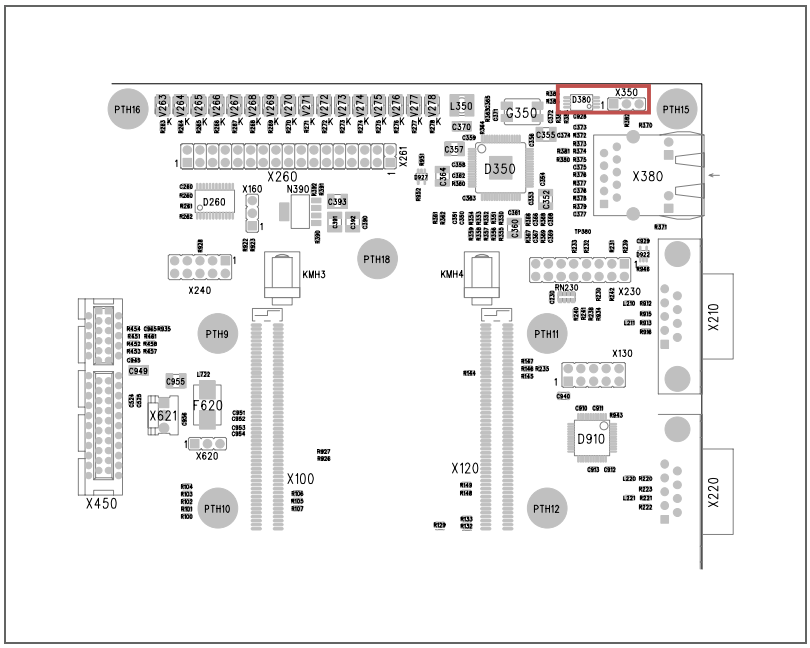
The LEDs integrated in the jack provide the following functions:

Green: lights up at an active Ethernet connection (LINK), blinks at network activity (ACTIVITY)
Yellow: lights up at a 100 Mbit connection (SPEED)

Optionally the Phy is configurable via an I²C-EEPROM (D380).
In the standard version the configuration-EEPROM for the Phy is not assembled.
The I²C-bus between Phy and EEPROM can be accessed at header X350.

The following illustration shows the position of the configuration-EEPROM and the accompanying header on the STKP2020:

Illustration 10: Position of SGMII configuration-EEPROM and header



Interface: eTSEC2 of the P2020
Configuration: MDIO (address 0x00)
PHY interrupt: IRQ3

Table 10: Pinout of Ethernet jack (X380)

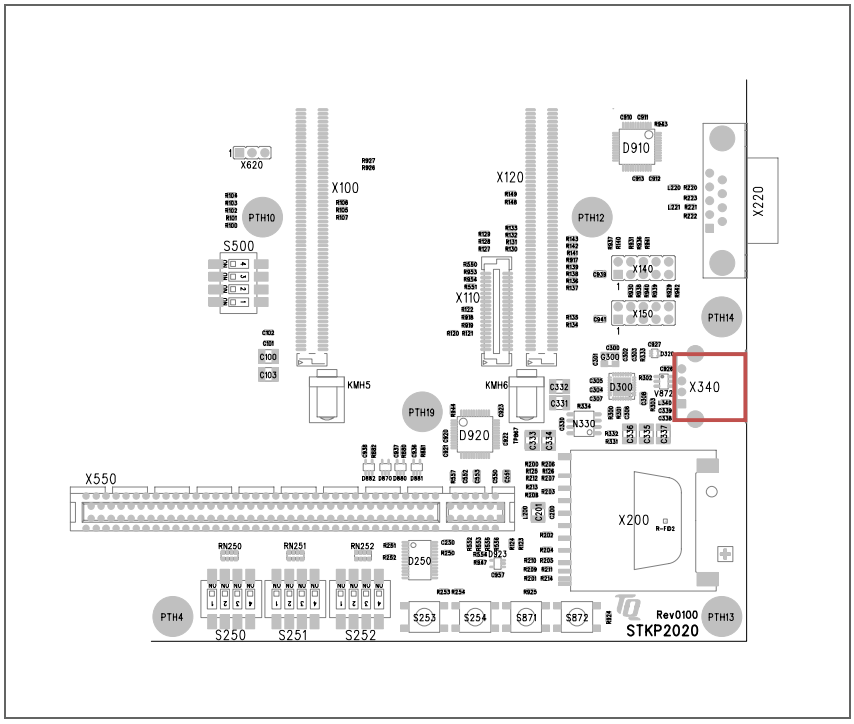
Pin	Signal name	Remark
1	BI_DA+	Bidirectional pair +A
2	BI_DA–	Bidirectional pair –A
3	BI_DB+	Bidirectional pair +B
4	BI_DB–	Bidirectional pair –B
5	BI_DC+	Bidirectional pair +C
6	BI_DC–	Bidirectional pair –C
7	BI_DD+	Bidirectional pair +D
8	BI_DD–	Bidirectional pair –D

3.3.1.5 USB

The STKP2020 provides a USB 2.0 hosts interface. It is brought out to a USB jack type A (X340).

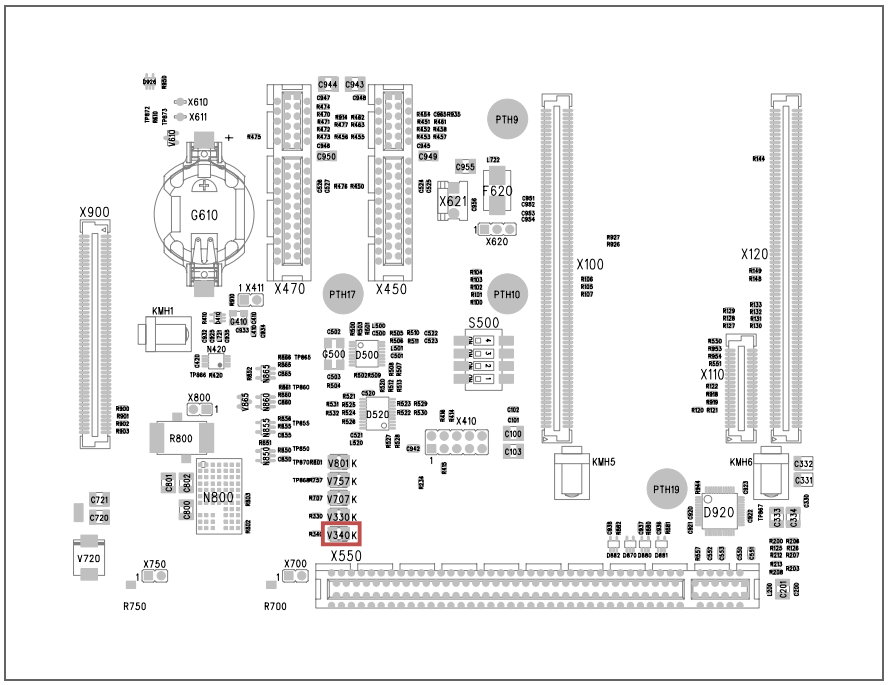
The following illustration shows the position of the USB jack on the STKP2020:

Illustration 11: Position of USB jack



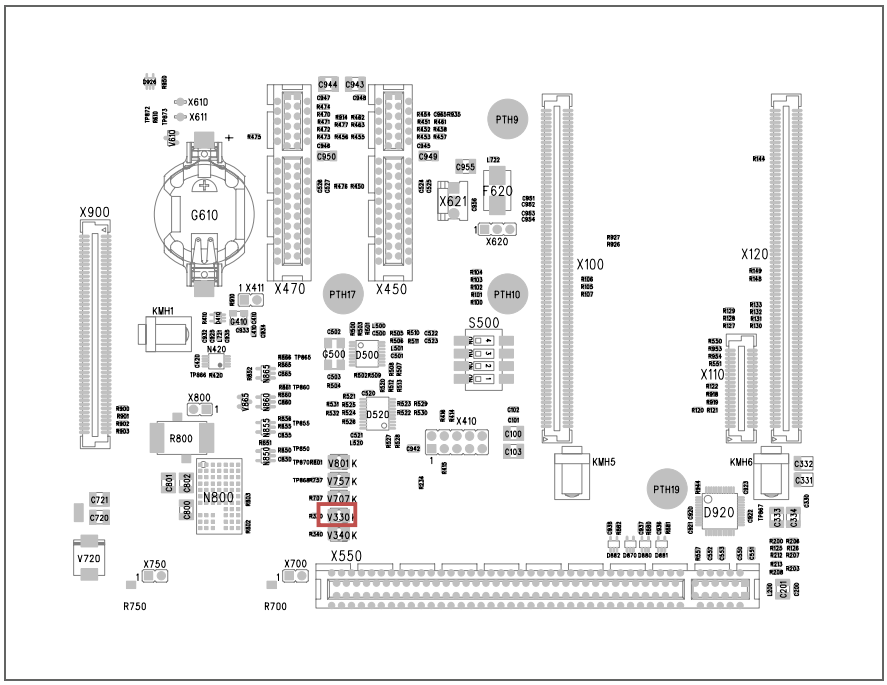
The STKP2020 supplies a USB device with a maximum of 500 mA @ 5 V.
A USB power switch protects the USB voltage against short circuit and overload.
Two LEDs indicate the state of the USB's power supply.
V340: "USB_PWR_OK" shows the presence of the supply voltage VBUS on the USB interface.

Illustration 12: Position of USB_PWR_OK LED



V330: The USB power switch controls "USB_PWR ERR" and indicates errors of the USB power supply (short circuit, overload).

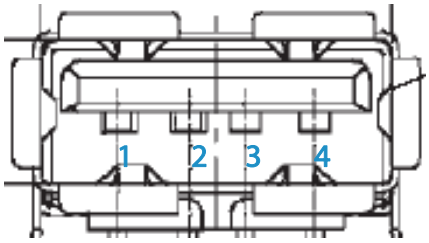
Illustration 13: Position of USB_PWR ERR LED



Interface: USB port of the P2020

The following illustration shows the pinout of the USB jack:

Table 11: Pinout of USB jack

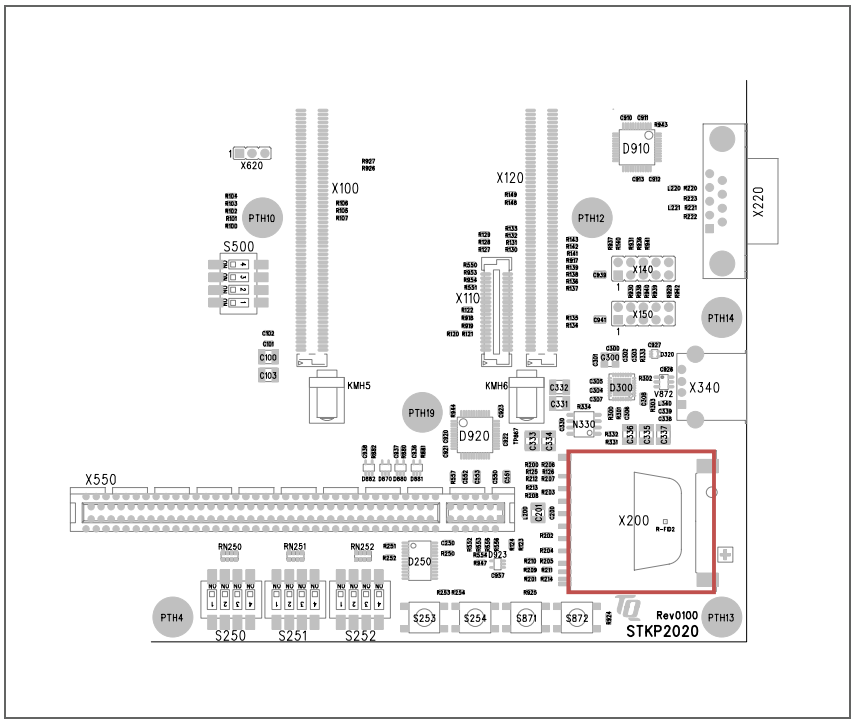
X340 host USB type A	Pin	Signal
	1	VBUS
	2	DM
	3	DP
	4	GND

3.3.1.6 SD card slot

The STKP2020 provides an SD card slot (X200). SD cards as well as MMC cards are supported.
The interface provides four data lines and supports 1-bit or 4-bit communication.
The cards operate at 3.3 V.
The SD card slot is directly connected to the Enhanced Secure Digital Host Controller (eSDHC) of the P2020.
The eSDHC is compatible with the SD Memory Card Specification, version 2.0 and provides an integrated transceiver.

The following illustration shows the position of the SD card slot on the STKP2020:

Illustration 14: Position of SD card slot



Interface: eSDHC (Enhanced Secure Digital Host Controller) of the P2020

Table 12: Pinout of SD card slot (X200)

Pin	Signal name	Remark
1	CD/DAT3/ CS	DATA3 (alternatively: Card Detect, Chip Select)
2	CMD/DI	COMMAND (alternatively: Data In)
3	VSS1	Ground
4	VDD	3.3 V
5	CLK	Clock
6	VSS2	Ground
7	DAT0/DO	DATA0 (alternatively: Data Out)
8	DAT1	DATA1
9	DAT2	DATA2
CDS	CDS	Card Detect
COM	COMMON	Ground
WP	WP	Write Protect
M1	SHIELD	Ground
M2	SHIELD	Ground

	The following modifications were carried out at the SD card interface: • SD card Card-Detect requires a pull-up instead of a pull-down ⇨ R214 removed, R201 assembled • SD card interface does not work because of a missing series resistor in the SDHC_CLK line ⇨ Pin 5 of X200 lifted, 33 Ω resistor soldered between pad 5 of X200 and the lifted pin, ⇨ ESD diode R202 removed and soldered between the lifted pin 5 of X200 and GND. • Internal pull-up at SDHC_DATA3 is too weak in some SD cards ⇨ R213 removed, 10 kΩ pull-up to VCC3V3 assembled at SDHC_DATA3.
	These modifications are not included in the original version of the circuit diagram (STKP2020.SP.0100.pdf).

3.3.1.7 COP/JTAG P2020

To connect a debugger for the processor on the TQMP2020 a 16-pin header (2.54 mm pitch) with the standard pinout is provided. This enables debugging / programming of the processor P2020.

The following illustration shows the position of the COP/JTAG connector on the STKP2020:

Illustration 15: Position of COP/JTAG connector

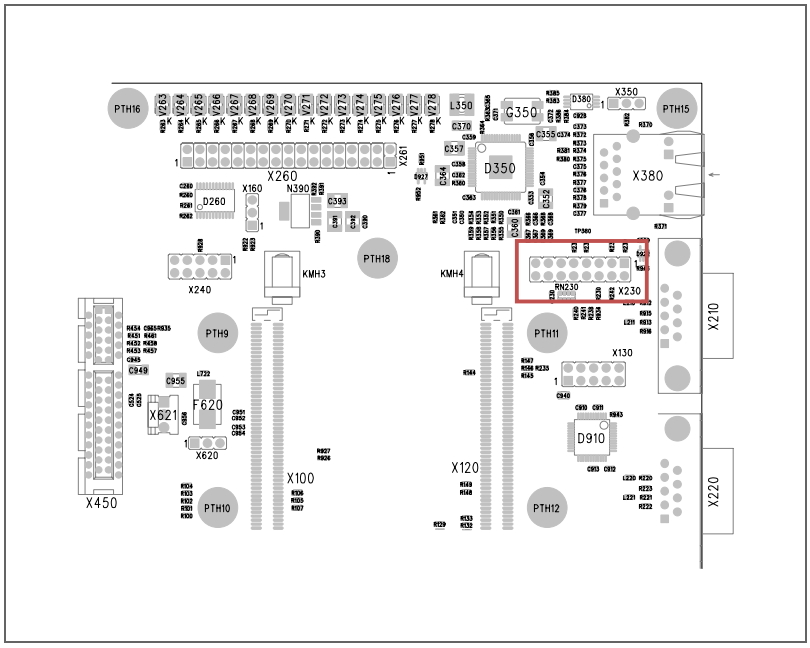


Table 13: Pinout of COP/JTAG (X230)

Pin	Signal	Type	Description
1	TDO	OUT	JTAG test data out
2	NC	–	Not connected
3	TDI	IN	JTAG test data in
4	TRST#	IN	JTAG test reset
5	NC	–	Not connected
6	3.3 V	OUT	Power out (220 Ω PU)
7	TCK	IN	JTAG Test Clock
8	CKSTP_IN0#, CKSTP_IN1#	–	Checkstop input 0 (via 0 Ω), Checkstop input 1 (via 0 Ω), 10 kΩ PU
9	TMS	IN	JTAG test mode select
10	NC	–	Not connected
11	SRESET#	IN	Soft reset
12	GND	–	Digital ground
13	RESIN#	IN	Hard reset
14	NC	–	Not connected
15	CKSTP_OUT0#, CKSTP_OUT1#	OUT	Checkstop output 0 (via 0 Ω), Checkstop output 1 (via 0 Ω)
16	GND	–	Digital ground

Table 14: Used type of connector (COP/JTAG)

Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 16-pin

3.3.1.8 JTAG chain

In addition to the COP/JTAG interface of the processor more JTAG capable components are switched in a separate chain.
This chain is accessible at header (X240).
More information about the JTAG chain can be found in section 3.3.3.7.
The header X240 is not assembled by default.

The following illustration shows the position of the JTAG chain header on the STKP2020:

Illustration 16: Position of JTAG chain header

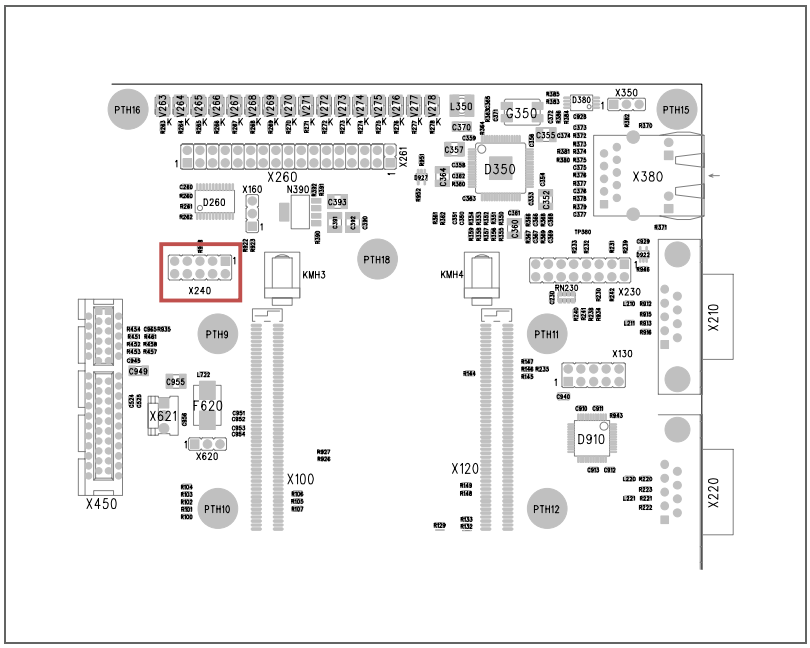


Table 15: Pinout of JTAG chain header (X240)

Pin	Signal	Type	Description
1	TCK	IN	JTAG test clock
2	GND	–	Digital ground
3	TMS	IN	JTAG test mode select
4	GND	–	Digital ground
5	TDO	OUT	JTAG test data out
6	GND	–	Digital ground
7	TDI	IN	JTAG test data in
8	GND	–	Digital ground
9	TRST#	IN	JTAG test reset
10	NC	–	Not connected

Table 16: Used type of connector (JTAG chain header)

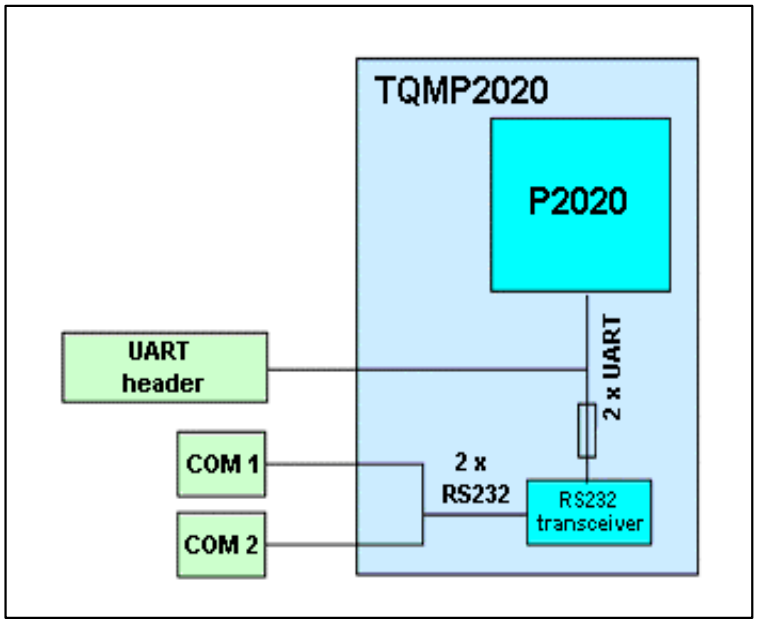
Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 10-pin

3.3.1.9 UART

The processor P2020 provides two UART interfaces. These interfaces are routed to RS232 transceivers on the TQMP2020 module by default. To provide the interfaces COM1 and COM2 the RS232 signals are routed to the STKP2020 (cf. section 3.3.1.2).
In addition, both UART interfaces are directly routed to the STKP2020 and are there accessible at header (X130).
The outputs of the transceiver are decoupled by a 4.7 kΩ resistor from the directly accessible LVTTL signals UART_SIN[0:1]#.

The following illustration shows this:

Illustration 17: UART interfaces, schematic illustration



The UART interfaces can be used at the COM ports as well as at the header.
No reconfiguration/alternative assembly on the module is necessary.
The simultaneous use of the same UART is not possible.

The following illustration shows the position of the UART header on the STKP2020:

Illustration 18: Position of UART header

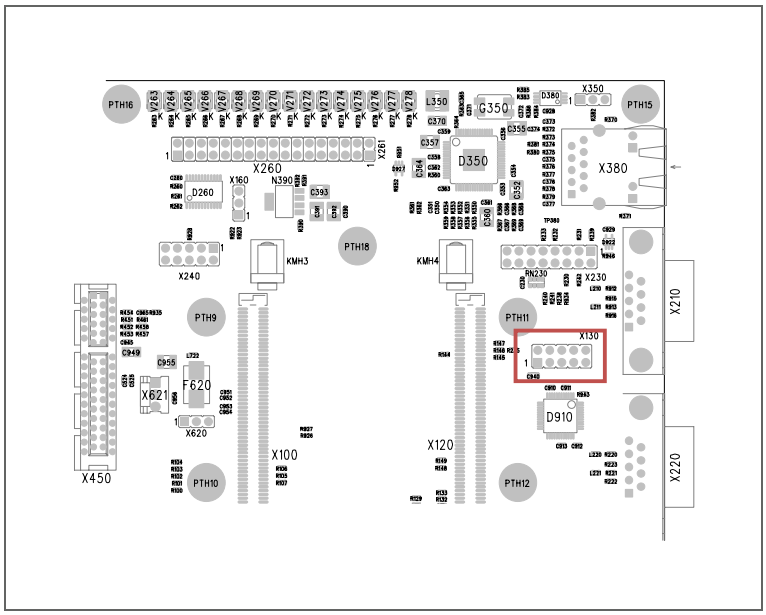


Table 17: Pinout of UART header (X130)

Pin	Signal	Description
1	VCC3V3	3.3 V
2	UART_SIN0#	UART 0 SIN
3	UART_SOUT0#	UART 0 SOUT
4	UART_RTS0#	UART 0 RTS
5	UART_CTS0#	UART 0 CTS
6	UART_SIN1#	UART 1 SIN
7	UART_SOUT1#	UART 1 SOUT
8	UART_RTS1#	UART 1 RTS
9	UART_CTS1#	UART 1 CTS
10	GND	Digital ground

The level of the UART signals is 3.3 V.

Table 18: Used type of connector (UART header)

Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 10-pin

3.3.1.10 SPI

The processor P2020 provides an SPI interface.
It is routed to the STKP2020 and accessible there at header (X140).

The following illustration shows the position of the SPI header on the STKP2020:

Illustration 19: Position of SPI header

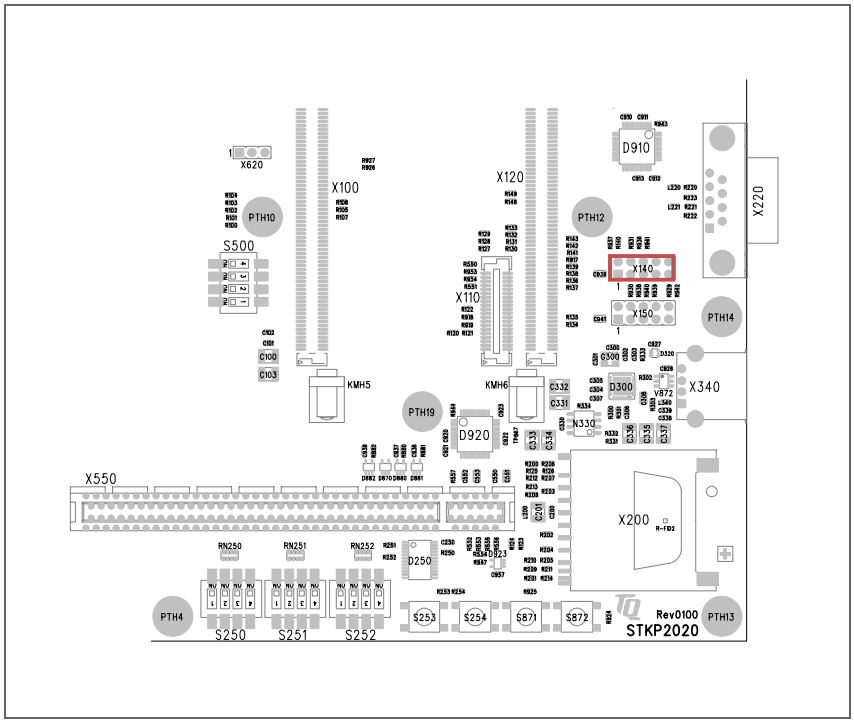


Table 19: Pinout of SPI header (X140)

Pin	Signal	Description
1	VCC3V3	3.3 V
2	SPI_MISO	Master input slave output (10 kΩ PU)
3	SPI_MOSI	Master output slave input (10 kΩ PU)
4	SPI_CS0#	Chip select 0 (10 kΩ PU)
5	SPI_CS1#	Chip select 1
6	SPI_CS2#	Chip select 2
7	SPI_CS3#	Chip select 3
8	GND	Digital ground
9	SPI_CLK	Output serial clock (1 kΩ PD)
10	GND	Digital ground

The level of the SPI signals is 3.3 V.

Table 20: Used type of connector (SPI header)

Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 10-pin

3.3.1.11 GPIO

The processor P2020 provides several GPIOs.
Some of the GPIOs are routed to the STKP2020 and there accessible at header (X150).

The following illustration shows the position of the GPIO header on the STKP2020:

Illustration 20: Position of GPIO header

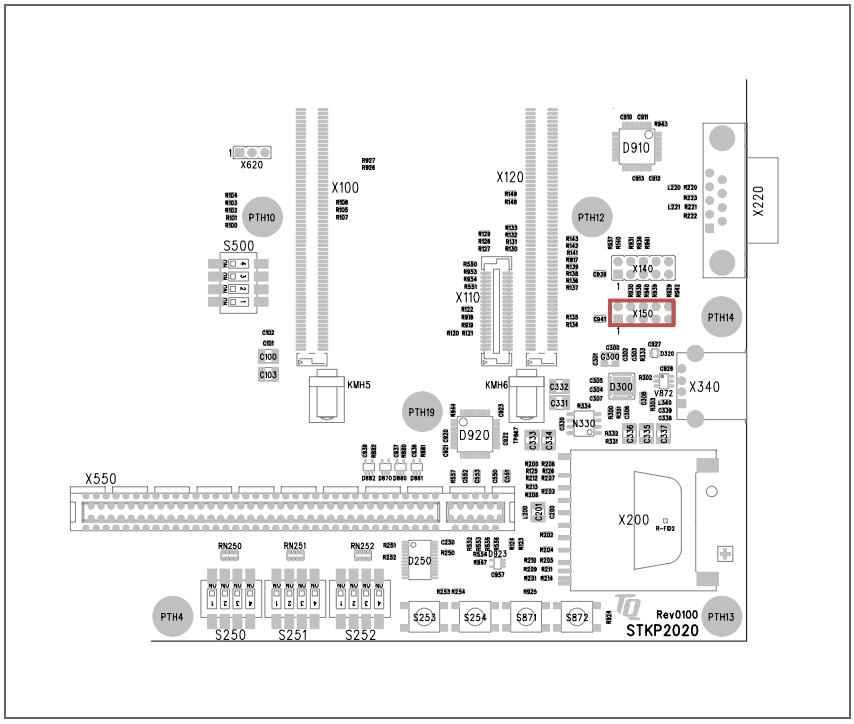


Table 21: Pinout of GPIO header (X150)

Pin	Signal	Description
1	VCC3V3	3.3 V
2	GPIO_5	General purpose I/O 5
3	GPIO_6	General purpose I/O 6
4	GPIO_7	General purpose I/O 7
5	GPIO_11/USB_PCTL1	General purpose I/O 11 (alternatively: USB power control 1)
6	GPIO_12	General purpose I/O 12
7	GPIO_13	General purpose I/O 13
8	GPIO_14	General purpose I/O 14
9	GPIO_15	General purpose I/O 15
10	GND	Digital ground

The level of the GPIOs is 3.3 V.

Table 22: Used type of connector (GPIO header)

Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 10-pin

3.3.1.12 IEEE® 1588

In its eTSEC controllers the P2020/2010 provide the possibility to mark incoming and outgoing Ethernet packets with a time stamp. This permits time synchronisation with other devices via Ethernet in the nanosecond to microsecond range.
The standard IEEE® 1588 describes the protocol for time synchronisation via Ethernet.
Based on a synchronised time

- Events can be time stamped
- Alarms can be triggered
- Periodical signals can be served.

This is enabled via dedicated I/O signals of the processor.
These are routed to the STKP2020 and there accessible at header (X410).

The following illustration shows the position of the IEEE® 1588 header on the STKP2020:

Illustration 21: Position of IEEE® 1588 header

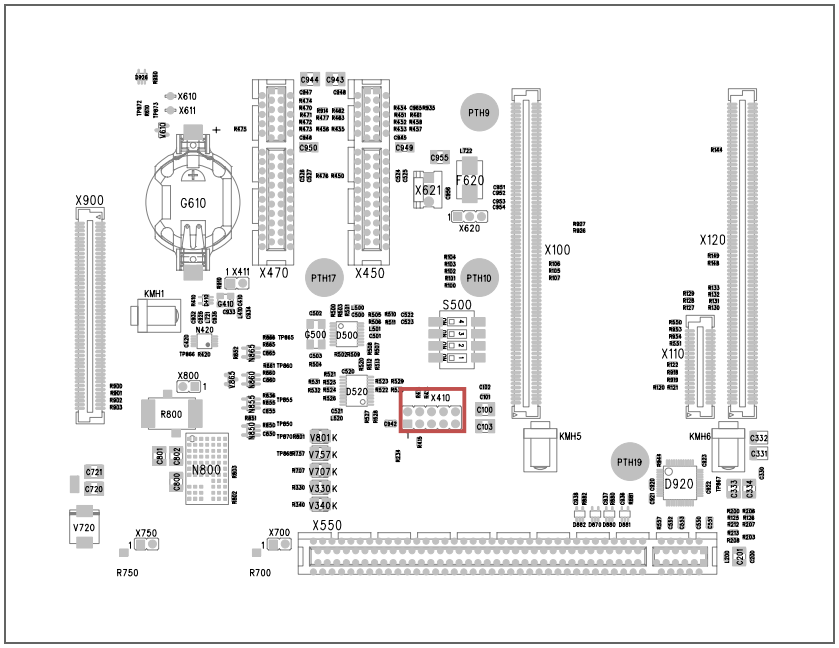


Table 23: Pinout of IEEE® 1588 header (X410)

Pin	Signal	Description
1	VCC2V5	2.5 V
2	TSEC_1588_CLK_IN	1588 clock input
3	TSEC_1588_TRIG_IN1	1588 trigger in 1
4	TSEC_1588_TRIG_IN2	1588 trigger in 2
5	TSEC_1588_ALARM_OUT1	1588 timer alarm 1
6	TSEC_1588_ALARM_OUT2	1588 timer alarm 2
7	TSEC_1588_PULSE_OUT1	1588 pulse out 1
8	TSEC_1588_PULSE_OUT2	1588 pulse out 2
9	TSEC_1588_CLK_OUT	1588 clock output
10	GND	Digital ground

The level of the IEEE® 1588 signals is **2.5 V**.

Table 24: Used type of connector (IEEE® 1588 header)

Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 10-pin

3.3.1.13 I²C

The processor P2020 provides two I²C-buses.
They are routed to the STKP2020 and each of them is accessible at a header (X160, X170).
Section3.3.3.4, I²C-bus, provides an overview of all components at the I²C-buses.

The following illustration shows the position of the I²C headers on the STKP2020:

Illustration 22: Position of I²C headers

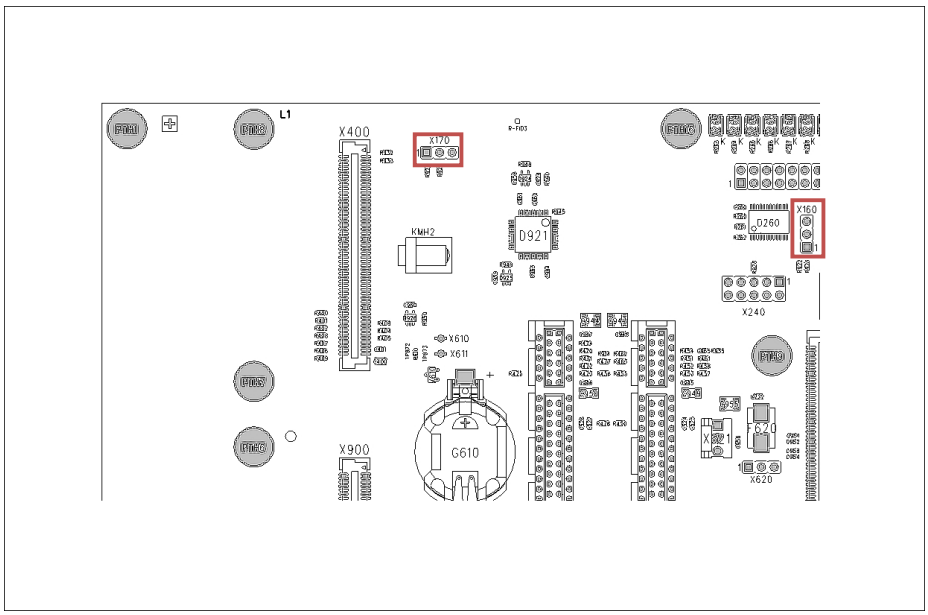


Table 25: Pinout of I²C 1 header (X160)

Pin	Signal	Description
1	IIC1_SDA	I²C 1 SDA (10 kΩ PU)
2	IIC1_SCL	I²C 1 SCL (10 kΩ PU)
3	GND	Digital ground

Table 26: Pinout of I²C 2 header (X170)

Pin	Signal	Description
1	IIC2_SDA	I²C 2 SDA (10 kΩ PU)
2	IIC2_SCL	I²C 2 SCL (10 kΩ PU)
3	GND	Digital ground

The level of the I²C signals is 3.3 V.

Table 27: Used type of connector (I²C 1 header)

Manufacturer / type	Description
Pin header	Single row, 2.54 mm pitch, 3-pin

Table 28: Used type of connector (I²C 2 header)

Manufacturer / type	Description
Pin header	Single row, 2.54 mm pitch, 3-pin

3.3.2 Internal interfaces

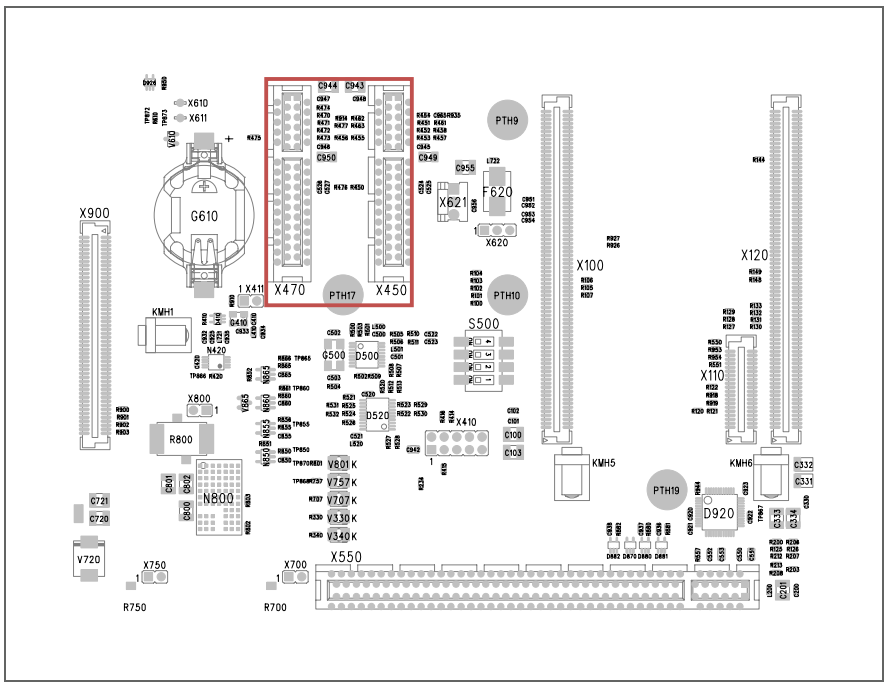
In the following all interfaces of the STKP2020, which are not interfaces to external systems, are described. This primarily covers the slots for plug-in cards.

3.3.2.1 PCIe slots

The STKP2020 provides two PCIe ×1 interfaces (X450, X470).
These are designed for standard PCIe ×1 cards, as they are used in PCs.

The following illustration shows the position of the PCIe slots on the STKP2020:

Illustration 23: Position of PCIe slots



The pinout of both PCIe slots is as follows (in accordance with specification PCIe 1.0A):

Table 29: Pinout of PCIe-slot 1 (X450)

X450	PCIe B	Pin	Pin	PCIe A	X450
VCC12V_PCIE	+12V	1	1	PRSNT1#	GND
VCC12V_PCIE	+12V	2	2	+12V	VCC12V_PCIE
NC	RSVD	3	3	+12V	VCC12V_PCIE
GND	GND	4	4	GND	GND
IIC2_SCL (optional)[1]	SMCLK	5	5	TCK	TCK (optional)[2]
IIC2_SDA (optional)	SMDAT	6	6	TDI	TDI (optional)
GND	GND	7	7	TDO	TDO (optional)
VCC3V3_PCIE	+3V3	8	8	TMS	TMS (optional)
TRST (optional)	TRST#	9	9	+3V3	VCC3V3_PCIE
VCC3V3_PCIE	3V3AUX	10	10	+3V3	VCC3V3_PCIE
NC	WAKE#	11	11	PWRGD	STK_RES#
Key notch					
NC	RSVD	12	12	GND	GND
GND	GND	13	13	REFCLK+	SD_REF_CLK0
SD_TX0	PETP[0]	14	14	REFCLK–	SD_REF_CLK0#
SD_TX0#	PETN[0]	15	15	GND	GND
GND	GND	16	16	PERP[0]	SD_RX0
PCIE_S1_PRSNT	PRSNT2#	17	17	PERN[0]	SD_RX0#
GND	GND	18	18	GND	GND
NC	PETP[1]	19	19	RSVD	NC
NC	PETN[1]	20	20	GND	GND
GND	GND	21	21	PERP[1]	NC
GND	GND	22	22	PERN[1]	NC
NC	PETP[2]	23	23	GND	GND
NC	PETN[2]	24	24	GND	GND
GND	GND	25	25	PERP[2]	NC
GND	GND	26	26	PERN[2]	NC
NC	PETP[3]	27	27	GND	GND
NC	PETN[3]	28	28	GND	GND
GND	GND	29	29	PERP[3]	NC
NC	RSVD	30	30	PERN[3]	NC
4.7 kΩ PU to 3V3_PCIE	PRSNT2#	31	31	GND	GND
GND	GND	32	32	RSVD	NC

1 To route the I^2C-bus to PCIe slot 1, the Ω resistors R462 and R463 must be assembled.
2 To connect the JTAG interface with PCIe slot 1, the 0 Ω resistors R451 – R455 must be assembled. More information can be found in section 3.3.3.7.

Table 30: Pinout of PCIe-Slot 2 (X470)

X470	PCIe B	Pin	Pin	PCIe A	X470
VCC12V_PCIE	+12V	1	1	PRSNT1#	GND
VCC12V_PCIE	+12V	2	2	+12V	VCC12V_PCIE
NC	RSVD	3	3	+12V	VCC12V_PCIE
GND	GND	4	4	GND	GND
IIC2_SCL (optional)[3]	SMCLK	5	5	TCK	TCK (optional)[4]
IIC2_SDA (optional)	SMDAT	6	6	TDI	TDI (optional)
GND	GND	7	7	TDO	TDO (optional)
VCC3V3_PCIE	+3V3	8	8	TMS	TMS (optional)
TRST (optional)	TRST#	9	9	+3V3	VCC3V3_PCIE
VCC3V3_PCIE	3V3AUX	10	10	+3V3	VCC3V3_PCIE
NC	WAKE#	11	11	PWRGD	STK_RES#
Key notch					
NC	RSVD	12	12	GND	GND
GND	GND	13	13	REFCLK+	SD_REF_CLK1
SD_TX1	PETP[0]	14	14	REFCLK–	SD_REF_CLK1#
SD_TX1#	PETN[0]	15	15	GND	GND
GND	GND	16	16	PERP[0]	SD_RX1
PCIE_S2_PRSNT	PRSNT2#	17	17	PERN[0]	SD_RX1#
GND	GND	18	18	GND	GND
NC	PETP[1]	19	19	RSVD	NC
NC	PETN[1]	20	20	GND	GND
GND	GND	21	21	PERP[1]	NC
GND	GND	22	22	PERN[1]	NC
NC	PETP[2]	23	23	GND	GND
NC	PETN[2]	24	24	GND	GND
GND	GND	25	25	PERP[2]	NC
GND	GND	26	26	PERN[2]	NC
NC	PETP[3]	27	27	GND	GND
NC	PETN[3]	28	28	GND	GND
GND	GND	29	29	PERP[3]	NC
NC	RSVD	30	30	PERN[3]	NC
4.7 kΩ PU to 3V3_PCIE	PRSNT2#	31	31	GND	GND
GND	GND	32	32	RSVD	NC

The signals PCIE_S2_PRSNT and PCIE_S1_PRSNT are routed to the clock buffer (D520) to automatically switch on the reference clock when a PCIe card is present.
The SERDES interface on the TQMP2020 can be supplied with different clock frequencies.
To improve EMC characteristics the clock can additionally be spread (spread spectrum).
The setting of these parameters is described in section 3.3.3.2, SERDES clock generation.

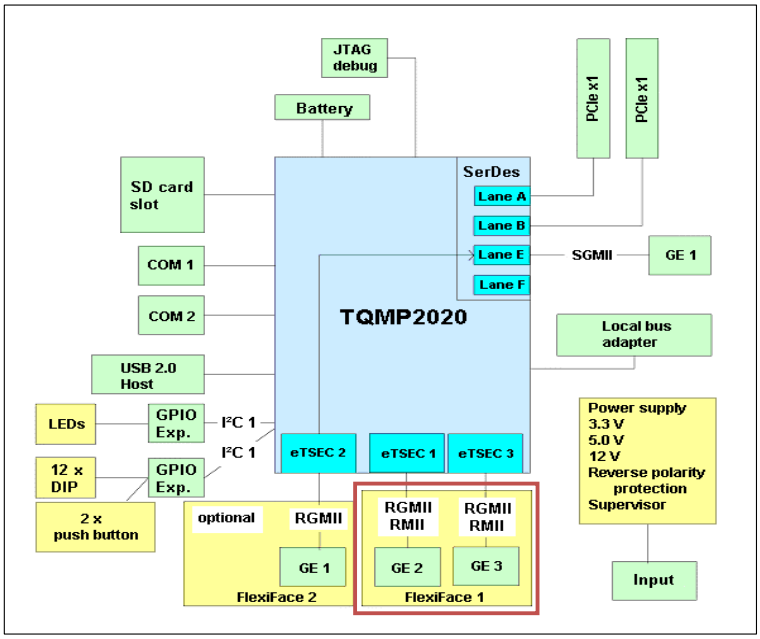
Please note:
The maximum load on the 12 V rail (VCC12V_PCIE) of both PCIe slots is 3 A in total.
The maximum load on the 3.3 V rail (VCC3V3_PCIE) of both PCIe slots is 12 A in total.

3 To route the I^2C-bus to PCIe slot 2, the 0 Ω resistors R914 and R477 must be assembled.
4 To connect the JTAG interface with PCIe slot 2, the 0 Ω resistors R471 – R475 must be assembled.

3.3.2.2 FlexiFace® 1 (2 × gigabit Ethernet)

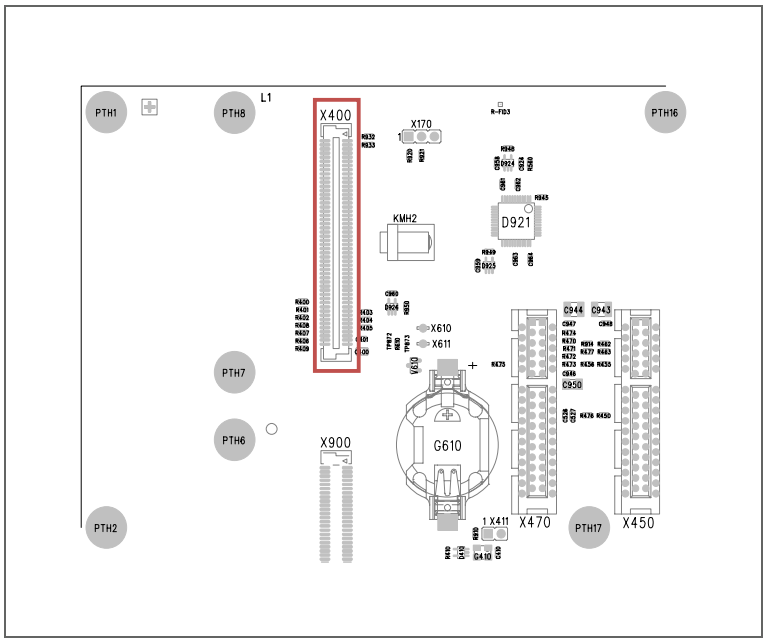
eTSEC1 and eTSEC3 of the P2020 are brought out to the FlexiFace® 1 slot (X400). If a suitable FlexiFace® board (TQF-P2020) is present in this slot, two more gigabit Ethernet interfaces can be used in addition to the on-board interface.

Illustration 24: FlexiFace® 1, schematic illustration



The following illustration shows the position of the FlexiFace® 1 - slot on the STKP2020:

Illustration 25: Position of FlexiFace® 1 - slot



The Media Independent Interface (MII) of eTSEC1 & 3 to FlexiFace® 1 are each implemented as RGMII.
Corresponding Phys, shielded RJ45 jacks with integrated transformers, as well as several diagnostic LEDs are available on the FlexiFace® board (TQF-P2020).
A more detailed description of the FlexiFace® board TQF-P2020 can be obtained from TQS-Support.

Interface:	eTSEC1 and eTSEC3 of the P2020
Configuration:	MDIO (Phy address of eTSEC1 is 0x15, Phy address of eTSEC3 is 0x16)
PHY interrupt:	IRQ1

The pinout of FlexiFace® 1 is as follows:

Table 31: Pinout of FlexiFace® 1 (X400)

Signal name	Pin	Pin	Signal name
EC_MDIO	1	2	IIC2_SDA
EC_MDC	3	4	IIC2_SCL
GND	5	6	GND
TSEC1_RXD0	7	8	TSEC1_GTX_CLK
TSEC1_RXD1	9	10	TSEC1_TX_EN
TSEC1_RX_CLK	11	12	GND
TSEC1_RXD2	13	14	TSEC1_TXD0
TSEC1_RXD3	15	16	TSEC1_TXD1
GND	17	18	NC
TSEC1_RX_DV	19	20	TSEC1_TXD2
NC	21	22	TSEC1_TXD3
NC	23	24	GND
NC	25	26	NC
NC	27	28	NC
GND	29	30	NC
NC	31	32	NC
NC	33	34	NC
NC	35	36	GND
NC	37	38	TSEC1_TXD4/TSEC3_TXD0
TSEC1_CRS/TSEC3_RX_DV	39	40	TSEC1_TXD5/TSEC3_TXD1
GND	41	42	NC
TSEC1_RXD4/TSEC3_RXD0	43	44	TSEC1_TXD6/TSEC3_TXD2
TSEC1_RXD5/TSEC3_RXD1	45	46	TSEC1_TXD7/TSEC3_TXD3
TSEC1_COL/TSEC3_RX_CLK	47	48	GND
TSEC1_RXD6/TSEC3_RXD2	49	50	TSEC2_TXD5/TSEC3_TX_EN
TSEC1_RXD7/TSEC3_RXD3	51	52	TSEC2_TXD4/TSEC3_GTX_CLK
GND	53	54	NC
NC	55	56	NC
NC	57	58	NC
NC	59	60	GND
NC	61	62	NC
NC	63	64	NC
GND	65	66	NC
NC	67	68	NC
NC	69	70	NC
NC	71	72	GND
NC	73	74	NC
NC	75	76	GND
GND	77	78	EC_GTX_CLK125_FF
NC	79	80	GND
NC	81	82	NC
STK_RES_2V5#	83	84	EEPROM A0
IRQ1	85	86	EEPROM A1
TRST_2V5 (optional)5	87	88	EEPROM A2
TMS_2V5 (optional)	89	90	TCK_2V5 (optional)
TDO_FF1_2V5 (optional)	91	92	TDO_PHY_2V5 (optional)
ENA_CLK125_FF#	93	94	VCC3V3
VCC3V3	95	96	VCC3V3
VCC3V3	97	98	VCC3V3
VCC3V3	99	100	VCC3V3

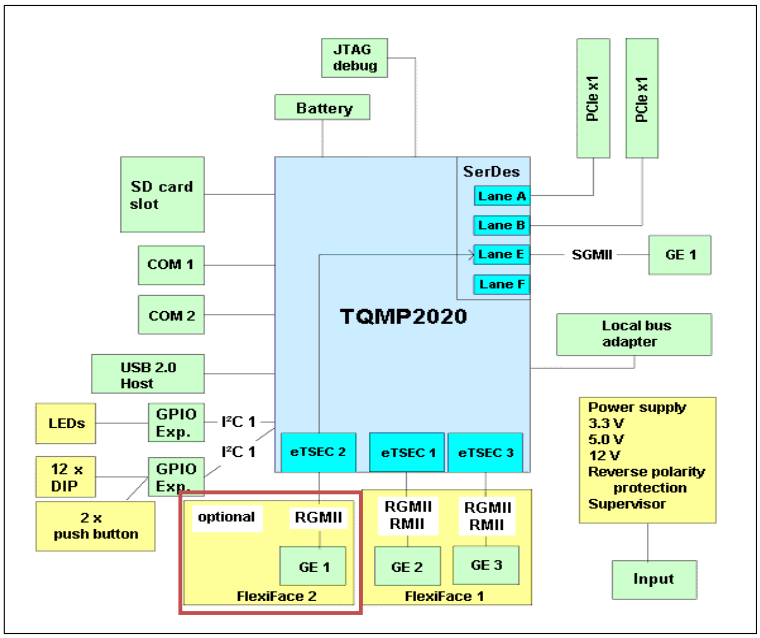
The FlexiFace® specific I^2C address for the EEPROM on the FlexiFace® is coded at pins 84, 86, and 88.
The interrupt line (IRQ1) on pin 85 is directly routed to the module.
The reset line (Pin83, STK_RES_2V5#) comes from the central reset generation.
The signal ENA_CLK125_FF# comes from a jumper on the FlexiFace® and causes the FlexiFace® to provide the Ethernet clock EC_GTX_CLK125_FF for the TQMP2020 and therefore all Ethernet interfaces on the STKP2020 (cf. section 3.3.3.3, Ethernet clock generation).
The unoccupied pins (87, 89 to 92) are used as JTAG test pins during production (see section 3.3.3.7, JTAG chain).

5 To connect the JTAG interface with the FlexiFace® 1, the 0 Ω resistors R403 – R408 must be assembled. More information can be found in section 3.3.3.7.

3.3.2.3 FlexiFace® 2 (1 × gigabit Ethernet)

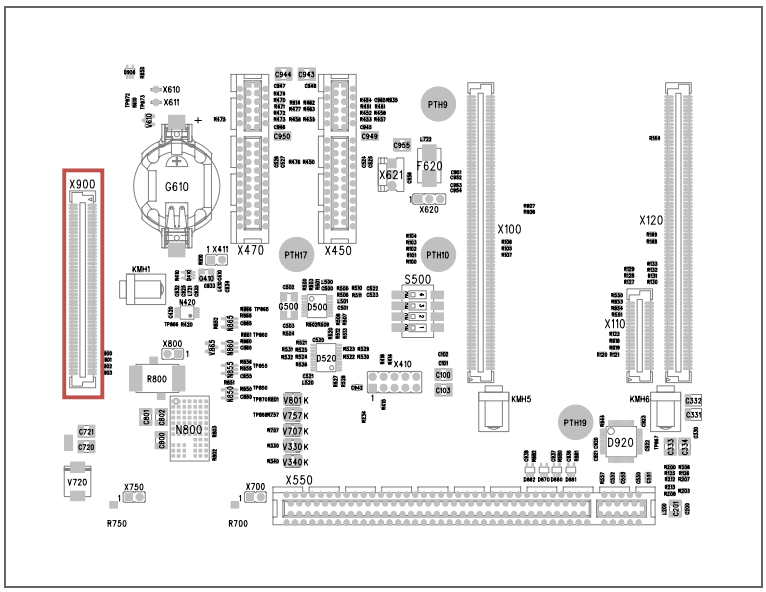
In the default configuration eTSEC2 is brought out via the on-board gigabit Ethernet interface (see section 3.3.1.4, On-board gigabit Ethernet). The eTSEC2 can also be brought out via FlexiFace® 2 (X900). The module has to be reconfigured for this. Details can be found in the User's Manual of the TQMP2020.
If a suitable FlexiFace® board (TQF-P2020) is plugged into slot (X900) after reconfiguration, eTSEC2 can be used as a gigabit Ethernet interface via FlexiFace® 2. The on-board gigabit Ethernet interface is then deactivated.

Illustration 26: FlexiFace® 2, schematic illustration



The following illustration shows the position of the FlexiFace® 2 - slot on the STKP2020:

Illustration 27: Position of FlexiFace® 2 slot



The Media Independent Interface (MII) from eTSEC2 to FlexiFace® 2 is implemented as RGMII.
Corresponding Phys, shielded RJ45 jacks with integrated transformers, as well as several diagnostic LEDs are available on the FlexiFace® board (TQF-P2020).
A more detailed description of the FlexiFace® board TQF-P2020 can be obtained from TQS-Support.

Interface:	eTSEC2 of the P2020
Configuration:	MDIO (Phy address of eTSEC2 is 0x11, Phy address of the unused Phy is 0x12)
PHY interrupt:	IRQ4

The pinout of FlexiFace® 2 is as follows:

Table 32: Pinout of FlexiFace® 2 (X900)

Signal name	Pin	Pin	Signal name
EC_MDIO	1	2	IIC2_SDA
EC_MDC	3	4	IIC2_SCL
GND	5	6	GND
TSEC2_RXD0	7	8	TSEC2_GTX_CLK
TSEC2_RXD1	9	10	TSEC2_TX_EN
TSEC2_RX_CLK	11	12	GND
TSEC2_RXD2	13	14	TSEC2_TXD0
TSEC2_RXD3	15	16	TSEC2_TXD1
GND	17	18	NC
TSEC2_RX_DV	19	20	TSEC2_TXD2
NC	21	22	TSEC2_TXD3
NC	23	24	GND
NC	25	26	NC
NC	27	28	NC
GND	29	30	NC
NC	31	32	NC
NC	33	34	NC
NC	35	36	GND
NC	37	38	NC
NC	39	40	NC
GND	41	42	NC
NC	43	44	NC
NC	45	46	NC
NC	47	48	GND
NC	49	50	NC
NC	51	52	NC
GND	53	54	NC
NC	55	56	NC
NC	57	58	NC
NC	59	60	GND
NC	61	62	NC
NC	63	64	NC
GND	65	66	NC
NC	67	68	NC
NC	69	70	NC
NC	71	72	GND
NC	73	74	NC
NC	75	76	GND
GND	77	78	NC
NC	79	80	GND
NC	81	82	NC
STK_RES_2V5#	83	84	EEPROM A0
IRQ4	85	86	EEPROM A1
TRST_2V5 (optional)[6]	87	88	EEPROM A2
TMS_2V5 (optional)	89	90	TCK_2V5 (optional)
TDO_FF2_2V5 (optional)	91	92	TDO_FF1_2V5 (optional)
NC	93	94	VCC3V3
VCC3V3	95	96	VCC3V3
VCC3V3	97	98	VCC3V3
VCC3V3	99	100	VCC3V3

The FlexiFace® specific I^2C address for the EEPROM on the FlexiFace® is coded at pins 84, 86, and 88.
The interrupt line (IRQ4) on pin 85 is directly routed to the module.
The reset line (Pin83, STK_RES_2V5#) comes from the central reset generation.
The unoccupied pins (87, 89 to 92) are used as JTAG test pins during production (see section 3.3.3.7, JTAG chain).

6 To connect the JTAG interface with the FlexiFace® 2, the 0 Ω resistors R900 – R905 must be assembled. More information can be found in section 3.3.3.7.

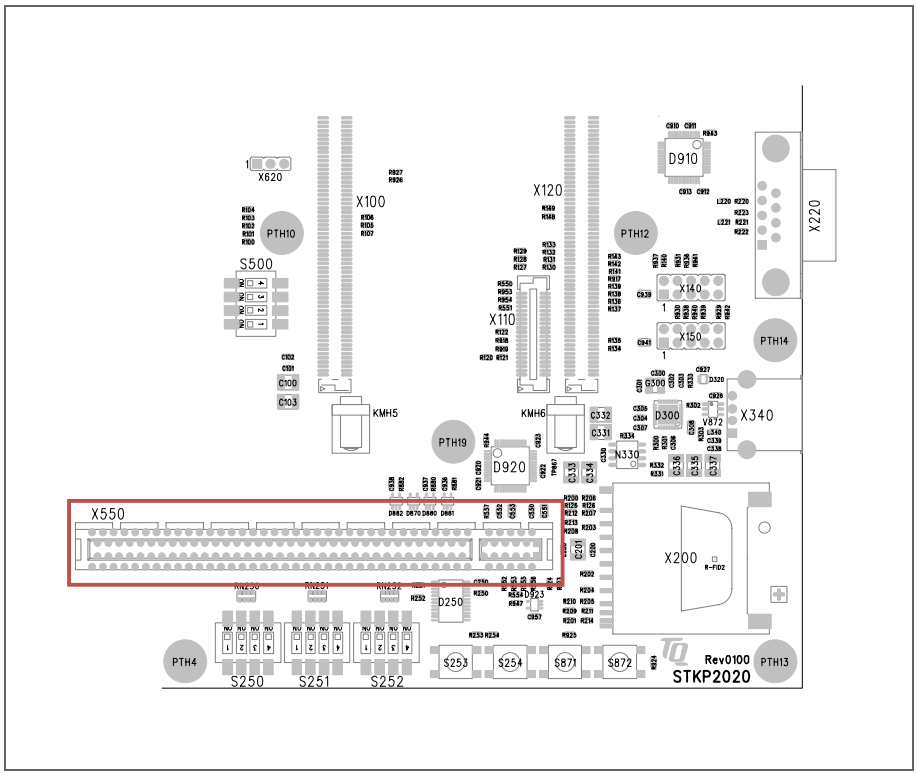
3.3.2.4 Local bus slot

The local bus of the processor P2020 is routed to a header (X550) on the STKP2020.
A converted PCIe ×16 slot is used as a plug connector.
Purpose of this "slot" is that users can develop an assembly and connect it easily to the local bus.

Routing guideline for baseboards	
	To guarantee the signal integrity and the timing ***on the module*** the following lengths of tracks and clock frequencies on the baseboard must be taken note of if an external bus subscriber is connected: • Length of track LALE on baseboard: maximum 45 mm • Length of track other local bus signals on baseboard: maximum 120 mm • CSB clock maximum: 400 MHz Timing on the baseboard: Compliance with the parameter t_LBONOT (address latch hold time) must be ensured. Therefore the run-times of the signals LALE and LAD[0:15] including possible reflexions have to be taken into account.

The following illustration shows the position of the local bus slot on the STKP2020:

Illustration 28: Position of local bus slot



The pinout of the local bus slot is as follows:

Table 33: Pinout of local bus slot (X550)

X550			
Signal	Pin	Pin	Signal
VCC5V	B1	A1	VCC5V
VCC5V	B2	A2	VCC5V
VCC5V	B3	A3	VCC5V
GND	B4	A4	GND
IIC1_SCL	B5	A5	TCK (optional)[7]
IIC1_SDA	B6	A6	TDI (optional)
GND	B7	A7	TDO (optional)
VCC3V3	B8	A8	TMS (optional)
TRST (optional)	B9	A9	VCC3V3
VCC3V3	B10	A10	VCC3V3
VCC3V3	B11	A11	STK_RES#
Key notch			
GND	B12	A12	GND
LAD0	B13	A13	LA16
LAD1	B14	A14	LA17
GND	B15	A15	LA18
LAD2	B16	A16	LA19
LAD3	B17	A17	LA20
LAD4	B18	A18	GND
LAD5	B19	A19	LA21
LAD6	B20	A20	LA22
GND	B21	A21	LA23
LAD7	B22	A22	LA24
LAD8	B23	A23	LA25
LAD9	B24	A24	GND
LAD10	B25	A25	LA26
LAD11	B26	A26	LA27
GND	B27	A27	LA28
LAD12	B28	A28	LA29
LAD13	B29	A29	LA30
LAD14	B30	A30	GND
LAD15	B31	A31	LA31
LDP0	B32	A32	NC
GND	B33	A33	NC
LDP1	B34	A34	LALE
LBCTL	B35	A35	LWE0#/LFWE#/LBS#
NC	B36	A36	GND
NC	B37	A37	LWE1#/LBS1#
NC	B38	A38	NC
GND	B39	A39	NC
NC	B40	A40	LGPL0/LFCLE
NC	B41	A41	LGPL1/LFALE
LCS0#/CS_NOR#	B42	A42	GND

7 To connect the JTAG interface with the local bus slot, the 0 Ω resistors R552 – R557 must be assembled. More information can be found in section 3.3.3.7.

Table 33: Pinout of local bus slot (X550) (continued)

X550			
Signal	Pin	Pin	Signal
LCS1#	B43	A43	LGPL2/FREQ#/LOE#
LCS2#	B44	A44	LGPL3/LFWP#
GND	B45	A45	LGPL4/LGTA#/LFRB/LUPWAIT/LPBSE
LCS3#	B46	A46	LGPL5
GND	B47	A47	GND
LCLK0	B48	A48	LSYNC_IN_LBA
GND	B49	A49	LSYNC_OUT_LBA
CLKOE	B50	A50	LCLK1
GND	B51	A51	GND
SYSCLK_CPU	B52	A52	IRQ0
GND	B53	A53	IRQ1
DDRCLK_CPU	B54	A54	IRQ2
GND	B55	A55	IRQ3
DMA1_DREQ#	B56	A56	IRQ4
DMA1_DACK#	B57	A57	IRQ5
DMA1_DDONE#	B58	A58	GND
UDE0#	B59	A59	DMA2_DREQ0#
MCP0#	B60	A60	DMA2_DACK0#
GND	B61	A61	DMA2_DDONE0#
IRQ6	B62	A62	LCS5#/ DMA2_DREQ1#
GPIO_0/IRQ7	B63	A63	LCS6#/ DMA2_DACK1#
GPIO_1/IRQ8	B64	A64	GND
GPIO_2/IRQ9	B65	A65	LCS7#/ DMA2_DDONE1#
GPIO_3/IRQ10	B66	A66	TRIG_OUT/READY_P0/QUIESCE#
GPIO_4/IRQ11	B67	A67	TRIG_IN
GND	B68	A68	MDVAL
MSRCID0	B69	A69	LCS4#
MSRCID1	B70	A70	GND
MSRCID2	B71	A71	NC
MSRCID3	B72	A72	SCAN_MODE#
MSRCID4	B73	A73	TEST_SEL#
NC	B74	A74	ASLEEP
GND	B75	A75	GND
IRQ_OUT#	B76	A76	CLK_OUT
RTC_INT#	B77	A77	RTC
TEMP_OS#	B78	A78	READY_P1
NC	B79	A79	MCP1#
GND	B80	A80	UDE1#
GND	B81	A81	GND
GND	B82	A82	GND

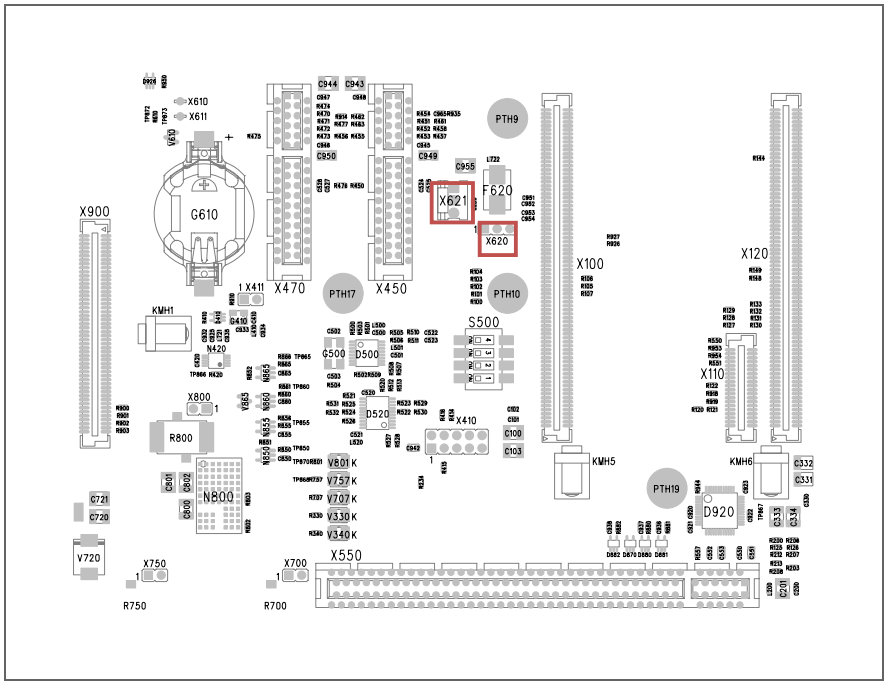
With synchronous local bus designs it can be necessary to open the loop of LSYNC_OUT to LSYNC_IN located on the STKP2020 and to implement the loop on the plug-in card. Therefore the resistors R550 and R551 must be removed and the resistors R953 and R954 must be assembled on the STKP2020.
Mechanically the local bus connector corresponds to a PCIe ×16 slot.
The position in the middle of the STKP2020 should prevent PCIe ×16 cards to be plugged in.

3.3.2.5 Fan connector

The STKP2020 provides a fan connector (X621) as it can be found in PC systems to cool the module or other assemblies. Depending on the position of the jumper X620 the fan is supplied with 5 V or 12 V.

The following illustration shows the position of the fan connector (X621) as well as the affiliated jumper (X620) on the STKP2020:

Illustration 29: Position of fan connector and jumper



The configuration of the fan connector is as follows:

Table 34: Pinout of fan connector (X621)

Pin	Signal	Description
1	GND	Digital ground
2	FAN VOLTAGE	Fan voltage according to jumper X620
3	NC	Not connected

Table 35: Pinout of jumper fan voltage (X620)

Pin	Signal	Description
1	VCC5V	5 V
2	FAN VOLTAGE	Fan voltage
3	VCC12V	12 V

If pin 1 and 2 are bridged with a jumper, the fan is supplied with 5 V.
If pin 2 and 3 are bridged with a jumper, the fan is supplied with 12 V.

Table 36: Used type of connector (fan connector)

Manufacturer / type	Description
TE Connectivity /	Friction lock, 3-pin

Table 37: Used type of connector (Jumper fan voltage header)

Manufacturer / type	Description
Pin header	Single row, 2.54 mm pitch, 3-pin

The fan connector is equipped with an electronic, self-resetting fuse (F620, 1.1 A).

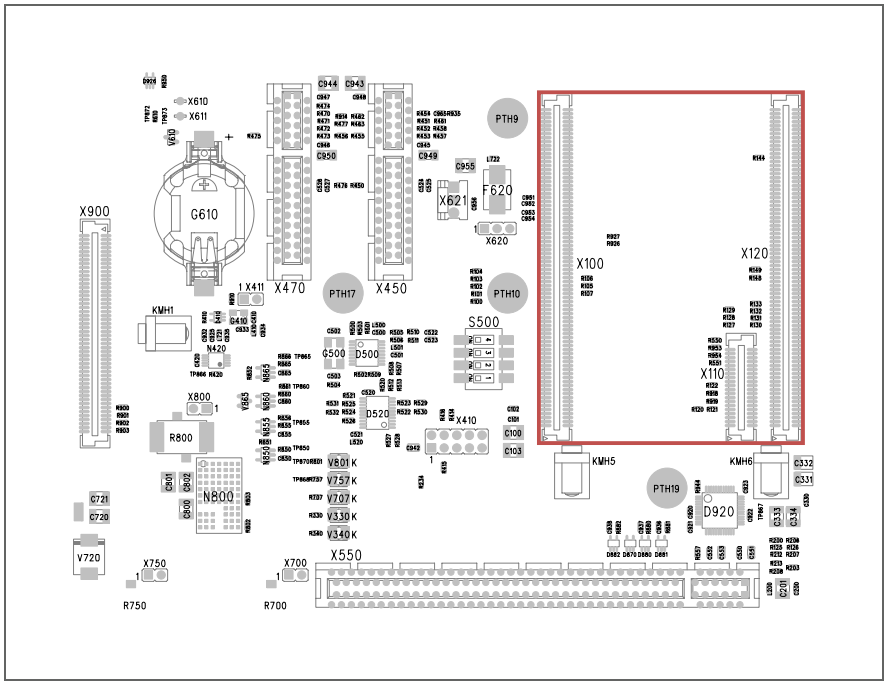
3.3.3 System components

3.3.3.1 Processor board TQMP2020

The STKP2020 serves as a Starterkit for the processor module TQMP2020.
The TQMP2020 is plugged on the plug connectors X100, X110 and X120.

The following illustration shows the position of the plug connectors (X100, X110, and X120) for the TQMP2020 on the STKP2020:

Illustration 30: Position of plug connectors for TQMP2020



The following tables show the routing of the single signals between STKP2020 and TQMP2020:[8]

Table 38: Pinout of TQMP2020 module connector (X100)

Group	Signal name	Pin No.		Signal name	Group
Power	VCC3V3	1	2	VCC3V3	Power
	VCC3V3	3	4	VCC3V3	
	VCC3V3	5	6	VCC3V3	
	VCC3V3	7	8	VCC3V3	
	VCC3V3	9	10	VBAT	
	VCC3V3	11	12	TSEC2_RXD0	Ethernet
Ethernet	TSEC1_RXD0	13	14	TSEC2_RXD1	
	TSEC1_RXD1	15	16	TSEC2_RXD2	
	TSEC1_RXD2	17	18	TSEC2_RXD3	
	TSEC1_RXD3	19	20	GND	Power
	TSEC1_RXD4/ TSEC3_RXD0	21	22	TSEC2_RXD4	Ethernet
	TSEC1_RXD5/ TSEC3_RXD1	23	24	TSEC2_RXD5	
	TSEC1_RXD6/ TSEC3_RXD2	25	26	TSEC2_RXD6	
Power	GND	27	28	TSEC2_RXD7	
Ethernet	TSEC1_RXD7/ TSEC3_RXD3	29	30	TSEC2_RX_DV	
	TSEC1_RX_DV	31	32	TSEC2_RX_ER	
	TSEC1_RX_ER	33	34	TSEC2_RX_CLK	
	TSEC1_RX_CLK	35	36	GND	Power
	TSEC1_TXD0	37	38	TSEC2_TXD0	Ethernet
	TSEC1_TXD1	39	40	TSEC2_TXD1	
	TSEC1_TXD2	41	42	TSEC2_TXD2	
Power	GND	43	44	TSEC2_TXD3	
Ethernet	TSEC1_TXD3	45	46	TSEC2_TXD4/ TSEC3_GTX_CLK	
	TSEC1_TXD4/ TSEC3_TXD0	47	48	TSEC2_TXD5/ TSEC3_TX_EN	
	TSEC1_TXD5/ TSEC3_TXD1	49	50	TSEC2_TXD6	
	TSEC1_TXD6/ TSEC3_TXD2	51	52	GND	Power
	TSEC1_TXD7/ TSEC3_TXD3	53	54	TSEC2_TXD7	Ethernet
	TSEC1_TX_EN	55	56	TSEC2_TX_EN	
	TSEC1_TX_ER	57	58	TSEC2_TX_ER	
Power	GND	59	60	TSEC2_TX_CLK	
Ethernet	TSEC1_TX_CLK	61	62	TSEC2_GTX_CLK	
	TSEC1_GTX_CLK	63	64	TSEC2_CRS/TSEC3_RX_ER	
	TSEC1_CRS/ TSEC3_RX_DV	65	66	TSEC2_COL/TSEC3_TX_CLK	
	TSEC1_COL TSEC3_RX_CLK	67	68	GND	Power
	TSEC_1588_CLK_IN	69	70	TSEC_1588_CLK_OUT	Ethernet
	TSEC_1588_TRIG_IN1	71	72	TSEC_1588_PULSE_OUT1	
	TSEC_1588_TRIG_IN2	73	74	TSEC_1588_PULSE_OUT2	
Power	GND	75	76	EC_MDC	
Ethernet	TSEC_1588_ALARM_OUT1	77	78	EC_MDIO	
	TSEC_1588_ALARM_OUT2	79	80	EC_GTX_CLK125	
NC	NC (RSVD4080/EMI2_MDC)	81	82	ASLEEP	Control
	NC (RSVD4080/EMI2_MDIO)	83	84	GND	Power
Power	GND	85	86	SD_REF_CLK	SerDes
	GND	87	88	SD_REF_CLK#	
NC	NC (SD_TX3)	89	90	GND	Power
	NC (SD_TX3#)	91	92	GND	
Power	GND	93	94	NC (SD_RX3)	NC
	GND	95	96	NC (SD_RX3#)	
SGMII	SD_TX2	97	98	GND	Power
	SD_TX2#	99	100	GND	
Power	GND	101	102	SD_RX2	SGMII
	GND	103	104	SD_RX2#	

8 Signals in parentheses are not connected with the TQMP2020 and STKP2020 but, however, give the configuration for future module versions.

Table 38: Pinout of TQMP2020 module connector (X100) (continued)

Group	Signal name	Pin No.		Signal name	Group
PCIe Slot 2	SD_TX1	105	106	GND	Power
	SD_TX1#	107	108	GND	
Power	GND	109	110	SD_RX1	PCIe Slot 2
	GND	111	112	SD_RX1#	
PCIe Slot 1	SD_TX0	113	114	GND	Power
	SD_TX0#	115	116	GND	
Power	GND	117	118	SD_RX0	PCIe Slot 1
	GND	119	120	SD_RX0#	
NC	NC (RSVD1022/SD2_REF_CLK)	121	122	GND	Power
	NC (RSVD1022/SD2_REF_CLK#)	123	124	GND	
Power	GND	125	126	NC (RSVD1022/SD2_RX1)	NC
	GND	127	128	NC (RSVD1022/SD2_RX1#)	
NC	NC (RSVD1022/SD2_TX1)	129	130	GND	Power
	NC (RSVD1022/SD2_TX1#)	131	132	GND	
Power	GND	133	134	NC (RSVD1022/SD2_RX0)	NC
	GND	135	136	NC (RSVD1022/SD2_RX0#)	
NC	NC (RSVD1022/SD2_TX0)	137	138	GND	Power
	NC (RSVD1022/SD2_TX0#)	139	140	GND	
Power	GND	141	142	NC (RSVD4080/SD_2)	NC
	GND	143	144	NC (RSVD4080/SD_2#)	
NC	NC (RSVD4080/SD_0)	145	146	GND	Power
	NC (RSVD4080/SD_0#)	147	148	GND	
Power	GND	149	150	NC (RSVD4080/SD_3)	NC
	GND	151	152	NC (RSVD4080/SD_3#)	
NC	NC (RSVD4080/SD_1)	153	154	GND	Power
	NC (RSVD4080/SD_1#)	155	156	GND	
Power	GND	157	158	PGOOD	Control
NC	NC (RSVD1022/POWER_OK/GPIO3_19)	159	160	NC (RSVD1022/POWER_EN)	NC

Table 39: Pinout of TQMP2020 module connector (X120)

Group	Signal name	Pin No.		Signal name	Group
Power	3V3[9]	1	2	GPIO_0/IRQ7	GPIO
	CVDD	3	4	GPIO_1/IRQ8	
	LVDD	5	6	GPIO_2/IRQ9	
	2V5	7	8	GND	Power
	1V8	9	10	GPIO_3/IRQ10	GPIO
GPIO	GPIO_5	11	12	GPIO_4/IRQ11	
	GPIO_7	13	14	GPIO_6	
Power	GND	15	16	GPIO_8/SDHC_CD#	
GPIO	GPIO_9/SDHC_WP	17	18	GPIO_10/USB_PCTL0	
	GPIO_11/USB_PCTL1	19	20	GPIO_12	
	GPIO_13	21	22	GPIO_14	
	GPIO_15	23	24	GND	Power
SPI	SPI_MISO	25	26	SPI_CS0#/SDHC_DATA4	SPI
	SPI_MOSI	27	28	SPI_CS1#/SDHC_DATA5	
	SPI_CLK	29	30	SPI_CS2#/SDHC_DATA6	
Power	GND	31	32	SPI_CS3#/SDHC_DATA7	
SDHC	SDHC_DATA0	33	34	NC (RSVD1022/SDHC_CD)	NC
	SDHC_DATA1	35	36	SDHC_CMD	SDHC
	SDHC_DATA2	37	38	SDHC_CLK	
	SDHC_DATA3	39	40	GND	Power

9 The three voltages at the pins 1, 7 and 9 are brought out from the module. They are connected with CVDD and LVDD in such a way that the interfaces USB, SPI, SD card and Ethernet each run with the correct voltage. This existing circuitry on the STKP2020 should not be altered.

Table 39: Pinout of TQMP2020 module connector (X120) (continued)

Group	Signal name	Pin No.		Signal name	Group
USB	USB_NXT	41	42	NC (RSVD1022/SDHC_WP)	NC
	USB_DIR	43	44	USB_STP	USB
	USB_CLK	45	46	USB_PWRFAULT	
Power	GND	47	48	USB_D0	
USB	USB_D1	49	50	USB_D2	
	USB_D3	51	52	USB_D4	
	USB_D5	53	54	USB_D6	
	USB_D7	55	56	GND	Power
Local bus	LWE0#/LFWE#/LBS#	57	58	LCLK0	Local bus
	LCS7#/DMA2_DDONE1#	59	60	LAD0	
	LGPL4/LGTA#/LFRB/LUPWAIT/LPBSE	61	62	LAD1	
Power	GND	63	64	LAD2	
Local bus	LALE	65	66	LAD3	
	LBCTL	67	68	LAD4	
	LAD6	69	70	LAD5	
	LAD7	71	72	GND	Power
	LA24	73	74	LA25	Local bus
Control	DDRCLK_CPU	75	76	LA26	
Power	GND	77	78	LA27	
Control	SYSCLK_CPU	79	80	LA28	
	CLK_OUT	81	82	LA29	
Power	GND	83	84	LA30	
Control	RTC	85	86	LA31	
	MSRID0	87	88	MDVAL	Control
	MSRID1	89	90	GND	Power
	MSRID2	91	92	SCAN_MODE#	Control
	MSRID3	93	94	TEST_SEL#	
	MSRID4	95	96	TQM_TDI	JTAG
Power	GND	97	98	TQM_TDO	
Control	TRIG_IN	99	100	TQM_TMS	
	TRIG_OUT/READY_P0/QUIESCE#	101	102	TQM_TCK	
	READY_P1	103	104	TQM_TRST#	
Control	MCP0#	105	106	GND	Power
	MCP1#	107	108	DMA1_DREQ#	Control
	UDE0#	109	110	DMA1_DACK#	
	UDE1#	111	112	DMA1_DDONE#	
Power	GND	113	114	DMA2_DREQ0#	
Control	IRQ0	115	116	DMA2_DACK0#	
	IRQ1	117	118	DMA2_DDONE0#	
	IRQ2	119	120	IRQ_OUT#	
	IRQ3	121	122	GND	Power
	IRQ4	123	124	NC (RSVD1022/IRQ7)	NC
	IRQ5	125	126	NC (RSVD1022/IRQ8)	
	IRQ6	127	128	NC (RSVD1022/IRQ9)	
Power	GND	129	130	NC (RSVD1022/IRQ10)	
I^2C	IIC1_SCL	131	132	IIC2_SCL	I^2C
	IIC1_SDA	133	134	IIC2_SDA	
JTAG	TQM_CKSTP_IN0#	135	136	TQM_CHKSTP_IN1#	JTAG

Table 39: Pinout of TQMP2020 module connector (X120) (continued)

Group	Signal name	Pin No.		Signal name	Group
Control	HRESET#	137	138	GND	Power
	HRESET_REQ#	139	140	TQM_CHKSTP_OUT1#	JTAG
	SRESET#	141	142	TQM_CHKSTP_OUT0#	
	RESIN#	143	144	CLKOE	Control
Power	GND	145	146	TEMP_OS#	
UART	SIN0	147	148	RTC_INT#	
	SOUT0	149	150	SIN1	UART
	UART_SIN0#	151	152	SOUT1	
	UART_SOUT0#	153	154	GND	Power
	UART_RTS0#	155	156	UART_CTS1#	UART
	UART_CTS0#	157	158	UART_RTS1#	
	UART_SIN1#	159	160	UART_SOUT1#	

Table 40: Pinout of TQMP2020 module connector (X110)

Group	Signal name	Pin No.		Signal name	Group
NC	NC (RSVD1022/IRQ11)	1	2	LWE1#/LBS1#	Local bus
Power	GND	3	4	LCS5#/DMA2_DREQ1#	
Local bus	LGPL0/LFCLE	5	6	LCS6#/DMA2_DACK1#	
	LGPL1/LFALE	7	8	LDP0	
	LGPL2/LFRE#/LOE#	9	10	LDP1	
	LGPL3/LFWP#	11	12	GND	Power
	LGPL5	13	14	LAD8	Local bus
	LCS0#/CS_NOR#	15	16	LAD9	
	LCS1#	17	18	LAD10	
Power	GND	19	20	LAD11	
Local bus	LCS2#	21	22	LAD12	
	LCS3#	23	24	LAD13	
	LCS4#	25	26	LAD14	
	LA23	27	28	GND	Power
	LA22	29	30	LAD15	Local bus
	LA21	31	32	LA16	
	LCLK1	33	34	LA17	
Power	GND	35	36	LA18	
Local bus	LSYNC_IN	37	38	LA19	
	LSYNC_OUT	39	40	LA20	

Table 41: Used parts (connectors to the processor board)

Manufacturer / type	Description
1 × tyco / 5177986-1	Board-to-board plug connector, 40-pin, 5 mm height
2 × tyco / 5177986-8	Board-to-board plug connector, 160-pin, 5 mm height

Details of the module TQMP2020 can be found in the User's Manual of the TQMP2020.

3.3.3.2 SERDES clock generation

The STKP2020 provides a circuit, which generates a reference clock for the SERDES interfaces of the TQMP2020. This reference clock is routed to both PCIe slots.

The SERDES interface of the TQMP2020 can be supplied with different clock frequencies. To improve EMC characteristics the clock can additionally be spread (spread spectrum).

These parameters can be set with DIP switch S500.

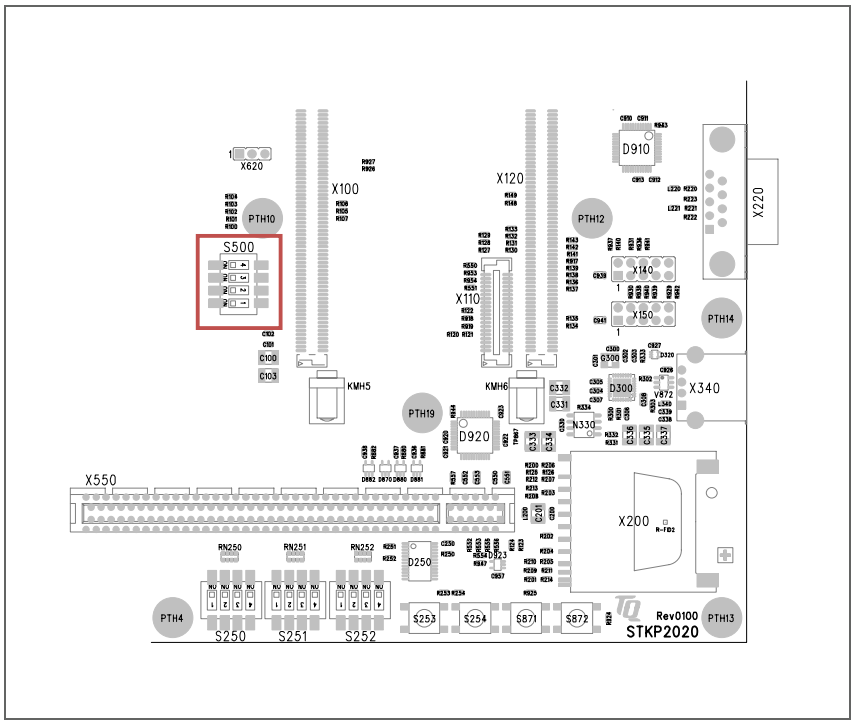
It depends on the protocols with which the single SERDES lanes operate, which reference clock the TQMP2020 requires for its SERDES interfaces.

Table 42: SERDES reference frequency per protocol

Reference frequency	Protocol
100 MHz	PCIe (2.5 Gbps)
100 MHz or 125 MHz	Serial Rapid I/O (1.25 Gbps or 2.5 Gbps), SGMII (1.25 Gbps)
125 MHz	Serial Rapid I/O (3.125 Gbps)

The following illustration shows the position of DIP switch S500 to parameterise the SERDES clock on the STKP2020:

Illustration 31: Position of DIP switch for SERDES clock parametrisation



The following tables show the configuration possibilities with the SERDES clock to parametrisation:

Table 43: Configuration of SERDES clock frequency

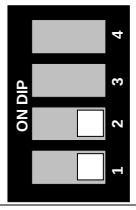
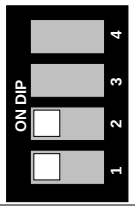
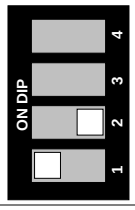
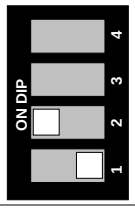
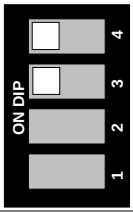
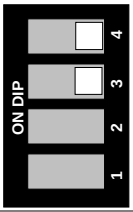
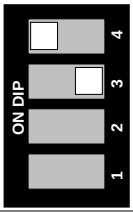
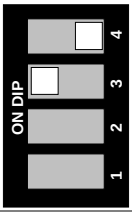
SERDES clock 100 MHz	SERDES clock 125 MHz	SERDES clock 25 MHz (not used)	SERDES clock 200 MHz (not used)
			

Table 44: Configuration of SERDES clock spread spectrum

No spread	Center ±0.25	Down –0.5	Down –0.75
			

For more information about the configuration of the SERDES clock see table 4.15 in the P2020 Reference Manual P2020RM.

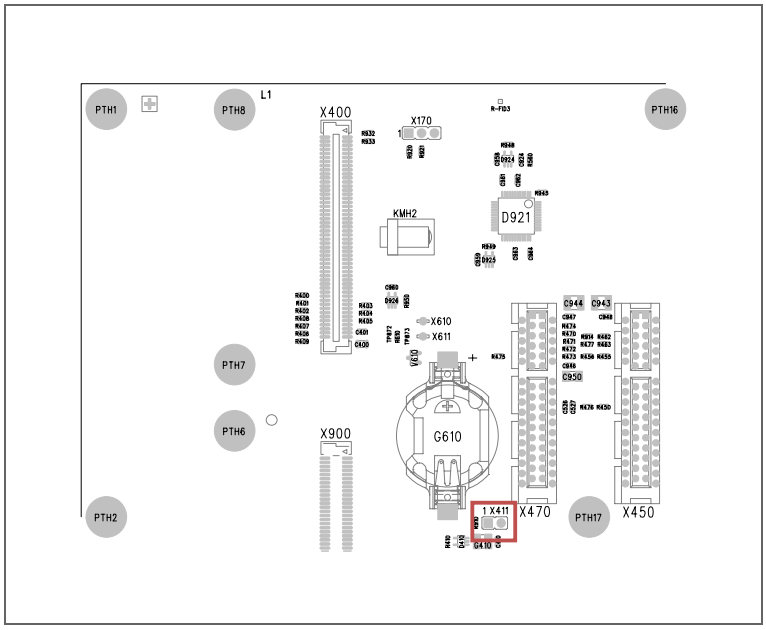
3.3.3.3 Ethernet clock generation

The Ethernet clock frequency between processor/MAC and the Phys (on-board and FlexiFaces®) is 125 MHz on all interfaces. This clock can be supplied by different sources:

- FlexiFace® 1
  Condition: Jumper on FlexiFace® closed, jumper X411 closed
- On-board gigabit Ethernet Phy (D350)
  Condition: Jumper on FlexiFace® open, jumper X411 closed
- Oscillator (G410)
  Condition: Jumper on FlexiFace® open, jumper X411 open

The following illustration shows the position of jumper X411 for Ethernet clock selection on the STKP2020:

Illustration 32: Position of jumper for Ethernet clock selection

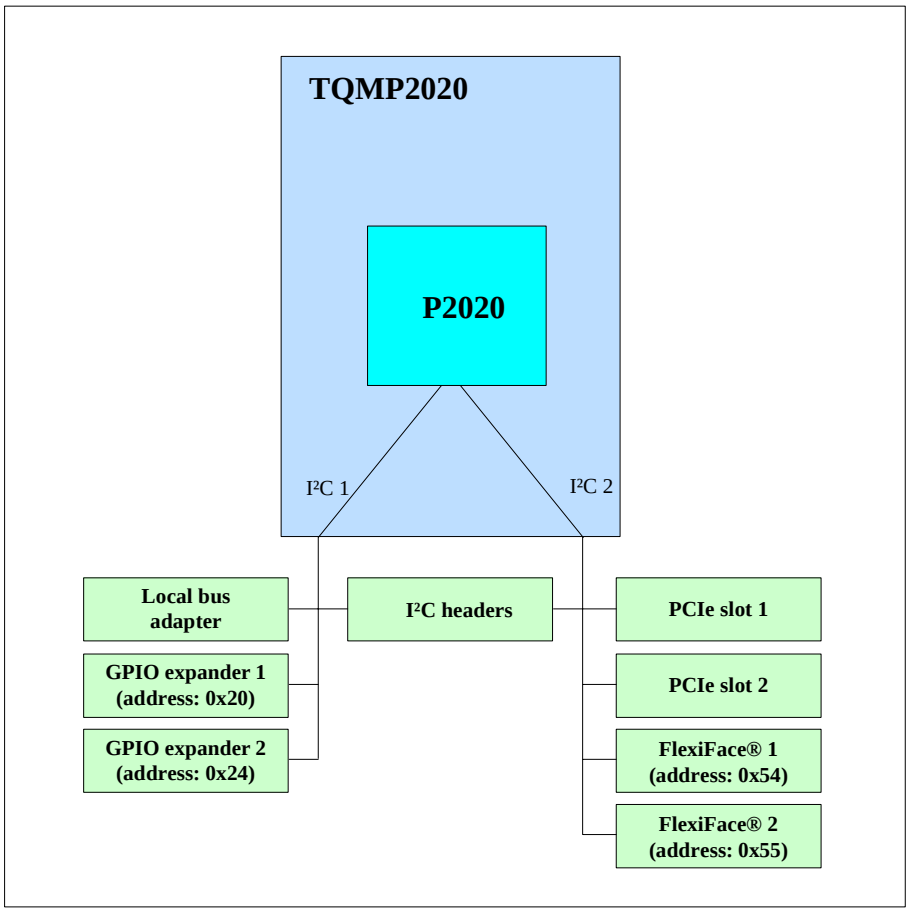


3.3.3.4 I²C-bus

The processor P2020 provides two I²C-buses. Both buses are routed to the STKP2020.

The following illustration provides an overview of the wiring of both buses:

Illustration 33: Wiring of I²C buses



The pinout of the I²C headers is shown in section 3.3.1.13, I²C.

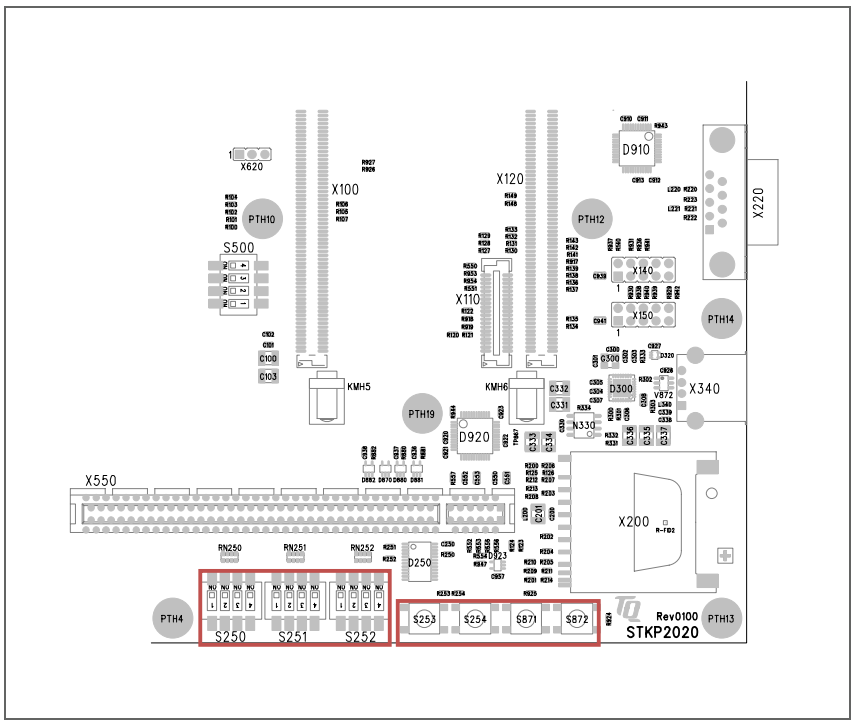
The functions of the I²C I/O expanders are described in the following two sections.

3.3.3.5 I²C I/O expander 1 (DIP switches, push-buttons)

The STKP2020 provides three 4-fold DIP switch (S250, S251, S252) and four push-buttons (S253, S254, S871, S872) for user's inputs. Their state can be read out with a 16-channel I²C I/O expander (D250).
It is selected via I²C (address 0x20).

The following illustration shows the position of the DIP switches and push-buttons on the STKP2020:

Illustration 34: Position of DIP switches and push-buttons



Both 8-bit I/O ports are wired as follows:

Table 45: Assignment of I²C I/O expander 1 to DIP switches and push-buttons

IO0 0 … 7							
IO0_0	IO0_1	IO0_2	IO0_3	IO0_4	IO0_5	IO0_6	IO0_7
S250/1	S250/2	S250/3	S250/4	S251/1	S251/2	S251/3	S251/4
IO1 0 … 7							
IO1_0	IO1_1	IO1_2	IO1_3	IO1_4	IO1_5	IO1_6	IO1_7
S252/1	S252/2	S252/3	S252/4	S253	S254	S871	S872

DIP switch position OFF = input logic '1', position ON = input logic '0'.
Button not pressed = input logic '1', pressed = input logic '0'.

Furthermore the GPIO expander provides an interrupt output, which is connected to IRQ2 of the P2020.
By this the I²C I/O expander can signal changes at one of the inputs to the processor.

Interface: I²C 1 of the P2020
I²C address: 0x20 (0100000)
Interrupt: IRQ2

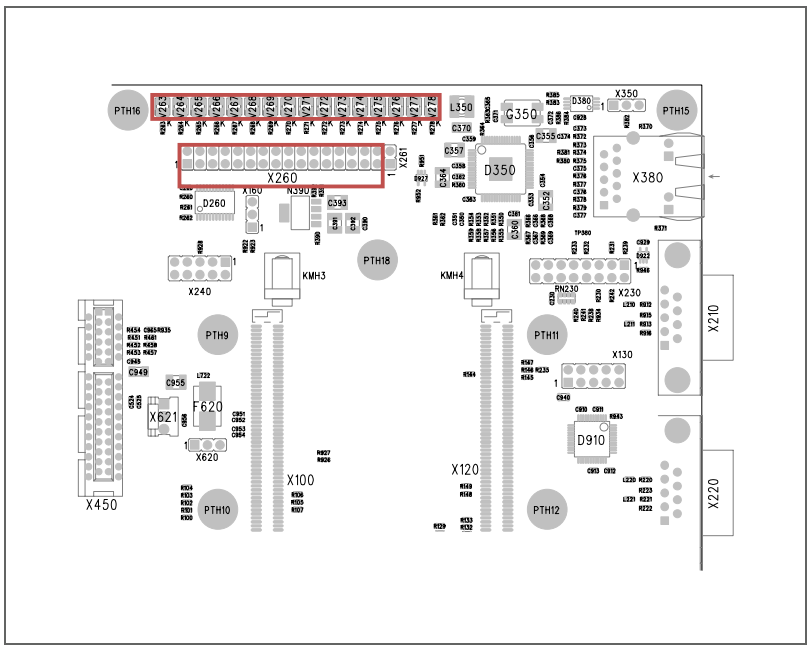
Attention: destruction or malfunction!	
	After a reset all port I/O pins are configured as input. This should be maintained, as the outputs of the device can be destroyed if a DIP switch is set to ON or if a push-button is pressed (output solidly connected to GND)!

3.3.3.6 I²C I/O expander 2 (LEDs)

A 16-channel I²C I/O expander (D260) serves to display the operational conditions of the module. The 16-channel I²C I/O expander can drive up to 16 LEDs. It is selected via I²C (address 0x24). Header X260 must be bridged with 16 jumpers to enable the LEDs to light up. Please note, that the two pins on the very right must not be bridged, as these lead VCC3V3 and GND.

The following illustration shows the position of the LEDs and jumpers on the STKP2020:

Illustration 35: Position of user LEDs and jumpers



Both 8-bit I/O ports are wired as follows:

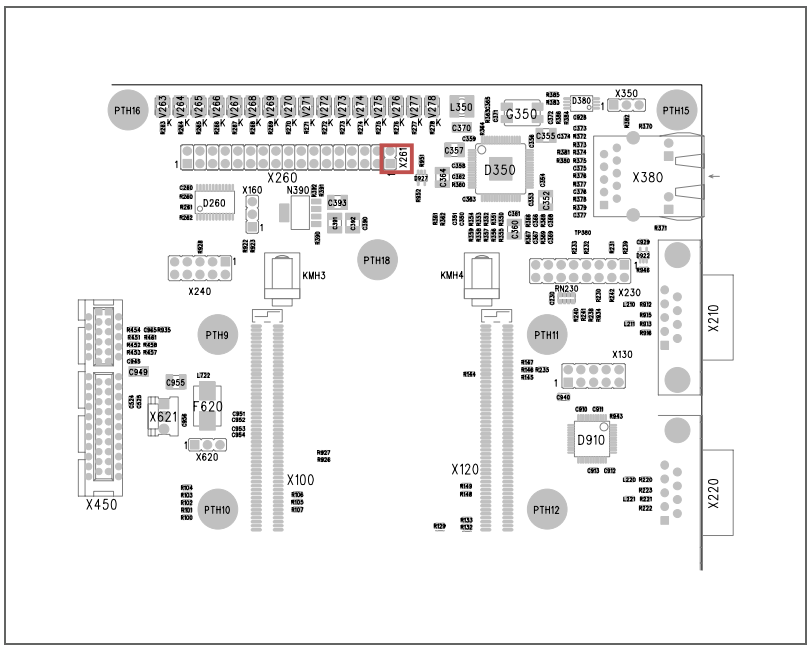
Table 46: Assignment of I²C I/O expander 2 to LEDs

LED0 … 7							
IO0_0	IO0_1	IO0_2	IO0_3	IO0_4	IO0_5	IO0_6	IO0_7
V263	V264	V265	V266	V267	V268	V269	V270
LED8 … 15							
IO1_0	IO1_1	IO1_2	IO1_3	IO1_4	IO1_5	IO1_6	IO1_7
V271	V272	V273	V274	V275	V276	V277	V278

LED output high = LED off, output low = LED on (open drain)

Optionally the jumpers for the LEDs can also be used as a plug connector to route out GPIOs.
An extension board can be plugged on and the 16-channel I²C LED driver can serve as a GPIO device.
Two more pins (X261) with 3.3 V and GND are placed directly next to the LED jumpers for this.
(See Illustration 35 and Illustration 36).

Illustration 36: Position of X621 for extension board GPIO



After a reset all port I/O pins are configured as input.
To activate the LEDs, they must be configured as output and then set to LOW.

Furthermore the GPIO expander provides an interrupt output, which is connected to IRQ2 of the P2020.
By this the I^2C I/O expander can signal changes at one of the inputs to the processor.

Interface:	I^2C 1 of the P2020
I^2C address:	0x24 (0100100)
Interrupt:	IRQ2

Table 47: Pinout of LED jumper header (X260)

Signal	Pin	Pin	Signal
IO0_0	1	2	LED V263
IO0_1	3	4	LED V264
IO0_2	5	6	LED V265
IO0_3	7	8	LED V266
IO0_4	9	10	LED V267
IO0_5	11	12	LED V268
IO0_6	13	14	LED V269
IO0_7	15	16	LED V270
IO1_0	17	18	LED V271
IO1_1	19	20	LED V272
IO1_2	21	22	LED V273
IO1_3	23	24	LED V274
IO1_4	25	26	LED V275
IO1_5	27	28	LED V276
IO1_6	29	30	LED V277
IO1_7	31	32	LED V278

Table 48: Pinout of additional header for extension board (X261)

Signal	Pin	Pin	Signal
GND	1	2	VCC3V3

Table 49: Used type of connector (LED jumper header)

Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 32-pin

Table 50: Used type of connector (additional header for extension board)

Manufacturer / type	Description
Pin header	Single row, 2.54 mm pitch, 2-pin

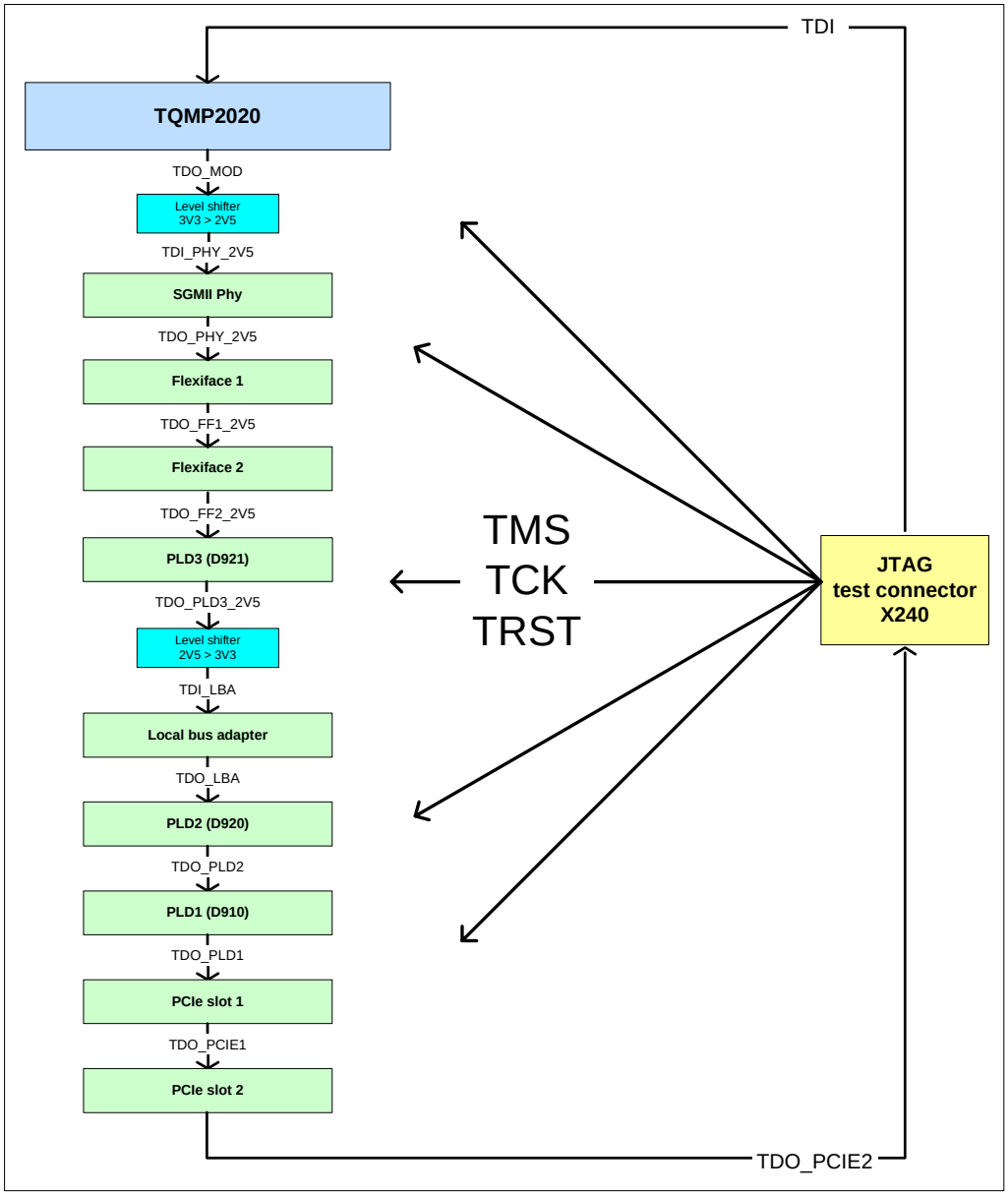
3.3.3.7 JTAG chain

To allow a production test, all JTAG capable devices are connected in a chain (JTAG chain).
This permits an automated test, whether the pins of the components are connected correctly or not.

Via the JTAG test connector X240 the JTAG chain is externally accessible.

The following illustration shows the JTAG chain architecture:

Illustration 37: Architecture of JTAG chain



The following illustration shows the position of the JTAG test connector X240 on the STKP2020:

Illustration 38: Position of JTAG test connector

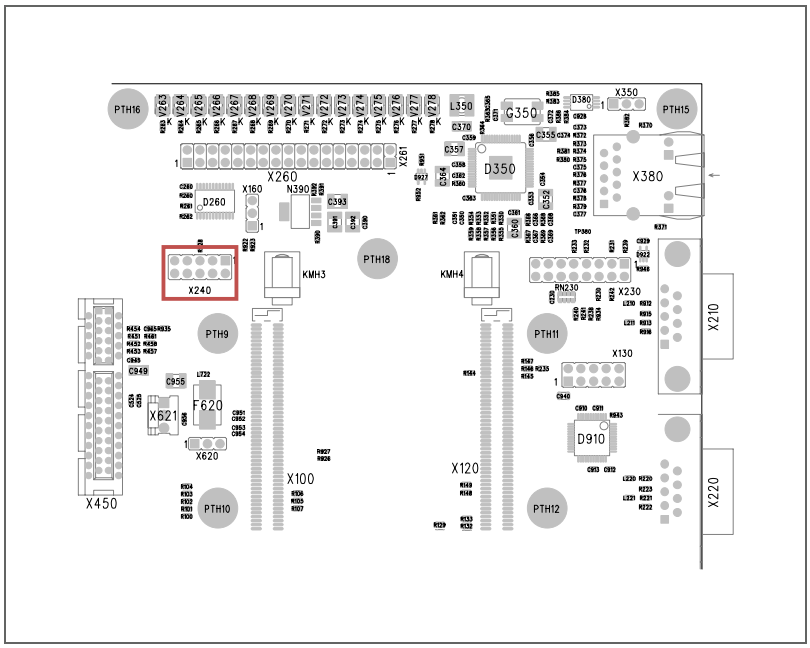


Table 51: Pinout of JTAG test connector (X240)

Pin	Signal	Type	Description
1	TCK	IN	JTAG test clock
2	GND	–	Digital ground
3	TMS	IN	JTAG test mode select
4	GND	–	Digital ground
5	TDO_PCIE2	OUT	JTAG test data out
6	GND	–	Digital ground
7	TDI	IN	JTAG test data in
8	GND	–	Digital ground
9	TRST#	IN	JTAG test reset
10	NC	–	Not connected

In the standard version of the STKP2020 the JTAG chain, i.e. all components relevant for this, are not assembled. Only the CPU is accessible by JTAG via the separate COP/JTAG connector (see section 3.3.1.7, COP/JTAG P2020).

Table 52: Used type of connector (JTAG test connector)

Manufacturer / type	Description
Pin header	Double row, 2.54 mm pitch, 10-pin

3.3.3.8 Battery socket

The TQMP2020 is equipped with a real time clock (RTC). A lithium battery CR2032 on the STKP2020 supplies the RTC. Therefore the STKP2020 is equipped with a battery socket (G610).

Alternatively the buffer voltage can be supplied externally at the pins X610 and X611, or the battery voltage be measured.

The following illustration shows the position of the battery socket, as well as the pins X610 and X611 on the STKP2020:

Illustration 39: Position of battery socket

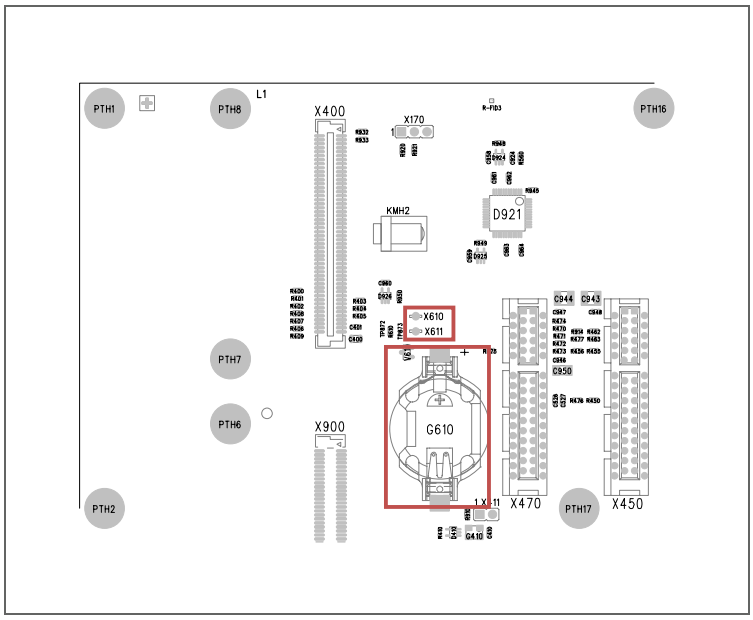


Table 53: Pinout of RTC battery external supply / measurement (X610, X611)

Pin	Pinout
X610	Positive pole of battery
X611	GND

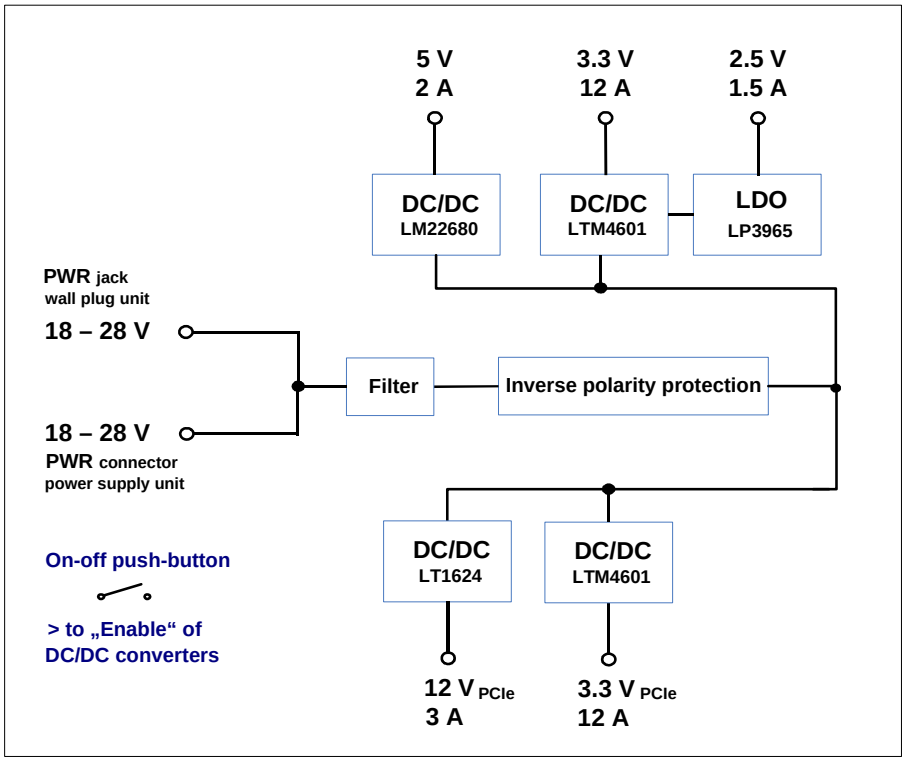
The battery is protected against short circuit, over current and reverse polarity.
An extricable insulating foil to prevent an inadvertent short circuit or the discharge of the lithium battery during transport protects the buffer battery.

3.3.3.9 Power supply

3.3.3.9.1 Power supply block diagram

The following block diagram shows schematically the power supply and how the required voltages are generated on the STKP2020:

Illustration 40: Power supply block diagram



3.3.3.9.2 Input power supply

The specification of an external supplied power is described in section 3.3.1.1, Power supply.

3.3.3.9.3 Voltage generation 5 V

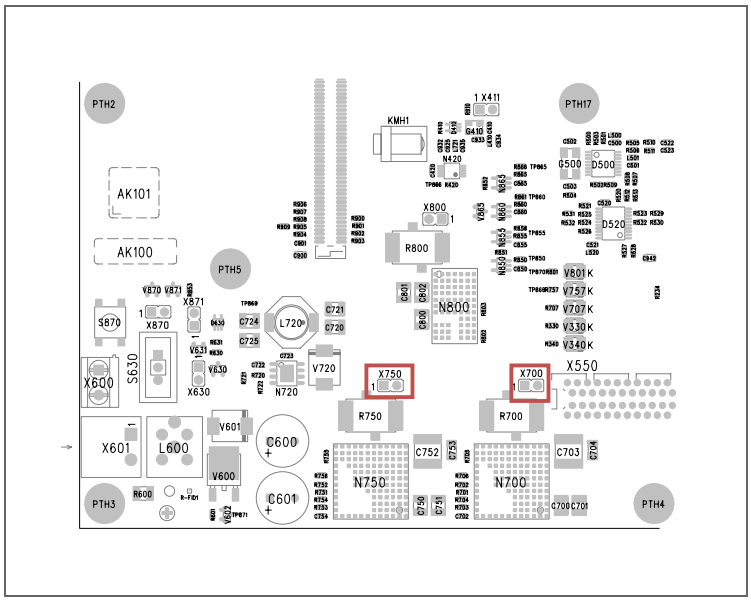
The Starterkit-internal 5 V (VCC5V) is generated from the input voltage by a DC /DC converter (N720).

3.3.3.9.4 Voltage generation 3.3 V and 3.3 V PCIe

The Starterkit-internal 3.3 V (VCC3V3, VCC3V3_PCIE) are generated from the input voltage by DC/DC converters (N700, N750). There is a low-impedance measuring resistor (R700, R750) after each DC/DC converter, through which the currents can be measured.
These measuring resistors can be tapped at headers X700 (VCC3V3) and X750 (VCC3V3_PCIE).

The following illustration shows the position of the headers for the 3.3 V measuring resistors on the STKP2020:

Illustration 41: Position of headers "3.3 V measuring resistors"

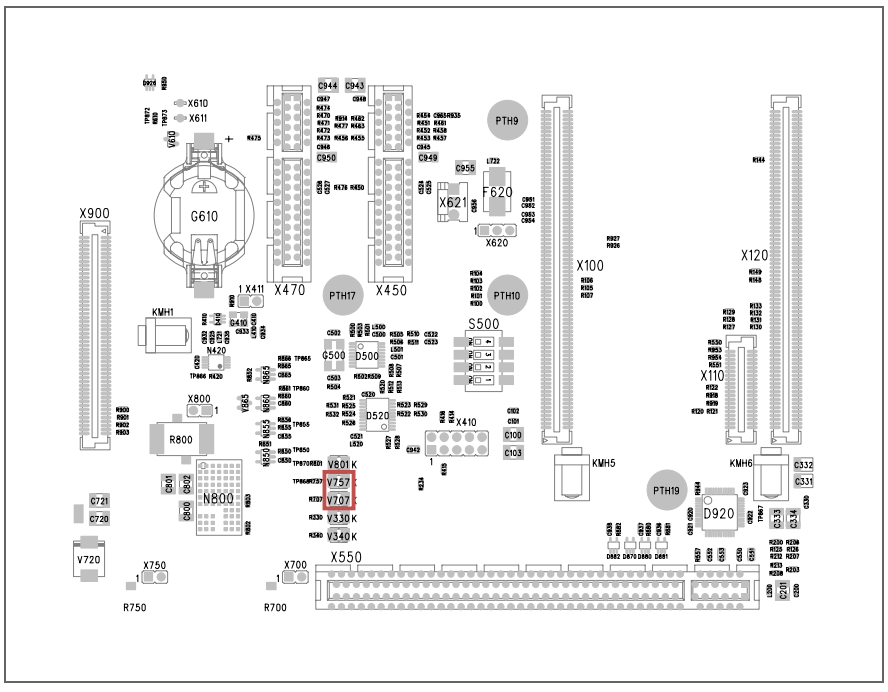


More details concerning the current measurement can be found in section 3.3.3.9.8, Current measurement.
Both DC/DC converters provide a "Power Good" output, which is connected to a red LED in each case.
The LEDs light up, as soon as the "Power Good" signal goes low, indicating that an error has occurred.
As the respective DC/DC converter shuts down at an error, the LED only lights up for a very short time.

- LED V707: "3V3 ERR"
- LED V757: "3V3 PCIE ERR"

The following illustration shows the position of the Error-LEDs for the voltages VCC3V3 and VCC3V3_PCIE on the STKP2020:

Illustration 42: Position of Error-LEDs VCC3V3, VCC3V3_PCIE



3.3.3.9.5 Voltage generation 2.5 V

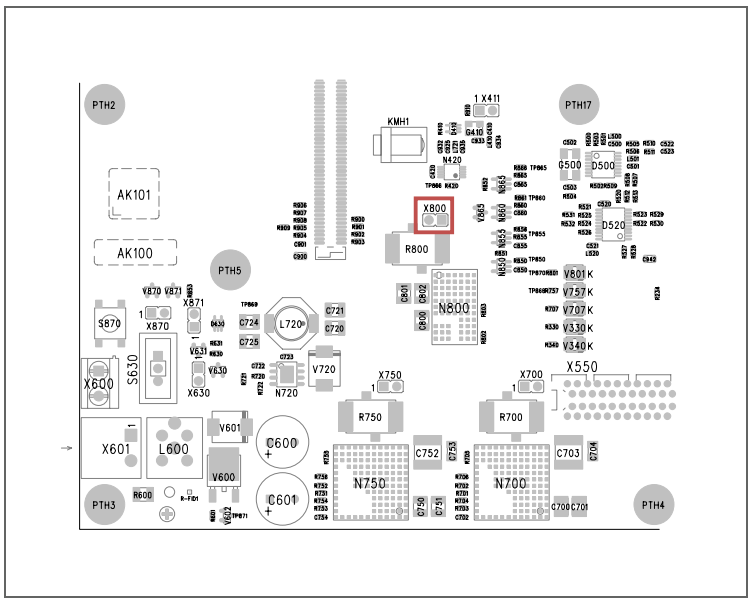
An LDO (N390) generates the Starterkit-internal 2.5 V (VCC2V5) from VCC3V3.

3.3.3.9.6 Voltage generation 12 V PCIe

The Starterkit-internal 12 V (VCC12V_PCIE) is generated from the input voltage by DC/DC converter (N800).
There is a low-impedance measuring resistor (R800) after the DC/DC converter, through which the current can be measured.
This measuring resistor can be tapped at header X800.

The following illustration shows the position of the header for the 12 V PCIe measuring resistor on the STKP2020:

Illustration 43: Position of header “12 V PCIe measuring resistor”

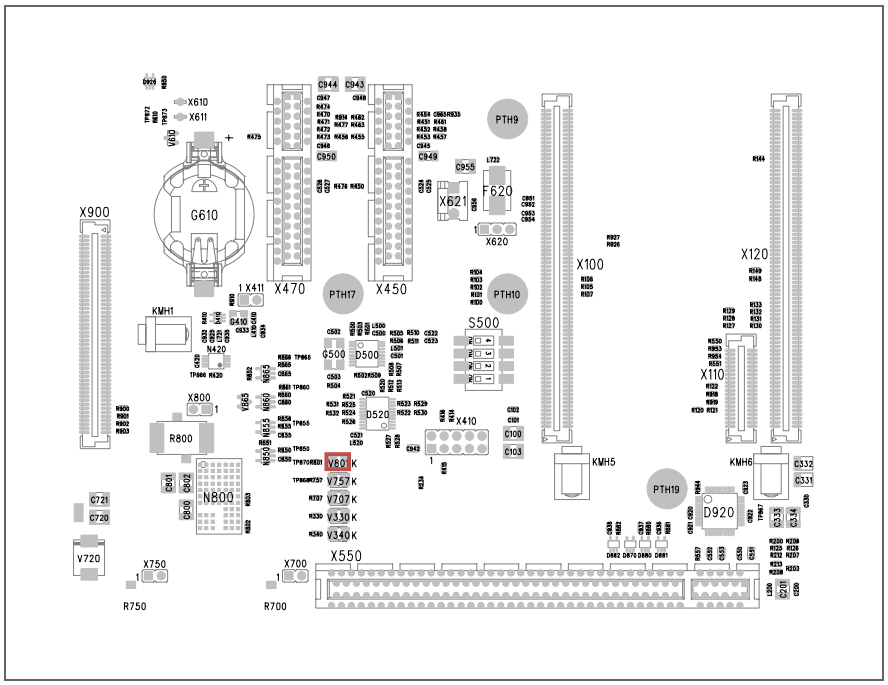


More details concerning the current measurement can be found in section 3.3.3.9.8, Current measurement.
The DC/DC converter provides a "Power Good" output, which is connect to a red LED.
The LED lights up, as soon as the "Power Good" signal goes low, indicating that an error has occurred.
As the DC/DC converter shuts down at an error, the LED only lights up for a very short time.

3.3.3.9.7 LED V810: 12 V PCIE ERR

The following illustration shows the position of the Error-LED for the voltage VCC12V_PCIE on the STKP2020:

Illustration 44: Position of Error-LED VCC12V_PCIE



3.3.3.9.8 Current measurement

The following table shows the single measurable voltages, their corresponding measuring resistor and the voltage drop per 0.1 A/1 A.

Table 54: Current measurement on the STKP2020

Voltage	Maximum current	Measuring resistor	Value	Measurement at pin header	Voltage drop per 0.1 A	Voltage drop per 1 A
VCC3V3	12 A	R700	5 mΩ	X700	0.5 mV	5 mV
VCC3V3_PCIE	12 A	R750	5 mΩ	X750	0.5 mV	5 mV
VCC12V_PCIE	3 A	R800	5 mΩ	X800	0.5 mV	5 mV

It is recommended to measure the voltage drop with a high impedance voltage meter.

3.3.3.9.9 Power consumption

The following table shows the current consumption of the STKP2020 in different load scenarios:

Table 55: Current consumption STKP2020 in different load scenarios

Load scenario	Current consumption
U-Boot, both cores active	1.92 A
Linux shell	1.56 A
PQ software	2.2 A (maximum)

The following table shows all voltages generated on the STKP2020, as well as the maximum current which the respective voltage source can supply.

Table 56: Voltages and currents on the STKP2020

Voltage	Maximum current total	Components / interfaces / comment
5 V VCC5V	2 A	USB interfaces 0.5 A Local bus slot Galvanic separation of the ports COM Fan
3.3 V VCC3V3	12 A	Module Local bus slot SD/MMC card I^2C GPIO expander FlexiFace® 1, 2 USB Phy Clock generation and clock distribution Fan LDO to 2V5 Test PLDs User LEDs GPIO adapter board Headers (GPIO, UART, SPI)
3.3 V VCC3V3_PCIE	12 A	2 × PCIe, maximum 3 A per slot
12 V VCC12V_PCIE	3 A	2 × PCIe, maximum 2.1 A per slot Galvanic separation ports COM
2.5 V VCC2V5	1.5 A	On-board gigabit Ethernet Test PLD Header (IEEE® 1588)

Based on the specifications of the connectors / headers the maximum permitted current is given for every external interface. It may not be exceeded permanently.

3.3.3.10 Voltage supervision and reset generation

The voltages on the STKP2020 are monitored by comparators, which compare the monitored voltage with a reference voltage. If one of the voltages drops below a threshold, the reset input of the TQMP2020 (RESIN#) is pulled low and a reset of the TQMP2020 is triggered.
Other RESIN# sources are the reset push-button (see section 3.3.4.2), and the signal HRESET_REQ# from the TQMP2020. Jumper X871 must be closed to make HRESET_REQ# a source for RESIN#.

The following illustration shows the position of the HRESET_REQ# jumper (X871) on the STKP2020:

Illustration 45: Position of HRESET_REQ# jumper

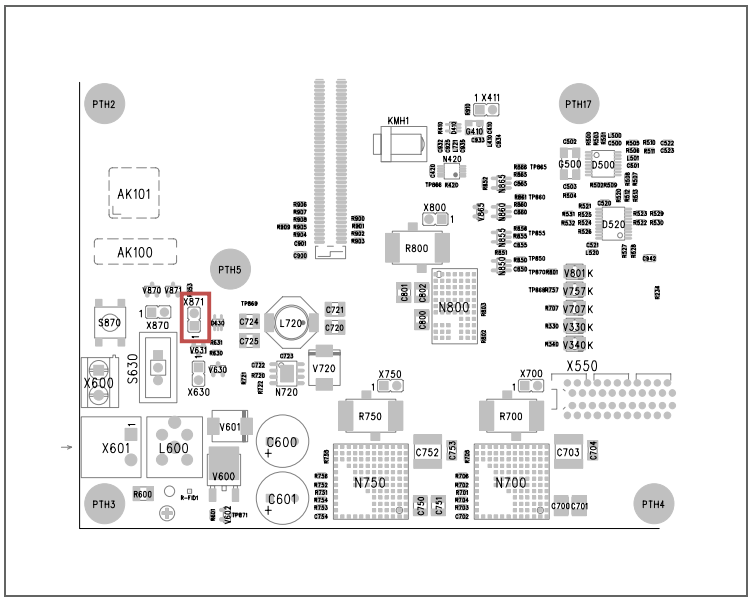


Table 57: Pinout of HRESET_REQ# jumper (X871)

Pin	Signal	Description
1	MR#	MR# of the supervisor device D870
2	HRESET_REQ#	HRESET_REQ#

Table 58: Used type of connector (HRESET_REQ# jumper)

Manufacturer / type	Description
Pin header	Single row, 2.54 mm pitch, 2-pin

If the TQMP2020 is reset by RESIN#, the signal (HRESET#) on the STKP2020 is triggered to reset all components on the STKP2020.

3.3.4 User's interfaces

3.3.4.1 On-off switch

The voltages required on the STKP2020 are generated from the input voltage by several DC/DC converters and LDOs. To switch on these converters, the on-off switch (S630) must be pressed.

More information about the on-off switch can be found in section 3.3.1.1, Power supply.

3.3.4.2 Reset push-button

There is a reset push-button on the STKP2020 to reset the board at any time again into a defined condition.

More information about reset generation can be found in section 3.3.3.10, Voltage supervision and reset generation.

3.3.4.3 User DIP switches

The STKP2020 provides three 4-fold DIP switches (S250, S251, and S252) for user's inputs.
Their state can be read out with an I²C I/O expander.

More information about the user's DIP switches can be found in section 3.3.3.5, I²C I/O expander 1 (DIP switches, push-buttons).

3.3.4.4 User push-buttons

The STKP2020 provides four push-buttons (S253, S254, S871, and S872) for user's inputs.
Their state can be read out with an I²C I/O expander.

More information about the user's push-buttons can be found in section 3.3.3.5, I²C I/O expander 1 (DIP switches, push-buttons).

3.3.4.5 User LEDs

16 User-LEDs serve to display the operational conditions of the module.
An I²C I/O expander drives them.

More information about the user's LEDs can be found in section 3.3.3.6, I²C I/O expander 2 (LEDs).

3.3.4.6 Status / Error LEDs

Several LEDs are provided to display status and function of the STKP2020:

- V340: "USB_PWR_OK" see section 3.3.1.5, USB
- V330: "USB_PWR ERR" see section 3.3.1.5, USB
- LED V707: "3V3 ERR" see section 3.3.3.9.4, Voltage generation 3.3 V and 3.3 V PCIe
- LED V757: "3V3 PCIE ERR" see section 3.3.3.9.4, Voltage generation 3.3 V and 3.3 V PCIe
- LED V810: "12V PCIE ERR" see section 3.3.3.9.6, Voltage generation 12 V PCIe

3.3.4.7 Ethernet LEDs

- On-board gigabit Ethernet: see section 3.3.1.4, On-board gigabit Ethernet

3.3.4.8 SERDES clock DIP switch

The STKP2020 provides a 4-fold DIP switch (S500) to set the SERDES clock source and spread spectrum.

More information about the SERDES clock DIP switch can be found in section 3.3.3.2, SERDES clock generation.

4. SOFTWARE SPECIFICATION

The software specification is dealt with in a separate project.

5. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

5.1 EMC characteristics

The Starterkit STKP2020 is operated as a development platform with module without housing.
The EMC behaviour is not taken into consideration.

5.2 Operational safety and personal security

Due to the occurring voltages (≤ 28 V DC), and its use as a development platform, tests with respect to the operational and personal safety have not been carried out.

6. CLIMATIC AND OPERATIONAL CONDITIONS

Environmental temperature (min):	0 °C
Component temperature (max):	70 °C or according to the specification of the single components
Storage temperature:	–20 °C to +70 °C
Protection class	IP00

6.1 Reliability and product life

The Starterkit STKP2020 serves as a development platform.
The components used were designed in principle for the commercial temperature range.
Further considerations with regard to climate and operating conditions were not made.

6.2 Environment protection

6.2.1 RoHS compliance

The Starterkit STKP2020 is manufactured RoHS compliant.

6.2.2 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as information. Tests or certifications were not carried out with respect to this.

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