# TQMa91xxCA
# Preliminary User's Manual

TQMa91xxCA UM 0004
03.04.2025

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# FIGURE DIRECTORY

# REVISION HISTORY

| Rev. | Date | Name | Pos. | Modification |
|---|---|---|---|---|
| 0001 | 30.11.2023 | Kreuzer | | First issue |
| 0002 | 01.08.2024 | Kreuzer | 1.4, 6.5, 6.6, 6.7, 7.5<br>Figure 25 | Chapter added<br>Figure corrected |
| 0003 | 29.10.2024 | Kreuzer | 3.1.2 | Connector source added |
| 0004 | 03.04.2025 | Kreuzer | Table 2<br>3.2.6.8 | RGB alternative use added<br>Chapter added |

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## 1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

## 1.7 Symbols and typographic conventions

Table 1: Terms and conventions

| Symbol | Meaning |
|---|---|
|  | This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V. |
|  | This symbol indicates the possible use of voltages higher than 24 V.<br>Please note the relevant statutory regulations in this regard.<br>Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component. |
|  | This symbol indicates a possible source of danger.<br>Ignoring the instructions described can cause health damage, or damage the hardware. |
|  | This symbol represents important details or aspects for working with TQ-products. |
| `Command` | A font with fixed-width is used to denote commands, contents, file names, or menu items. |

## 1.8 Handling and ESD tips

General handling of your TQ-products

| | |
|---|---|
|  | The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.<br>A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.<br>Violation of this guideline may result in damage / destruction of the TQMa91xxCA and be dangerous to your health.<br>Improper handling of your TQ-product would render the guarantee invalid. |

Proper ESD handling

| | |
|---|---|
|  | The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).<br>Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices. |

## 1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

## 1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa91xxCA circuit diagram
- MBa91xxCA User's Manual
- i.MX 91 Data Sheet
- i.MX 91 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa91xxCA (in progress)

# 2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of the TQMa91xxCA as of revision 01xx, in combination with the MBa91xxCA as of revision 01xx and refers to some software settings. A certain TQMa91xxCA derivative does not necessarily provide all features described in this Preliminary User's Manual.

This Preliminary User's Manual does neither replace the i.MX 91 Reference Manual (1), nor the i.MX 91 Data Sheet (2), nor any other documents from NXP.

The TQMa91xxCA is a universal Minimodule based on the NXP Arm® Cortex®-A55 based i.MX 91 CPU family, see also Table 4.

## 2.1 Key functions and characteristics

The TQMa91xxCA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

All essential i.MX 91 signals are routed to the TQMa91xxCA connectors. There are therefore no restrictions for customers using the TQMa91xxCA with respect to an integrated customised design. All essential components like CPU, LPDDR4, eMMC, and PMIC are already integrated on the TQMa91xxCA.

The main features of the TQMa91xxCA are:

- 64 bit NXP i.MX 91 CPU with 1 x Arm Cortex A55
- Up to 2 Gbyte of LPDDR4 RAM
- Up to 256 Gbyte of eMMC NAND Flash, eMMC standard 5.1
- Up to 256 Mbyte QSPI NOR Flash (optional)
- 64 Kbit EEPROM (optional)
- Temperature sensor + EEPROM
- NXP Power Management Integrated Circuit PCA9451
- RTC (optional)
- Trust Secure Element (optional)
- Gyroscope (optional)
- All essential i.MX 91 signals are routed to the TQMa91xxCA connectors
- Single supply voltage 5 V

## 2.2 CPU block diagram

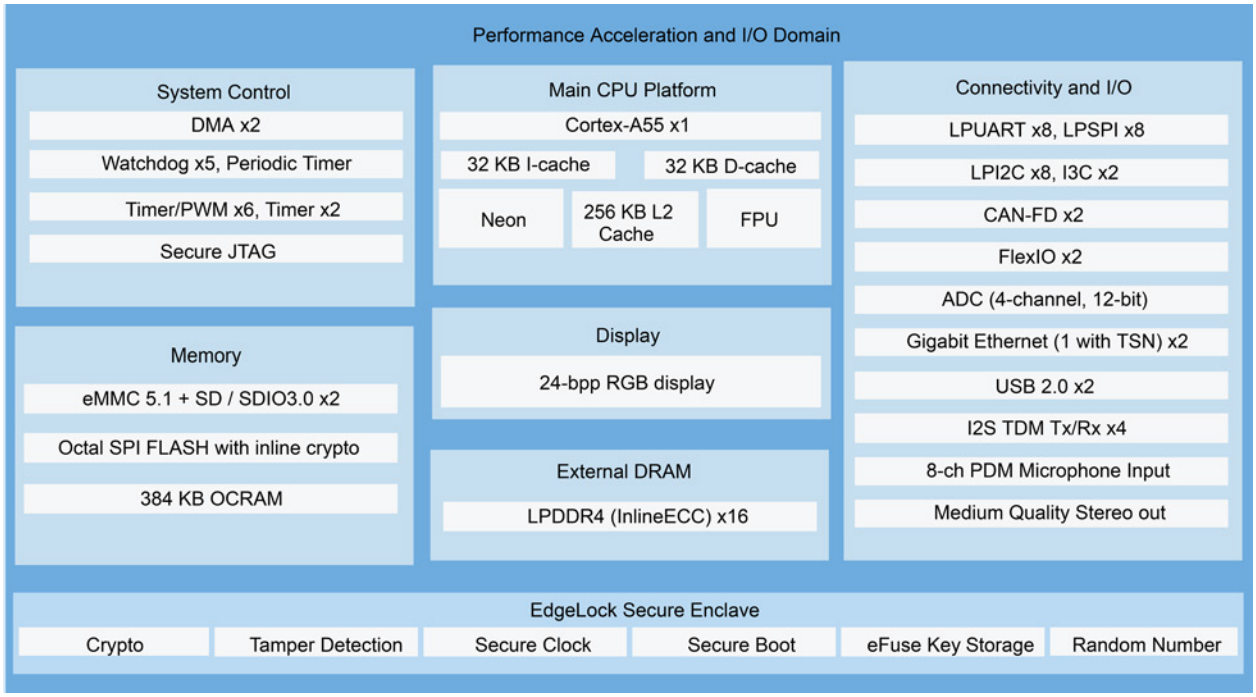


Figure 1: Block diagram i.MX 91
(Source: NXP)

# 3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa91xxCA, and the BSP provided by TQ-Systems GmbH, see also chapter 4.

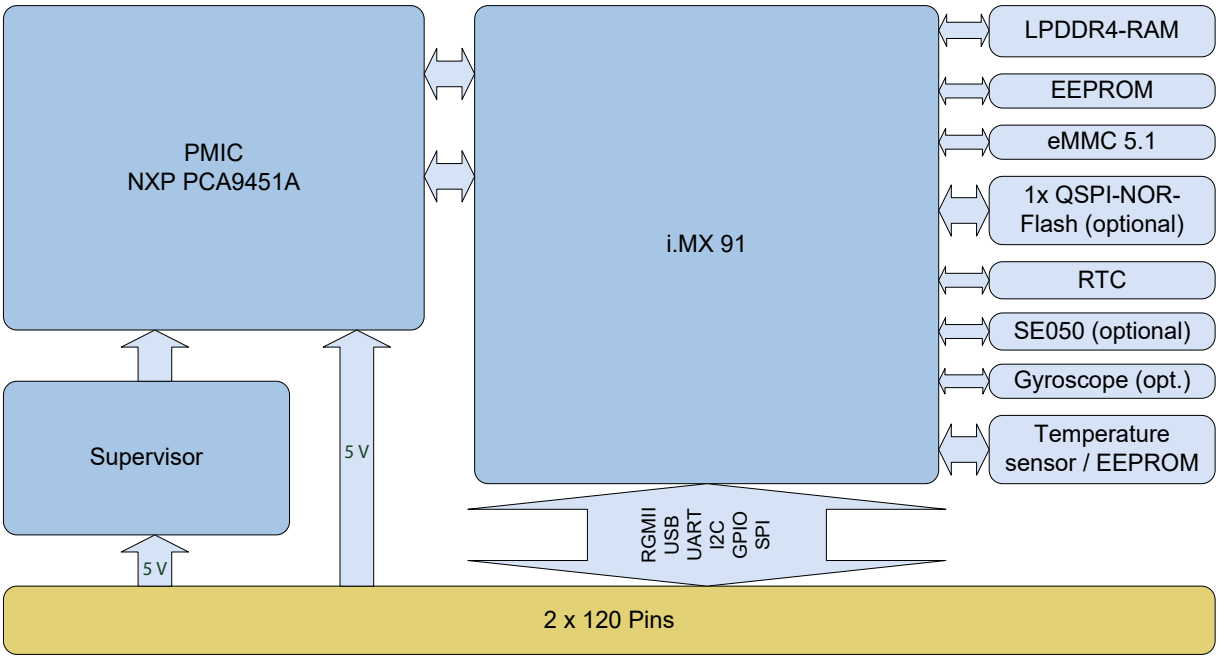


Figure 2: Block diagram TQMa91xxCA (simplified)

## 3.1 Interfaces to other systems and devices

### 3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX 91 internal function units must be taken note of.
The pin assignment in Table 3 refers to a TQMa91xxCA with i.MX 91 CPU in combination with the carrier board MBa91xxCA.
NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).
The electrical and pin characteristics are to be taken from the i.MX 91 and PMIC documentation, see Table 37.

| Attention: Destruction or malfunction, pin multiplexing | |
|---|---|
|  | Depending on the configuration, many i.MX 91 pins can provide several different functions.<br>Please take note of the information concerning the configuration of these pins in the i.MX 91 Reference Manual (1), before integration or start-up of your carrier board / Starterkit.<br>Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa91xxCA.<br><br>The descriptions given in the following tables should be taken note of:<br>– DNC: These pins must never be connected and have to be left open.<br><br>Please contact TQ-Support for details. |

### 3.1.2 Pinout TQMa91xxCA

Table 2: Pinout TQMa91xxCA, X1

| Cpu ball | Dir. | Level | TQ Multiplexing | Pin | | TQ Multiplexing | Level | Dir. | CPU ball |
|---|---|---|---|---|---|---|---|---|---|
| - | P | 5 V | V_5V_IN | X1-A1 | X1-B1 | V_5V_IN | 5 V | P | - |
| - | P | | V_5V_IN | X1-A2 | X1-B2 | V_5V_IN | | P | - |
| - | P | | V_5V_IN | X1-A3 | X1-B3 | V_5V_IN | | P | - |
| - | - | 0 V | GND | X1-A4 | X1-B4 | GND | 0 V | - | - |
| AA2 | O | 1.8 V | GPIO3_IO26 | X1-A5 | X1-B5 | ENET1_TXC | 1.8 V | O | U10 |
| - | - | 0 V | GND | X1-A6 | X1-B6 | GND | 0 V | - | - |
| Y3 | O | 1.8 V | GPIO3_IO27 | X1-A7 | X1-B7 | ENET1_TX_CTL | 1.8 V | O | V10 |
| U4 | O | | CLK3_OUT | X1-A8 | X1-B8 | ENET1_TXD0 | | O | W11 |
| V4 | O | | GPIO4_IO29 | X1-A9 | X1-B9 | ENET1_TXD1 | | O | T12 |
| - | - | 0 V | GND | X1-A10 | X1-B10 | ENET1_TXD2 | | O | U12 |
| - | I/O | 3.3 V | PMIC_SCLH | X1-A11 | X1-B11 | ENET1_TXD3 | | O | V12 |
| - | I/O | | PMIC_SDAH | X1-A12 | X1-B12 | GND | 0 V | - | - |
| - | - | 0 V | GND | X1-A13 | X1-B13 | ENET1_RXC | 1.8 V | I | AA7 |
| - | I/O | 1.8 V | PMIC_SDAL | X1-A14 | X1-B14 | GND | 0 V | - | - |
| - | I/O | | PMIC_SCLL | X1-A15 | X1-B15 | ENET1_RX_CTL | 1.8 V | I | Y8 |
| - | - | 0 V | GND | X1-A16 | X1-B16 | GND | 0 V | - | - |
| AA19 | O | V_SD2 | SD2_CLK | X1-A17 | X1-B17 | ENET1_RXD0 | 1.8 V | I | AA8 |
| - | - | 0 V | GND | X1-A18 | X1-B18 | ENET1_RXD1 | | I | Y9 |
| Y19 | I/O | V_SD2 | SD2_CMD | X1-A19 | X1-B19 | ENET1_RXD2 | | I | AA9 |
| Y17 | I | | SD2_CD# | X1-A20 | X1-B20 | ENET1_RXD3 | | I | Y10 |
| - | - | 0 V | GND | X1-A21 | X1-B21 | GND | 0 V | - | - |
| Y18 | I/O | V_SD2 | SD2_DATA0 | X1-A22 | X1-B22 | ENET1_MDC | 1.8 V | O | AA11 |
| AA18 | I/O | | SD2_DATA1 | X1-A23 | X1-B23 | ENET1_MDIO | | I/O | AA10 |
| Y20 | I/O | | SD2_DATA2 | X1-A24 | X1-B24 | GND | 0 V | - | - |
| AA20 | I/O | | SD2_DATA3 | X1-A25 | X1-B25 | QSPI_SCLK[1] | 1.8 V | O | V16 |
| - | - | 0 V | GND | X1-A26 | X1-B26 | GND | 0 V | - | - |
| AA17 | O | V_SD2 | SD2_RST# | X1-A27 | X1-B27 | QSPI_SS0#[1] | 1.8 V | O | U16 |
| - | - | 0 V | GND | X1-A28 | X1-B28 | QSPI_DATA0[1] | | I/O | T16 |
| - | P | 1.8 V / 3.3V | V_SD2 | X1-A29 | X1-B29 | QSPI _DATA1[1] | | I/O | V14 |
| - | - | 0 V | GND | X1-A30 | X1-B30 | QSPI _DATA2[1] | | I/O | U14 |
| - | P | 3.3 V | V_3V3_SD[2] | X1-A31 | X1-B31 | QSPI _DATA3[1] | | I/O | T14 |
| - | - | 0 V | GND | X1-A32 | X1-B32 | GND | 0 V | - | - |
| - | P | 3.3 V | V_3V3[3] | X1-A33 | X1-B33 | RFU | - | - | - |
| - | P | 1.8 V | V_1V8[3] | X1-A34 | X1-B34 | RFU | - | - | - |
| - | - | 0 V | GND | X1-A35 | X1-B35 | GND | 0 V | - | - |
| R20 | I/O | V_GPIO | SAI3_MCLK[4] | X1-A36 | X1-B36 | PMIC_RST# | 1.8 V | I | - |
| - | - | 0 V | GND | X1-A37 | X1-B37 | RESET_OUT# | open drain, needs external pull-up | | |
| T21 | I/O | V_GPIO | SAI3_TXD0[4] | X1-A38 | X1-B38 | GPIO1_IO02 | 3.3 V | I/O | D20 |
| V20 | I/O | | SAI3_TXFS[4] | X1-A39 | X1-B39 | GND | 0 V | - | - |
| R21 | I/O | | SAI3_TXC[4] | X1-A40 | X1-B40 | UART6_RXD[4] | V_GPIO | I/O | L18 |
| - | - | O V | GND | X1-A41 | X1-B41 | UART6_TXD[4] | | I/O | L17 |
| T20 | I/O | V_GPIO | SAI3_RXD0[4] | X1-A42 | X1-B42 | GND | 0 V | - | - |
| R17 | I/O | | SAI3_RXFS[4] | X1-A43 | X1-B43 | TPM5_CH0[4] | V_GPIO | I/O | L20 |
| R18 | I/O | | SAI3_RXC[4] | X1-A44 | X1-B44 | GPIO2_IO07[4] | | I/O | L21 |
| - | - | 0 V | GND | X1-A45 | X1-B45 | GND | 0 V | - | - |
| N20 | I/O | V_GPIO | UART8_TXD[4] | X1-A46 | X1-B46 | SPI6_PCS0#[4] | V_GPIO | I/O | J21 |
| N21 | I/O | | UART8_RXD[4] | X1-A47 | X1-B47 | SPI6_SIN[4] | | I/O | J20 |
| - | - | 0 V | GND | X1-A48 | X1-B48 | SPI6_SOUT[4] | | I/O | K20 |
| P20 | I/O | V_GPIO | UART3_TXD[4] | X1-A49 | X1-B49 | SPI6_SCK[4] | | I/O | K21 |
| P21 | I/O | | UART3_RXD[4] | X1-A50 | X1-B50 | GND | 0 V | - | - |
| - | - | 0 V | GND | X1-A51 | X1-B51 | GPIO2_IO10[4] | V_GPIO | I/O | N17 |
| U21 | I/O | V_GPIO | GPIO2_IO24[4] | X1-A52 | X1-B52 | TPM3_EXTCLK[4] | | I/O | M21 |
| U20 | I/O | | I2C5_SCL[4] | X1-A53 | X1-B53 | TPM6_CH0[4] | | I/O | M20 |
| U18 | I/O | | I2C5_SDA[4] | X1-A54 | X1-B54 | GPIO2_IO11[4] | | I/O | N18 |
| - | - | 0 V | GND | X1-A55 | X1-B55 | GND | 0 V | - | - |
| W21 | I/O | V_GPIO | CAN2_RX[4] | X1-A56 | X1-B56 | GPIO1_IO14 | 3.3 V | O | H20 |
| V21 | I/O | | CAN2_TX[4] | X1-A57 | X1-B57 | GPIO1_IO12 | | I | G20 |
| - | - | 0 V | GND | X1-A58 | X1-B58 | GPIO1_IO11 | | O | G21 |
| Y21 | I/O | V_GPIO | I2C3_SCL | X1-A59 | X1-B59 | UART2_RTS# | | O | H21 |
| W20 | I/O | | I2C3_SDA | X1-A60 | X1-B60 | GND | 0 V | - | - |

[1] NC if NOR-Flash is placed

[2] Power-Output (max. 400 mA)

[3] Power-Output (max. 500 mA)

[4] Alternative use as RGB interface

Table 3: Pinout TQMa91xxCA, X2

| CPU ball | Dir. | Level | TQ Multiplexing | Pin | | TQ Multiplexing | Level | Dir. | CPU ball |
|---|---|---|---|---|---|---|---|---|---|
| - | I/O | 3.3 V | ISO_14443_LA | X2-A1 | X2-B1 | DNC | - | - | C1 |
| - | I/O | | ISO_14443_LB | X2-A2 | X2-B2 | DNC | | - | B1 |
| - | - | 0 V | GND | X2-A3 | X2-B3 | GND | 0 V | - | - |
| - | I | 3.3 V | ISO_7816_CLK | X2-A4 | X2-B4 | DNC | - | - | B3 |
| - | I/O | | ISO_7816_IO1 | X2-A5 | X2-B5 | DNC | | - | A3 |
| - | - | 0 V | GND | X2-A6 | X2-B6 | GND | 0 V | - | - |
| - | I/O | 3.3 V | ISO_7816_IO2 | X2-A7 | X2-B7 | DNC | - | - | B2 |
| - | I | 3.3 V | ISO_7816_RST | X2-A8 | X2-B8 | DNC | | - | A2 |
| - | - | 0 V | GND | X2-A9 | X2-B9 | GND | 0 V | - | - |
| W1 | I | 1.8 V | JTAG_TDI | X2-A10 | X2-B10 | DNC | - | - | B4 |
| Y2 | O | | JTAG_TDO | X2-A11 | X2-B11 | DNC | | - | A4 |
| Y1 | O | | JTAG_TCK | X2-A12 | X2-B12 | GND | 0 V | - | - |
| W2 | I/O | | JTAG_TMS | X2-A13 | X2-B13 | DNC | - | - | B5 |
| - | - | 0 V | GND | X2-A14 | X2-B14 | DNC | | - | A5 |
| - | P | 0.9…5.5 V | V_LICELL | X2-A15 | X2-B15 | RTC_EVENT# | open drain, needs external pull-up | | |
| - | - | 0 V | GND | X2-A16 | X2-B16 | GND | 0 V | - | - |
| U6 | O | 1.8 V | ENET2_TXC | X2-A17 | X2-B17 | TEMP_EVENT# | open drain, needs external pull-up | | |
| - | - | 0 V | GND | X2-A18 | X2-B18 | DNC | - | - | A6 |
| V6 | O | 1.8 V | ENET2_TX_CTL | X2-A19 | X2-B19 | DNC | | - | B6 |
| T8 | O | | ENET2_TXD0 | X2-A20 | X2-B20 | GND | 0 V | - | - |
| U8 | O | | ENET2_TXD1 | X2-A21 | X2-B21 | DNC | - | - | A7 |
| V8 | O | | ENET2_TXD2 | X2-A22 | X2-B22 | DNC | | - | B7 |
| T10 | O | | ENET2_TXD3 | X2-A23 | X2-B23 | GND | 0 V | - | - |
| - | - | 0 V | GND | X2-A24 | X2-B24 | DNC | - | - | D6 |
| AA3 | I | 1.8 V | ENET2_RXC | X2-A25 | X2-B25 | DNC | | - | E6 |
| - | - | 0 V | GND | X2-A26 | X2-B26 | GND | 0 V | - | - |
| Y4 | I | 1.8 V | ENET2_RX_CTL | X2-A27 | X2-B27 | DNC | - | - | A8 |
| AA4 | I | | ENET2_RXD0 | X2-A28 | X2-B28 | DNC | | - | B8 |
| Y5 | I | | ENET2_RXD1 | X2-A29 | X2-B29 | GND | 0 V | - | - |
| AA5 | I | | ENET2_RXD2 | X2-A30 | X2-B30 | DNC | - | - | A9 |
| Y6 | I | | ENET2_RXD3 | X2-A31 | X2-B31 | DNC | | - | B9 |
| - | - | 0 V | GND | X2-A32 | X2-B32 | GND | 0 V | - | - |
| AA6 | I/O | 1.8 V | ENET2_MDIO | X2-A33 | X2-B33 | DNC | - | - | A11 |
| Y7 | O | | ENET2_MDC | X2-A34 | X2-B34 | DNC | | - | B11 |
| - | - | 0 V | GND | X2-A35 | X2-B35 | GND | 0 V | - | - |
| C20 | O | 3.3 V | I2C1_SCL | X2-A36 | X2-B36 | DNC | - | - | D10 |
| C21 | I/O | | I2C1_SDA | X2-A37 | X2-B37 | DNC | | - | E10 |
| - | - | 0 V | GND | X2-A38 | X2-B38 | GND | 0 V | - | - |
| J17 | I | 3.3 V | CAN1_RX | X2-A39 | X2-B39 | DNC | - | - | A10 |
| G17 | O | | CAN1_TX | X2-A40 | X2-B40 | DNC | | - | B10 |
| - | - | 0 V | GND | X2-A41 | X2-B41 | GND | 0 V | - | - |
| G18 | I/O | 3.3 V | GPIO1_IO10 | X2-A42 | X2-B42 | ONOFF | 1.8 V | I | A19 |
| B16 | I/O | 1.8 V | TAMPER0 | X2-A43 | X2-B43 | USB1_ID | 1.8 V | I | C11 |
| F14 | I/O | | TAMPER1 | X2-A44 | X2-B44 | USB2_ID | | I | E12 |
| - | - | 0 V | GND | X2-A45 | X2-B45 | GND | 0 V | - | - |
| B17 | I | 1.8 V | CLK1_IN | X2-A46 | X2-B46 | V_GPIO[5] | 1.8 V / 3.3 V | P | N15 |
| A18 | I | | CLK2_IN | X2-A47 | X2-B47 | USB1_VBUS | 3.3 V | P | F12 |
| J18 | O | 3.3 V | WDOG_ANY | X2-A48 | X2-B48 | USB2_VBUS | (5 V tolerant) | P | E14 |
| - | I | 3.3 V | PMIC_WDOG_IN# | X2-A49 | X2-B49 | GND | 0 V | - | - |
| - | - | 0 V | GND | X2-A50 | X2-B50 | DNC | - | - | B12 |
| B19 | I | 1.8 V | ADC_IN0 | X2-A51 | X2-B51 | DNC | | - | A12 |
| A20 | I | | ADC_IN1 | X2-A52 | X2-B52 | GND | 0 V | - | - |
| B20 | I | | ADC_IN2 | X2-A53 | X2-B53 | DNC | - | - | B13 |
| B21 | I | | ADC_IN3 | X2-A54 | X2-B54 | DNC | | - | A13 |
| - | - | 0 V | GND | X2-A55 | X2-B55 | GND | 0 V | - | - |
| E20 | I | 3.3 V | UART1_RXD | X2-A56 | X2-B56 | USB1_DP | 3.3 V | I/O | B14 |
| E21 | O | 3.3 V | UART1_TXD | X2-A57 | X2-B57 | USB1_DN | | I/O | A14 |
| F20 | I | 3.3 V | UART2_RXD | X2-A58 | X2-B58 | GND | 0 V | - | - |
| F21 | O | 3.3 V | UART2_TXD | X2-A59 | X2-B59 | USB2_DP | 3.3 V | I/O | B15 |
| - | - | 0 V | GND | X2-A60 | X2-B60 | USB2_DN | | I/O | A15 |

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX 91 documentation (1), (2), (3), as well as the PMIC Data Sheet (4).

[5] Power-Input for NVCC_GPIO

The TQMa91xxCA has a total of 240 connector pins (2 x 120). The mating connectors for X1 and X2 are available from ept GmbH in two heights:

Table 4: Mating connectors

| Name | Part number | Height |
|---|---|---|
| Colibri Plug 120, 5mm | 401-51401-51 | 5 mm |
| Colibri Plug 120, 8mm | 401-55401-51 | 8 mm |

Connector samples are available from: https://www.ept.de/index.php?tq-colibri-lp

## 3.2 System components

### 3.2.1 i.MX 91

#### 3.2.1.1 i.MX 91 derivatives

Depending on the TQMa91xxCA version, one of the following i.MX 91 derivatives is assembled.

Table 5: i.MX 91 derivatives

| TQMa91xxCA version | i.MX 91 derivative | i.MX 91 clocks | Temperature range |
|---|---|---|---|
| TQMa91x1CA | i.MX 9152 | 1 x A55: 1.4 GHz | –25 °C … +85 °C |
| TBD | TBD | TBD | TBD |

#### 3.2.1.2 i.MX 91 errata

| Attention: Destruction or malfunction, i.MX 91 errata | |
|---|---|
|  | Please take note of the current i.MX 91 errata (5). |

#### 3.2.1.3 Boot modes

The i.MX 91 has a ROM with integrated boot loader. After the release of PMIC_POR# the System Controller (SCU) boots from the internal ROM and then loads the program image from the selected boot device. For example, the integrated eMMC or the optional QSPI NOR Flash can be selected as the default boot device. The following boot sources are supported by TQMa91xxCA:

- eMMC (SD1)
- QSPI/FlexSPI NOR Flash (SD1 + SD3)
- SD card (SD2)
- Serial Download (USB1)

Alternatively, an image can be loaded into the internal RAM using the serial downloader.
More information about the boot flow can be found in the Reference Manual (1), and the Data Sheet (2) of i.MX 91.

#### 3.2.1.4 Boot configuration

This section provides information on boot mode configuration pins allocation and boot device interface allocation. The i.MX 91 uses four BOOT_MODE signals provided on the TQMa91xxCA's connector pins. These require pull-up/pull-down (4.7 kΩ/ 100 kΩ) wiring to 3.3 V and Ground. However, the BOOT_MODE signals are not dedicated to this function, but have other functionalities in normal operation. The boot mode is initialized by sampling the BOOT_MODE[3:0] inputs when the reset is deactivated and are to be set high or low according to the desired boot source at the time of readout. After these inputs are sampled, their subsequent state does not affect the contents of the BOOT_MODE internal register.

The exact boot source configuration can be seen in the following table:

Table 6: Boot configuration i.MX 91

| Boot source | Boot Core | BOOT_MODE3 | BOOT_MODE2 | BOOT_MODE1 | BOOT_MODE0 |
|---|---|---|---|---|---|
| Boot from eFuse | A55 | 0 | 0 | 0 | 0 |
| Serial Downloader (USB1) | | 0 | 0 | 0 | 1 |
| Boot from eMMC 5.1 (USDHC1, 8-bit)) | | 0 | 0 | 1 | 0 |
| Boot from SD 3.0 card (USDHC2, 4-bit) | | 0 | 0 | 1 | 1 |
| Boot from FlexSPI Serial NOR | | 0 | 1 | 0 | 0 |
| Boot from FlexSPI NAND 2K (not supported) | | 0 | 1 | 0 | 1 |

### 3.2.2 Memory

#### 3.2.2.1 LPDDR4 SDRAM

The memory interface of the i.MX 91 supports LPDDR4 memory (16 bit bus) with a maximum clock rate of 1200 MHz, which meets JEDEC LPDDR4-2400 standard. 1 GByte is the standard configuration, a maximum of 2 Gbyte of LPDDR4 SDRAM is supported.

#### 3.2.2.2 eMMC

An eMMC is provided on the TQMa91xxCA for boot loader, operating system and application software. It is connected to the i.MX 91 via SD1-interface. A maximum transfer rate of 400 MB/s is supported (HS400 mode). Resets have to be done via software.

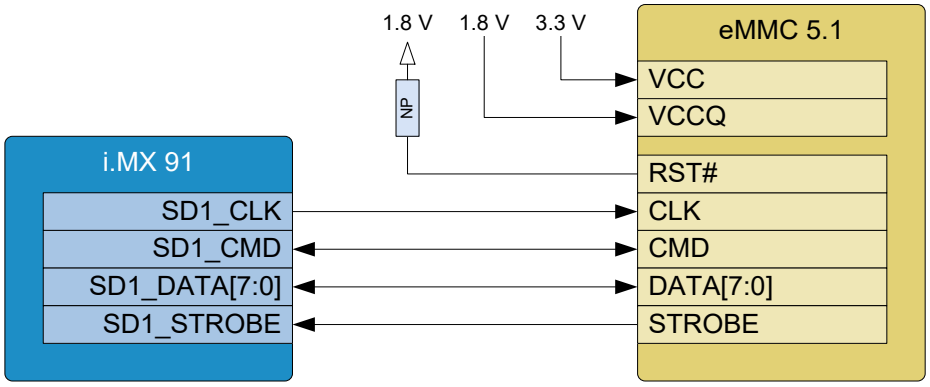


Figure 3: Block diagram eMMC

The boot configuration is described in chapter 3.2.1.3

#### 3.2.2.3 QSPI NOR Flash / NAND Flash

QSPI NOR flash can optionally be assembled on the TQMa91xxCA. Because a separation of the signal paths is not possible, these connector pins must not be wired when equipped with NOR Flash. With unpopulated NOR Flash the signals of the SD3 interface can be used outside the module.

The NOR flash signals use a part of the NAND pins of the i.MX 91. All other NAND pins of the i.MX 91 are used from the TQMa91xxCA for the eMMC as SD1 boot source and for the SD-Card (SD2).

Table 7: QSPI signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| QSPI_DATA0 | T16 | X1-B28 | 1,8 V |
| QSPI_DATA1 | V14 | X1-B29 | |
| QSPI_DATA2 | U14 | X1-B30 | |
| QSPI_DATA3 | T14 | X1-B31 | |
| QSPI_SCLK | V16 | X1-B25 | |
| QSPI_SS0# | U16 | X1-B27 | |

#### 3.2.2.4 EEPROM M24C64-D

A 64 Kbit EEPROM is assembled by default on the TQMa91xxCA. The serial EEPROM is controlled by the I2C1 bus. The M24C64-D offers an additional page, named the Identification Page (32 Byte). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

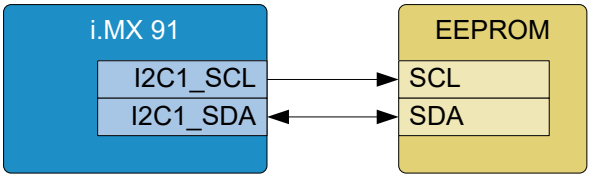


Figure 4: Block diagram EEPROM

- The EEPROM has I²C address `0x57 / 101 0111b`
- Identification Page (32 Byte) `0x5F / 101 1111b`

#### 3.2.2.5 EEPROM with temperature sensor SE97BTP

A serial EEPROM including temperature sensor type SE97BTP, controlled by the I2C1 bus, is assembled on the TQMa91xxCA.
The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write-Protected mode (PWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage.
The overtemperature output of the SE97BTP is connected as open drain to TQMa91xxCA pin X2-B17 (TEMP_EVENT#). The device is assembled on the top side of the TQMa91xxCA (component D6).

- The device provides the following I2C addresses:
  - EEPROM (Normal Mode): `0x53 / 101 0011b`
  - EEPROM (Protection Mode): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

### 3.2.3 Trust Secure Element SE050

An NXP Trust Secure Element SE050 is available on the TQMa91xxCA as an assembly option.

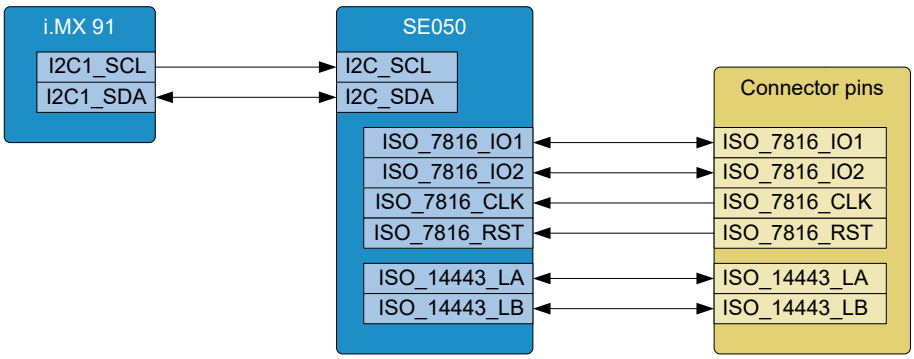


Figure 5: Block diagram SE050

When equipped, the chip provides two interfaces according to ISO 7816 and ISO 14443. Among other things, antennas can be connected to these.

Table 8: ISO_7816 and ISO_14443 signals

| Signal | Direction | TQMa91xxCA | Remark |
|---|---|---|---|
| ISO_7816_CLK | I | X2-A4 | Only with populated Trust Secure Element |
| ISO_7816_RST | I | X2-A8 | |
| ISO_7816_IO1 | I/O | X2-A5 | |
| ISO_7816_IO2 | I/O | X2-A7 | |
| ISO_14443_LA | I/O | X2-A1 | |
| ISO_14443_LB | I/O | X2-A2 | |

The SE050 is controlled by the I2C1 bus. More details can be found in (8).

- The Trust Secure Element has I²C address `0x48 / 100 1000b`

### 3.2.4 Accelerometer/Gyroscope

As an optional extension a 3D Digital Accelerometer / 3D Digital Gyroscope (ISM330DHCX from STMicroelectronics) is provided on theTQMa91xxCA, which has an I²C interface. It allows to determine the position of the module and provides two interrupts. However, these are not routed to the outside.

- The Accelerometer/Gyroscope has I²C address `0x6A / 110 1010b`

### 3.2.5 RTC

The TQMa91xxCA can use the internal Real Time Clock of the i.MX 91 or can be provided with an optional discrete RTC PCF85063A.

#### 3.2.5.1 i.MX 91 internal RTC

The i.MX 91 provides an internal RTC, which has its own power domain, supplied by the PMIC. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

| Note: RTC power supply | |
|---|---|
|  | The CPU internal RTC can be used in regular operation. If the TQMa91xxCA supply (5 V) fails, it is no longer available, since the i.MX 91 power rail is no longer supplied. |

#### 3.2.5.2 Discrete RTC PCF85063A

In addition to the i.MX 91 internal RTC the TQMa91xxCA provides a discrete RTC PCF85063A as an assembly option, which is controlled by the I2C1 bus. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

The discrete RTC has an interrupt output which provides the open-drain signal RTC_EVENT# at pin X2-B15. This pin requires a pull-up to 3.3 V (maximum 3.6 V) on the carrier board.

The RTC PCF85063A is only directly supplied by V_LICELL when the PMIC or the TQMa91xxCA supply is switched off.

During normal operation of the TQMa91xxCA, the PMIC supplies 3.3 V. To prevent charging a non-rechargeable backup supply, a diode on the baseboard is needed for V_LICELL.

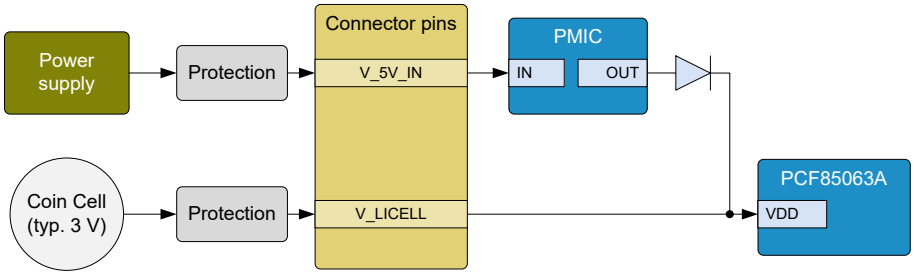


Figure 6: Block diagram RTC supply (TQMa91xxCA with discrete RTC)

- The discrete RTC has I2C address `0x51 / 101 0001b`

| Note: RTC power supply | |
|---|---|
| | The BBSM functions of the i.MX 91 can only be used if the TQMa91xxCA is supplied with 5 V.<br>Because the BBSM rail is not supplied when the TQMa91xxCA is not powered-up, we recommend using the optional RTC PCF85063A. |

### 3.2.6 Interfaces

#### 3.2.6.1 Overview

Except for the internal interfaces, all functional pins of the i.MX 91 are routed to TQMa91xxCA connector pins. Each customer must check the suitability of the multiplexing in the respective project and adapt it if necessary. The following table shows one exemplary multiplexing with the TQMa91xxCA to utilize the most primary interfaces simultaneously:

Table 9: TQMa91xxCA interfaces

| i.MX 91 Interface | Quantity | Remark |
|---|---|---|
| Internal interfaces | | |
| LPDDR4 | 1 | LPDDR4, x16 |
| SD3 (QSPI) | 1 | |
| SD1 (eMMC) | 1 | 8 bit (HS400) |
| External interfaces | | |
| ADC | 1 | 4 x inputs |
| CAN | 2 | |
| GPIO | 12 | |
| I2C | 3 | 1 x for internal components, 2x for other peripherals |
| JTAG | 1 | |
| RGMII | 2 | |
| SAI (Audio) | 1 | |
| SPI | 2 | 1 x CS each (2x CS possible with omission of GPIOs) |
| SmartCard ISO14443 / ISO7816 | 1 | optionally provided by TSE |
| TAMPER | 2 | |
| UART | 5 | 1 x incl. RTS/CTS |
| USB 2.0 | 2 | |
| SD2 (SD-Card) | 1 | 4 bit |

#### 3.2.6.2 ADC

The i.MX 91 has a 12-bit analog-digital converter with a reference voltage of 1.8 V and max. 4 channels.


Figure 7: Block diagram ADC

The reference voltage is provided on the module by the PMIC and is additionally filtered. The supply of an external reference voltage is not provided.

Table 10: Pin assignment ADC

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| ADC_IN0 | B19 | X2-A51 | VDD_ANA_1P8 (1.8 V) |
| ADC_IN1 | A20 | X2-A52 | |
| ADC_IN2 | B20 | X2-A53 | |
| ADC_IN3 | B21 | X2-A54 | |

#### 3.2.6.3 CAN FD

The i.MX 91 provides two CAN FD interfaces. Both are specified according to the CAN 2.0B protocol but have different electrical properties due to their multiplexing. CAN1 has a 3.3 V level. The levels of CAN2 are dependent on the voltage V_GPIO which is set via connector pin X2-B46.

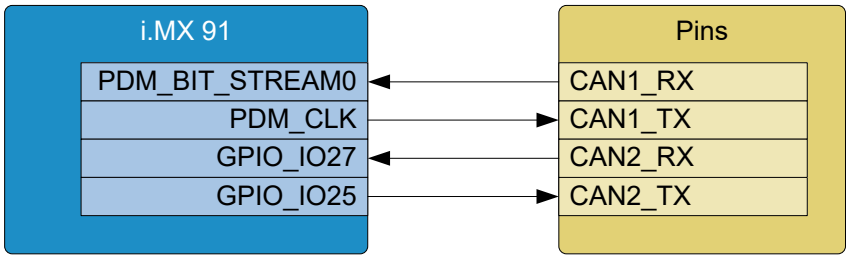


Figure 8: Block diagram CAN

Table 11: CAN FD signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| CAN1_TX | G17 | X2-A40 | NVCC_AON (3.3 V) |
| CAN1_RX | J17 | X2-A39 | |
| CAN2_TX | V21 | X1-A57 | NVCC_GPIO (1.8 V / 3.3 V) |
| CAN2_RX | W21 | X1-A56 | |

#### 3.2.6.4 Ethernet / RGMII

The i.MX 91 has two Ethernet MACs, each operating in maximum Gigabit full-duplex mode. MII, RMII or RGMII can be used as interfaces, the latter being used for standard multiplexing. Each MAC unit has its own MDIO/SMI interface. ENET1 supports both QOS (Quality-of-Service) and TSN (Time-sensitive Network).

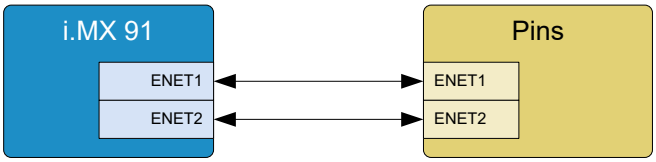


Figure 9: Block diagram RGMII

For RGMII an IO voltage of 1.8 V and for RMII an IO voltage of either 1.8 V or 3.3 V is specified. Due to an operation of both modes with 1.8 V the rail NVCC_WAKEUP is set to 1.8 V. The signals are length matched on the TQMa91xxCA and routed with a differential impedance of 100 Ω. On the carrier board they have to be connected according to RGMII specifications.

The following table shows the signals used in RGMII mode:

Table 12: ENET signals in RGMII mode

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| ENET1_RX_CTL | Y8 | X1-B15 | NVCC_WAKEUP (1.8 V) |
| ENET1_RXC | AA7 | X1-B13 | |
| ENET1_RXD0 | AA8 | X1-B17 | |
| ENET1_RXD1 | Y9 | X1-B18 | |
| ENET1_RXD2 | AA9 | X1-B19 | |
| ENET1_RXD3 | Y10 | X1-B20 | |
| ENET1_TX_CTL | V10 | X1-B7 | |
| ENET1_TXC | U10 | X1-B5 | |
| ENET1_TXD0 | W11 | X1-B8 | |
| ENET1_TXD1 | T12 | X1-B9 | |
| ENET1_TXD2 | U12 | X1-B10 | |
| ENET1_TXD3 | V12 | X1-B11 | |
| ENET1_MDC | AA11 | X1-B22 | |
| ENET1_MDIO | AA10 | X1-B23 | |
| ENET2_RX_CTL | Y4 | X2-A27 | |
| ENET2_RXC | AA3 | X2-A25 | |
| ENET2_RXD0 | AA4 | X2-A28 | |
| ENET2_RXD1 | Y5 | X2-A29 | |
| ENET2_RXD2 | AA5 | X2-A30 | |
| ENET2_RXD3 | Y6 | X2-A31 | |
| ENET2_TX_CTL | V6 | X2-A19 | |
| ENET2_TXC | U6 | X2-A17 | |
| ENET2_TXD0 | T8 | X2-A20 | |
| ENET2_TXD1 | U8 | X2-A21 | |
| ENET2_TXD2 | V8 | X2-A22 | |
| ENET2_TXD3 | T10 | X2-A23 | |
| ENET2_MDC | Y7 | X2-A34 | |
| ENET2_MDIO | AA6 | X2-A33 | |

### 3.2.6.5 I²C

The i.MX 91 provides up to eight I²C interfaces. I2C1 serves as system bus for internal components (RTC, EEPROM, temperature sensor, TSE, gyroscope and PMIC), has pull-ups on the module and is additionally available at connector pins.

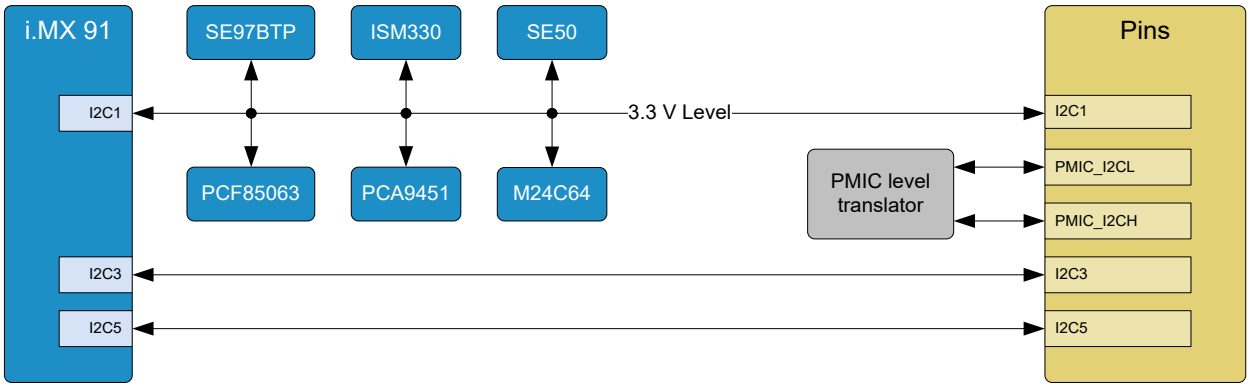


Figure 10: Block diagram I²C

I2C3 and I2C5 are provided as further buses, but without wiring on the TQMa91xxCA. Voltage levels and pull-up resistors are to be defined or placed outside the module.

The PMIC PCA9451 additionally provides an integrated I2C level translator. It is connected to four connector pins and can thus be used in customer designs. The corresponding wiring by means of pull-ups is to be provided outside TQMa91xxCA.

The TQMa91xxCA internal components with their associated addresses are listed in the following table.

Table 13: Address assignment I2C1 bus

| Component | Function | | 7-bit address |
|---|---|---|---|
| PCA9451 | PMIC | | 0x25 / 010 0101b |
| M24C64 | EEPROM | Memory array | 0x57 / 101 0111b |
| | | Identification page (32 Byte) | 0x5F / 101 1111b |
| PCF85063A | RTC | | 0x51 / 101 0001b |
| SE97BTP | EEPROM | Read / Write | 0x53 / 101 0011b |
| | | Protection command | 0x33 / 011 0011b |
| | Temperature sensor in EEPROM | | 0x1B / 001 1011b |
| SE050 (optional) | Trust Secure Element | | 0x48 / 100 1000b |
| ISM330 (optional) | Gyroscope | | 0x6A / 110 1010b |

The following table shows the I²C pin assignment on the TQMa91xxCA.

Table 14: Pin assignment I²C

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| I2C1_SCL | C20 | X2-A36 | NVCC_AON (3.3 V) |
| I2C1_SDA | C21 | X2-A37 | |
| I2C3_SCL | Y21 | X1-A59 | NVCC_GPIO (1.8 V / 3.3 V) |
| I2C3_SDA | W20 | X1-A60 | |
| I2C5_SCL | U20 | X1-A53 | |
| I2C5_SDA | U18 | X1-A54 | |
| PMIC_SCLL | - | X1-A15 | V_1V8 |
| PMIC_SDAL | - | X1-A14 | |
| PMIC_SCLH | - | X1-A11 | V_3V3 |
| PMIC_SDAH | - | X1-A12 | |

If more devices are connected to the I2C1 bus on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional pull-ups should be provided at the I²C bus on the carrier board, if required.

#### 3.2.6.6 JTAG

The processor provides a JTAG interface that can be used to debug the programs executed on the processor. A corresponding hardware tool is required for this. The JTAG signals are routed directly to the connector pins. Pull resistors must be provided on the mainboard.

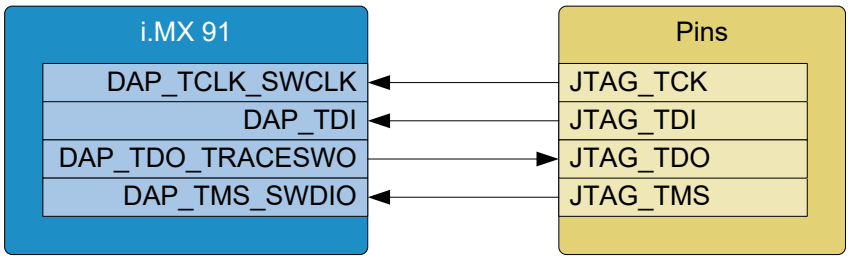


Figure 11: Block diagram JTAG interface

The following table shows the signals used by the JTAG interface. An external circuit on the mainboard has not to be provided.

Table 15: JTAG signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| JTAG_TCK | Y1 | X2-A12 | NVCC_WAKEUP (1.8 V) |
| JTAG_TDI | W1 | X2-A10 | |
| JTAG_TDO | Y2 | X2-A11 | |
| JTAG_TMS | W2 | X2-A13 | |

#### 3.2.6.7 GPIO

Except for dedicated differential signals, e.g. USB, most CPU signals routed to the TQMa91xxCA connector pins can be configured as GPIO. GPIO1_IO03 is not routed to the outside and is used internally in the module to connect the open drain signal PMIC_IRQ_B. The electrical characteristics of the GPIOs are to be taken from the i.MX 91 Data Sheet (2).
The following table shows the GPIO signals primarily configured as GPIO:

Table 16: GPIO signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| GPIO1_IO02 | D20 | X1-B38 | NVCC_AON (3.3 V) |
| GPIO1_IO10 | G18 | X2-A42 | |
| GPIO1_IO11 | G21 | X1-B58 | |
| GPIO1_IO12 | G20 | X1-B57 | |
| GPIO1_IO14 | H20 | X1-B56 | |
| GPIO2_IO07 | L21 | X1-B44 | NVCC_GPIO (1.8 V / 3.3 V) |
| GPIO2_IO10 | N17 | X1-B51 | |
| GPIO2_IO11 | N18 | X1-B54 | |
| GPIO2_IO24 | U21 | X1-A52 | |
| GPIO3_IO26 | AA2 | X1-A5 | NVCC_WAKEUP |
| GPIO3_IO27 | Y3 | X1-A7 | |
| GPIO4_IO29 | V4 | X1-A9 | |

#### 3.2.6.8 RGB

Not as a primary interface, but as an alternative, the CPU can provide a 24-bit RGB interface. This interface is available on the CPU pins GPIO_IO00...GPIO_IO27. For further information please refer to the CPU data sheet (2) or reference manual (1) as well as the available TQ multiplexing file.

This is the only display interface provided by the i.MX 91.

| Caution: Destruction or malfunction, pin multiplexing | |
|---|---|
|  | Due to a CPU erratum, the pixel clock must be reduced to 52 MHz if the V_GPIO power rail is supplied with 3.3 V, which limits the display selection options. If a higher frequency pixel clock is required, this power rail must be supplied with 1.8 V. See the CPU errata documentation (5) for more information. |

#### 3.2.6.9 SAI

The i.MX 91 has several SAI interfaces with different data bus widths. Due to limited multiplexing options, only the SAI3 interface is provided at the connector pins. SAI2 as the most extensive SAI interface (4-bit) can only be used if the second Ethernet interface is omitted.

The SAI interface is full-duplex capable and supports I2S, AC97, TDM and other codec interfaces.

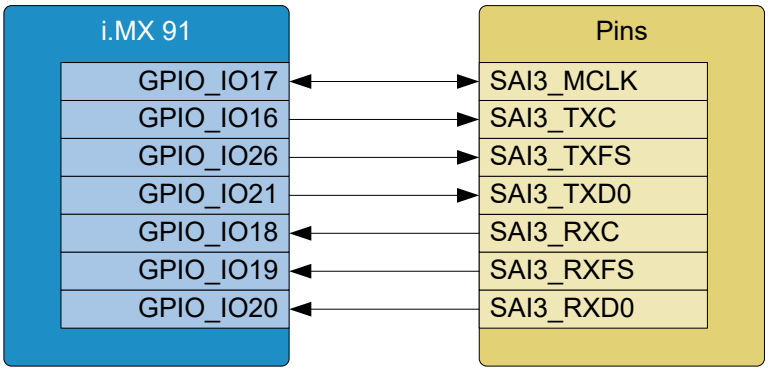


Figure 12: Block diagram SAI3

The following table lists all SAI signals provided by the TQMa91xxCA:

Table 17: SAI signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| SAI3_MLCK | R20 | X1-A36 | NVCC_GPIO (1.8 V / 3.3 V) |
| SAI3_TXC | R21 | X1-A40 | |
| SAI3_TXFS | V20 | X1-A39 | |
| SAI3_TXD0 | T21 | X1-A38 | |
| SAI3_RXD0 | T20 | X1-A42 | |
| SAI3_RXFS | R17 | X1-A43 | |
| SAI3_RXC | R18 | X1-A44 | |

#### 3.2.6.10 SPI

The TQMa91xxCA provides in the TQ standard multiplexing a SPI interface, which can be operated in both master and slave mode.

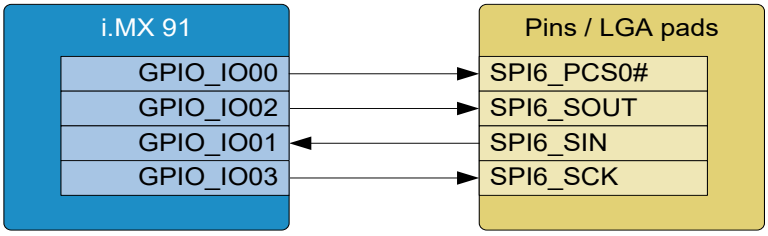


Figure 13: Block diagram SPI

Table 18: Pinning SPI

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| SPI6_PCS0# | J21 | X1-B46 | NVCC_GPIO (1.8 V / 3.3 V) |
| SPI6_SIN | J20 | X1-B47 | |
| SPI6_SOUT | K20 | X1-B48 | |
| SPI6_SCK | K21 | X1-B49 | |

#### 3.2.6.11 Tamper

As one of the safety functions of the BBSM unit of the i.MX 91, a total of two tamper signals are provided - one active and one passive. These are routed to the outside without any further circuitry.

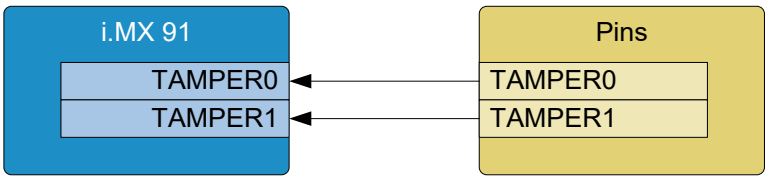


Figure 14: Block diagram Tamper

Table 19: Pinning Tamper

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| TAMPER0 | B16 | X2-A43 | NVCC_BBSM (1.8 V) |
| TAMPER1 | F14 | X2-A44 | |

#### 3.2.6.12 UART

In standard multiplexing five of eight possible UART interfaces are provided.
If less UARTs are required in customer applications, further interfaces, e.g. SPI or I2C, can be multiplexed at the same CPU pins.

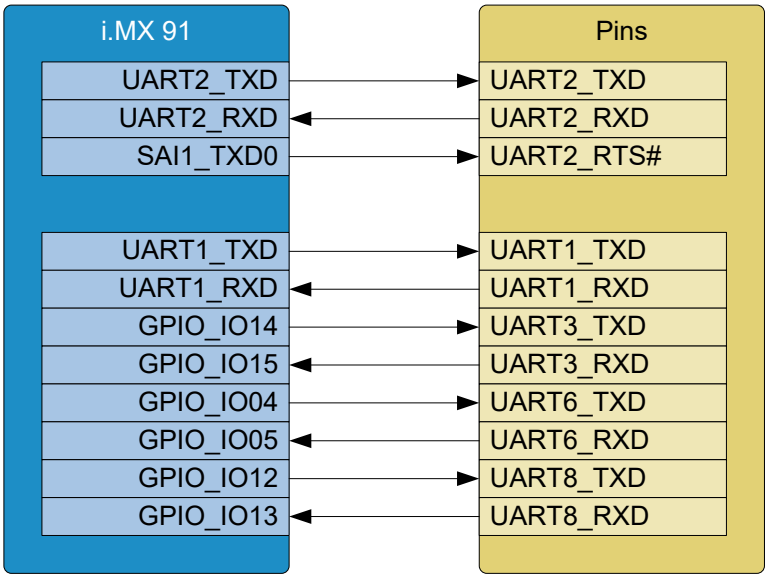


Figure 15: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces.

Table 20: UART signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| UART1_RXD | E20 | X2-A56 | NVCC_AON (3.3 V) |
| UART1_TXD | E21 | X2-A57 | |
| UART2_RXD | F20 | X2-A58 | |
| UART2_TXD | F21 | X2-A59 | |
| UART3_RXD | P21 | X1-A50 | NVCC_GPIO (1.8 V / 3.3 V) |
| UART3_TXD | P20 | X1-A49 | |
| UART6_RXD | L18 | X1-B40 | |
| UART6_TXD | L17 | X1-B41 | |
| UART8_RXD | N21 | X1-A47 | |
| UART8_TXD | N20 | X1-A46 | |

#### 3.2.6.13 USB

The i.MX 91 has two USB 2.0 OTG controllers, each providing device, host or OTG ports at high speed (480 Mbps). The OTG signals are not available by default because their multiplexing overlaps with the ENET1 interface.

Up to 5 V can be applied to the VBUS pins. The 30 kΩ resistors required by NXP are already provided on the module. The differential signals are length matched on the TQMa91xxCA and routed with a differential impedance of 90 Ω.

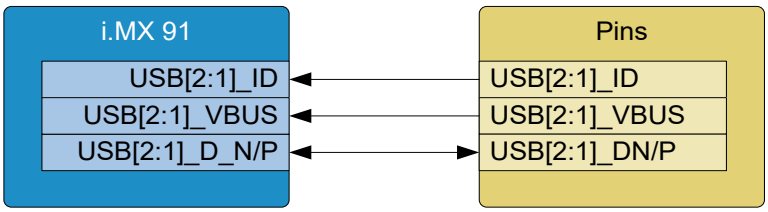


Figure 16: Block diagram USB interfaces

Table 21: USB signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| USB1_ID | C11 | X2-B43 | VDD_USB_1P8 (1.8 V) |
| USB2_ID | E12 | X2-B44 | |
| USB1_DN | A14 | X2-B57 | VDD_USB_3P3 (3.3 V) |
| USB1_DP | B14 | X2-B56 | |
| USB1_VBUS | F12 | X2-B47 | |
| USB2_DN | A15 | X2-B60 | |
| USB2_DP | B15 | X2-B59 | |
| USB2_VBUS | E14 | X2-B48 | |

#### 3.2.6.14 SD2 (SD-Card)

The i.MX 91 supports SD cards up to UHS-I in SDR104/DDR50 mode. This corresponds to SD card specification v3.0 and a maximum data width of 4 bit.

To enable booting from SD cards, the SD2 interface is routed to connector pins with the exception of SD2_VSELECT. SD2_RESET_B is available at a connector pin, but can remain unconnected because the actual reset function of this signal is already implemented on TQMa91xxCA.

The signals of the SD2 interface are supplied by a separate PMIC LDO whose IO voltage can be set to a 1.8 V or 3.3 V range by the signal SD2_VSELECT. SD2_VSELECT is automatically switched by the driver so that the fastest possible mode is used depending on the SD card used. The default setting at boot is 3.3 V.

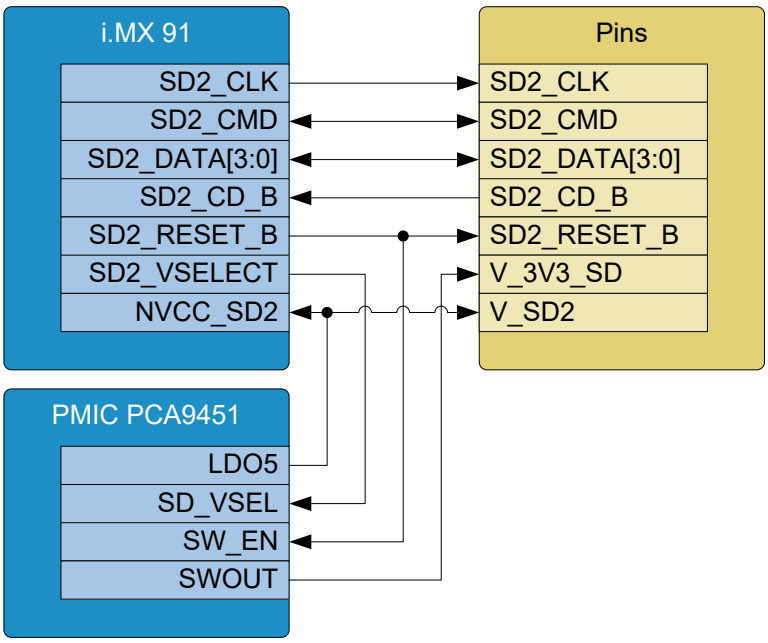


Figure 17: Block diagram SD card interface

Additionally the supply voltage V_SD2 is provided externally by the TQMa91xxCA. In customer designs this voltage can be used to connect the pull-up resistors of the SD card interface. Alternatively the use of CPU internal pull-up resistors is possible.

The voltage V_3V3_SD serves as main supply for SD cards. The TQMa91xxCA-internal wiring allows to interrupt the SD card supply at a module reset and thus to enable a reset of the SD card.

Table 22: SD2 signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| SD2_CD# | Y17 | X1-A20 | NVCC_SD2 (1.8 V / 3.3 V) |
| SD2_CLK | AA19 | X1-A17 | |
| SD2_CMD | Y19 | X1-A19 | |
| SD2_DATA0 | Y18 | X1-A22 | |
| SD2_DATA1 | AA18 | X1-A23 | |
| SD2_DATA2 | Y20 | X1-A24 | |
| SD2_DATA3 | AA20 | X1-A25 | |
| SD2_RST# | AA17 | X1-A27 | |

### 3.2.6.15 External clock sources

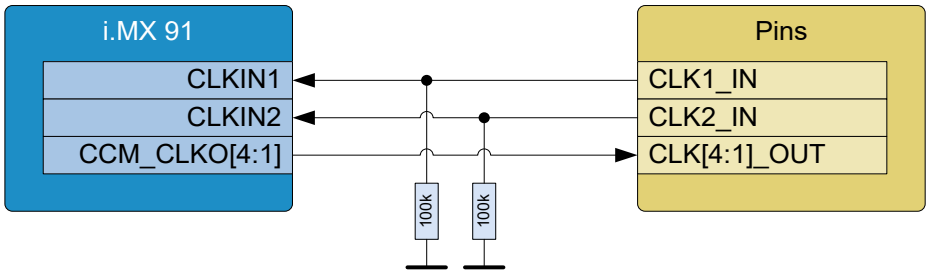


Figure 18: Block diagram external clocks

The i.MX 91 has the option to use two external oscillators as clock sources. Depending on the configuration of the internal clock tree, further reference clocks can be created.

All six i.MX 91 signals provided for this purpose are routed to TQMa91xxCA pins. The following table shows these clock signals.

Table 23: CLK signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| CLK1_IN[6] | B17 | X2-A46 | VDD_ANA_1P8 (1.8 V) |
| CLK2_IN[5] | A18 | X2-A47 | |
| CLK3_OUT[5] | U4 | X1-A8 | NVCC_WAKEUP (1.8 V) |

### 3.2.6.16 TPM / PWM

The TPM (Timer/PWM Module) of the i.MX 91 is a multi-channel timer that supports input capture, output compare, and the generation of PWM signals to control electrical motor and power management applications. The counter, compare, and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

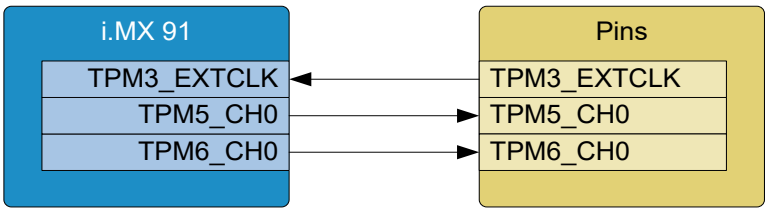


Figure 19: Block diagram TPM

[6] Default multiplexing

Table 24: TPM Signals

| Signal | i.MX 91 | TQMa91xxCA | Power group |
|---|---|---|---|
| TPM3_EXTCLK | M21 | X1-B52 | V_GPIO (1.8 V / 3.3 V) |
| TPM5_CH0 | L20 | X1-B43 | |
| TPM6_CH0 | M20 | X1-B53 | |

### 3.2.7 Reset and unspecific signals

Two reset options are provided by the TQMa91xxCA. A reset is triggered by the signal PMIC_RST#. This signal is fed to the PMIC from outside, is low-active and has an internal pull-up. By default, the PMIC is configured so that activation triggers a cold reset. The cold reset is a power cycle, with the exception of the LDO1 controller. The BBSM voltage is thus retained.

A second reset possibility is given by the signal PMIC_WDOG_IN#. This is a 3.3 V signal, which has a pull-up on the module. The corresponding PMIC behavior can be set via I2C. By default, a response to this signal is disabled.

The ONOFF pin of the CPU offers two reaction possibilities. It has an internal pull-up and is low-active. If this signal is held low for more than 5 s, the CPU enters OFF mode. If the signal is briefly pulled low in OFF mode, the CPU switches back to ON mode. A short low impuls in ON mode triggers an interrupt.

In addition, a module-internal supervisor triggers a reset when the module supply voltage drops.

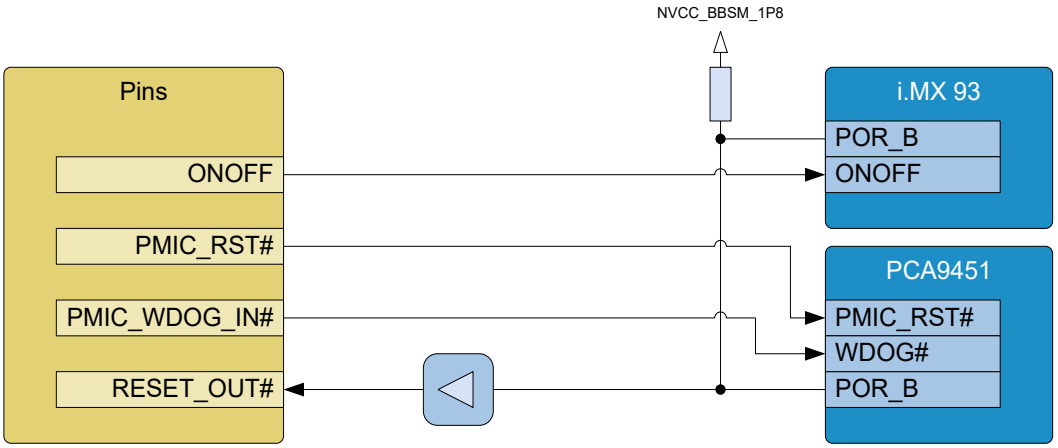


Figure 20: Block diagram Reset

RESET_OUT# is an open-drain output and is routed to a connector pin. In customer applications, this ensures feedback on a reset of the module to external components. In customer designs a pull-up is required at this output.

Table 25: Reset and unspecific signals

| Signal | i.MX 91 | Power group | Remark |
|---|---|---|---|
| PMIC_RST# | - | NVCC_BBSM (1.8 V) | • No pull-up on carrier board required; low-active.<br>• Programmable PMIC response (warm / cold reset). |
| ONOFF | [A19] ONOFF | | • ON/OFF function of the i.MX 91.<br>• No pull-up on carrier board required; low-active.<br>• Pull to GND for 5 s to activate. |
| RESET_OUT# | [A16] POR_B | | • Open drain output; low-active.<br>• Activates RESET of carrier board components.<br>• External pull-up required. |
| WDOG_ANY | [J18] WDOG_ANY | NVCC_AON (3.3 V) | |
| PMIC_WDOG_IN# | - | BUCK4 (3.3 V) | |
| RTC_EVENT# | - | Open Drain | |
| TEMP_EVENT# | - | | |

### 3.2.8 Power

#### 3.2.8.1 Power supply

The TQMa91xxCA requires a main supply voltage of 5 V ±5 %. All power supply and ground pins should be connected.

Through V_LICELL the TQMa91xxCA has an input for the backup voltage supply of the optional discrete RTC PCF85063A. Please refer to chapter 3.2.5.2

The characteristics and functions of a certain pin or signal is to be taken from the PMIC Data Sheet (4), and the i.MX 91 Data Sheet (2).

#### 3.2.8.2 Configurable voltages

V_GPIO must be powered by the baseboard to supply the CPU rail NVCC_GPIO. The required voltage is either 1.8 V (1.65…1.95 V) or 3.3 V (3.00…3.60 V).

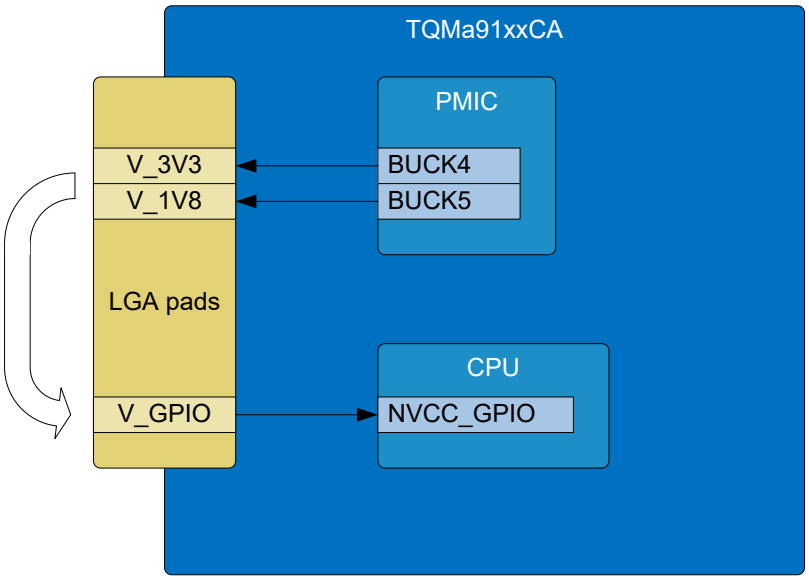


Figure 21: Possible power supply of the CPU-rail NVCC_GPIO

| Attention: Destruction or malfunction | |
|---|---|
|  | If V_GPIO is not connected to a power supply the corresponding CPU-Rail is not powered. This can cause malfunction or damage the CPU. |

#### 3.2.8.3 Power consumption

The given power consumption has to be seen as an approximate value.

The TQMa91xxCA power consumption strongly depends on the application, the mode of operation and the operating system.

The following table shows TQMa91xxCA power supply and power consumption parameters:

Table 26: Power consumption

| Mode of operation | Current @ 5 V | Power consumption @ 5 V |
|---|---|---|
| Theoretical calculated peak (worst case) | TBD | TBD |
| U-Boot prompt | TBD | TBD |
| Linux prompt | TBD | TBD |
| Linux stress test | TBD | TBD |
| Reset | TBD | TBD |

#### 3.2.8.4 Voltage monitoring

The TQMa91xxCA features a supervisor that monitors the input voltage ($V_{IN}$).

If the input voltage drops below 4.38 V, a Reset (PMIC_ON_REQ) is triggered and the TQMa91xxCA is held in reset until the input voltage is in the permitted range again.

| Attention: Destruction or malfunction, supply voltage exceedance | |
|---|---|
|  | The voltage monitoring does not detect an exceedance of the permitted input voltage.<br>An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa91xxCA. |

#### 3.2.8.5 Supply outputs

The TQMa91xxCA provides three voltages that can be used on the carrier board.

Table 27: Voltages provided by TQMa91xxCA

| Voltage | TQMa91xxCA | Usage | Max. load |
|---|---|---|---|
| V_1V8 | X1-A34 | General usage on carrier board | 500 mA |
| V_3V3 | X1-A33 | General usage on carrier board | 500 mA |
| V_3V3_SD | X1-A31 | SD card supply | 400 mA |

The voltage V_3V3 can be used as Power-Good signal for the supply of circuitry on the carrier board.

| Attention: Destruction or malfunction, current exceedance | |
|---|---|
|  | A load of up to 500 mA at V_1V8 or V_3V3, as well as up to 400 mA at V_3V3_SD causes an increased power consumption of the TQMa91xxCA and thus a higher self-heating.<br>These three voltages are outputs and must never be supplied from external sources!<br>Furthermore, the outputs are not short-circuit proof. Overloading the voltage outputs can damage the TQMa91xxCA. |

#### 3.2.8.6 Power-Up sequence TQMa91xxCA / carrier board

As the TQMa91xxCA operates with 5 V and the I/O voltages of the CPU signals are generated on the TQMa91xxCA, there are timing requirements for the carrier board design with respect to the voltages generated on the carrier board:

After power up of the 5V supply for the TQMa91xxCA, the PMIC power-up sequence starts. External TQMa91xxCA inputs driven by the carrier board may only be switched on after the power-up of V_3V3. Connector pin X1-A33 (V_3V3) can be used as feedback.

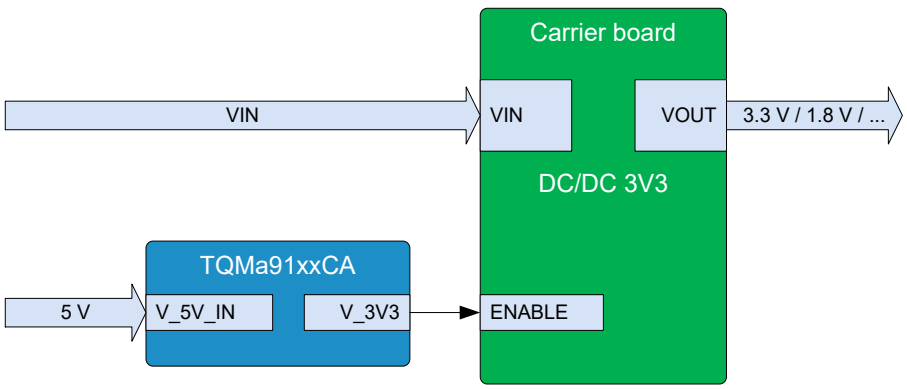


Figure 22: Block diagram power supply of carrier board

| Attention: Destruction or malfunction, Power-Up sequence | |
|---|---|
|  | To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed.<br>The end of the power-up sequence is indicated by a high level of signal V_3V3, connector pin X1-A33. |

#### 3.2.8.7 Standby and BBSM

In standby mode, several voltage controllers on the TQMa91xxCA are switched off.
The rail V_1V8_BBSM remain active, which ensures the correct function of the BBSM.

#### 3.2.8.8 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX 91 Reference Manual (1) and the PMIC Data Sheet (4). The PMIC is controlled by the I2C1 bus.

- The PMIC has I²C address `0x25 / 010 0101b`

The following PMIC and power management signals are available on the TQMa91xxCA connector pins

Table 28: PMIC signals

| Signal | Direction | TQMa91xxCA | Power group | Remark |
|---|---|---|---|---|
| PMIC_WDOG_IN# | I | X2-A49 | 3.3 V | • Low-active input |
| PMIC_RST# | I | X1-B36 | 1.8 V | • Low-active input |
| RESET_OUT# | O | X1-B37 | 1.8 V | • Low-active output<br>• Connected to PMIC POR#<br>• Can signal a TQMa91xxCA reset |
| SD_VSEL | – | – | – | • See chapter 3.2.6.16 |

| Attention: Destruction or malfunction, PMIC programming | |
|---|---|
|  | Improper programming of the PMIC may result in the i.MX 91 or periphery being operated outside its specification. This may lead to malfunctions, accelerated aging or destruction of the TQMa91xxCA. |

### 3.2.9 Impedances

By default, all single-ended signals have a nominal impedance of 50 Ω ±10 %.
However, some interfaces on the TQMa91xxCA are routed with different impedances, depending on the signal requirements.

The following table is taken from the Hardware Developer's Guide (3) and shows the respective interfaces:

Table 29: Trace impedance recommendations

| Signal / Interface | Impedance on TQMa91xxCA | Recommendation for carrier board |
|---|---|---|
| DDR DQS/CLK | 85 Ω, differential | 85 Ω ±10 %, differential |
| Differential USB signals | 90 Ω, differential | 90 Ω ±10 %, differential |
| Differential signals, including Ethernet | 100 Ω, differential | 100 Ω ±10 %, differential |

# 4. SOFTWARE

The TQMa91xxCA is delivered with a preinstalled boot loader U-Boot.
The BSP provided by TQ-Systems GmbH is configured for the combination of TQMa91xxCA and MBa91xxCA.
The boot loader U-Boot provides TQMa91xxCA-specific as well as board-specific settings, e.g.:

- i.MX 91 configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

Further information can be found in the https://support.tq-group.com/TQMa91xxCA.

If another bootloader is used, this data must be adapted. Contact TQ-Support for detailed information.

# 5. MECHANICS

## 5.1 Dimensions

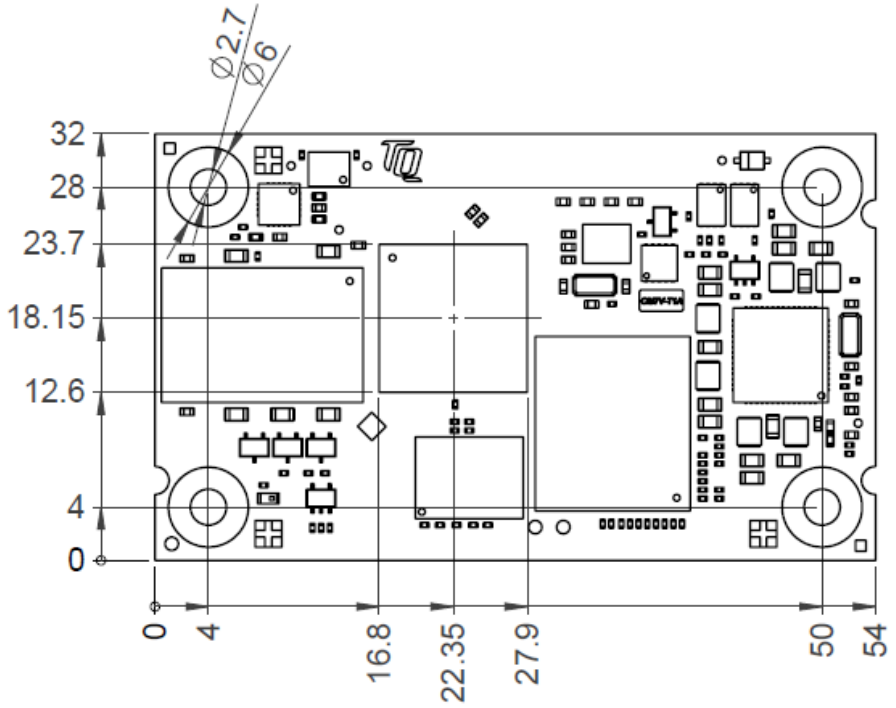


Figure 23: TQMa91xxCA dimensions, top view (dimensions in mm)

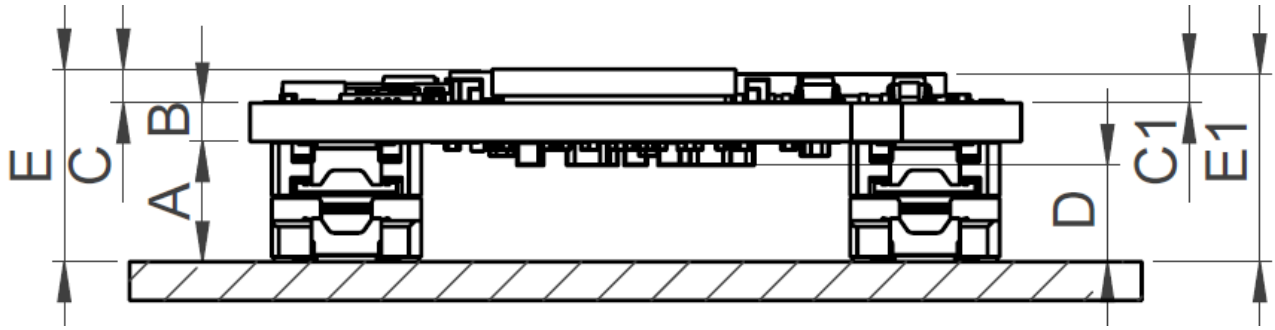


Figure 24: TQMa91xxCA dimensions, side view

Table 30: TQMa91xxCA heights

| Dim. | Value | Tolerance | Remark |
|---|---|---|---|
| A | 5.10 mm | +0.07 mm | Board to board distance |
| B | 1.60 mm | ±0.16 mm | PCB without solder resist |
| C | 1.05 mm | ±0.10 mm | Height of CPU |
| C1 | 1.08 mm | ±0.06 mm | Height of NOR Flash |

| Dim. | Value | Tolerance | Remark |
|---|---|---|---|
| D | 4.25 mm | ±0.21 mm | Space below module |
| E | 7.75 mm | ±0.20 mm | Overall height to CPU surface |
| E1 | 7.78 mm | ±0.18 mm | Overall height to NOR Flash |

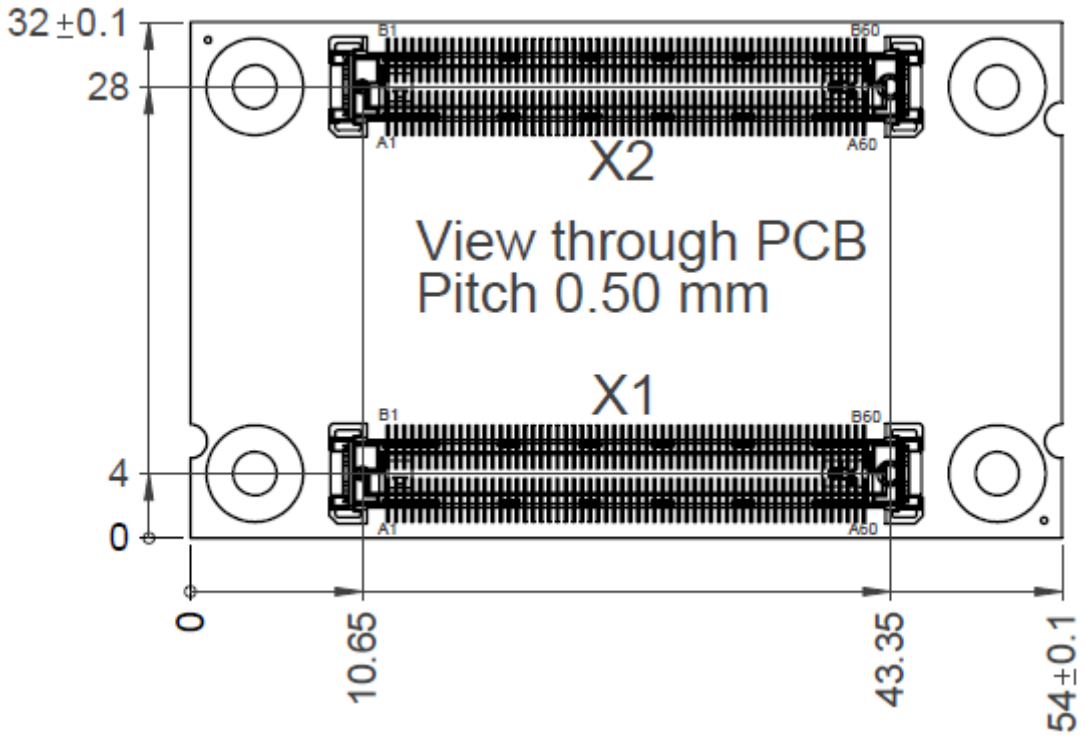


Figure 25: TQMa91xxCA dimensions (in mm), view through PCB

## 5.2 Component placement and labeling

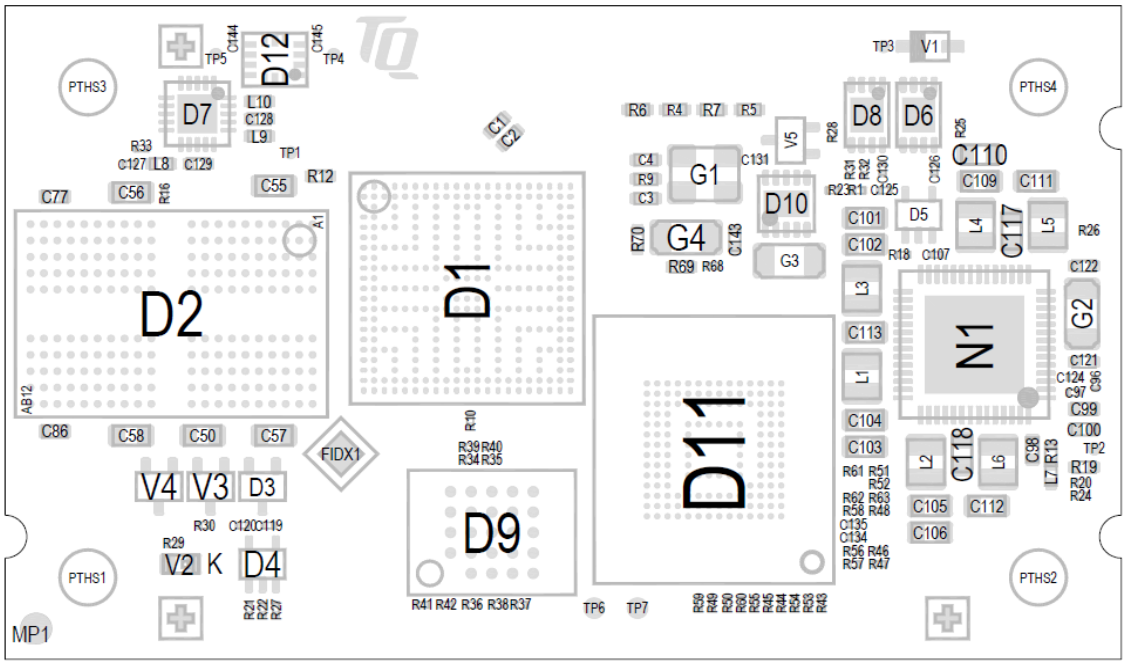


Figure 26: TQMa91xxCA, component placement top

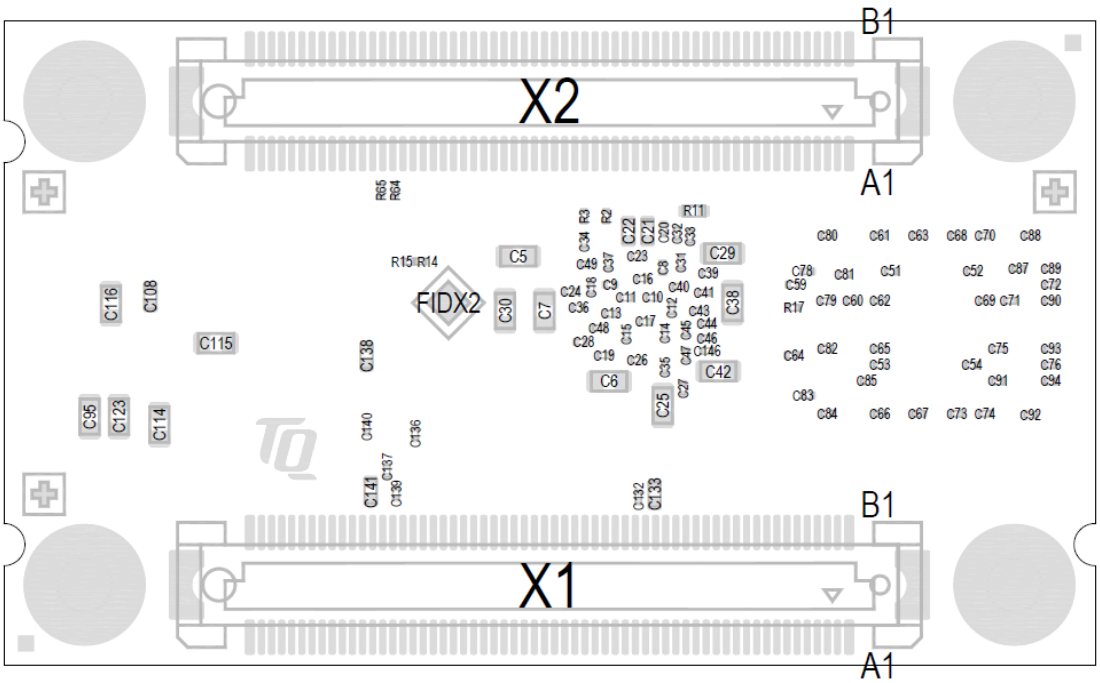


Figure 27: TQMa91xxCA, bottom view

The labels on the TQMa91xxCA show the following information:

Table 31: Labels on TQMa91xxCA

| Label | Content |
|---|---|
| AK1 | Serial number |
| AK2 | MAC address |
| AK3 | TQMa91xxCA version and revision |

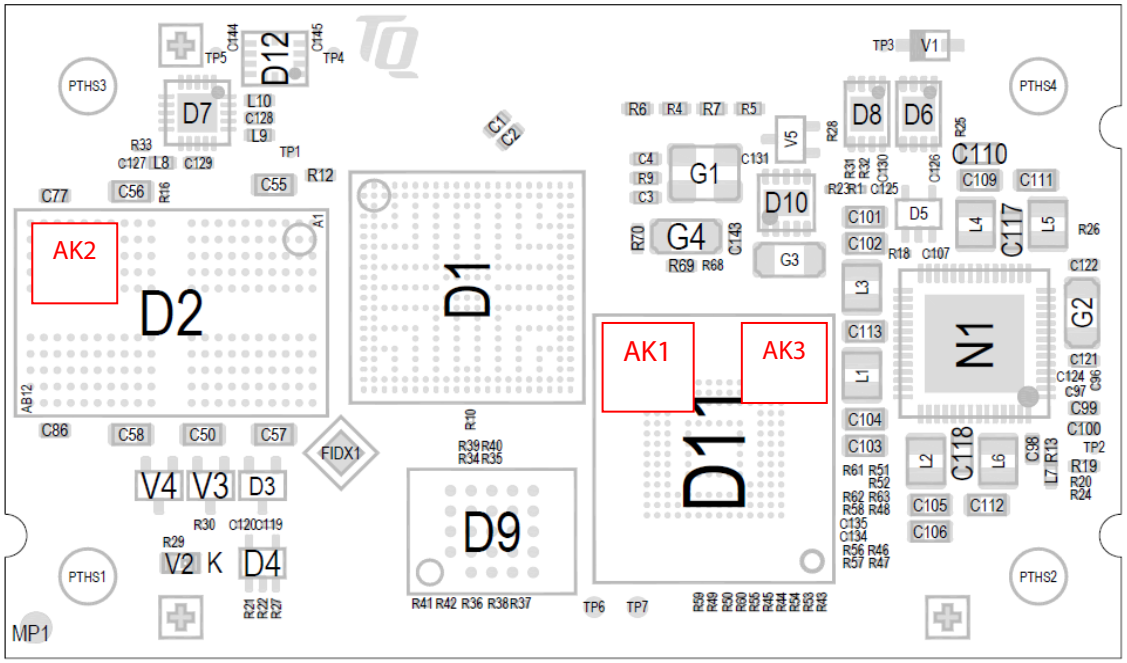


Figure 28: Labels on TQMa91xxCA

## 5.3 Adaptation to the environment

The TQMa91xxCA has overall dimensions (length × width) of 32 mm × 54.0 mm (± 0.1 mm).
The TQMa91xxCA has a maximum height above the carrier board of approximately 7.78 mm (± 0.18 mm).
The TQMa91xxCA has two 120-pin connectors (240 pins in total) with a pitch of 0.50 mm.
The TQMa91xxCA weighs approximately 11 g.

## 5.4 Protection against external effects

The TQMa91xxCA does not provide protection against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

## 5.5 Thermal management

To cool the TQMa91xxCA, note Table 27. The power dissipation originates primarily in the i.MX 91, the LPDDR4 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (6) and (7) for further information.

| Attention: Destruction or malfunction, TQMa91xxCA cooling | |
|---|---|
|  | The i.MX 91 belongs to a performance category in which a cooling system is essential.<br>It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).<br>Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 91 must be taken into consideration when connecting the heat sink, see (6). The i.MX 91 is not necessarily the highest component.<br>Inadequate cooling connections can lead to overheating of the TQMa91xxCA and thus malfunction, deterioration or destruction. |

## 5.6 Structural requirements

The TQMa91xxCA is held in the mating connectors by the retention force of the pins (240). For high requirements with respect to vibration and shock firmness, an additional retainer has to be provided in the final product to hold the TQMa91xxCA in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

# 6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

## 6.1 EMC

The TQMa91xxCA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

## 6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa91xxCA.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

## 6.3 Shock and Vibration

Table 32: Shock resistance

| Parameter | Details |
|---|---|
| Shock | According to DIN EN 60068-2-27 |
| Shock form | Half sine |
| Acceleration | 30 g |
| Residence time | 10 ms |
| Number of shocks | 3 shocks per direction |
| Excitation axes | 6X, 6Y, 6Z |

Table 33: Vibration resistance

| Parameter | Details |
|---|---|
| Oscillation, sinusoidal | According to DIN EN 60068-2-6 |
| Frequency ranges | 2 ~ 9 Hz, 9 ~ 200 Hz, 200 ~ 500 Hz |
| Wobble rate | 1.0 octaves / min |
| Excitation axes | X– Y – Z axis |
| Acceleration | 2 Hz to 9 Hz: 3.5 $m/s^2$<br>9 Hz to 200 Hz: 10 $m/s^2$<br>200 Hz to 500 Hz: 15 $m/s^2$ |

## 6.4 Climate and operational conditions

The TQMa91xxCA is available in different variants with different ambient temperature ranges. The operating temperature range for the TQMa91xxCA strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa91xxCA.

In general, a reliable operation is given when following conditions are met:

Table 34: Climate and operational conditions

| Parameter | | Range | Remark |
|---|---|---|---|
| Ambient temperature TQMa91xxCA | Standard | –25 °C to +85 °C | – |
| | Extended | –40 °C to +85 °C | – |
| $T_J$ temperature i.MX 91 | | –40 °C to +105 °C | – |
| $T_J$ temperature PMIC | | –40 °C to +125 °C | – |
| Case temperature LPDDR4 | | –40 °C to +95 °C | – |
| Case temperature other ICs | Standard | –25 °C to +85 °C | – |
| | Extended | –40 °C to +85 °C | – |
| Storage temperature TQMa91xxCA | | –40 °C to +100 °C | – |
| Relative humidity (operating / storage) | | 10 % to 90 % | Not condensing |

Detailed information concerning the i.MX 91 thermal characteristics is to be taken from NXP documents (6) and (7).

| Attention: Destruction or malfunction, TQMa91xxCA cooling | |
|---|---|
|  | The i.MX 91 belongs to a performance category in which a cooling system is essential.<br>It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).<br>Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 91 must be taken into consideration when connecting the heat sink, see (6). The i.MX 91 is not necessarily the highest component.<br>Inadequate cooling connections can lead to overheating of the TQMa91xxCA and thus malfunction, deterioration or destruction. |

## 6.5 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa91xxCA is only a sub-component of an overall system.

## 6.6 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

## 6.7 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

## 6.8 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

## 6.9 Reliability and service life

The MTBF calculated for the TQMa91xxCA is 1,107,304 hours with a constant error rate @ +40 °C, Ground Benign. The TQMa91xxCA is designed to be insensitive to shock and vibration.

The TQMa91xxCA must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.

Detailed information concerning the i.MX 91 service life under different operational conditions is to be taken from the NXP Application Note (7).

# 7. ENVIRONMENT PROTECTION

## 7.1 RoHS

The TQMa91xxCA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

## 7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa91xxCA was designed to be recyclable and easy to repair.

## 7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

## 7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa91xxCA always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa91xxCA on account of available Standby or Sleep-Modes of the components on the TQMa91xxCA.

## 7.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

## 7.6 Battery

No batteries are assembled on the TQMa91xxCA.

## 7.7 Packaging

The TQMa91xxCA is delivered in reusable packaging.

## 7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa91xxCA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa91xxCA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)

- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

# 8. APPENDIX

## 8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 35: Acronyms

| Acronym | Meaning |
|---|---|
| ARM® | Advanced RISC Machine |
| BBSM | Battery Backed Secure Module |
| BGA | Ball Grid Array |
| BIOS | Basic Input/Output System |
| BSP | Board Support Package |
| CAN | Controller Area Network |
| CAN-FD | CAN with Flexible Data-Rate |
| CPU | Central Processing Unit |
| CSI | CMOS Sensor Interface |
| DDR | Double Data Rate |
| DIN | Deutsche Industrienorm (German industry standard) |
| DNC | Do Not Connect |
| DSI | Display Serial Interface |
| EARC | Enhanced Audio Return Channel |
| ECSPI | Enhanced Configurable SPI |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| EMC | Electromagnetic Compatibility |
| eMMC | embedded Multimedia Card (Flash) |
| EN | Europäische Norm (European standard) |
| ESD | Electrostatic Discharge |
| EuP | Energy using Products |
| FR-4 | Flame Retardant 4 |
| Gbps | Gigabit per second |
| GPIO | General Purpose Input/Output |
| GPT | General-Purpose Timer |
| HDMI | High-Definition Multimedia Interface |
| I | Input |
| I/O | Input/Output |
| $I^2C$ | Inter-Integrated Circuit |
| IP00 | Ingress Protection 00 |
| IPU | Input with Pull-Up |
| JEDEC | Joint Electronic Device Engineering Council |
| JTAG® | Joint Test Action Group |
| LGA | Land Grid Array |
| LPDDR4 | Low Power DDR4 |
| LVDS | Low-Voltage Differential Signaling |
| MAC | Media Access Control |
| MIPI | Mobile Industry Processor Interface |
| ML/AI | Machine Learning / Artificial Intelligence |
| MMC | Multimedia Card |
| MTBF | Mean operating Time Between Failures |

## 8.1 Acronyms and definitions (continued)

Table 36: Acronyms (continued)

| Acronym | Meaning |
|---|---|
| NAND | Not-And |
| NOR | Not-Or |
| O | Output |
| OD | Open Drain |
| OOD | Output with Open Drain |
| OTG | On-The-Go |
| P | Power |
| PCB | Printed Circuit Board |
| PCIe | Peripheral Component Interconnect Express |
| PD | Pull-Down (resistor) |
| PHY | Physical (layer of the OSI model) |
| PMIC | Power Management Integrated Circuit |
| PU | Pull-Up (resistor) |
| PWM | Pulse-Width Modulation |
| PWP | Permanent Write Protected |
| QSPI | Quad Serial Peripheral Interface |
| RAM | Random Access Memory |
| RC | Resistor-Capacitor |
| REACH® | Registration, Evaluation, Authorisation (and restriction of) Chemicals |
| RF | Radio Frequency |
| RGMII | Reduced Gigabit Media Independent Interface |
| RMII | Reduced Media Independent Interface |
| RoHS | Restriction of (the use of certain) Hazardous Substances |
| ROM | Read-Only Memory |
| RTC | Real-Time Clock |
| RWP | Reversible Write Protection |
| SAI | Serial Audio Interface |
| SCU | System Control Unit |
| SD | Secure Digital |
| SDRAM | Synchronous Dynamic Random Access Memory |
| SNVS | Secure Non-Volatile Storage |
| SPDIF | Sony-Philips Digital Interface Format |
| SPI | Serial Peripheral Interface |
| SVHC | Substances of Very High Concern |
| TBD | To Be Determined |
| TSE | Trust Secure Element |
| UART | Universal Asynchronous Receiver/Transmitter |
| UM | User's Manual |
| USB | Universal Serial Bus |
| uSDHC | Ultra-Secured Digital Host Controller |
| WEEE® | Waste Electrical and Electronic Equipment |
| WP | Write-Protection |

## 8.2 References

Table 36: Further applicable documents

| No. | Name | Rev., Date | Company |
|---|---|---|---|
| (1) | i.MX 91 Applications Processor Reference Manual | TBD | NXP |
| (2) | i.MX 91 Application Processors Data Sheet | Rev. 1 Draft F, Sep 2023 | NXP |
| (3) | i.MX 91 Hardware Developer's Guide | TBD | NXP |
| (4) | Power management IC for i.MX 91 application processor | TBD | NXP |
| (5) | i.MX 91 Mask Set Errata | TBD | NXP |
| (6) | i.MX 91 Power Consumption Measurement | TBD | NXP |
| (7) | i.MX 91 Product Lifetime Usage | TBD | NXP |
| (8) | SE050 Trust Secure Element Data Sheet | Rev. 3.1, Dec 2020 | NXP |
| (9) | MBa91xxCA User's Manual | – current – | TQ-Systems |
| (10) | TQMa91xxCA Support-Wiki | – current – | TQ-Systems |
| (11) | TQMa91xxCA Processing instructions | – current – | TQ-Systems |

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