TQMa8Xx & TQMa8Xx4
User's Manual

TQMa8Xx UM 0110
07.07.2022

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	08.02.2021	Petz		Initial release
0101	14.02.2021	Petz	All Table 4 Table 6 Figure 10 3.1.22 3.2.1.3 Table 30 Figure 22, Figure 24, Figure 25 Figure 27, Figure 28, Figure 29 Figure 30 Table 38 Footnote 21	Non-functional changes, expressions, phrases “PU” added to “Dir.” of X2-25 Updated, I^2C devices added Updated and clarified Signal name MCLK_OUT ⇨ MCLK_OUT0 corrected Signal name PMIC_POR# ⇨ IMX_POR# corrected ECC configurations corrected Signal names clarified PU moved to signal PMIC_ON_REQ “PU” added to “Dir.” of signal PMIC_PGOOD Updated
0102	23.02.2021	Petz	All 2, 2.1, 2.2 Table 4 Table 5, Table 25 Table 11, Table 44, Table 45 Table 56	Non-functional changes, expressions, phrases Note added, restructured and reworked Level of RESET_IN# changed to 5.0 V Signal names TAMPER_IN3 / TAMPER_IN4 swapped Superfluous information removed T_J PMIC corrected
0103	16.03.2021	Petz	All	Damaged chapter structure restored
0104	23.03.2021	Petz	Table 42	Updated, values for TQMa8Xx4 added
0105	18.10.2021	Kreuzer	3.5.1	Copy/Paste failure removed
0106	19.01.2022	Kreuzer	All 4.4 Table 40 Table 42 Table 4 Figure 6 Figure 17 Figure 35, Figure 36	Non-functional changes, expressions, phrases TQMa8Xx4 weight added Remarks revised Table revised Level of RESET_IN# changed to 1.8 V M4_I2C pin assignment corrected TAMPER_IN3 / 4 swapped Module variants swapped
0107	10.02.2022	Kreuzer	Figure 6	Missing signal names added
0108	13.4.2022	Kreuzer	Table 3 Table 4 3.2.13 Figure 14 Table 21 Table 22 Table 58	Pin 71 USB_OTG1_ID level changed to 1.8V Pin 54 PMIC_AMUX_VSD changed to Power; Level added PMIC_AMUX_VSD explained PMIC_AMUX_VSD added PMIC_AMUX_VSD added USB_OTG1_ID changed to 1.8 V Updated
0109	27.4.2022	Kreuzer	Table 42	Footnotes added
0110	07.07.2022	Kreuzer	3.2.4	Assembly option added

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa8Xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8Xx schematics
- MBa8Xx User's Manual
- i.MX 8X Data Sheet
- i.MX 8X Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8Xx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa8Xx ≥ rev. 0300 and of the TQMa8Xx4 ≥ rev. 0100, in combination with the MBa8Xx ≥ rev. 0200 and refers to some software settings.

This User's Manual does neither replace the i.MX 8X Reference Manual (2), nor the i.MX 8X Data Sheet (1), nor any other documents from NXP.

Note: Designations "TQMa8Xx" and "TQMa8Xx4", available features and interfaces	
	In order to facilitate the readability of this User's Manual, the designation "TQMa8Xx" is used throughout. If technical aspects require a differentiation between "TQMa8Xx" and "TQMa8Xx4", the appropriate designation is used. This User's Manual describes all features and interfaces provided by the TQMa8Xx and TQMa8Xx4. A certain TQMa8Xx or TQMa8Xx4 derivative does not necessarily provide all features and interfaces described in this User's Manual.

The TQMa8Xx is a universal TQ-Minimodule based on NXP ARM® Cortex®-A35 i.MX 8X CPU series, see also Table 28.

The MBa8Xx serves as an evaluation platform for the TQMa8Xx.

The CPU derivatives provide Dual, and Quad ARM® Cortex®-A35 cores, and up to two Dual ARM® Cortex®-M4 co-processors.

In addition, the CPUs include an OpenGL ES 3.0 or 3.1 GPU as well as a VPU, supporting up to 4K h.265 decoder.

An i.MX 8X Cortex®-A35 core typically operates at 1.2 GHz.

2.1 Block diagram i.MX 8X

The TQMa8Xx extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX 8X derivative (i.MX 8DualX, i.MX 8DualXPlus or i.MX 8QuadXPlus) can be selected for each requirement.

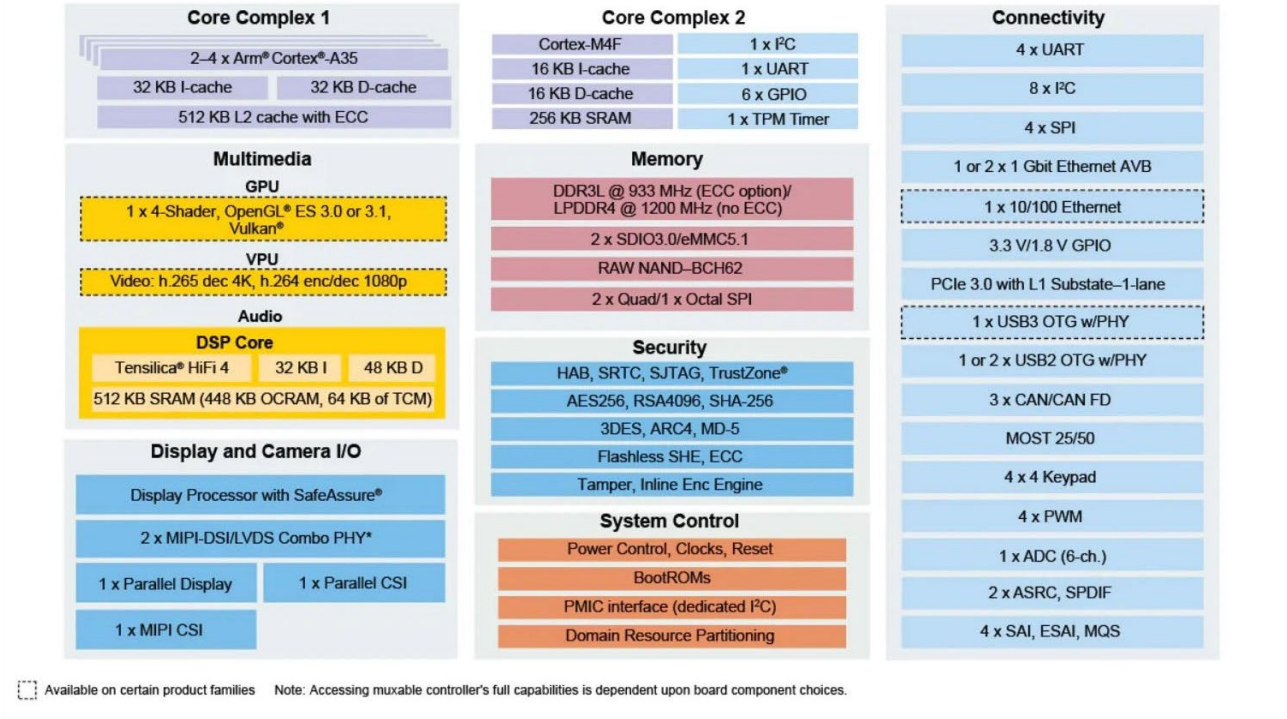


Figure 1: Block diagram i.MX 8X CPU
(Source: NXP)

2.2 Key functions and characteristics

All essential CPU signals are routed to the connectors. There are therefore no restrictions for customers using the TQMa8Xx with respect to an integrated customised design.
All essential components like CPU, DDR3L SDRAM (TQMa8Xx) or LPDDR4 SDRAM (TQMa8Xx4), eMMC, and power management are already integrated on the TQMa8Xx.
The main features of the TQMa8Xx are:

- 64-bit NXP i.MX 8X CPU with up to 4 × ARM® Cortex®-A35 and 1 × ARM® Cortex®-M4F
- Derivatives: i.MX 8DualX / i.MX 8DualXPlus / i.MX 8QuadXPlus
- TQMa8Xx: Up to 2 Gbyte DDR3L SDRAM with 2 × 16 bit data bus interface, optional one channel with ECC
- TQMa8Xx4: Up to 4 Gbyte LPDDR4 SDRAM with 1 × 32 bit data bus interface
- Up to 64 Gbyte eMMC NAND flash
- Up to 256 Mbyte QSPI NOR flash
- RTC
- Trust Secure Element
- 64 Kbit EEPROM
- EEPROM + temperature sensor
- NXP PMIC, “ASIL B” ready
- All essential CPU signals are routed to the TQMa8Xx connectors
- Extended temperature range
- Boot mode selection on TQMa8Xx
- 3.3 V single supply voltage

The i.MX 8X processor family used on the TQMa8Xx and TQMa8Xx4 TQ-Minimodules has a high level of integration to support graphics, video, image processing and audio applications and is ideal for safety-related and power-efficient requirements.
This results in the most diverse application areas, for example in the fields of industrial automation & control, HMI, robotics, building control, infotainment and telematics.
Full access to all signal pins on the TQMa8Xx connectors guarantees flexible applications and cost-efficient project development.
The following components are typically present on the TQMa8Xx:

- NXP CPU i.MX 8DualX or i.MX 8DualXPlus or i.MX 8QuadXPlus
- DDR3L SDRAM + optional ECC on TQMa8Xx, LPDDR4 SDRAM onTQMa8Xx4, no ECC
- PCIe clock generator (optional on TQMa8Xx4)
- eMMC NAND flash 5.1 (optional)
- QSPI NOR flash (optional)
- EEPROM (optional)
- EEPROM + Temperature sensor
- Trust Secure Element (optional)
- RTC (optional)
- Power Management Controller PMIC PF8100
- Three connectors (2 × 120 pins, 1 × 40 pins)

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa8Xx, and the BSP provided by TQ-Systems, see also chapter 5.

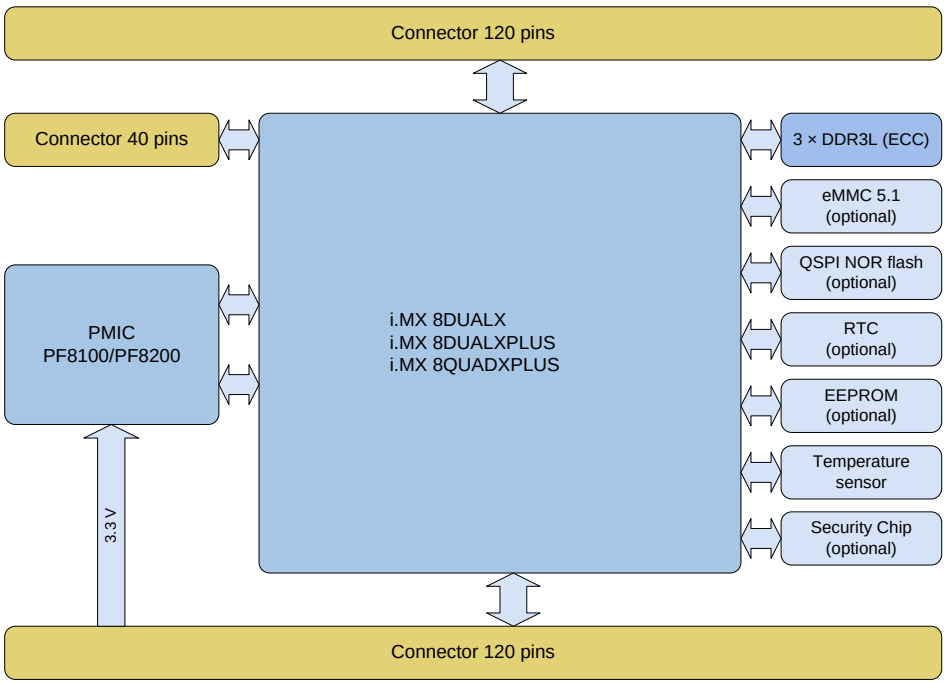


Figure 2: Block diagram TQMa8Xx

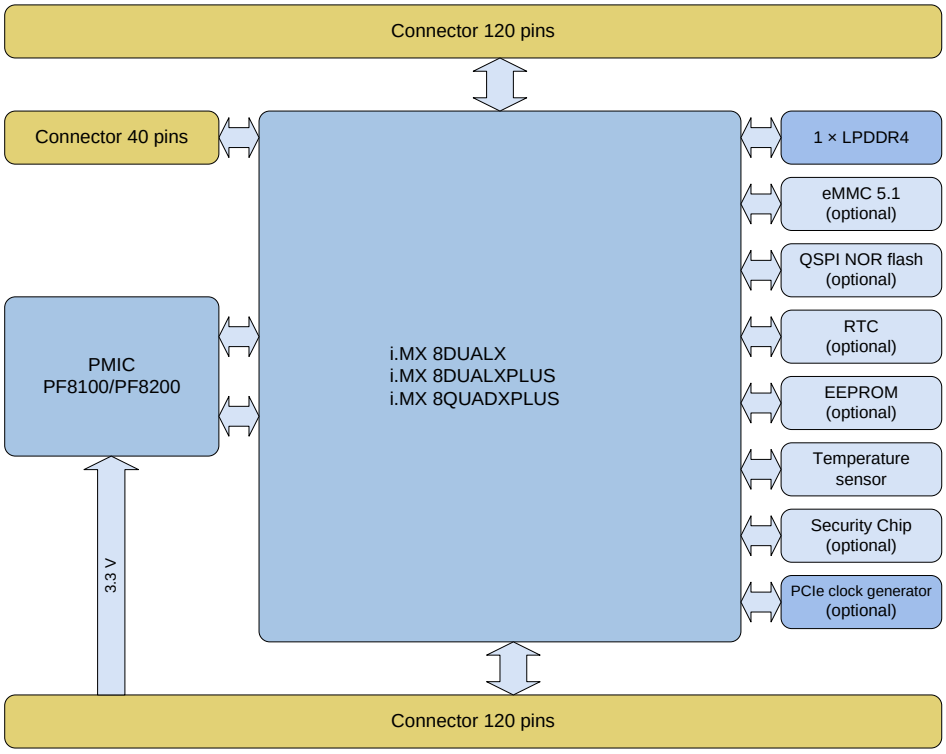


Figure 3: Block diagram TQMa8Xx4

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of.
NXP provides a tool showing the multiplexing and simplifies the selection and configuration (NXP Pin Mux Tool):
The pin assignment in Table 3 to Table 5 refers to the BSP provided by TQ-Systems in combination with the MBa8Xx.
The electrical and pin characteristics are to be taken from the i.MX 8X Data Sheet (1), the i.MX 8X Reference Manual (2), and the PMIC Data Sheet (4).

Attention: Destruction or malfunction, TQMa8Xx pin multiplexing	
	Depending on the configuration, many i.MX 8X balls can provide several different functions. Please take note of the information in the i.MX 8X Reference Manual (2), and the i.MX 8X Errata (3) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa8Xx. Some connector pins have manufacturer-specific functions. These are marked with DNC and must not be connected on the carrier board.

3.1.2 Impedances

By default, all signals have a single-ended impedance of nominal 50 Ω ±10 %.
Depending on the interface, other impedances are also used on the TQMa8Xx.
The following table shows the affected interfaces:

Table 2: Impedances

Signal / interface	Impedance TQMa8Xx	Recommendation for carrier board
PCIe	90 Ω differential	85 Ω ±15 % differential
MIPI CSI	100 Ω differential	100 Ω ±10 % differential [1]
MIPI DSI	100 Ω differential	100 Ω ±10 % differential [1]
USB OTG1 / OTG2	90 Ω differential	90 Ω ± 15 % differential [2]
USB SS 3.0 (only differential signals)	90 Ω differential	90 Ω ± 7 Ω differential [3]

1: See i.MX 8QuadMax/i.MX 8QuadXPlus Hardware Developer's Guide, Revision 1.0.
2: See Universal Serial Bus Specification, Revision 2.0.
3: See Universal Serial Bus 3.0 Specification, Revision 1.0.

3.1.3 TQMa8Xx pinout

Table 3: Pinout TQMa8Xx X1

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	–	0 V	Ground	GND	1	2	GND	Ground	0 V	–	–
E35	O	V_ENET [4]	ENET	ENET1_REFCLK_OUT [5]	3	4	TEMP_EVENT#	CONFIG	–	O_{OD} [6]	–
–	–	0 V	Ground	GND	5	6	GND	Ground	0 V	–	–
D32	I	V_ENET [4]	ENET	ENET1_RXC [5]	7	8	ENET1_TXC [5]	ENET	V_ENET [4]	O	F30
–	–	0 V	Ground	GND	9	10	GND	Ground	0 V	–	–
D34	I	V_ENET [4]	ENET	ENET1_RX_CTL [5]	11	12	ENET1_TX_CTL [5]	ENET	V_ENET [4]	O	H28
G31	I	V_ENET [4]	ENET	ENET1_RXD0 [5]	13	14	ENET1_TXD0 [5]	ENET	V_ENET [4]	O	F32
C33	I	V_ENET [4]	ENET	ENET1_RXD1 [5]	15	16	ENET1_TXD1 [5]	ENET	V_ENET [4]	O	J29
K28	I	V_ENET [4]	ENET	ENET1_RXD2 [5]	17	18	ENET1_TXD2 [5]	ENET	V_ENET [4]	O	G29
B34	I	V_ENET [4]	ENET	ENET1_RXD3 [5]	19	20	ENET1_TXD3 [5]	ENET	V_ENET [4]	O	E31
–	–	0 V	Ground	GND	21	22	GND	Ground	0 V	–	–
P34	I/O	V_IO [7]	M4 GPIO	M4_GPIO0_IO02	23	24	GPIO0_IO30	GPIO	V_IO [7]	I/O	L35
R33	I/O	V_IO [7]	M4 GPIO	M4_GPIO0_IO03	25	26	GPIO0_IO31	GPIO	V_IO [7]	I/O	N35
R31	I/O	V_IO [7]	M4 I2C	M4_I2C_SDA	27	28	GPIO1_IO07	GPIO	V_IO [7]	I/O	R35
P30	I/O	V_IO [7]	M4 I2C	M4_I2C_SCL	29	30	PMIC_PGOOD	CONFIG	1.8 V	O_{OD}	–
–	I_{PU}	1.8 V	CONFIG	PMIC_WDI	31	32	GND	Ground	0 V	–	–
H34	O	V_IO [7]	UART	UART1_TX	33	34	SPI2_SCK	SPI	1.8/3.3 V [7]	O	R29
L31	I	V_IO [7]	UART	UART1_RX	35	36	SPI2_SDO	SPI	1.8/3.3 V [7]	O	P32
N29	O	V_IO [7]	UART	UART1_RTS#	37	38	SPI2_SDI	SPI	1.8/3.3 V [7]	I	N31
K32	I	V_IO [7]	UART	UART1_CTS#	39	40	SPI2_CS0	SPI	1.8/3.3 V [7]	O	P28
–	–	0 V	Ground	GND	41	42	SPI1_CS0	SPI	1.8/3.3 V [7]	O	M34
D30	O	V_ENET [4]	ENET	ENET0_MDC	43	44	SPI1_CS1	SPI	1.8/3.3 V [7]	O	M32
B32	I/O	V_ENET [4]	ENET	ENET0_MDIO	45	46	SPI1_SDO	SPI	1.8/3.3 V [7]	O	K34
–	–	0 V	Ground	GND	47	48	SPI1_SDI	SPI	1.8/3.3 V [7]	I	J35
F28	O	V_ENET [4]	ENET	ENET0_REFCLK_OUT [5]	49	50	SPI1_SCK	SPI	1.8/3.3 V [7]	O	L33
–	–	0 V	Ground	GND	51	52	GND	Ground	0 V	–	–
D28	I	V_ENET [4]	ENET	ENET0_RXC [5]	53	54	ENET0_TXC [5]	ENET	V_ENET [4]	O	H24
–	–	0 V	Ground	GND	55	56	GND	Ground	0 V	–	–
B30	I	V_ENET [4]	ENET	ENET0_RX_CTL [5]	57	58	ENET0_TX_CTL [5]	ENET	V_ENET [4]	O	A29
–	–	0 V	Ground	GND	59	60	GND	Ground	0 V	–	–
A31	I	V_ENET [4]	ENET	ENET0_RXD0 [5]	61	62	ENET0_TXD0 [5]	ENET	V_ENET [4]	O	G25
C29	I	V_ENET [4]	ENET	ENET0_RXD1 [5]	63	64	ENET0_TXD1 [5]	ENET	V_ENET [4]	O	B28
G27	I	V_ENET [4]	ENET	ENET0_RXD2 [5]	65	66	ENET0_TXD2 [5]	ENET	V_ENET [4]	O	E27
H26	I	V_ENET [4]	ENET	ENET0_RXD3 [5]	67	68	ENET0_TXD3 [5]	ENET	V_ENET [4]	O	F26
–	–	0 V	Ground	GND	69	70	GND	Ground	0 V	–	–
G17	I	1.8 V	USB	USB_OTG1_ID	71	72	USB_OTG2_ID	USB	3.3 V	I	F16
H18	P	5 V	USB	USB_OTG1_VBUS	73	74	USB_OTG2_VBUS	USB	3.3 V	P	H16
F14	O	3.3 V	USB	USB_OTG1_PWR	75	76	USB_OTG2_PWR	USB	3.3 V	O	H14
G15	I	3.3 V	USB	USB_OTG1_OC	77	78	USB_OTG2_OC	USB	3.3 V	I	C15
–	–	0 V	Ground	GND	79	80	GND	Ground	0 V	–	–
E19	I/O	3.3 V	USB	USB_OTG1_DN	81	82	USB_OTG2_DN	USB	3.3 V	I/O	D16
D18	I/O	3.3 V	USB	USB_OTG1_DP	83	84	USB_OTG2_DP	USB	3.3 V	I/O	E17
–	–	0 V	Ground	GND	85	86	GND	Ground	0 V	–	–
C25	I/O	1.8 / 3.3 V	SD	SD1_CMD	87	88	USB_SS_TX_P [8]	USB	1.0 V	O	B16
–	–	0 V	Ground	GND	89	90	USB_SS_TX_N [8]	USB	1.0 V	O	A15
G23	O	1.8 / 3.3 V	SD	SD1_CLK	91	92	GND	Ground	0 V	–	–
–	–	0 V	Ground	GND	93	94	USB_SS_RX_P [8]	USB	1.0 V	I	A19
A27	I/O	1.8 / 3.3 V	SD	SD1_DATA0	95	96	USB_SS_RX_N [8]	USB	1.0 V	I	B18
B26	I/O	1.8 / 3.3 V	SD	SD1_DATA1	97	98	GND	Ground	0 V	–	–
D26	I/O	1.8 / 3.3 V	SD	SD1_DATA2	99	100	PCIE_TX_N	PCIE	0.7 V	O	A9
E25	I/O	1.8 / 3.3 V	SD	SD1_DATA3	101	102	PCIE_TX_P	PCIE	0.7 V	O	B10
–	–	0 V	Ground	GND	103	104	GND	Ground	0 V	–	–
D24	I	1.8 V	SD	SD1_WP	105	106	PCIE_RX_N	PCIE	0.7 V	I	B12
–	P	1.8 / 3.3 V	Power	V_ENET_IN	107	108	PCIE_RX_P	PCIE	0.7 V	I	A13
E23	I	1.8 V	SD	SD1_CD#	109	110	GND	Ground	0 V	–	–
B24	I/O	1.8 V	GPIO	GPIO4_IO19	111	112	PCIE_REFCLK_N	PCIE	0.7 V	I/O	D12
–	–	0 V	Ground	GND	113	114	PCIE_REFCLK_P	PCIE	0.7 V	I/O	E11
D10	I	3.3 V	PCIE	PCIE_CLKREQ#	115	116	GND	Ground	0 V	–	–
H10	O	3.3 V	PCIE	PCIE_PERST#	117	118	IMX_ONOFF	CONFIG	1.8 V	I_{PU}	AH28
A11	I	3.3 V	PCIE	PCIE_WAKE#	119	120	GND	Ground	0 V	–	–

4: Voltage is defined by V_ENET_IN at pin X1-107.
5: RGMII is not available with the i.MX 8DualX. RMII or an alternate multiplexing function can be used.
6: Open drain output. Requires an external pull-up to the supply voltage.
7: Voltage is defined by V_IO_IN at pin X2-11.
8: Pin is "NC" at the i.MX 8DualX.

3.1.3 TQMa8Xx pinout (continued)

Table 4: Pinout TQMa8Xx X2

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	P	3.3 V	Power	V_3V3_IN	1	2	V_3V3_IN	Power	3.3 V	P	–
–	P	3.3 V	Power	V_3V3_IN	3	4	V_3V3_IN	Power	3.3 V	P	–
–	P	3.3 V	Power	V_3V3_IN	5	6	V_3V3_IN	Power	3.3 V	P	–
–	–	0 V	Ground	GND	7	8	GND	Ground	0 V	–	–
–	–	0 V	Ground	GND	9	10	GND	Ground	0 V	–	–
–	P	1.8 / 3.3 V	Power	V_IO_IN	11	12	V_1V8_OUT [9]	Power	1.8 V	P	–
AJ31	I	1.8 V	CONFIG	BOOT_MODE0	13	14	GND	Ground	0 V	–	–
AK32	I	1.8 V	CONFIG	BOOT_MODE1	15	16	MCLK_OUT0	CLK	V_IO [10]	O	L29
AL31	I	1.8 V	CONFIG	BOOT_MODE2	17	18	MCLK_IN1	CLK	V_IO [10]	I	M28
AJ29	I	1.8 V	CONFIG	BOOT_MODE3	19	20	MCLK_IN0	CLK	V_IO [10]	I	G35
–	P	1.8 V	Power	V_1V8_ANA	21	22	GND	Ground	0 V	–	–
–	P	3 V	Power	V_LICELL	23	24	GPIO3_IO05	GPIO	1.8 V	I/O	AP26
–	$O_{OD/PU}$	1.8 V	CONFIG	PMIC_FSOB_EWARN	25	26	GPIO3_IO06	GPIO	1.8 V	I/O	AM24
AR31	I_{PU}	1.8 V	CONFIG	PMIC_PWRON	27	28	SCU_UART_RX	SCU UART	1.8 V	I	AF28
–	–	0 V	Ground	GND	29	30	SCU_UART_TX	SCU UART	1.8 V	O	AH30
AM22	I	1.8 V	CSI	MIPI_CSI_DN0	31	32	RESET_IN#	CONFIG	1.8 V	I_{PU}	AG31
AP22	I	1.8 V	CSI	MIPI_CSI_DP0	33	34	RESET_OUT#	CONFIG	–	O_{OD} [11]	–
–	–	0 V	Ground	GND	35	36	GND	Ground	0 V	–	–
AM20	I	1.8 V	CSI	MIPI_CSI_DN1	37	38	I2C2_SCL	I2C	V_IO [10]	I/O	AD30
AP20	I	1.8 V	CSI	MIPI_CSI_DP1	39	40	I2C2_SDA	I2C	V_IO [10]	I/O	AF34
–	–	0 V	Ground	GND	41	42	GND	Ground	0 V	–	–
AN23	I	1.8 V	CSI	MIPI_CSI_DN2	43	44	SPI3_SCK	SPI	V_IO [10]	O	H32
AR23	I	1.8 V	CSI	MIPI_CSI_DP2	45	46	SPI3_SDO	SPI	V_IO [10]	O	F34
–	–	0 V	Ground	GND	47	48	SPI3_SDI	SPI	V_IO [10]	I	G33
AN19	I	1.8 V	CSI	MIPI_CSI_DN3	49	50	SPI3_CS0	SPI	V_IO [10]	O	J31
AR19	I	1.8 V	CSI	MIPI_CSI_DP3	51	52	SPI3_CS1	SPI	V_IO [10]	O	K30
–	–	0 V	Ground	GND	53	54	PMIC_AMUX_VSD	Power	1.8/3.3 V	P	–
AN21	I	1.8 V	CSI	MIPI_CSI_CLKN	55	56	GND	Ground	0 V	–	–
AR21	I	1.8 V	CSI	MIPI_CSI_CLKP	57	58	MIPI_CSI_MCLK	CSI	1.8 V	O	AN25
–	–	0 V	Ground	GND	59	60	GND	Ground	0 V	–	–
AN15	O	1.8 V	DSI / LVDS	MIPI_DSI1_DN0	61	62	MIPI_DSI0_DN0	DSI / LVDS	1.8 V	O	AJ21
AR15	O	1.8 V	DSI / LVDS	MIPI_DSI1_DP0	63	64	MIPI_DSI0_DP0	DSI / LVDS	1.8 V	O	AK22
–	–	0 V	Ground	GND	65	66	GND	Ground	0 V	–	–
AN17	O	1.8 V	DSI / LVDS	MIPI_DSI1_DN1	67	68	MIPI_DSI0_DN1	DSI / LVDS	1.8 V	O	AJ17
AR17	O	1.8 V	DSI / LVDS	MIPI_DSI1_DP1	69	70	MIPI_DSI0_DP1	DSI / LVDS	1.8 V	O	AK18
–	–	0 V	Ground	GND	71	72	GND	Ground	0 V	–	–
AM14	O	1.8 V	DSI / LVDS	MIPI_DSI1_DN2	73	74	MIPI_DSI0_DN2	DSI / LVDS	1.8 V	O	AJ23
AP14	O	1.8 V	DSI / LVDS	MIPI_DSI1_DP2	75	76	MIPI_DSI0_DP2	DSI / LVDS	1.8 V	O	AK24
–	–	0 V	Ground	GND	77	78	GND	Ground	0 V	–	–
AM18	O	1.8 V	DSI / LVDS	MIPI_DSI1_DN3	79	80	MIPI_DSI0_DN3	DSI / LVDS	1.8 V	O	AJ15
AP18	O	1.8 V	DSI / LVDS	MIPI_DSI1_DP3	81	82	MIPI_DSI0_DP3	DSI / LVDS	1.8 V	O	AK16
–	–	0 V	Ground	GND	83	84	GND	Ground	0 V	–	–
AM16	O	1.8 V	DSI / LVDS	MIPI_DSI1_CLKN	85	86	MIPI_DSI0_CLKN	DSI / LVDS	1.8 V	O	AJ19
AP16	O	1.8 V	DSI / LVDS	MIPI_DSI1_CLKP	87	88	MIPI_DSI0_CLKP	DSI / LVDS	1.8 V	O	AK20
–	–	0 V	Ground	GND	89	90	GND	Ground	0 V	–	–
AK26	I/O	V_IO [10]	GPIO	GPIO3_IO00	91	92	GPIO3_IO02	GPIO	V_IO [10]	I/O	AP28
AM26	I/O	V_IO [10]	GPIO	GPIO3_IO01	93	94	GPIO3_IO03	GPIO	V_IO [10]	I/O	AR27
–	–	0 V	Ground	GND	95	96	GND	Ground	0 V	–	–
AK10	I	1.8 V	QSPI	QSPIB_DQS	97	98	SAI1_TXC	SAI	V_IO [10]	O	Y34
–	–	0 V	Ground	GND	99	100	SAI1_TXFS	SAI	V_IO [10]	O	Y32
AR11	O	1.8 V	QSPI	QSPIB_SCLK	101	102	SAI1_TXD	SAI	V_IO [10]	O	AA33
–	–	0 V	Ground	GND	103	104	GND	Ground	0 V	–	–
AM10	I/O	1.8 V	QSPI	QSPIB_DATA0	105	106	SAI1_RXC	SAI	V_IO [10]	I	AA31
AL9	I/O	1.8 V	QSPI	QSPIB_DATA1	107	108	SAI1_RXFS	SAI	V_IO [10]	I	AB34
AJ11	I/O	1.8 V	QSPI	QSPIB_DATA2	109	110	SAI1_RXD	SAI	V_IO [10]	I	AA35
AM8	I/O	1.8 V	QSPI	QSPIB_DATA3	111	112	GPIO3_IO07	GPIO	1.8 V	I/O	AP24
AH10	O [12]	1.8 V	QSPI	QSPIB_SS0#	113	114	GPIO3_IO08	GPIO	1.8 V	I/O	AR25
AJ9	O	1.8 V	QSPI	QSPIB_SS1#	115	116	I2C1_SDA	I2C	V_IO [10]	I/O_{PU}	AE35
AK12	I/O	1.8 V	GPIO	GPIO3_IO15	117	118	I2C1_SCL	I2C	V_IO [10]	I/O_{PU}	AD32
–	–	0 V	Ground	GND	119	120	GND	Ground	0 V	–	–

9: Maximum load of 0.7 A.
10: Voltage is defined by V_IO_IN at pin X2-11.
11: Open drain output. Requires an external pull-up to the supply voltage (maximum 6.5 V).
12: DNC for TQMa8Xx variants with Octal, Twin Quad, Hyperflash or Xccela flash.

3.1.3 TQMa8Xx pinout (continued)

Table 5: Pinout TQMa8Xx X3

Ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	Ball
–	–	0 V	Ground	GND	1	2	GND	Ground	0 V	–	–
W29	I/O	1.8 V	GPIO	GPIO1_IO14	3	4	JTAG_TCK	JTAG	1.8 V	I	AE31
V34	I/O	1.8 V	GPIO	GPIO1_IO13	5	6	JTAG_TDI	JTAG	1.8 V	I	AH34
–	–	0 V	Ground	GND	7	8	JTAG_TDO	JTAG	1.8 V	O	AF32
AE33	I/O	V_IO [13]	GPIO	GPIO1_IO29	9	10	JTAG_TMS	JTAG	1.8 V	I	AG35
AC29	I/O	V_IO [13]	GPIO	GPIO1_IO30	11	12	SCU_WDOG_OUT [14]	CONFIG	1.8 V	O	AD28
AC31	I/O	V_IO [13]	GPIO	GPIO1_IO25	13	14	GND	Ground	0 V	–	–
AB28	I/O	V_IO [13]	GPIO	GPIO1_IO26	15	16	CAN0_RX	CAN	V_IO [13]	I	AB32
–	–	0 V	Ground	GND	17	18	CAN0_TX	CAN	V_IO [13]	O	AA29
AK28	O	V_IO [13]	TAMPER	TAMPER_OUT0	19	20	CAN1_RX	CAN	V_IO [13]	I	AD34
AL29	O	V_IO [13]	TAMPER	TAMPER_OUT1	21	22	CAN1_TX	CAN	V_IO [13]	O	AC35
AP30	O	V_IO [13]	TAMPER	TAMPER_OUT2	23	24	GND	Ground	0 V	–	–
AJ27	O	V_IO [13]	TAMPER	TAMPER_OUT3	25	26	ADC_IN0	ADC	1.8 V	I	U35
AN29	O	V_IO [13]	TAMPER	TAMPER_OUT4	27	28	ADC_IN1	ADC	1.8 V	I	U33
AM30	I	V_IO [13]	TAMPER	TAMPER_IN0	29	30	ADC_IN2	ADC	1.8 V	I	V32
AJ25	I	V_IO [13]	TAMPER	TAMPER_IN1	31	32	ADC_IN3	ADC	1.8 V	I	V30
AM28	I	V_IO [13]	TAMPER	TAMPER_IN2	33	34	V_ADC_IN	ADC	1.8 V	I	U29
AL27	I	V_IO [13]	TAMPER	TAMPER_IN4	35	36	PMIC_I2C_SDA	PMIC I2C	1.8 V	DNC	AH32
AR29	I	V_IO [13]	TAMPER	TAMPER_IN3	37	38	PMIC_I2C_SCL	PMIC I2C	1.8 V	DNC	AJ35
–	–	0 V	Ground	GND	39	40	GND	Ground	0 V	–	–

3.2 Data interfaces

To ensure flexible use of all i.MX 8X functions, all i.MX 8X pins, or interfaces, are routed to the connectors where possible and are therefore available on the carrier board. Besides some pins that are not available due to TQMa8Xx-internal functions like SDRAM and for technical reasons, there are minimal restrictions in the availability of i.MX 8X pins, which are shown in the following table.

Table 6: TQMa8Xx-internal interfaces

i.MX 8X interface	Chapter	Usage
USDHC0	3.3.2.3	eMMC, 8 bit (optional)
QSPIA	3.3.2.4	QSPIA used for optional SPI NOR flash, QSPIB routed to TQMa8Xx connectors
SDRAM	3.3.2.1	TQMa8Xx: 32 bit DDR3L no ECC, or 32 bit DDR3L + 8 bit ECC
	3.3.2.2	TQMa8Xx4: 32 bit LPDDR4 no ECC

13: Voltage is defined by V_IO_IN at pin X2-11.
14: Changed from JTAG_TRST# to SCU_WDOG_OUT. Signal JTAG_TRST# is not supported anymore by the i.MX 8X.

3.2.1 ADC

The i.MX 8X offers a 12-bit AD converter with a reference voltage of 1.8 V and a maximum of six channels.
ADC_IN[3:0] are supported as ADC inputs in the BSP provided by TQ-Systems.
GPIO1_IO14 (ADC_IN4) is multiplexed as GPIO by default. For details refer to the CPU documentation in (1) and (2).
The ADC interfaces require a 1.8 V reference voltage at TQMa8Xx pin V_ADC_IN.
For applications with low accuracy, a reference voltage generated by the PMIC is provided via TQMa8Xx pin V_1V8_OUT.
In this case this can be connected directly to V_ADC_IN.
For applications with high accuracy a dedicated voltage reference must be connected to V_ADC_IN.
The voltage at pin V_ADC_IN is filtered on the TQMa8Xx, it should at least meet the following parameters:

- Voltage at V_ADC_IN: 1.0 V to 1.8 V
- Must meet i.MX 8X power sequencing, see chapter 3.5.10

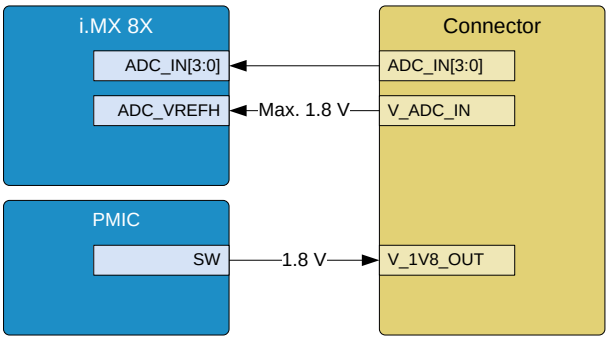


Figure 4: Block diagram ADC

The following table shows the available ADC interface signals:

Table 7: ADC signals

Signal	TQMa8Xx	Power group
ADC_IN3	X3-32	1.8 V
ADC_IN2	X3-30	
ADC_IN1	X3-28	
ADC_IN0	X3-26	
V_ADC_IN	X3-34	1.0 V to 1.8 V

3.2.2 CAN

The i.MX 8X provides three integrated CAN controllers, of which two (CAN0, CAN1) are available as CAN interfaces on the TQMa8Xx connectors. The required driver components have to be provided on the mainboard.

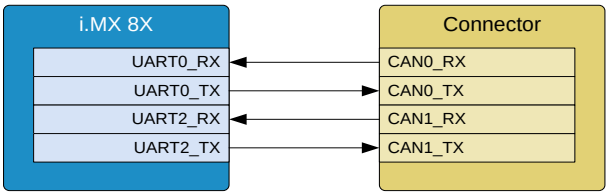


Figure 5: Block diagram CAN

Table 8: CAN signals

Signal	TQMa8Xx	Power group
CAN0_RX	X3-16	V_IO_IN
CAN0_TX	X3-18	
CAN1_RX	X3-20	
CAN1_TX	X3-22	

3.2.3 GPIO

Except dedicated differential signals (e.g. MIPI DSI/CSI, USB), most CPU pins can be configured as GPIO.
The following signals are configured as GPIO in their primary function:

Table 9: GPIO signals

Signal	TQMa8Xx	Power group
GPIO1_IO13	X3-5	1.8 V
GPIO1_IO14	X3-3	
GPIO3_IO05	X2-24	
GPIO3_IO06	X2-26	
GPIO3_IO07	X2-112	
GPIO3_IO08	X2-114	
GPIO3_IO15	X2-117	
GPIO4_IO19	X1-111	
GPIO0_IO30	X1-24	V_IO_IN
GPIO0_IO31	X1-26	
GPIO1_IO07	X1-28	
GPIO1_IO25	X3-13	
GPIO1_IO26	X3-15	
GPIO1_IO29	X3-9	
GPIO1_IO30	X3-11	
GPIO3_IO00	X2-91	
GPIO3_IO01	X2-93	
GPIO3_IO02	X2-92	
GPIO3_IO03	X2-94	
M4_GPIO0_IO02	X1-23	
M4_GPIO0_IO03	X1-25	

3.2.4 I²C

The I2C interfaces I2C1, I2C2, PMIC_I2C and M4_I2C (depending on module variant) are provided on module connectors.
Components are already connected to I2C1 on the TQMa8Xx. Therefore, the required pull-up resistors are also already equipped on the TQMa8Xx.
I2C2 and the dedicated I²C bus of the M4 core processor (depending on the module variant) are connected to the module headers without any further components.
The PMIC_I2C interface represents a special I²C bus of the SCU interface and is used to configure the PMIC by the SCU firmware.
All essential configurations (power sequencing) are predefined. Changing the PMIC configuration is not recommended.

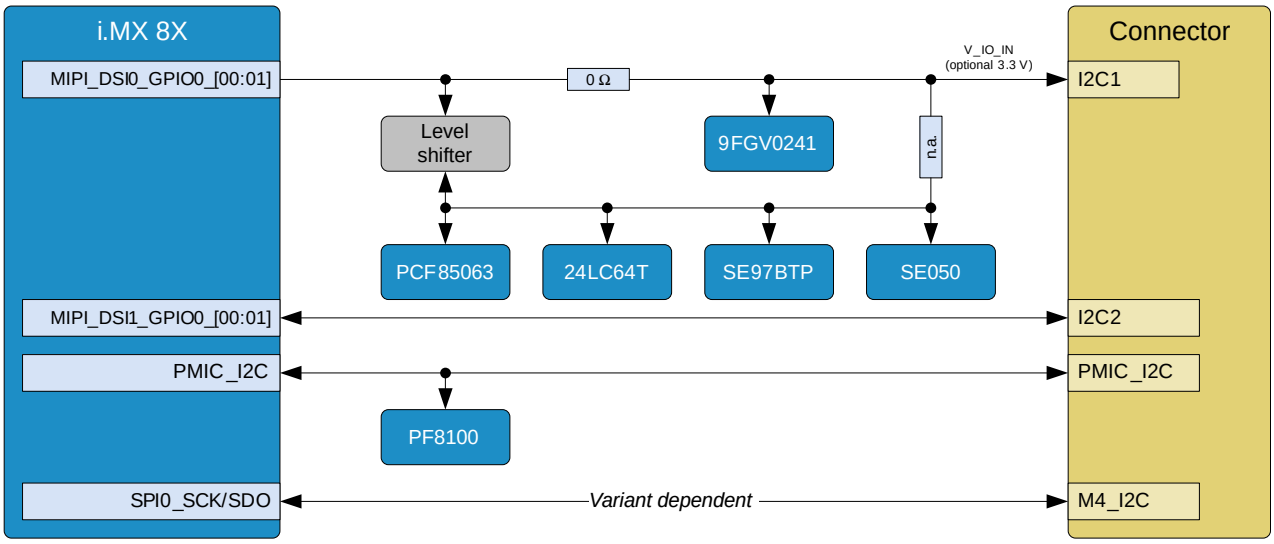


Figure 6: Block diagram I²C

The following table shows the signals used by the I²C interfaces.

Table 10: I²C signals

Signal	TQMa8Xx	Remark	Power group
I2C1_SCL	X2-118	2.2 kΩ PU on TQMa8Xx	V_IO_IN
I2C1_SDA	X2-116	2.2 kΩ PU on TQMa8Xx	
I2C2_SCL	X2-38	No PU on TQMa8Xx	
I2C2_SDA	X2-40	No PU on TQMa8Xx	
M4_I2C_SCL [15]	X1-29	No PU on TQMa8Xx	
M4_I2C_SDA [15]	X1-27	No PU on TQMa8Xx	
PMIC_I2C_SCL	X3-38	1.5 kΩ PU on TQMa8Xx	V_1V8_ANA
PMIC_I2C_SDA	X3-36	1.5 kΩ PU on TQMa8Xx	

Note: I²C address conflicts, pull-up resistors	
	Make sure that no address conflicts occur when further I²C components are connected on the carrier board. Otherwise, malfunctions may occur. If more devices are connected to the I²C buses on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional pull-ups should be provided on the carrier board, if required.

15: For TQMa8Xx variants with populated Trust Secure Element, the M4_I2C bus is not available at the TQMa8Xx connector, see also chapter 3.3.4.

3.2.4 I²C (continued)

The following table shows the I²C devices on the TQMa8Xx.

Table 11: I²C addresses

I²C bus	Device	Function	7-bit address	Remark
PMIC_I2C	PF8100	PMIC	0x08 / 000 1000b	Should not be altered
I2C1	PCF85063A	RTC	0x51 / 101 0001b	Assembly option
	24LC64	EEPROM	0x57 / 101 0111b	Assembly option
	SE050	Secure Element	0x48 / 100 1000b	Assembly option
	SE97BTP	Temperature sensor	0x1B / 001 1011b	–
		EEPROM	0x53 / 101 0011b	Normal Mode (RWP)
			0x33 / 011 0011b	Protected Mode (PWP)
	9FGV0241	PCIe clock generator	0x6A / 110 1010b	TQMa8Xx4 only
I2C2	–	–	–	Not used on TQMa8Xx
M4_I2C	–	–	–	Not used on TQMa8Xx

By default, the I/O voltage for the I2C1 bus at the module connector is freely selectable via pin V_IO_IN pin (1.8 V or 3.3 V). Per assembly option the I/O voltage for the two signals X2-116 (I2C1_SDA) and X2-118 (I2C1_SCL) can be permanently set to 3.3 V. This requires a change of the resistors from R59/R60 to R61/R62.

3.2.5 JTAG

The i.MX 8X JTAG port is directly routed to the TQMa8Xx connectors, without any additional circuitry.

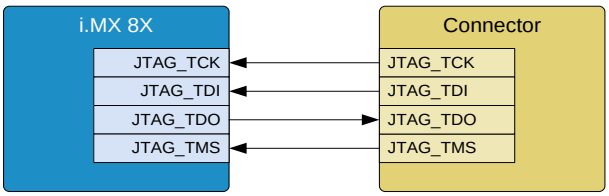


Figure 7: Block diagram JTAG

The following table shows the JTAG interface signals.

Table 12: JTAG signals

Signal	TQMa8Xx	Power group
JTAG_TCK	X3-4	V_1V8_ANA
JTAG_TDI	X3-6	
JTAG_TDO	X3-8	
JTAG_TMS	X3-10	

Note: JTAG_TRST#	
	Signal JTAG_TRST# is no longer supported by the i.MX 8X.

3.2.6 MIPI CSI

The TQMa8Xx provides a MIPI CSI camera interface. Up to 1.5 Gbps are transmitted on four data pairs.
The maximum image format is 4K@30 fps.

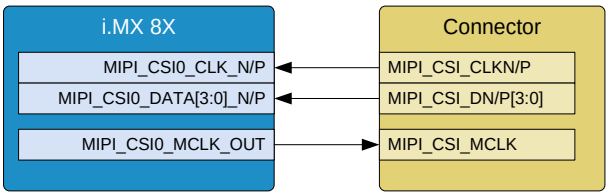


Figure 8: Block diagram MIPI CSI

The following table shows the signals used by the MIPI CSI interface.

Table 13: MIPI CSI signals

Signal	TQMa8Xx	Power group
MIPI_CSI_DN3	X2-49	1.8 V
MIPI_CSI_DP3	X2-51	
MIPI_CSI_DN2	X2-43	
MIPI_CSI_DP2	X2-45	
MIPI_CSI_DN1	X2-37	
MIPI_CSI_DP1	X2-39	
MIPI_CSI_DN0	X2-31	
MIPI_CSI_DP0	X2-33	
MIPI_CSI_CLKN	X2-55	
MIPI_CSI_CLKP	X2-57	
MIPI_CSI_MCLK	X2-58	

3.2.7 MIPI DSI

The TQMa8Xx offers two DSI interfaces. As a secondary function, the pins can be defined as LVDS PHYs.
The MIPI-DSI PHY supports formats up to 1920x1200 @ 60 fps, the LVDS-PHY 1920x1080 @ 60 fps.

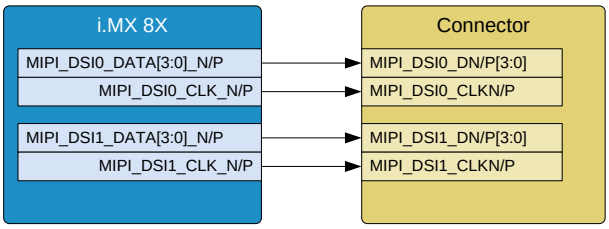


Figure 9: Block diagram MIPI DSI

The following table shows the signals used by the MIPI DSI interfaces.

Table 14: MIPI DSI0 / DSI1 signals

Signal	TQMa8Xx	Power group
MIPI_DSI0_DN3	X2-80	1.8 V
MIPI_DSI0_DP3	X2-82	
MIPI_DSI0_DN2	X2-74	
MIPI_DSI0_DP2	X2-76	
MIPI_DSI0_DN1	X2-68	
MIPI_DSI0_DP1	X2-70	
MIPI_DSI0_DN0	X2-62	
MIPI_DSI0_DP0	X2-64	
MIPI_DSI0_CLKN	X2-86	
MIPI_DSI0_CLKP	X2-88	
MIPI_DSI1_DN3	X2-79	
MIPI_DSI1_DP3	X2-81	
MIPI_DSI1_DN2	X2-73	
MIPI_DSI1_DP2	X2-75	
MIPI_DSI1_DN1	X2-67	
MIPI_DSI1_DP1	X2-69	
MIPI_DSI1_DN0	X2-61	
MIPI_DSI1_DP0	X2-63	
MIPI_DSI1_CLKN	X2-85	
MIPI_DSI1_CLKP	X2-87	

3.2.8 ENET

The i.MX 8X has two Ethernet MACs that can operate in Gigabit full-duplex mode.
RMII or RGMII mode can be used, RGMII is supported in the BSP provided by TQ-Systems.
The IO voltage of both MACs and the MDIO signals is determined by the voltage at TQMa8Xx pin V_ENET_IN (X1-107).

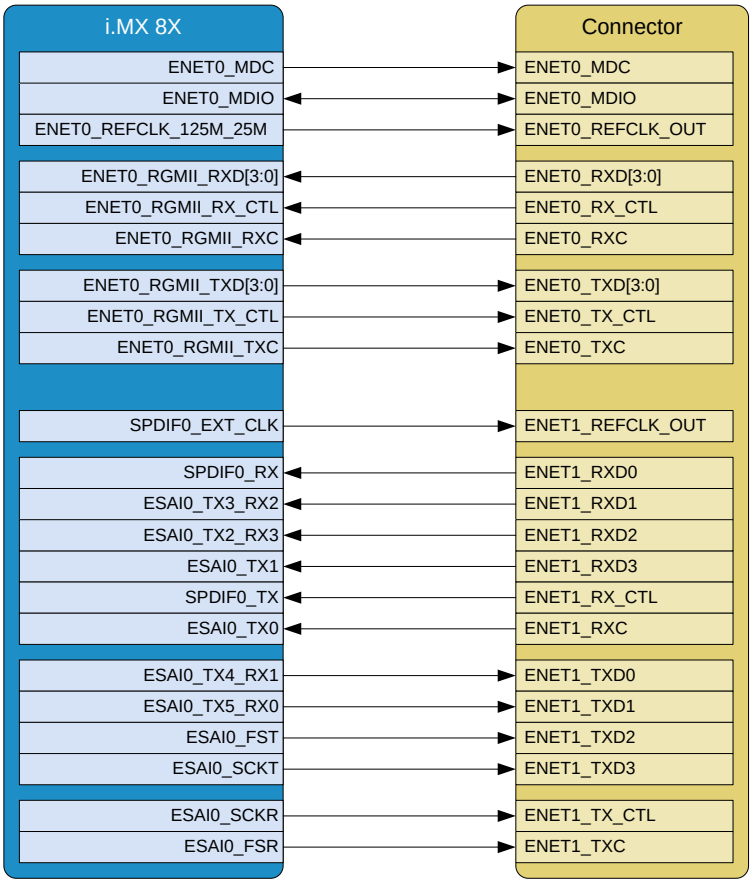


Figure 10: Block diagram ENET0 / ENET1

Note: MDIO/SMI interface	
	For both MACs the i.MX 8X provides only one MDIO/SMI interface. This has to be taken into account when assigning addresses to the RGMII-PHYs on the carrier board.

Note: ENET0 and ENET1, 2.5V IO voltage not supported	
	Due to CPU erratum ERR010913 an IO voltage of 2.5 V is not supported for ENET0 and ENET1.

3.2.8.1 RGMII pinout

The following TQMa8Xx signals are used in the RGMII configuration.

Table 15: ENET signals RGMII mode

Signal	TQMa8Xx	Power group
ENET0_TXD3	X1-68	V_ENET_IN
ENET0_TXD2	X1-66	
ENET0_TXD1	X1-64	
ENET0_TXD0	X1-62	
ENET0_RXD3	X1-67	
ENET0_RXD2	X1-65	
ENET0_RXD1	X1-63	
ENET0_RXD0	X1-61	
ENET0_TXC	X1-54	
ENET0_RXC	X1-53	
ENET0_TX_CTL	X1-58	
ENET0_RX_CTL	X1-57	
ENET0_REFCLK_OUT	X1-49	
ENET0_MDIO	X1-45	
ENET0_MDC	X1-43	
ENET1_TXD3	X1-20	
ENET1_TXD2	X1-18	
ENET1_TXD1	X1-16	
ENET1_TXD0	X1-14	
ENET1_RXD3	X1-19	
ENET1_RXD2	X1-17	
ENET1_RXD1	X1-15	
ENET1_RXD0	X1-13	
ENET1_TXC	X1-8	
ENET1_RXC	X1-7	
ENET1_TX_CTL	X1-12	
ENET1_RX_CTL	X1-11	
ENET1_REFCLK_OUT	X1-3	

3.2.8.2 RMII pinout

The following TQMa8Xx signals are used in the RMII configuration.

Table 16: ENET signals RMII mode

Signal	Function in RMII mode	TQMa8Xx	Power group
ENET0_TXD1	ENET0_TXD1	X1-64	V_ENET_IN
ENET0_TXD0	ENET0_TXD0	X1-62	
ENET0_RXD2	ENET0_RX_ER	X1-65	
ENET0_RXD1	ENET0_RXD1	X1-63	
ENET0_RXD0	ENET0_RXD0	X1-61	
ENET0_TXC	ENET0_REF_CLK	X1-54	
ENET0_TX_CTL	ENET0_TX_EN	X1-58	
ENET0_RX_CTL	ENET0_CRS_DV	X1-57	
ENET0_MDIO	ENET0_MDIO	X1-45	
ENET0_MDC	ENET0_MDC	X1-43	
ENET1_TXD1	ENET1_TXD1	X1-16	
ENET1_TXD0	ENET1_TXD0	X1-14	
ENET1_RXD2	ENET1_RX_ER	X1-17	
ENET1_RXD1	ENET1_RXD1	X1-15	
ENET1_RXD0	ENET1_RXD0	X1-13	
ENET1_TXC	ENET1_REF_CLK	X1-8	
ENET1_TX_CTL	ENET1_TX_EN	X1-12	
ENET1_RX_CTL	ENET1_CRS_DV	X1-11	

3.2.9 PCIe

The i.MX 8X provides one PCIe lane with transfer rates of up to 8 Gbps, according to the PCI Express Base Specification, Revision 4.0 (Version 0.7).

The reference clock of 100 MHz can be generated on the TQMa8Xx4 and output to PCIE_REFCLK_N/P for the PCIe card or must be provided to PCIE_REFCLK_N/P.

The TQMa8Xx4 is available in a variant with a discrete clock generator, which generates the PCIe reference clock for the i.MX 8X, as well as the connected PCIe device. For more information see chapter 3.3.6.

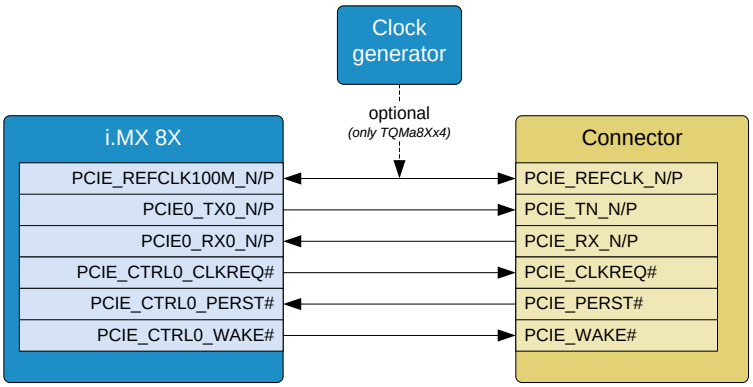


Figure 11: Block diagram PCIe

Table 17: Mini PCIe signals

Signal	TQMa8Xx	Power group
PCIE_TX_N	X1-100	V_VDD_PCIE_1P0_CAP (1.0 V)
PCIE_TX_P	X1-102	
PCIE_RX_N	X1-106	
PCIE_RX_P	X1-108	
PCIE_REFCLKOUT_N	X1-112	1.8 V
PCIE_REFCLKOUT_P	X1-114	
PCIE_CLKREQ#	X1-115	3.3 V or V_IO_IN [16]
PCIE_WAKE#	X1-119	
PCIE_PERST#	X1-117	

16: PCIe signals are standard-compliant with 3.3 V, but can be set to 1.8 V with V_IO_IN. A fixed IO voltage of 3.3 V is possible as an assembly option.

3.2.10 SPI

The SPI interfaces of the i.MX 8X are full-duplex capable and support master and slave modes. SPI1, SPI2 and SPI3 are routed to the connectors as primary function. SPI1 and SPI3 provide two chip selects each, SPI2 provides one chip select.

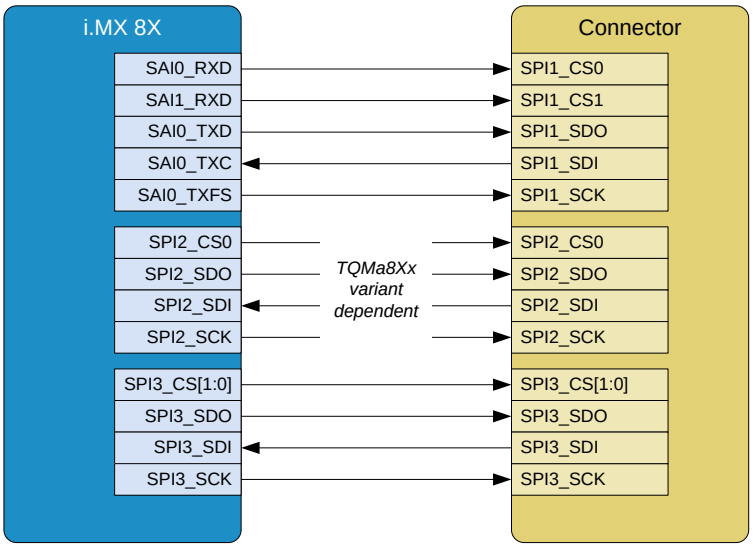


Figure 12: Block diagram SPI

The following table shows the signals used by the SPI interface.

Table 18: SPI signals

Signal	TQMa8Xx	Power group
SPI1_CS0	X1-42	V_IO_IN
SPI1_CS1	X1-44	
SPI1_SCK	X1-50	
SPI1_SDI	X1-48	
SPI1_SDO	X1-46	
SPI2_CS0 [17]	X1-40	
SPI2_SCK [17]	X1-34	
SPI2_SDI [17]	X1-38	
SPI2_SDO [17]	X1-36	
SPI3_CS0	X2-50	
SPI3_CS1	X2-52	
SPI3_SCK	X2-44	
SPI3_SDI	X2-48	
SPI3_SDO	X2-46	

17: For TQMa8Xx variants with populated Trust Secure Element, SPI2 is not available at the TQMa8Xx connector, see also chapter 3.3.4.

3.2.11 QSPI

The QSPIB interface is routed to the TQMa8Xx connectors to connect QSPI NOR flash on the carrier board.
Depending on the TQMa8Xx variant, a QSPI NOR flash is populated on the TQMa8Xx.
More information about the QSPI interface can be found in chapter 3.3.2.4.

Attention: Destruction or malfunction, QSPIB	
	For TQMa8Xx variants with Octal, Twin Quad SPI, Hyper or Xccela Flash (or technically comparable types) the chip select signal QSPIB_SS0# is not available for use on the base board and must not be connected!

3.2.12 SAI

The SAI interface provides a full duplex interface for audio interfaces. I2S, AC97, TDM and other codec interfaces are supported.

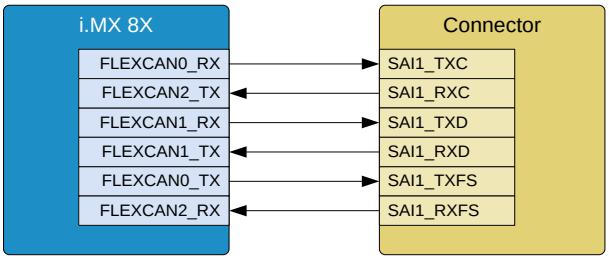


Figure 13: Block diagram SAI

Table 19: SAI signals

Signal	TQMa8Xx	Power group
SAI1_TXC	X2-98	V_IO_IN
SAI1_RXC	X2-106	
SAI1_TXD	X2-102	
SAI1_RXD	X2-110	
SAI1_TXFS	X2-100	
SAI1_RXFS	X2-108	

3.2.13 SD card

The i.MX 8X supports SD cards up to UHS-I in SDR104/DDR50 mode. This corresponds to SD card specification v3.0 and a maximum data width of 4 bit. For this purpose, the uSDHC1 bus including the Write-Protect and Card-Detect signals is routed to the TQMa8Xx connectors.

The signals of the uSDHC1 interface are supplied via a PMIC regulator whose IO voltage (V_SD) can be set to a 1.8 V or 3.3 V by the PMIC signal SD1_VSELECT. SD1_VSELECT is automatically switched by the software driver so that the fastest possible mode is used depending on the SD card used.

In addition, the voltage V_SD (PMIC_AMUX_VSD) is available at the module connector. This can be used as reference voltage for the pull-ups of the data lines (DATA[3:0]; CMD).

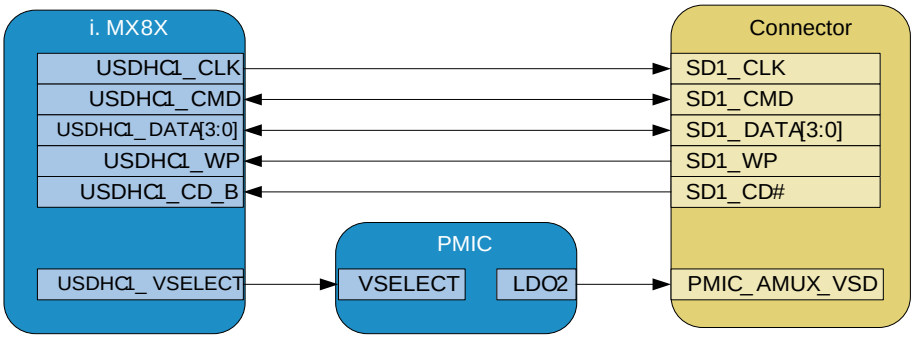


Figure 14: Block diagram uSDHC1

Table 20: SD1_VSELECT states

SD1_VSELECT	V_SD	Remark
High	1.8 V	–
Low	3.3 V	Default at boot (i.MX 8X internal pull-down)

Signals WP, CD# and VSELECT are not affected by the voltage switchover. They are fixed supplied with 1.8 V.

Table 21: SD card signals (uSDHC1)

Signal	TQMa8Xx	Power group
SD1_CLK	X1-91	V_SD (switched by SD1_VSELECT)
SD1_CMD	X1-87	
SD1_DATA3	X1-101	
SD1_DATA2	X1-99	
SD1_DATA1	X1-97	
SD1_DATA0	X1-95	
SD1_VSELECT	–	1.8 V
SD1_WP	X1-105	
SD1_CD#	X1-109	
PMIC_AMUX_VSD	X2-54	–

3.2.14 USB 2.0 OTG1

The i.MX 8X features a USB 2.0 OTG controller that provides a high-speed (480 Mbps) device, host or OTG port on the TQMa8Xx connectors.

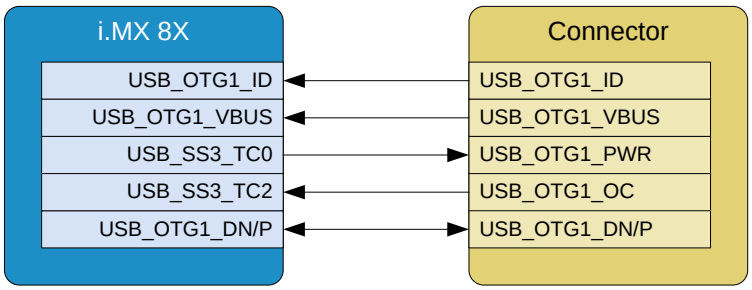


Figure 15: Block diagram USB 2.0 OTG1

Table 22: USB 2.0 OTG1 signals

Signal	TQMa8Xx	Power group
USB_OTG1_ID	X1-71	1.8 V
USB_OTG1_DN	X1-81	3.3 V
USB_OTG1_DP	X1-83	
USB_OTG1_OC	X1-77	
USB_OTG1_PWR	X1-75	
USB_OTG1_VBUS	X1-73	Supplied externally (5 V)

Note: Trace length match and impedance	
	The differential signals of the USB OTG1 interface must be length matched on the carrier board and have a differential impedance of 90 Ω.

3.2.15 USB 2.0 OTG2 / USB 3.0

The USB 3.0 block of the i.MX 8X contains a USB 3.0 and a USB 2.0 OTG controller (OTG2) that can be used independently of each other. USB 3.0 can achieve transfer rates of up to 5 Gbit/s (Super Speed).

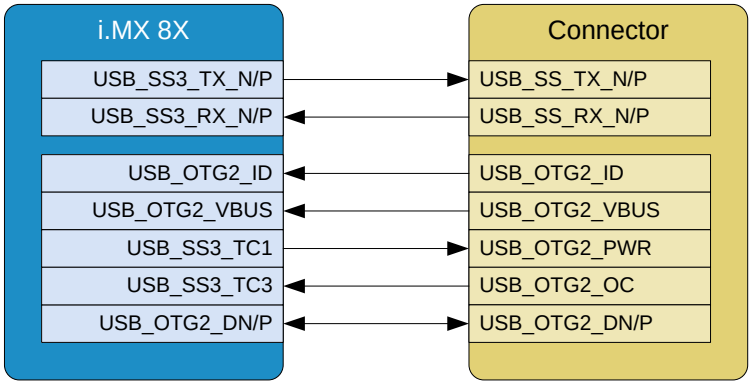


Figure 16: Block diagram USB 3.0

Table 23: USB 2.0 OTG2 signals

Signal	TQMa8Xx	Power group
USB_OTG2_DN	X1-82	VDD_USB_3P3 (3.3 V)
USB_OTG2_DP	X1-84	
USB_OTG2_ID	X1-72	
USB_OTG2_OC	X1-78	
USB_OTG2_PWR	X1-76	
USB_OTG2_VBUS	X1-74	Supplied externally (3.3 V)

Table 24: USB 3.0 signals

Signal	TQMa8Xx	Power group
USB_SS_RX_N	X1-96	V_VDD_USB_OTG_1P0 (1.0 V)
USB_SS_RX_P	X1-94	
USB_SS_TX_N	X1-90	
USB_SS_TX_P	X1-88	

Attention: 3.3 V supply for USB_OTG2_VBUS	
	Due to the different implementation of the OTG2 controller compared to the dedicated USB 2.0 OTG1 controller (see chapter 3.2.14) the pin USB_OTG2_VBUS must be supplied with 3.3 V instead of 5 V!

3.2.16 TAMPER

In addition to other safety functions of the i.MX 8X, the SNVS unit provides 10 tamper signals.

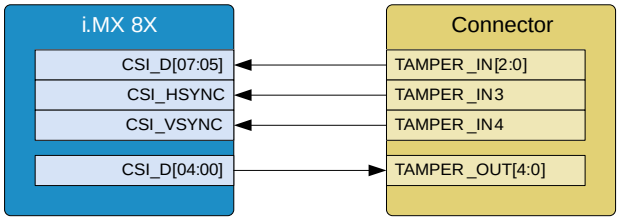


Figure 17: Block diagram TAMPER

Table 25: TAMPER signals

Signal	TQMa8Xx	Power group
TAMPER_OUT0	X3-19	V_IO_IN
TAMPER_OUT1	X3-21	
TAMPER_OUT2	X3-23	
TAMPER_OUT3	X3-25	
TAMPER_OUT4	X3-27	
TAMPER_IN0	X3-29	
TAMPER_IN1	X3-31	
TAMPER_IN2	X3-33	
TAMPER_IN3	X3-37	
TAMPER_IN4	X3-35	

3.2.17 UART

Two of the i.MX 8X's UART interfaces, UART1 and SCU_UART, are routed to the TQMa8Xx connectors and are supported by the BSP provided by TQ-Systems.
They also serve as debug interfaces, UART1 for the ARM core in Linux and the dedicated SCU_UART for the SCU.

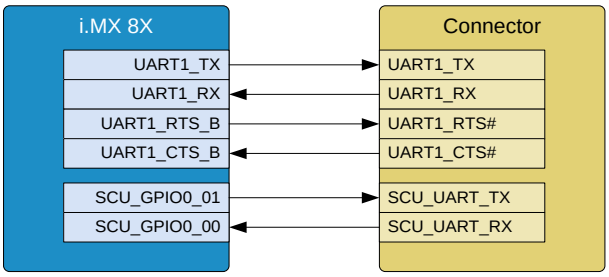


Figure 18: Block diagram UART

Table 26: UART signals

Signal	TQMa8Xx	Power group
UART1_TX	X1-33	V_IO_IN
UART1_RX	X1-35	
UART1_RTS#	X1-37	
UART1_CTS#	X1-39	
SCU_UART_TX	X2-30	V_1V8_ANA
SCU_UART_RX	X2-28	

3.2.18 MCLK

The two inputs MCLK_IN0 and MCLK_IN1 are available as freely usable clock inputs for the i.MX 8X.
For the freely configurable output of a clock, MCLK_OUT0 is also available at the TQMa8Xx connector.

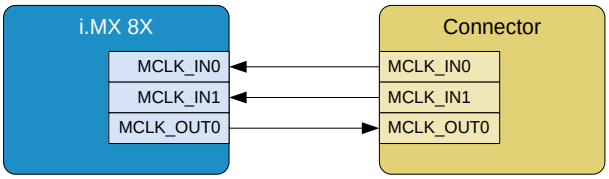


Figure 19: Block diagram MCLK

Table 27: MCLK signals

Signal	TQMa8Xx	Power group
MCLK_IN1	X2-18	V_IO_IN
MCLK_IN0	X2-20	
MCLK_OUT0	X2-16	

3.3 System components

3.3.1 i.MX 8X CPU

3.3.1.1 i.MX 8X derivatives

Depending on the TQMa8Xx version, one of the following i.MX 8X derivatives is assembled.

Table 28: i.MX 8X derivatives

TQMa8Xx variant	CPU derivative	Cortex®-A35 clock	Cortex®-M4 clock	T_{amb}
TQMa8XD-XX	i.MX 8DualX	1.2 GHz	266 MHz	–40 °C to +85 °C
TQMa8XDP-XX	i.MX 8DualXPlus	1.2 GHz	266 MHz	–40 °C to +85 °C
TQMa8XQP-XX	i.MX 8QuadXPlus	1.2 GHz	266 MHz	–40 °C to +85 °C

3.3.1.2 i.MX 8X errata

Attention: Destruction or malfunction, i.MX 8X Errata	
	Please take note of the current i.MX 8X Errata (3).

3.3.1.3 Boot modes

After release of IMX_POR#, the System Controller Unit (SCU) starts from the internal ROM. Depending on the OTP fuses (eFuse) and the boot mode settings of the system controller, the TQMa8Xx boots from the specified boot source:

- eMMC
- QSPI-NOR flash
- SD card

More information about boot interfaces and its configuration is to be taken from the i.MX 8X Data Sheet (1) and the i.MX 8X Reference Manual (2). Alternatively, a binary image can be loaded into the internal RAM via serial downloader.

It is also possible to make further settings in the DCD by the system controller (e.g. DDR timing).

The four BOOT_MODE signals of the i.MX 8X that are required for the boot device configurations are available on the TQMa8Xx connectors. All four BOOT_MODE pins have internal 50 kΩ pull-down resistors. The Boot-Mode must be set with pull-up and pull-down resistors on the carrier board, 4.7 kΩ pull-up and pull-down resistors are recommended. On the carrier board the TQMa8Xx voltage V_1V8_ANA must be used as pull-up voltage.

The following table shows configurations for the available boot devices.

Table 29: Boot-Mode configuration / BT_FUSE_SEL

BOOT_MODE[3:0]	Boot source	Boot interface
0 0 0 0	Boot from eFuse	–
0 0 0 1	Serial Downloader	USB OTG1 or OTG2
0 0 1 0	Boot from eMMC	uSDHC0
0 0 1 1	Boot from SD card	uSDHC1
0 1 0 x	Boot from NAND	(Not supported)
0 1 1 0	Boot from QSPI (3-byte read)	QSPIA / QSPIB
0 1 1 1	Boot from QSPI (Hyperflash)	QSPIA / QSPIB

Note: Field software updates	
	When designing a carrier board, it is recommended to have a redundant update concept for field software updates.

3.3.2 Memory

3.3.2.1 DDR3L SDRAM, TQMa8Xx

Depending on the ECC option, the TQMa8Xx can be equipped with up to three DDR3L memory chips with an effective memory width of 32 bits. The third DDR3L memory chip for the ECC option uses 8 bits.
The CPUs i.MX 8DualXPlus and i.MX 8QuadXPlus support 2 ×16 bits, the i.MX 8DualX supports only 1 ×16 bits, see Table 30.
The interface timing complies with JEDEC standard DDR3-1866 with a maximum IO clock of 933 MHz.

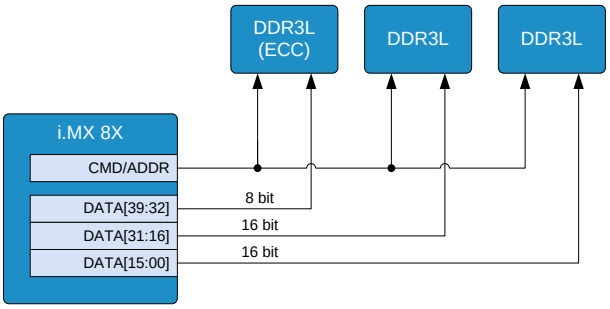


Figure 20: Block diagram DDR3L

Depending on the i.MX 8X derivative, the following SDRAM configurations are possible.

Table 30: DDR3L configuration

i.MX 8X derivative	SDRAM	Remark
i.MX 8DualX	1 × DDR3L ×16	No ECC
i.MX 8DualXPlus	2 × DDR3L ×16	No ECC
	2 × DDR3L ×16 + 1 × DDR3L ×8	With ECC
i.MX 8QuadXPlus	2 × DDR3L ×16	No ECC
	2 × DDR3L ×16 + 1 × DDR3L ×8	With ECC

3.3.2.2 LPDDR4 SDRAM, TQMa8Xx4

The TQMa8Xx4 is equipped with one LPDDR4 memory chip with a memory width of 32 bits. ECC is not available.
The interface timing complies with JEDEC standard LPDDR4-2400, with a maximum IO clock of 1200 MHz.

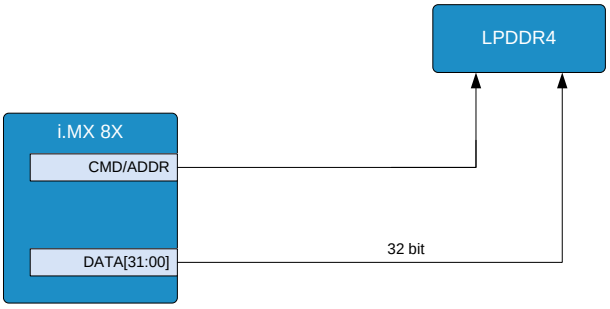


Figure 21: Block diagram LPDDR4

Table 31: LPDDR4 configuration

i.MX 8X derivative	SDRAM	Remark
i.MX 8DualX i.MX 8DualXPlus i.MX 8QuadXPlus	1 × LPDDR4 ×32	No ECC

3.3.2.3 eMMC NAND flash

The TQMa8Xx is assembled with eMMC by default for programs and data (e.g., bootloader, operating system, application).

The i.MX 8X supports MMC card transfer modes up to the current eMMC standard v5.1. This allows a data rate of up to 400 Mbyte/s in DDR mode (HS400).

The eMMC can be used as boot medium. The boot configuration is described in 3.3.1.3.

The eMMC operates in MLC mode by default. Conversion to SLC is possible on request. Please contact TQ-Support for details.

The following block diagram shows the interface of the eMMC to the i.MX 8X:

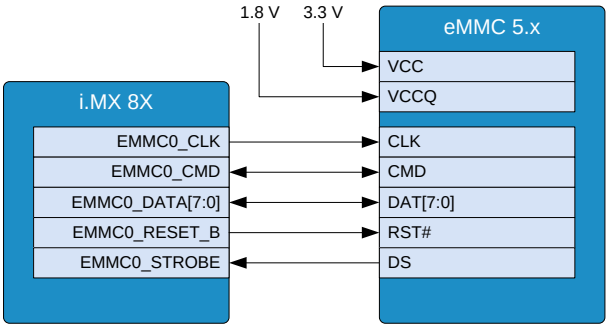


Figure 22: Block diagram eMMC

3.3.2.4 QSPI NOR flash

The i.MX 8X has two QSPI interfaces, which can also be combined into an Octal-SPI or Twin-Quad-SPI if required. On the TQMa8Xx optionally different types of serial NOR-Flashes can be used, which use one or both QSPI interfaces depending on the type. The second QSPI interface (QSPIB) is available on a module connector.

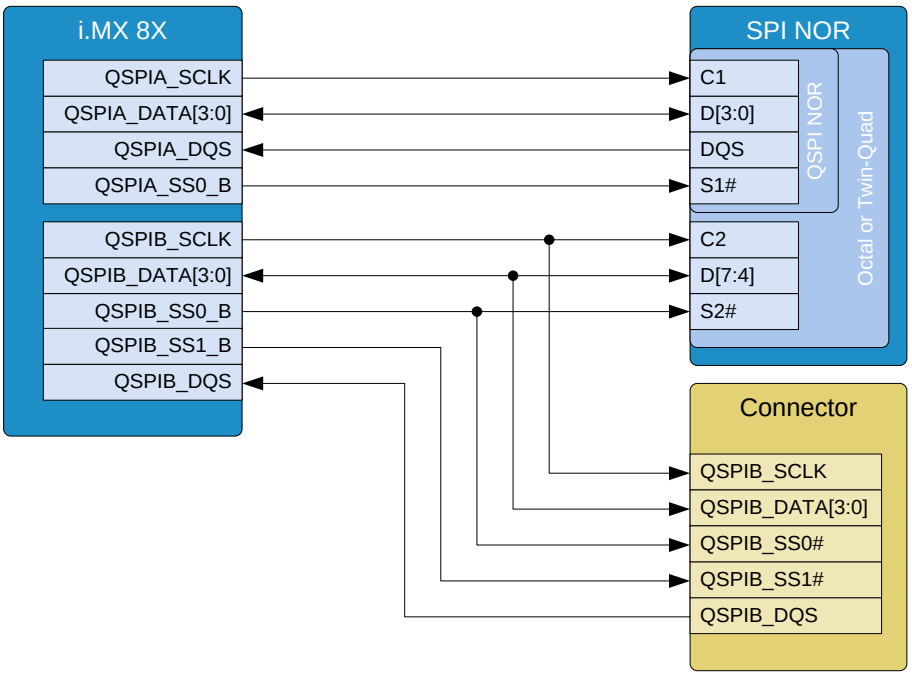


Figure 23: Block diagram QSPI

For TQMa8Xx variants with Octal, Twin Quad, Hyperflash or Xccela flash (or technically comparable types), the QSPIB signals, which are also routed to the TQMa8Xx connectors, are partly provided with pull-up or pull-down resistors on the TQMa8Xx. The following table shows the QSPIB signal wiring with populated Octal, Twin Quad, Hyperflash or Xccela flash.

Table 32: QSPIB signals with populated Octal, Twin Quad, Hyperflash or Xccela flash

Signal	TQMa8Xx	Pull-up / pull-down	Power group
QSPIB_DATA0	X2-105	i.MX 8X-internal PU	1.8 V
QSPIB_DATA1	X2-107	i.MX 8X-internal PU	
QSPIB_DATA2	X2-109	10 kΩ PU	
QSPIB_DATA3	X2-111	10 kΩ PU	
QSPIB_SCLK	X2-101	100 kΩ PD	
QSPIB_SS0#	X2-113	10 kΩ PU	
QSPIB_SS1#	X2-115	–	
QSPIB_DQS	X2-97	–	

3.3.2.5 EEPROM, 24LC64T

A serial 64 Kbit EEPROM type Microchip 24LC64T, controlled by the I2C1 bus, is assembled. Write-Protect (WP#) is not supported.
To store data "read-only", the EEPROM with temperature sensor must be used, see 3.3.2.6.

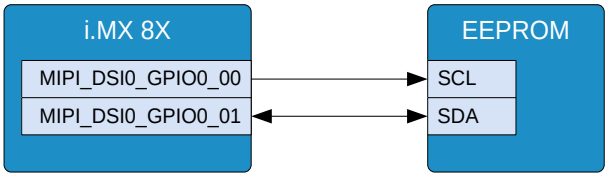


Figure 24: Block diagram 24LC64T EEPROM

- The EEPROM has I²C address `0x57 / 101 0111b`

3.3.2.6 EEPROM with temperature sensor, SE97BTP

A 2 Kbit EEPROM including temperature sensor, controlled by the I2C1 bus, is assembled on the TQMa8Xx.
The lower 128 bytes (00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software.
The upper 128 bytes (80h to FFh) are not write protected and can be used for general purpose.
The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa8Xx.

- The SE97BTP has three I²C addresses:
  - EEPROM (Normal Mode): `0x53 / 101 0011b`
  - EEPROM (Protected Mode): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

The following block diagram shows the interface of the temperature sensor to the i.MX 8X.

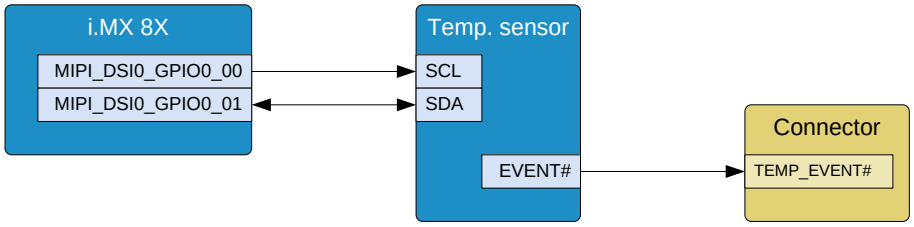


Figure 25: Block diagram SE97BTP temperature sensor

The EEPROM with temperature sensor is assembled on the bottom side of the TQMa8Xx, see Figure 39 or Figure 41, D7.
The over-temperature output of the sensor is connected as open drain to connector X1-4 (TEMP_EVENT#).
A pull-up resistor to 3.3 V (max. 3.6 V) must be provided on the carrier board.
The following table shows details of the temperature sensor.

Table 33: Temperature sensor SE97BTP

Manufacturer	Device	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±1 °C	+75 °C to +95 °C
			Max. ±2 °C	+40 °C to +125 °C
			Max. ±3 °C	–40 °C to +125 °C

3.3.3 RTC

The TQMa8Xx offers two possibilities to use an RTC:

Table 34: TQMa8Xx RTC variants

Variant	Function / description
Without discrete RTC	• i.MX 8X-internal RTC • V_LICELL supplies the i.MX 8X SNVS rail via the VSNVS controller of the PMIC
With discrete RTC	• V_LICELL supplies discrete RTC PCF85063A • i.MX 8X SNVS rail is only supplied when V_3V3_IN is present

3.3.3.1 i.MX 8X-internal RTC

The i.MX 8X has an internal RTC that is powered by its own power rail (SNVS). The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C. The i.MX 8X-internal RTC is supplied via V_LICELL at TQMa8Xx connector X2-23.

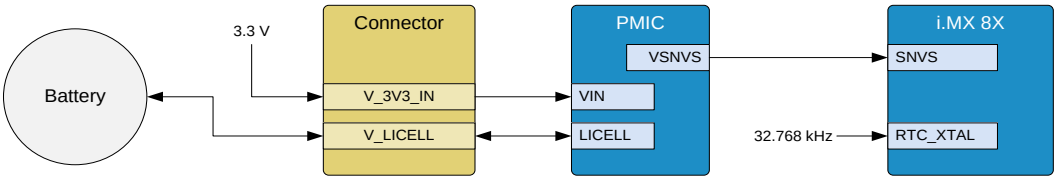


Figure 26: Block diagram RTC, TQMa8Xx without discrete RTC

Note: Current consumption of i.MX 8X-internal RTC	
	The i.MX 8X-internal RTC can always be used in ON-mode since the TQMa8Xx is supplied at V_3V3_IN. In OFF-mode (the TQMa8Xx is not supplied at V_3V3_IN), the i.MX 8X-internal RTC can only be used with TQMa8Xx variants without discrete RTC. For TQMa8Xx variants with discrete RTC, the i.MX 8X-internal RTC resets in case of TQMa8Xx supply failure (3.3 V), since the SNVS rail of the i.MX 8X is no longer supplied in this case. It is not recommended to use the i.MX 8X-internal RTC for extended periods of time, as the current consumption is too high to be sustained by a coin cell battery for an extended period of time.

The following table shows the current consumption at the LICELL pin for TQMa8Xx variants without discrete RTC:

Table 35: Current consumption pin LICELL, i.MX 8X-internal RTC

Voltage LICELL	Current consumption LICELL	Remark
3.2 V	Typical 7.1 µA; maximum 10 µA	V_3V3_IN = 0 V T_{amb} = 25 °C
3.0 V	Typical 7.1 µA; maximum 10 µA	
2.1 V	Typical 6.1 µA; maximum 10 µA	

Given the high current consumption of the SNVS rail, it is recommended to use the discrete RTC, see following chapter.

3.3.3.2 TQMa8Xx discrete RTC

In addition to the i.MX 8X-internal RTC, the TQMa8Xx provides a discrete RTC PCF85063A as an assembly option:
The RTC is connected to the I2C1 bus. I²C addresses see chapter 3.2.4.
The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.
The RTC is supplied by V_LICELL when the PMIC is switched off or the TQMa8Xx supply is switched off.
During runtime, the PMIC takes over the supply via the 3.3 V TQMa8Xx supply.
The interrupt output of the RTC is not connected and can therefore not be used.

- The PCF85063A has I²C address `0x51 / 101 0001b`

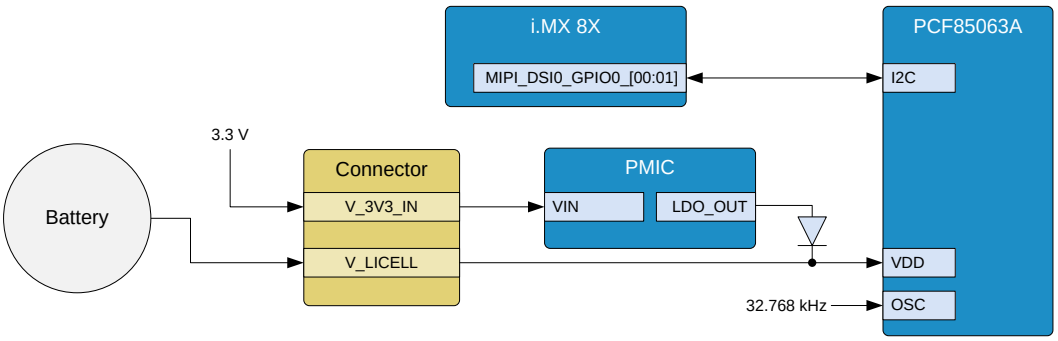


Figure 27: Block diagram discrete RTC supply

Note: Power supply for discrete RTC	
	For TQMa8Xx with populated discrete RTC the SNVS rail is not buffered by V_LICELL. Therefore, the SNVS functions of the i.MX 8X can only be used if the TQMa8Xx supply is available. For TQMa8Xx with discrete RTC, the PMIC's charging function at pin V_LICELL is not available. The RTC is only supplied by V_LICELL when the PMIC or TQMa8Xx supply is switched off. During runtime, the PMIC takes over the supply via the 3.3 V TQMa8Xx supply.

The following table shows the current consumption at the LICELL pin for TQMa8Xx variants with discrete RTC:

Table 36: Current consumption pin LICELL, discrete RTC

Voltage LICELL	Current consumption LICELL	Remark
3.2 V	Typical 0.44 µA; maximum 0.7 µA	V_3V3_IN = 0 V T_{amb} = 25 °C
3.0 V	Typical 0.44 µA; maximum 0.7 µA	
2.1 V	Typical 0.4 µA; maximum 0.7 µA	

3.3.4 Trust Secure Element

Depending on the TQMa8Xx variant, a Trust Secure Element (TSE) is populated on the TQMa8Xx, which is controlled by the I2C1 bus of the i.MX 8X.

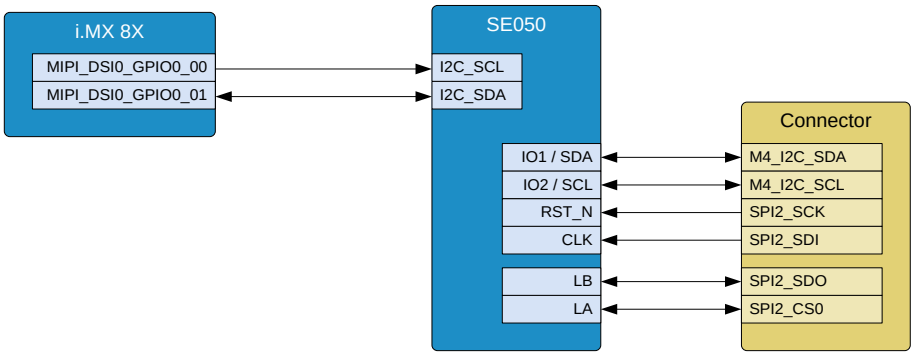


Figure 28: Block diagram Trust Secure Element

In addition to the I²C interface, the TSE SE050 from NXP provides additional smart card interfaces according to ISO 14443 and ISO 7816. The antenna for ISO 14443, or the sensor for ISO 7816, must be connected on the carrier board.
The following TQMa8Xx signals are used to provide the smartcard interfaces.

Table 37: Signals Trust Secure Element

Signal	ISO signal name	TQMa8Xx	Power group
M4_I2C_SDA	ISO 7816 IO1 / SDA	X1-27	3.3 V
M4_I2C_SCL	ISO 7816 IO2 / SCL	X1-29	
SPI2_SCK	ISO 7816 RST#	X1-34	
SPI2_SDI	ISO 7816 CLK	X1-38	
SPI2_SDO	ISO 14443 LB	X1-36	ISO 14443 (Antenna)
SPI2_CS0	ISO 14443 LA	X1-40	

Note: Signal availability	
	For TQMa8Xx variants with populated Trust Secure Element, the signals listed in the above table are disconnected from the i.MX 8X and thus no longer available in their default functions (M4_I2C and SPI2).

- The Trust Secure Element has I²C address `0x48 / 100 1000b`

3.3.5 PMIC

The PMIC PF8100 is used on the TQMa8Xx. The PF8100 is connected to the dedicated I²C bus (PMIC_I2C) of the i.MX 8X. Optionally, the PF8200 can be populated. The PF8200 provides additional safety and monitoring functions that can be used for ASIL requirements. The block diagram shows the available PMIC and power management signals:

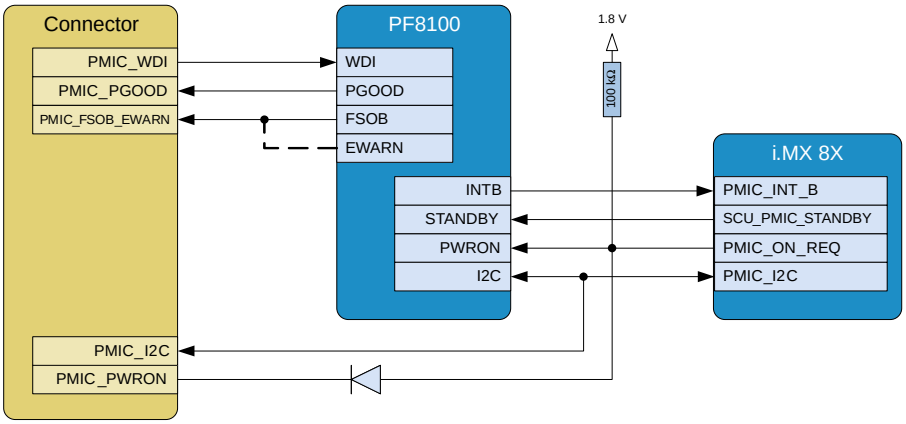


Figure 29: Block diagram PMIC

The following PMIC control and power management signals are available at the TQMa8Xx connectors:

Table 38: PMIC and power management signals

Signal	Dir.	TQMa8Xx	Power rail	Function	Remark
PMIC_WDI	I_{PU}	X1-31	V_1V8_ANA	Watchdog input	• PMIC internal pull-up resistor (1 MΩ). • It is recommended to connect WDI to the watchdog output of the i.MX 8X (SCU_WDOG_OUT)
PMIC_PGOOD	$O_{OD/PU}$	X1-30	V_1V8_ANA	Power-Good indicator	• "Low" when a power rail of the PMIC signals undervoltage or overvoltage • Requires pull-up resistor (100 kΩ) on the carrier board
PMIC_FSOB_EWARN	O_{OD}	X2-25	V_1V8_ANA	Diagnostics output	• Connected to FSOB (default) optionally to EWARN (placement option)
PMIC_I2C_SCL	O	X3-38	V_1V8_ANA	Control interface	• Dedicated PMIC interface • Can be used for power management on carrier board
PMIC_I2C_SDA	I/O	X3-36			
PMIC_PWRON	I_{PU}	X2-27	V_SNVS_CAP (1.8 V)	Enable-Signal for PMIC	• Automatically activated at Power-up by PU on TQMa8Xx • To activate: Float or apply high level (typ. 1.8 V, max. 5.5 V) • To deactivate: Connect to GND

Further information about the characteristics and function of these signals can be found in the PMIC data sheet (4) and the i.MX 8X documentation (1), (2).

3.3.5 PMIC (continued)

Table 39: Voltage levels of PMIC and power management signals

Signal	Parameter	Min.	Typ.	Max.	Remark
Input voltage PMIC_WDI	High level	1.26 V	–	5.5 V	Active high
	Low level	–	–	0.54 V	
Output voltage PMIC_PGOOD	High level	–	–	– [18]	Active high
	Low level	–	–	0.4 V	
Output voltage PMIC_FSOB_EWARN [19]	High level	–	1.8 V	– [20]	Active high
	Low level	–	–	0.4 V	
Input voltage PMIC_PWRON	High level	1.2 V	1.8 V	5.5 V	Active high
	Low level	–	–	0.5 V	

Attention: Malfunction or destruction	
	The PMIC can be controlled via the dedicated i.MX 8X I²C bus (PMIC_I2C). Improper PMIC programming may cause the i.MX 8X or other peripherals on the TQMa8Xx to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa8Xx.

3.3.6 PCIe clock generator, TQMa8Xx4

Depending on the TQMa8Xx4 variant, a Renesas 9FGV0241 PCIe clock generator is populated, which is connected to the I2C1 bus of the i.MX 8X. This clock generator can be used to supply the i.MX 8X and PCIe components connected to the carrier board with a stable PCIe reference clock.

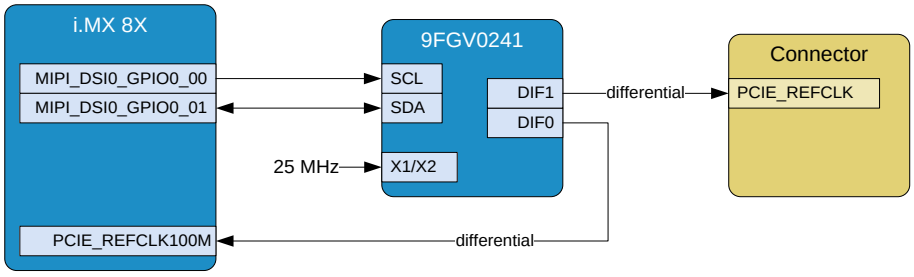


Figure 30: Block diagram PCIe clock generator

➢ The PCIe clock generator on the TQMa8Xx4 has I²C address `0x6A / 110 1010b`

18: External pull-up required. Recommendation: 100 kΩ to 1.8 V, max. 5.5 V.
19: Other technical data apply when using the EWARN signal.
20: A 470 kΩ pull-up is assembled on the TQMa8Xx. Maximum pull-up voltage is 5.5 V.

3.4 Reset

Several Reset input and output signals are available on the TQMa8Xx connectors.

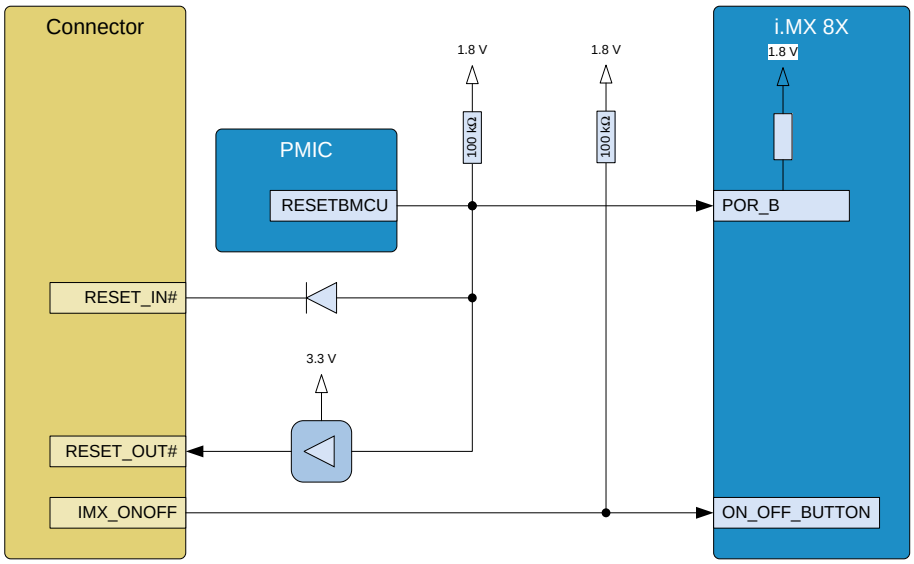


Figure 31: Block diagram Reset

The following table describes the reset and configuration signals available on the TQMa8Xx connector.

Table 40: Reset and configuration signals

Signal	Dir.	Power group	Function	TQMa8Xx	Remark
RESET_IN#	I_{PU}	VDD_ANA_1P8	i.MX 8X Reset input	X2-32	Low Active signal Deactivate: float
RESET_OUT#	O_{OD}	Defined by PU on carrier board	TQMa8Xx Reset output	X2-34	Low Active signal Requires pull-up on carrier board [21]
IMX_ONOFF	I_{PU}	V_SNVS_CAP (1.8 V)	i.MX 8X ON/OFF signal	X1-118	Low Active signal To switch off the CPU, connect the signal to GND for min. 5 s Deactivate: float

Table 41: Voltage levels of Reset and configuration signals

Signal	Parameter	Min.	Typ.	Max.	Remark
Input voltage RESET_IN#	High level	1.2 V	1.8 V	5.5 V	Active low
	Low level	–	–	0.5 V	
Output voltage RESET_OUT#	High level	–	–	– [22]	Active low
	Low level	–	–	0.5 V	
Input voltage IMX_ONOFF	High level	–	– [23]	–	Active low
	Low level	–	–	0.5 V	

21: External pull-up to max. 6.5 V required.
22: External pull-up required (to max. 6.5 V).
23: Signal has internal pull-up and should be floating in the ON-state.

3.5 Power

3.5.1 Power supply

The TQMa8Xx requires a single power supply of 3.3 V ±5 %.
All other voltages are generated on the TQMa8Xx.
The following block diagram shows the TQMa8Xx supply structure:

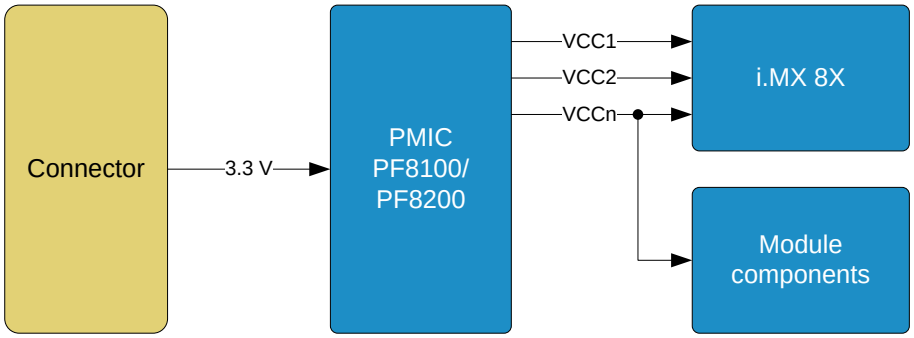


Figure 32: Block diagram power supply TQMa8Xx

3.5.2 V_3V3_IN, power consumption

The power consumption of the TQMa8Xx strongly depends on the application, the mode of operation and the operating system.
For this reason the given values have to be seen as approximate values.
The following table shows power supply and power consumption parameters of the TQMa8Xx:

Table 42: TQMa8Xx current consumption @ 3.3 V

Mode of operation	TQMa8XDP	TQMa8XQP	TQMa8XDP4	TQMa8XQP4	Remark
Power-Off-Mode	62 µA	64 µA	63 µA	62 µA	PMIC_PWRON = low
Reset	160 mA	160 mA	160 mA	160 mA	RESET_IN# = low
U-Boot-Idle	586 mA	596 mA	356 mA	375 mA	Console prompt
Linux-Idle	572 mA	733 mA	356 mA	517 mA	Console prompt
Linux, 100 % CPU load[24]	1046 mA	1468 mA	746 mA	1082 mA	
Full load[25]	3.7 A	3.7 A	3.7 A	3.7 A	Theoretical worst case

[24] If additional interfaces are used in parallel, higher current consumption must be expected.
[25] A theoretically determined value that can be used as a design basis for the module supply.

3.5.3 RTC supply V_LICELL

Coin cells can be connected to the LICELL input of the TQMa8Xx connector (X2-23).

For TQMa8Xx variants without discrete RTC, the voltage at V_LICELL supplies the SNVS rail of the i.MX 8X.

For TQMa8Xx variants with discrete RTC, the SNVS rail is not supplied. In this case V_LICELL supplies the discrete RTC, see chapter 3.3.3 for more information.

Voltage sources with low capacity (e.g. Super-Caps) connected to V_LICELL can be charged. For this purpose the PMIC provides a constant current charging function. Further information can be found in the PMIC data sheet (4).

The following table shows details of the power consumption at the LICELL pin.

Table 43: Characteristics of V_LICELL

V_LICELL	Parameter	Min.	Typ.	Max.	Remark
Input voltage	No discrete RTC	2.8 V	–	4.2 V	
	Discrete RTC	0.9 V	–	5.5 V	
Input current [26]	–	–	220 nA	450 nA	V_3V3_IN = 0 V, T_{amb} = +25 °C
	–	–	250 nA	500 nA	V_3V3_IN = 0 V, T_{amb} = +50 °C
	–	–	470 nA	600 nA	V_3V3_IN = 0 V, T_{amb} = +85 °C
Charging current	PMIC in Run-Mode	–	10 µA	–	
	PMIC in Standby	–	60 µA	–	

Note: Functional scope of RTC	
	Depending on the TQMa8Xx variant, the range of functions is reduced in battery mode (only LICELL supplied), since no SNVS function of the i.MX 8X is available when using the RTC.

3.5.4 V_ENET_IN

The voltage input V_ENET_IN at TQMa8Xx connector X1-107 serves as IO voltage for both Ethernet MACs as well as MDIO/MDC. If the Ethernet interfaces should operate in 1.8 V mode, V_ENET_IN can be connected directly to the TQMa8Xx pin V_1V8_OUT. To configure 3.3 V mode, a separate supply must be provided on the carrier board, which has to be switched on by V_1V8_OUT to comply with the power sequencing of the i.MX 8X. See also chapter 3.5.10 for more information.

Table 44: Ethernet IO voltage V_ENET_IN

Function	Min.	Typ.	Max.	Maximum current
V_ENET_IN: 1.8 V (RGMII)	1.65 V	1.8 V	1.95 V	V_ENET_IN: 114 mA
V_ENET_IN: 3.3 V (RMII)	3.0 V	3.3 V	3.6 V	

26: Values of discrete RTC.

3.5.5 V_IO_IN

The voltage input V_IO_IN at TQMa8Xx connector X2-11 serves as IO voltage for all freely usable GPIO and/or single-ended signals. V_IO_IN must be externally supplied with 1.8 V or 3.3 V. See section 3.2.3 for a description of all affected TQMa8Xx pins.
For 1.8 V mode, V_IO_IN can be connected directly to the TQMa8Xx pin V_1V8_OUT.
To configure 3.3 V mode, a separate supply must be provided on the carrier board, which has to be switched on by V_1V8_OUT to comply with the power sequencing of the i.MX 8X. See also chapter 3.5.10 for more information.

Table 45: GPIO voltage V_IO_IN

Function	Min.	Typ.	Max.	Maximum current
V_IO_IN: 1.8 V	1.65 V	1.8 V	1.95 V	V_IO_IN: 180 mA
V_IO_IN: 3.3 V	3.0 V	3.3 V	3.6 V	

Note: V_IO_IN 3.3 V	
	If 1.8 V are used, V_IO_IN (X2-11) can be connected directly to V_1V8_OUT (X2-12). Since the TQMa8Xx does not provide 3.3 V, an external power supply must be used in this case, which is powered up by V_1V8_OUT to comply with the power sequencing of the i.MX 8X.

3.5.6 V_ADC_IN

The voltage input V_ADC_IN at TQMa8Xx connector X3-34 serves as voltage reference for the ADC of the i.MX 8X.
This voltage is filtered on the TQMa8Xx and connected to pin V_ADC_VREFH of the i.MX 8X.
Further information about the ADC can be found in the data sheet of the i.MX 8X (1).

Note: V_ADC_IN	
	The supply of V_ADC_IN with typically 1.8 V is mandatory, even if the ADC function of the i.MX 8X is not used. Depending on the accuracy requirements, V_1V8_OUT can be used directly for this purpose.

3.5.7 USB_OTG[2:1]_VBUS

The voltage inputs USB_OTG1_VBUS and USB_OTG2_VBUS are used to detect the voltage USB-VBUS.
They are usually connected to the VBUS voltage switched by the USB host.
Due to the different implementations of the OTG PHYs in the i.MX 8X, different voltages must be used for this.

Table 46: USB_OTG[2:1]_VBUS

Signal	TQMa8Xx	Voltage	Usage
USB_OTG1_VBUS	X1-73	5 V	Input for VBUS comparator OTG1
USB_OTG2_VBUS	X1-74	3.3 V	Input for VBUS comparator OTG2

3.5.8 TQMa8Xx, provided voltages

Two supply voltages generated on the TQMa8Xx are available at the TQMa8Xx connectors to use them as supply and control voltages on the carrier board. The voltages are available at the TQMa8Xx pins V_1V8_OUT and V_1V8_ANA.

Table 47: TQMa8Xx, provided voltages

Voltage	TQMa8Xx	Max. current	Usage
V_1V8_OUT	X2-12	0.7 A	• Internal TQMa8Xx supply for periphery and I/O. • Free use on carrier board permitted. • It is strongly recommended to use V_1V8_OUT on the carrier board as switching signal for the power sequencing, see also chapter 3.5.10.
V_1V8_ANA	X2-21	5 mA	• Pull-up voltage for pins BOOT_MODE[3:0]

Voltage V_1V8_OUT has to be used to switch the carrier board supply.

Note: Voltages V_1V8_OUT and V_1V8_ANA	
	Up to 0.7 A can be drawn from V_1V8_OUT, which increases the PMIC's power consumption and thus the TQMa8Xx's self-heating. The BOOT_MODE pins should be pulled-up to V_1V8_ANA, or a voltage switched by V_1V8_ANA. This ensures that the boot mode pins are read-in correctly and that no cross-supply occurs.

Attention: Destruction or malfunction, overload	
	The voltages mentioned are outputs and must not be supplied externally under any circumstances. The outputs are not short-circuit proof. An overload at one of the voltage outputs causes the PMIC to reset and thus resetting the TQMa8Xx.

3.5.9 Voltage monitoring

The 3.3 V input voltage is monitored on the TQMa8Xx.
If the input voltage is too low, a reset is triggered until the input voltage is within the defined range again.

Attention: Destruction or malfunction, overvoltage	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. An excessively high supply voltage can lead to malfunctions, untimely ageing or destruction of the TQMa8Xx.

3.5.10 TQMa8Xx, Power-Up sequence / carrier board

The TQMa8Xx meets the required sequencing of the i.MX 8X by using the PMIC (4).

Since the TQMa8Xx operates at 3.3 V and the 1.8 V I/O voltage of the CPU signals is generated on the TQMa8Xx, the carrier board design must meet requirements regarding the chronological behaviour of the voltages generated on the carrier board.

If TQMa8Xx inputs are supplied by the carrier board, these voltages may only be switched on together with V_1V8_OUT.

The following block diagram shows the suggested voltage regulator control for a carrier board.

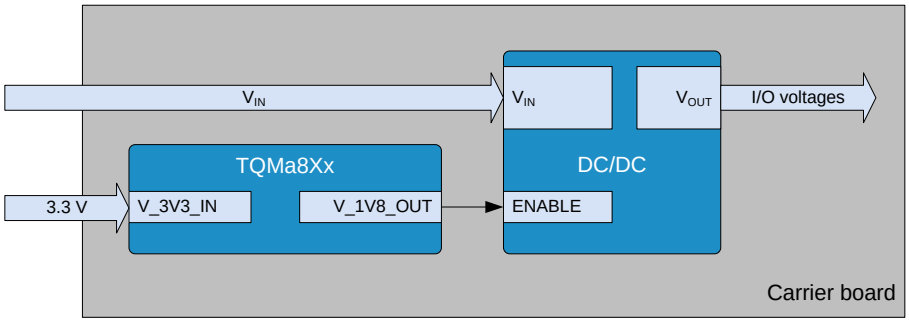


Figure 33: Block diagram power supply carrier board

Attention: Destruction or malfunction, Power-Up sequence	
	To avoid cross-supplies and errors in the power-up sequence of the TQMa8Xx, no I/O pins may be externally supplied or driven until the power-up sequence of the I/O voltages on the TQMa8Xx is completed. At the same time, the carrier board component supply voltages must be stable before the release of RESET_OUT# occurs. This is ensured by activating the carrier board supply voltages by a 1.8 V voltage level at V_1V8_OUT.

4. MECHANICS

4.1 Connectors

The TQMa8Xx is connected to the carrier board with 280 pins on three connectors.

The following table shows details of the connectors used:

Table 48: TQMa8Xx connectors

Manufacturer	Pin count / part number	Remark
TE connectivity	40-pin: 5177985-1 120-pin: 5177985-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

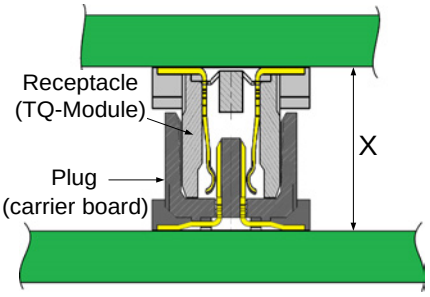
The TQMa8Xx is held in the mating connectors with a retention force of approximately 28 N.

To avoid damaging the connectors of the TQMa8Xx as well as the connectors on the carrier board while removing the TQMa8Xx the use of the extraction tool MOZI8XXL is strongly recommended. See chapter 4.8 for further information.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa8Xx for the extraction tool MOZI8XXL.

The following table shows some suitable mating connectors for the carrier board.

Table 49: Carrier board mating connectors

Manufacturer	Pin count / part number	Remark	Stack height (X)	
TE connectivity	40-pin: 5177986-1 120-pin: 5177986-5	On MBa8Xx	5 mm	
	40-pin: 1-5177986-1 120-pin: 1-5177986-5	–	6 mm	
	40-pin: 2-5177986-1 120-pin: 2-5177986-5	–	7 mm	
	40-pin: 3-5177986-1 120-pin: 3-5177986-5	–	8 mm	

The pin assignment in Table 3 to Table 5 refers to the BSP provided by TQ-Systems in combination with the MBa8Xx.

For information regarding I/O pins in Table 3 to Table 5 refer to the i.MX 8X Data Sheet (1).

4.2 Dimensions

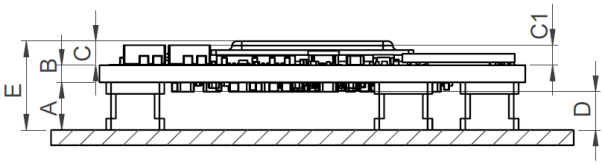


Figure 34: TQMa8Xx dimensions, side view

Table 50: TQMa8Xx heights

Dim.	Value	Tolerance	Remark
A	5.10 mm	±0.07 mm	Board-to-Board distance
B	1.84 mm	±0.18 mm	PCB thickness
C	2.27 mm	±0.15 mm	CPU (highest component)
C1	2.05 mm	±0.11 mm	Inductors
D	3.98 mm	±0.10 mm	Free space under TQMa8Xx
E	9.09 mm	±0.25 mm	Total height above carrier board

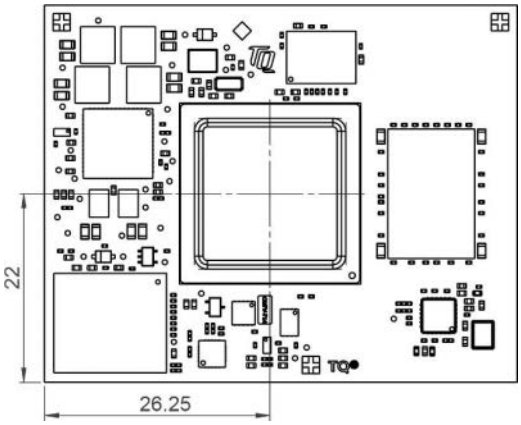


Figure 35: TQMa8Xx4 CPU position

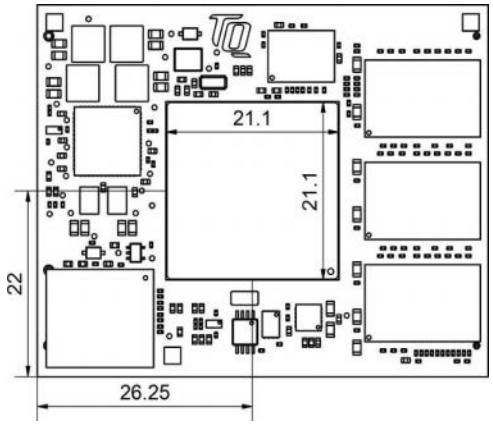


Figure 36: TQMa8Xx CPU position

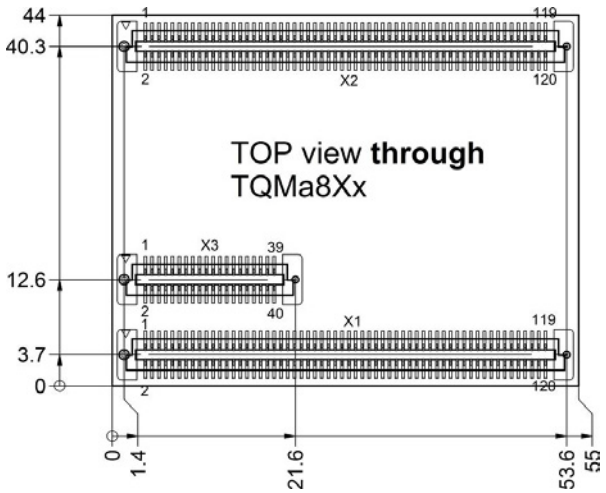


Figure 37: TQMa8Xx, TQMa8Xx4 dimensions, top through-view

4.3 Assembly TQMa8Xx, TQMa8Xx4

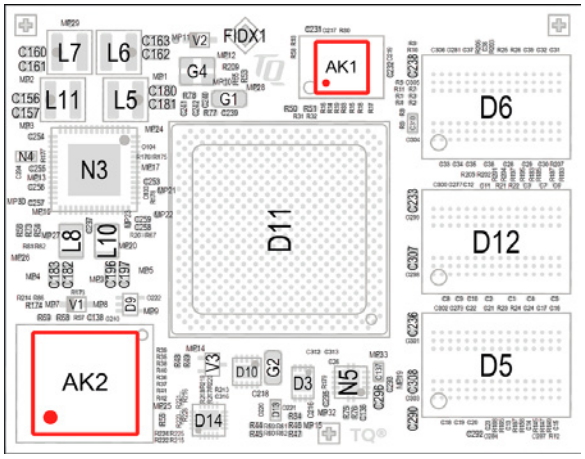


Figure 38: TQMa8Xx, assembly top

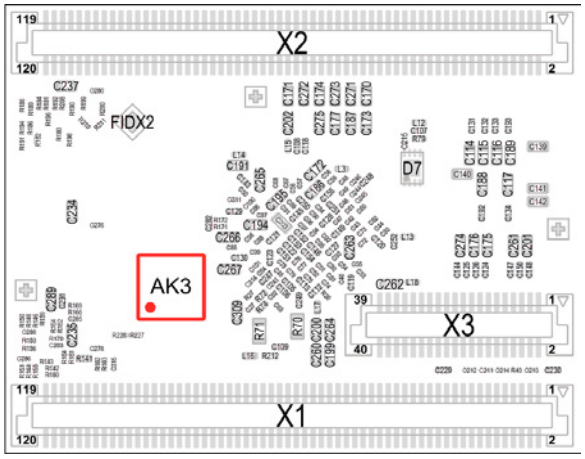


Figure 39: TQMa8Xx, assembly bottom

Table 51: Labels on TQMa8Xx

Label	Content
AK1	Serial number
AK2	First MAC address plus one additional reserved consecutive MAC address, tests performed
AK3	TQMa8Xx version and revision

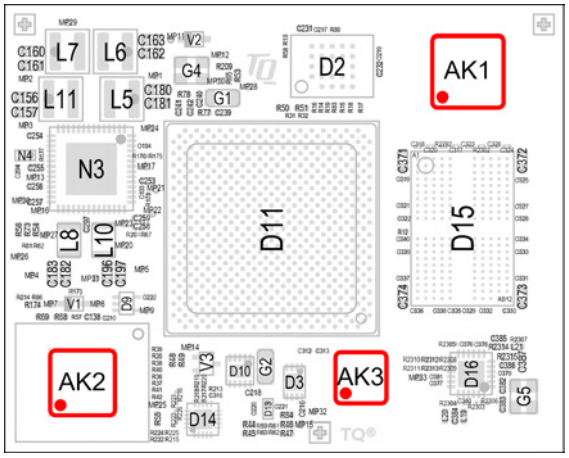


Figure 40: TQMa8Xx4, assembly top

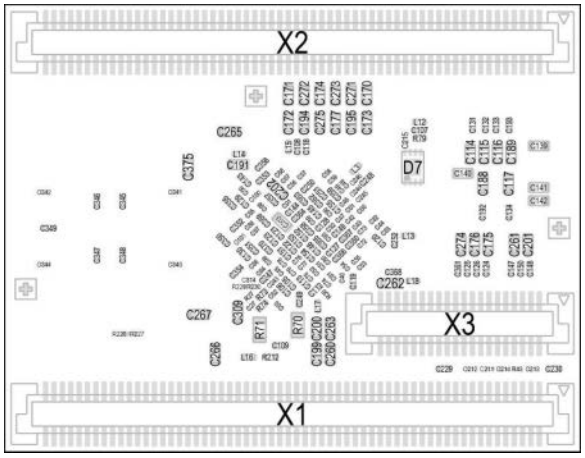


Figure 41: TQMa8Xx4, assembly bottom

Table 52: Labels on TQMa8Xx4

Label	Content
AK1	First MAC address plus one additional reserved consecutive MAC address, tests performed
AK2	TQMa8Xx4 version and revision
AK3	Serial number

4.4 Adaptation to the environment

The TQMa8Xx has overall dimensions (length × width) of 55 × 44 mm².
The TQMa8Xx has a maximum height above the carrier board of approximately 9.1 mm.
The TQMa8Xx weighs approximately 20 g, TQMa8Xx4 weighs approximately 21 g.

4.5 Protection against external effects

As an embedded module, the TQMa8Xx is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa8Xx, in average approximately 4 W must be dissipated, see Table 42.
The power dissipation originates primarily in the i.MX 8X, the SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See i.MX 8X Data Sheet (1) for further information.

Attention: Destruction or malfunction, TQMa8Xx heat dissipation	
	The TQMa8Xx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8X must be taken into consideration when connecting the heat sink. The i.MX 8X is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Xx and thus malfunction, deterioration or destruction.

4.7 Structural requirements

The TQMa8Xx is held in the mating connectors with a retention force of approximately 28 N. For high requirements with respect to shock and vibration, an additional retainer has to be provided in the final product to hold the TQMa8Xx in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

4.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa8Xx may only be extracted from the carrier board by using the extraction tool MOZI8XXL that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa8Xx for the extraction tool MOZI8XXL.

5. SOFTWARE

The TQMa8Xx comes with a preinstalled boot loader U-Boot, which is tailored for the combination of TQMa8Xx and MBa8Xx.
The boot loader U-Boot provides TQMa8Xx-specific as well as board-specific settings, e.g.:

- i.MX 8X configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.
TQ-Systems GmbH provides a Board Support Package, which can be used for evaluation purposes.
More information can be found in the Support Wiki for the TQMa8Xx.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa8Xx was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the TQMa8Xx.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Shock and Vibration

Table 53: Shock resistance

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 msec
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 54: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 ~ 9 Hz, 9 ~ 200 Hz, 200 ~ 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Acceleration	2 Hz to 9 Hz: 3.5 m/s^2 9 Hz to 200 Hz: 10 m/s^2 200 Hz to 500 Hz: 15 m/s^2

6.4 Climate and operational conditions

The operating temperature range for the TQMa8Xx strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa8Xx.
In general, a reliable operation is given when following conditions are met:

Table 55: Climate and operational conditions

Variant	Ambient temperature		Relative humidity, operational / storage	Remark
	Operational	Storage		
C	0 °C to +85 °C	–40 °C to +85 °C	10 % to 90 % not condensing	Consumer
E	–25 °C to +85 °C			Extended (default)
I	–40 °C to +85 °C			Industrial

Table 56: Maximum operating temperatures

Parameter	Temp. range
T_J i.MX 8X	–40 °C to +105 °C
T_J PMIC	–40 °C to +105 °C
Case temperature SDRAM	–40 °C to +85 °C
Case temperature other ICs	Ambient temperature see Table 55

Detailed information concerning the thermal characteristics of the i.MX 8X is to be taken from the NXP documents (1), and (2).

Attention: Destruction or malfunction, TQMa8Xx heat dissipation	
	The TQMa8Xx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8X must be taken into consideration when connecting the heat sink. The i.MX 8X is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8Xx and thus malfunction, deterioration or destruction.

6.5 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.6 Reliability and service life

The calculated MTBF of the TQMa8Xx is 785,441 h @ +40 °C ambient temperature, Ground, Benign.
The calculated MTBF of the TQMa8Xx4 is 979,334 h @ +40 °C ambient temperature, Ground, Benign.
The TQMa8Xx is designed to be insensitive to shock and vibration.
High quality industrial grade connectors are assembled on the TQMa8Xx.

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa8Xx is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa8Xx was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Eco Design Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa8Xx must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa8Xx enable compliance with EuP requirements for the TQMa8Xx.

7.5 Battery

No batteries are assembled on the TQMa8Xx.

7.6 Packaging

The TQMa8Xx is delivered in reusable packaging.

7.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa8Xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa8Xx is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 57: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ASIL	Automotive Safety Integrity Level
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR	Double Data Rate
DDR3L	DDR3 Low voltage
DNC	Do Not Connect
DSI	Display Serial Interface
DVI	Digital Visual Interface
ECC	Error-Correcting Code
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card
ESD	Electrostatic Discharge
EU	European Union
EuP	Energy using Products
GPIO	General-Purpose Input/Output
GPMC	General-Purpose Memory Controller
GPO	General-Purpose Output
HDMI	High Definition Multimedia Interface
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IP00	Ingress Protection 00
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LPDDR4	Low Power DDR4
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MIPI	Mobile Industry Processor Interface
MMC	Multimedia Card
MOZI	Modulzieher (module extractor)
MTBF	Mean (operating) Time Between Failures

8.1 Acronyms and definitions (continued)

Table 57: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
OD	Open Drain
OTG	On-The-Go
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRU	Programmable Real-Time Unit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGB	Red Green Blue
RMII	Reduced Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
SAI	Serial Audio Interface
SATA	Serial ATA
SCU	System Controller Unit
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SNVS	Secure Non-Volatile Storage
SPI	Serial Peripheral Interface
SVHC	Substance of Very High Concern
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment

8.2 References

Table 58: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8X i.MX 8QuadXPlus and 8DualXPlus Data Sheet	Rev. 1, 01/2022	NXP
(2)	i.MX 8X i.MX 8QuadXPlus and 8DualXPlus Reference Manual	Rev. 0, 05/2020	NXP
(3)	i.MX 8X Chip Errata	Rev. 1, 05/2020	NXP
(4)	PF8100 PMIC	Rev. 11, 02/2021	NXP
(5)	MBa8Xx User's Manual	– current –	TQ-Systems
(6)	TQMa8Xx Support-Wiki	– current –	TQ-Systems

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