TQMa67xx
User's Manual

TQMa67xx UM 0100
27.03.2026

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	27.03.2026	M. Kreuzer		Initial release

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TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive devices and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa67xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you power up the TQMa67xx or the Starterkit, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manuals of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa67xx circuit diagram
- MBa67xx User's Manual
- Jacinto™ AM67x Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqmax67xx

2. BRIEF DESCRIPTION

The TQMa67xx is a universal TQ mini module based on the TI Jacinto family AM67x with ARM Cortex A53, Cortex R5F and C7 DSP cores. This User's Manual describes the hardware of the TQMa67xx Rev.020x and refers to some software settings.

It does not replace the AM67x Reference Manual (2).

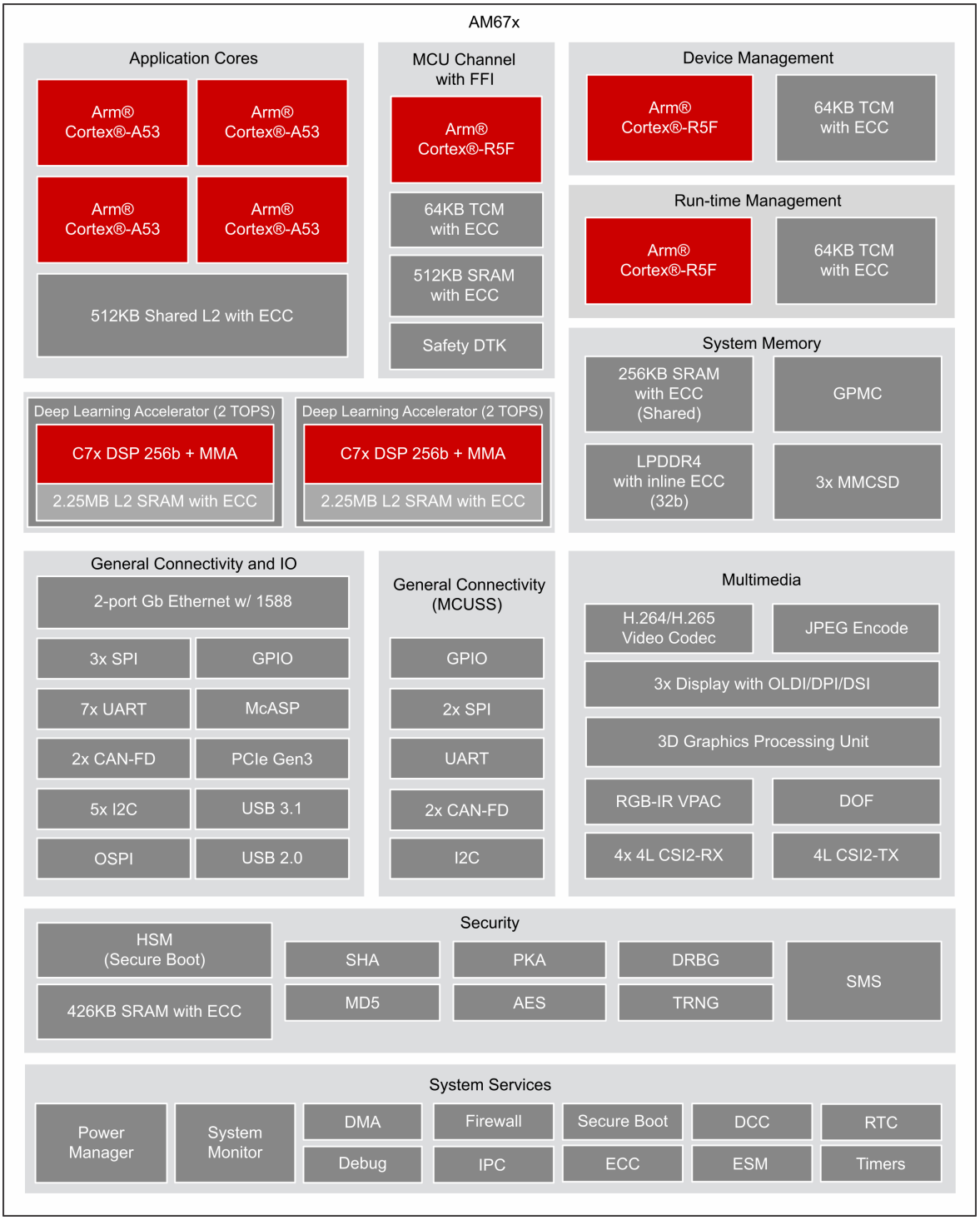


Figure 1: Block diagram AM67x

(Source: Texas Instruments)

All useful AM67x signals are routed to the TQMa67xx connectors (2 x 220 pins). There are no restrictions for customers using the TQMa67xx with respect to an integrated customised design.

Please take note of that not all interfaces can be used simultaneously.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa67xx, and the BSP provided by TQ-Systems GmbH, see also section 4.

3.1 System overview

3.1.1 System architecture / block diagram

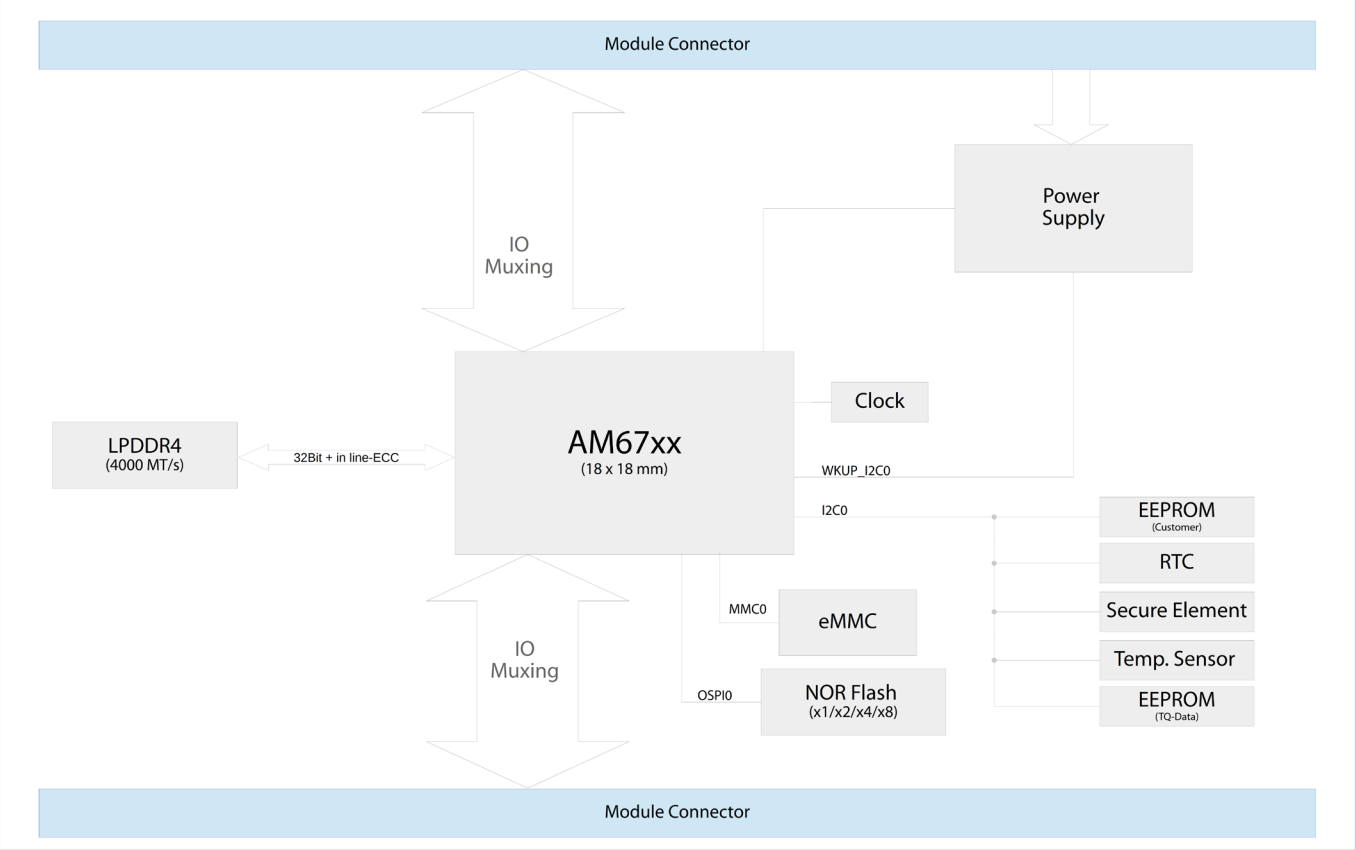


Figure 2: Block diagram TQMa67xx

3.1.2 Functionality

The following key functions are implemented on the TQMa67xx:

- Minimodule in form factor 64 mm x 34 mm
- AM67x processor (up to 4 x A53 and 1x R5F)
- Deep Learning Accelerator with up to 2 x C7x DSP and MMA
- Up to 8 GByte LPDDR4 memory with/without in-line ECC
- Up to 128 GByte eMMC Flash
- Up to 256 Mbyte QSPI Flash (optional)
- Up 64 Kbit customer EEPROM
- 2 Kbit TQ factory EEPROM
- Real-time clock (optional)
- Secure Element chip (optional)
- Temperature sensor (optional)
- Single Power Supply 5.0 V
- Availability of all essential signals of the AM67x at the module connector (2 x 220-pin)

3.1.3 Pin multiplexing

The pin multiplexing of the AM67x permits to use many pins for different interfaces.
The information provided in this User's Manual is based on the BSP provided by TQ-Systems GmbH.

Attention: Destruction or malfunction	
	Many AM67x pins can be configured as different function. Please take note of the information in the AM67 data sheet (1) concerning the configuration of these pins before integration / start-up of your carrier board / Starter kit. Please also take note of the latest AM67x errata (3).

3.2 System components

3.2.1 Processor derivatives

Depending on the TQMa67xx version, one of the following AM67x derivatives is assembled:
AM67A94 / AM67A74 / AM6754 / AM6734

Please refer to the AM67x data sheet (1) for full processor features. The main differences between the AM67x derivatives are as follows:

Feature	Reference Name	AM67A94	AM67A74	AM6754	AM6734
C7x Floating Point, Vector DSP	C7x256V DSP	Dual Core		No	
Deep Learning Accelerator	MMA	Dual Core		No	
Graphics Processing Unit	GPU	Yes	No	Yes	No
Video Encoder / Decoder	VENC/VDEC	Yes			No
Motion JPEG Encoder	JPEG	Yes			No
Depth and Motion Processing Accelerators	DMPAC	Yes		No	
Vision Processing Accelerators	VPAC3L	Yes		No	

3.2.2 Booting

3.2.2.1 Boot source

The boot source is selected via the boot strapping pins of the AM67x. The signals are directly routed to the module connectors and will be available again as GPIO after reading the boot configuration.

After the release of MCU_PORz the boot configuration is read in at the BOOTMODE[15:0] pins. Independent of the boot device, the ROM bootloader is executed first, which assists in reading and executing the application code. The data can be read and loaded either directly from the memory device or by a peripheral.

The following figure shows the implementation of boot strapping on the module:

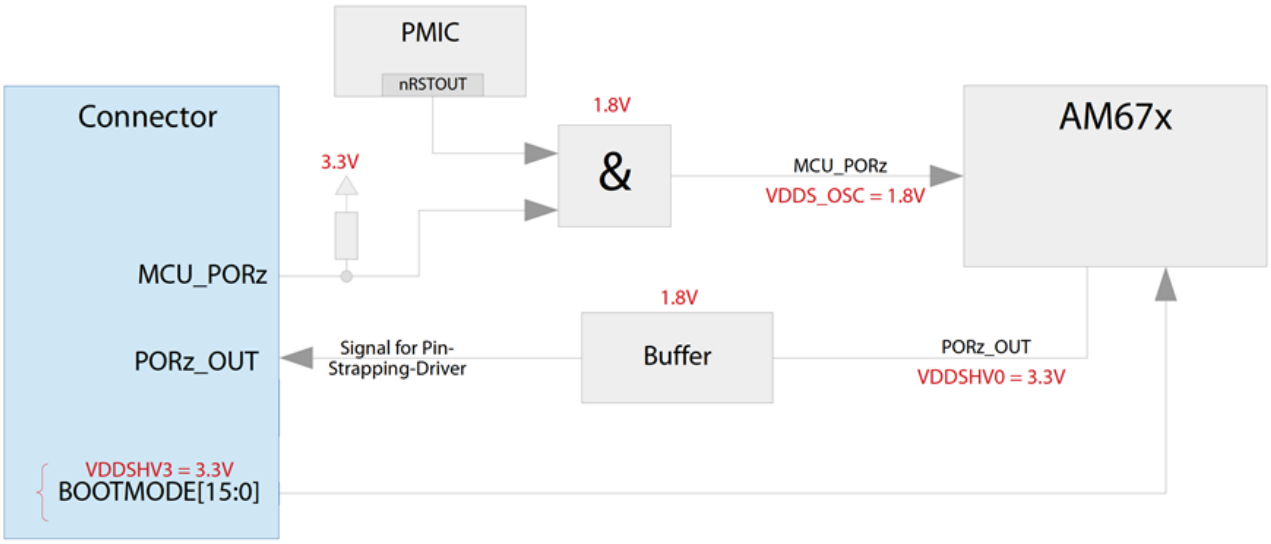


Figure 3: Block diagram boot strapping

According to the Reference Manual (2) the general boot configuration at the TQMa67xx can be set as follows:

Table 2: Selecting the General Boot Configuration

Boot configuration pin	Setting	TQMa67xx
BOOTMODE[15:14]	Reserved, fixed to 0	00
BOOTMODE[13:10]	Select the backup boot mode, if primary boot device failed	Don't care
BOOTMODE[9:3]	See following chapters for primary boot devices	-
BOOTMODE[2:0]	Ref Clock Select: 000 = reserved 001 = reserved 010 = 24 MHz 011 = 25 MHz 100 = 26 MHz 101 = reserved 110 = reserved 111 = reserved	011

Attention: Malfunction	
	All BOOTMODE[15:00] signals must have either a pullup (to V_3V3) or pulldown (to Ground). Undefined levels can lead to a malfunction during booting.

3.2.2.2 Boot device eMMc

Table 3: Boot device selection eMMC

Boot configuration pin	Setting	TQMa67xx
BOOTMODE[9]	Port: MMCSD Port 0 (8 bit width) This bit must be set to 0	000
BOOTMODE[8]	Reserved	
BOOTMODE[7]	0 = Filesystem Mode 1 = Raw Mode	
BOOTMODE[6:3]	Primary Boot Mode: 0000 = Serial NAND 0001 = OSPI 0010 = QSPI 0011 = SPI 0100 = Ethernet RGMII 0101 = Ethernet RMII 0110 = I2C 0111 = UART 1000 = MMCSD boot 1001 = eMMC Boot 1010 = USB 1011 = GPMC NAND 1100 = GPMC NOR 1101 = Fast-xSPI 1110 = xSPI 1111 = No-boot/Dev boot	1000

3.2.2.3 Boot device NOR-flash

Table 4: Selection of the boot device NOR flash

Boot configuration pin	Setting	TQMa67xx
BOOTMODE9	Reserved, fixed to 0	Don't Care
BOOTMODE8	SPI mode: 0 = SPI Mode 0 1 = SPI Mode 3	0
BOOTMODE7	Chip-Select: 0 = Boot-Flash is on CS0 1 = Boot-Flash is on CS1	0
BOOTMODE[6:3]	Primary Boot Mode: 0000 = Serial NAND 0001 = OSPI 0010 = QSPI 0011 = SPI 0100 = Ethernet RGMII 0101 = Ethernet RMII 0110 = I2C 0111 = UART 1000 = MMCSD Boot 1001 = eMMC Boot 1010 = USB 1011 = GPMC NAND 1100 = GPMC NOR 1101 = Fast-xSPI 1110 = xSPI 1111 = No-boot/Dev boot	0011

Further boot configurations can be found in the Reference Manual (2).

Besides the mentioned boot configurations above, it is recommended to consider an alternative boot source during development, e.g. USB boot or no-boot mode for JTAG debug.

Note: Update	
	When designing a mainboard, it is recommended to plan a redundant update concept for software updates in the field. Furthermore, it is recommended to switch the conversion of the boot strap pins to high impedance after reading in.

3.2.3 Memory

3.2.3.1 LPDDR4 SDRAM

The TQMa67xx has LPDDR4 memory with the use of in-line ECC:

- 32-bit bus width with optional ECC (24-bit data + 8-bit ECC). 1/9th of the total SDRAM space is used for ECC storage.
- Up to 4000 Mbps = 2000 MHz
- 1 GByte (=8 Gbit) / 2 GByte (=16 Gbit) / 4 GByte (=32 Gbit) / 8 GByte (=64 Gbit)

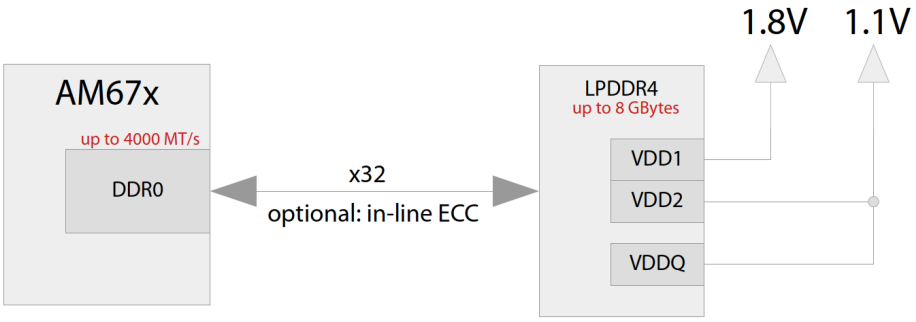


Figure 4: Block diagram LPDDR4 SDRAM connection

3.2.3.2 eMMC

An eMMC is available to the TQMa67xx as non-volatile data memory for programs and data (e.g. boot loader, operating system). The MMC0 signals that are used can be made available on the module connector as an option.

- MMC0 is connected to the eMMC Flash
- 8 / 16 / 32 / 64 /128 GByte

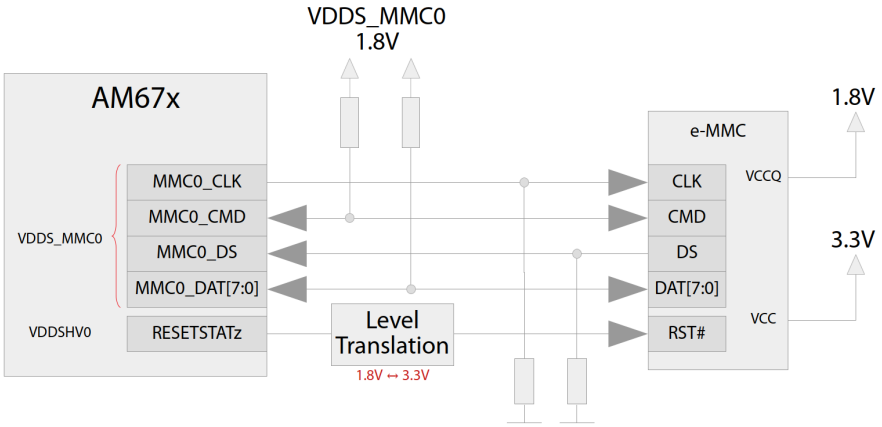


Figure 5: Block diagram eMMC flash interface

The TQMa67xx supports the following transmission modes:

Table 5: eMMC Flash modes

Mode	1-bit	4-bit	8-bit	Note
Default Speed	n/a	n/a	n/a	
High Speed	n/a	n/a	Yes	Boot process
HS200	n/a	n/a	Yes	U-boot / Linux (default)
HS400	n/a	n/a	n/a	

3.2.3.3 NOR-Flash

A NOR-Flash on the TQMa67xx is available as non-volatile memory. The OSPI0 signals that are used can be made available on the module connector as an option.

- The NOR-Flash variants Quad SPI Flash and Octal SPI Flash are usable
- 512 / 1024 / 2048 Mbit

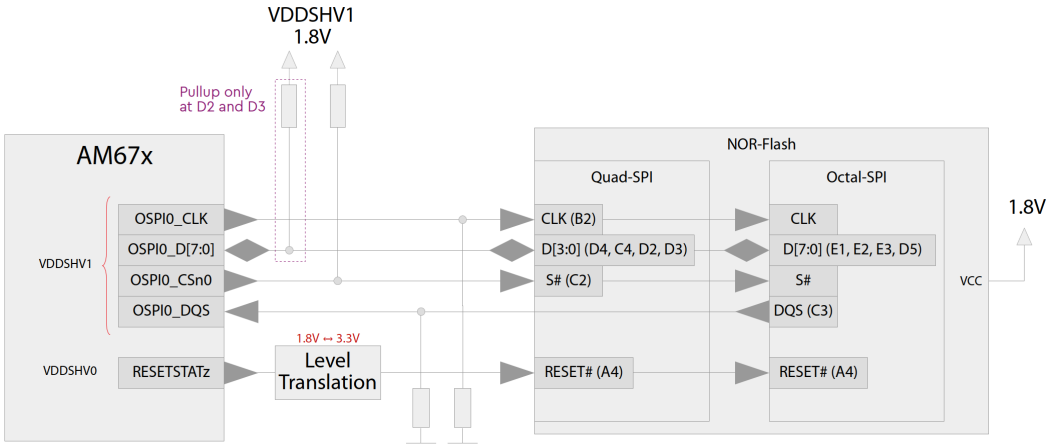


Figure 6: Block diagram NOR-Flash

The TQMa67xx supports the following transmission modes:

Table 6: NOR-Flash modes

Mode	Read	Write	Note
Extended SPI (SDR)	1-4-4	1-1-4	Clock = max. 83.33 MHz

3.2.3.4 EEPROMs

I²C EEPROMs are provided on the TQMa67xx for non-volatile storage. A distinction is made here between:

- Customer data, freely accessible
- TQ manufacturing data (Serial Number, MAC, ...)

All I²C slave address and bus structure are summarized in chapter 3.2.8.3.

3.2.4 Clock supply

The clock supply of the TQMa67xx is represented as follows:

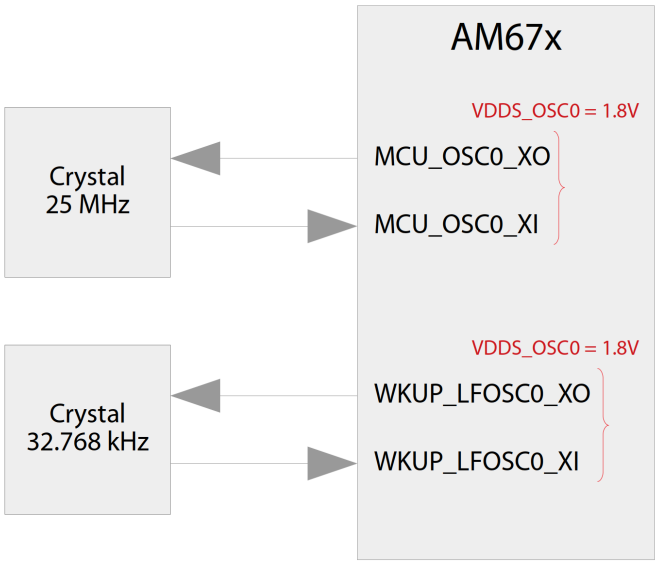


Figure 7: Block diagram clock supply

To get the module executable only with a 5.0 V supply, MCU_OSC0_XO / XI and WKUP_LFOSC_XO / XI are implemented as clock on the module.

The remaining clock inputs can either be derived from the system clock or fed externally via the module connectors, as an example the following clocks can be fed externally:

- EXT_REFCLK1
- MCU_EXT_REFCLK0 (optional external System Clock inputs)
- CP_GMAC_CPTS0_RFT_CLK (optional CPTS Reference Clock input)
- AUDIO_EXT_REFCLK0/1 (optional, External Clock input to McASP)
- SERDES0/1_REFCLK0N/P (optional, Serdes PHY Reference Clock input)
- …

For more information, please refer to the relevant datasheet (1).

3.2.5 RTC

An optional RTC (NXP PCF85063A) can be equipped on the TQMa67xx. The connection is realized as follows:

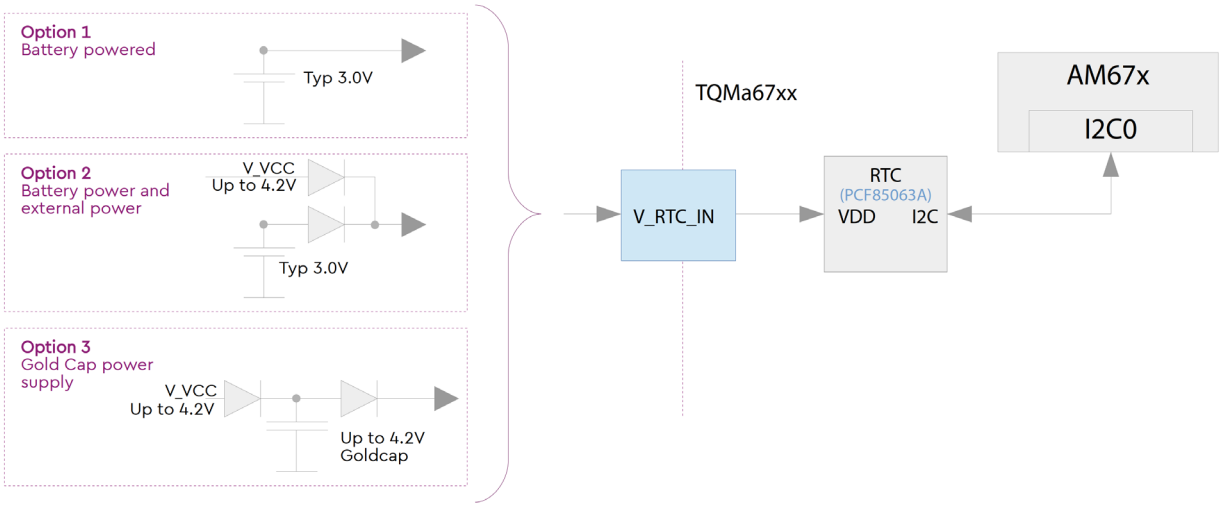


Figure 8: Block diagram RTC

- The RTC can be supplied from the base board via V_RTC_IN. V_RTC_IN = 2.0 V to 4.2 V
- RTC_INT# and RTC_CLKOUT is accessible at the module connectors.
- RTC_CLKOUT is only activated as soon as the TQMa67xx is supplied with V_5V_IN.
- I2C is connected via I2C0 (I^2C addresses are described in chapter 3.2.8.3)

Note: Equipping the base board	
	The RTC is supplied directly via V_RTC_IN. This allows the user an easy use of Gold-Caps or Coin cells on the main board.

3.2.6 Secure Element

A Secure Element Chip can optionally be fitted on the TQMa67xx. The connection can be seen in the following figure:

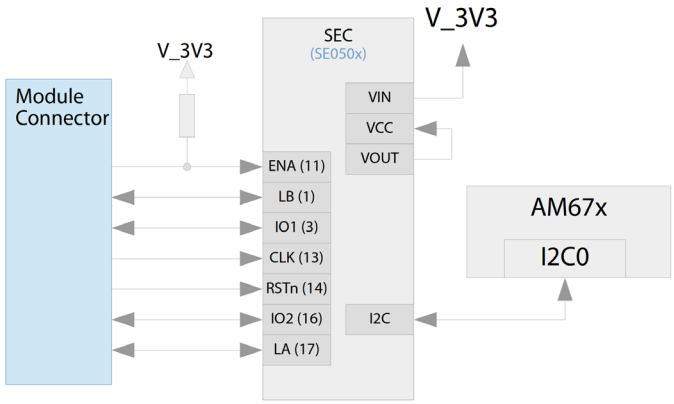


Figure 9: Block diagram SEC

The SE050E2HQ1/Z01Z3 from NXP is used as the secure element. All I^2C addresses are described in chapter 3.2.8.3.

3.2.7 Temperature sensor

A temperature sensor (TI TMP1075DSGR) is placed on the TQMa67xx to monitor the module temperature.
The over temperature output (TEMP_ALERT) of the sensor is available at the module connectors as an open drain output.
The I²C addresses are described in chapter 3.2.8.3.

3.2.8 Interfaces

In general, except for the memory connection, all IO pins of the AM67x are provided at the module connectors.
For further information about the interfaces and the pin multiplexing refer to the Processor Reference Manual (2).

3.2.8.1 GPIO

Besides their interface function, most AM67x pins can also be used as GPIOs. Details are to be taken from the AM67x Data Sheet (1).

3.2.8.2 JTAG

The AM67x has a JTAG interface that is directly accessible at the module connectors. The following default configuration is provided on the TQMa67xx:

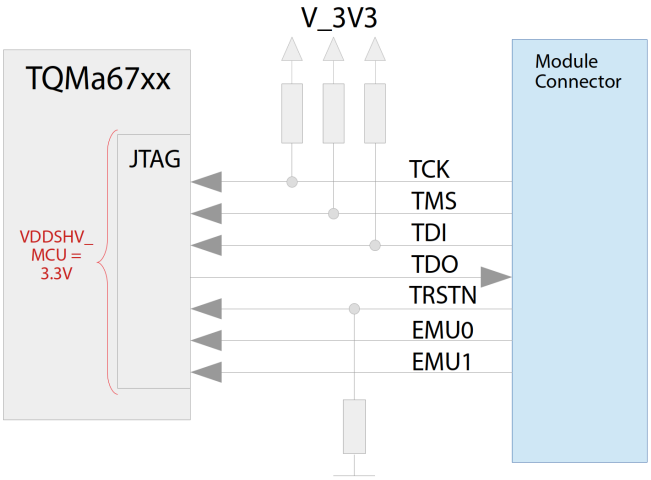


Figure 10: Block diagram JTAG

The following table shows the signals used by the JTAG interface.

Table 7: JTAG signals

Signal / Multiplexing	I/O	Power domain	Note
TCK	I	VDDSHV_MCU (3.3 V)	10 kΩ Pull-up on module
TDI	I		10 kΩ Pull-up on module
TDO	OZ		
TMS	I		10 kΩ Pull-up on module
TRST#	I		4.7 kΩ Pull-up on module
EMU[1:0]	IO		Optional signals, not required for JTAG

For more information please refer to the Reference Manual (2).

3.2.8.3 I²C

The accessible I²C buses depend on the pin multiplexing. To use the internal I²C devices, the WKUP_I2C0- and I2C0-bus are permanently provided on the TQMa67xx. The following devices are connected to the module:

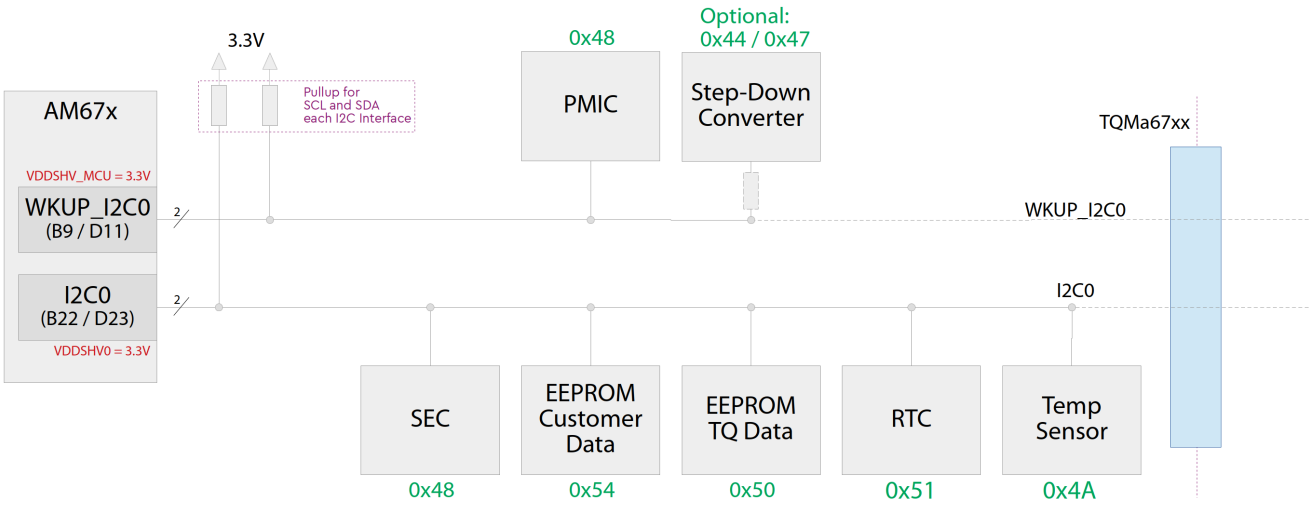


Figure 11: Block diagram I2C bus on the TQMa67xx

Table 8: I2C address assignment on the module

Bus	Component	Address	Note
WKUP_I2C	PMIC TPS652G1	0b1001000 / 0x48	
	DC/DC	0b1000100 / 0x44 0b1000111 / 0x47	Optional
I2C0	Temperature sensor TMP1075	0b1001010 / 0x4A	
	EEPROM M24C02	0b1010000 / 0x50	TQ-Data
	EEPROM M24C64	0b1010100 / 0x54	Customer EEPROM
	RTC PCF85063ATL	0b1010001 / 0x51	
	SEC	0b1001000 / 0x48	

3.2.9 Reset

The following figure describes the implementation of the reset structure of the TQMa67xx:

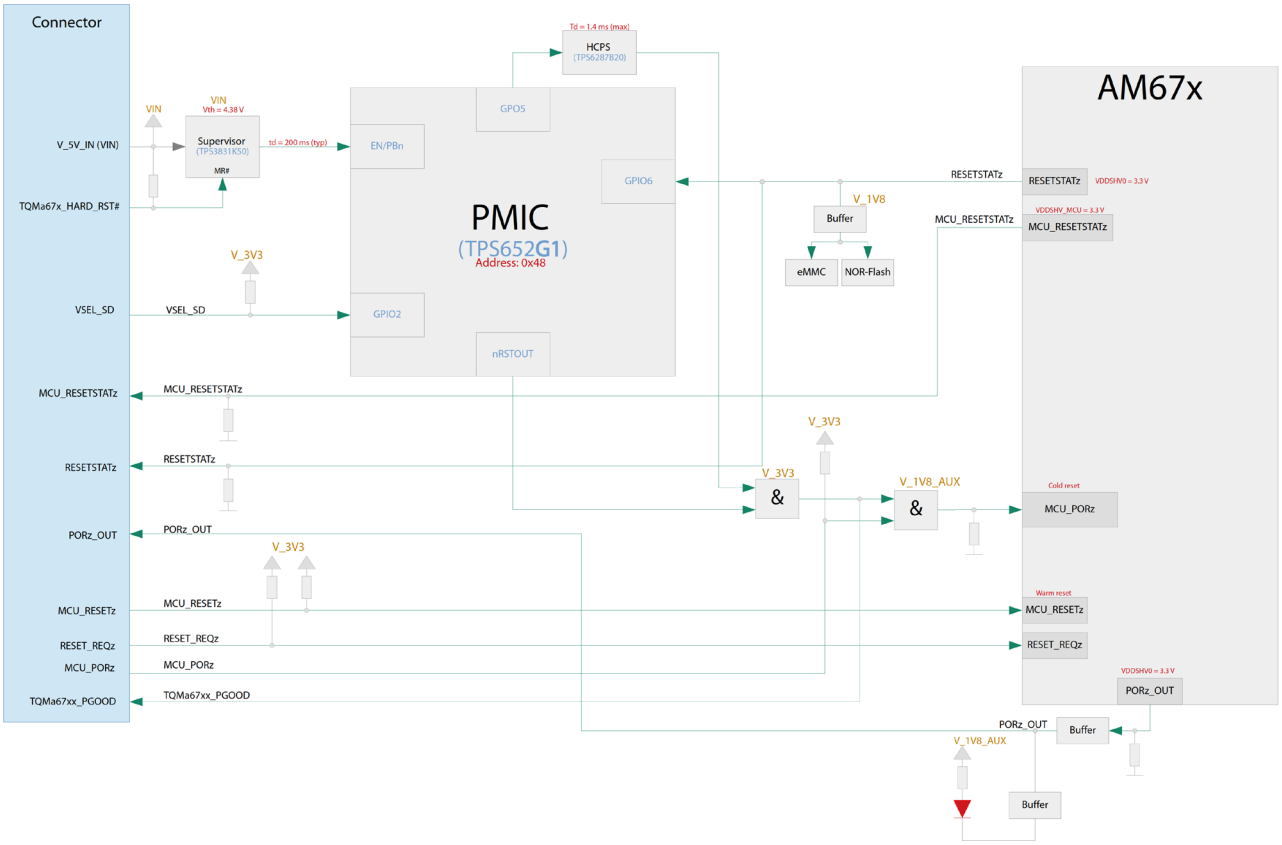


Figure 12: Block diagram Reset

3.2.9.1 Reset Options (Input)

3.2.9.1.1 TQMa67xx_HARD_RST#

The input signal TQMa67xx_HARD_RST# is used to control the entire module. Coming from the module connectors a reset with power cycle of the module is executed. As soon as the signal becomes HIGH, the power-up sequencing takes place after a delay of approx. 200 ms.

Per default the signal is connected with a pullup to V_5V_IN (5.0 V), therefore only a LOW can reset the module with power cycle.

3.2.9.1.2 MCU_PORz

The MCU_PORz signal is used to control a cold reset. Between the module connector signal MCU_PORz and the AM67x MCU_PORz signal is an AND element and a PMIC, which keeps the signal at LOW during power sequencing and pulls it HIGH afterwards.

By default the signal is connected with a pullup to 3.3 V, so only a LOW can trigger a cold reset of the module.

3.2.9.1.3 MCU_RESETz

The MCU_RESETz signal is used to control a warm reset of the MCU domain of the AM67x.

By default the signal is connected to a pullup to 3.3 V, so only a LOW can trigger a warm reset of the MCU domain on the module.

3.2.9.1.4 RESET_REQz

The RESET_REQz signal is used to control a warm reset of the main domain of the AM67x.

By default the signal is connected to a pullup to 3.3 V, so only a LOW can trigger a warm reset of the main domain on the module.

3.2.9.2 Reset Status (Output)

3.2.9.2.1 PORz_OUT

The PORz_OUT signal serves as status signal for a cold reset of the main domain of the AM67x.

By default the signal is driven via a buffer with 1.8 V.

3.2.9.2.2 MCU_RESETSTATz

The MCU_RESETSTATz signal serves as a status signal for a warm reset of the MCU domain.

By default the signal is connected with a pulldown to ground.

3.2.9.2.3 RESETSTATz

The RESETSTATz signal serves as a status signal for a warm reset of the main domain.

By default the signal is connected with a pulldown to ground.

3.2.9.3 Control signals

3.2.9.3.1 TQMa67xx_PGOOD

TQMa67xx_PGOOD serves as a status signal to the base board that the voltages on the main board can now be switched on. Power GOOD (PGOOD) is only active when the power sequencing on the module has been successfully completed.

By default the signal is driven via a buffer with 3.3 V

3.2.9.3.2 VSEL_SD

VSEL_SD is used to select the V_VDDSHV5 supply voltage:

- LOW: V_VDDSHV5 = 1.8 V
- HIGH: V_VDDSHV5 = 3.3 V

By default the signal is connected with a pullup to 3.3 V, thus initially V_VDDSHV5 is always supplied with 3.3 V.

3.2.10 Power supply

3.2.10.1 Main power supply

The main supply of the TQMa67xx is defined to typ. 5.0 V. By applying the 5.0 V voltage the module generates all required voltages.

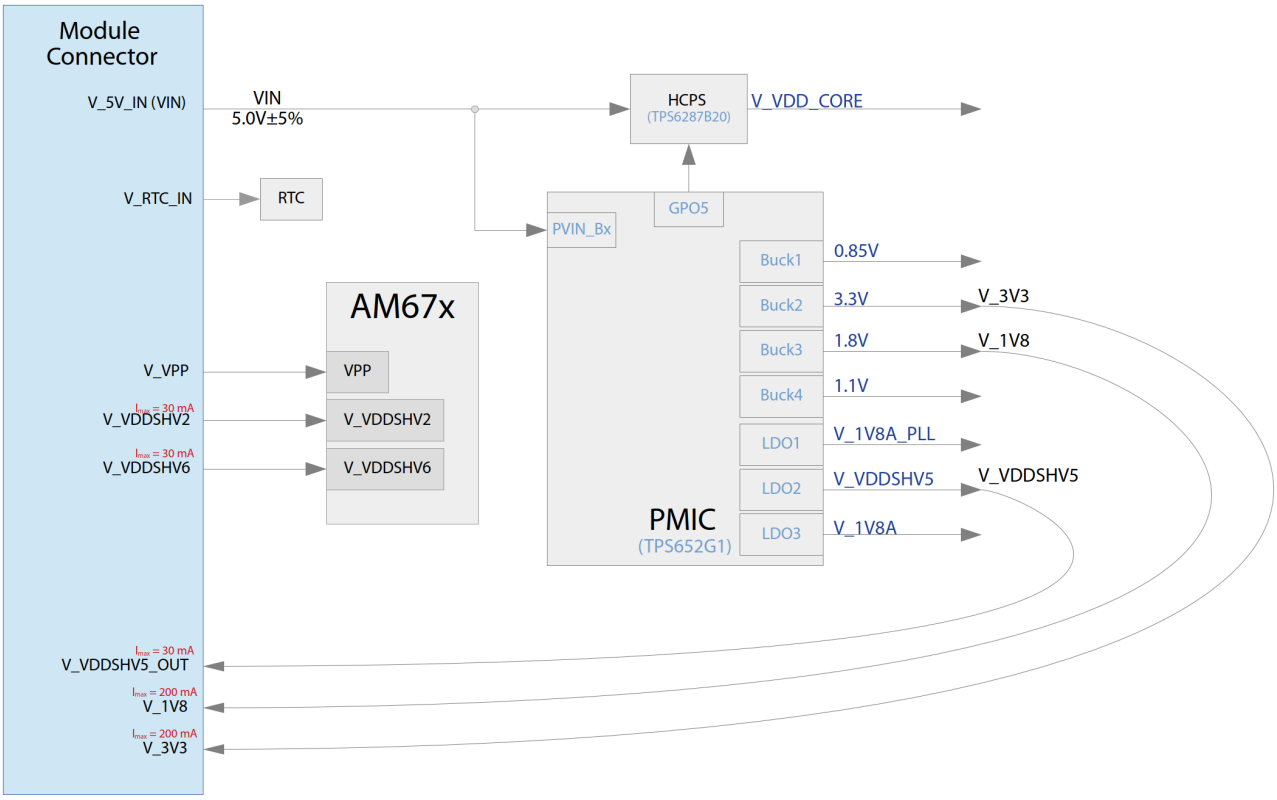


Figure 13: Block diagram power supply

3.2.10.2 Overview TQMa67xx supply

The following table shows all relevant supply voltages of the TQMa67xx.

Table 9: Supply voltages

Module pin / Signal	Voltage	Current	Use
V_5V_IN	4.75 V to 5.25 V	see Table 11	Input: module supply
V_3V3	3.201 V to 3.399 V	max. 100 mA	Output: for Boot-Configuration
V_1V8	1.746 V to 1.854 V	max. 100 mA	Output
V_VDDSHV5	1.8 V / 3.3 V	< 30 mA	Output: MMC1 IO-Bank supply
V_RTC_IN	2.0 V to 5.5 V	see 3.2.5	Input: supply for module RTC
V_VPP	1.8 V	max. 400 mA	Input: supply for eFuse programming
V_VDDSHV2	1.8 V / 3.3 V	max. 30 mA	Input: can be supplied by V_3V3 / V_1V8
V_VDSSHV6	1.8 V / 3.3 V	max. 30 mA	Input: can be supplied by V_3V3 / V_1V8
USB0_VBUS USB1_VBUS	typ. 5 V	< 1 mA	Input: Used to detect the USB-VBUS voltage and is usually supplied with the VBUS voltage switched by the USB host. External circuitry is required – see (2).

Attention: Malfunction	
	If the absolute maximum voltages of the AM67x are exceeded, malfunctions and component failures may occur. The mentioned outputs may not be supplied externally under any circumstances.

3.2.10.3 Power sequencing

After switching on the module supply V_5V_IN and TQMa67xx_HARD_RST# to HIGH the power-up sequence starts. With completion of the power sequencing the supply of the external mainboard components is signaled via TQMa67xx_PGOOD. The following figure shows the chronological sequence of the signals involved.

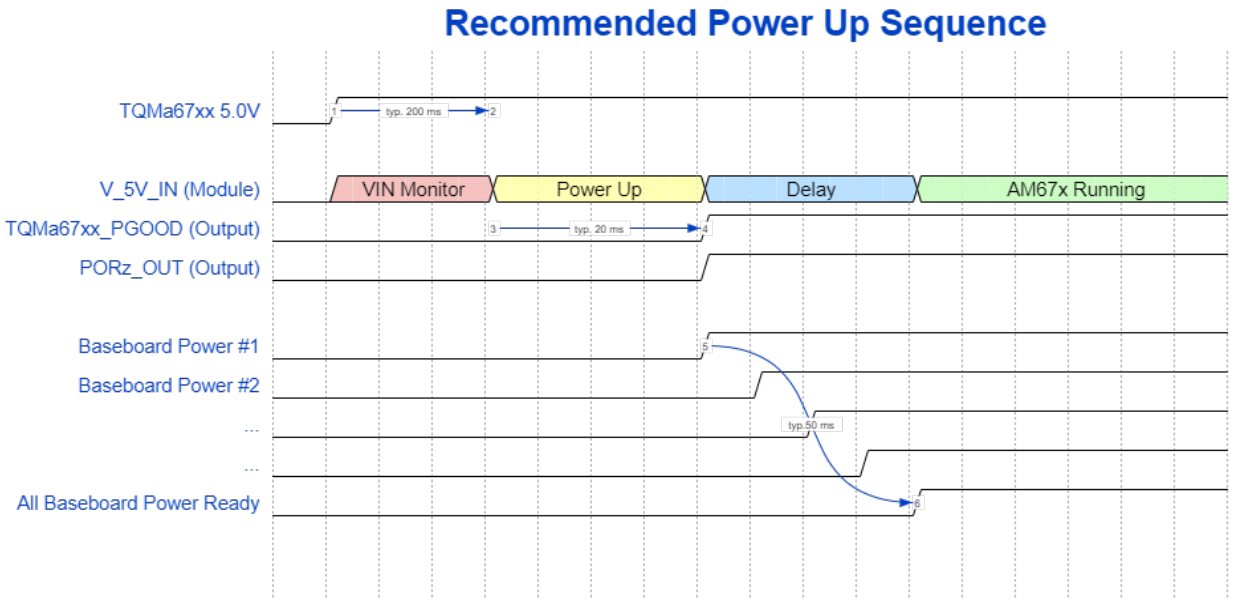


Figure 14: Recommended power up sequence

Attention: Malfunction	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence is completed. The end of the power-up sequence is signaled by a high level of the TQMa67xx_PGOOD signal.

3.2.10.4 Power modes

The TQMa67xx has the following power modes:

- Active Mode - The module is powered and everything is active.

Depending on the use of the processor, different power / module domains can be switched off. For more information, refer to the AM67x Reference Manual (2).

Independent of the AM67x, the following low power modes can be provided:

- Module RTC Mode
  - Module is no longer supplied via V_5V_IN
  - Only V_RTC_IN remains supplied and active
  - The current consumption is then determined solely by the current consumption of the RTC
- Self-Refresh Mode (Suspend to RAM)
  - The LPDDR4 memory can be set to self-refresh mode using an SRE command.
  - IDD6 is specified in self-refresh, typ. current consumption at 25 °C ambient temperature is approx. 0.4 mA to 2.7 mA

3.2.10.5 Power consumption

The following table lists some technical parameters of the module supply. The specified current consumptions are to be regarded as a guide value. Since the current consumption of the TQMa67xx can differ greatly depending on the application, modes and operating system, the values listed here should only be used for a performance estimate.

Table 10: Current consumption TQMa67xx

TQMa67A94 (16Gbit LPDDR4, 512 Mbit NOR-Flash, 8 GByte eMMC-Flash)		
Current consumption Power OFF	13 mA	TQMa67xx_HARD_RST# = LOW
Current consumption Reset mode	192 mA	MCU_PORz = LOW
Current consumption theoretical Worst Case	4.8 A	Current consumption @ 5.0 V
Current consumption U-Boot prompt	419 mA	U-Boot Idle
Current consumption Linux prompt	507 mA	Linux Idle
Current consumption Linux (stressapptest -W -s 407500 -M 1408 -m 4 -C 4 -i 4 stress-ng --cpu-load 95 --cpu 4 --timeout 407500)	660 mA	Higher current consumption must be expected when using additional interfaces in parallel

3.3 TQMa67xx interface

3.3.1 Pin assignment

The TQMa67xx has a total of 440 pins, divided between two module connectors X1 and X2 (each 402-51101-51). Possible connector counterparts for the base board are EPT 401-51101-51 and 401-55101-51 which provide a board-to-board distance of 5 mm and 8 mm. Connector samples are available from: https://www.ept-connectors.com/ncrwl/index.php?tq-colibri-lp-en

The electrical and pin characteristics are to be taken from the AM67x (1).

Attention: Destruction or malfunction	
	The multiple pin configurations of all AM67x internal function units must be taken note of. The pin assignment shown in Table 11 / Table 12 refers to the corresponding BSP provided by TQ-Systems GmbH.

3.3.2 Pinout TQMa67xx

Table 11: Pinout X1

CPU Ball	IO	Level	Group	Signal	Pin	Pin	Signal	Group	Level	IO	CPU Ball
-	P			DGND	X1-A1	X1-B1	DGND			P	-
R22	IO	3.3 V	GPMC0	GPMC0_AD0	X1-A2	X1-B2	GPMC0_AD8	GPMC0	3.3 V	IO	U27
R23	IO	3.3 V	GPMC0	GPMC0_AD1	X1-A3	X1-B3	GPMC0_AD9	GPMC0	3.3 V	IO	U26
R26	IO	3.3 V	GPMC0	GPMC0_AD2	X1-A4	X1-B4	GPMC0_AD10	GPMC0	3.3 V	IO	V27
T27	IO	3.3 V	GPMC0	GPMC0_AD3	X1-A5	X1-B5	GPMC0_AD11	GPMC0	3.3 V	IO	V25
-	P			DGND	X1-A6	X1-B6	DGND			P	-
T25	IO	3.3 V	GPMC0	GPMC0_AD4	X1-A7	X1-B7	GPMC0_AD12	GPMC0	3.3 V	IO	V26
T24	IO	3.3 V	GPMC0	GPMC0_AD5	X1-A8	X1-B8	GPMC0_AD13	GPMC0	3.3 V	IO	V24
T21	IO	3.3 V	GPMC0	GPMC0_AD6	X1-A9	X1-B9	GPMC0_AD14	GPMC0	3.3 V	IO	V22
T22	IO	3.3 V	GPMC0	GPMC0_AD7	X1-A10	X1-B10	GPMC0_AD15	GPMC0	3.3 V	IO	V23
-	P			DGND	X1-A11	X1-B11	DGND			P	-
N21	O	3.3 V	GPMC0	GPMC0_ADV#_ALE	X1-A12	X1-B12	GPMC0_CLK	GPMC0	3.3 V	O	T23
P27	O	3.3 V	GPMC0	GPMC0_BE0#_CLE	X1-A13	X1-B13	DGND			P	-
P26	O	3.3 V	GPMC0	GPMC0_BE1#	X1-A14	X1-B14	GPMC0_CS0#	GPMC0	3.3 V	O	R27
N25	O	3.3 V	GPMC0	GPMC0_DIR	X1-A15	X1-B15	GPMC0_CS1#	GPMC0	3.3 V	O	P21
V21	I	3.3 V	GPMC0	GPMC0_WAIT0	X1-A16	X1-B16	GPMC0_CS2#	GPMC0	3.3 V	O	P22
W26	I	3.3 V	GPMC0	GPMC0_WAIT1	X1-A17	X1-B17	GPMC0_CS3#	GPMC0	3.3 V	O	P23
N24	O	3.3 V	GPMC0	GPMC0_WP#	X1-A18	X1-B18	DGND			P	-
N22	O	3.3 V	GPMC0	GPMC0_OE#_RE#	X1-A19	X1-B19	MCAN0_TX	MCAN0	3.3 V	O	D22
N23	O	3.3 V	GPMC0	GPMC0_WE#	X1-A20	X1-B20	MCAN0_RX	MCAN0	3.3 V	I	C22
-	P			DGND	X1-A21	X1-B21	DGND			P	-
K27	IO	1.8 V	OSPI0	OSPI0_D0_CON	X1-A22	X1-B22	OSPI0_CLK_CON	OSPI0	1.8 V	O	L24
L27	IO	1.8 V	OSPI0	OSPI0_D1_CON	X1-A23	X1-B23	DGND			P	-
L26	IO	1.8 V	OSPI0	OSPI0_D2_CON	X1-A24	X1-B24	DGND			P	-
L25	IO	1.8 V	OSPI0	OSPI0_D3_CON	X1-A25	X1-B25	OSPI0_LBCLKO	OSPI0	1.8 V	IO	L23
-	P			DGND	X1-A26	X1-B26	OSPI0_CS1#	OSPI0	1.8 V	O	K23
L21	IO	1.8 V	OSPI0	OSPI0_D4_CON	X1-A27	X1-B27	OSPI0_CS2#	OSPI0	1.8 V	O	K22
M26	IO	1.8 V	OSPI0	OSPI0_D5_CON	X1-A28	X1-B28	OSPI0_CS3#	OSPI0	1.8 V	O	J22
N27	IO	1.8 V	OSPI0	OSPI0_D6_CON	X1-A29	X1-B29	OSPI0_DQS_CON	OSPI0	1.8 V	I	L22
M27	IO	1.8 V	OSPI0	OSPI0_D7_CON	X1-A30	X1-B30	OSPI0_CS0#_CON	OSPI0	1.8 V	O	K26
-	P			DGND	X1-A31	X1-B31	DGND			P	-
B22	IO	3.3 V	I2C0	I2C0_SDA	X1-A32	X1-B32	PMIC_LPM_EN0	System	3.3 V	O	A8
D23	IO	3.3 V	I2C0	I2C0_SCL	X1-A33	X1-B33	RTC_INT#	RTC	3.3 V	O	-
A22	IO	3.3 V	I2C1	I2C1_SDA	X1-A34	X1-B34	PCIE0_CLKREQ	PCIE0	3.3 V	IO	F25
C24	IO	3.3 V	I2C1	I2C1_SCL	X1-A35	X1-B35	DGND			P	-
-	P			DGND	X1-A36	X1-B36	WKUP_CLKOUT0	WKUP	3.3 V	O	F12
J21	I	1.8 V / 3.3 V	Power	V_VDDSHV6	X1-A37	X1-B37	DGND			P	-
-	P			DGND	X1-A38	X1-B38	EXT_REFCLK1	EXT	3.3 V	I	A23
E19	IO	3.3 V	SPI0	SPI0_D0	X1-A39	X1-B39	DGND			P	-
E20	IO	3.3 V	SPI0	SPI0_D1	X1-A40	X1-B40	MCASP0_ACLKX	MCASP0	3.3 V	IO	D25
-	P			DGND	X1-A41	X1-B41	DGND			P	-
D20	IO	3.3 V	SPI0	SPI0_CLK	X1-A42	X1-B42	MCASP0_AFSX	MCASP0	3.3 V	IO	C26
-	P			DGND	X1-A43	X1-B43	MCASP0_AXR2	MCASP0	3.3 V	IO	A26
B20	IO	3.3 V	SPI0	SPI0_CS0	X1-A44	X1-B44	MCASP0_AXR3	MCASP0	3.3 V	IO	A25
C20	IO	3.3 V	SPI0	SPI0_CS1	X1-A45	X1-B45	DGND			P	-
F18	I	max. 3.6 V	USB1	USB1_VBUS	X1-A46	X1-B46	MCASP0_ACLKR	MCASP0	3.3 V	IO	F24

3.3.2 Pinout TQMa67xx (Table continued)

CPU Ball	IO	Level	Group	Signal	Pin	Pin	Signal	Group	Level	IO	CPU Ball
B27	O	3.3 V	USB1	USB1_DRVVBUS	X1-A47	X1-B47	DGND			P	-
-	P			DGND	X1-A48	X1-B48	MCASP0_AFSR	MCASP0	3.3 V	IO	C27
E17	IO	-	USB1	USB1_DM	X1-A49	X1-B49	MCASP0_AXR0	MCASP0	3.3 V	IO	F23
D17	IO	-	USB1	USB1_DP	X1-A50	X1-B50	MCASP0_AXR1	MCASP0	3.3 V	IO	B25
-	P			DGND	X1-A51	X1-B51	DGND			P	-
A20	I	-	SERDES0	SERDES0_RX0_N	X1-A52	X1-B52	SERDES1_RX0_N	SERDES1	-	I	C14
A19	I	-	SERDES0	SERDES0_RX0_P	X1-A53	X1-B53	SERDES1_RX0_P	SERDES1	-	I	C15
-	P			DGND	X1-A54	X1-B54	DGND			P	-
B19	O	-	SERDES0	SERDES0_TX0_N	X1-A55	X1-B55	SERDES1_TX0_N	SERDES1	-	O	A13
B18	O	-	SERDES0	SERDES0_TX0_P	X1-A56	X1-B56	SERDES1_TX0_P	SERDES1	-	O	A14
-	P			DGND	X1-A57	X1-B57	DGND			P	-
A17	IO	-	SERDES0	SERDES0_REFCLK0_N	X1-A58	X1-B58	SERDES1_REFCLK0_N	SERDES1	-	IO	B15
A16	IO	-	SERDES0	SERDES0_REFCLK0_P	X1-A59	X1-B59	SERDES1_REFCLK0_P	SERDES1	-	IO	B16
-	P			DGND	X1-A60	X1-B60	DGND			P	-
-	I	5.0 V	Reset	TQMa67xx_HARD_RST#	X1-A61	X1-B61	MCU_ERROR#	System	1.8 V	IO	B7
B23	I	3.3 V	System	EXTINT#	X1-A62	X1-B62	MCU_RESETz	Reset	3.3 V	I	D10
E27	O	3.3 V	Reset	RESETSTATz	X1-A63	X1-B63	MCU_RESETSTATz	Reset	3.3 V	O	E13
D27	O	1.8 V	Reset	PORz_OUT	X1-A64	X1-B64	MCU_PORz	Reset	3.3 V	I	E8
-	O	3.3 V	TEMP	TEMP_ALERT	X1-A65	X1-B65	TQMa67xx_PGOOD	System	3.3 V	O	-
T19	I	1.8V / 3.3V	Power	V_VDDSHV2	X1-A66	X1-B66	RESET_REQz	Reset	3.3 V	I	E26
-	P			DGND	X1-A67	X1-B67	DGND			P	-
E11	IO	3.3 V	MCU_I2C0	MCU_I2C0_SDA	X1-A68	X1-B68	WKUP_I2C0_SDA	WKUP_I2C0	3.3 V	IO	D11
B13	IO	3.3 V	MCU_I2C0	MCU_I2C0_SCL	X1-A69	X1-B69	WKUP_I2C0_SCL	WKUP_I2C0	3.3 V	IO	B9
-	P			DGND	X1-A70	X1-B70	DGND			P	-
E22	I	3.3 V	UART0	UART0_CTS#	X1-A71	X1-B71	EMU0	Debug	3.3 V	IO	C9
B21	O	3.3 V	UART0	UART0_RTS#	X1-A72	X1-B72	EMU1	Debug	3.3 V	IO	F9
F20	O	3.3 V	UART0	UART0_TXD	X1-A73	X1-B73	RFU1	-	-	-	-
F19	I	3.3 V	UART0	UART0_RXD	X1-A74	X1-B74	RFU2	-	-	-	-
-	P			DGND	X1-A75	X1-B75	RFU3	-	-	-	-
B8	I	3.3 V	MCU_UART0	MCU_UART0_RXD	X1-A76	X1-B76	WKUP_UART0_RXD	WKUP_UART0	3.3 V	I	B3
B4	O	3.3 V	MCU_UART0	MCU_UART0_TXD	X1-A77	X1-B77	WKUP_UART0_TXD	WKUP_UART0	3.3 V	O	C8
B5	I	3.3 V	MCU_UART0	MCU_UART0_CTS#	X1-A78	X1-B78	WKUP_UART0_CTS#	WKUP_UART0	3.3 V	I	C4
C5	O	3.3 V	MCU_UART0	MCU_UART0_RTS#	X1-A79	X1-B79	WKUP_UART0_RTS#	WKUP_UART0	3.3 V	O	C3
-	P			DGND	X1-A80	X1-B80	DGND			P	-
A9	IO	3.3 V	MCU_SPI0	MCU_SPI0_CLK	X1-A81	X1-B81	USB0_DP	USB0	-	IO	AA6
-	P			DGND	X1-A82	X1-B82	USB0_DM	USB0	-	IO	AB5
B12	IO	3.3 V	MCU_SPI0	MCU_SPI0_D0	X1-A83	X1-B83	DGND			P	-
C11	IO	3.3 V	MCU_SPI0	MCU_SPI0_D1	X1-A84	X1-B84	USB0_VBUS	USB0	max. 3.6 V	I	W7
C12	IO	3.3 V	MCU_SPI0	MCU_SPI0_CS0	X1-A85	X1-B85	USB0_DRVVBUS	USB0	3.3 V	O	E25
A10	IO	3.3 V	MCU_SPI0	MCU_SPI0_CS1	X1-A86	X1-B86	DGND			P	-
-	P			DGND	X1-A87	X1-B87	DGND			P	-
B2	O	3.3V	MCU_MCAN0	MCU_MCAN0_TX	X1-A88	X1-B88	MCU_MCAN1_TX	MCU_MCAN1	3.3V	O	C1
D8	I	3.3V	MCU_MCAN0	MCU_MCAN0_RX	X1-A89	X1-B89	MCU_MCAN1_RX	MCU_MCAN1	3.3V	I	B1
-	P			DGND	X1-A90	X1-B90	DGND			P	-

3.3.2 Pinout TQMa67xx (Table continued)

CPU Ball	IO	Level	Group	Signal	Pin	Pin	Signal	Group	Level	IO	CPU Ball
E12	I	3.3 V	Debug	TDI	X1-A91	X1-B91	TCK	Debug	3.3 V	I	A11
F10	O	3.3 V	Debug	TDO	X1-A92	X1-B92	DGND			P	-
B10	I	3.3 V	Debug	TRST#	X1-A93	X1-B93	TMS	Debug	3.3 V	I	F11
-	P			DGND	X1-A94	X1-B94	DGND			P	-
AC12	I	1.8 V	CSI2	CSI2_RXP3	X1-A95	X1-B95	CSI3_RXP3	CSI3	1.8 V	I	AC16
AC13	I	1.8 V	CSI2	CSI2_RXN3	X1-A96	X1-B96	CSI3_RXN3	CSI3	1.8 V	I	AC15
-	P			DGND	X1-A97	X1-B97	DGND			P	-
AD12	I	1.8 V	CSI2	CSI2_RXP2	X1-A98	X1-B98	CSI3_RXP2	CSI3	1.8 V	I	AD14
AD11	I	1.8 V	CSI2	CSI2_RXN2	X1-A99	X1-B99	CSI3_RXN2	CSI3	1.8 V	I	AD15
-	P			DGND	X1-A100	X1-B100	DGND			P	-
-	P			DGND	X1-A101	X1-B101	DGND			P	-
AG9	I	1.8 V	CSI2	CSI2_RXCLKP	X1-A102	X1-B102	CSI3_RXCLKP	CSI3	1.8 V	I	AG11
AG8	I	1.8 V	CSI2	CSI2_RXCLKN	X1-A103	X1-B103	CSI3_RXCLKN	CSI3	1.8 V	I	AG12
-	P			DGND	X1-A104	X1-B104	DGND			P	-
AE11	I	1.8 V	CSI2	CSI2_RXP1	X1-A105	X1-B105	CSI3_RXP1	CSI3	1.8 V	I	AE13
AE10	I	1.8 V	CSI2	CSI2_RXN1	X1-A106	X1-B106	CSI3_RXN1	CSI3	1.8 V	I	AE14
-	P			DGND	X1-A107	X1-B107	DGND			P	-
AF10	I	1.8 V	CSI2	CSI2_RXP0	X1-A108	X1-B108	CSI3_RXP0	CSI3	1.8 V	I	AF12
AF9	I	1.8 V	CSI2	CSI2_RXN0	X1-A109	X1-B109	CSI3_RXN0	CSI3	1.8 V	I	AF13
-	P			DGND	X1-A110	X1-B110	DGND			P	-

Table 12: Pinout X2

CPU Ball	IO	Level	Group	Signal	Pin	Pin	Signal	Group	Level	IO	CPU Ball
-	P			DGND	X2-A1	X2-B1	DGND			P	-
-	P	5.0 V	Power	V_5V_IN	X2-A2	X2-B2	V_5V_IN	Power	5.0 V	P	-
-	P	5.0 V	Power	V_5V_IN	X2-A3	X2-B3	V_5V_IN	Power	5.0 V	P	-
-	P	5.0 V	Power	V_5V_IN	X2-A4	X2-B4	V_5V_IN	Power	5.0 V	P	-
-	P	5.0 V	Power	V_5V_IN	X2-A5	X2-B5	V_5V_IN	Power	5.0 V	P	-
-	P	5.0 V	Power	V_5V_IN	X2-A6	X2-B6	V_5V_IN	Power	5.0 V	P	-
-	P			DGND	X2-A7	X2-B7	DGND			P	-
-	P			DGND	X2-A8	X2-B8	DGND			P	-
-	P			DGND	X2-A9	X2-B9	DGND			P	-
G9	P	1.8 V	Power	V_VPP	X2-A10	X2-B10	V_3V3	Power	3.3 V	O	-
-	P			DGND	X2-A11	X2-B11	DGND			P	-
-	P	1.8 V	Power	V_1V8A	X2-A12	X2-B12	V_1V8	Power	1.8 V	O	-
-	P	1.8 V	Power	V_1V8_AUX	X2-A13	X2-B13	V_1V8A_PLL	Power	1.8 V	P	-
-	P			DGND	X2-A14	X2-B14	V_1V1	Power	1.1 V	P	-
-	P	0.85 V	Power	V_0V85	X2-A15	X2-B15	DGND			P	-
-	P	0.75 V / 0.85 V	Power	V_VDD_CORE	X2-A16	X2-B16	VSEL_SD	System	3.3 V	I	-
H19	O	1.8 V / 3.3 V	Power	V_VDDSHV5	X2-A17	X2-B17	V_RTC_IN	Power	2.0 V... 4.2 V	P	-
-	P			DGND	X2-A18	X2-B18	DGND			P	-
-	IO	3.3 V	Secure	SE_ISO7816_IO1	X2-A19	X2-B19	SE_ISO14443_LA	Secure	3.3 V	IO	-
-	IO	3.3 V	Secure	SE_ISO7816_IO2	X2-A20	X2-B20	SE_ISO14443_LB	Secure	3.3 V	IO	-
-	P			DGND	X2-A21	X2-B21	DGND			P	-
-	I	3.3 V	Secure	SE_ISO7816_RST#	X2-A22	X2-B22	SE_ISO7816_CLK	Secure	3.3 V	I	
-	I	3.3 V	Secure	SE_ENA	X2-A23	X2-B23	DGND			P	-
F26	I	1.8 V / 3.3 V	MMC2	MMC2_SDCD	X2-A24	X2-B24	MMC1_SDCD	MMC1	3.3 V	I	B24
-	P			DGND	X2-A25	X2-B25	DGND			P	-
AA20	IO	1.8 V	OLDI0	OLDI0_A7P	X2-A26	X2-B26	OLDI0_A3P	OLDI0	1.8 V	IO	AG21
AB19	IO	1.8 V	OLDI0	OLDI0_A7N	X2-A27	X2-B27	OLDI0_A3N	OLDI0	1.8 V	IO	AG20
-	P			DGND	X2-A28	X2-B28	DGND			P	-
AE19	IO	1.8 V	OLDI0	OLDI0_CLK1P	X2-A29	X2-B29	OLDI0_CLK0P	OLDI0	1.8 V	IO	AE20
AD20	IO	1.8 V	OLDI0	OLDI0_CLK1N	X2-A30	X2-B30	OLDI0_CLK0N	OLDI0	1.8 V	IO	AF21
-	P			DGND	X2-A31	X2-B31	DGND			P	-
-	P			DGND	X2-A32	X2-B32	DGND			P	-
AG18	IO	1.8 V	OLDI0	OLDI0_A6P	X2-A33	X2-B33	OLDI0_A2P	OLDI0	1.8 V	IO	AB21
AG17	IO	1.8 V	OLDI0	OLDI0_A6N	X2-A34	X2-B34	OLDI0_A2N	OLDI0	1.8 V	IO	AB20
-	P			DGND	X2-A35	X2-B35	DGND			P	-
AF18	IO	1.8 V	OLDI0	OLDI0_A5P	X2-A36	X2-B36	OLDI0_A1P	OLDI0	1.8 V	IO	AG23
AF19	IO	1.8 V	OLDI0	OLDI0_A5N	X2-A37	X2-B37	OLDI0_A1N	OLDI0	1.8 V	IO	AG22
-	P			DGND	X2-A38	X2-B38	DGND			P	-
AC21	IO	1.8 V	OLDI0	OLDI0_A4P	X2-A39	X2-B39	OLDI0_A0P	OLDI0	1.8 V	IO	AG24
AD21	IO	1.8 V	OLDI0	OLDI0_A4N	X2-A40	X2-B40	OLDI0_A0N	OLDI0	1.8 V	IO	AF23
-	P			DGND	X2-A41	X2-B41	DGND			P	-
H26	IO	1.8 V / 3.3 V	MMC2	MMC2_CLK	X2-A42	X2-B42	MMC1_CLK	MMC1	1.8 V / 3.3 V	IO	H24
-	P			DGND	X2-A43	X2-B43	DGND			P	-
G26	IO	1.8 V / 3.3 V	MMC2	MMC2_DAT0	X2-A44	X2-B44	MMC1_DAT0	MMC1	1.8 V / 3.3 V	IO	H23

3.3.2 Pinout TQMa67xx (Table continued)

CPU Ball	IO	Level	Group	Signal	Pin	Pin	Signal	Group	Level	IO	CPU Ball
G27	IO	1.8 V / 3.3 V	MMC2	MMC2_DAT1	X2-A45	X2-B45	MMC1_DAT1	MMC1	1.8 V / 3.3 V	IO	H20
-	P			DGND	X2-A46	X2-B46	DGND			P	-
H27	IO	1.8 V / 3.3 V	MMC2	MMC2_DAT2	X2-A47	X2-B47	MMC1_DAT2	MMC1	1.8 V / 3.3 V	IO	J23
J27	IO	1.8 V / 3.3 V	MMC2	MMC2_DAT3	X2-A48	X2-B48	MMC1_DAT3	MMC1	1.8 V / 3.3 V	IO	H25
H21	I	1.8 V / 3.3 V	MMC2	MMC2_SDWP	X2-A49	X2-B49	MMC1_SDWP	MMC1	1.8 V / 3.3 V	I	A24
F27	IO	1.8 V / 3.3 V	MMC2	MMC2_CMD	X2-A50	X2-B50	MMC1_CMD	MMC1	1.8 V / 3.3 V	IO	H22
-	P			DGND	X2-A51	X2-B51	DGND			P	-
Y26	O	3.3 V	VOUT0	VOUT0_DATA6	X2-A52	X2-B52	VOUT0_DATA0	VOUT0	3.3 V	O	W27
Y27	O	3.3 V	VOUT0	VOUT0_DATA7	X2-A53	X2-B53	VOUT0_DATA1	VOUT0	3.3 V	O	W25
-	P			DGND	X2-A54	X2-B54	DGND			P	-
AA24	O	3.3 V	VOUT0	VOUT0_DATA8	X2-A55	X2-B55	VOUT0_DATA2	VOUT0	3.3 V	O	W24
AA27	O	3.3 V	VOUT0	VOUT0_DATA9	X2-A56	X2-B56	VOUT0_DATA3	VOUT0	3.3 V	O	W23
-	P			DGND	X2-A57	X2-B57	DGND			P	-
AA25	O	3.3 V	VOUT0	VOUT0_DATA10	X2-A58	X2-B58	VOUT0_DATA4	VOUT0	3.3 V	O	W22
AB25	O	3.3 V	VOUT0	VOUT0_DATA11	X2-A59	X2-B59	VOUT0_DATA5	VOUT0	3.3 V	O	W21
-	P			DGND	X2-A60	X2-B60	DGND			P	-
AC26	O	3.3 V	VOUT0	VOUT0_PCLK	X2-A61	X2-B61	VOUT0_DATA12	VOUT0	3.3 V	O	AA23
-	P			DGND	X2-A62	X2-B62	VOUT0_DATA13	VOUT0	3.3 V	O	AA22
AC27	O	3.3 V	VOUT0	VOUT0_DE	X2-A63	X2-B63	DGND			P	-
AB24	O	3.3 V	VOUT0	VOUT0_HSYNC	X2-A64	X2-B64	VOUT0_DATA14	VOUT0	3.3 V	O	AB26
AB23	O	3.3 V	VOUT0	VOUT0_VSYNC	X2-A65	X2-B65	VOUT0_DATA15	VOUT0	3.3 V	O	AB27
-	P			DGND	X2-A66	X2-B66	DGND			P	-
AE27	I	1.8 V / 3.3 V	RGMII1	RGMII1_RXC	X2-A67	X2-B67	RGMII1_RD0	RGMII1	1.8 V / 3.3 V	I	AC25
-	P			DGND	X2-A68	X2-B68	RGMII1_RD1	RGMII1	1.8 V / 3.3 V	I	AD27
AE26	I	1.8 V / 3.3 V	RGMII1	RGMII1_RD3	X2-A69	X2-B69	RGMII1_RD2	RGMII1	1.8 V / 3.3 V	I	AE24
-	P			DGND	X2-A70	X2-B70	DGND			P	-
AG26	O	1.8 V / 3.3 V	RGMII1	RGMII1_TXC	X2-A71	X2-B71	RGMII1_TD0	RGMII1	1.8 V / 3.3 V	O	AF27
-	P			DGND	X2-A72	X2-B72	RGMII1_TD1	RGMII1	1.8 V / 3.3 V	O	AE23
AF24	O	1.8 V / 3.3 V	RGMII1	RGMII1_TD3	X2-A73	X2-B73	RGMII1_TD2	RGMII1	1.8 V / 3.3 V	O	AG25
-	P			DGND	X2-A74	X2-B74	DGND			P	-
AF25	O	1.8 V / 3.3 V	RGMII1	RGMII1_TX_CTL	X2-A75	X2-B75	DSI0_TXN0	DSI0	1.8 V	IO	AD17
AD23	I	1.8 V / 3.3 V	RGMII1	RGMII1_RX_CTL	X2-A76	X2-B76	DSI0_TXP0	DSI0	1.8 V	IO	AD18
-	I	3.3 V	EEPROM	CUST_EEPROM_WC#	X2-A77	X2-B77	DGND			P	-
-	I	3.3 V	-	TQ_EEPROM_WC#	X2-A78	X2-B78	DSI0_TXN1	DSI0	1.8 V	IO	AF15
-	O	3.3 V	RTC	RTC_CLKOUT	X2-A79	X2-B79	DSI0_TXP1	DSI0	1.8 V	IO	AF16
-	P			DGND	X2-A80	X2-B80	DGND			P	-
AD25	IO	1.8 V / 3.3 V	MDIO0	MDIO0_MDIO	X2-A81	X2-B81	DSI0_TXCLKN	DSI0	1.8 V	IO	AE16
AC24	O	1.8 V / 3.3 V	MDIO0	MDIO0_MDC	X2-A82	X2-B82	DSI0_TXCLKP	DSI0	1.8 V	IO	AE17

3.3.2 Pinout TQMa67xx (Table continued)

CPU Ball	IO	Level	Group	Signal	Pin	Pin	Signal	Group	Level	IO	CPU Ball
-	P			DGND	X2-A83	X2-B83	DGND			P	-
AE1	IO	1.8 V	MMC0	MMC0_CLK_CON	X2-A84	X2-B84	DSI0_TXN2	DSI0	1.8 V	IO	AG14
-	P			DGND	X2-A85	X2-B85	DSI0_TXP2	DSI0	1.8 V	IO	AG15
AD1	IO	1.8 V	MMC0	MMC0_DS_CON	X2-A86	X2-B86	DGND			P	-
AE2	IO	1.8 V	MMC0	MMC0_CMD_CON	X2-A87	X2-B87	DSI0_TXN3	DSI0	1.8 V	IO	AC18
AD3	IO	1.8 V	MMC0	MMC0_DAT0_CON	X2-A88	X2-B88	DSI0_TXP3	DSI0	1.8 V	IO	AC19
AD2	IO	1.8 V	MMC0	MMC0_DAT1_CON	X2-A89	X2-B89	DGND			P	-
-	P			DGND	X2-A90	X2-B90	DGND			P	-
AB4	IO	1.8 V	MMC0	MMC0_DAT2_CON	X2-A91	X2-B91	MMC0_DAT5_CON	MMC0	1.8 V	IO	AB3
AC2	IO	1.8 V	MMC0	MMC0_DAT3_CON	X2-A92	X2-B92	MMC0_DAT6_CON	MMC0	1.8 V	IO	AF1
AC3	IO	1.8 V	MMC0	MMC0_DAT4_CON	X2-A93	X2-B93	MMC0_DAT7_CON	MMC0	1.8 V	IO	AB2
-	P			DGND	X2-A94	X2-B94	DGND			P	-
AF7	I	1.8 V	CSI1	CSI1_RXN0	X2-A95	X2-B95	CSI0_RXN0	CSI0	1.8 V	I	AD6
AF6	I	1.8 V	CSI1	CSI1_RXP0	X2-A96	X2-B96	CSI0_RXP0	CSI0	1.8 V	I	AD5
-	P			DGND	X2-A97	X2-B97	DGND			P	-
AE8	I	1.8 V	CSI1	CSI1_RXN1	X2-A98	X2-B98	CSI0_RXN1	CSI0	1.8 V	I	AE5
AE7	I	1.8 V	CSI1	CSI1_RXP1	X2-A99	X2-B99	CSI0_RXP1	CSI0	1.8 V	I	AE4
-	P			DGND	X2-A100	X2-B100	DGND			P	-
-	P			DGND	X2-A101	X2-B101	DGND			P	-
AG6	I	1.8 V	CSI1	CSI1_RXCLKN	X2-A102	X2-B102	CSI0_RXCLKN	CSI0	1.8 V	I	AC7
AG5	I	1.8 V	CSI1	CSI1_RXCLKP	X2-A103	X2-B103	CSI0_RXCLKP	CSI0	1.8 V	I	AC6
-	P			DGND	X2-A104	X2-B104	DGND			P	-
AD9	I	1.8 V	CSI1	CSI1_RXN2	X2-A105	X2-B105	CSI0_RXN2	CSI0	1.8 V	I	AF4
AD8	I	1.8 V	CSI1	CSI1_RXP2	X2-A106	X2-B106	CSI0_RXP2	CSI0	1.8 V	I	AF3
-	P			DGND	X2-A107	X2-B107	DGND			P	-
AC10	I	1.8 V	CSI1	CSI1_RXN3	X2-A108	X2-B108	CSI0_RXN3	CSI0	1.8 V	I	AG3
AC9	I	1.8 V	CSI1	CSI1_RXP3	X2-A109	X2-B109	CSI0_RXP3	CSI0	1.8 V	I	AG2
-	P			DGND	X2-A110	X2-B110	DGND			P	-

4. SOFTWARE

The TQMa67xx is shipped with a specially adapted bootloader, which is configured for use on an MBa67xx.
This bootloader contains module specific as well as board specific adjustments like e.g.

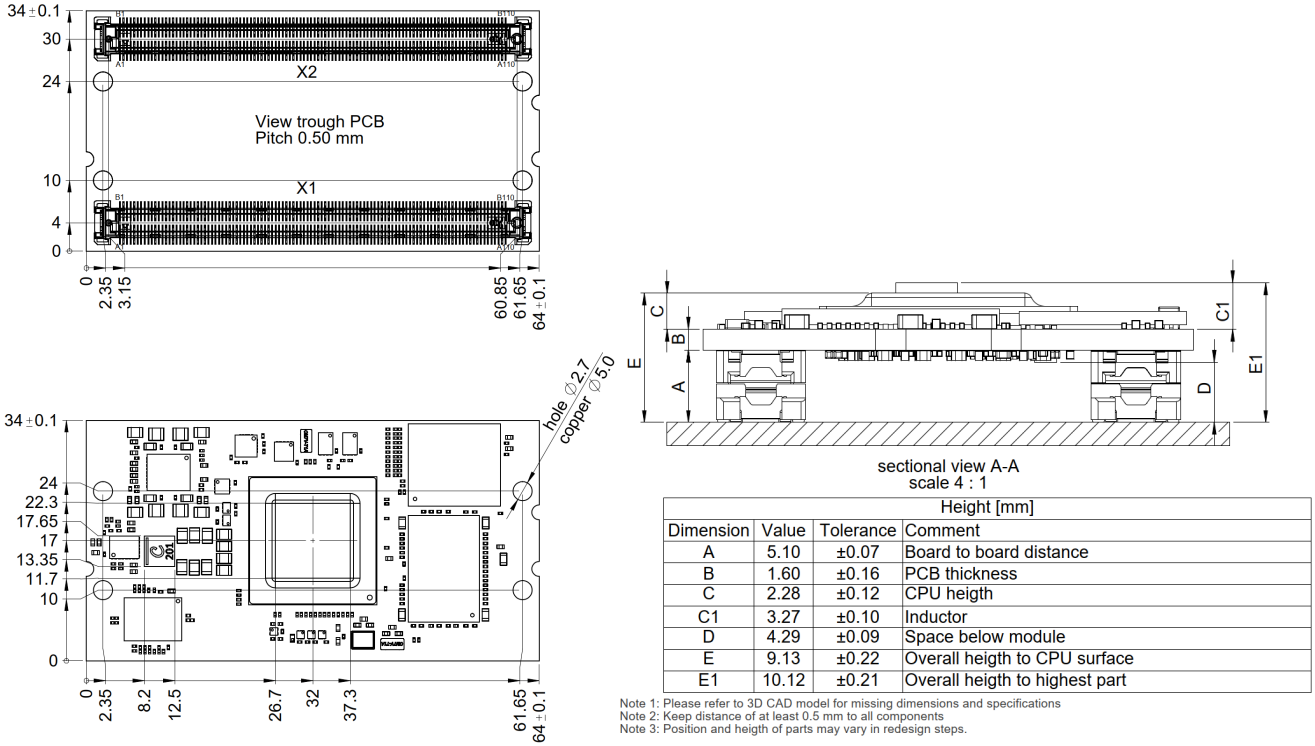
- AM67x configuration
- RAM configuration / timing
- Muxing
- Clocks
- Driver strengths

When using a different bootloader this data has to be adapted. Details can be requested from TQ support. More information can be found in the Support Wiki for the TQMa67xx.

5. MECHANICS

5.1 TQMa67xx dimensions and footprint

The overall dimensions (length × width) of the TQMa67xx are 64.0 mm × 34.0 mm (± 0.1 mm).
Mounting hole: 4 x 2.7 mm (diameter).
The mass of TQMa67xx94 is 17 g (± 2 g).



Height [mm]			
Dimension	Value	Tolerance	Comment
A	5.10	±0.07	Board to board distance
B	1.60	±0.16	PCB thickness
C	2.28	±0.12	CPU heigth
C1	3.27	±0.10	Inductor
D	4.29	±0.09	Space below module
E	9.13	±0.22	Overall heigth to CPU surface
E1	10.12	±0.21	Overall heigth to highest part

Note 1: Please refer to 3D CAD model for missing dimensions and specifications
Note 2: Keep distance of at least 0.5 mm to all components
Note 3: Position and heigth of parts may vary in redesign steps.

Figure 15: Dimensions

5.2 TQMa67xx component placement and labeling

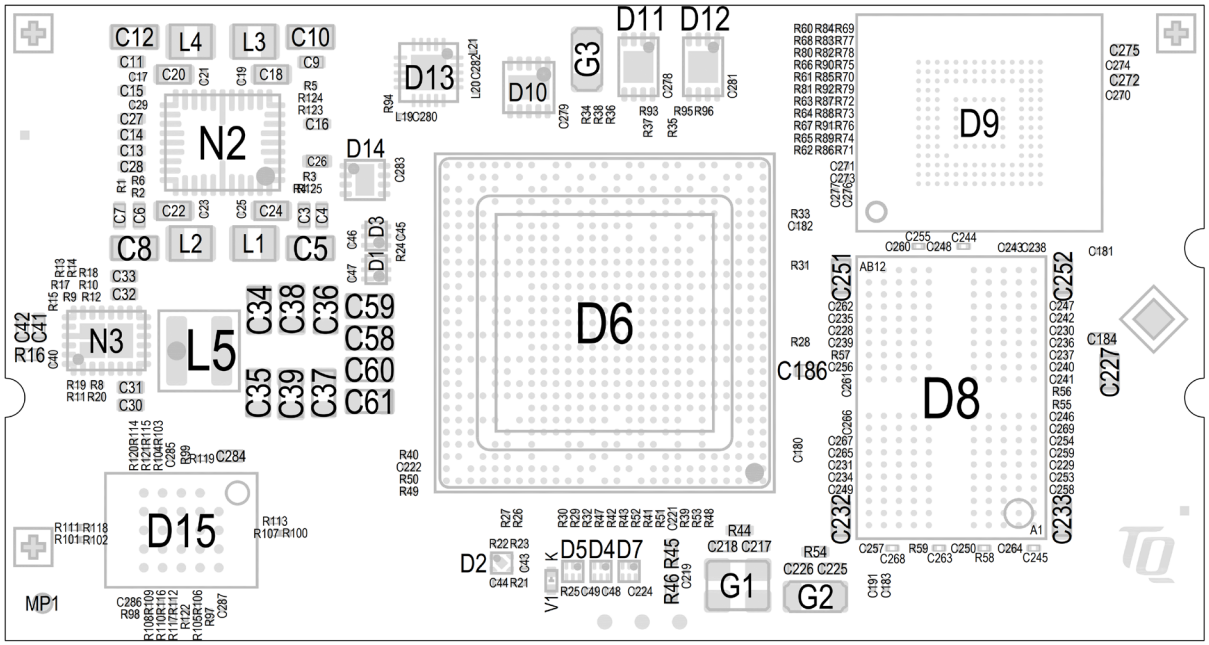


Figure 16: TQMa67xx top view

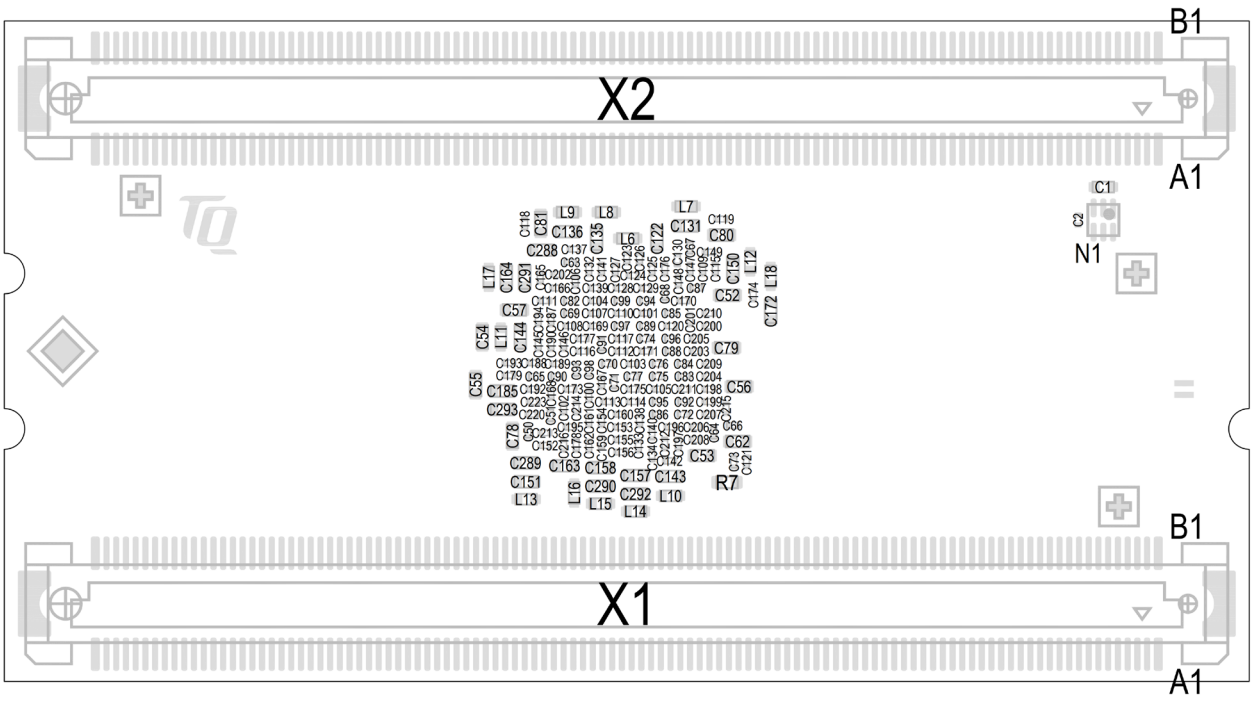


Figure 17: TQMa67xx bottom view

5.3 Protection against external effects

As an embedded module the TQMa67xx is not protected against dust, external impact and contact (IP00).

Adequate protection has to be guaranteed by the surrounding system.

5.4 Thermal management

The power dissipation mainly depends on the software used and can vary according to the application. The power dissipation mainly arises at the processor, the switching regulators and the LPDDR4 devices. It is the customer's responsibility to define a suitable cooling method for his use case.

Attention: Destruction or malfunction, TQMa67xx cooling	
	The AM67x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM67x must be taken into consideration when connecting the heat sink. The AM67x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa67xx and thus malfunction, deterioration or destruction.

5.5 Structural requirements

The TQMa67xx is held in the connectors with a considerable holding force. It is recommended to use a pulling tool to avoid damaging the connectors of the TQMa67xx as well as those of the base board when removing the TQMa67xx.

If the requirements for vibration and shock resistance are high, a module holder must be provided in the final application to additionally hold the TQMa67xx in position. Since no heavy and large components are used, no further requirements are needed.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa67xx was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding besides, take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.
As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa67xx.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤ 5 V DC), tests with respect to the operational and personal safety haven't been carried out.

6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa67xx is only a sub-component of an overall system.

6.5 Climatic and operational conditions

The temperature range, in which the TQMa67xx works reliably, strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 13: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Environmental temperature	–40 °C to +85 °C	With appropriate cooling
Permitted storage temperature	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

6.6 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the

Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.7 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.8 Reliability and service life

For the TQMa67xx, a constant error rate results in an MTBF of approximately 921,716 hours (TQMa67A94).

Attention must be paid to a construction that is insensitive to vibration and shock.

Service life-limiting components such as electrolytic capacitors were not used.

6.9 Environment protection

6.9.1 RoHS

The TQMa67xx is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

6.9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa67xx was designed to be recyclable and easy to repair.

6.10 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

6.11 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa67xx must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMa67xx enable compliance with EuP requirements for the TQMa67xx.

6.12 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct

human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

6.13 Battery

No batteries are used on the TQMa67xx.

6.14 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa67xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa67xx is delivered in reusable packaging.

6.15 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

7. APPENDIX

7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 14: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AIN	Analog In
ARM®	Advanced RISC Machine
AVS	Adaptive Voltage Scaling
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
DC	Direct Current
DDR3L	Double Data Rate Type three Low voltage
DIN	Deutsche Industrie Norm
DVS	Dynamic Voltage Scaling
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multi-Media Card
EN	Europäische Norm
ESD	Electro-Static Discharge
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input/Output
GPMC	General Purpose Memory Controller
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IP	Ingress Protection
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MCSPI	Multichannel Serial Port Interface
MD	Management Data
MII	Media-Independent Interface
MMC	Multi-Media Card
MTBF	Mean operating Time Between Failures

7.1 Acronyms and definitions (continued)

Table 14: Acronyms (continued)

Acronym	Meaning
n.a.	Not Available
NC	Not Connected
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRCM	Power and Clock Management
PU	Pull-Up
PWM	Pulse-Width Modulation
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection
WXGA	Wide Extended Graphics Array

7.2 References

Table 15: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	AM67x Processors Datasheet	A / Sep. 2024	Texas Instruments
(2)	AM67x Processors Silicon Revision 1.0 Technical Reference Manual	A / Jan. 2025	Texas Instruments
(3)	AM67x Processor Errata	1.0 / Nov. 2023	Texas Instruments
(4)	MBa67xx User's Manual	– current –	TQ-Systems
(5)	Support-Wiki for the TQMa67xx	– current –	TQ-Systems
(6)	Processing instructions for TQMa67xx	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

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