MBa67xx
User's Manual

MBa67xx UM 0100
27.03.2026

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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	27.03.2026	M. Kreuzer		First issue

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa67xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa67xx circuit diagram
- TQMa67xx User's Manual
- AM67 Data Sheets
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqma67xx

2. BRIEF DESCRIPTION

The MBa67xx is designed as a carrier board for the TQMa67xx and TQMa67xxL. The AM67x processor characteristics can be evaluated, and therefore the software development for a TQMa67xx project can be started immediately. This User's Manual specifies the hardware of the MBa67xx mainboard in revision Rev.020x.

The MBa67xx supports all TQMa67xx as well as TQMa67xxL (via adapter TQMa67xxL-ADAP) modules. In the further course of this User's Manual, only the TQMa67xx module is mentioned for the sake of simplicity - however, all statements apply accordingly to the TQMa67xxL module as well.

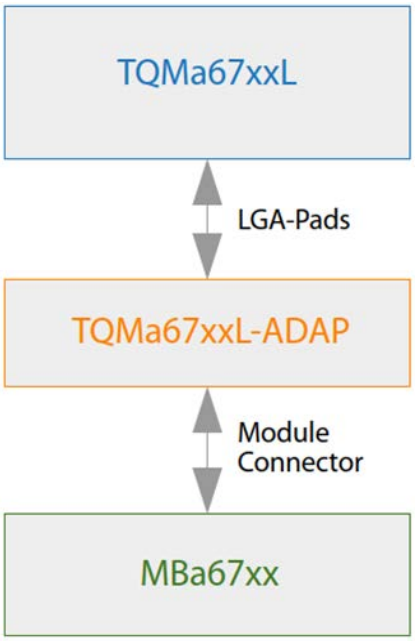

Figure 1: Block diagram TQMa67xx – TQMa67xxL-ADAP – MBa67xx

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 Block diagram

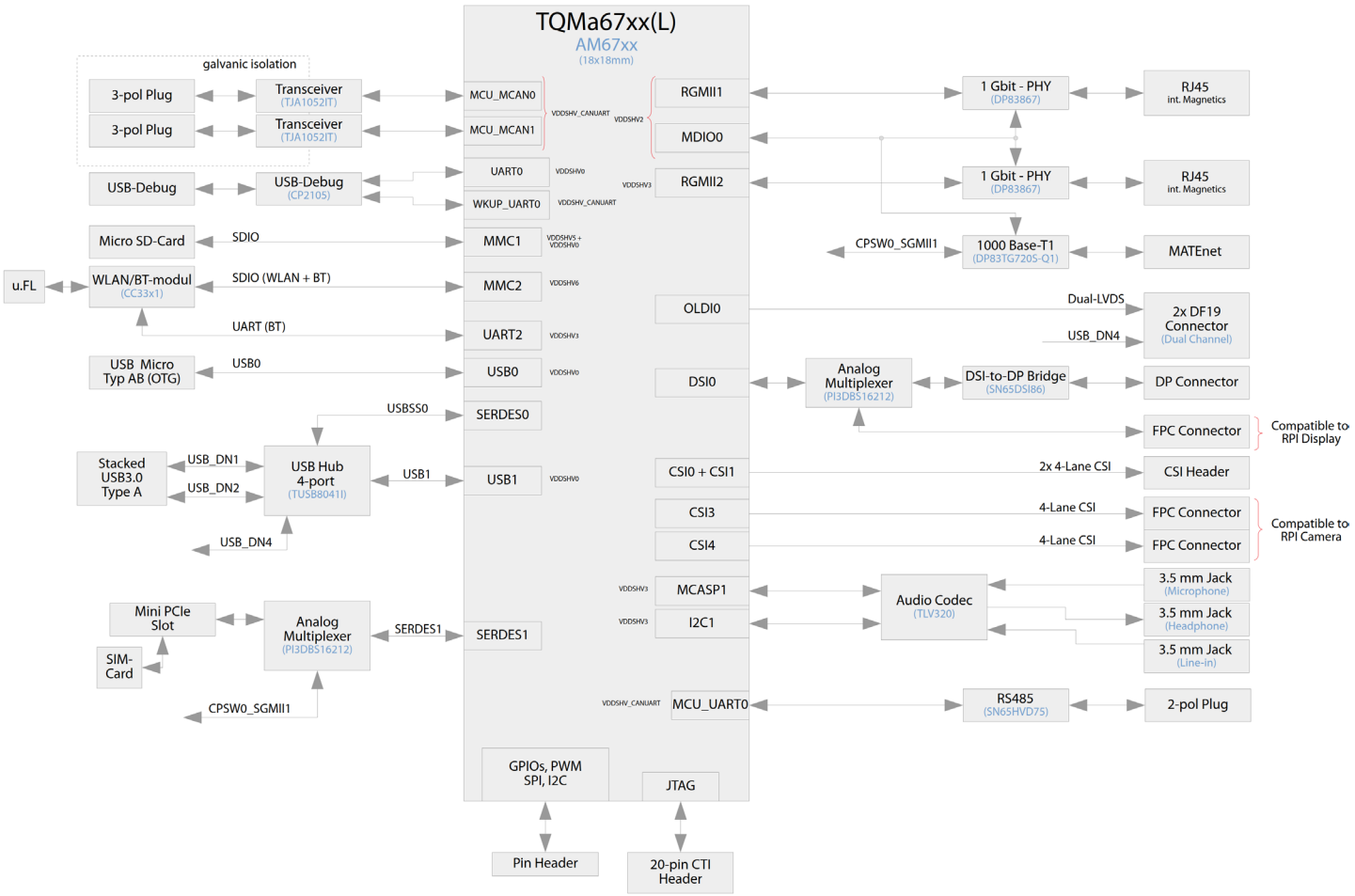

Figure 2: Block diagram MBa67xx

3.1.2 Functionality

The system core is the TQMa67xx processor module with Texas Instruments AM67x processor.

The TQMa67xx connects all peripheral components to each other.

In addition to the standard communication interfaces like USB, Ethernet, RS485 etc. all other available signals of the TQMa67xx are routed to standard headers.

The following interfaces / functions and user's interfaces are provided on the MBa67xx:

Table 2: Overview interfaces

Interface	Qty.	Type of connector	Note
Ethernet 1000BASE-T	2	RJ45 receptacle	Receptacle with integrated magnetics
Ethernet 1000 Base-T1	1	MATEnet	1 Gbit Single Pair Ethernet
CAN	2	Phoenix basic housing	Galv. separated, 3-pole
USB2.0 OTG	1	USB receptacle Type AB (Micro)	USB2.0 OTG
USB 3.0 Host	2	USB receptacle Type A	Stacked, max. 900 mA per port
Debug-USB	1	USB receptacle Type Micro B	2 x COM ports for Debug-UART
Mini PCIe module	1	Mini PCIe socket	Mini PCIe
	1	SIM card holder	SIM card holder
WLAN / WPAN module	1	1 x u.FL	Antenna for WLAN and wireless
RS485	1	Phoenix basic housing	2-pole
SD card	1	Push-Push-Type (Micro)	SDR104 speed-grade (UHS-I)
Audio	3	Jack socket 3.5 mm	1x Line-Out (stereo, green) 1x Line-In (stereo, blue) 1x MIC-In (mono, pink)
LVDS	2	DF19 header	Dual LVDS data (2x 4 lanes), LVDS control signals (USB 2.0, backlight control)
DisplayPort	1	DisplayPort	20-pin DisplayPort
DSI	1	FPC connector	Compatible with RPI display
CSI	1	PCB connector	TQ uniform CSI pinout (2x 4 lanes)
CSI	2	FPC connector	Compatible with RPI camera
Headers	2	Header, 2.54 mm pitch	1 x GPIO signals 1 x Factory tests connector / control signals
Header	1	Header, 1.27 mm pitch	1x SEC (Interface of TQMa67xx) – ISO 14443
Battery holder	1	CR2032 holder	Backup battery RTC of TQMa67xx

Table 3: Overview diagnose and user's interfaces

Interface	Qty.	Component	Note
Status-LEDs	1	LED blue	Power indicator VIN
	1	LED blue	DBG VBUS
	1	LED red / green	PGOOD TQMa67xx
	1	LED red / green	PGOOD MBa67xx
	1	LED yellow	GPIO-LED
	3	LED green / yellow	Ethernet LEDs (activity / speed)
	8	LED green	WWAN WLAN WPAN GPIO-LED VBUS OTG, H1, H2 and H4
Reset buttons	1	Push button	Power-cycle module
User buttons	2	Push button	Processor Reset (cold) GPIO (user button)
Boot Mode configuration	4	DIP switch	4 x Boot mode configuration
CAN termination	2	DIP switch	120 Ohm termination
RS485 termination	1	DIP switch	120 Ohm termination
JTAG	1	20-pole header, 1.27 mm pitch	cTI 20-pin header, Pin 6 is keyed
Fan	1	Header 2.54 mm pitch	4-pole header for PWM control
Power In	1	Jack socket (2.5 mm / 5.5 mm, X5) Screw terminal 2-pole (X6)	16 V to 30 V

4. ELECTRONICS

4.1 System components

4.1.1 TQMa67xx

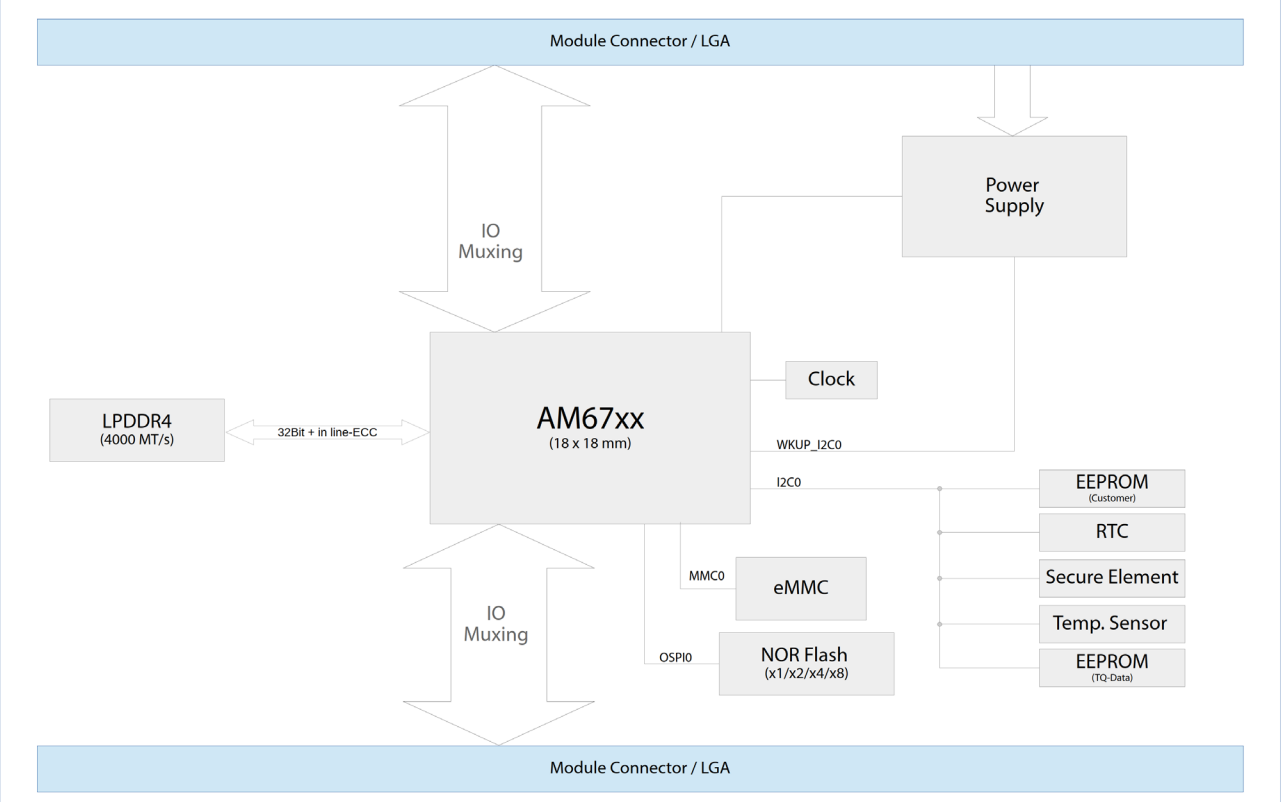

Figure 3: Block diagram TQMa67xx

The TQMa67xx with the AM67x CPU is the central system component. It provides LPDDR4 SDRAM, eMMC, NOR flash and EEPROM memory.

The available signals are routed to module connector pins. When using the processor signals, it is essential to observe the multiple assignment of the pins by different processor-internal function units (multiplexing). More detailed information is to be taken from the accompanying TQMa67xx User's Manual. Connector samples are available from:
https://www.ept.de/index.php?tq-colibri-lp

The TQMa67xx boot behaviour can be customised.

To use the LGA module TQMa67xxL on the MBa67xx an additional adapter board, TQMa67xxL-ADAP, is required. The adapter board serves as an intermediate board that passes the signals from the LGA pads directly to the connectors.

Attention: Destruction or malfunction	
	To avoid damage due to mechanical stresses, the module may only be removed from the mainboard using the MOZIA6UL extraction tool.

4.1.2 I²C address mapping

The accessible I²C buses depend on the pin multiplexing. The I2C0 and WKUP_I2C0 bus is permanently provided for the I²C devices on the TQMa67xx. The following devices are connected on the MBa67xx:

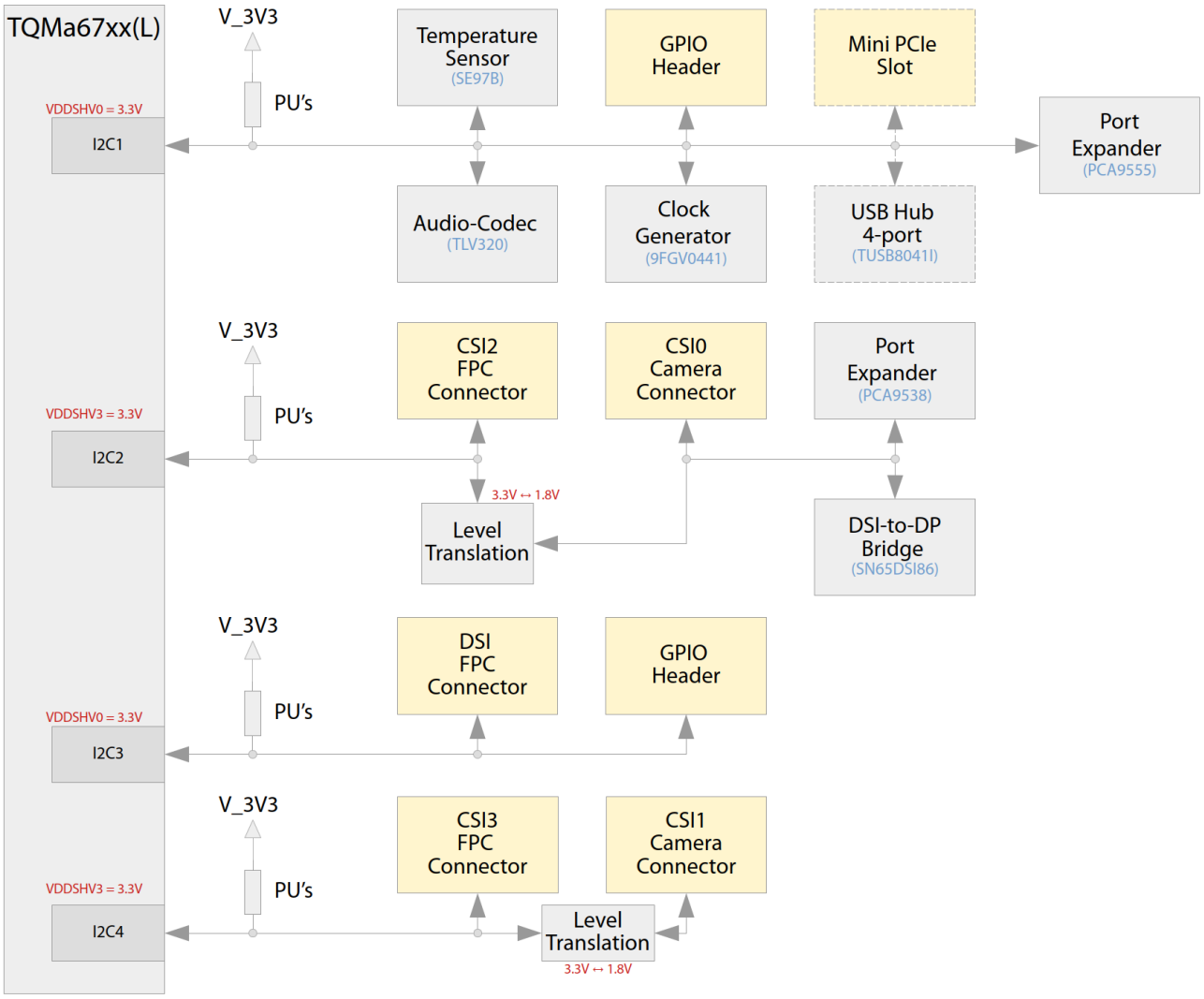

Figure 4: Block diagram I²C bus of the MBa67xx

The following table shows the used addresses of all I²C buses:

Table 4: Address mapping of the TQMa67xx module

Bus	Component	Address	Note
I2C1	Clock generator	0b1101000 / 0x68	D19
	Audio-Codec	0b0011000 / 0x18	N25
	USB hub	0b1000100 / 0x44	D8
	Mini PCIe	depends on usage	X29
	Port expander	0b0100000 / 0x20	D23
	Temp.sensor EEPROM EEPROM protection	0b0011100 / 0x1C 0b1010100 / 0x54 0b0110100 / 0x34	D26
	GPIO header	depends on usage	X30
I2C2	Camera interface	depends on usage	X19
	CSI	depends on usage	X28
	DisplayPort	0b0101100 / 0x2C	N27
	Port-Expander	0b1110000 / 0x70	D22
I2C3	Display interface	depends on usage	X23
	GPIO header	depends on usage	X30
I2C4	Camera interface	depends on usage	X20
	CSI	depends on usage	X18

4.1.3 RTC backup supply

For the backup supply of the RTC on the TQMa67xx a lithium battery (3 V coin cell type CR2032) with very low self-discharge is used on the MBa67xx. The TQMa67xx is supplied via pin V_RTC_IN.

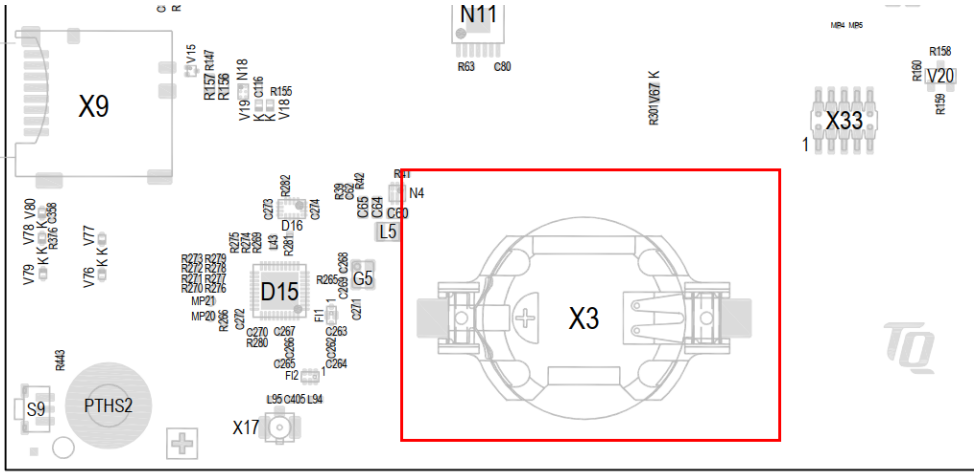

Figure 5: Placement battery holder X3

4.1.4 Reset structure

On the MBa67xx, different possibilities are available for a complete or partial reset (periphery) of the module.
The following signals from the TQMa67xx are used on the MBa67xx:

Table 5: Reset signals

Signal	Type	Level	Description
TQMa67xx_HARD_RST#	I	5.0 V	• Activates power sequencing on module after approx. 200 ms delay (LOW --> HIGH) • Pull-up on module • Connect to GND to activate (e.g. push button)
MCU_PORz	I	3.3 V	• Control of a cold reset • Pull-up on module • Connect to GND to activate (e.g. push button)
MCU_RESETz	I	3.3 V	• Control of a warm reset of the MCU domain • Pull-up on module • Connect to GND to activate (e.g. push button)
RESET_REQz	I	3.3 V	• Control of a warm reset of the main domain • Pull-up on module • Connect to GND to activate (e.g. push button)
TRST#	I	3.3 V	• Connects directly to the TRST# of the module • Pull-down on module
PORz_OUT	O	1.8 V	• Status signal for a cold reset of the main domain • Driver on module
MCU_RESETSTATz	O	3.3 V	• Status signal for a warm reset of the MCU domain • Pull-down on module
RESETSTATz	O	3.3 V	• Status signal for a warm reset of the main domain • Pull-down on module
TQMa67xx_PGOOD	O	3.3 V	• Status signal that is used to indicate the power sequencing on the module
GPIOx	O	3.3 V / 1.8 V	• Activates RESET of various peripherals on the mainboard • Is controlled by software

Attention: Damage	
	The periphery on the base board should never be supplied before the module, otherwise the module may be damaged. This is ensured by the signal PGOOD.

4.1.5 Power supply

The main supply of the MBa67xx is V_24V_VIN via connector X5 (Type: CUI INC PJ-102BH) or X6 (Type: Lumberg KRM02).

On the MBa67xx there is a two part supply:

- 12 V and 5 V supply
  - Permanently activated as soon as the MBa67xx is supplied
  - Module supply / Reset button / LED
- Remaining Power Supply
  - Supply of the periphery
  - Switched by PGOOD
  - Switched off if PGOOD is not present on the module

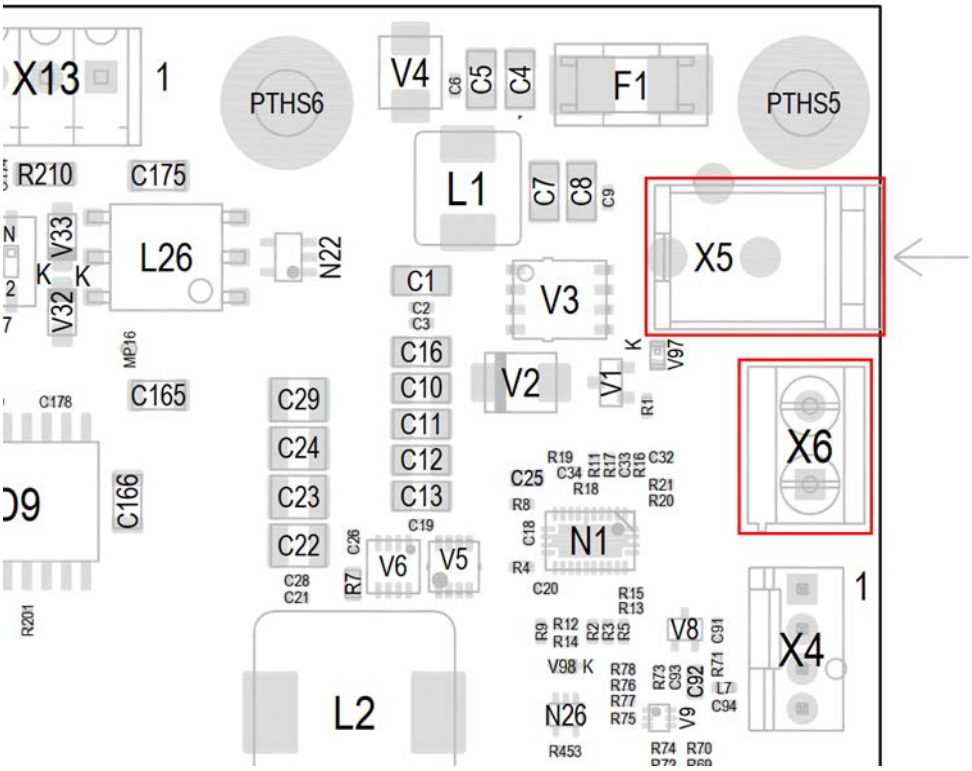

Figure 6: Position X5 and X6

The following figure shows all voltage rails on the mainboard. In order to comply with the required power sequencing, the signal PGOOD is used to control the respective rails.

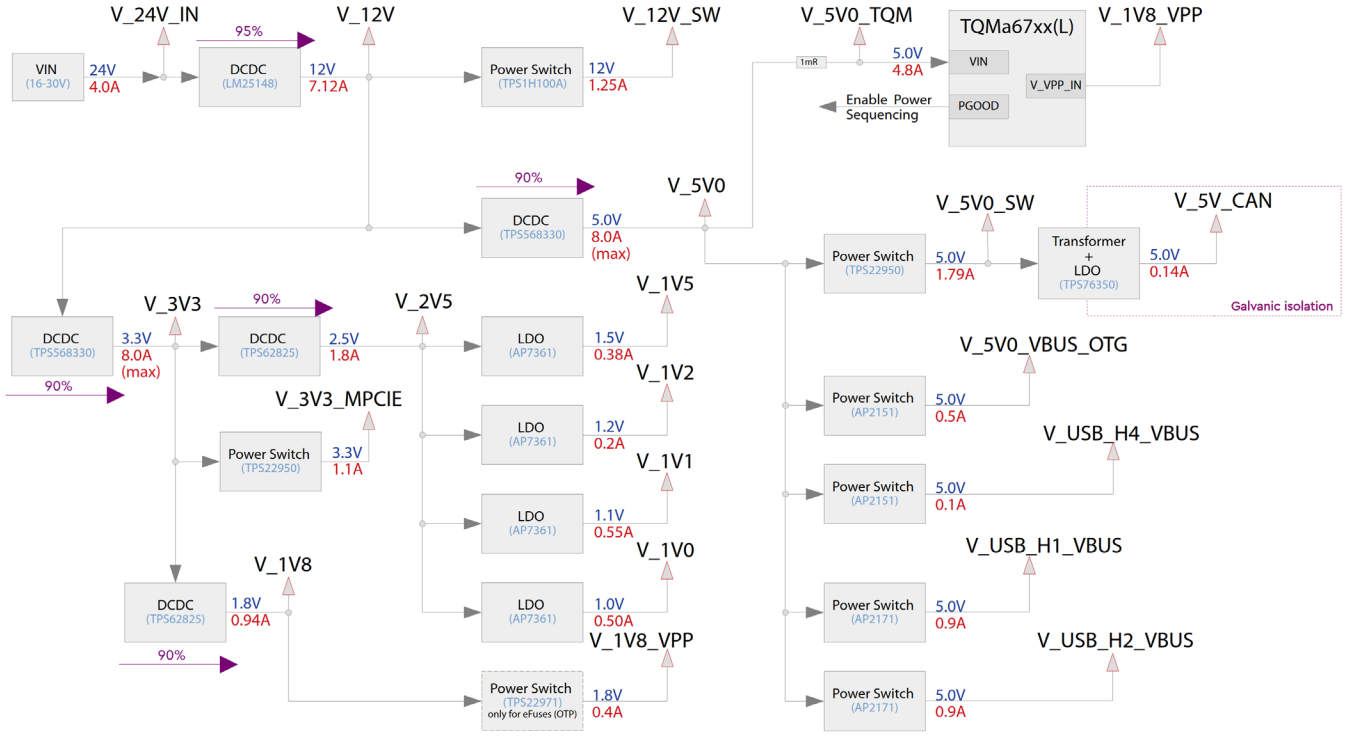

Figure 7: Block diagram power supply chain

The following protective circuits are implemented for the input voltage of the MBa67xx:

- Fuse 5A, slow blow
- Excess voltage protection diode
- PI filter
- Inverse-polarity protection
- Capacitors for voltage smoothing

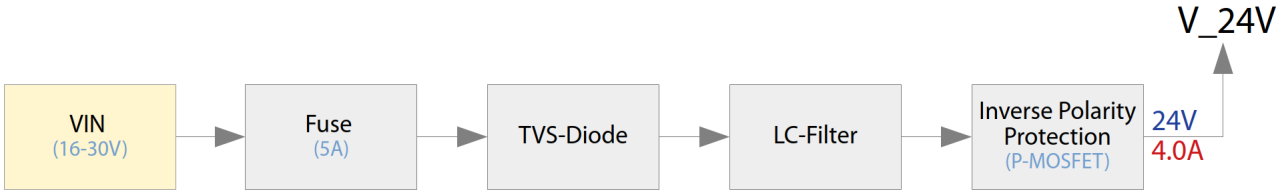

Figure 8: MBa67xx input circuit

The overvoltage limitation is 31.1 V to 34.4 V.

The mainboard MBa67xx, including TQMa67xx, consumes 96 W under full load (all supply voltages are loaded with maximum current, e.g. by connecting external modules to the pin headers). The power supply used must be selected accordingly. In most applications, however, the power consumption will be significantly lower.

Attention: Overload	
	The internal voltages (3.3 V, 1.8 V) provided at the starter kit pin headers are not additionally protected. Technically, an overload of the fuse is therefore possible. The resulting total current consumption of the MBa67xx should be observed.

Table 6: Electrical parameters of the supply voltages

Parameter	Min.	Typ.	Max.	Unit	Note
V_5V0					
Output voltage	4.941	5	5.059	V	
Max. load current			8.0	A	
Current limit		10.0		A	
V_5V0_SW					
Output voltage	4.941	5	5.059	V	
Max. load current			1.79	A	
Current limit		1.96		A	
V_3V3					
Output voltage	3.276	3.3	3.354	V	
Max. load current			5.4	A	
Current limit		9.6		A	
V_3V3_MPCIE					
Output voltage	3.276	3.3	3.354	V	
Max. load current			1.10	A	
Current limit		1.30		A	
V_2V5					
Output voltage	2.484	2.513	2.541	V	
Max. load current			1.8	A	
Current limit		3.9		A	
V_1V8					
Output voltage	1.780	1.8	1.820	V	
Max. load current			0.5	A	
Current limit		3.9		A	
V_1V5					
Output voltage	1.482	1.511	1.541	V	
Max. load current			0.38	A	
Current limit		1.5		A	
V_1V2					
Output voltage	1.180	1.200	1.220	V	
Max. load current			0.2	A	
Current limit		1.5		A	
V_1V1					
Output voltage	1.083	1.100	1.117	V	
Max. load current			0.55	A	
Current limit		1.5		A	
V_1V0					
Output voltage	0.986	1.000	1.014	V	
Max. load current			0.50	A	
Current limit		1.5		A	
V_12V					
Output voltage	11.660	12	12.349	V	
Max. load current			7.12	A	
Current limit		9.5		A	
V_12V_SW					
Output voltage	11.660	12	12.349	V	
Max. load current			1.25	A	
Current limit		1.52		A	
V_5V0_VBUS_OTG / V_USB_H4_VBUS					
Output voltage		5.0		V	
Max. load current			0.5	A	
Current Limit	0.5			A	
V_USB_H1/2_VBUS					
Output voltage		5.0		V	
Max. load current			0.9	A	
Current Limit	1.1			A	
V_1V8_VPP					
Output voltage	1.758	1.8	1.842	V	
Max. load current			0.4	A	
V_5V_CAN					
Output voltage	4.825	5.0	5.175	V	
Max. load current			0.15	A	

The power sequencing of the mainboard MBa67xx is defined as following:

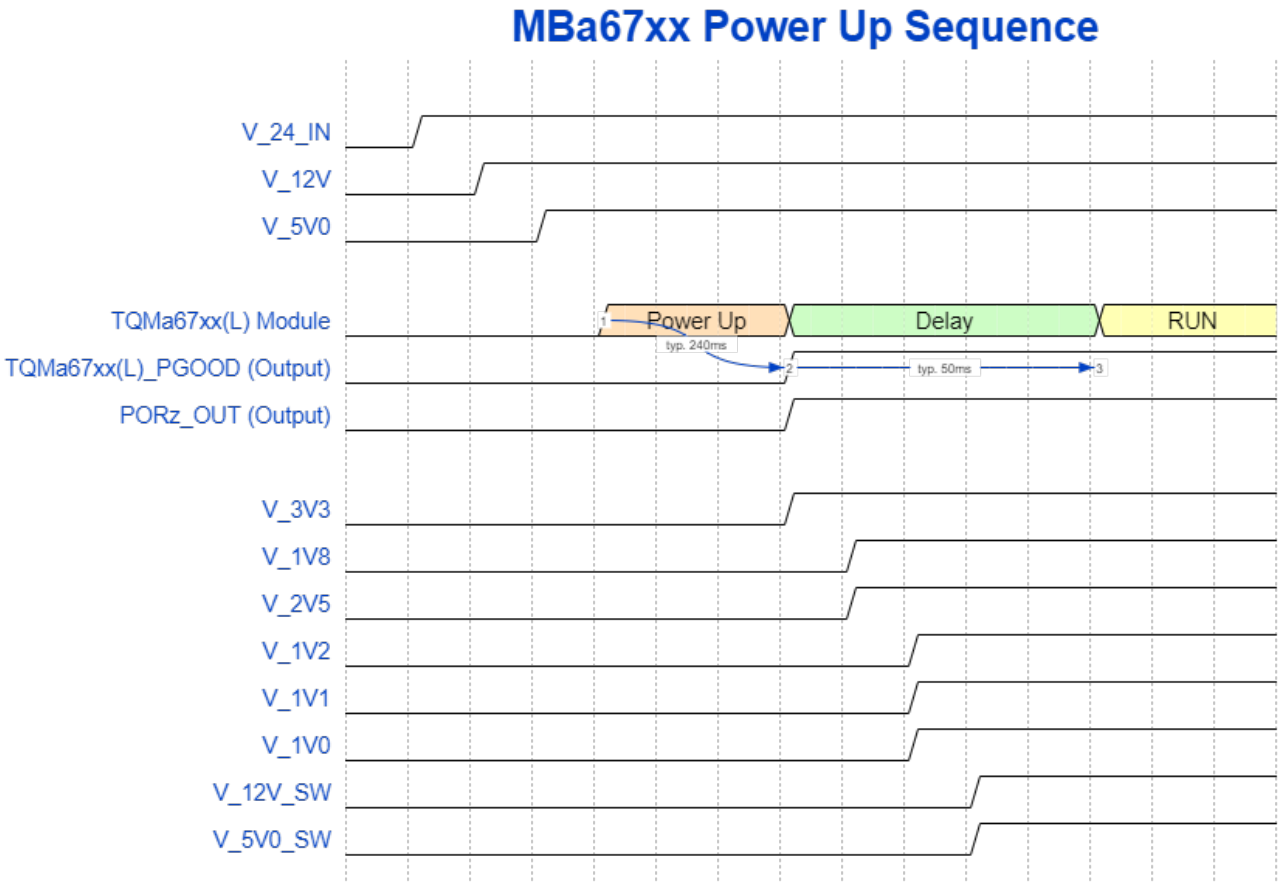

Figure 9: MBa67xx Power up sequenz

- The 5.0 V supply for the TQMa67xx is permanently present when the 12 V supply („always“ ON) is switched on.
- The TQMa67xx executes the power sequencing independently and returns a PGOOD signal for the MBa67xx.
- As soon as the PGOOD signal is present, the MBa67xx performs the power sequencing independently. The used switching regulators / LDOs are controlled by EN and PGOOD signals.
- The time constant between PGOOD and reset of the CPU is approx. 50 ms.

4.2 Communication interfaces

4.2.1 UART- / Debug-interface

To get debug outputs of the CPU, the UART0 and WKUP_UART0 interface of the CPU is used. The used UART of the CPU is connected to a Micro USB connector (X7) via a USB-to-UART bridge.

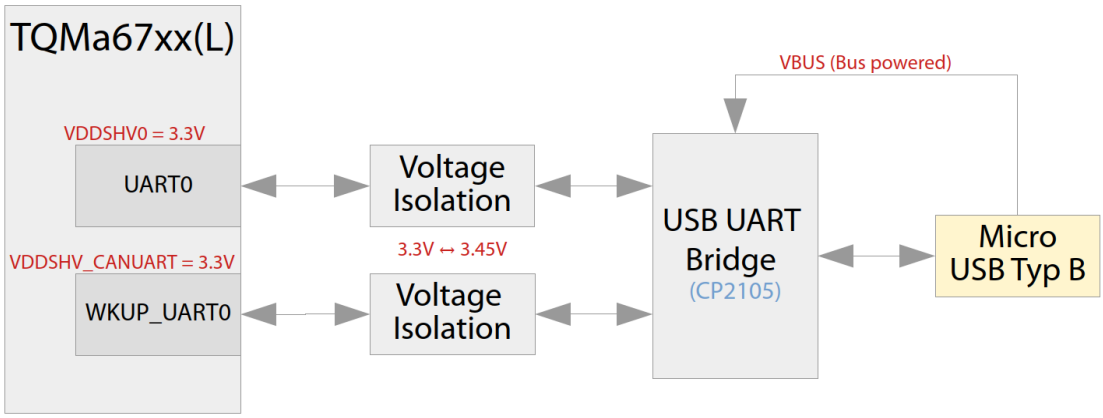

Figure 10: Block diagram UART- / Debug-interface

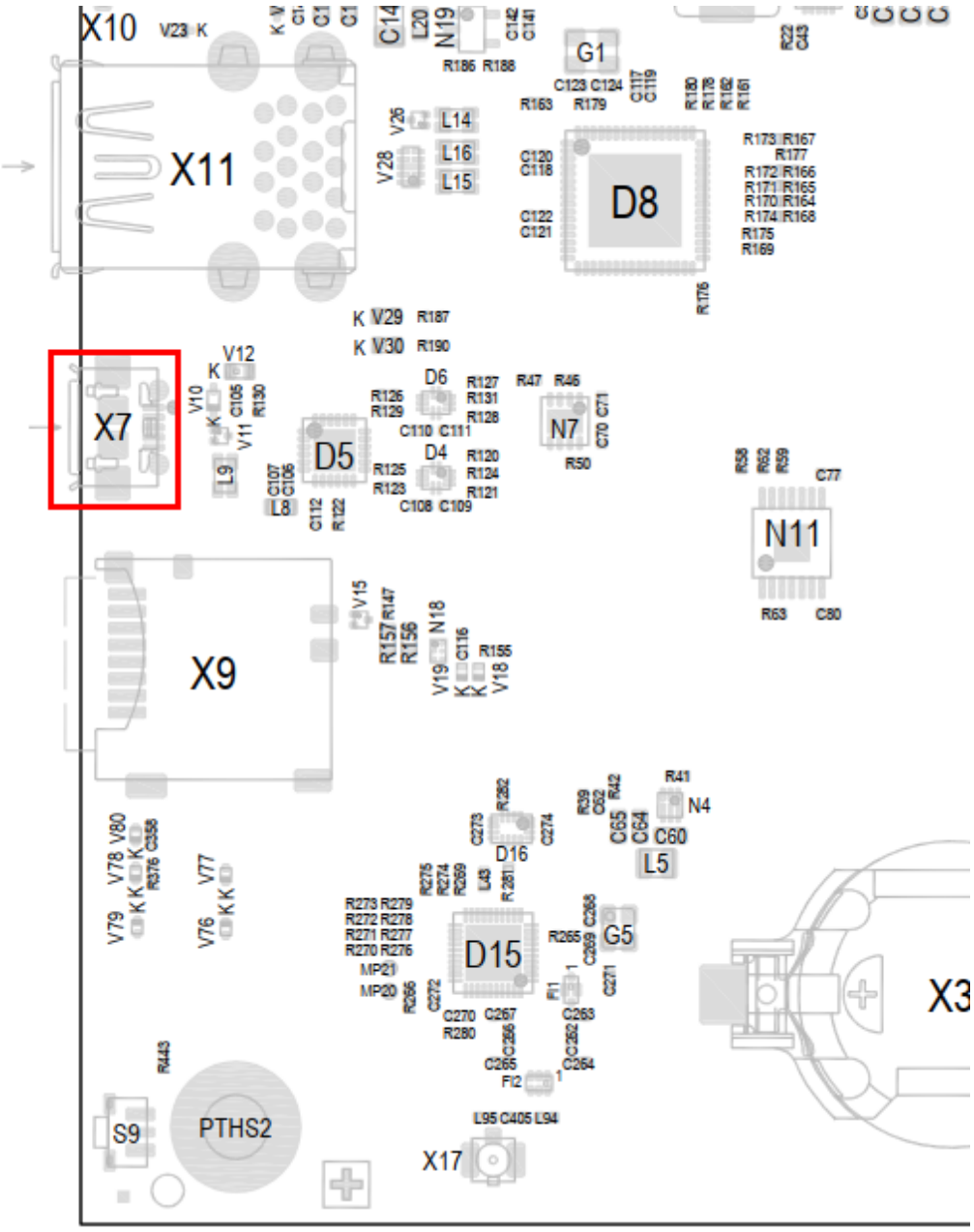

Figure 11: Position X7

4.2.2 USB interface

4.2.2.1 USB OTG

The MBa67xx provides a USB2.0 OTG interface. The USB 2.0 interface also serves as boot source (see also chapter 4.5.4).

- Protection circuit for USB0_VBUS according to Reference Manual (1).
- 5 V power switch depending on the USB ID (GPIO) pin.

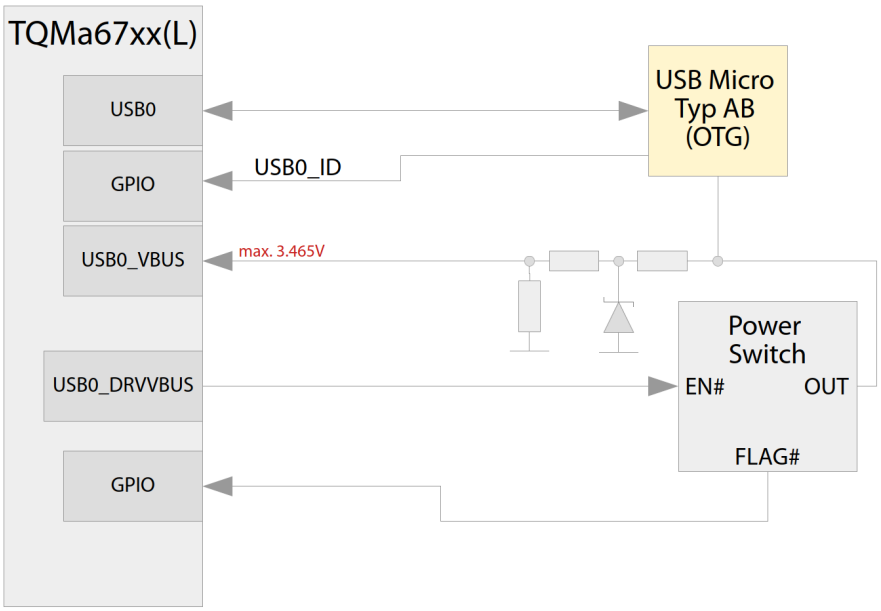

Figure 12: Block diagram USB OTG interface

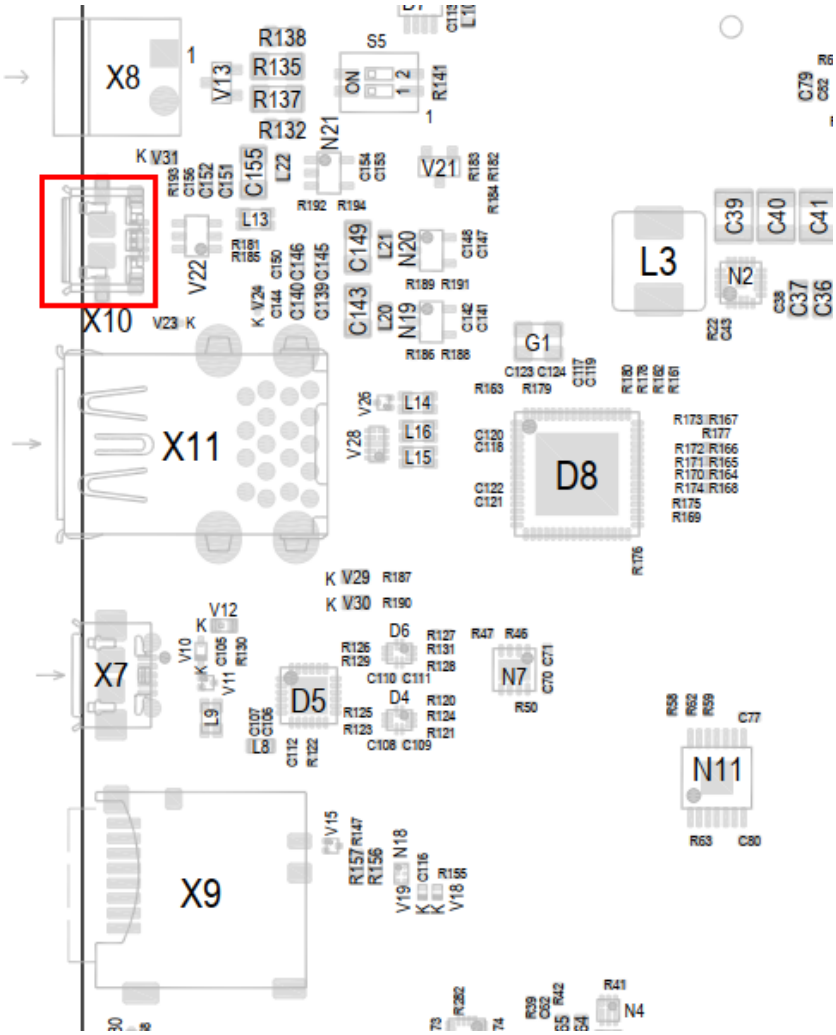

Figure 13: Position of USB interface

4.2.2.2 USB Hub

The MBa67xx also provides a 4-port USB 3.0 hub via USB1 ans SERDES0 of the CPU. This results in a double socket (X11) for the use of USB host (e.g. USB stick) as well as the use of Mini PCIe and the LVDS display.

Protective circuit for USB1_VBUS according to Reference Manual (1).

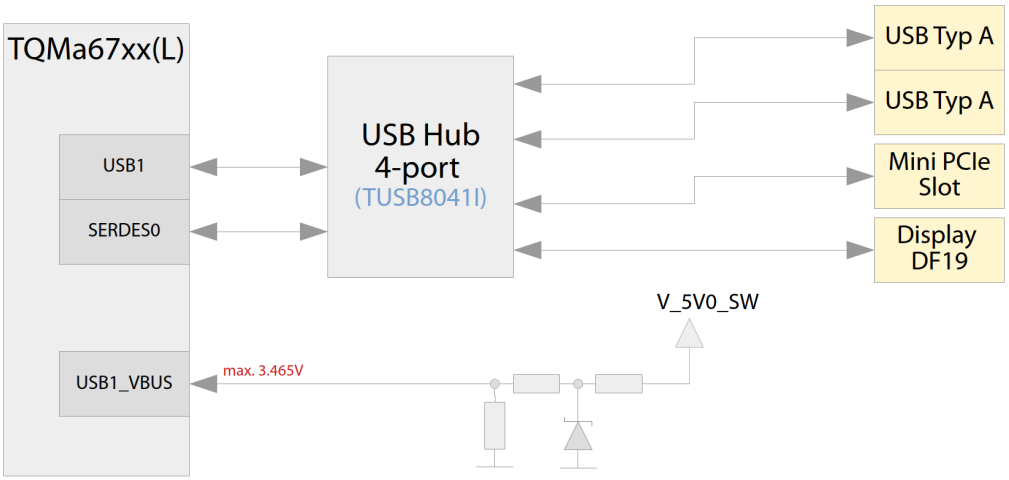

Figure 14: Block Diagram USB hub

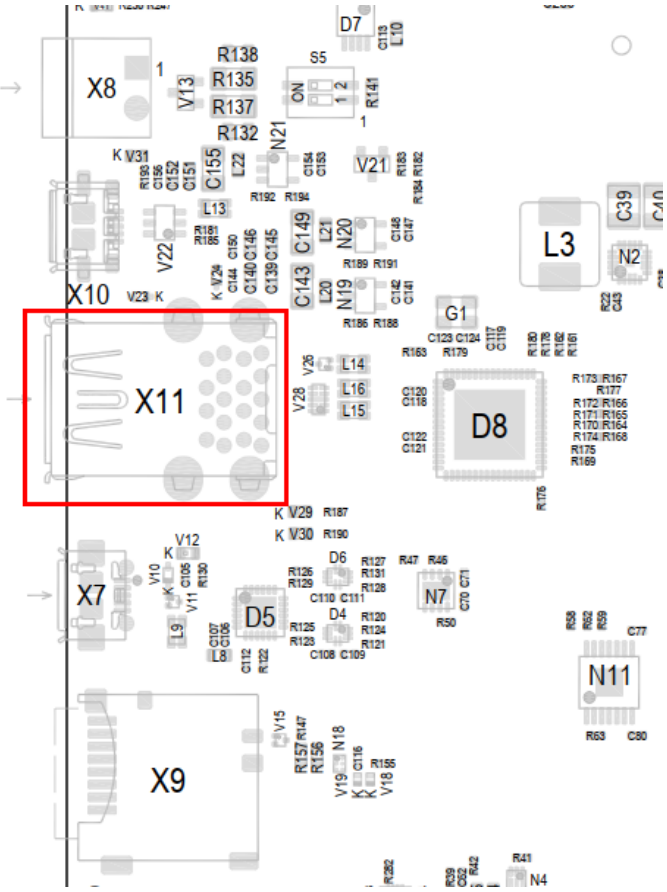

Figure 15: Position USB, X11

4.2.3 Ethernet interface

There are two Gigabit-Ethernet interfaces and one 1000Base-T1 interface on the MBa67xx. Texas Instruments' PHY DP83867ISRZGZ is used for Gigabit-Ethernet and supports IEEE 802.3 10BASE-T, 100BASE-TX and 1000BASE-T. The DP83TG720S PHY from TI is used for 1000Base-T1 (SPE).

The following interfaces are used:

- RGMII at connector X14 or X15
- 1000Base-T1 at connector X16 (TE 2304372-1)

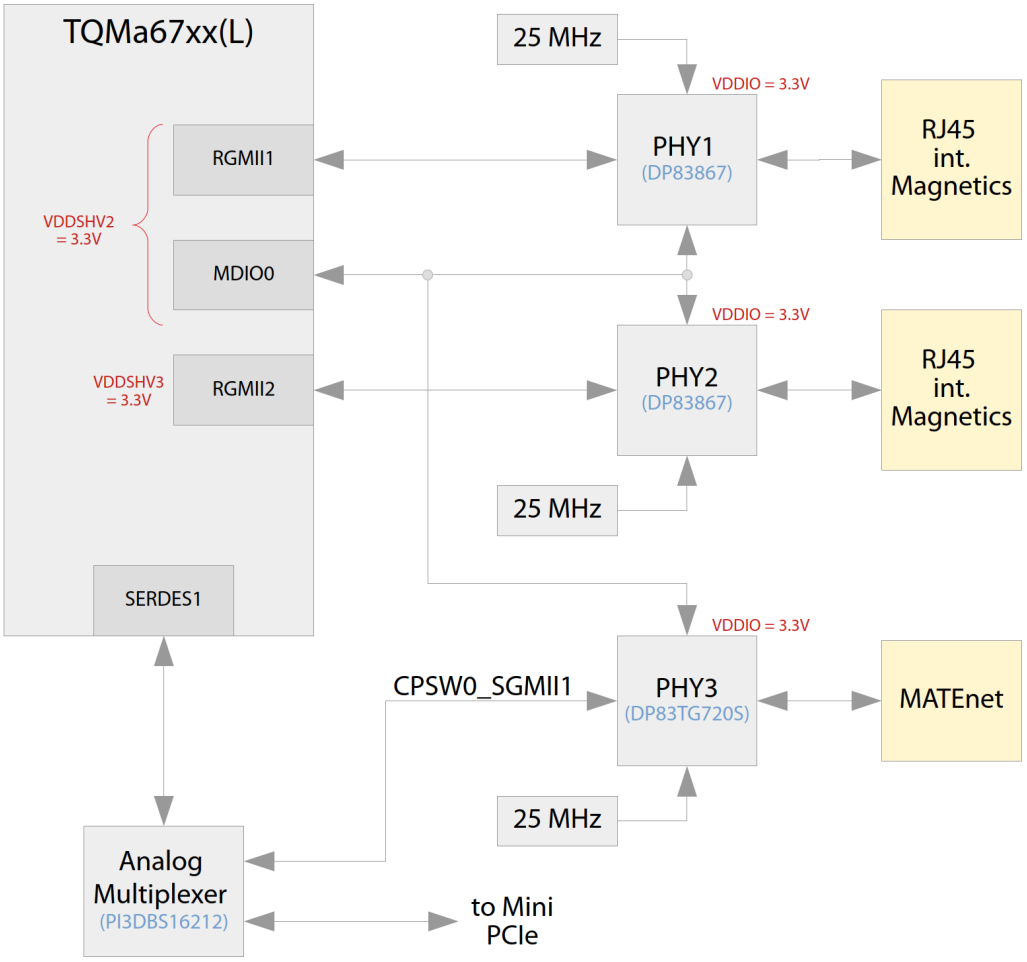

Figure 16: Block diagram Ethernet interface

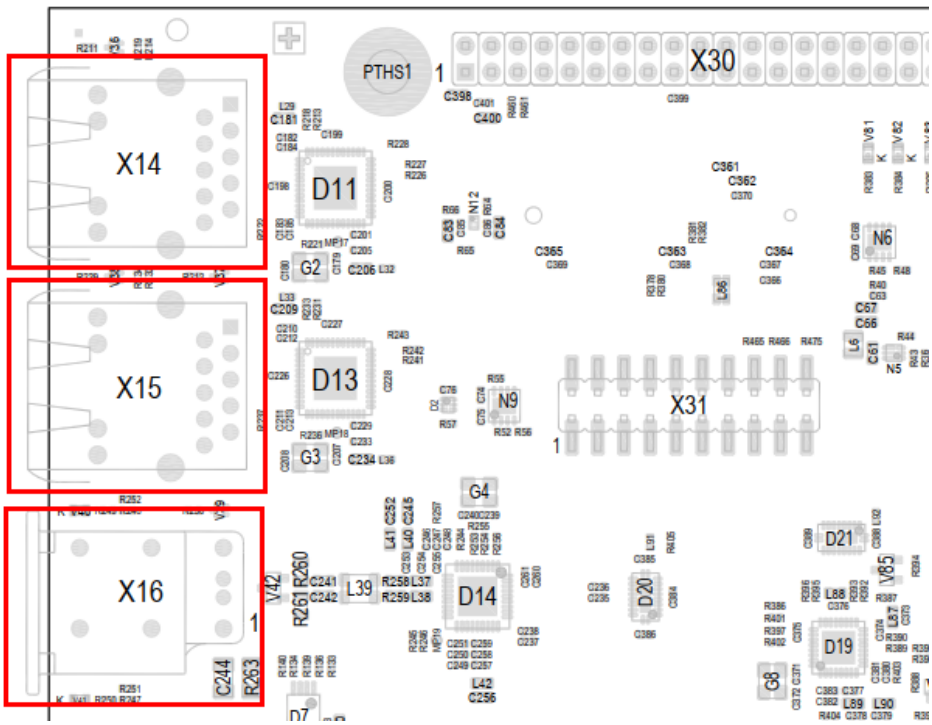

Figure 17: Position of X14, X15 and X16

4.2.4 LVDS

The OLDI interface (OLDI0) of the TQMa67xx is provided with the two single-link Open LVDS Display Interface (4 lanes + 1 clock per channel) on the MBa67xx's X21 and X22 connectors.

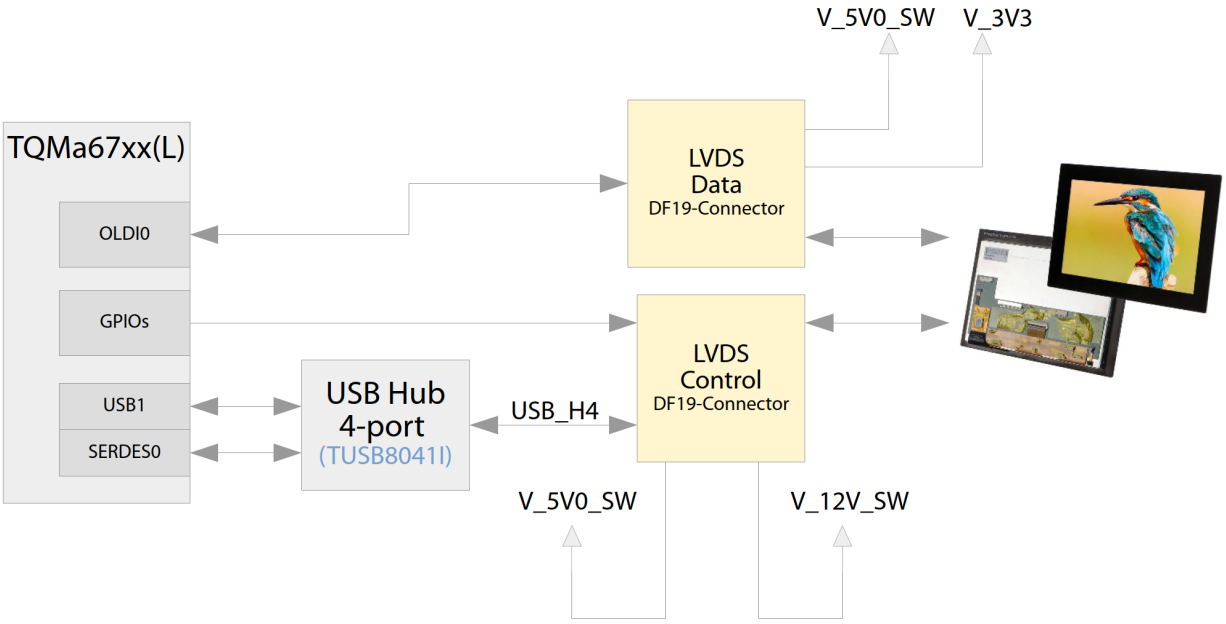

Figure 18: Block diagram LVDS

The selection of the connectors (Type: Hirose DF19G-30P-1H(52) and Hirose DF19G-20P-1H(52)) and the pin assignment correspond to the TQ-specific specifications for the uniform design of the interface, which ensures the connection of dedicated LVDS displays.

Table 7: LVDS pinout X21

Pin	Signal	Type	Level	Note
1	OLDI0_A0N	O	1.8 V	OLDI0-Interface 1 (Lane 0)
2	OLDI0_A0P	O	1.8 V	
3	OLDI0_A1N	O	1.8 V	OLDI0-Interface 1 (Lane 1)
4	OLDI0_A1P	O	1.8 V	
5	OLDI0_A2N	O	1.8 V	OLDI0-Interface 1 (Lane 2)
6	OLDI0_A2P	O	1.8 V	
7	DGND	P	0 V	Ground
8	OLDI0_CLK0N	O	1.8 V	OLDI0-Interface 1 (Clock)
9	OLDI0_CLK0P	O	1.8 V	
10	OLDI0_A3N	O	1.8 V	OLDI0-Interface 1 (Lane 3)
11	OLDI0_A3P	O	1.8 V	
12	OLDI0_A4N	O	1.8 V	OLDI0-Interface 2 (Lane 0)
13	OLDI0_A4P	O	1.8 V	
14	DGND	P	0 V	Ground
15	OLDI0_A5N	O	1.8 V	OLDI0-Interface 2 (Lane 1)
16	OLDI0_A5P	O	1.8 V	
17	DGND	P	0 V	Ground
18	OLDI0_A6N	O	1.8 V	OLDI0-Interface 2 (Lane 2)
19	OLDI0_A6P	O	1.8 V	
20	OLDI0_CLK1N	O	1.8 V	OLDI0-Interface 2 (Clock)
21	OLDI0_CLK1P	O	1.8 V	
22	OLDI0_A7N	O	1.8 V	OLDI0-Interface 2 (Lane 3)
23	OLDI0_A7P	O	1.8 V	
24	DGND	P	0 V	Ground
25	V_5V_LVDS0	P	5 V	5 V supply voltage (filtered from V_5V0_SW)
26	V_5V_LVDS0	P	5 V	
27	V_5V_LVDS0	P	5 V	
28	V_3V3_LVDS0	P	3.3 V	3.3 V supply voltage (filtered from V_3V3)
29	V_3V3_LVDS0	P	3.3 V	
30	V_3V3_LVDS0	P	3.3 V	
M1, M2	DGND	P	0 V	Ground

Table 8: LVDS pinout X22

Pin	Signal	Type	Level	Note
1	V_12V	P	12 V	12 V supply voltage (filtered)
2	V_12V	P	12 V	
3	V_12V	P	12 V	
4	DGND	P	0 V	Ground
5	DGND	P	0 V	
6	DGND	P	0 V	
7	V_5V0	P	5 V	5 V supply voltage
8	V_5V0	P	5 V	
9	DGND	P	0 V	Ground
10	DGND	P	0 V	
11	V_USB_H4_VBUS	P	5 V	VBUS voltage USB Host 4 (filtered)
12	DGND	P	0 V	Ground
13	USB_H4_DN	I/O	3.3 V	Data lines USB Host 4
14	USB_H4_DP	I/O	3.3 V	
15	DGND	P	0 V	Ground
16	LVDS0_RESET#	O	3.3 V	Reset (GPIO0_21), Pulldown on MBa67xx
17	LVDS0_BLT_EN	O	3.3 V	Backlight-Enable (GPIO0_22), Pulldown on MBa67xx
18	LVDS0_PWR_EN	O	3.3 V	Power-Enable (GPIO0_25), Pulldown on MBa67xx
19	LVDS0_PWM	O	3.3 V	PWM for contrast/brightness adjustment (EHRPWM0_A)
20	DGND	P	0 V	Ground
M1, M2	DGND	P	0 V	

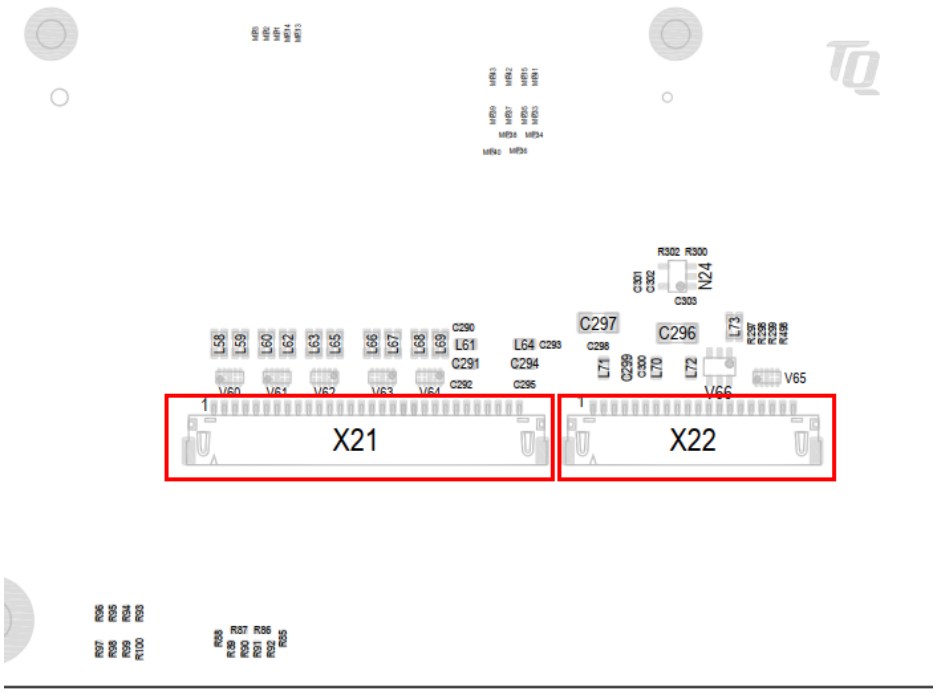

Figure 19: Position X21 and X22

4.2.5 DSI interface

The MBa67xx provides a DSI interface via an analog multiplexer. The signals are available directly at connector X23 and via a display port bridge at connector X24. Connector X23 corresponds to the 22-pin pinout for Raspberry Pi displays; Connector X24 corresponds to a DisplayPort.

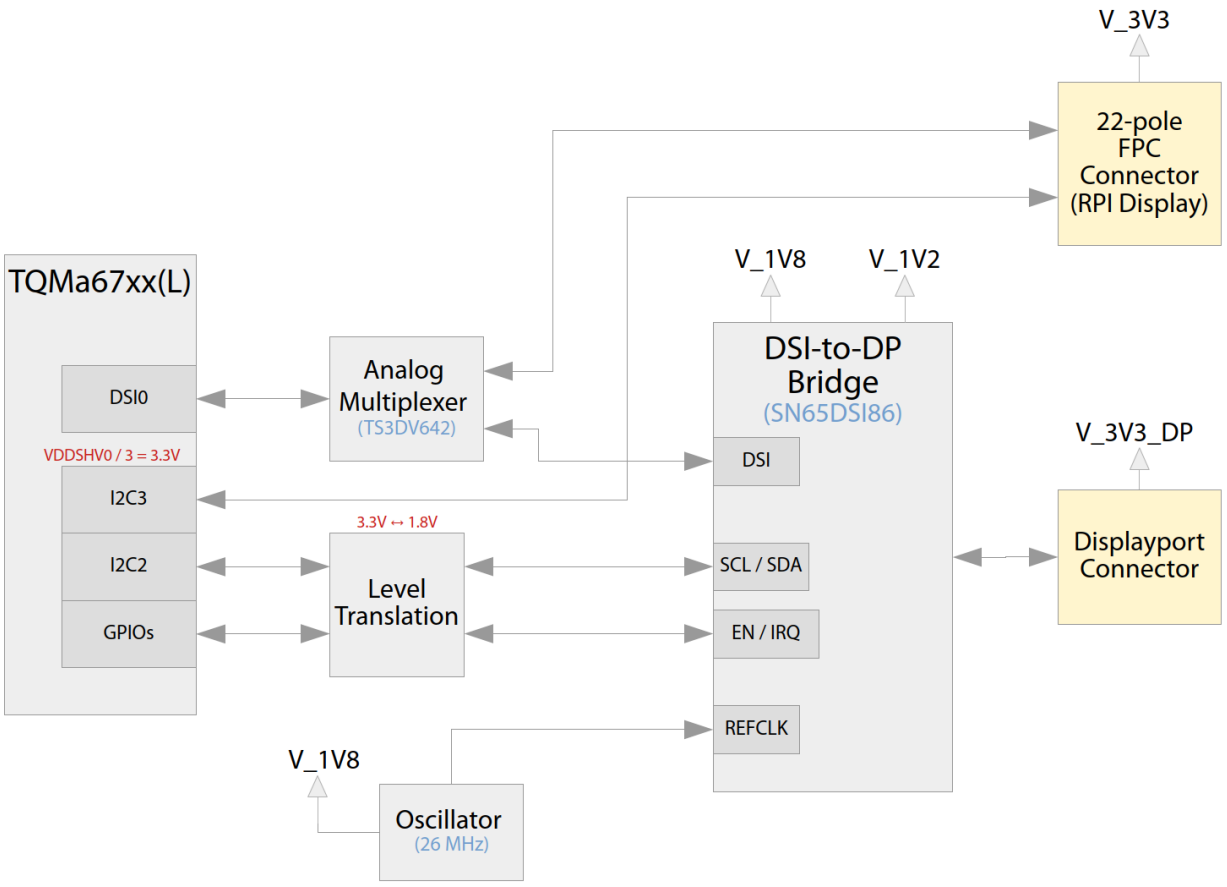

Figure 20: Block diagram MIPI-DSI interface

Table 9: Pinout MIPI-DSI (X23)

Pin	Signal	Type	Level	Note
1	V_3V3	P	3.3 V	Supply max. 1.0 A
2	I2C3_SDA	I/O	3.3 V	Data for I2C configuration interface
3	I2C3_SCL	I/O	3.3 V	Data for I2C configuration interface
4	DGND	P	0 V	Ground
5	NC	-	-	Not connected
6	NC	-	-	Not connected
7	DGND	P	0 V	Ground
8	DSI0_DATA3_P_L	O	1.8 V	DSI interface (Lane 3)
9	DSI0_DATA3_N_L	O	1.8 V	DSI interface (Lane 3)
10	DGND	P	0 V	Ground
11	DSI0_DATA2_P_L	O	1.8 V	DSI interface (Lane 2)
12	DSI0_DATA2_N_L	O	1.8 V	DSI interface (Lane 2)
13	DGND	P	0 V	Ground
14	DSI0_CLK_P_L	O	1.8 V	DSI interface (Clock)
15	DSI0_CLK_N_L	O	1.8 V	DSI interface (Clock)
16	DGND	P	0 V	Ground
17	DSI0_DATA1_P_L	O	1.8 V	DSI interface (Lane 1)
18	DSI0_DATA1_N_L	O	1.8 V	DSI interface (Lane 1)
19	DGND	P	0 V	Ground
20	DSI0_DATA0_P_L	O	1.8 V	DSI interface (Lane 0)
21	DSI0_DATA0_N_L	O	1.8 V	DSI interface (Lane 0)
22	DGND	P	0 V	Ground

Table 10: Pinout DisplayPort (X24)

Pin	Signal	Type	Level	Note
1	DP_ML0+	O	1.8 V	Lane 0
2	DGND	P	0 V	Ground
3	DP_ML0-	O	1.8 V	Lane 0
4	DP_ML1+	O	1.8 V	Lane 1
5	DGND	P	0 V	Ground
6	DP_ML1-	O	1.8 V	Lane 1
7	DP_ML2+	O	1.8 V	Lane 2
8	DGND	P	0 V	Ground
9	DP_ML2-	O	1.8 V	Lane 2
10	DP_ML3+	O	1.8 V	Lane 3
11	DGND	P	0 V	Ground
12	DP_ML3-	O	1.8 V	Lane 3
13	DP_CFG1	I	0 V	Config1 - 1M pulldown to GND
14	DP_CFG2	I	0 V	Config2 - 1M pulldown to GND
15	DP_AUX_CH+	I/O	1.8 V	AUX-Channel
16	DGND	P	0 V	Ground
17	DP_AUX_CH-	I/O	1.8 V	AUX-Channel
18	DP_HPD	I	3.3 V	Hot-Plug detect
19	DGND	P	0 V	Ground
20	V_3V3_DP	P	3.3 V	Supply max. 500 mA

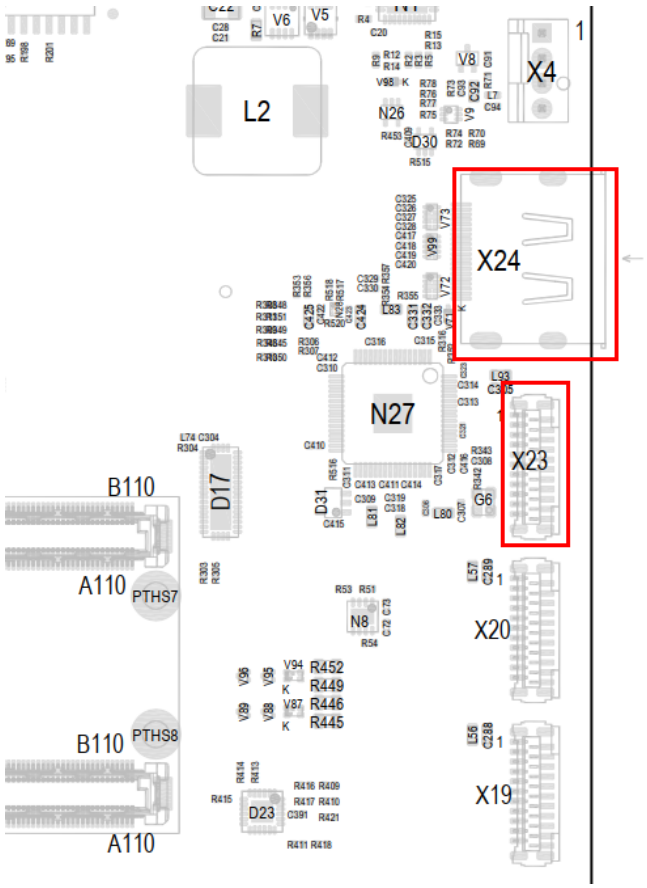

Figure 21: Position X23 (MIPI-DSI) and X24 (DisplayPort)

4.2.6 MIPI-CSI

The four Camera Serial Interfaces (CSI[3:0]) on the TQMa67xx are available with four lanes each on connectors X18, X19, and X20 of the MBa67xx.

The selection of the X18 connector and the pin assignment correspond to the TQ-specific specifications for the standardized design of the interface, which enables the connection of the TQ camera adapter. The camera adapter enables the connection of dedicated cameras. The selection of connector X19 and X20 corresponds to the 22-pin pinout for Raspberry PI.

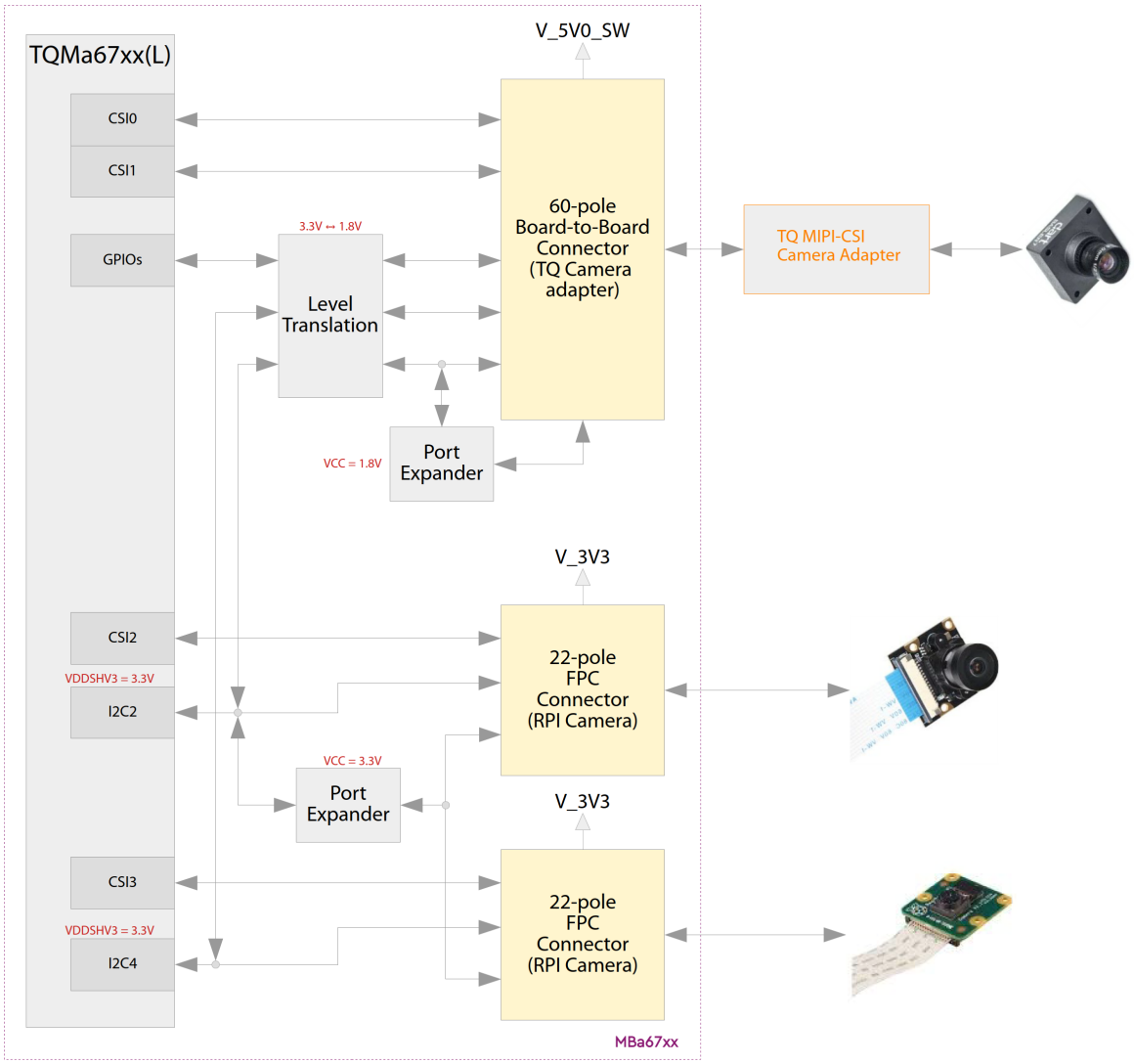

Figure 22: Block diagram MIPI-CSI interface

The selection of the connector X18 (Type: TE 5177986-2) and the pin assignment correspond to the TQ-specific specifications for the uniform design of the interface which enables the connection of the TQ camera adapter. The camera adapter enables the connection of dedicated cameras. The selection of connector X19 and X20 corresponds to the 22-pin pinout for Raspberry PI.

Table 11: MIPI-CSI pinout X18

Pin	Signal	Type	Level	Note
1	DGND	P	0 V	Ground
2	DGND	P	0 V	
3	CSI0_EN	O	1.8 V	CSI enable, pulldown on MBa67xx
4	CSI1_EN	O	1.8 V	CSI enable, pulldown on MBa67xx
5	CSI0_RST#	O	1.8 V	Reset, pulldown on MBa67xx
6	CSI1_RST#	O	1.8 V	Reset, pulldown on MBa67xx
7	CSI0_TRIGGER	I	1.8 V	General purpose input (e.g. trigger input)
8	CSI1_TRIGGER	I	1.8 V	General purpose input (e.g. trigger input)
9	CSI0_SYNC	I	1.8 V	General purpose input (e.g. sync input)
10	CSI1_SYNC	I	1.8 V	General purpose input (e.g. sync input)
11	NC	-	-	Not connected
12	NC	-	-	
13	DGND	P	0 V	Ground
14	DGND	P	0 V	
15	CSI0_RXN3	I	1.8 V	CSI interface (Lane 3)
16	CSI1_RXN3	I	1.8 V	CSI interface (Lane 3)
17	CSI0_RXP3	I	1.8 V	CSI interface (Lane 3)
18	CSI1_RXP3	I	1.8 V	CSI interface (Lane 3)
19	DGND	P	0 V	Ground
20	DGND	P	0 V	
21	CSI0_RXN2	I	1.8 V	CSI interface (Lane 2)
22	CSI1_RXN2	I	1.8 V	CSI interface (Lane 2)
23	CSI0_RXP2	I	1.8 V	CSI interface (Lane 2)
24	CSI1_RXP2	I	1.8 V	CSI interface (Lane 2)
25	DGND	P	0 V	Ground
26	DGND	P	0 V	
27	CSI0_RXN1	I	1.8 V	CSI interface (Lane 1)
28	CSI1_RXN1	I	1.8 V	CSI interface (Lane 1)
29	CSI0_RXP1	I	1.8 V	CSI interface (Lane 1)
30	CSI1_RXP1	I	1.8 V	CSI interface (Lane 1)
31	DGND	P	0 V	Ground
32	DGND	P	0 V	
33	CSI0_RXN0	I	1.8 V	CSI interface (Lane 0)
34	CSI1_RXN0	I	1.8 V	CSI interface (Lane 0)
35	CSI0_RXP0	I	1.8 V	CSI interface (Lane 0)
36	CSI1_RXP0	I	1.8 V	CSI interface (Lane 0)
37	DGND	P	0 V	Ground
38	DGND	P	0 V	
39	CSI0_RXCLKN	I	1.8 V	CSI interface (Clock)
40	CSI1_RXCLKN	I	1.8 V	CSI interface (Clock)
41	CSI0_RXCLKP	I	1.8 V	CSI interface (Clock)
42	CSI1_RXCLKP	I	1.8 V	CSI interface (Clock)
43	DGND	P	0 V	Ground
44	DGND	P	0 V	
45	I2C2_1V8_SDA	I/O	1.8 V	Data for I2C configuration interface
46	I2C4_1V8_SDA	I/O	1.8 V	Data for I2C configuration interface
47	I2C2_1V8_SCL	O	1.8 V	Clock for I2C configuration interface
48	I2C4_1V8_SCL	O	1.8 V	Clock for I2C configuration interface
49	DGND	P	0 V	Ground
50	DGND	P	0 V	Ground
51	EHRPWM2_A	O	1.8 V	Master clock (PWM signal fromAM67x)
52	EHRPWM2_B	O	1.8 V	Master clock (PWM signal from AM67x)
53	DGND	P	0 V	Ground
54	DGND	P	0 V	
55	NC	-	-	Not connected
56	V_5V0_SW	P	5 V	5 V supply (filtered from V_5V0_SW)
57	NC	-	-	Not connected
58	V_5V0_SW	P	5 V	5 V supply (filtered from V_5V0_SW)
59	NC	-	-	Not connected
60	V_5V0_SW	P	5 V	5 V supply (filtered from V_5V0_SW)

Table 12: Pinout X19

Pin	Signal	Type	Level	Note
1	DGND	P	0 V	Ground
2	CSI2_RXN0	I	1.8 V	CSI interface (Lane 0)
3	CSI2_RXP0	I	1.8 V	CSI interface (Lane 0)
4	DGND	P	0 V	Ground
5	CSI2_RXN1	I	1.8 V	CSI interface (Lane 1)
6	CSI2_RXP1	I	1.8 V	CSI interface (Lane 1)
7	DGND	P	0 V	Ground
8	CSI2_RXCLKN	I	1.8 V	CSI interface (Clock)
9	CSI2_RXCLKP	I	1.8 V	CSI interface (Clock)
10	DGND	P	0 V	Ground
11	CSI2_RXN2	I	1.8 V	CSI interface (Lane 2)
12	CSI2_RXP2	I	1.8 V	CSI interface (Lane 2)
13	DGND	P	0 V	Ground
14	CSI2_RXN3	I	1.8 V	CSI interface (Lane 3)
15	CSI2_RXP3	I	1.8 V	CSI interface (Lane 3)
16	DGND	P	0 V	Ground
17	CAM1_GPIO1	O	3.3 V	GPIO, pulldown on MBa67xx
18	CAM1_GPIO1	O	3.3 V	GPIO, pulldown on MBa67xx
19	DGND	P	0 V	Ground
20	I2C2_SCL	I/O	3.3 V	Data for I2C configuration interface
21	I2C2_SDA	I/O	3.3 V	Data for I2C configuration interface
22	V_3V3	P	3.3 V	Supply max. 1 A

Table 13: Pinout X20

Pin	Signal	Type	Level	Note
1	DGND	P	0 V	Ground
2	CSI3_RXN0	I	1.8 V	CSI interface (Lane 0)
3	CSI3_RXP0	I	1.8 V	CSI interface (Lane 0)
4	DGND	P	0 V	Ground
5	CSI3_RXN1	I	1.8 V	CSI interface (Lane 1)
6	CSI3_RXP1	I	1.8 V	CSI interface (Lane 1)
7	DGND	P	0 V	Ground
8	CSI3_RXCLKN	I	1.8 V	CSI interface (Clock)
9	CSI3_RXCLKP	I	1.8 V	CSI interface (Clock)
10	DGND	P	0 V	Ground
11	CSI3_RXN2	I	1.8 V	CSI interface (Lane 2)
12	CSI3_RXP2	I	1.8 V	CSI interface (Lane 2)
13	DGND	P	0 V	Ground
14	CSI3_RXN3	I	1.8 V	CSI interface (Lane 3)
15	CSI3_RXP3	I	1.8 V	CSI interface (Lane 3)
16	DGND	P	0 V	Ground
17	CAM2_GPIO1	O	3.3 V	GPIO, pulldown on MBa67xx
18	CAM2_GPIO1	O	3.3 V	GPIO, pulldown on MBa67xx
19	DGND	P	0 V	Ground
20	I2C4_SCL	I/O	3.3 V	Data for I2C configuration interface
21	I2C4_SDA	I/O	3.3 V	Data for I2C configuration interface
22	V_3V3	P	3.3 V	Supply max. 1 A

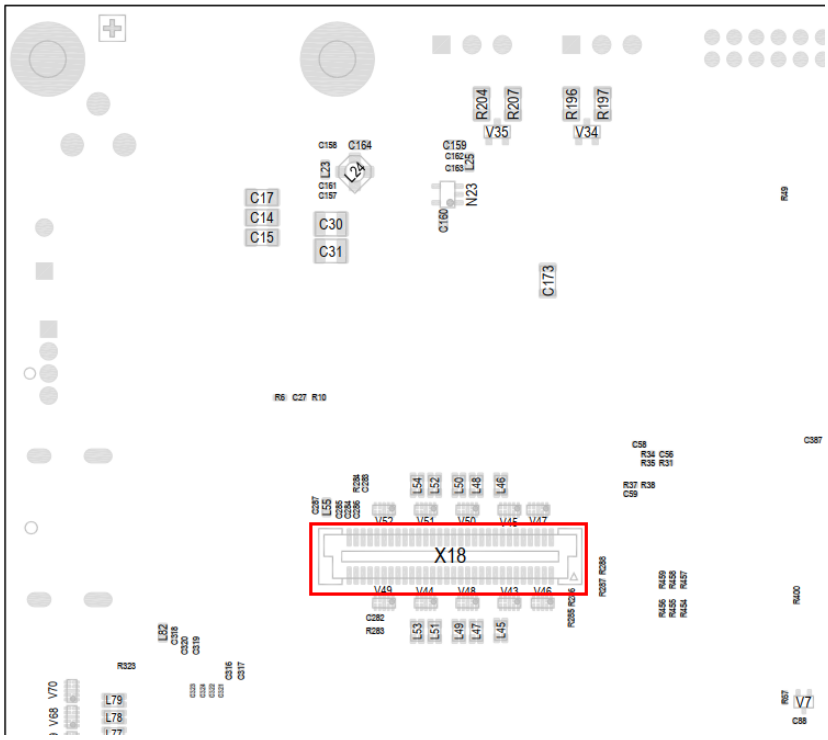

Figure 23: Position X18

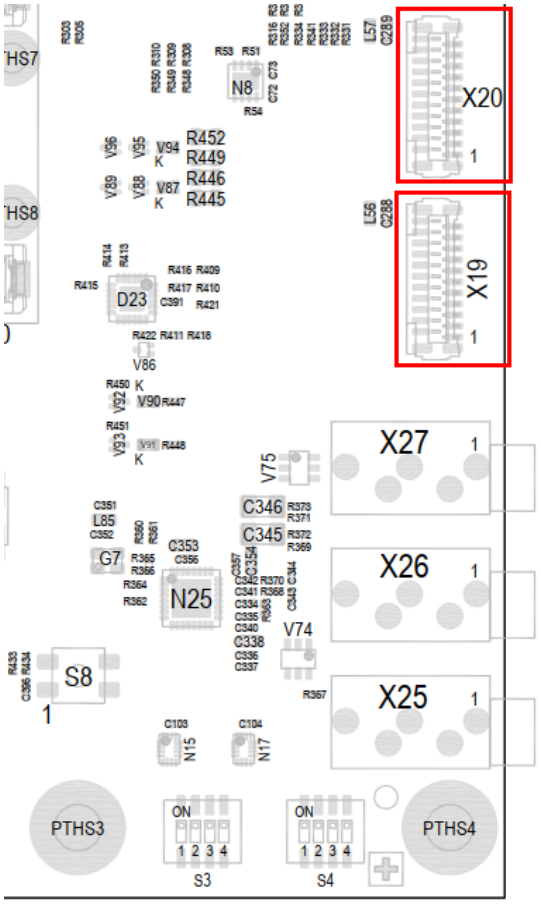

Figure 24: Position X19 and X20

4.2.7 CAN

Two CAN interfaces are implemented on MBa67xx according to the ISO 11898 standard. The signals are each provided on a 3-pin socket X12 and X13 (Type: Phoenix Contact MCV 1,5/ 3-G-3,5).

Both interfaces are galvanically isolated with an isolation voltage of 1 kV, but not from each other.

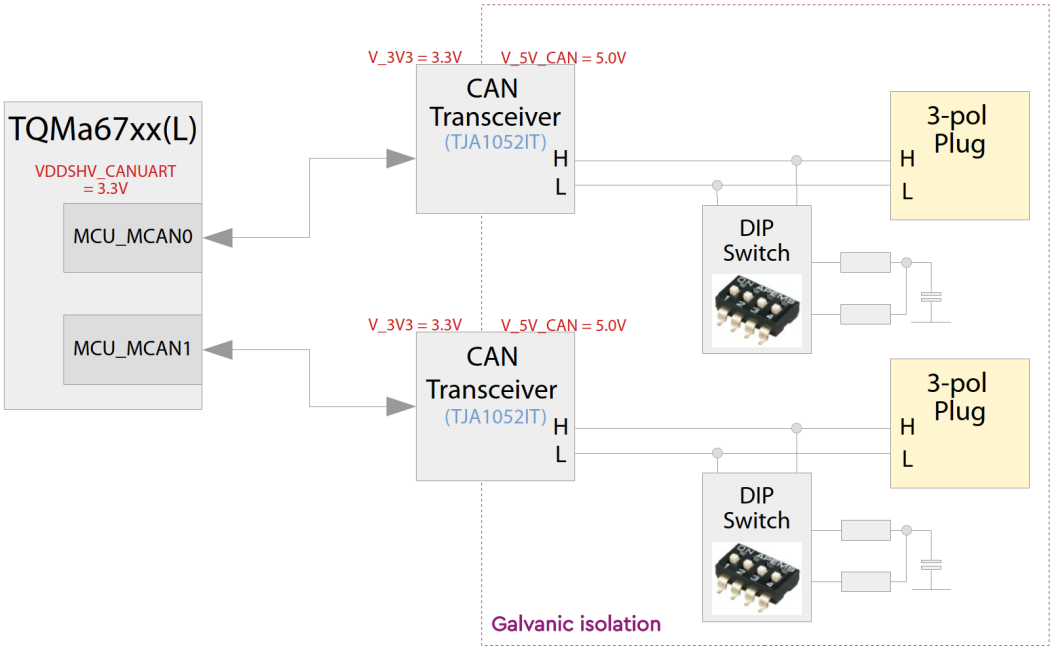

Figure 25: Block diagram CAN

The following tables show the pin assignment of the CAN connectors and the DIP switch for the 120 Ω CAN signal termination:

Table 14: CAN0 pinout (X12)

Pin	Pin name	Signal	I/O	Note
1	CAN_H	CAN0_H	I/O	galvanically isolated
2	CAN_L	CAN0_L	I/O	galvanically isolated
3	DGND	DGND_CAN	P	galvanically isolated

Table 15: CAN1 pinout (X13)

Pin	Pin name	Signal	I/O	Note
1	CAN_H	CAN1_H	I/O	galvanically isolated
2	CAN_L	CAN1_L	I/O	galvanically isolated
3	DGND	DGND_CAN	P	galvanically isolated

Table 16: CAN termination

DIP-Switch	Interface	ON	OFF
S6	CAN0	Termination CAN0 with 120 Ω	No termination CAN0
S7	CAN1	Termination CAN1 with 120 Ω	No termination CAN1

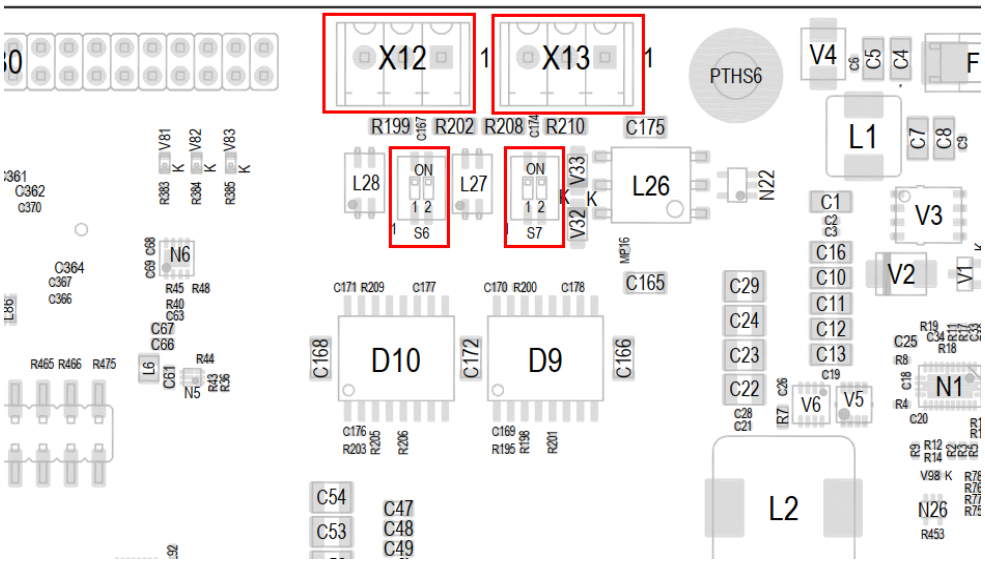

Figure 26: Position of CAN connectors and DIP switches

4.2.8 RS485

On the MBa67xx a RS485 interface on connector X8 (type: Phoenix Contact MC1,5/2-G-3,5) with automatic direction switching is realized, which allows the use of Profibus. The direction switching is done via GPIO.

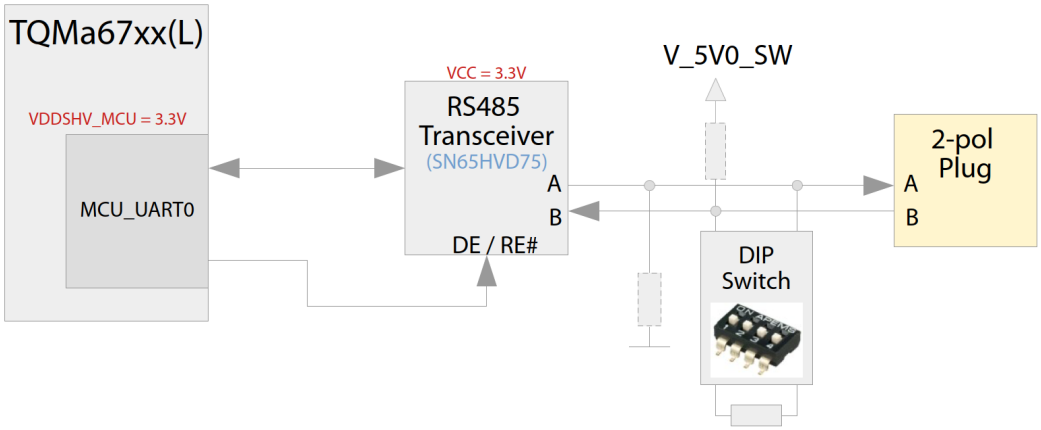

Figure 27: Block diagram RS485

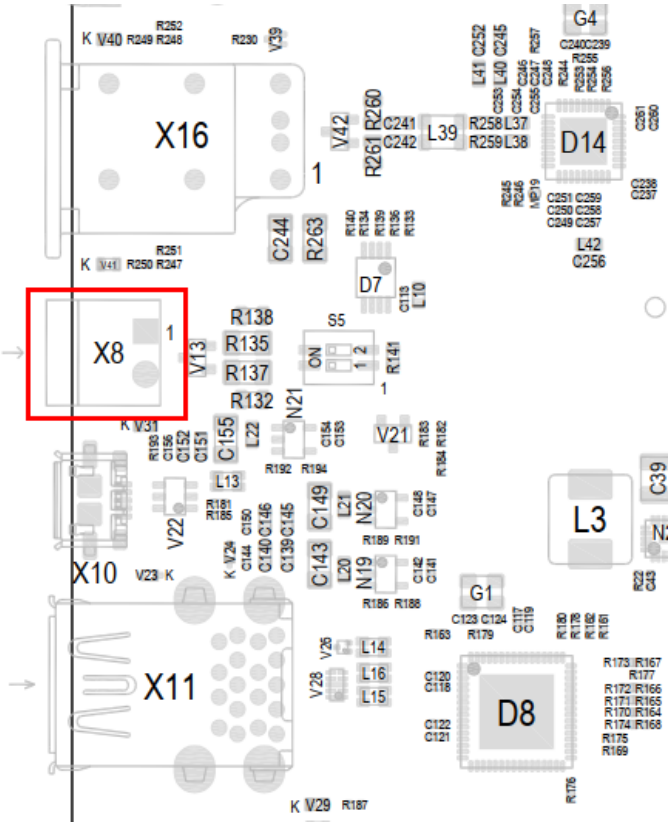

Figure 28: Position of RS485, X8

4.2.9 WLAN / WPAN

The WiFi / WPAN Companion IC CC3351 from Texas Instruments is integrated on the MBa67xx:

- IEEE 802.11 a/b/g/n/ax (2.4 GHz, 5 GHz) - dual band
- Interfaces
  - SDIO via MMC2
  - UART via UART2
- The WLAN / WPAN has one antenna connector (u.FL sockets)

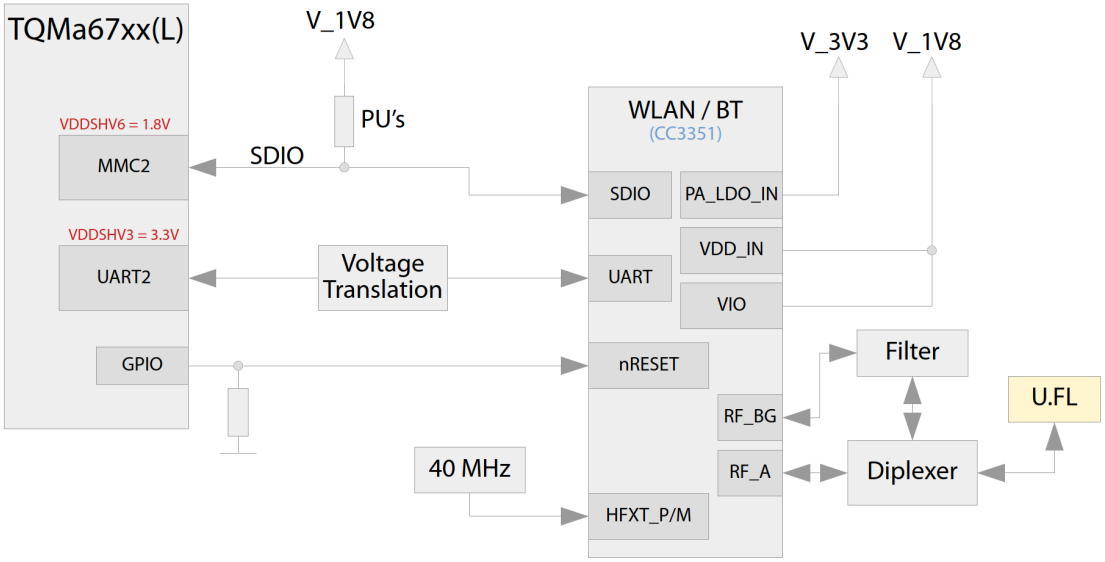

Figure 29: Block diagram WLAN / WPAN module

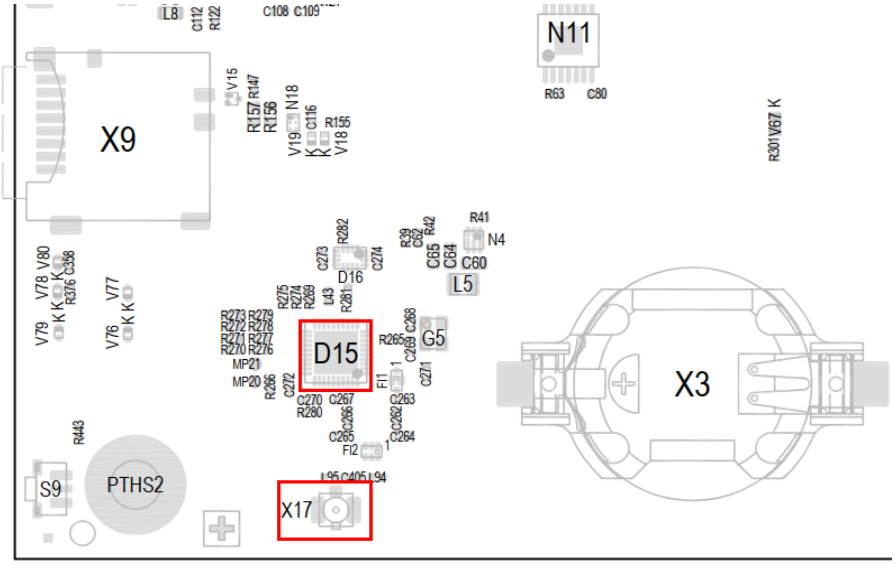

Figure 30: Position WLAN Companion IC and antenna socket X17

4.2.10 Mini PCIe + SIM card

In addition to the SGMII interface, the SERDES1 lane on the MBa67xx is multiplexed as PCIe by an analog multiplexer. This enables the use of a mini PCIe interface.

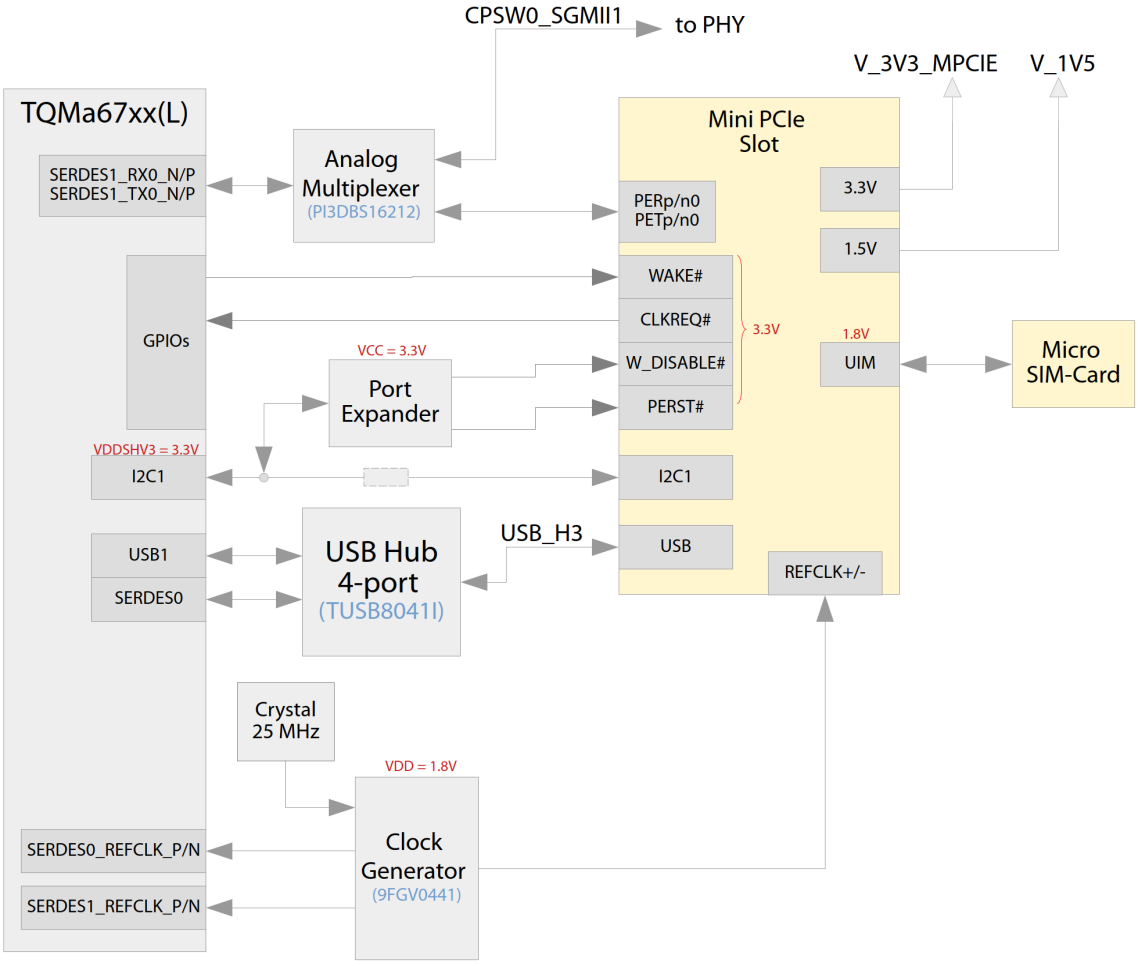

Figure 31: Block diagram Mini PCIe + SIM Card

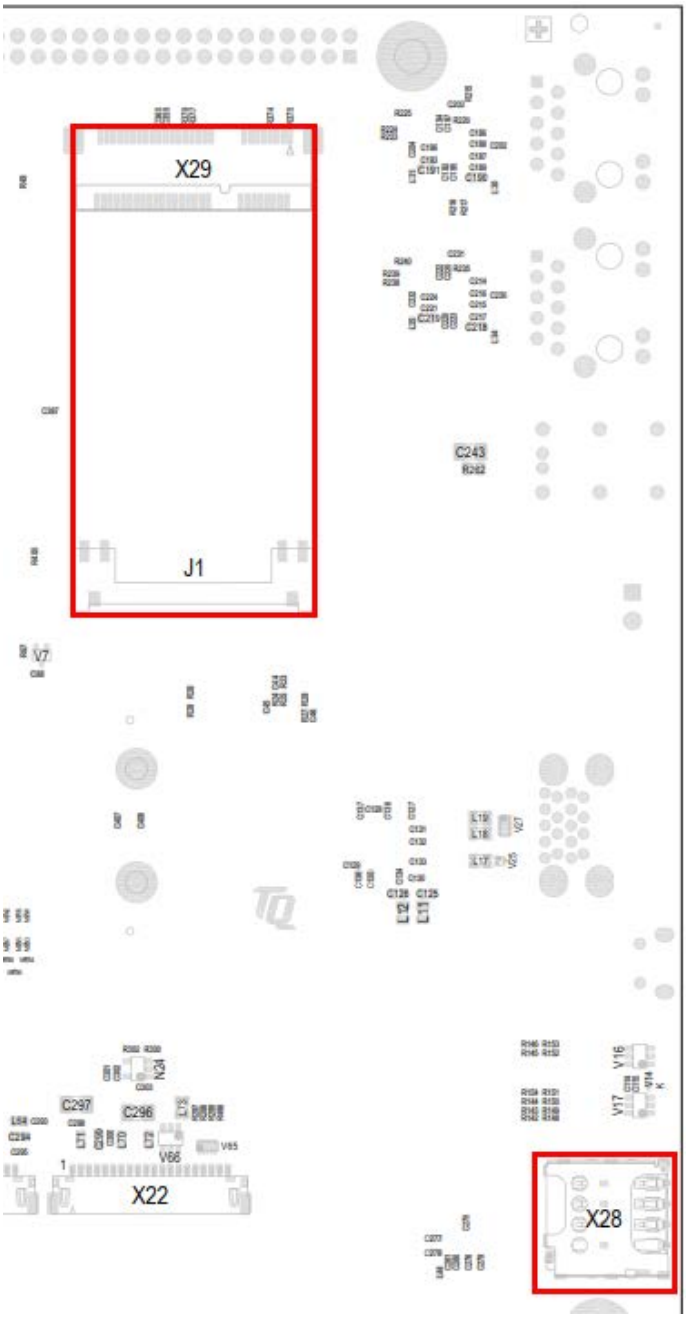

Figure 32: Position MiniPCIe (X29) and SIM card holder (X28)

4.2.11 SD card

On the MBa67xx a SDIO (MMC1) interface of the CPU is implemented for a SD card connection (connector X9):

- MMC1 interface with 4 bit bus width
- Module provides an adapted supply voltage VDDSHV5 (1.8 V / 3.3 V) depending on the mode
- VDDSHV5 can be used for pull-up supply
- Power switch (3.3 V) provided for SD card supply
    - Power Cycle with RESETSTATz or via GPIO (MMC1_SD_EN)

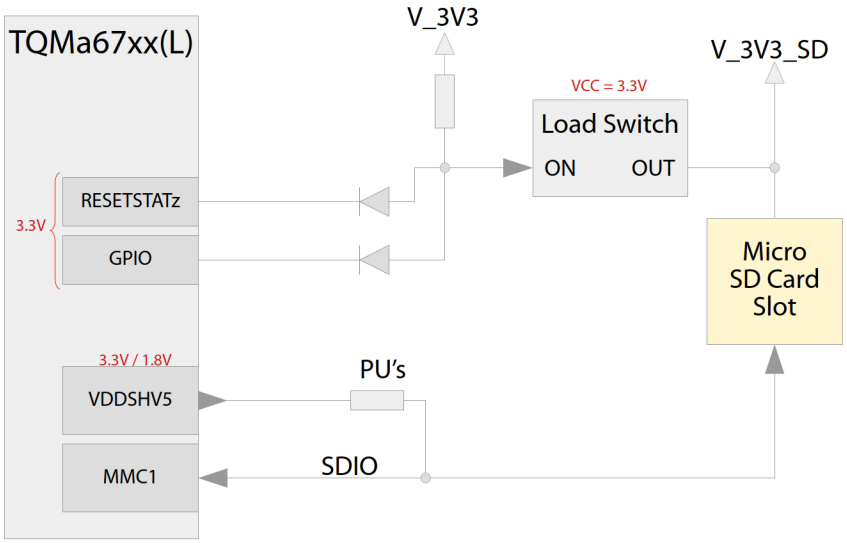

Figure 33: Block diagram SD card slot, X3

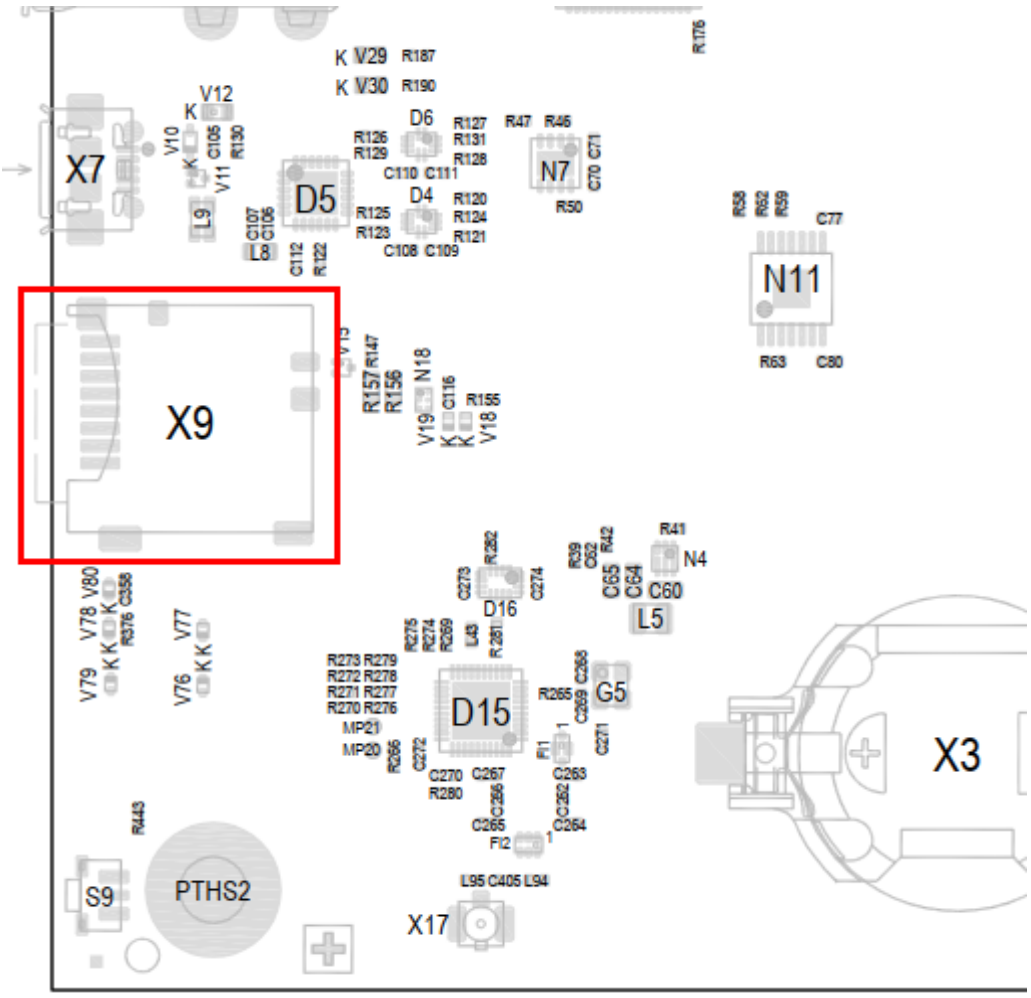

Figure 34: Position SD-Card, X9

4.2.12 JTAG interface

The JTAG signals of the CPU are provided on the 20-pin header X32.

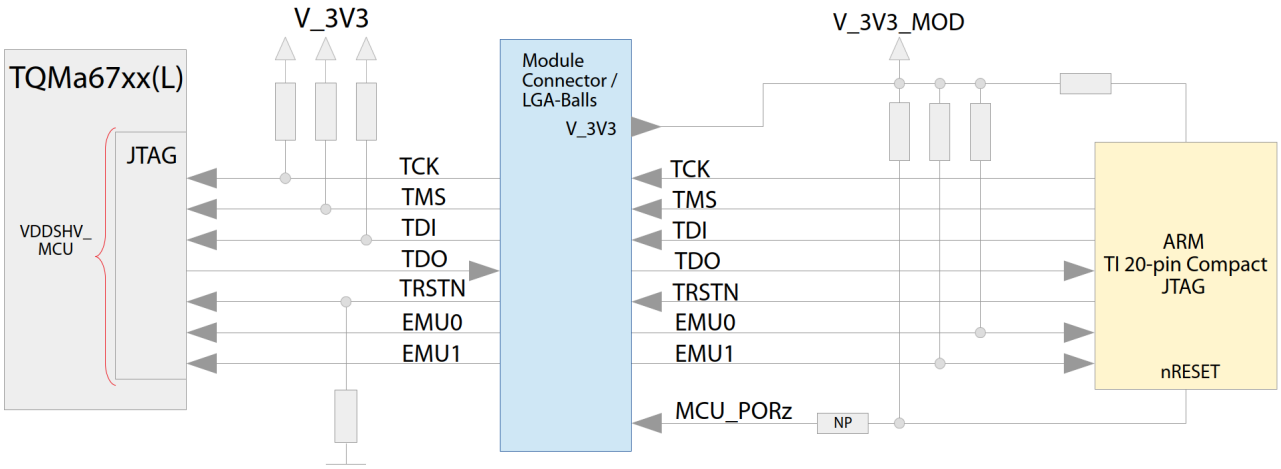

Figure 35: Block diagram JTAG

Table 17: JTAG signals

Signal / Multiplexing	I/O	Power group	Note
TCK	I	VDDSHV_MCU (3.3 V)	10 kΩ Pull-Up on module
TDI	I		10 kΩ Pull-Up on module
TDO	O		
TMS	I		10 kΩ Pull-Up on module
TRST#	I		4.7 kΩ Pull-Up on module
EMU[1:0]	IO		Optional signals, not required for JTAG

Table 18: Pinout JTAG interface X32 (Segger TI-CTI-20 Adapter)

Signal	Pin	Pin	Signal
TMS	1	2	TRST
TDI	3	4	GND
VTref	5		NC (Key)
TDO	7	8	GND
RTCK	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1
NSRST	15	16	GND
NC	17	18	NC
NC	19	20	GND

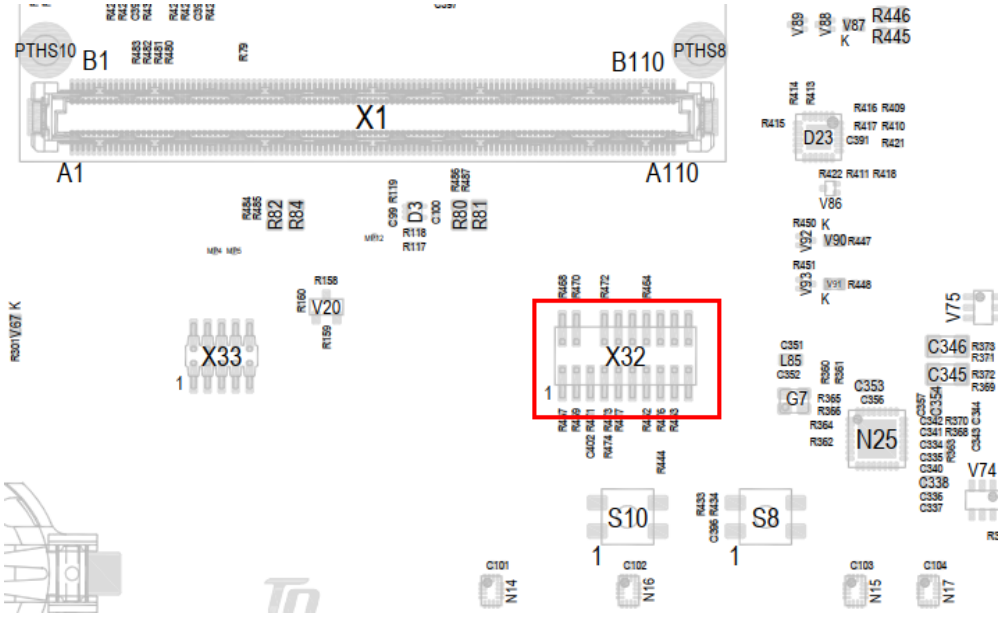

Figure 36: Position of JTAG, X32

4.3 Audio

The MBa67xx provides one microphone, line-in and line-out interface each. The signals can be tapped via 3.5 mm jack sockets, which are provided by an audio code via SAI and I2C interfaces by the TQMa67xx.

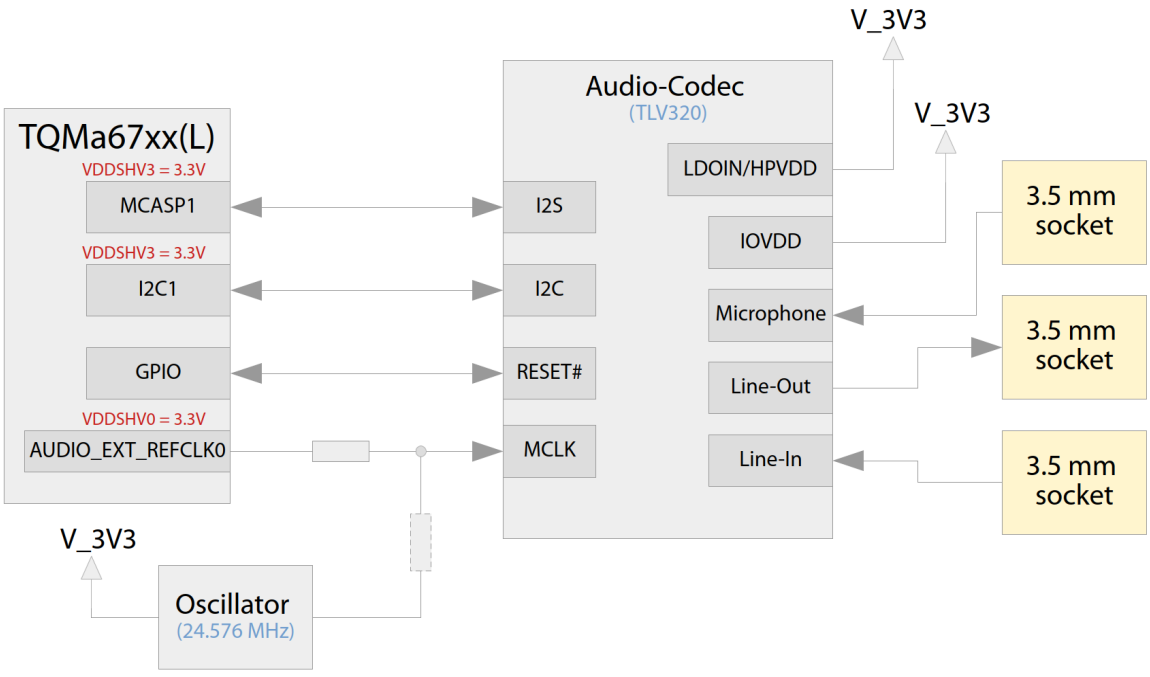

Figure 37: Block diagram audio interface

Optionally, the line-out interface can also be configured as a headphone output. Further details can be found in the following table:

Table 19: Placement ootions for audio interface

Mode	R340	R342	R343	R344	Note
Headphone	n.p.	n.p.	0R	0R	
Line-out	0R	0R	n.p.	n.p.	Default option

4.4 Headers X30, X31, X33

Control signals, GPIOs or factory test signals are routed to pin headers as follows:

- GPIOs at X30
- Control signals at X31
- SEC interface at X33

Figure 38: Position of headers X30, X31, X33

Table 20: Pinout header X30

Pin	Signal	I/O	Note
1	V_3V3	P	
2	V_5V0_SW	P	
3	I2C3_SDA	I/O	
4	V_5V0_SW	P	
5	I2C3_SCL	O	
6	DGND	P	
7	GPIO4	I/O	
8	UART1_TXD	O	
9	DGND	P	
10	UART1_RXD	I	
11	UART1_RTS#	O	
12	GPIO18	I/O	
13	GPIO27	I/O	
14	DGND	P	
15	GPIO22	I/O	
16	GPIO23	I/O	
17	V_3V3	P	
18	GPIO24	I/O	
19	MCU_SPI0_D0	I/O	
20	DGND	P	
21	MCU_SPI0_D1	I/O	
22	GPIO25	I/O	
23	MCU_SPI0_CLK	O	
24	MCU_SPI0_CS0	O	
25	DGND	P	
26	MCU_SPI0_CS1	O	
27	I2C1_SDA	I/O	
28	I2C1_SCL	O	
29	GPIO5	I/O	
30	DGND	P	

Table 21: Pinout header X31

Pin	Signal	I/O	Note
1	V_3V3	P	
2	V_1V8	P	
3	DGND	P	
4	DGND	P	
5	TQMa67xx_HARD_RST#	I	
6	PORz_OUT	O	
7	MCU_PORz	I	
8	MCU_RESETSTATz	O	
9	MCU_RESETz	I	
10	RESETSTATz	O	
11	RESET_REQz	I	
12	DGND	P	
13	TQ_EEPROM_WC#	I	Data EEPROM (do not connect)
14	RTC_CLKOUT	O	
15	DGND	P	
16	RTC_INT#	O	GPIO
17	CUST_EEPROM_WC#	I	
18	TEMP_ALERT	O	
19	TQMa67xx_PGOOD	O	
20	MCU_ERROR#	I/O	

Table 22: Pinout header X33

Pin	Signal	I/O	Note
1	V_3V3	P	
2	V_1V8	P	
3	SE_7816_IO1	I/O	3.3 V IO-logic
4	SE_14443_LA	I/O	
5	SE_7816_IO2	I/O	
6	SE_14443_LB	I/O	
7	SE_7816_CLK	I	
8	SE_ENA	I	
9	SE_7816_RST#	I	
10	DGND	P	

4.5 Diagnosis- and user interfaces

4.5.1 Diagnosis LEDs

The MBa67xx provides the following status LEDs to indicate the system condition:

Table 23: Status LEDs

Reference	Description	Control signal	Colour
V87	TQMa67xx PGOOD	TQMa67xx_PGOOD	Green / red
V94	MBa67xx PGOOD	PG_12V_5V_SW	Green / red
V97	Power X5 / X6	V_24V_IN	Blue
V90	User LED 1	USER_LED_1 (MCU_GPIO0_11)	Green
V91	User LED 2	USER_LED_2 (MCU_GPIO0_12)	Yellow
V31	VBUS OTG	USB0_DRVVBUS	Green
V29	VBUS H1	EN_USB_H1_VBUS	Green
V30	VBUS H2	EN_USB_H2_VBUS	Green
V67	VBUS H4	EN_USB_H4_VBUS	Green
X14 / X15 / X16	Activity / Link LED (Ethernet)	PHY-LED signales	Green / yellow
V12	USB Debug Self-Power (5 V)	5 V input of X7	Blue
V81	WWAN	LED_WWAN#	Green
V82	WLAN	LED_WLAN#	Green
V83	WPAN	LED_WPAN#	Green

4.5.2 Navigation button

A navigation button (user button) is available to the user on the MBa67xx.

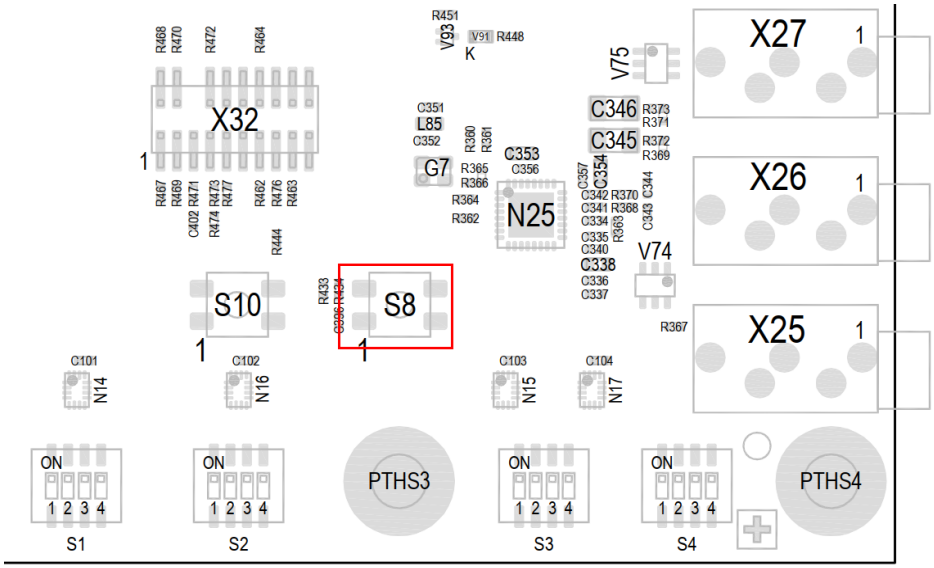

Figure 39: Position of navigation button S8

4.5.3 Reset buttons

Two reset buttons are available to the user on the MBa67xx.

Table 24: Reset buttons

Reference	Description	Control signal
S9	Activates the power sequencing on the module	TQMa67xx_HARD_RST#
S10	Control of cold reset	MCU_PORz

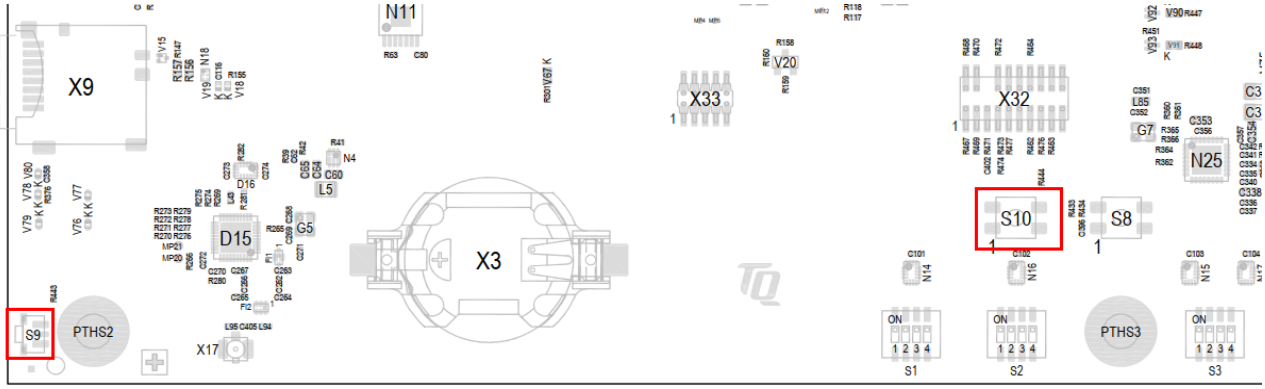

Figure 40: Position reset buttons S9 / S10

4.5.4 Boot-Mode configuration

The MBa67xx supports the following boot sources of the TQMa67xx:

- eMMC Flash (internal to module)
- QSPI-NOR flash (internal to module)
- UART (external host) via Debug-USB (X7)
- USB slave (USB boot from external host) via USB-OTG (X10)

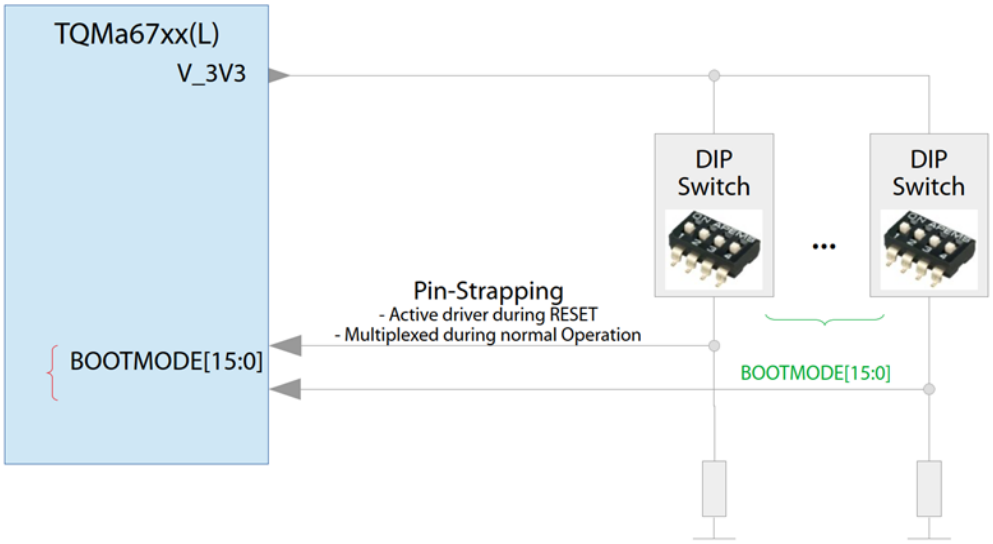

Figure 41: Block diagram boot source

The boot source is selected via the corresponding boot strap pins which can be set via DIP switches. The following table shows the settings of the DIP switch configuration.

Table 25: Boot mode configuration

DIP-Switch		Signal	eMMC	SPI-NOR	SD-Card	UART	USB
S1	1	BOOTMODE00	ON	ON	ON	ON	ON
	2	BOOTMODE01	ON	ON	ON	ON	ON
	3	BOOTMODE02	OFF	OFF	OFF	OFF	OFF
	4	BOOTMODE03	OFF	ON	OFF	ON	OFF
S2	1	BOOTMODE04	OFF	ON	OFF	ON	ON
	2	BOOTMODE05	OFF	OFF	OFF	ON	OFF
	3	BOOTMODE06	ON	OFF	ON	OFF	ON
	4	BOOTMODE07	OFF	OFF	OFF	Don't care	OFF
S3	1	BOOTMODE08	OFF	ON	OFF	Don't care	OFF
	2	BOOTMODE09	OFF	Don't care	ON	Don't care	OFF
	3	BOOTMODE10	Don't care	Don't care	Don't care	Don't care	Don't care
	4	BOOTMODE11	Don't care	Don't care	Don't care	Don't care	Don't care
S4	1	BOOTMODE12	Don't care	Don't care	Don't care	Don't care	Don't care
	2	BOOTMODE13	Don't care	Don't care	Don't care	Don't care	Don't care
	3	BOOTMODE14	OFF	OFF	OFF	OFF	OFF
	4	BOOTMODE15	OFF	OFF	OFF	OFF	OFF

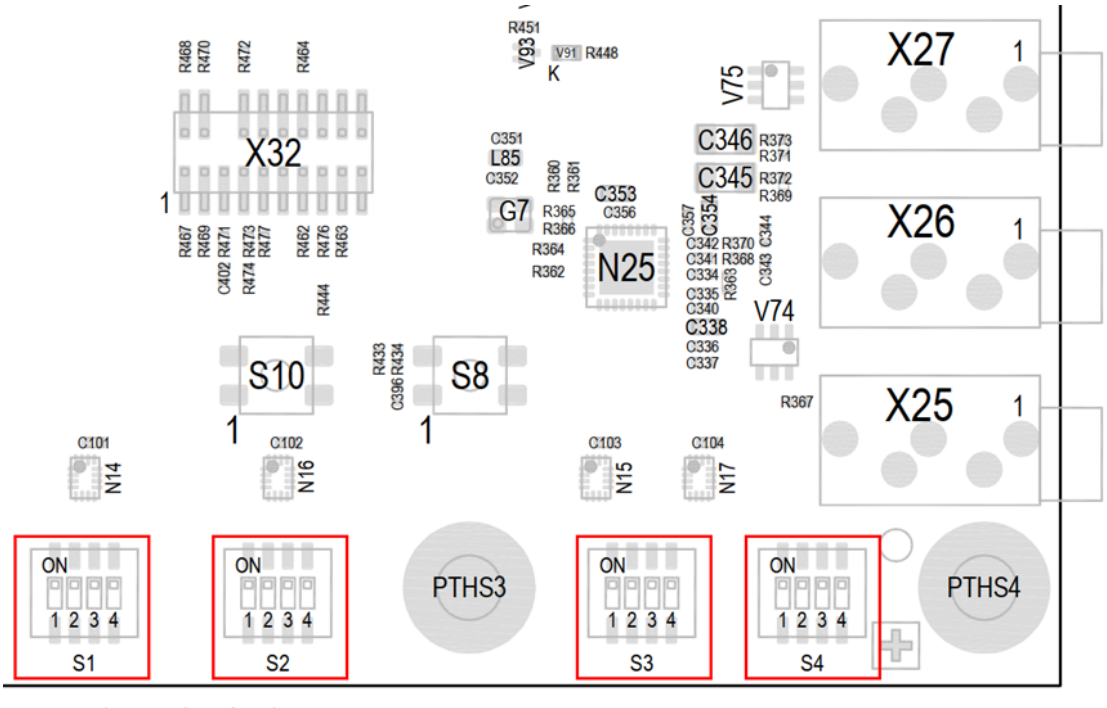

Figure 42: Placement DIP switches for boot source

4.6 Impedances

Typically, all signals have a single-ended impedance of nominal 50 Ω with a tolerance of ±10 %. Deviating from this, other impedances are also used on the MBa67xx depending on the signal requirements. The following table shows the affected interfaces:

Table 26: Impedances

Signal / Interface	Impedance TQMa67xx(L)	Recommended for mainboard
OLDI0	differential 100 Ω	differential 100 Ω ±10 %
DSI0	differential 100 Ω	differential 100 Ω ±10 %
CSI[3:0]	differential 100 Ω	differential 100 Ω ±10 %
SERDES[1:0]	differential 85 Ω	differential 85 Ω ±10 %
USB[1:0]	differential 90 Ω	differential 90 Ω ±10 %

5. SOFTWARE

No software is required for the MBa67xx.
Suitable software is only required on the module TQMa67xx and is not a part of this specification.
More information can be found in the Support Wiki for the TQMa67xx.

6. MECHANICS

6.1 Dimensions

The MBa67xx has overall dimensions (length × width) of 170.0 mm × 170.0 mm (± 0.1 mm).
There are holes for six housing fixings with 4.2 mm Ø each and four holes with 2.7 mm Ø each for heat sink fixings.
The mass of the MBa67xx is 190 g (± 2 g)

6.2 Thermal management

Depending on the application, the power consumption of the CPU makes it necessary to ensure a cooling of the CPU. For this a 4-pin connector X4 (Type: Molex 47053-1000) is provided on the MBa67xx for a standard fan. For more information, please refer to the TQMa67xx User's Manual.

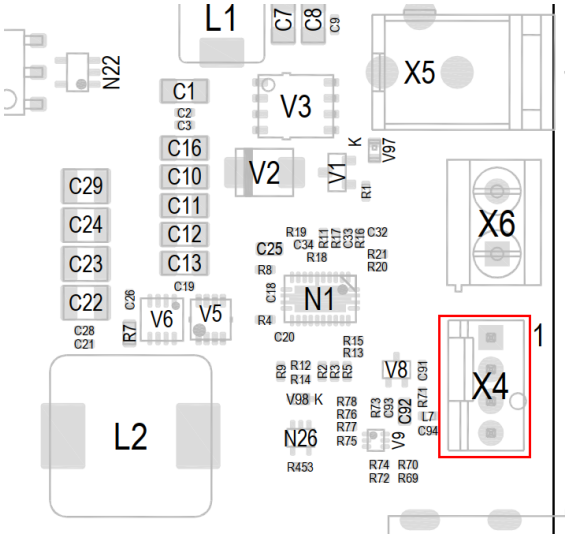

Figure 43: Position X4

Table 27: Pinout X33

Pin	Signal	Note
1	DGND	
2	V_FAN	Imax: 150 mA @ 12 V
3	FAN_RPM	
4	FAN_PWM	

6.3 MBa67xx assembly

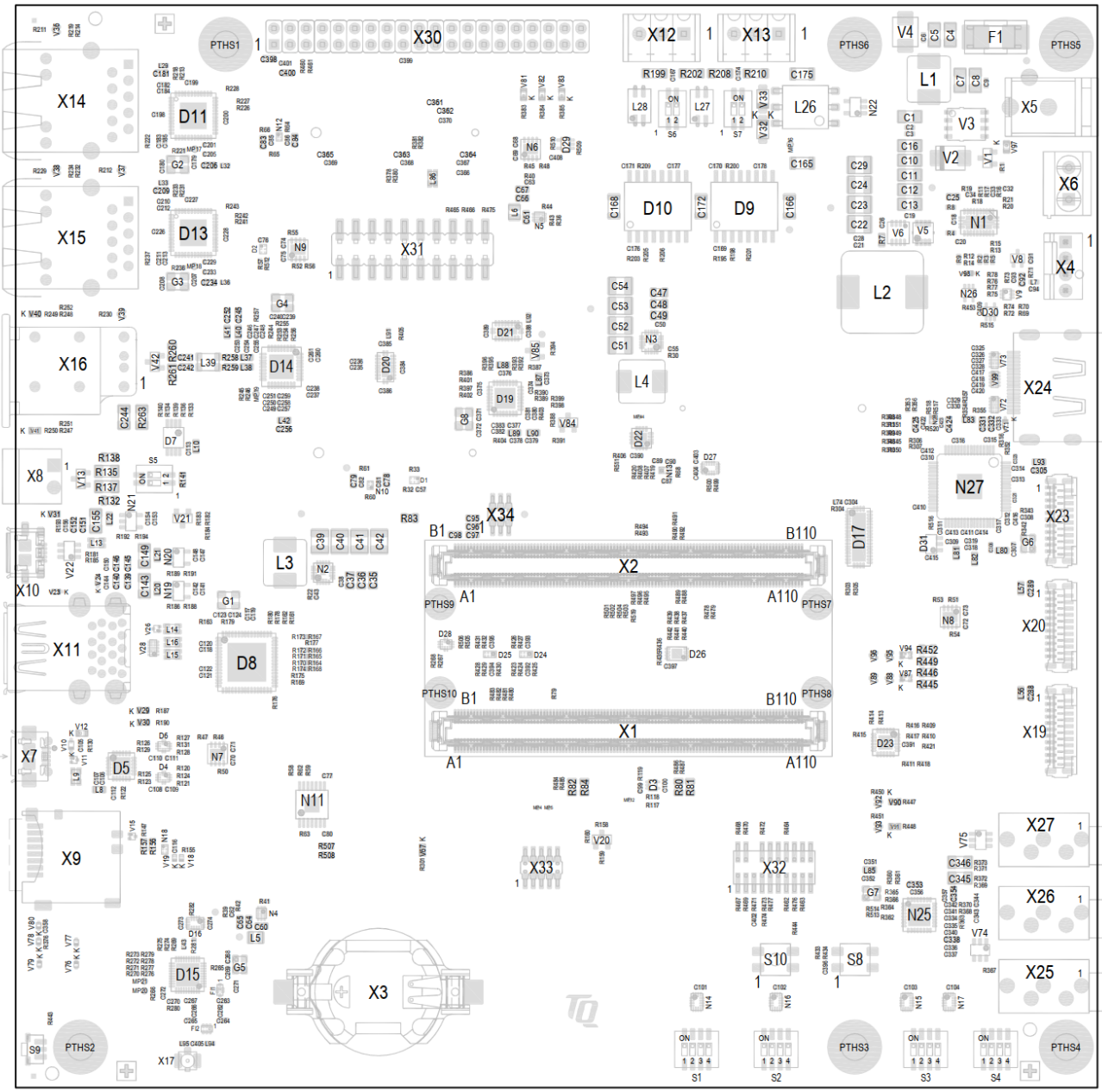

Figure 44: MBa67xx, component placement top

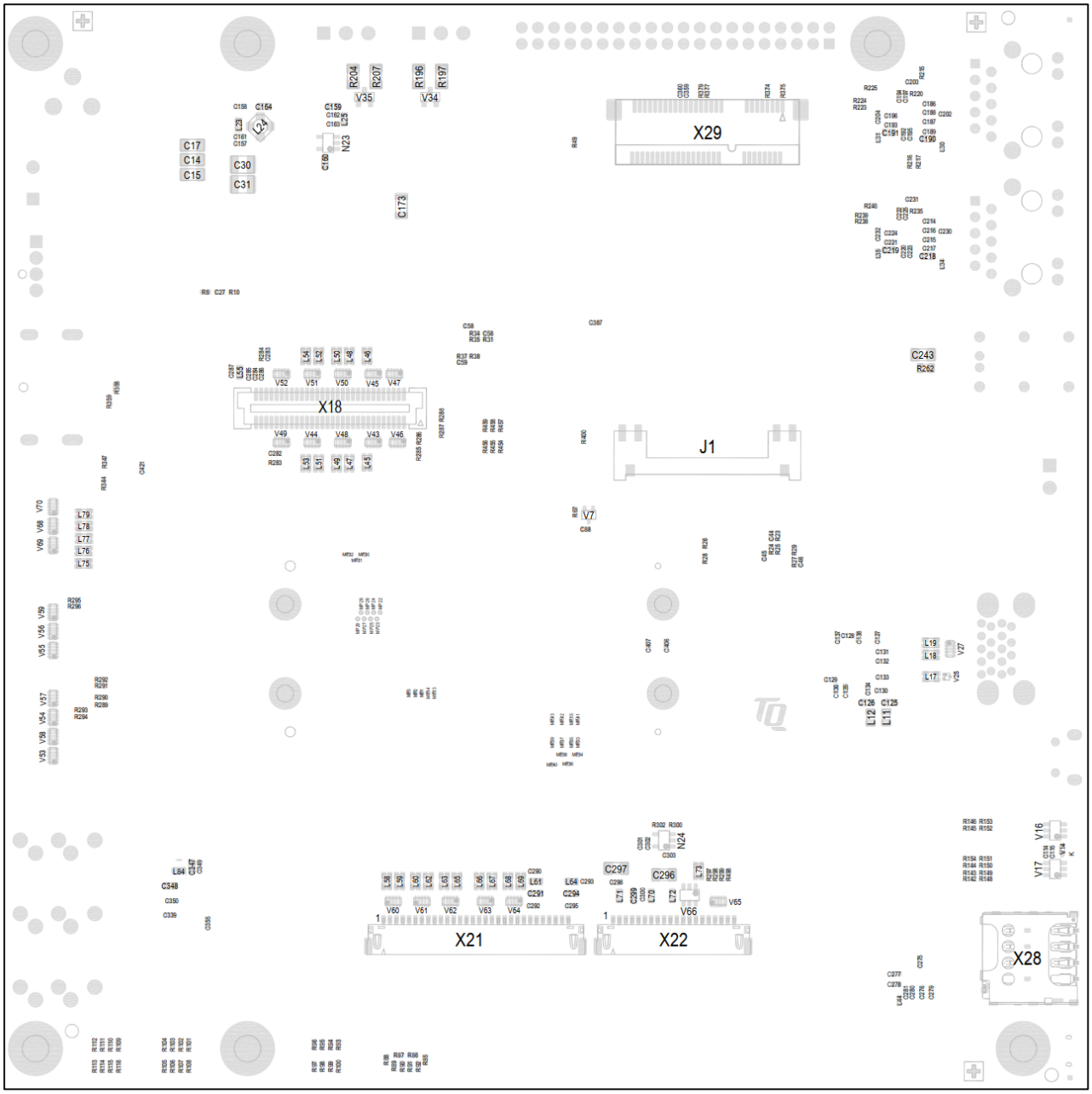

Figure 45: MBa67xx, component placement bottom

6.4 Label placement

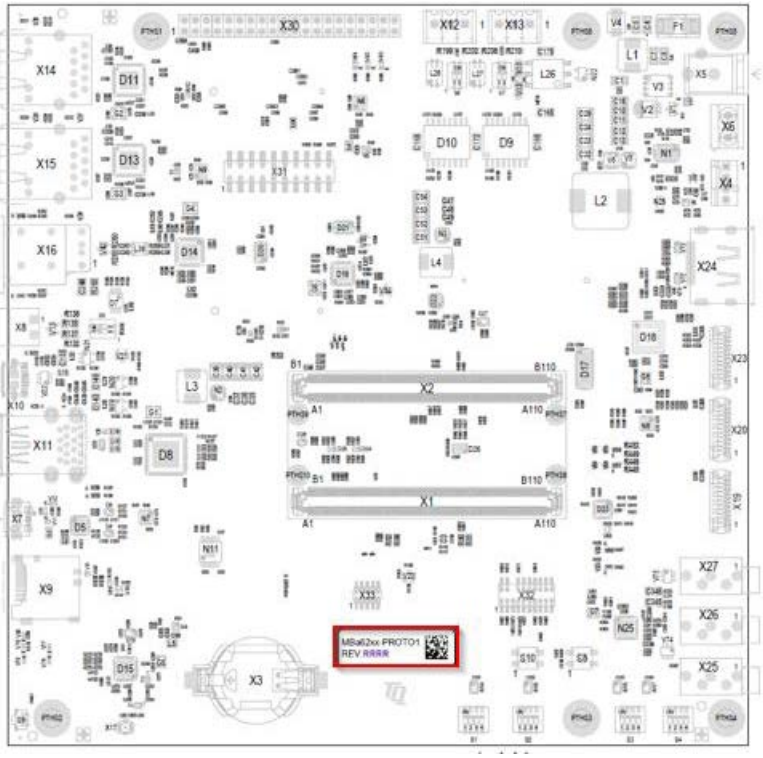

Figure 46: Label placement

Table 28: Label

Name	Note
AK1	TQ Serial number and article description

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The MBa67xx was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs for multi-pole interfaces (e.g. LC display)

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the MBa67xx.

The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

7.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety haven't been carried out.

7.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the MBa67xx is only a sub-component of an overall system.

7.5 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

7.6 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.

- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

8. CLIMATIC AND OPERATIONAL CONDITIONS

The permissible temperature range of the module depends strongly on the installation situation (heat dissipation through heat conduction and convection) and the use. Therefore, no fixed value can be given for the entire module group. In general, reliable operation is ensured if the following conditions are met:

Table 29: Climatic and operational conditions MBa67xx

Parameter	Range	Note
Environmental temperature	-40 °C to +85 °C	Without Lithium battery
Storage temperature	-40 °C to +100 °C	–
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Attention:	
	The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the user's responsibility to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). When connecting the heat sink, special attention must be paid to the tolerance chain (PCB thickness, PCB curvature, BGA balls, BGA package, thermopad, heat sink). The CPU is not the highest component in every case. A defective cooling connection can lead to overheating of the module and thus to malfunctions, premature aging or destruction.

8.1 Protection against external effects

Protection class IP00 was defined for the MBa67xx. There is no protection against foreign objects, touch or humidity.

8.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa67xx.
The MBa67xx is designed to be insensitive to vibration and impact.
Service life limiting components such as electrolytic capacitors were not used.

9. ENVIRONMENT PROTECTION

9.1 RoHS

The MBa67xx is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa67xx was designed to be recyclable and easy to repair.

9.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

9.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa67xx must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the MBa67xx enable compliance with EuP requirements for the MBa67xx.

9.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

9.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa67xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The MBa67xx is delivered in reusable packaging.

9.7 Batteries

9.7.1 General notes

Due to technical reasons a battery is necessary for the MBa67xx. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

9.7.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 g
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).

- Basic lithium content per battery not more than 2 g
  (except for lithium ion batteries for which a lithium content of not more than 8 g per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa67xx, it is produced in such a way, that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls). These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

10. APPENDIX

10.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document.

Table 30: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR3L	DDR3 Low Voltage
DIN	German industry standard (Deutsche Industrie Norm)
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	European standard (Europäische Norm)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FFC	Flat Flex Cable
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
HP	Headphone
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LVDS	Low Voltage Differential Signal
MCASP	Multichannel Audio Serial Port
MII	Media Independent Interface
MMC	Multimedia Card
MSB	Most Significant Bit
MTBF	Mean operating Time Between Failures

Table 29: Acronyms (continued)

Acronym	Meaning
n.c.	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (OSI model layer)
PMIC	Power Management Integrated Circuit
PRU	Programmable Real-Time Unit
PU	Pull-Up
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ45	Registered Jack 45
RMS	Root Mean Square
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232, RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SD card	Secure Digital card
SD/MMC	Secure Digital Multimedia Card
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SMD	Surface-Mounted Device
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
THD	Through-Hole Device
THT	Through-Hole Technology
UART	Universal Asynchronous Receiver/Transmitter
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write-Protection
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

10.2 References

Table 31: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	J722S/TDA4VEN/TDA4AEN/AM67 Processor Silicon Revision 1.0 Technical Reference Manual	1.0 / Apr. 2025	Texas Instruments
(2)	AM67x Processors Datasheet	A / Sep. 2024	Texas Instruments
(3)	TQMa67xx User's Manual	– current –	TQ-Systems
(4)	Support-Wiki for the TQMa67xx	– current –	TQ-Systems

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