TQMa57xx
User's Manual

TQMa57xx UM 0105
08.02.2021

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TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	08.05.2018	Petz		Initial release
0101	04.06.2018	Petz	All	External links updated
0102	26.10.2018	Petz	All 3.2.6.5 Table 40, Table 41	Links updated, Registered Trademark symbol added Information regarding M24C64, SE97BTP, and DS1339U added Warning updated “Package temperature” replaced with “Case temperature” Case temperature DDR3L SDRAM changed to +95 °C
0103	20.03.2020	Petz	Tables 1.9, 8.2 Illustration 1, Illustration 2 3.1.2 Table 2 to Table 7, Table 18 Table 8 3.2.4.1 Table 26 3.2.4.18, Table 31 Table 35 6.5 Table 43	All reworked and updated Link to PTXdist documentation removed, Link to Yocto documentation added, all links updated Updated Chapters 3.1.2 to 3.1.5 merged Updated Added Table 15 removed Direction of “TXEN” signals corrected UART5 removed Completely reworked and updated MTBF added Updated
0104	25.03.2020	Petz	Table 2, Table 3, Table 4, Table 5 Table 36 4.6	Some signal directions and voltages corrected Column “Voltage” added Statements rephrased
0105	08.02.2021	Petz	All 2 3.2.4.11, 3.2.4.12 Table 39	Formatting, expression, non-functional changes MBa57xx revision 01xx ⇨ 02xx Note regarding PCIe clock added Information added

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa57xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa57xx circuit diagram
- MBa57xx User's Manual
- AM572x Data Sheet
- AM572x Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa57xx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of TQMa57xx revision 01xx in combination with the MBa57xx revision 02xx and refers to some software settings. The MBa57xx serves as an evaluation board for the TQMa57xx.

A certain TQMa57xx version does not necessarily provide all features described in this User's Manual. This User's Manual does also not replace the TI AM572x Reference Manual (6).

The AM57xx processor family is the successor of the AM335x processor family. The CPU derivatives provide single and dual ARM® Cortex®-A15 cores, which provide up to two C66x Floating-Point DSPs, up to two Dual ARM® Cortex®-M4 coprocessors, up to two Dual-Core Programmable Real-Time Unit and Industrial Communication Subsystems (PRU-ICSS).

In addition, they include up to two SGX544 (3D) graphics accelerators and a Vivante® GC320 (2D) core.

The TQMa57xx is a universal Minimodule based on these Texas Instruments ARM® Cortex®-A15 AM57xx CPUs, see also Table 7.

An AM57xx Cortex®-A15 core typically operates at 1.5 GHz.

2.1 Block diagrams AM57xx derivatives

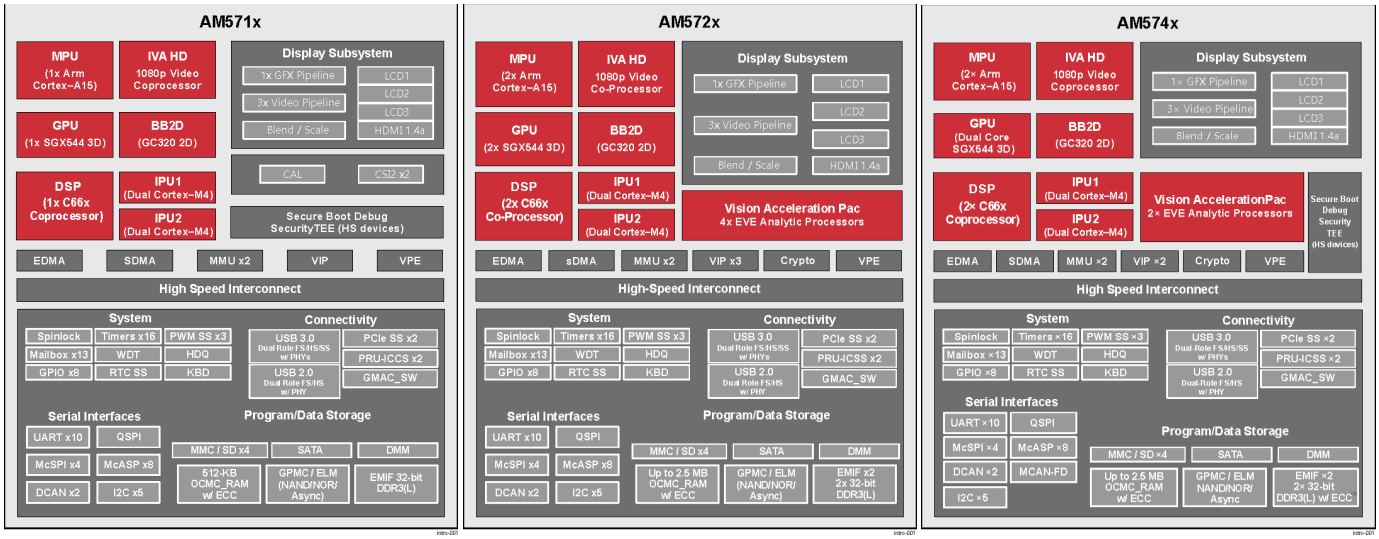


Figure 1: Block diagrams AM57xx CPUs
(Source: Texas Instruments)

The TQMa57xx extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable AM57xx derivative (AM571x, AM572x, or AM574x) can be selected matching the requirements.

All essential CPU signals are routed to the connectors. There are therefore no restrictions for customers using the TQMa57xx with respect to an integrated customised design. All essential components like CPU, DDR3L SDRAM, eMMC, and power management are already integrated on the TQMa57xx. The main features of the TQMa57xx are:

- Texas Instruments AM5718 / AM5728 / AM5748 CPU
- Up to 2 Gbyte DDR3L SDRAM, with 2 × 32 bit data bus interface
- Up to 32 Gbyte eMMC NAND flash
- Up to 256 Mbyte QSPI NOR flash
- 64 kbit EEPROM (M24C64)
- EEPROM + temperature sensor (SE97BTP)
- Texas Instruments Power Management Integrated Circuit (TPS6590379ZWS)
- All essential CPU signals are routed to the TQMa57xx connectors
- Extended temperature range
- Boot mode selection on TQMa57xx
- 5 V single supply voltage

2.2 Key functions and characteristics

The following components are implemented on the TQMa57xx:

- Texas Instruments AM571x / AM572x / AM574x CPU
- DDR3L SDRAM
- eMMC NAND flash
- QSPI NOR flash
- EEPROM (M24C64)
- Temperature sensor + EEPROM (SE97BTP)
- RTC (DS1339U-33)
- Supervisor with Reset structure
- Power supply by PMIC with Power Sequencing (single 5 V supply)
- Boot configuration
- Four connectors (2 × 120 pins, 2 × 80 pins)

The following primary interfaces are provided at the TQMa57xx connectors: [1]

- 2 × Ethernet 10/100 MII (PRU)
- 2 × GbE (Gigabit Ethernet)
- 2 × I^2C + 1 × I^2C for the devices on the TQMa57xx
- 1 × JTAG
- 1 × Parallel LCD RGB 24-bit interface
- 2 × DCAN (AM574x: 1 × DCAN and 1 × MCAN)
- 1 × SPI
- 1 × USB 2.0 OTG
- 1 × USB 3.0
- 86 × GPIO (AM5728)
- 4 × GPI-PRU (AM5728)
- 7 × GPO-PRU (AM5728)
- 4 × UART
- 1 × SD 4-bit (SDIO / MMC / SD card)
- 1 × QSPI (for additional SPI NOR flash; CS0 and CS1)
- 1 × HDMI (HDMI 1.4a and DVI 1.0 compliant)
- 1 × I^2S (MCASP)
- 1 × PCIe, 2 lanes (Gen2 compliant) (AM5718: only 1 lane)
- 1 × SATA Gen2

As an alternative to the standard configuration mentioned above, further interfaces of the AM57xx can also be used if the pin configuration is modified. These are, among others:

- Camera Sensor-Interfaces 8-bit (CSI – CMOS Sensor Interface) (AM571x)
- Video-In: Up to 2 × parallel LCD RGB 24-bit
- Synchronous Audio Interface (SAI – e.g., I^2S)
- PWM
- ADC
- GPMC
- More GPIOs
- More audio interfaces
- One more I^2C interface
- More SPI interfaces
- One more UART

1: Number of interfaces depend on AM57xx derivative.

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa57xx, and the BSP provided by TQ-Systems GmbH, see also chapter 5.

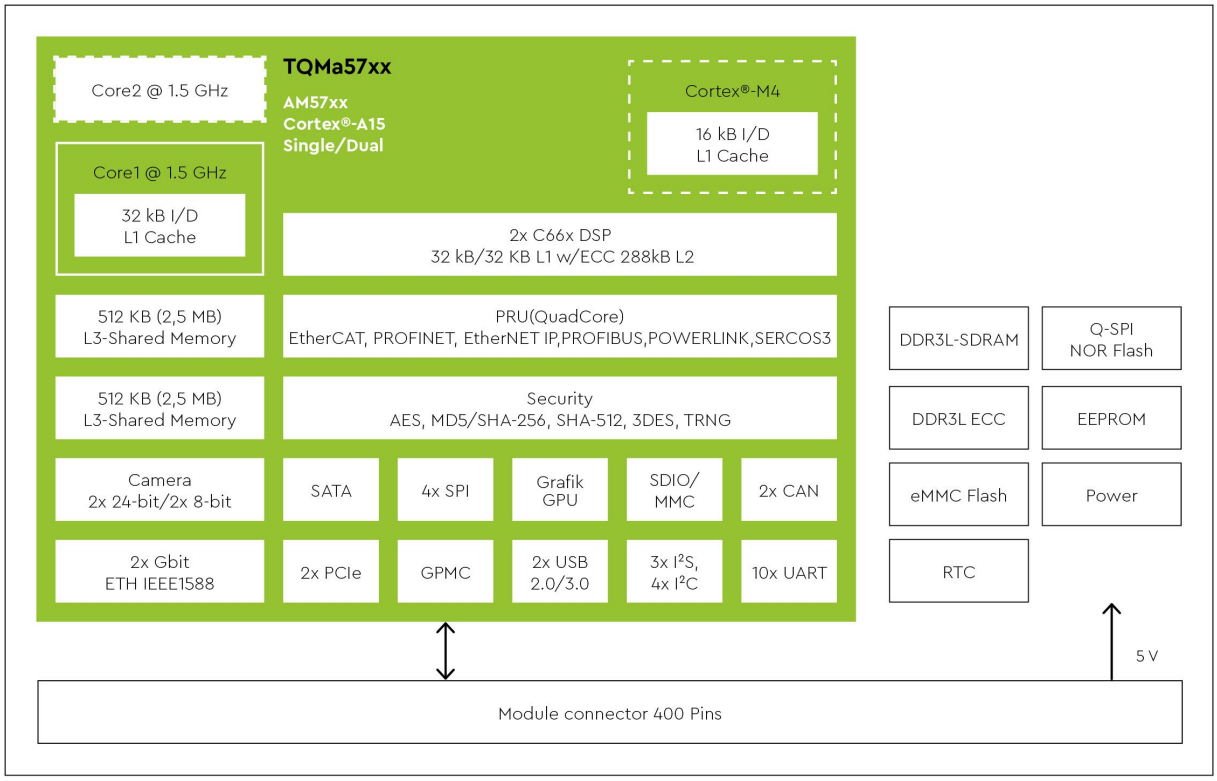


Figure 2: Block diagram TQMa57xx

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of. TI provides a tool showing the multiplexing and simplifies the selection and configuration (TI Pin Mux Tool):
https://processors.wiki.ti.com/index.php/TI_PinMux_Tool?keyMatch=pinmux&tisearch=Search-EN-Everything

The pin assignment listed in Table 2 to Table 5 refer to a TQMa5728 in combination with the MBa57xx and the BSP provided by TQ-Systems. The pin assignment differences between the AM57xx variants are shown in Table 6.

The electrical and pin characteristics are to be taken from the AM57xx Data Sheet (1), the AM57xx Reference Manual (6), and the PMIC Data Sheet (7).

Attention: Destruction or malfunction	
	Depending on the configuration, many AM57xx balls can provide several different functions. Please take note of the information concerning the configuration of these pins in the AM572x Reference Manual (6), and the AM572x Errata (2) before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa57xx.

3.1.2 Pinout TQMa57xx connectors

Table 2: Pinout connector X1

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
–	P	0 V	GND	DGND	1	2	DGND	GND	0 V	P	–
C9	O	1.8 V	LCD	VOUT1_D[20]	3	4	UART10_RTS#	UART	3.3 V	O	F4
A7	O	1.8 V	LCD	VOUT1_D[18]	5	6	UART10_RXD	UART	3.3 V	I	D1
B7	O	1.8 V	LCD	VOUT1_D[16]	7	8	UART10_TXD	UART	3.3 V	O	E2
C8	O	1.8 V	LCD	VOUT1_D[14]	9	10	DGND	GND	0 V	P	–
A5	O	1.8 V	LCD	VOUT1_D[12]	11	12	VOUT1_D[23]	LCD	1.8 V	O	A10
D7	O	1.8 V	LCD	VOUT1_D[10]	13	14	VOUT1_D[22]	LCD	1.8 V	O	B9
E8	O	1.8 V	LCD	VOUT1_D[8]	15	16	VOUT1_D[21]	LCD	1.8 V	O	A9
–	P	0 V	GND	DGND	17	18	VOUT1_D[19]	LCD	1.8 V	O	A8
F8	O	1.8 V	LCD	VOUT1_D[6]	19	20	VOUT1_D[17]	LCD	1.8 V	O	B8
G11	O	1.8 V	LCD	VOUT1_D[3]	21	22	VOUT1_D[15]	LCD	1.8 V	O	C7
F10	O	1.8 V	LCD	VOUT1_D[2]	23	24	VOUT1_D[13]	LCD	1.8 V	O	C6
G10	O	1.8 V	LCD	VOUT1_D[1]	25	26	DGND	GND	0 V	P	–
F11	O	1.8 V	LCD	VOUT1_D[0]	27	28	VOUT1_D[11]	LCD	1.8 V	O	D8
B11	I/O	1.8 V	GPIO	VOUT1_FLD (GPIO4_21)	29	30	VOUT1_D[9]	LCD	1.8 V	O	D9
B10	O	1.8 V	LCD	VOUT1_DE	31	32	VOUT1_D[7]	LCD	1.8 V	O	E7
–	P	0 V	GND	DGND	33	34	VOUT1_D[5]	LCD	1.8 V	O	F9
D11	O	1.8 V	LCD	VOUT1_CLK	35	36	VOUT1_D[4]	LCD	1.8 V	O	E9
–	I	3.3 V	Config	RST_FROM_MB#	37	38	VOUT1_VSYNC	LCD	1.8 V	O	E11
–	O	3.3 V	Config	RST_TO_MB#	39	40	VOUT1_HSYNC	LCD	1.8 V	O	C11
D20	I	3.3 V	JTAG	JTAG_TRSTN	41	42	DGND	GND	0 V	P	–
F18	I	3.3 V	JTAG	JTAG_TMS	43	44	GPIO4_0_G6	GPIO	3.3 V	I/O	G6
F19	O	3.3 V	JTAG	JTAG_TDO	45	46	GPIO4_1_F2 (PMIC_INT)	Config	3.3 V	I	F2
D23	I	3.3 V	JTAG	JTAG_TDI	47	48	GPIO4_2_F3 (TEMP_INT#)	Config	3.3 V	I	F3
–	P	0 V	GND	DGND	49	50	GPIO4_5_D2	GPIO	3.3 V	I/O	D2
E20	I	3.3 V	JTAG	JTAG_TCLK	51	52	GPIO5_1_J14	GPIO	3.3 V	I/O	J14
E18	O	3.3 V	JTAG	JTAG_RTCK	53	54	USB2.0_OTG_OC#	USB	3.3 V	I	G13
D24	I/O	3.3 V	JTAG	JTAG_EMU1	55	56	GPIO5_5_J11	GPIO	3.3 V	I/O	J11
G21	I/O	3.3 V	JTAG	JTAG_EMU0	57	58	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	59	60	MCASP8_ACLKX	AUDIO	3.3 V	I/O	B17
E12	I/O	3.3 V	GPIO	GPIO5_6_E12	61	62	MCASP8_FSX	AUDIO	3.3 V	I/O	A17
F13	I/O	3.3 V	GPIO	GPIO5_7_F13	63	64	MCASP8_AXR[0]	AUDIO	3.3 V	I/O	D15
C12	I/O	3.3 V	GPIO	GPIO5_8_C12	65	66	MCASP8_AXR[1]	AUDIO	3.3 V	I/O	B16
D12	I/O	3.3 V	GPIO	GPIO5_9_D12	67	68	MCASP8_AXR[2]	AUDIO	3.3 V	I/O	E15
–	P	0 V	GND	DGND	69	70	MCASP8_AXR[3]	AUDIO	3.3 V	I/O	A20
C18	I/O	3.3 V	AUDIO	MCASP4_C18	71	72	MCASP8_AHCLKX	AUDIO	3.3 V	O	C23
A15	I/O	3.3 V	AUDIO	MCASP2_A15	73	74	DGND	GND	0 V	P	–
F22	I	3.3 V	Config	AM57XX_PORZ#	75	76	DCAN1_RX	CAN	3.3 V	I	G19
F23	O	3.3 V	Config	RSTOUT#	77	78	DCAN1_TX	CAN	3.3 V	O	G20
E23	I	3.3 V	Config	RESET#	79	80	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	81	82	DCAN2_RX	CAN	3.3 V	I	F20
A22	O	3.3 V	SATA	SATA1_LED	83	84	DCAN2_TX	CAN	3.3 V	O	E21
B15	I/O	3.3 V	AUDIO	MCASP2_B15	85	86	DGND	GND	0 V	P	–
–	O	5 V	Config	PMIC_REGEN1	87	88	I2C4_SDA	I2C	3.3 V	I/O	B14
B20	I/O	3.3 V	HDMI	HDMI1_CEC	89	90	I2C4_SCL	I2C	3.3 V	O	A21
B21	I	3.3 V	HDMI	HDMI1_HPD	91	92	DGND	GND	0 V	P	–
F17	I/O	3.3 V	HDMI	HDMI1_DDC_SDA	93	94	I2C5_SDA	I2C	3.3 V	I/O	AA3
C25	O	3.3 V	HDMI	HDMI1_DDC_SCL	95	96	I2C5_SCL	I2C	3.3 V	O	AB9
–	P	0 V	GND	DGND	97	98	DGND	GND	0 V	P	–
G17	I/O	3.3 V	GPIO	GPIO7_16_G17	99	100	UART3_RXD	UART	3.3 V	I	A26
B24	I/O	3.3 V	GPIO	GPIO7_17_B24	101	102	UART3_TXD	UART	3.3 V	O	B22
D28	I/O	3.3 V	SDIO	MMC4_DAT[0]	103	104	DGND	GND	0 V	P	–
D26	I/O	3.3 V	SDIO	MMC4_DAT[1]	105	106	UART4_RXD	UART	3.3 V	I	G16
D27	I/O	3.3 V	SDIO	MMC4_DAT[2]	107	108	UART4_TXD	UART	3.3 V	O	D17
C28	I/O	3.3 V	SDIO	MMC4_DAT[3]	109	110	DGND	GND	0 V	P	–
C26	I	3.3 V	SDIO	MMC4_SDWP	111	112	UART8_RTS#	UART	3.3 V	O	AH6
–	P	0 V	GND	DGND	113	114	UART8_RXD	UART	3.3 V	I	AE8
E25	O	3.3 V	SDIO	MMC4_CLK	115	116	UART8_TXD	UART	3.3 V	O	AD8
C27	I/O	3.3 V	SDIO	MMC4_CMD	117	118	GPIO3_28_E1	GPIO	3.3 V	I/O	E1
B27	I	3.3 V	SDIO	MMC4_SDCD	119	120	DGND	GND	0 V	P	–

3.1.2 Pinout TQMa57xx connectors (continued)

Table 3: Pinout connector X2

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
–	P	5 V	Power	VDD5V	1	2	VDD5V	Power	5 V	P	–
–	P	5 V	Power	VDD5V	3	4	VDD5V	Power	5 V	P	–
–	P	5 V	Power	VDD5V	5	6	VDD5V	Power	5 V	P	–
–	P	5 V	Power	VDD5V	7	8	VDD5V	Power	5 V	P	–
–	P	0 V	GND	DGND	9	10	VDD5V	Power	5 V	P	–
–	P	0 V	GND	DGND	11	12	DGND	GND	0 V	P	–
–	P	3.3 V	BAT	V_BAT	13	14	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	15	16	DGND	GND	0 V	P	–
F6	I/O	3.3 V	ENET	PR1_MDIO_DATA / GMAC_MDIO_DATA	17	18	WAKEUP0	Config	3.3 V	I	AD17
D3	O	3.3 V	ENET	PR1_MDIO_MDCLK / GMAC_MDIO_MCLK	19	20	GPIO3_29_G2	GPIO	3.3 V	I/O	G2
–	P	0 V	GND	DGND	21	22	PR1_MII1_TXEN	ENET	3.3 V	O	E4
A4	I	3.3 V	ENET	PR1_MII1_CRS / RGMII1_RXD0	23	24	PR1_MII1_MT_CLK	ENET	3.3 V	I	C1
B5	I	3.3 V	ENET	PR1_MII1_COL / RGMII1_RXD1	25	26	DGND	GND	0 V	P	–
B4	I	3.3 V	ENET	PR1_MII1_RXLINK / RGMII1_RXD2	27	28	PR1_MII1_TXD1 / RGMII1_TXC	ENET	3.3 V	O	D5
B3	I	3.3 V	ENET	PR1_MII1_RXER / RGMII1_RXD3	29	30	PR1_MII1_TXD0 / RGMII1_TXCTL	ENET	3.3 V	O	C2
–	P	0 V	GND	DGND	31	32	PR1_MII1_TXD2	ENET	3.3 V	O	E6
D6	I/O	3.3 V	ENET	PR1_MII1_RXD2 / RGMII1_TXD0	33	34	PR1_MII1_TXD3	ENET	3.3 V	O	F5
B2	I/O	3.3 V	ENET	PR1_MII1_RXD3 / RGMII1_TXD1	35	36	PR1_MII1_RXD0 / RGMII1_RXCTL	ENET	3.3 V	I	A3
C4	I/O	3.3 V	ENET	PR1_MII1_RXDV / RGMII1_TXD2	37	38	PR1_MII1_RXD1 / RGMII1_RXC	ENET	3.3 V	I	C5
C3	I/O	3.3 V	ENET	PR1_MII1_MR_CLK / RGMII1_TXD3	39	40	DGND	GND	0 V	P	–
–	I	5 V	USB	VUSB_VBUS2	41	42	GPIO3_30_H7	GPIO	3.3 V	I/O	H7
–	I	5 V	Config	PMIC_PWRON#	43	44	PR2_MDIO_DATA	ENET	3.3 V	I/O	D14
K14	I	1.8 V	Config	E–FUSE_1V8	45	46	PR2_MDIO_MDCLK	ENET	3.3 V	O	C14
–	P	0 V	GND	DGND	47	48	DGND	GND	0 V	P	–
A13	I	3.3 V	ENET	PR2_MII0_MR_CLK	49	50	PR2_MII0_MT_CLK	ENET	3.3 V	I	F12
G12	I	3.3 V	ENET	PR2_MII0_RXER	51	52	PR2_MII0_TXEN	ENET	3.3 V	O	B12
C15	I	3.3 V	ENET	PR2_MII0_RXD[0]	53	54	PR2_MII0_TXD[0]	ENET	3.3 V	O	E14
A18	I	3.3 V	ENET	PR2_MII0_RXD[1]	55	56	DGND	GND	0 V	P	–
A19	I	3.3 V	ENET	PR2_MII0_RXD[2]	57	58	PR2_MII0_TXD[1]	ENET	3.3 V	O	A12
F14	I	3.3 V	ENET	PR2_MII0_RXD[3]	59	60	PR2_MII0_TXD[2]	ENET	3.3 V	O	B13
–	P	0 V	GND	DGND	61	62	PR2_MII0_TXD[3]	ENET	3.3 V	O	A11
G14	I	3.3 V	ENET	PR2_MII0_RXDV	63	64	PR2_MII0_COL	ENET	3.3 V	I	F15
A16	I	3.3 V	ENET	PR2_MII0_RXLINK	65	66	PR2_MII0_CRS	ENET	3.3 V	I	B18
F21	I/O	3.3 V	GPIO	GPIO6_16_F21	67	68	DGND	GND	0 V	P	–
B26	I/O	3.3 V	GPIO	GPIO6_19_B26	69	70	PR2_MII1_RXLINK	ENET	3.3 V	I	C17
B25	I/O	3.3 V	SPI	SPI1_D0	71	72	PR2_MII1_CRS	ENET	3.3 V	I	E17
F16	I/O	3.3 V	SPI	SPI1_D1	73	74	PR2_MII1_COL	ENET	3.3 V	I	D18
–	P	0 V	GND	DGND	75	76	GPIO3_1_AF9	GPIO	3.3 V	I/O	AF9
A25	O	3.3 V	SPI	SPI1_SCLK	77	78	NMIN_DSP	Config	3.3 V	I	D21
A24	O	3.3 V	SPI	SPI1_CS0	79	80	DGND	GND	0 V	P	–

3.1.2 Pinout TQMa57xx connectors (continued)

Table 4: Pinout connector X3

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
N6	O	1.8 V	GPMC	GPMC_BE#[0] (GPIO2_26)	1	2	DGND	GND	0 V	P	–
M4	O	1.8 V	GPMC	GPMC_BE#[1] (GPIO2_27)	3	4	GPMC_CLK (GPIO2_22)	GPMC	1.8 V	O	P7
M6	I/O	1.8 V	Boot/GPMC	GPMC_AD[0] (GPIO1_6)	5	6	GPMC_CS0 (GPIO2_19)	GPMC	1.8 V	O	T1
M2	I/O	1.8 V	Boot/GPMC	GPMC_AD[1] (GPIO1_7)	7	8	GPMC_OE#_RE# (GPIO2_24)	GPMC	1.8 V	O	M5
–	P	0 V	GND	DGND	9	10	GPMC_WE# (GPIO2_25)	GPMC	1.8 V	O	M3
L5	I/O	1.8 V	Boot/GPMC	GPMC_AD[2] (GPIO1_8)	11	12	GPMC_ADV#_ALE (GPIO2_23)	GPMC	1.8 V	O	N1
M1	I/O	1.8 V	Boot/GPMC	GPMC_AD[3] (GPIO1_9)	13	14	GPMC_A[1] (GPIO7_4)	GPMC	1.8 V	O	T9
L6	I/O	1.8 V	Boot/GPMC	GPMC_AD[4] (GPIO1_10)	15	16	GPMC_A[2] (GPIO7_5)	GPMC	1.8 V	O	T6
L4	I/O	1.8 V	Boot/GPMC	GPMC_AD[5] (GPIO1_11)	17	18	DGND	GND	0 V	P	–
L3	I/O	1.8 V	Boot/GPMC	GPMC_AD[6] (GPIO1_12)	19	20	GPMC_A[3] (GPIO7_6)	GPMC	1.8 V	O	T7
L2	I/O	1.8 V	Boot/GPMC	GPMC_AD[7] (GPIO1_13)	21	22	GPMC_A[4] (GPIO1_26)	GPMC	1.8 V	O	P6
L1	I/O	1.8 V	Boot/GPMC	GPMC_AD[8] (GPIO7_18)	23	24	GPMC_A[5] (GPIO1_27)	GPMC	1.8 V	O	R9
–	P	0 V	GND	DGND	25	26	GPMC_A[6] (GPIO1_28)	GPMC	1.8 V	O	R5
K2	I/O	1.8 V	Boot/GPMC	GPMC_AD[9] (GPIO7_19)	27	28	GPMC_A[7] (GPIO1_29)	GPMC	1.8 V	O	P5
J1	I/O	1.8 V	Boot/GPMC	GPMC_AD[10] (GPIO7_28)	29	30	GPMC_A[8] (GPIO1_30)	GPMC	1.8 V	O	N7
J2	I/O	1.8 V	Boot/GPMC	GPMC_AD[11] (GPIO7_29)	31	32	GPMC_A[9] (GPIO1_31)	GPMC	1.8 V	O	R4
H1	I/O	1.8 V	Boot/GPMC	GPMC_AD[12] (GPIO1_18)	33	34	DGND	GND	0 V	P	–
J3	I/O	1.8 V	Boot/GPMC	GPMC_AD[13] (GPIO1_19)	35	36	GPMC_A[10] (GPIO2_0)	GPMC	1.8 V	O	N9
H2	I/O	1.8 V	Boot/GPMC	GPMC_AD[14] (GPIO1_20)	37	38	GPMC_A27_AF4 (GPIO3_19)	GPMC	3.3 V	O	AF4
H3	I/O	1.8 V	Boot/GPMC	GPMC_AD[15] (GPIO1_21)	39	40	GPMC_A27_G1 (GPIO3_31)	GPMC	3.3 V	O	G1
AD9	I/O	3.3 V	GPIO	GPIO3_0_AD9	41	42	DGND	GND	0 V	P	–
B19	I	3.3 V	ENET	PR2_MII1_RXER	43	44	PR1_MII0_MT_CLK / RGMII0_RXC	ENET	3.3 V	I	U5
–	P	0 V	GND	DGND	45	46	PR1_MII0_COL (GPIO5_15)	ENET	3.3 V	I	V1
Y1	I	3.3 V	ENET	PR1_MII0_MR_CLK (GPIO5_19)	47	48	PR1_MII0_TXD3 / RGMII0_RXCTL	ENET	3.3 V	I/O	V5
V2	I	3.3 V	ENET	PR1_MII0_RXDV (GPIO5_18)	49	50	DGND	GND	0 V	P	–
U7	I/O	3.3 V	ENET	PR1_MII0_RXER / RGMII0_TXD2	51	52	PR1_MII0_TXD0 / RGMII0_RXD0	ENET	3.3 V	I/O	W2
V7	I/O	3.3 V	ENET	PR1_MII0_CRS / RGMII0_TXD3	53	54	PR1_MII0_TXD1 / RGMII0_RXD1	ENET	3.3 V	I/O	Y2
U6	I/O	3.3 V	ENET	PR1_MII0_RXD0 / RGMII0_TXD0	55	56	PR1_MII0_TXD2 / RGMII0_RXD3	ENET	3.3 V	I/O	V4
V6	I/O	3.3 V	ENET	PR1_MII0_RXD1 / RGMII0_TXD1	57	58	PR1_MII0_TXEN / RGMII0_RXD2	ENET	3.3 V	I/O	V3
–	P	0 V	GND	DGND	59	60	DGND	GND	0 V	P	–
W9	I/O	3.3 V	ENET	PR1_MII0_RXD3 / RGMII0_TXC	61	62	PR2_MII1_RXD[0]	ENET	3.3 V	I	AB5
V9	I/O	3.3 V	ENET	PR1_MII0_RXD2 / RGMII0_TXCTL	63	64	PR2_MII1_RXD[1]	ENET	3.3 V	I	AB8
U4	I	3.3 V	ENET	PR1_MII0_RXLINK (GPIO5_16)	65	66	PR2_MII1_RXD[2]	ENET	3.3 V	I	AD6
–	P	0 V	GND	DGND	67	68	PR2_MII1_RXD[3]	ENET	3.3 V	I	AC8
U3	I/O	3.3 V	ENET	RMII_MHZ_50_CLK	69	70	PR2_MII1_TXEN	ENET	3.3 V	O	AB4
–	P	0 V	GND	DGND	71	72	PR2_MII1_TXD[0]	ENET	3.3 V	O	AC6
AC9	I	3.3 V	ENET	PR2_MII1_MR_CLK	73	74	PR2_MII1_TXD[1]	ENET	3.3 V	O	AC7
AC3	I	3.3 V	ENET	PR2_MII1_RXDV	75	76	PR2_MII1_TXD[2]	ENET	3.3 V	O	AC4
AC5	I	3.3 V	ENET	PR2_MII1_MT_CLK	77	78	PR2_MII1_TXD[3]	ENET	3.3 V	O	AD4
–	P	0 V	GND	DGND	79	80	DGND	GND	0 V	P	–

3.1.2 Pinout TQMa57xx connectors (continued)

Table 5: Pinout connector X4

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
–	P	0 V	GND	DGND	1	2	USB3.0_DRVVBUS	USB	3.3 V	O	AB10
AC12	I/O	3.3 V	USB	USB3.0_DM	3	4	DGND	GND	0 V	P	–
AD12	I/O	3.3 V	USB	USB3.0_DP	5	6	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	7	8	DGND	GND	0 V	P	–
AC11	O	1.8 V	USB	USB3.0_TXN0	9	10	USB3.0_RXP0	USB	1.8 V	I	AE12
AD11	O	1.8 V	USB	USB3.0_TXP0	11	12	USB3.0_RXN0	USB	1.8 V	I	AF12
–	P	0 V	GND	DGND	13	14	DGND	GND	0 V	P	–
AE11	I/O	3.3 V	USB	USB2.0_DP	15	16	USB2.0_DM	USB	3.3 V	I/O	AF11
AC16	I	3.3 V	USB	USB2.0_OTG_ID	17	18	USB2.0_DRVVBUS	USB	3.3 V	O	AC10
–	P	0 V	GND	DGND	19	20	DGND	GND	0 V	P	–
AH9	I	1.8 V	SATA	SATA1_RXN0	21	22	SATA1_TXN0	SATA	1.8 V	O	AG10
AG9	I	1.8 V	SATA	SATA1_RXP0	23	24	SATA1_TXP0	SATA	1.8 V	O	AH10
–	P	0 V	GND	DGND	25	26	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	27	28	PCIE_RXN1	PCIE	1.8 V	I	AG11
–	P	0 V	GND	DGND	29	30	PCIE_RXP1	PCIE	1.8 V	I	AH11
AG13	I	1.8 V	PCIE	PCIE_RXN0	31	32	DGND	GND	0 V	P	–
AH13	I	1.8 V	PCIE	PCIE_RXP0	33	34	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	35	36	PCIE_TXN1	PCIE	1.8 V	O	AG12
–	P	0 V	GND	DGND	37	38	PCIE_TXP1	PCIE	1.8 V	O	AH12
AG15	I	1.8 V	PCIE	PCIE_CLKP	39	40	DGND	GND	0 V	P	–
AH15	I	1.8 V	PCIE	PCIE_CLKN	41	42	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	43	44	PCIE_TXN0	PCIE	1.8 V	O	AG14
–	P	0 V	GND	DGND	45	46	PCIE_TXP0	PCIE	1.8 V	O	AH14
AG16	O	1.8 V	HDMI	HDMI1_CLOCKX	47	48	DGND	GND	0 V	P	–
AH16	O	1.8 V	HDMI	HDMI1_CLOCKY	49	50	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	51	52	DGND	GND	0 V	P	–
AG18	O	1.8 V	HDMI	HDMI1_DATA1X	53	54	HDMI1_DATA0X	HDMI	1.8 V	O	AG17
AH18	O	1.8 V	HDMI	HDMI1_DATA1Y	55	56	HDMI1_DATA0Y	HDMI	1.8 V	O	AH17
–	P	0 V	GND	DGND	57	58	DGND	GND	0 V	P	–
AH19	O	1.8 V	HDMI	HDMI1_DATA2Y	59	60	HDMI1_DATA2X	HDMI	1.8 V	O	AG19
–	P	0 V	GND	DGND	61	62	DGND	GND	0 V	P	–
R6	I/O	1.8 V	GPIO	GPIO7_3_R6	63	64	QSPI_SCK	QSPI	1.8 V	O	R2
Y9	I	3.3 V	SD	MMC1_SDWP	65	66	QSPI_RTCLK	QSPI	1.8 V	I	R3
–	P	0 V	GND	DGND	67	68	QSPI_SS1#	QSPI	1.8 V	O	P1
W6	O	3.3 V	SD	MMC1_CLK	69	70	DGND	GND	0 V	P	–
Y6	I/O	3.3 V	SD	MMC1_CMD	71	72	QSPI_DATA0	QSPI	1.8 V	I/O	U1
AA6	I/O	3.3 V	SD	MMC1_DAT[0]	73	74	QSPI_DATA1	QSPI	1.8 V	I/O	P3
Y4	I/O	3.3 V	SD	MMC1_DAT[1]	75	76	QSPI_DATA2	QSPI	1.8 V	I/O	U2
AA5	I/O	3.3 V	SD	MMC1_DAT[2]	77	78	QSPI_DATA3	QSPI	1.8 V	I/O	T2
Y3	I/O	3.3 V	SD	MMC1_DAT[3]	79	80	DGND	GND	0 V	P	–
W7	I	3.3 V	SD	MMC1_SDCD	81	82	QSPI_SS0#	QSPI	1.8 V	O	P2
–	P	0 V	GND	DGND	83	84	GPIO3_22_AE5	GPIO	3.3 V	I/O	AE5
AE9	I/O	3.3 V	GPIO	GPIO3_2_AE9	85	86	GPIO3_23_AE1	GPIO	3.3 V	I/O	AE1
AF8	I/O	3.3 V	GPIO	GPIO3_3_AF8	87	88	GPIO3_24_AE2	GPIO	3.3 V	I/O	AE2
–	P	0 V	GND	DGND	89	90	GPIO3_25_AE6	GPIO	3.3 V	I/O	AE6
AF6	I/O	3.3 V	GPIO	GPIO3_17_AF6	91	92	GPIO3_26_AD2	GPIO	3.3 V	I/O	AD2
AF3	I/O	3.3 V	GPIO	GPIO3_18_AF3	93	94	GPIO3_27_AD3	GPIO	3.3 V	I/O	AD3
AF1	I/O	3.3 V	GPIO	GPIO3_20_AF1	95	96	PR1_PRU0_GPO5_AG4	ENET	3.3 V	O	AG4
AE3	I/O	3.3 V	GPIO	GPIO3_21_AE3	97	98	DGND	GND	0 V	P	–
AG7	I/O	3.3 V	GPIO	GPIO3_6_AG7	99	100	PR1_PRU0_GPO6_AG2	ENET	3.3 V	O	AG2
AH3	I	3.3 V	ENET	PR1_PRU0_GPI1_AH3	101	102	PR1_PRU0_GPO7_AG3	ENET	3.3 V	O	AG3
AH5	I	3.3 V	ENET	PR1_PRU0_GPI2_AH5	103	104	PR1_PRU0_GPO8_AG5	ENET	3.3 V	O	AG5
–	P	0 V	GND	DGND	105	106	PR1_PRU0_GPO9_AF2	ENET	3.3 V	O	AF2
AG6	I	3.3 V	ENET	PR1_PRU0_GPI3_AG6	107	108	GPIO2_28_N2	GPIO	1.8 V	I/O	N2
AH4	I	3.3 V	ENET	PR1_PRU0_GPI4_AH4	109	110	GPIO2_30_AG8	GPIO	3.3 V	I/O	AG8
AC17	I/O	3.3 V	GPIO	GPIO1_1_AC17	111	112	GPIO2_31_AH7	GPIO	3.3 V	I/O	AH7
AB16	I/O	3.3 V	GPIO	GPIO1_2_AB16	113	114	DGND	GND	0 V	P	–
P9	I/O	1.8 V	GPIO	GPIO2_1_P9	115	116	MCASP5_AA4 (PR2_PRU1_GPO4)	AUDIO	3.3 V	I/O	AA4
P4	I/O	1.8 V	GPIO	GPIO2_2_P4	117	118	MCASP5_AB3 (PR2_PRU1_GPO3)	AUDIO	3.3 V	I/O	AB3
–	P	0 V	GND	DGND	119	120	DGND	GND	0 V	P	–

3.1.3 TQMa57xx pinout differences

Table 6: TQMa57xx pinout differences

CPU ball	TQMa57xx	Signal	TQMa571x	TQMa572x	TQMa574x
AC17	X4-111	GPIO1_1_AC17	(N/A)	GPIO1_1	GPIO1_1
AB16	X4-113	GPIO1_2_AB16	(N/A)	GPIO1_2	GPIO1_2
AG8	X4-110	GPIO2_30_AG8	(N/A)	GPIO2_30	GPIO2_30
AH7	X4-112	GPIO2_31_AH7	CSI2_1_DX2	GPIO2_31	GPIO2_31
AD9	X3-41	GPIO3_0_AD9	(N/A)	GPIO3_0	GPIO3_0
AF9	X2-76	GPIO3_1_AF9	(N/A)	GPIO3_1	GPIO3_1
AF6	X4-91	GPIO3_17_AF6	(N/A)	GPIO3_17	GPIO3_17
AF3	X4-93	GPIO3_18_AF3	CSI2_0_DY2	GPIO3_18	GPIO3_18
AE9	X4-85	GPIO3_2_AE9	(N/A)	GPIO3_2	GPIO3_2
AF1	X4-95	GPIO3_20_AF1	CSI2_0_DX1	GPIO3_20	GPIO3_20
AE3	X4-97	GPIO3_21_AE3	(N/A)	GPIO3_21	GPIO3_21
AE5	X4-84	GPIO3_22_AE5	(N/A)	GPIO3_22	GPIO3_22
AE1	X4-86	GPIO3_23_AE1	CSI2_0_DX0	GPIO3_23	GPIO3_23
AE2	X4-88	GPIO3_24_AE2	CSI2_0_DY1	GPIO3_24	GPIO3_24
AE6	X4-90	GPIO3_25_AE6	(N/A)	GPIO3_25	GPIO3_25
AD2	X4-92	GPIO3_26_AD2	CSI2_0_DY0	GPIO3_26	GPIO3_26
AD3	X4-94	GPIO3_27_AD3	(N/A)	GPIO3_27	GPIO3_27
AF8	X4-87	GPIO3_3_AF8	(N/A)	GPIO3_3	GPIO3_3
AG7	X4-99	GPIO3_6_AG7	CSI2_1_DY2	GPIO3_6	GPIO3_6
AF4	X3-38	GPMC_A27_AF4	(N/A)	GPIO3_19	GPIO3_19
AG11	X4-28	PCIE_RXN1	(N/A)	PCIE_RXN1	PCIE_RXN1
AH11	X4-30	PCIE_RXP1	(N/A)	PCIE_RXP1	PCIE_RXP1
AG12	X4-36	PCIE_TXN1	(N/A)	PCIE_TXN1	PCIE_TXN1
AH12	X4-38	PCIE_TXP1	(N/A)	PCIE_TXP1	PCIE_TXP1
AH3	X4-101	PR1_PRU0_GPI1_AH3	CSI2_0_DX4	PR1_PRU0_GPI1	PR1_PRU0_GPI1
AH5	X4-103	PR1_PRU0_GPI2_AH5	CSI2_1_DY0	PR1_PRU0_GPI2	PR1_PRU0_GPI2
AG6	X4-107	PR1_PRU0_GPI3_AG6	CSI2_1_DX1	PR1_PRU0_GPI3	PR1_PRU0_GPI3
AH4	X4-109	PR1_PRU0_GPI4_AH4	CSI2_0_DX3	PR1_PRU0_GPI4	PR1_PRU0_GPI4
AG4	X4-96	PR1_PRU0_GPO5_AG4	CSI2_0_DY3	PR1_PRU0_GPO5	PR1_PRU0_GPO5
AG2	X4-100	PR1_PRU0_GPO6_AG2	(N/A)	PR1_PRU0_GPO6	PR1_PRU0_GPO6
AG3	X4-102	PR1_PRU0_GPO7_AG3	CSI2_0_DY4	PR1_PRU0_GPO7	PR1_PRU0_GPO7
AG5	X4-104	PR1_PRU0_GPO8_AG5	CSI2_1_DX0	PR1_PRU0_GPO8	PR1_PRU0_GPO8
AF2	X4-106	PR1_PRU0_GPO9_AF2	CSI2_0_DX2	PR1_PRU0_GPO9	PR1_PRU0_GPO9
AH6	X1-112	UART8_RTS#	CSI2_1_DY1	UART8_RTS#	UART8_RTS#
AE8	X1-114	UART8_RXD	(N/A)	UART8_RXD	UART8_RXD
AD8	X1-116	UART8_TXD	(N/A)	UART8_TXD	UART8_TXD

3.2 System components

3.2.1 AM57xx CPU

3.2.1.1 AM57xx derivatives

Depending on the TQMa57xx version, one of the following AM57xx derivatives is assembled.

Table 7: AM57xx derivatives

Derivative	Cortex®-A15	Cortex®-M4	C66x DSP	CPU clock	DDR interface	Temperature range
AM5718	1	2	1	1.5 GHz	1 × 32 bit	–40 °C to +105 °C
AM5728	2	2	2	1.5 GHz	2 × 32 bit	–40 °C to +105 °C
AM5748	2	2	2	1.5 GHz	2 × 32 bit, one with ECC	–40 °C to +105 °C

Other AM57xx derivatives are available on request.

3.2.1.2 AM57xx errata

Attention: AM57xx malfunction	
	Please take note of the current AM57xx errata (2).

3.2.1.3 Boot modes

The AM57xx has an on-chip boot ROM with integrated bootloader.
After start-up, the boot code initializes the hardware and then loads the program image from the selected boot device.
The default boot device can be e.g. the eMMC or the QSPI NOR flash on the TQMa57xx.
Additional boot interfaces are available as an alternative to booting from the integrated eMMC or the QSPI NOR flash.
When designing a mainboard, it is recommended to include a redundant update concept for field software updates.
More information about boot interfaces and its configuration is to be taken from the AM57xx Data Sheet (1) and the AM57xx Reference Manual (6).

Table 8: SYSBOOT pins, Boot Mode configuration, compact

SYSBOOT	TQMa57xx	eMMC	SD card	QSPI NOR	AM57xx derivative
SYSBOOT_15	X3-39	0	0	0	TQMa571x
		1	1	1	TQMa572x & TQMa574x
SYSBOOT_14	X3-37	0	0	0	–
SYSBOOT_13	X3-35	0	0	0	–
SYSBOOT_12	X3-33	0	0	0	–
SYSBOOT_11	X3-31	0	0	0	–
SYSBOOT_10	X3-29	0	0	0	–
SYSBOOT_9	X3-27	0	0	0	–
SYSBOOT_8	X3-23	1	1	1	–
SYSBOOT_7	X3-21	0	0	0	–
SYSBOOT_6	X3-19	0	0	0	–
SYSBOOT_5	X3-17	1	1	1	–
SYSBOOT_4	X3-15	0	1	1	–
SYSBOOT_3	X3-13	0	0	0	–
SYSBOOT_2	X3-11	0	0	1	–
SYSBOOT_1	X3-7	0	0	1	–
SYSBOOT_0	X3-5	0	0	0	–

3.2.1.4 Boot configuration

The configuration of boot pins SYSBOOT[15:0] with their default values on the TQMa57xx can be found in the following table. SYSBOOT[15:0] signals are configured with 100 kΩ resistors on the TQMa57xx, and can be overwritten with 10 kΩ resistors on the carrier board.

Table 9: SYSBOOT pins, Boot Mode configuration, detailed

SYSBOOT	Default	Function	Configuration	Signal	Pin
SYSBOOT_15	1	Pull-up resistor configuration	0b0 = internal pull-ups configurable per SW 0b1 = internal pull-ups permanently disabled	GPMC_AD15	X3-39
SYSBOOT_14	0	Bit reserved	Must be "0"	GPMC_AD14	X3-37
SYSBOOT_13	1	GPMC configuration for XIP / NAND	0b0 = 8-bit bus 0b1 = 16-bit bus	GPMC_AD13	X3-35
SYSBOOT_12	0		0b00 = non-multiplexed device 0b01 = Address/data-multiplexed device	GPMC_AD12	X3-33
SYSBOOT_11	1			GPMC_AD11	X3-31
SYSBOOT_10	0		0b0 = Wait-pin monitor disabled 0b1 = Wait-pin monitor enabled	GPMC_AD10	X3-29
SYSBOOT_9	0	SYS_CLK1 configuration	0b00 = reserved 0b01 = 20 MHz 0b10 = 27 MHz 0b11 = 19.2 MHz	GPMC_AD9	X3-27
SYSBOOT_8	1			GPMC_AD8	X3-23
SYSBOOT_7	0	Sector offset for redundant SBL image	0b00 = 64 KiB offset 0b01 = 128 KiB offset 0b10 = 256 KiB offset 0b11 = 512 KiB offset	GPMC_AD7	X3-21
SYSBOOT_6	0			GPMC_AD6	X3-19
SYSBOOT_5	1	Booting scenario	0b00 = Peripheral preferred booting 0b01 = Recovery / development booting 0b10 = Memory preferred booting 0b11 = Production booting	GPMC_AD5	X3-17
SYSBOOT_4	1			GPMC_AD4	X3-15
SYSBOOT_3	0	Boot source or boot device order	0b0000 = USB (at booting scenario = 0b01) 0b0110 = QSPI (at booting scenario = 0b11) 0b0111 = QSPI (at booting scenario = 0b11) For more information see AM572x Reference Manual (6)	GPMC_AD3	X3-13
SYSBOOT_2	1			GPMC_AD2	X3-11
SYSBOOT_1	1			GPMC_AD1	X3-7
SYSBOOT_0	0			GPMC_AD0	X3-5

Attention: AM57xx Boot Configuration	
	QSPI_1 (QSPI NOR-Flash) is preset as boot device on the TQMa57xx at delivery. This can be overwritten by the carrier board.

3.2.2 Memory

3.2.2.1 DDR3L SDRAM

Depending on the version, two to five 16-bit wide DDR3L memory chips are used on the TQMa57xx.
The number of EMIF controllers and the maximum possible transmission speed can be found in (1).
The 32-bit wide EMIFs are then split into two memory interfaces.
The features of the memory interface are shown in the following table:

Table 10: AM57xx SDRAM interface

AM57xx derivative	Bus width	Frequency	EMIF controller	ECC on EMIF1	No. of SDRAM chips	TQ-BSP
AM5718	32	1333 MHz	1	No	2	Yes
AM5728	32	1066 MHz	2	No	4	Yes
AM5748	32	1333 MHz	2	Yes	5	Yes

3.2.2.2 eMMC NAND flash

An eMMC NAND flash is assembled on the TQMa57xx. The eMMC is connected to MMC2 (eMMC Standard v4.5 compliant).
The following modes are supported:

- Standard JC64 SDR, 8-bit data, half cycle
- High-Speed JC64 SDR, 8-bit data, half cycle
- High-Speed JC64 DDR, 8-bit data
- High-Speed HS200 JC64 SDR, 8-bit data, half cycle

3.2.2.3 QSPI NOR flash

A QSPI-NOR flash is also available as non-volatile memory. This can be used as boot device or e.g. as recovery device.
The QSPI interface is also available on the TQMa57xx connectors with an additional CS.
The QSPI NOR chip select is also routed to the TQMa57xx connectors and can be used, if no QSPI-NOR flash is assembled.

Attention: QSPI NOR flash	
	The signals can only be used on a carrier board if the QSPI NOR flash is not assembled. During a soft reset or wakeup it may happen that the CPU controller and QSPI NOR Flash are in different QSPI modes. This condition can only be cleared by a reset.

3.2.2.4 EEPROM

A serial EEPROM, controlled by the I2C1 bus, is assembled. Write-Control (WC#) is not supported.
To store data read-only, the EEPROM with temperature sensor must be used, see 3.2.2.5.
The following table shows details of the EEPROM.

Table 11: EEPROM

Manufacturer	Part number	Size	Temperature range
STM	M24C64-RDW6	64 Kbit	–45 °C to +85 °C

➢ The device provides the following I²C addresses:
  - Memory: `0x54 / 101 0100b`
  - ID page: `0x5C / 101 1100b`

3.2.2.5 EEPROM with temperature sensor

A serial EEPROM including temperature sensor, controlled by the I2C1 bus, is assembled.
The lower 128 bytes (addresses 00h to 7Fh) can be set to Permanent Write Protected (PWP) mode or Reversible Write Protected (RWP) mode by software.
The upper 128 bytes (addresses 80h to FFh) cannot be write-protected and can be used for general data storage.
The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa57xx.
The following table shows details of the Manufacturer EEPROM.

Table 12: Manufacturer EEPROM

Manufacturer	Part number	Size	Temperature range
NXP	SE97BTP	2 × 128 bytes	–45 °C to +85 °C

- The device provides the following I²C addresses:
  - EEPROM (Normal Mode): `0x57 / 101 0111b`
  - EEPROM (Protection Mode): `0x37 / 011 0111b`
  - Temperature sensor: `0x1F / 001 1111b`

3.2.3 RTCSS

The TQMa57xx provides a discrete DS1339U-33 RTC, which can wake up the CPU via the dedicated wakeup pin Wakeup0.
The accuracy of the RTC is essentially determined by the characteristics of the quartz used.
The type CM7V-T1A used on the TQMa57xx has a standard frequency tolerance of ±20 ppm at +25 °C.
The RTC is connected via the I2C1 bus. The RTC power domain is supplied by VDD3V3. The RTC can be buffered via V_BAT on the pin header. If the RTC backup battery is to be charged, a suitable circuit must be provided on the carrier board.

- The RTC has I²C address `0x68 / 110 1000b`

Note: RTC long-term bridging	
	For long-term bridging, the use of the I²C-RTC in combination with a Li-Coin-Cell is recommended. The RTC can wake up the CPU via the Wakeup0 signal. For long-term bridging, the charging circuitry must be implemented on the carrier board.

3.2.4 Interfaces

The TQMa57xx provides interfaces with primary functions. They can all be used simultaneously independent of their configuration. Some primary functions are not available if a secondary function is used.
In this User's Manual only the external interfaces with primary function are described.

Table 13: TQMa57xx internal interfaces

Interface	Qty.	Function	Chapter	Remark
EMIF1/2	1	Primary	3.2.2.1	DDR3L SDRAM, 32 bit
MMC2	1	Primary	3.2.2.2	eMMC 8 bit
QSPI	1	Primary	3.2.2.3	QSPI NOR flash, 4 bit
I2C1	1	Primary	–	Exclusively used on TQMa57xx. EEPROM, EEPROM with Temp. sensor, RTC, PMIC

3.2.4 Interfaces (continued)

Table 14: External interfaces

Interface	Qty.	Function	Chapter	Remark
CHIPGLUE	1	Secondary	–	Multiplexing has to be adapted
CSI2	1	Primary	3.2.4.1	CSI2_0 and CSI2_1 only with TQMA571x
DCAN	2	Primary	3.2.4.2	DCAN1, DCAN2. TQMa574x with 1 × MCAN.
DEBUGSS	1	Primary	3.2.4.3	JTAG
eCAP	3	Secondary	–	Multiplexing has to be adapted
eHRPWM	3	Secondary	–	Multiplexing has to be adapted
eQEP	3	Secondary	–	Multiplexing has to be adapted
GMAC_MDIO	1	Primary	3.2.4.4	Gbit Ethernet
GMAC_SW	2	Primary	3.2.4.4	Gbit Ethernet 1, Gbit Ethernet 2
GPIO	7	Primary	3.2.4.5	Selection from groups GPIO1_x to GPIO7_x
GPIO	8	Secondary	–	Multiplexing has to be adapted
GPMC	1	Secondary	–	Multiplexing has to be adapted, Video Out 3
HDMI	1	Primary	3.2.4.6	HDMI1
HDQ	1	Secondary	–	Multiplexing has to be adapted
I^2C	2	Primary	3.2.4.7	I2C4, I2C5
I^2C	2	Secondary	–	Multiplexing has to be adapted
INTC	1	Primary	3.2.4.8	NMIN_DSP
KBD	1	Secondary	–	Multiplexing has to be adapted
MCASP	1	Primary	3.2.4.9	MCASP8 = Audio
MMC	2	Primary	3.2.4.10	MMC1 = SD card, MMC4 = SDIO
MMC	1	Secondary	–	Multiplexing has to be adapted
PCIE	2	Primary	3.2.4.11	PCIe (Lane 0), Mini-PCIe (Lane 1). TQMa571x only 1 × Lane.
PRCM	1	Primary	3.2.5	Reset signals
PRUSS1_eCAP	1	Secondary	–	Multiplexing has to be adapted
PRUSS1_ECAT	1	Secondary	–	Multiplexing has to be adapted
PRUSS1_MDIO	1	Secondary	–	Multiplexing has to be adapted
PRUSS1_MII	2	Secondary	–	Multiplexing has to be adapted
PRUSS1_PRU	1	Primary	3.2.4.13	Selection from groups GPIx and GPOx
PRUSS1_PRU	1	Secondary	–	Multiplexing has to be adapted
PRUSS1_UART	1	Secondary	–	Multiplexing has to be adapted
PRUSS2_eCAP	1	Secondary	–	Multiplexing has to be adapted
PRUSS2_ECAT	1	Secondary	–	Multiplexing has to be adapted
PRUSS2_MDIO	1	Primary	3.2.4.13	10/100 Mbit Ethernet
PRUSS2_MII	2	Primary	3.2.4.13	10/100 Mbit Ethernet
PRUSS2_PRU	1	Primary	3.2.4.13	Selection from groups GPIx and GPOx
PRUSS2_PRU	1	Secondary	–	Multiplexing has to be adapted
PRUSS2_UART	1	Secondary	–	Multiplexing has to be adapted
QSPI	1	Primary	3.2.2.3	QSPI
RTCSS	1	Primary	3.2.3	Wakeup0, On_Off
SATA	1	Primary	3.2.4.16	SATA M.2 Key-B
SDMA	1	Secondary	–	Multiplexing has to be adapted
SPI	1	Primary	3.2.4.17	SPI1
SPI	3	Secondary	–	Multiplexing has to be adapted
TIMER	16	Secondary	–	Multiplexing has to be adapted
UART	4	Primary	3.2.4.18	UART3 (RS-232), UART4, UART8 (TQMa572x and TQMa574x) UART10 (RS-485)
UART	6	Secondary	–	Multiplexing has to be adapted
USB	2	Primary	3.2.4.19	USB3.0, USB2.0 OTG
VIN	10	Secondary	–	Multiplexing has to be adapted
VOUT	1	Primary	3.2.4.20	VOUT1 (= Video Out 1)
VOUT	2	Secondary	–	Multiplexing has to be adapted

3.2.4.1 CSI2 – Camera Serial Interface

The TQMa571x provides two Camera Serial Interfaces.
All pins of interface CSI2_0 are available; with CSI2_1 only two data lines are available.
For variants TQMa572x and TQMa574x these pins are configured as GPIOs.

3.2.4.2 DCAN – Dual CAN

The TQMa57xx provides two integrated CAN 2.0B controllers. Both CAN signal pairs are routed to the TQMa57xx connectors.
With the TQMa574x, CAN1 controller is MCAN (CAN-FD) capable.
The CAN drivers must be provided on the carrier board.
The following table shows the CAN interface signals.

Table 15: DCAN signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
DCAN1_RX	I	G19	X1-76	3.3 V
DCAN1_TX	O	G20	X1-78	
DCAN2_RX	I	F20	X1-82	
DCAN2_TX	O	E21	X1-84	

3.2.4.3 DEBUGSS – JTAG

The TQMa57xx provides a full JTAG interface, which is routed to the TQMa57xx connectors.
The following table shows the JTAG signals.

Table 16: JTAG signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
JTAG_EMU0	I/O	G21	X1-57	3.3 V
JTAG_EMU1	I/O	D24	X1-55	
JTAG_RTCK	O	E18	X1-53	
JTAG_TCLK	I	E20	X1-51	
JTAG_TDI	I	D23	X1-47	
JTAG_TDO	O	F19	X1-45	
JTAG_TMS	I	F18	X1-43	
JTAG_TRSTN	I	D20	X1-41	

3.2.4.4 GMAC – Gbit Ethernet

The TQMa57xx provides a 2-channel Gigabit Ethernet, which supports RGMII. With an adapted pin multiplexing an MII or an RMII interface is also possible. The signals for RGMII are available as primary function on the TQMa57xx connectors.
The following table shows the RGMII interface signals.

Table 17: RGMII signals

Signal	Dir.	CPU ball	TQMa57xx	Power-Group
PR1_MDIO_DATA / GMAC_MDIO_DATA	I/O	F6	X2-17	3V3
PR1_MDIO_MDCLK / GMAC_MDIO_MCLK	O	D3	X2-19	
PR1_MII0_COL (GPIO5_15)	I	V1	X3-46	3.3 V
PR1_MII0_CRS / RGMII0_TXD3	I/O	V7	X3-53	
PR1_MII0_MR_CLK (GPIO5_19)	I	Y1	X3-47	
PR1_MII0_MT_CLK / RGMII0_RXC	I	U5	X3-44	
PR1_MII0_RXD0 / RGMII0_TXD0	I/O	U6	X3-55	
PR1_MII0_RXD1 / RGMII0_TXD1	I/O	V6	X3-57	
PR1_MII0_RXD2 / RGMII0_TXCTL	I/O	V9	X3-63	
PR1_MII0_RXD3 / RGMII0_TXC	I/O	W9	X3-61	
PR1_MII0_RXDV (GPIO5_18)	I	V2	X3-49	
PR1_MII0_RXER / RGMII0_TXD2	I/O	U7	X3-51	
PR1_MII0_RXLINK (GPIO5_16)	I	U4	X3-65	
PR1_MII0_TXD0 / RGMII0_RXD0	I/O	W2	X3-52	
PR1_MII0_TXD1 / RGMII0_RXD1	I/O	Y2	X3-54	
PR1_MII0_TXD2 / RGMII0_RXD3	I/O	V4	X3-56	
PR1_MII0_TXD3 / RGMII0_RXCTL	I/O	V5	X3-48	
PR1_MII0_TXEN / RGMII0_RXD2	I/O	V3	X3-58	
PR1_MII1_COL / RGMII1_RXD1	I	B5	X2-25	3.3 V
PR1_MII1_CRS / RGMII1_RXD0	I	A4	X2-23	
PR1_MII1_MR_CLK / RGMII1_TXD3	I/O	C3	X2-39	
PR1_MII1_MT_CLK	I	C1	X2-24	
PR1_MII1_RXD0 / RGMII1_RXCTL	I	A3	X2-36	
PR1_MII1_RXD1 / RGMII1_RXC	I	C5	X2-38	
PR1_MII1_RXD2 / RGMII1_TXD0	I/O	D6	X2-33	
PR1_MII1_RXD3 / RGMII1_TXD1	I/O	B2	X2-35	
PR1_MII1_RXDV / RGMII1_TXD2	I/O	C4	X2-37	
PR1_MII1_RXER / RGMII1_RXD3	I	B3	X2-29	
PR1_MII1_RXLINK / RGMII1_RXD2	I	B4	X2-27	
PR1_MII1_TXD0 / RGMII1_TXCTL	O	C2	X2-30	
PR1_MII1_TXD1 / RGMII1_TXC	O	D5	X2-28	
PR1_MII1_TXD2	O	E6	X2-32	
PR1_MII1_TXD3	O	F5	X2-34	
PR1_MII1_TXEN	O	E4	X2-22	

3.2.4.5 GPIO / PRUSS_PRU

Most AM57xx pins can also be used as GPIO in addition to their interface function. Many of these GPIO are interrupt-capable. Details can be found in the AM57xx Technical Reference Manual (6). In addition, various pins are already configured as GPIO and available on the TQMa57xx connectors. Attention: The pin multiplexing of the TQMa571x deviates.
The following table shows the usable GPIO signals of the TQMa572x.

Table 18: GPIOs, PRUSS_PRUs

Signal	CPU ball	TQMa57xx	Voltage
GPIO1_1	AC17	X4-111	3.3 V
GPIO1_2	AB16	X4-113	3.3 V
GPIO1_6	M6	X3-5	1.8 V (3.3 V)
GPIO1_7	M2	X3-7	1.8 V (3.3 V)
GPIO1_8	L5	X3-11	1.8 V (3.3 V)
GPIO1_9	M1	X3-13	1.8 V (3.3 V)
GPIO1_10	L6	X3-15	1.8 V (3.3 V)
GPIO1_11	L4	X3-17	1.8 V (3.3 V)
GPIO1_12	L3	X3-19	1.8 V (3.3 V)
GPIO1_13	L2	X3-21	1.8 V (3.3 V)
GPIO1_18	H1	X3-33	1.8 V (3.3 V)
GPIO1_19	J3	X3-35	1.8 V (3.3 V)
GPIO1_20	H2	X3-37	1.8 V (3.3 V)
GPIO1_21	H3	X3-39	1.8 V (3.3 V)
GPIO1_26	P6	X3-22	1.8 V (3.3 V)
GPIO1_27	R9	X3-24	1.8 V (3.3 V)
GPIO1_28	R5	X3-26	1.8 V (3.3 V)
GPIO1_29	P5	X3-28	1.8 V (3.3 V)
GPIO1_30	N7	X3-30	1.8 V (3.3 V)
GPIO1_31	R4	X3-32	1.8 V (3.3 V)
GPIO2_0	N9	X3-36	1.8 V (3.3 V)
GPIO2_1	P9	X4-115	1.8 V (3.3 V)
GPIO2_2	P4	X4-117	1.8 V (3.3 V)
GPIO2_19	T1	X3-6	1.8 V (3.3 V)
GPIO2_22	P7	X3-4	1.8 V (3.3 V)
GPIO2_23	N1	X3-12	1.8 V (3.3 V)
GPIO2_24	M5	X3-8	1.8 V (3.3 V)
GPIO2_25	M3	X3-10	1.8 V (3.3 V)
GPIO2_26	N6	X3-1	1.8 V (3.3 V)
GPIO2_27	M4	X3-3	1.8 V (3.3 V)
GPIO2_28	N2	X4-108	1.8 V (3.3 V)
GPIO2_30	AG8	X4-110	3.3 V
GPIO2_31	AH7	X4-112	3.3 V

Signal	CPU ball	TQMa57xx	Voltage
GPIO3_0	AD9	X3-41	3.3 V
GPIO3_1	AF9	X2-76	3.3 V
GPIO3_2	AE9	X4-85	3.3 V
GPIO3_3	AF8	X4-87	3.3 V
GPIO3_6	AG7	X4-99	3.3 V
GPIO3_17	AF6	X4-91	3.3 V
GPIO3_18	AF3	X4-93	3.3 V
GPIO3_19	AF4	X3-38	3.3 V
GPIO3_20	AF1	X4-95	3.3 V
GPIO3_21	AE3	X4-97	3.3 V
GPIO3_22	AE5	X4-84	3.3 V
GPIO3_23	AE1	X4-86	3.3 V
GPIO3_24	AE2	X4-88	3.3 V
GPIO3_25	AE6	X4-90	3.3 V
GPIO3_26	AD2	X4-92	3.3 V
GPIO3_27	AD3	X4-94	3.3 V
GPIO3_28	E1	X1-118	3.3 V
GPIO3_29	G2	X2-20	3.3 V
GPIO3_30	H7	X2-42	3.3 V
GPIO3_31	G1	X3-40	3.3 V
GPIO4_0	G6	X1-44	3.3 V
GPIO4_5	D2	X1-50	3.3 V
GPIO4_21	B11	X1-29	1.8 V
GPIO5_1	J14	X1-52	3.3 V
GPIO5_5	J11	X1-56	3.3 V
GPIO5_6	E12	X1-61	3.3 V
GPIO5_7	F13	X1-63	3.3 V
GPIO5_8	C12	X1-65	3.3 V
GPIO6_16	F21	X2-67	3.3 V
GPIO7_3	R6	X4-63	1.8 V
GPIO7_4	T9	X3-14	1.8 V (3.3 V)
GPIO7_5	T6	X3-16	1.8 V (3.3 V)
GPIO7_6	T7	X3-20	1.8 V (3.3 V)
GPIO7_16	G17	X1-99	3.3 V
GPIO7_17	B24	X1-101	3.3 V
GPIO7_18	L1	X3-23	1.8 V (3.3 V)
GPIO7_19	K2	X3-27	1.8 V (3.3 V)
GPIO7_28	J1	X3-29	1.8 V (3.3 V)
GPIO7_29	J2	X3-31	1.8 V (3.3 V)

3.2.4.6 HDMI – High Definition Multimedia Interface

The TQMa57xx provides an HDMI interface. The following table shows these signals.

Table 19: HDMI signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
HDMI1_CLOCKX	O	AG16	X4-47	1.8 V
HDMI1_CLOCKY	O	AH16	X4-49	
HDMI1_DATA0X	O	AG17	X4-54	
HDMI1_DATA0Y	O	AH17	X4-56	
HDMI1_DATA1X	O	AG18	X4-53	
HDMI1_DATA1Y	O	AH18	X4-55	
HDMI1_DATA2X	O	AG19	X4-60	
HDMI1_DATA2Y	O	AH19	X4-59	
HDMI1_DDC_SCL	O	C25	X1-95	3.3 V
HDMI1_DDC_SDA	I/O	F17	X1-93	
HDMI1_CEC	I/O	B20	X1-89	
HDMI1_HPD	I	B21	X1-91	

3.2.4.7 I²C

The TQMa57xx provides two I²C interfaces, which are available as primary functions on the TQMa57xx connectors.
Further I²C interfaces can be provided by adapted muxing.
The following table shows the I²C interface signals.

Table 20: I²C signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
I2C4_SCL	O	A21	X1-90	3.3 V
I2C4_SDA	I/O	B14	X1-88	
I2C5_SCL	O	AB9	X1-96	
I2C5_SDA	I/O	AA3	X1-94	

3.2.4.8 INTC – Interrupt Controller

Interrupt controller signal NMIN_DSP is routed to the TQMa57xx connector.

Table 21: INTC signal

Signal	Dir.	CPU ball	TQMa57xx	Voltage
NMIN_DSP	I	D21	X2-78	3.3 V

3.2.4.9 MCASP – Multichannel Audio Serial Port

The TQMa57xx has a full audio interface as primary function. The MCASP8 module is used as primary function.

Table 22: MCASP signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
MCASP8_ACLKX	I/O	B17	X1-60	3.3 V
MCASP8_AHCLKX	O	C23	X1-72	
MCASP8_FSX	I/O	A17	X1-62	
MCASP8_AXR[0]	I/O	D15	X1-64	
MCASP8_AXR[1]	I/O	B16	X1-66	
MCASP8_AXR[2]	(Not used)	E15	X1-68	
MCASP8_AXR[3]	(Not used)	A20	X1-70	

Signals marked as "Not used" are declared as GPIOs in the default pin multiplexing and cannot be used for the audio interface without software adaptation.

3.2.4.10 MMC – Multimedia Card

The TQMa57xx provides four MMC interfaces, of which MMC2 is used internally for the eMMC. MMC1 and MMC4 are routed to the TQMa57xx connectors and can be used as e.g., SD card or SDIO. See MBa57xx schematics for reference.
MMC3 is not a primary function, but can be used with an adapted pin multiplexing.

Table 23: MMC signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage	Mba57xx
MMC1_CLK	O	W6	X4-69	3.3 V	SD card
MMC1_CMD	I/O	Y6	X4-71		
MMC1_SDCD	I	W7	X4-81		
MMC1_SDWP	I	Y9	X4-65		
MMC1_DAT[0]	I/O	AA6	X4-73		
MMC1_DAT[1]	I/O	Y4	X4-75		
MMC1_DAT[2]	I/O	AA5	X4-77		
MMC1_DAT[3]	I/O	Y3	X4-79		
MMC4_CLK	O	E25	X1-115	3.3 V	SDIO
MMC4_CMD	I/O	C27	X1-117		
MMC4_SDCD	I	B27	X1-119		
MMC4_SDWP	I	C26	X1-111		
MMC4_DAT[0]	I/O	D28	X1-103		
MMC4_DAT[1]	I/O	D26	X1-105		
MMC4_DAT[2]	I/O	D27	X1-107		
MMC4_DAT[3]	I/O	C28	X1-109		

3.2.4.11 PCIe – Peripheral Component Interconnect Express

The TQMa57xx supports communication via PCIe. The default configuration supports two PCIe ports, with one lane each. TQMa572x and TQMa574x each support two lanes for PCIe (Lane 0) and Mini-PCIe (Lane 1). TQMa571x can only provide Lane 0 due to the reduced pin count. The PCIe bus operates at 1.8 V.

Table 24: PCIe signals

Signal	Dir.	CPU ball	TQMa57xx	Remark
PCIE_CLKP	I	AG15	X4-39	–
PCIE_CLKN	I	AH15	X4-41	
PCIE_RXP0	I	AH13	X4-33	Lane 0
PCIE_RXN0	I	AG13	X4-31	
PCIE_TXP0	O	AH14	X4-46	
PCIE_TXN0	O	AG14	X4-44	
PCIE_RXP1	I	AH11	X4-30	Lane 1
PCIE_RXN1	I	AG11	X4-28	
PCIE_TXP1	O	AH12	X4-38	
PCIE_TXN1	O	AG12	X4-36	

Note: PCIe clock	
	Since the PCIe clock provided by the AM57xx does not meet the PCIe specification, a dedicated clock generator is assembled on the MBa57xx. Further information can be found in the MBa57xx schematics.

3.2.4.12 PRCM – Power, Reset, and Clock Management

Some Reset and Clock signals are routed to the TQMa57xx connector.

Table 25: INTC signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
AM57xx_PORZ#	I	F22	X1-75	3.3 V
RSTOUT#	O	F23	X1-77	
RESET#	I	E23	X1-79	
RMII_MHz_50_CLK	I/O	U3	X3-69	

Note: PCIe clock	
	Since the PCIe clock provided by the AM57xx does not meet the PCIe specification, a dedicated clock generator is assembled on the MBa57xx. Further information can be found in the MBa57xx schematics.

3.2.4.13 PRUSS2_MDIO and _MII – 10/100 Mbit Ethernet

The TQMa57xx provides a two channel 10/100 Mbit Ethernet by the Programmable Real-time Unit, which supports MII.
Other functions are also possible with an adapted pin multiplexing; see TI's Technical Reference Manual (6).
The signals for MII are available as a primary function on the TQMa57xx connectors.
The following table shows the Ethernet interface signals.

Table 26: MII signals

Signal	Dir.	CPU ball	TQMa57xx	Power-Group
PR2_MDIO_DATA	I/O	D14	X2-44	3.3 V
PR2_MDIO_MDCLK	O	C14	X2-46	
PR2_MII0_COL	I	F15	X2-64	3.3 V
PR2_MII0_CRS	I	B18	X2-66	
PR2_MII0_MR_CLK	I	A13	X2-49	
PR2_MII0_MT_CLK	I	F12	X2-50	
PR2_MII0_RXDV	I	G14	X2-63	
PR2_MII0_RXER	I	G12	X2-51	
PR2_MII0_RXLINK	I	A16	X2-65	
PR2_MII0_TXEN	O	B12	X2-52	
PR2_MII0_RXD[0]	I	C15	X2-53	
PR2_MII0_RXD[1]	I	A18	X2-55	
PR2_MII0_RXD[2]	I	A19	X2-57	
PR2_MII0_RXD[3]	I	F14	X2-59	
PR2_MII0_TXD[0]	O	E14	X2-54	
PR2_MII0_TXD[1]	O	A12	X2-58	
PR2_MII0_TXD[2]	O	B13	X2-60	
PR2_MII0_TXD[3]	O	A11	X2-62	
PR2_MII1_COL	I	D18	X2-74	3.3 V
PR2_MII1_CRS	I	E17	X2-72	
PR2_MII1_MR_CLK	I	AC9	X3-73	
PR2_MII1_MT_CLK	I	AC5	X3-77	
PR2_MII1_RXDV	I	AC3	X3-75	
PR2_MII1_RXER	I	B19	X3-43	
PR2_MII1_RXLINK	I	C17	X2-70	
PR2_MII1_TXEN	O	AB4	X3-70	
PR2_MII1_RXD[0]	I	AB5	X3-62	
PR2_MII1_RXD[1]	I	AB8	X3-64	
PR2_MII1_RXD[2]	I	AD6	X3-66	
PR2_MII1_RXD[3]	I	AC8	X3-68	
PR2_MII1_TXD[0]	O	AC6	X3-72	
PR2_MII1_TXD[1]	O	AC7	X3-74	
PR2_MII1_TXD[2]	O	AC4	X3-76	
PR2_MII1_TXD[3]	O	AD4	X3-78	

3.2.4.14 QSPI – Quad SPI

The TQMa57xx provides a quad SPI interface, which is used for the NOR flash on the TQMa57xx.
To provide more QSPI NOR flash on the carrier board, the interface is routed to the TQMa57xx connectors. Depending on the VDDSHV10 supply configuration, 3.3 V or 1.8 V are available. The QSPI NOR flash devices must be selected accordingly.
The following table shows the QSPI interface signals.

Table 27: QSPI signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
QSPI_DATA0	I/O	U1	X4-72	1.8 V (3.3 V)
QSPI_DATA1	I/O	P3	X4-74	
QSPI_DATA2	I/O	U2	X4-76	
QSPI_DATA3	I/O	T2	X4-78	
QSPI_RTCLK	I	R3	X4-66	
QSPI_SCK	O	R2	X4-64	
QSPI_SS0#	O	P2	X4-82	
QSPI_SS1#	O	P1	X4-68	

3.2.4.15 RTCSS – Real Time Clock Subsystem

The following signal of the Real Time Clock subsystem is used.

Table 28: RTCSS signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
WAKEUP0	I	AD17	X2-18	1.8 V (3.3 V)

3.2.4.16 SATA

The TQMa57xx provides a SATA interface according to standard V2.6.
The following table shows the SATA interface signals.

Table 29: SATA signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
SATA1_RXP0	I	AG9	X4-23	1.8 V
SATA1_RXN0	I	AH9	X4-21	
SATA1_TXP0	O	AH10	X4-24	
SATA1_TXN0	O	AG10	X4-22	
SATA1_LED	O	A22	X1-83	3.3 V

3.2.4.17 SPI

The TQMa57xx provides a primary SPI interface, SPI1. Further SPI interfaces are possible with an adapted pin multiplexing.
SPI1 is configured as Master, Full Duplex, and routed to the TQMa57xx connectors.
The following table shows the SPI interface signals.

Table 30: SPI signals

Signal	Dir.	CPU ball	TQMa57xx	Voltage
SPI1_SCLK	O	A25	X2-77	3.3 V
SPI1_CS0	O	A24	X2-79	
SPI1_D0	I/O	B25	X2-71	
SPI1_D1	I/O	F16	X2-73	

3.2.4.18 UART

The TQMa57xx provides four primary UART interfaces. Further interfaces are possible with an adapted pin multiplexing.
UART 3, 4 and 10 are available with all three CPU variants. UART 8 is only for AM572x and AM574x enabled as primary function.
The following table shows the UART interface signals. All UARTS operate at 3.3 V.

Table 31: UART signals

Signal	Dir.	CPU ball	TQMa57xx	Remark
UART3_RXD	I	A26	X1-100	RS-232 for Debug switch on MBa57xx
UART3_TXD	O	B22	X1-102	
UART4_RXD	I	G16	X1-106	–
UART4_TXD	O	D17	X1-108	
UART8_RXD	I	AE8	X1-114	Only on TQMa572x, and TQMa574x
UART8_TXD	O	AD8	X1-116	
UART8_RTS#	O	AH6	X1-112	
UART10_RXD	I	D1	X1-6	RS-485 (Full Duplex) on MBa57xx
UART10_TXD	O	E2	X1-8	
UART10_RTS#	O	F4	X1-4	

3.2.4.19 USB

The TQMa57xx provides two independent USB controllers with integrated PHY.
USB1 supports USB3.0 SuperSpeed (SS) and complies with USB3.0 standard V1.0 with a maximum data rate of 5 Gbps.
With an adapted pin multiplexing this interface can also be used as USB2.0 High Speed Interface.
USB2 supports USB2.0 High-Speed and complies with USB2.0 standard V2.0 with a maximum data rate of 480 Mbps.
The USB2.0 interface is designed as USB-OTG. Both USB interfaces are routed as primary functions on the TQMa57xx connectors.
The following table shows the USB interface signals.

Table 32: USB signals

Signal	Dir.	CPU ball	TQMa57xx	Remark
USB3.0_DP	I/O	AD12	X4-5	USB3.0
USB3.0_DM	I/O	AC12	X4-3	
USB3.0_DRVVBUS	O	AB10	X4-2	
USB3.0_RXP0	I	AE12	X4-10	
USB3.0_RXN0	I	AF12	X4-12	
USB3.0_TXP0	O	AD11	X4-11	
USB3.0_TXN0	O	AC11	X4-9	
USB2.0_DP	I/O	AE11	X4-15	USB2.0 OTG
USB2.0_DM	I/O	AF11	X4-16	
USB2.0_DRVVBUS	O	AC10	X4-18	
USB2.0_OTG_ID	I	AC16	X4-17	
USB2.0_OTG_OC#	I	G13	X1-54	

3.2.4.20 VOUT – Video Output

The TQMa57xx provides a parallel display interface VOUT1 as primary function on the TQMa57xx connectors.
With an adapted pin multiplexing two further video outputs or a video input (VIN) are possible.
The interface consists of a 24-bit data bus, synchronization and other control signals, and works at 1.8 V
The following table shows the VOUT1 interface signals.

Table 33: VOUT1 signals

Signal	CPU ball	TQMa57xx
VOUT1_D[0]	F11	X1-27
VOUT1_D[1]	G10	X1-25
VOUT1_D[2]	F10	X1-23
VOUT1_D[3]	G11	X1-21
VOUT1_D[4]	E9	X1-36
VOUT1_D[5]	F9	X1-34
VOUT1_D[6]	F8	X1-19
VOUT1_D[7]	E7	X1-32
VOUT1_D[8]	E8	X1-15
VOUT1_D[9]	D9	X1-30
VOUT1_D[10]	D7	X1-13
VOUT1_D[11]	D8	X1-28
VOUT1_D[12]	A5	X1-11
VOUT1_D[13]	C6	X1-24
VOUT1_D[14]	C8	X1-9
VOUT1_D[15]	C7	X1-22
VOUT1_D[16]	B7	X1-7
VOUT1_D[17]	B8	X1-20
VOUT1_D[18]	A7	X1-5
VOUT1_D[19]	A8	X1-18
VOUT1_D[20]	C9	X1-3
VOUT1_D[21]	A9	X1-16
VOUT1_D[22]	B9	X1-14
VOUT1_D[23]	A10	X1-12
VOUT1_CLK	D11	X1-35
VOUT1_DE	B10	X1-31
VOUT1_HSYNC	C11	X1-40
VOUT1_VSYNC	E11	X1-38

3.2.5 Reset

Reset inputs and outputs are available on the TQMa57xx connectors.
A red LED signals the RESET# state.
The following table describes the reset signals available on the TQMa57xx connector.

Table 34: Reset signals

Signal	Dir.	TQMa57xx	Voltage	Remark
TQMa57xx_RST_IN# (RST_FROM_MB#)	I	X1-37	3.3 V	• Reset input • Generates PORz for AM57xx • Low-active signal • PORz is the only reliable Reset signal (Errata i862)
RST_TO_MB#	O	X1-39	3.3 V	• Reset output • Usage: reset external peripherals • Equivalent to TQMa57xx_RST_IN#
RSTOUT#	O	X1-77	3.3 V	• Low-active signal • Generated by PMIC (RESWARM#), or AM57xx RSTOUT#

3.2.6 Power

3.2.6.1 Power supply

The TQMa57xx only requires a single power supply of 5 V ±5 %.

3.2.6.2 Power consumption

The power consumption of the TQMa57xx strongly depends on the application, the mode of operation and the operating system. For this reason the given values have to be seen as approximate values.
The following table shows power supply and power consumption parameters of the TQMa57xx:

Table 35: TQMa57xx power consumption

TQMa57xx	Mode of operation	Current @ 5 V	Power @ 5 V	Remark
TQMa57xx	@ +25 °C	3.067 A	15.335 W	TI: AM572x_power_estimation.max.load.0002.xlsm
	@ +85 °C	3.509 A	17.546 W	TI: AM572x_power_estimation.max.load.0002.xlsm
	Suspend to RAM	0.6 ~ 0.9 A	3 ~ 4.5 W	Post in TI E2E community
TQMa5718	RESET	193 mA	965 mW	Reset button S8 on MBa57xx pressed
	U-Boot idle	419 mA	2,095 mW	–
	Linux idle	434 mA	2,170 mW	–
	Linux 100 % load	682 mA	3,410 mW	`stressapptest -s 60 -M 512 -m 8 -C 8 -i 8 -W`
TQMa5728	RESET	210 mA	1,050 mW	Reset button S8 on MBa57xx pressed
	U-Boot idle	555 mA	2,775 mW	–
	Linux idle	623 mA	3,115 mW	–
	Linux 100 % load	1,135 mA	5,675 mW	`stressapptest -s 60 -M 1256 -m 8 -C 8 -i 8 -W`
TQMa5748	RESET	379 mA	1,895 mW	Reset button S8 on MBa57xx pressed
	U-Boot idle	683 mA	3,415 mW	–
	Linux idle	692 mA	3,460 mW	–
	Linux 100 % load	1,223 mA	6,115 mW	`stressapptest -s 60 -M 1256 -m 8 -C 8 -i 8 -W`
TQMa5748 + ECC	RESET	185 mA	925 mW	Reset button S8 on MBa57xx pressed
	U-Boot idle	580 mA	2,900 mW	–
	Linux idle	590 mA	2,950 mW	–
	Linux 100 % load	1,212 mA	6,060 mW	`stressapptest -s 60 -M 1256 -m 8 -C 8 -i 8 -W`

3.2.6.3 Provided TQMa57xx voltages

In addition to the TQMa57xx supply input, some TQMa57xx-internal voltages are available on the TQMa57xx connectors.
The following table shows these voltages:

Table 36: Provided TQMa57xx voltages

Signal	Voltage	Source	Usage	TQMa57xx
PMIC_REGEN1	5 V	PMIC REGEN1	• Sequencing signal for external components • Enable for 3.3 V on carrier board	X1-87
V_BAT	3.3 V	LICELL	• RTC DS1339 supply	X2-13

3.2.6.4 Voltage monitoring

A supervisor on the TQMa57xx monitors the input voltage (VCC5V). If the input voltage is too low, the TQMa57xx is held in reset until the input voltage is within the defined range. The supervisor typically triggers at 4.7385 V and has a delay of 300 msec.

Attention: Malfunction or destruction	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. An excessively high supply voltage can lead to malfunctions, untimely aging or destruction of the TQMa57xx.

3.2.6.5 Power-Up sequence TQMa57xx / carrier board

The TQMa57xx meets the required sequencing of the AM57xx (6) by using the PMIC (7).

The TQMa57xx operates with 5 V; the 3.3 V I/O voltage of the AM57xx signals is generated on the TQMa57xx.

This leads to requirements for the carrier board design concerning the chronological characteristics of the voltages generated on the carrier board.

Attention: Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. To ensure a correct power-up, the following sequence must be met on the carrier board: The supply voltage of 5 V for the TQMa57xx is present and the carrier board supply of 3.3 V is activated with TQMa57xx pin PMIC_REGEN1 (X1-87).

3.2.6.6 Power modes

- Suspend to RAM
- Standby
- DVFS
- IDLE

Which power-modes are supported is TBD.

3.2.6.7 PMIC

On the TQMa57xx the PMIC TPS6590379 is used.

Note: PMIC signals	
	The PMIC INT signal is available via GPIO4_1_F2 (X1-46).

Attention: Malfunction or destruction	
	The PMIC can be controlled via I^2C bus 1 of the AM57xx. Improper PMIC programming may cause the AM57xx or other peripherals on the TQMa57xx to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa57xx.

4. MECHANICS

4.1 TQMa57xx connectors

The TQMa57xx is connected to the carrier board with 400 pins on four connectors.
The following table shows details of the connectors used:

Table 37: Connectors assembled on TQMa57xx

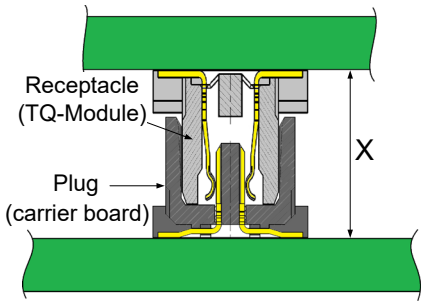
Manufacturer	Part number	Remark
TE connectivity	80-pin: 5177985-3 120-pin: 5177985-5	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMa57xx is held in the mating connectors by 400 pins with a retention force of approximately 40 N.
To avoid damaging the connectors of the TQMa57xx as well as the connectors on the carrier board while removing the TQMa57xx, the use of the extraction tool MOZIA57XX is strongly recommended. See chapter 4.8 for further information.

Attention: Component placement on the carrier board	
	2.5 mm should be kept free on the carrier board, on both cross sides of the TQMa57xx for the extraction tool MOZIA57XX.

The following table shows some suitable mating connectors for the carrier board.

Table 38: Carrier board mating connectors

Manufacturer	Part number	Remark	Stack height (X)	
TE connectivity	80-pin: 5177986-3 120-pin: 5177986-5	On MBa57xx	5 mm	
	80-pin: 1-5177986-3 120-pin: 1-5177986-5	–	6 mm	
	80-pin: 2-5177986-3 120-pin: 2-5177986-5	–	7 mm	
	80-pin: 3-5177986-3 120-pin: 3-5177986-5	–	8 mm	

The pin assignment listed in Table 2 to Table 5 refer to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in listed in Table 2 to Table 5 refer to the AM57xx Data Sheet (1).

4.2 Dimensions

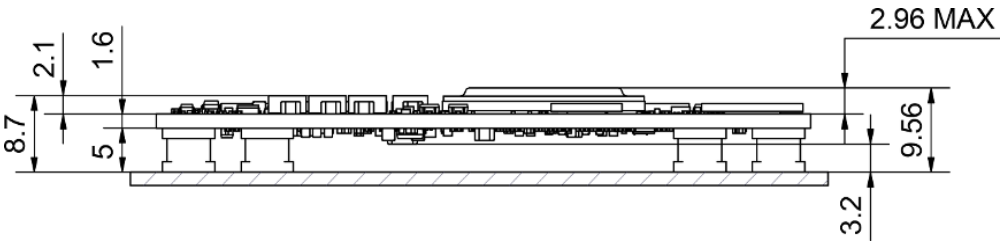


Figure 3: TQMa57xx dimensions, side view

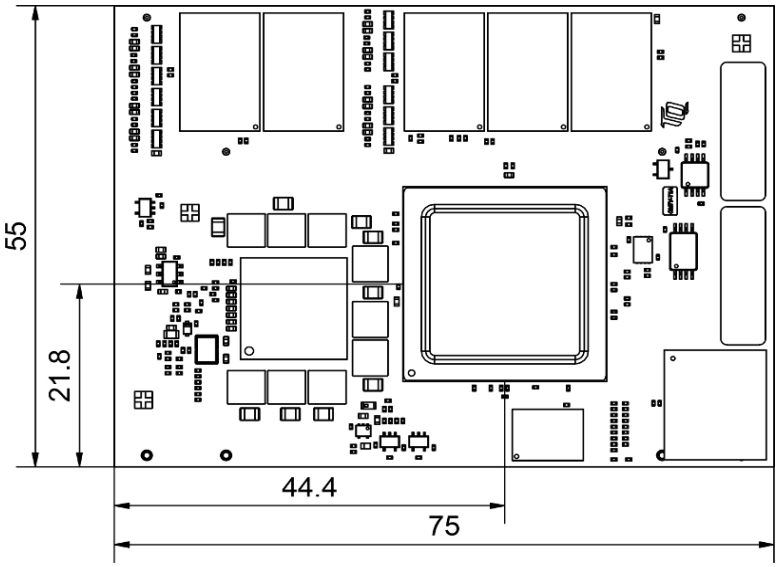


Figure 4: TQMa57xx dimensions, top view

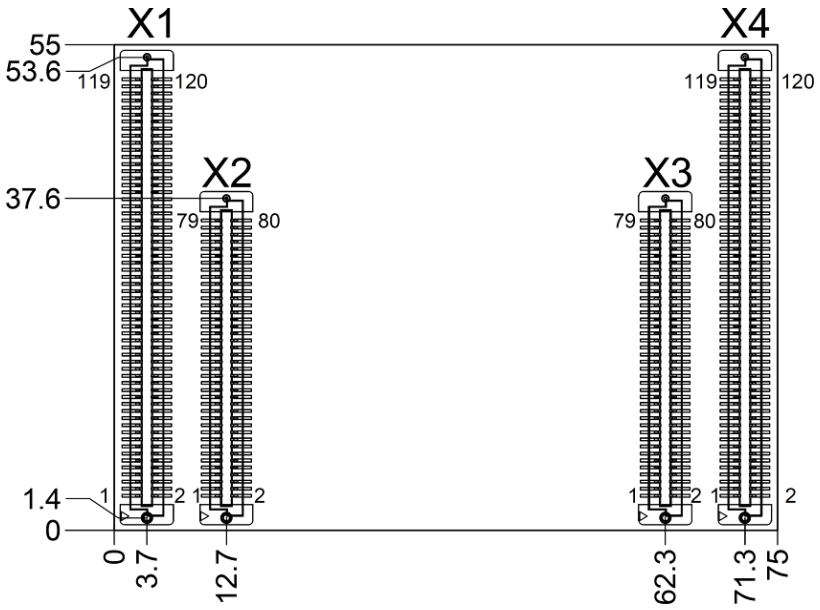


Figure 5: TQMa57xx dimensions, top view through TQMa57xx

4.3 Component placement

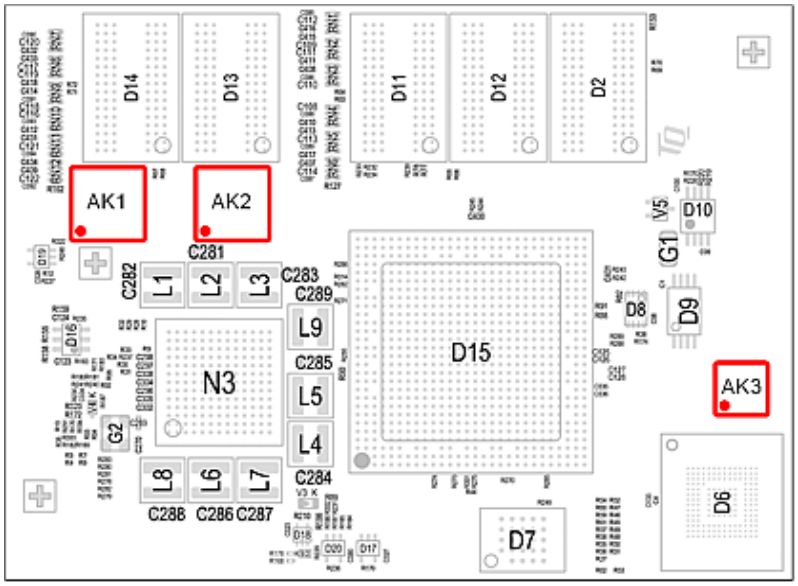


Figure 6: TQMa57xx, component placement top

The labels on the TQMa57xx show the following information:

Table 39: Labels on TQMa57xx

Label	Content
AK1	TQMa57xx version and revision, tests performed
AK2	First MAC address plus three additional reserved consecutive MAC addresses
AK3	Serial number

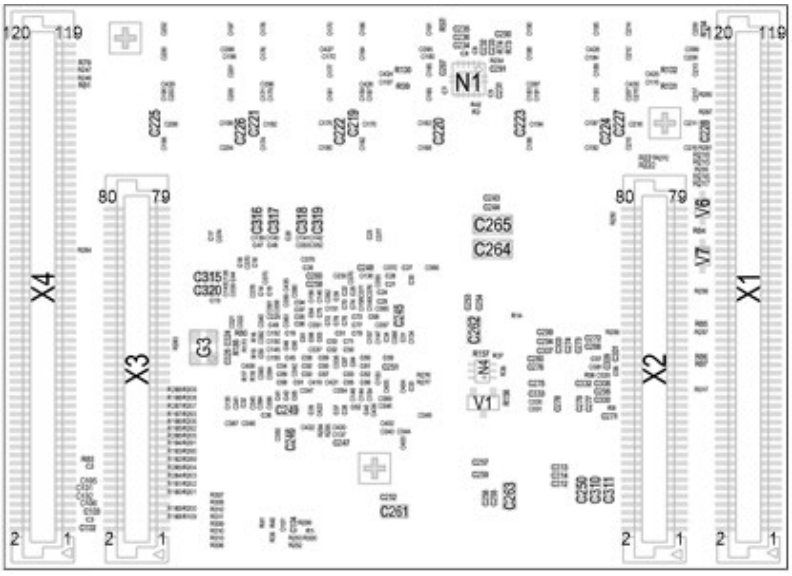


Figure 7: TQMa57xx, component placement bottom

4.4 Adaptation to the environment

The TQMa57xx has overall dimensions (length × width × height) of 75 × 55 × 8.16 mm³.
The TQMa57xx has a maximum height above the carrier board of approximately 9.56 mm.
The TQMa57xx weighs approximately 32 grams.

4.5 Protection against external effects

As an embedded module, the TQMa57xx is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa57xx, approximately 6 Watt must be dissipated, see Table 35 for peak currents.
The cooling solution must be able to dissipate this power peak; it will never occur permanently in normal operation.
The power dissipation originates primarily in the AM57xx, the DDR3L SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See TI documents (3), and (4) for further information.

Attention: Destruction or malfunction, TQMa57xx heat dissipation	
	The TQMa57xx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM57xx must be taken into consideration when connecting the heat sink, see (3). The AM57xx is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa57xx and thus malfunction, deterioration or destruction.

4.7 Structural requirements

The TQMa57xx is held in the mating connectors by the 400 pins with a retention force of approximately 40 N.

4.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa57xx may only be extracted from the carrier board by using the extraction tool MOZIAM57XX that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both cross sides of the TQMa57xx for the extraction tool MOZIA57XX.

5. SOFTWARE

The TQMa57xx is delivered with a preinstalled boot loader U-Boot and a TQ-BSP, which is tailored for the MBa57xx.
The boot loader U-Boot provides TQMa57xx-specific as well as MBa57xx-specific settings, e.g.:

- AM57xx configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.
More information can be found in the TQMa57xx Support Wiki.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa57xx was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa57xx.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering, perhaps Zener diode(s)
- Fast signals: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The operating temperature range for the TQMa57xx strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa57xx.

In general, a reliable operation is given when following conditions are met:

Table 40: Climate and operational conditions extended temperature range –25 °C to +85 °C

Parameter	Range	Remark
Chip temperature AM57xx	–40 °C to +105 °C	Typical max +90 °C
Ambient temperature AM57xx	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	–
Ambient temperature PMIC	–40 °C to +85 °C	–
Case temperature DDR3L-SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–25 °C to +85 °C	–
Storage temperature TQMa57xx	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 41: Climate and operational conditions industrial temperature range –40 °C to +85 °C

Parameter	Range	Remark
Chip temperature AM57xx	–40 °C to +105 °C	Typical max +90 °C
Ambient temperature AM57xx	–40 °C to +85 °C	–
Chip temperature PMIC	–40 °C to +125 °C	–
Ambient temperature PMIC	–40 °C to +85 °C	–
Case temperature DDR3L-SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Storage temperature TQMa57xx	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the thermal characteristics of the AM57xx is to be taken from the TI documents (3), and (4).

6.5 Reliability and service life

The calculated theoretical MTBF of the TQMa57xx is 742,256 h @ +40 °C environmental temperature, ground benign.

The TQMa57xx is designed to be insensitive to shock and vibration.

High quality industrial grade connectors are assembled on the TQMa57xx.

Detailed information regarding the AM57xx service life under varying operating conditions can be obtained on the TI homepage using the DPPM/ FIT/ MTBF Estimator. (https://www.ti.com/quality/docs/estimator.tsp)

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa57xx is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa57xx was designed to be recyclable and easy to repair.

7.3 REACH®

The EU chemicals regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, authorisation and restriction of SVHC substances (substances of very high concern, e.g. carcinogenic, mutagenic and/or persistent, bioaccumulative and toxic).
It applies to all SVHC substances placed on the market in quantities of more than 1 t per year per manufacturer or importer.
No control over REACH® beyond the RoHS test was conducted.

7.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa57xx must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the TQMa57xx enable compliance with EuP requirements for the TQMa57xx.

7.5 Battery

No batteries are assembled on the TQMa57xx.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa57xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa57xx is minimised by suitable measures. The TQMa57xx is delivered in reusable packaging.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 42: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CAN-FD	CAN with Flexible Data-Rate
CAT	Control Automation Technology
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DCAN	Dual Controller Area Network
DDR	Double Data Rate
DDR3L	Double Data Rate 3 Low voltage
DPPM	Defective Parts Per Million
DSP	Digital Signal Processor
DVFS	Dynamic Voltage and Frequency Scaling
DVI	Digital Visual Interface
eCAP	Enhanced Capture Module
ECAT	EtherCAT
ECC	Error-Correcting Code
EEPROM	Electrically Erasable Programmable Read-only Memory
eHRPWM	Enhanced High-Resolution Pulse-Width Modulator
EMC	Electromagnetic Compatibility
EMIF	External Memory Interface
eMMC	embedded Multimedia Card (Flash)
ENET	Ethernet
eQEP	Enhanced Quadrature Encoder Pulse
ESD	Electro-Static Discharge
EU	European Union
EuP	Energy using Products
FIT	Failure In Time
GbE	Gigabit Ethernet
GMAC	Gigabit-Ethernet MAC
GMII	Gigabit Media-Independent Interface
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPMC	General Purpose Memory Controller
GPO	General Purpose Output
HDMI®	High-Definition Multimedia Interface
HDQ™	Harmonic Differential Quadrature
HS	High Speed (USB: 480 Mbit/s)
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
ICSS	Industrial Communication Subsystem
IP00	Ingress Protection 00
JTAG	Joint Test Action Group
KBD	Keyboard
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCAN	Multimaster CAN

8.1 Acronyms and definitions (continued)

Table 42: Acronyms (continued)

Acronym	Meaning
MCASP	Multichannel Audio Serial Port
MDIO	Management Data Input/Output
MII	Media-Independent Interface
MMC	Multimedia Card
MTBF	Mean operating Time Between Failures
N/A	Not Applicable
NAND	Not-And
NOR	Not-Or
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRCM	Power, Reset, and Clock Management
PRU	Programmable Real-Time Unit
PRUSS	Programmable Real-Time Unit Subsystem
PU	Pull-Up
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGB	Red Green Blue
RGMII	Reduced Gigabit Media-Independent Interface
RJ45	Registered Jack 45
RMII	Reduced Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RS-232, RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
RTCSS	Real-Time Clock Subsystem
RWP	Reversible Write Protected
SAI	Serial Audio Interface
SATA	Serial ATA
SBL	Secondary Bootloader
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDMA	System Direct Memory Access
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SS	SuperSpeed (USB: 5 Gbit/s)
SVHC	Substances of Very High Concern
SW	Software
TBD	To Be Determined
TP	Test Point
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
USB-OTG	Universal Serial Bus - On-The-Go
WC	Write-Control
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 43: Further applicable documents

No.	Name	Rev., Date	Company
(1)	AM572x Datasheet, am572x_Silicon_Rev_2.0.pdf	Rev. 2.0, 06/2017	Texas Instruments
(2)	AM572x Chip Errata, am572x_Errata.pdf	Rev. 1.1 & 2.0, 03/2017	Texas Instruments
(3)	AM572x Power Estimation, AM572x_Power_Estimation.0001.xlsm	Rev. 2, 04/2015	Texas Instruments
(4)	AM572x Product Usage Lifetime Estimator DPPM/FIT/MTBF estimator	Online	Texas Instruments
(5)	AM572x General Purpose EVM HW User Guide	Online	Texas Instruments
(6)	AM572x Technical Reference Manual, am572x_Technical_Reference_Manual.pdf	Rev. 2.0, 10/2018	Texas Instruments
(7)	Power management integrated circuit, tps659037.pdf	Rev. 7, 07/2017	Texas Instruments
(8)	MBa57xx User's Manual	– current –	TQ-Systems
(9)	Support-Wiki for the TQMa57xx	– current –	TQ-Systems

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