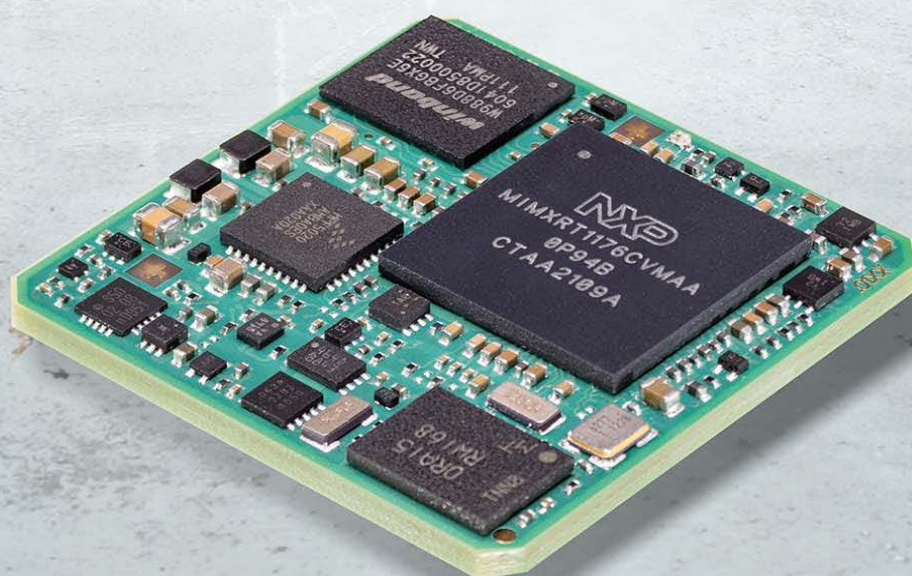




# TQMa117xL User's Manual

TQMa117xL UM 0101  
14.11.2025





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## REVISION HISTORY

| Rev. | Date       | Name    | Pos.                                | Modification                                                   |
|------|------------|---------|-------------------------------------|----------------------------------------------------------------|
| 0001 | 14.10.2021 | Kreuzer |                                     | First preliminary issue                                        |
| 0002 | 24.03.2022 | Kreuzer | 3.2.2.3<br>3.2.6.1                  | EEPROM structure revised<br>I <sup>2</sup> C structure revised |
| 0003 | 09.06.2022 | Kreuzer | Table 3                             | Changed TQMa117xL_HARD_RESET# to VIN with Pullup               |
| 0100 | 29.08.2023 | Kreuzer | All                                 | Reworked the whole document to module revision 0200            |
| 0101 | 14.11.2025 | Kreuzer | 1.4, 6.4, 6.5, 6.6, 7.5<br>Table 12 | Chapter added<br>EEPROM function corrected                     |



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## 1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

## 1.7 Symbols and typographic conventions

Table 1: Terms and conventions

| Symbol                                                                              | Meaning                                                                                                                                                                                                                                                                                         |
|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|   | This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V. |
|  | This symbol indicates the possible use of voltages higher than 24 V.<br>Please note the relevant statutory regulations in this regard.<br>Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.                              |
|  | This symbol indicates a possible source of danger.<br>Ignoring the instructions described can cause health damage, or damage the hardware.                                                                                                                                                      |
|  | This symbol represents important details or aspects for working with TQ-products.                                                                                                                                                                                                               |
| <b>Command</b>                                                                      | A font with fixed-width is used to denote commands, contents, file names, or menu items.                                                                                                                                                                                                        |

## 1.8 Handling and ESD tips

General handling of your TQ-products

|                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.</p> <p>Violation of this guideline may result in damage / destruction of the TQMa117xL and be dangerous to your health.</p> <p>Improper handling of your TQ-product would render the guarantee invalid.</p> |
|-------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Proper ESD handling



The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

## 1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring. The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

## 1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**  
These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**  
The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**  
It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**  
No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**  
Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa117xL circuit diagram
- [MBa117xL User's Manual](#)
- [i.MX RT1170 Data Sheet](#)
- i.MX RT1170 Reference Manual
- U-Boot documentation: [www.denx.de/wiki/U-Boot/Documentation](http://www.denx.de/wiki/U-Boot/Documentation)
- FreeRTOS documentation: [www.freertos.org/Documentation/RTOS\\_book.html](http://www.freertos.org/Documentation/RTOS_book.html)
- TQ-Support Wiki: [Support-Wiki TQMa117xL](#)

## 2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa117xL  $\geq$  Rev. 02xx, in combination with the MBa117xL  $\geq$  Rev. 02xx and refers to some software settings. A certain TQMa117xL derivative does not necessarily provide all features described in this User's Manual.

This User's Manual does neither replace the i.MX RT1170 Reference Manual (1), nor the i.MX RT1170 Data Sheet (2), nor any other documents from NXP.

The TQMa117xL is a universal Minimodule based on the NXP ARM® Cortex®-M7 based i.MX RT1170 CPU family, consisting of models RT1171, RT1172, RT1173, RT1175 and RT1176.

See also Table 4.

### 2.1 Key functions and characteristics

The TQMa117xL extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

All essential i.MX RT117x signals are routed to the TQMa117xL LGA pads. There are therefore no restrictions for customers using the TQMa117xL with respect to an integrated customised design. All essential components like CPU and Memory are already integrated on the TQMa117xL.

The main features of the TQMa117xL are:

- LPSPDRAM memory
- NOR Flash device as boot source
- Own clock supply
- Power supply adapted for the TQMa117xL
- External RTC
- Temperature sensor + EEPROM
- Trust Secure Element
- EEPROM for TQ data and costumer data

### 2.2 CPU block diagram

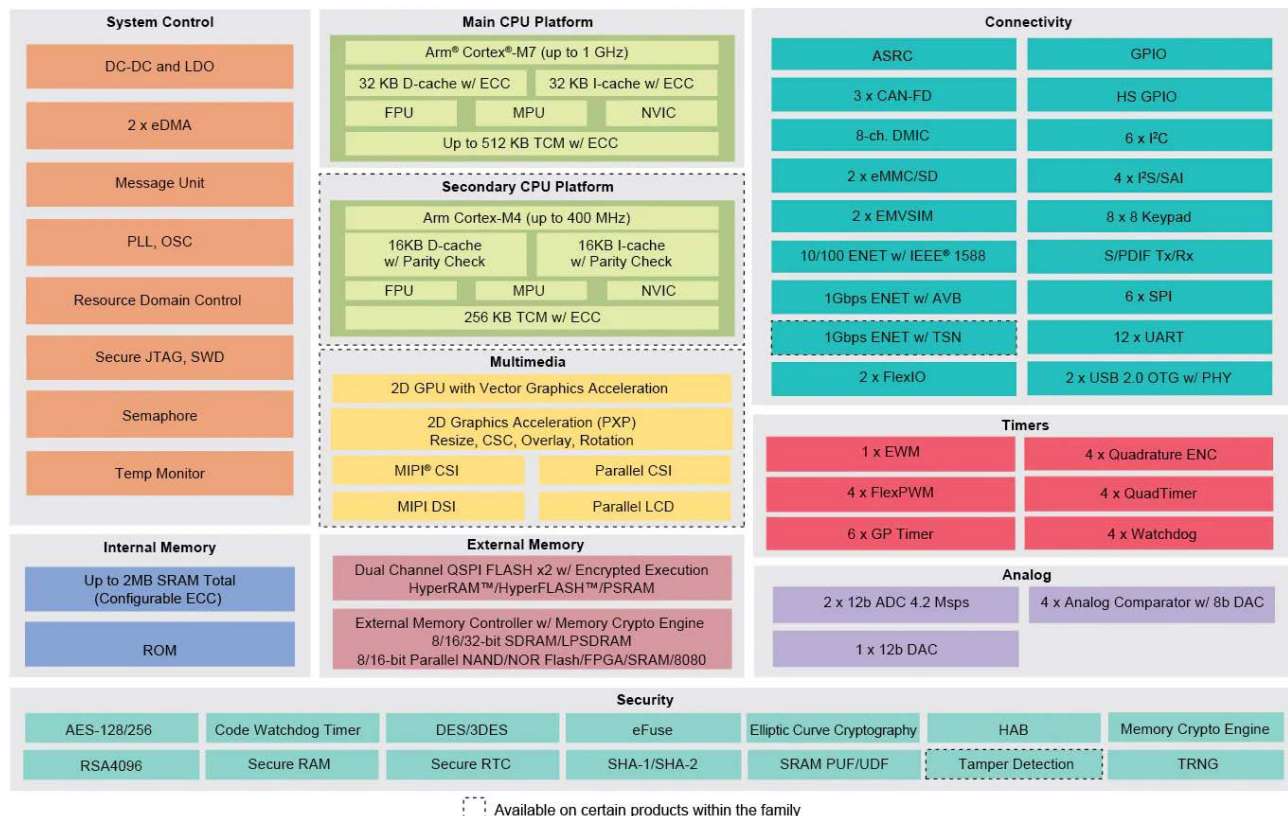


Figure 1: Block diagram RT117x CPU  
(Source: [NXP](#))

### 3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa117xL, and the [BSP provided by](#) TQ-Systems GmbH, see also chapter 4.

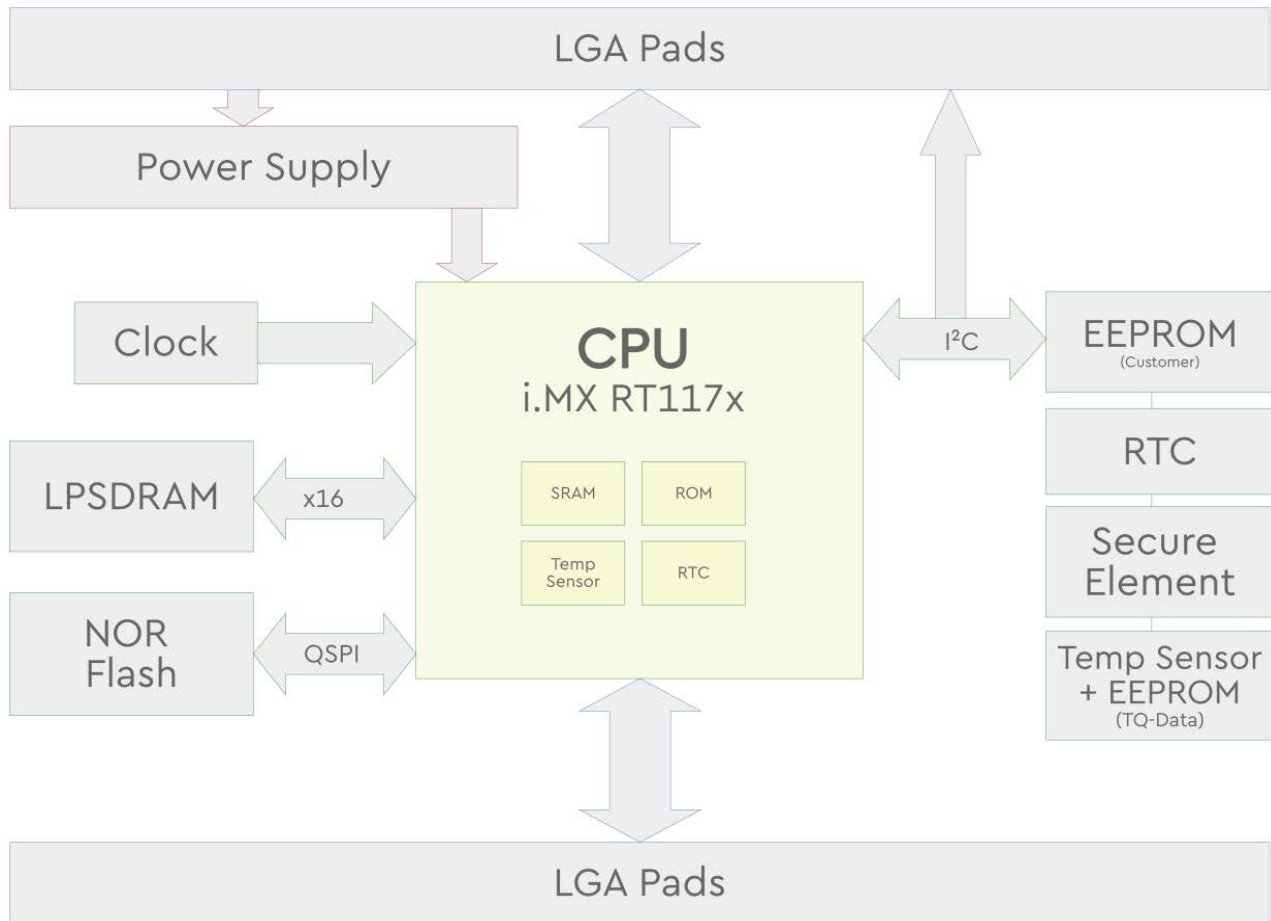


Figure 2: Block diagram TQMa117xL (simplified)

#### 3.1 Interfaces to other systems and devices

##### 3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX RT117x-internal function units must be taken note of. The pin assignment in Table 2 refers to a TQMa117xL with i.MX RT117x CPU in combination with the carrier board MBa117xL. NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool). The electrical and pin characteristics are to be taken from the i.MX RT117x and PMIC documentation.

#### Attention: Destruction or malfunction, pin multiplexing



Depending on the configuration, many i.MX RT117x pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX RT117x Reference Manual (1), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa117xL.

The descriptions given in the following tables should be taken note of:

- DNC: These pins must never be connected and have to be left open.

Please contact [TQ-Support](#) for details.



### 3.1.1.1 Pinout TQMa117xL

The TQMa117xL has a total of 277 LGA pads. The TQMa117xL is soldered and thus permanently connected to the carrier board.

It is not trivial and it is not recommended to remove the TQMa117xL from the carrier board.

The following table shows the TQMa117xL pad-out, top view through the TQMa117xL.

Table 2: Pinout TQMa117xL, top view through TQMa117xL

|    | A              | B              | C               | D                 | E              | F              | G              | H              | J              | K              | L               | M               | N               | P               | R               | T               | U               |    |
|----|----------------|----------------|-----------------|-------------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----|
| 17 |                | GPIO_EMC_B2_20 | GPIO_EMC_B2_18  | GND               | GPIO_EMC_B2_14 | GPIO_EMC_B2_11 | GND            | VIN            | VIN            | VIN            | GND             | VCC1V8          | VCC1V8          | GND             | GPIO_DISP_B2_09 | GPIO_DISP_B2_10 |                 | 17 |
| 16 | HARD_RESET#    | GND            | GPIO_EMC_B2_17  | GPIO_EMC_B2_16    | GND            | GPIO_EMC_B2_10 | GND            | VIN            | VIN            | GND            | VCC1V8          | VCC1V8          | GND             | GPIO_DISP_B2_07 | GPIO_DISP_B2_08 | GND             | GPIO_DISP_B2_11 | 16 |
| 15 | SE_ISO7816_CLK | GPIO_EMC_B2_19 | GND             | GPIO_EMC_B2_15    | GPIO_EMC_B2_13 | GND            | GND            | GND            | GND            | GND            | GND             | GND             | GPIO_DISP_B2_05 | GPIO_DISP_B2_06 | GND             | GPIO_DISP_B2_12 | GPIO_DISP_B2_13 | 15 |
| 14 | GND            | SE_ISO7816_IO2 | SE_ISO14443_LA  | GND               | GPIO_EMC_B2_12 | GPIO_EMC_B2_09 | GND            | GPIO_EMC_B2_05 | GPIO_EMC_B2_03 | GPIO_EMC_B2_00 | GND             | GPIO_DISP_B2_02 | GPIO_DISP_B2_03 | GND             | GPIO_DISP_B2_14 | GPIO_DISP_B2_15 | GND             | 14 |
| 13 | SE_ISO7816_IO1 | GND            | SE_ISO7816_RST# | DNC               | GND            | GPIO_EMC_B2_08 | GPIO_EMC_B2_07 | GND            | GPIO_EMC_B2_02 | GND            | GPIO_DISP_B2_01 | GPIO_DISP_B2_00 | GND             | GPIO_DISP_B2_04 | GPIO_DISP_B1_07 | GND             | GPIO_DISP_B1_04 | 13 |
| 12 | VRTC_IN        | SE_ISO14443_LB | GND             | SE_ENA            | DNC            | GND            | GPIO_EMC_B2_06 | GPIO_EMC_B2_04 | GPIO_EMC_B2_01 | GPIO_EMC_B1_41 | GPIO_EMC_B1_40  | GND             | GPIO_DISP_B1_02 | GPIO_DISP_B1_03 | GND             | GPIO_DISP_B1_06 | GPIO_DISP_B1_08 | 12 |
| 11 | GND            | DNC            | JTAG_TDI        | GND               | JTAG_TDO       | JTAG_TRST#     | GND            | GND            | GND            | PMIC_WDI       | GND             | GND             | GPIO_DISP_B1_01 | GND             | GPIO_DISP_B1_05 | GND             | RESET_OUT#      | 11 |
| 10 | RTC_CLKOUT     | GND            | JTAG_TMS        | JTAG_MOD          | GND            | JTAG_TCK       | PGOOD          |                |                |                | GND             | GPIO_DISP_B1_00 | GND             | GPIO_DISP_B1_09 | GPIO_DISP_B1_10 | DSI_DN0         | GND             | 10 |
| 9  | GPIO_LPSR_03   | GPIO_LPSR_02   | GND             | GPIO_LPSR_01      | GPIO_LPSR_00   | GND            | GND            |                |                |                | GND             | GPIO_SD_B2_00   | GPIO_SD_B2_01   | GPIO_DISP_B1_11 | GND             | DSI_DP0         | DSI_CKN         | 9  |
| 8  | RTC_INT#       | GND            | GPIO_LPSR_04    | CUSTOM_EEPROM_WC# | GND            | SOFT_RESET#    | TEMP_ALERT     | GND            |                |                | GPIO_SD_B2_02   | GPIO_SD_B2_03   | GND             | GPIO_SD_B1_04   | GPIO_SD_B1_05   | GND             | DSI_CKP         | 8  |
| 7  | GND            | VBAT_IN        | GPIO_LPSR_05    | GND               | GPIO_LPSR_08   | GPIO_LPSR_09   | GND            | MCU_Wakeup     | GND            | LP_UART1_TXD   | GND             | GPIO_SD_B2_04   | GPIO_SD_B2_05   | GND             | GPIO_SD_B1_03   | DSI_DN1         | GND             | 7  |
| 6  | GPIO_SNV_09    | GPIO_SNV_08    | GND             | GPIO_SNV_06       | PWR_BTN#       | GND            | GND            | LPI2C6_MOD_SCL | LPI2C6_MOD_SDA | LP_UART1_RXD   | GPIO_SD_B2_06   | GND             | GPIO_SD_B1_01   | GPIO_SD_B1_02   | GND             | DSI_DP1         | CSL_DN0         | 6  |
| 5  | GPIO_SNV_07    | GND            | GPIO_SNV_05     | GPIO_SNV_04       | GND            | GPIO_AD_14     | GPIO_AD_15     | GND            | GPIO_AD_26     | GND            | GPIO_SD_B2_07   | GPIO_SD_B2_08   | GND             | GPIO_SD_B1_00   | CTRL_NVCC_SD1   | GND             | CSL_DP0         | 5  |
| 4  | GND            | GPIO_SNV_02    | GPIO_SNV_03     | GND               | GPIO_AD_12     | GPIO_AD_13     | GND            | GPIO_AD_16     | GPIO_AD_27     | GPIO_AD_28     | GND             | GPIO_SD_B2_09   | GPIO_SD_B2_10   | GND             | NVCC_SD1        | CSL_CKN         | GND             | 4  |
| 3  | GPIO_SNV_00    | GPIO_SNV_01    | GND             | GPIO_AD_05        | GPIO_AD_06     | GND            | GPIO_AD_11     | GPIO_AD_29     | GND            | GPIO_AD_30     | GPIO_AD_32      | GND             | GPIO_SD_B2_11   | NVCC_SD2        | GND             | CSL_CKP         | CSL_DN1         | 3  |
| 2  | GPIO_AD_00     | GND            | GPIO_AD_03      | GPIO_AD_04        | GND            | GPIO_AD_09     | GPIO_AD_10     | GND            | GPIO_AD_34     | GND            | DAC_OUT         | CTRL_NVCC_SD2   | GND             | USB2_DN         | USB2_DP         | GND             | CSL_DP1         | 2  |
| 1  |                | GPIO_AD_01     | GPIO_AD_02      | GND               | GPIO_AD_07     | GPIO_AD_08     | GND            | GPIO_AD_31     | GPIO_AD_33     | GPIO_AD_35     | GND             | USB1_DN         | USB1_DP         | GND             | USB1_VBUS       | USB2_VBUS       |                 | 1  |
|    | A              | B              | C               | D                 | E              | F              | G              | H              | J              | K              | L               | M               | N               | P               | R               | T               | U               |    |

No pads at corner position A1 / A17 / U1 / U17

No pads at center position H9 / H10 / J8 / J9 / J10 / K8 / K9 / K10

### 3.1.1.2 TQMa117xL signals

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX RT1170 documentation (1), (2), (3), as well as the PMIC Data Sheet (4).

Table 3: TQMa117xL, signals

| Module Pad | Signal                | CPU BALL | IO | Group              | Description / Usage                                                                                                                      | Voltage Level            |       |
|------------|-----------------------|----------|----|--------------------|------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------|
| H16        | VIN                   | -        | P  | Input Power Supply | Module Main Power Input                                                                                                                  | 5 V ±5%                  |       |
| H17        |                       |          |    |                    |                                                                                                                                          |                          |       |
| J16        |                       |          |    |                    |                                                                                                                                          |                          |       |
| J17        |                       |          |    |                    |                                                                                                                                          |                          |       |
| K17        |                       |          |    |                    |                                                                                                                                          |                          |       |
| B7         | VBAT_IN               | -        | P  |                    | VBAT Power Supply Input                                                                                                                  | min. 2.8 V<br>max. 3.6 V |       |
| A12        | VRTC_IN               | -        | P  |                    | RTC Power Supply Input                                                                                                                   | min. 2.0 V<br>max. 5.5 V |       |
| R4         | NVCC_SD1              | -        | P  | Output Power       | NVCC_SD1 Power Supply<br>max. 20 mA                                                                                                      | 1.8 V<br>or<br>3.3 V     |       |
| P3         | NVCC_SD2              | -        | P  |                    | NVCC_SD2 Power Supply<br>max. 20 mA                                                                                                      | 1.8 V<br>or<br>3.3 V     |       |
| M16        | VCC1V8                | -        | P  |                    | Output Power<br>max. 600 mA                                                                                                              | 1.8 V                    |       |
| L16        |                       |          |    |                    |                                                                                                                                          |                          |       |
| M17        |                       |          |    |                    |                                                                                                                                          |                          |       |
| N17        |                       |          |    |                    |                                                                                                                                          |                          |       |
| E6         | TQMa117xL_PWR_BTN#    | U10      | I  | Module Control     | ONOFF Control                                                                                                                            | 1.8 V                    |       |
| F8         | TQMa117xL_SOFT_RESET# | T10      | I  |                    | POR# to CPU                                                                                                                              |                          |       |
| A16        | TQMa117xL_HARD_RESET# | -        | I  |                    | Hard Reset to TQMa117xL<br>including Power Cycle<br>4K7 Pullup to VIN                                                                    | 5 V<br>(VIN)             |       |
| G10        | TQMa117xL_PGOOD       | -        | O  |                    | TQMa117xL PGOOD Status                                                                                                                   | 1.8 V                    |       |
| U11        | TQMa117xL_RESET_OUT#  | -        | O  |                    | TQMa117xL Reset Status                                                                                                                   |                          |       |
| H7         | MCU_WAKEUP            | T8       | I  |                    | Wakeup form LP                                                                                                                           |                          |       |
| K11        | PMIC_WDI              | -        | I  |                    | Optional PMIC Watchdog                                                                                                                   |                          |       |
| R5         | CTRL_NVCC_SD1         | -        | I  |                    | NVCC_SD1 Power Control<br>Low: NVCC_SD1 = 3.3 V<br>High: NVCC_SD1 = 1.8 V                                                                |                          | 1.8 V |
| M2         | CTRL_NVCC_SD2         | -        | I  |                    | 47K Pulldown on TQMa117xL<br>NVCC_SD2 Power Control<br>Low: NVCC_SD2 = 3.3V<br>High: NVCC_SD2 = 1.8 V                                    |                          |       |
|            |                       |          |    |                    | 47K Pulldown on TQMa117xL                                                                                                                |                          |       |
| K7         | LPUART1_TXD           | L13      | O  | LPUART1            | LPUART1 used for debug<br>console                                                                                                        | 1.8 V                    |       |
| K6         | LPUART1_RXD           | M15      | I  |                    |                                                                                                                                          |                          |       |
| J6         | LPI2C6_MOD_SDA        | P8       | IO | LPI2C6             | I <sup>2</sup> C Interface used for I <sup>2</sup> C De-<br>vices on TQMa117xL                                                           | 1.8 V                    |       |
| H6         | LPI2C6_MOD_SCL        | R8       | O  |                    | Pullups on TQMa117xL                                                                                                                     |                          |       |
| L2         | DAC_OUT               | H16      | O  | DAC                | DAC Output                                                                                                                               | 1.8 V                    |       |
| F11        | JTAG_TRST#            | R5       | I  | Debug              | JTAG Interface<br><br>Optional SWD Interface:<br>JTAG_TCK = SWD_CLK<br>JTAG_TMS = SWD_DIO<br><br>JTAG_MOD: 4.7K Pulldown on<br>TQMa117xL | 1.8 V                    |       |
| E11        | JTAG_TDO              | T5       | O  |                    |                                                                                                                                          |                          |       |
| C11        | JTAG_TDI              | U5       | I  |                    |                                                                                                                                          |                          |       |
| F10        | JTAG_TCK              | T6       | I  |                    |                                                                                                                                          |                          |       |
| C10        | JTAG_TMS              | U7       | IO |                    |                                                                                                                                          |                          |       |
| D10        | JTAG_MOD              | U6       | I  |                    |                                                                                                                                          |                          |       |

| Module Pad | Signal        | CPU BALL | IO | Group      | Description / Usage | Voltage Level                    |
|------------|---------------|----------|----|------------|---------------------|----------------------------------|
| A2         | GPIO_AD_00    | N12      | IO | GPIO_AD    | IO Muxing Options   | 1.8 V                            |
| B1         | GPIO_AD_01    | R14      | IO |            |                     |                                  |
| C1         | GPIO_AD_02    | R13      | IO |            |                     |                                  |
| C2         | GPIO_AD_03    | P15      | IO |            |                     |                                  |
| D2         | GPIO_AD_04    | M13      | IO |            |                     |                                  |
| D3         | GPIO_AD_05    | P13      | IO |            |                     |                                  |
| E3         | GPIO_AD_06    | N13      | IO |            |                     |                                  |
| E1         | GPIO_AD_07    | T17      | IO |            |                     |                                  |
| F1         | GPIO_AD_08    | R15      | IO |            |                     |                                  |
| F2         | GPIO_AD_09    | R16      | IO |            |                     |                                  |
| G2         | GPIO_AD_10    | R17      | IO |            |                     |                                  |
| G3         | GPIO_AD_11    | P16      | IO |            |                     |                                  |
| E4         | GPIO_AD_12    | P17      | IO |            |                     |                                  |
| F4         | GPIO_AD_13    | L12      | IO |            |                     |                                  |
| F5         | GPIO_AD_14    | N14      | IO |            |                     |                                  |
| G5         | GPIO_AD_15    | M14      | IO |            |                     |                                  |
| H4         | GPIO_AD_16    | N17      | IO |            |                     |                                  |
| J5         | GPIO_AD_26    | L14      | IO |            |                     |                                  |
| J4         | GPIO_AD_27    | N16      | IO |            |                     |                                  |
| K4         | GPIO_AD_28    | L17      | IO |            |                     |                                  |
| H3         | GPIO_AD_29    | M17      | IO |            |                     |                                  |
| K3         | GPIO_AD_30    | K17      | IO |            |                     |                                  |
| H1         | GPIO_AD_31    | J17      | IO |            |                     |                                  |
| L3         | GPIO_AD_32    | K16      | IO |            |                     |                                  |
| J1         | GPIO_AD_33    | H17      | IO |            |                     |                                  |
| J2         | GPIO_AD_34    | J16      | IO |            |                     |                                  |
| K1         | GPIO_AD_35    | G17      | IO |            |                     |                                  |
| P5         | GPIO_SD_B1_00 | B16      | IO | GPIO_SD_B1 | IO Muxing Options   | NVCC_SD1<br>1.8 V<br>or<br>3.3 V |
| N6         | GPIO_SD_B1_01 | D15      | IO |            |                     |                                  |
| P6         | GPIO_SD_B1_02 | C15      | IO |            |                     |                                  |
| R7         | GPIO_SD_B1_03 | B17      | IO |            |                     |                                  |
| P8         | GPIO_SD_B1_04 | B15      | IO |            |                     |                                  |
| R8         | GPIO_SD_B1_05 | A16      | IO | GPIO_SD_B2 | IO Muxing Options   | NVCC_SD2<br>1.8 V<br>or<br>3.3 V |
| M9         | GPIO_SD_B2_00 | J15      | IO |            |                     |                                  |
| N9         | GPIO_SD_B2_01 | J14      | IO |            |                     |                                  |
| L8         | GPIO_SD_B2_02 | H13      | IO |            |                     |                                  |
| M8         | GPIO_SD_B2_03 | E15      | IO |            |                     |                                  |
| M7         | GPIO_SD_B2_04 | F14      | IO |            |                     |                                  |
| N7         | GPIO_SD_B2_05 | E14      | IO |            |                     |                                  |
| L6         | GPIO_SD_B2_06 | F17      | IO |            |                     |                                  |
| L5         | GPIO_SD_B2_07 | G14      | IO |            |                     |                                  |
| M5         | GPIO_SD_B2_08 | F15      | IO |            |                     |                                  |
| M4         | GPIO_SD_B2_09 | H15      | IO |            |                     |                                  |
| N4         | GPIO_SD_B2_10 | H14      | IO | GPIO_LPSR  | IO Muxing Options   | 1.8 V                            |
| N3         | GPIO_SD_B2_11 | H16      | IO |            |                     |                                  |
| E9         | GPIO_LPSR_00  | N6       | IO |            |                     |                                  |
| D9         | GPIO_LPSR_01  | R6       | IO |            |                     |                                  |
| B9         | GPIO_LPSR_02  | P6       | IO |            |                     |                                  |
| A9         | GPIO_LPSR_03  | T7       | IO |            |                     |                                  |
| C8         | GPIO_LPSR_04  | N7       | IO |            |                     |                                  |
| C7         | GPIO_LPSR_05  | N8       | IO |            |                     |                                  |
| E7         | GPIO_LPSR_08  | U8       | IO |            |                     |                                  |
| F7         | GPIO_LPSR_09  | P5       | IO |            |                     |                                  |

| Module Pad | Signal          | CPU BALL | IO | Group        | Description / Usage | Voltage Level |
|------------|-----------------|----------|----|--------------|---------------------|---------------|
| M10        | GPIO_DISP_B1_00 | E13      | IO | GPIO_DISP_B1 | IO Muxing Options   | 1.8 V         |
| N11        | GPIO_DISP_B1_01 | D13      | IO |              |                     |               |
| N12        | GPIO_DISP_B1_02 | D11      | IO |              |                     |               |
| P12        | GPIO_DISP_B1_03 | E11      | IO |              |                     |               |
| U13        | GPIO_DISP_B1_04 | E10      | IO |              |                     |               |
| R11        | GPIO_DISP_B1_05 | C11      | IO |              |                     |               |
| T12        | GPIO_DISP_B1_06 | D10      | IO |              |                     |               |
| R13        | GPIO_DISP_B1_07 | E12      | IO |              |                     |               |
| U12        | GPIO_DISP_B1_08 | A15      | IO |              |                     |               |
| P10        | GPIO_DISP_B1_09 | C13      | IO |              |                     |               |
| R10        | GPIO_DISP_B1_10 | B14      | IO |              |                     |               |
| P9         | GPIO_DISP_B1_11 | A14      | IO |              |                     |               |
| M13        | GPIO_DISP_B2_00 | -        | IO | GPIO_DISP_B2 | IO Muxing Options   | 1.8 V         |
| L13        | GPIO_DISP_B2_01 | -        | IO |              |                     |               |
| M14        | GPIO_DISP_B2_02 | -        | IO |              |                     |               |
| N14        | GPIO_DISP_B2_03 | -        | IO |              |                     |               |
| P13        | GPIO_DISP_B2_04 | -        | IO |              |                     |               |
| N15        | GPIO_DISP_B2_05 | -        | IO |              |                     |               |
| P15        | GPIO_DISP_B2_06 | -        | IO |              |                     |               |
| P16        | GPIO_DISP_B2_07 | -        | IO |              |                     |               |
| R16        | GPIO_DISP_B2_08 | -        | IO |              |                     |               |
| R17        | GPIO_DISP_B2_09 | -        | IO |              |                     |               |
| T17        | GPIO_DISP_B2_10 | -        | IO |              |                     |               |
| U16        | GPIO_DISP_B2_11 | -        | IO |              |                     |               |
| T15        | GPIO_DISP_B2_12 | -        | IO |              |                     |               |
| U15        | GPIO_DISP_B2_13 | -        | IO |              |                     |               |
| R14        | GPIO_DISP_B2_14 | -        | IO |              |                     |               |
| T14        | GPIO_DISP_B2_15 | -        | IO |              |                     |               |
| L12        | GPIO_EMC_B1_40  | K1       | IO | GPIO_EMC_B1  | IO Muxing Options   | 1.8 V         |
| K12        | GPIO_EMC_B1_41  | L1       | IO |              |                     |               |
| K14        | GPIO_EMC_B2_00  | K2       | IO | GPIO_EMC_B2  | IO Muxing Options   | 1.8 V         |
| J12        | GPIO_EMC_B2_01  | K4       | IO |              |                     |               |
| J13        | GPIO_EMC_B2_02  | K3       | IO |              |                     |               |
| J14        | GPIO_EMC_B2_03  | R1       | IO |              |                     |               |
| H12        | GPIO_EMC_B2_04  | M1       | IO |              |                     |               |
| H14        | GPIO_EMC_B2_05  | N1       | IO |              |                     |               |
| G12        | GPIO_EMC_B2_06  | T1       | IO |              |                     |               |
| G13        | GPIO_EMC_B2_07  | M3       | IO |              |                     |               |
| F13        | GPIO_EMC_B2_08  | P1       | IO |              |                     |               |
| F14        | GPIO_EMC_B2_09  | N2       | IO |              |                     |               |
| F16        | GPIO_EMC_B2_10  | R2       | IO |              |                     |               |
| F17        | GPIO_EMC_B2_11  | L4       | IO |              |                     |               |
| E14        | GPIO_EMC_B2_12  | M4       | IO |              |                     |               |
| E15        | GPIO_EMC_B2_13  | K5       | IO |              |                     |               |
| E17        | GPIO_EMC_B2_14  | M4       | IO |              |                     |               |
| D15        | GPIO_EMC_B2_15  | L2       | IO |              |                     |               |
| D16        | GPIO_EMC_B2_16  | P2       | IO |              |                     |               |
| C16        | GPIO_EMC_B2_17  | T2       | IO |              |                     |               |
| C17        | GPIO_EMC_B2_18  | N3       | IO |              |                     |               |
| B15        | GPIO_EMC_B2_19  | U2       | IO |              |                     |               |
| B17        | GPIO_EMC_B2_20  | R3       | IO |              |                     |               |



| Module Pad | Signal          | CPU BALL                                                                                                                                                                                                                                                                                                                                                                                                                                                | IO | Group              | Description / Usage                                                              | Voltage Level |
|------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|--------------------|----------------------------------------------------------------------------------|---------------|
| A3         | GPIO_SNVS_00    | R10                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO | GPIO_SNVS          | IO Muxing Options                                                                | 1.8 V         |
| B3         | GPIO_SNVS_01    | P10                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO |                    |                                                                                  |               |
| B4         | GPIO_SNVS_02    | L9                                                                                                                                                                                                                                                                                                                                                                                                                                                      | IO |                    |                                                                                  |               |
| C4         | GPIO_SNVS_03    | M10                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO |                    |                                                                                  |               |
| D5         | GPIO_SNVS_04    | N10                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO |                    |                                                                                  |               |
| C5         | GPIO_SNVS_05    | P9                                                                                                                                                                                                                                                                                                                                                                                                                                                      | IO |                    |                                                                                  |               |
| D6         | GPIO_SNVS_06    | M9                                                                                                                                                                                                                                                                                                                                                                                                                                                      | IO |                    |                                                                                  |               |
| A5         | GPIO_SNVS_07    | R9                                                                                                                                                                                                                                                                                                                                                                                                                                                      | IO |                    |                                                                                  |               |
| B6         | GPIO_SNVS_08    | N9                                                                                                                                                                                                                                                                                                                                                                                                                                                      | IO |                    |                                                                                  |               |
| A6         | GPIO_SNVS_09    | R11                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO |                    |                                                                                  |               |
| N1         | USB1_DP         | E17                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO | USB1               | Differential Data Line USB 2.0                                                   | -             |
| M1         | USB1_DN         | E16                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO |                    | USB VBUS Detection                                                               | 5 V           |
| R1         | USB1_VBUS       | D17                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  | USB2               | Differential Data Line USB 2.0                                                   | -             |
| R2         | USB2_DP         | C17                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO |                    | USB VBUS Detection                                                               | 5 V           |
| P2         | USB2_DN         | C16                                                                                                                                                                                                                                                                                                                                                                                                                                                     | IO |                    |                                                                                  |               |
| T1         | USB2_VBUS       | D16                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  | MIPI CSI           | MIPI CSI Data Lane 0                                                             | 1.8 V         |
| U5         | CSI_DP0         | B11                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  |                    | MIPI CSI Data Lane 1                                                             |               |
| U6         | CSI_DN0         | A11                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  |                    | MIPI CSI Clock                                                                   |               |
| U2         | CSI_DP1         | B13                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  |                    |                                                                                  |               |
| U3         | CSI_DN1         | A13                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  |                    |                                                                                  |               |
| T3         | CSI_CKP         | B12                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  | MIPI DSI           | MIPI DSI Data Lane 0                                                             | 1.8 V         |
| T4         | CSI_CKN         | A12                                                                                                                                                                                                                                                                                                                                                                                                                                                     | I  |                    | MIPI DSI Data Lane 1                                                             |               |
| T9         | DSI_DP0         | B8                                                                                                                                                                                                                                                                                                                                                                                                                                                      | O  |                    | MIPI DSI Clock                                                                   |               |
| T10        | DSI_DN0         | A8                                                                                                                                                                                                                                                                                                                                                                                                                                                      | O  |                    |                                                                                  |               |
| T6         | DSI_DP1         | B10                                                                                                                                                                                                                                                                                                                                                                                                                                                     | O  |                    |                                                                                  |               |
| T7         | DSI_DN1         | A10                                                                                                                                                                                                                                                                                                                                                                                                                                                     | O  |                    |                                                                                  |               |
| U8         | DSI_CKP         | B9                                                                                                                                                                                                                                                                                                                                                                                                                                                      | O  | RTC                | RTC Interrupt Output Open Drain -> Pullup required                               | max 3.3 V     |
| U9         | DSI_CKN         | A9                                                                                                                                                                                                                                                                                                                                                                                                                                                      | O  |                    | RTC clock out                                                                    | 1.8 V         |
| A8         | RTC_INT#        | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | O  | Temperature Sensor | Programmable Alert Output                                                        | 1.8 V         |
| A10        | RTC_CLKOUT      | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | O  |                    |                                                                                  |               |
| G8         | TEMP_ALERT      | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | O  | EEPROM             | Customer EEPROM Write Protection Control Low / Float: Read/Write High: Read Only | 1.8 V         |
| D8         | CUST_EEPROM_WC# | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | I  |                    |                                                                                  |               |
| A13        | SE_ISO7816_IO1  | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | IO | SEC                | SEC Interface                                                                    | 1.8 V         |
| B14        | SE_ISO7816_IO2  | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | IO |                    |                                                                                  |               |
| A15        | SE_ISO7816_CLK  | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | O  |                    |                                                                                  |               |
| C13        | SE_ISO7816_RST# | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | I  |                    |                                                                                  |               |
| C14        | SE_ISO14443_LA  | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | IO |                    |                                                                                  |               |
| B12        | SE_ISO14443_LB  | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | IO |                    |                                                                                  |               |
| D12        | SE_ENA          | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | I  | Factory Test Only  | Factory Test only Do not connect                                                 | 1.8 V         |
| B11        | DNC             | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | I  |                    |                                                                                  | 3.3 V         |
| D13        | DNC             | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | P  |                    |                                                                                  | 1.8 V         |
| E12        | DNC             | -                                                                                                                                                                                                                                                                                                                                                                                                                                                       | P  |                    |                                                                                  |               |
| GND        |                 | D1, G1, L1, P1, B2, E2, H2, K2, N2, T2, C3, F3, J3, M3, R3, A4, D4, G4, L4, P4, U4, B5, E5, H5, K5, N5, T5, C6, F6, G6, M6, R6, A7, D7, G7, J7, L7, P7, U7, B8, E8, H8, N8, T8, C9, F9, G9, L9, R9, B10, E10, L10, N10, U10, A11, D11, G11, H11, J11, L11, M11, P11, T11, C12, F12, M12, R12, B13, E13, H13, K13, N13, T13, A14, D14, G14, L14, P14, U14, C15, F15, G15, H15, J15, K15, L15, M15, R15, B16, E16, G16, K16, N16, T16, D17, G17, L17, P17 |    |                    |                                                                                  |               |

IO Types: I: Input, O: Output, IO: Input / Output, P: Power

## 3.2 System components

### 3.2.1 i.MX RT1170

#### 3.2.1.1 i.MX RT1170 derivatives

Depending on the TQMa117xL version, one of the following i.MX RT1170 derivatives is assembled.

Table 4: i.MX RT1170 derivatives

| i.MX RT1170 derivative | i.MX RT1170 clocks       | Temperature range  |
|------------------------|--------------------------|--------------------|
| i.MX RT1176            | M7: 800 MHz, M4: 400 MHz | –40 °C ... +105 °C |
| i.MX RT1175            | M7: 800 MHz, M4: 400 MHz | –40 °C ... +105 °C |
| i.MX RT1173            | M7: 800 MHz, M4: 400 MHz | –40 °C ... +105 °C |
| i.MX RT1172            | M7: 800 MHz, M4: -       | –40 °C ... +105 °C |
| i.MX RT1171            | M7: 800 MHz, M4: -       | –40 °C ... +105 °C |
| i.MX RT117T            | M7: 800 MHz, M4: 400 MHz | –40 °C ... +105 °C |
| i.MX RT117H            | M7: 800 MHz, M4: 400 MHz | –40 °C ... +105 °C |
| i.MX RT117F            | M7: 800 MHz, M4: -       | –40 °C ... +105 °C |
| i.MX RT117C            | M7: 800 MHz, M4: -       | –40 °C ... +105 °C |

Furthermore, there are differences in the range of available interfaces. These concern:

Table 5: Different interfaces of the CPU derivatives

|                             | i.MX RT1176 | i.MX RT1175 | i.MX RT1173 | i.MX RT1172 | i.MX RT1171 | i.MX RT117T | i.MX RT117H | i.MX RT117F | i.MX RT117C |
|-----------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Parallel LCD and CSI        | Yes         | -           | Yes         | Yes         | -           | Yes         | Yes         | Yes         | Yes         |
| MIPI DSI and CSI            | Yes         | -           | Yes         | Yes         | -           | Yes         | Yes         | Yes         | Yes         |
| GPU2D                       | Yes         | -           | Yes         | Yes         | -           | Yes         | Yes         | Yes         | Yes         |
| PXP                         | Yes         | -           | Yes         | Yes         | -           | Yes         | Yes         | Yes         | Yes         |
| CAN-FD                      | x3          | x3          | x3          | x3          | x3          | x3          | x3          | x3          | x3          |
| 1 Gb ENET with AVB          | x1          | x1          | x1          | x1          | x1          | x1          | x1          | x1          | x1          |
| 1 Gb ENET with TSN          | x1          | -           | -           | -           | -           | x1          | x1          | -           | -           |
| 10/100 Mb ENET with 1588    | x1          | x1          | x1          | x1          | x1          | x1          | x1          | x1          | x1          |
| Tamper                      | -           | -           | Yes         | -           | -           | -           | -           | -           | -           |
| Face/Gesture Recognition    | -           | -           | -           | -           | -           | Yes         | Yes         | Yes         | -           |
| Smart Voice                 | -           | -           | -           | -           | -           | Yes         | Yes         | -           | Yes         |
| Additional language support | -           | -           | -           | -           | -           | Yes         | -           | -           | -           |

With regard to the different CPU variants, no individual adjustments have to be made on the module itself. All variants are 1:1 compatible, the muxing can be adapted via software.

#### 3.2.1.2 i.MX RT1170 errata

Attention: Destruction or malfunction, i.MX RT1170 errata



Please take note of the current i.MX RT1170 errata (5).



### 3.2.1.3 Boot modes

The i.MX RT117x boots in four different ways:

- In "Internal Boot" mode, the boot source / configuration is read in via the GPIOs BOOT\_CFG. This mode is recommended for the development phase.
- In "Serial Downloader" mode, a program image can be loaded into the on-chip RAM via UART or USB.
- The "Boot from Fuses" mode corresponds to the Internal Boot Mode, except that not the GPIOs are read in, but the blown fuses. The GPIO pin strapping is ignored. This mode is recommended for series production.
- The fourth mode is reserved for NXP use.

The boot mode is selected based on the binary value stored in the internal BOOT\_MODE register. The BOOT\_MODE register is initialized by sampling the BOOT\_MODE0 and BOOT\_MODE1 inputs on the rising edge of POR\_B. After these inputs are sampled, their subsequent state does not affect the contents of the internal BOOT\_MODE register.

The state of the internal BOOT\_MODE register may be read from the BMOD[1:0] field of the SRC Boot Mode Register (SRC\_SBMR2). See this table for settings:

Table 6: Boot\_Mode

| Boot_Mode[1:0] | Boot Type         |
|----------------|-------------------|
| 00             | Boot from fuses   |
| 01             | Serial downloader |
| 10             | Internal boot     |
| 11             | Reserved          |

More information about the boot flow can be found in the Reference Manual (1) and the Data Sheet (2) of the i.MX RT1170.

### 3.2.1.4 Boot configuration

The following boot sources are supported by TQMa117xL:

- NOR Flash via FlexSPI
- SD Card via SDHC1
- eMMC via SDHC2 (no eMMC is installed on the TQMa117xL)

In general, the boot source is set via pin strapping using the BOOT\_CFG signals:

Table 7: BOOT\_CFG [7:4] for boot device selection

| BOOT_CFG[7:4] | Boot device                  |
|---------------|------------------------------|
| 0000b         | Serial NOR boot via FlexSPI  |
| 01xxb         | SD Boot via uSDHC            |
| 10xxb         | eMMC/MMC boot via uSDHC      |
| 001xb         | SLC NAND boot via SEMC       |
| 11xxb         | Serial NAND boot via FlexSPI |



The BOOT\_CFG [7:4] bits only represent a rough preselection of the boot source. Overall, BOOT\_CFG [11:0] must be set correctly, which varies depending on the preselection via BOOT\_CFG [7:4]:

Table 8: BOOT\_CFG[11:0] for boot configuration

| Boot_CFG[x] | FlexSPI – Serial NOR                                                                                                                                                               | SD Card via SDHC1                                                                   | eMMC via SDHC2                                                                                 |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------|
| 11          | FLEXSPI_INSTANCE<br>0 – FLEXSPI1<br>1 – FLEXSPI2                                                                                                                                   | Reserved                                                                            | Reserved                                                                                       |
| 10          | xSPI_FLASH_TYPE<br>000 – Boot with default 0x03 Read Enabled<br>001 – Reserved<br>010 – HyperFLASH 1V8<br>011 – HyperFLASH 3V0<br>100 – MXIC Octal Read<br>101 – Micron Octal Read | Reserved                                                                            | Bus Width:<br>00 – 4-bit<br>01 – 8-bit<br>10 – 4-bit DDR (MMC 4.4)<br>11 – 8-bit DDR (MMC 4.4) |
| 9           |                                                                                                                                                                                    | Bus Width:<br>0 – 1-bit<br>1 – 4-bit                                                |                                                                                                |
| 8           |                                                                                                                                                                                    | Reserved                                                                            | SD2_VOLTAGE_SELECTION:<br>0 – 3.3V<br>1 – 1.8V                                                 |
| 7           | 0                                                                                                                                                                                  | 0                                                                                   | 1                                                                                              |
| 6           | 0                                                                                                                                                                                  | 1                                                                                   | 0                                                                                              |
| 5           | 0                                                                                                                                                                                  | SD/SDXC Speed:<br>00 – Normal/SDR12<br>01 – High/SDR25<br>10 – SDR50<br>11 – SDR104 | SD/MMC Speed:<br>0 – Normal<br>1 – High                                                        |
| 4           | 0                                                                                                                                                                                  |                                                                                     | Fast Boot Acknowledge enable:<br>0 – Boot Ack disabled<br>1 – Boot Ack enabled                 |
| 3           | FLASH_PROBE_TYPE<br>00 – QuadSPI NOR<br>01 – MXIC Octal<br>10 – Micron Octal<br>11 – Adesto Octal                                                                                  | SD Power Cycle Enable:<br>0 – No power cycle<br>1 – Enabled via USDHC_RST pad       | SD Power Cycle Enable:<br>0 – No power cycle<br>1 – Enabled via USDHC_RST pad                  |
| 2           |                                                                                                                                                                                    | SD Loopback Source Sel: (for SDR50 and SDR104 only)<br>0 – through SD<br>1 – direct | SD Loopback Source Sel: (for SDR50 and SDR104 only)<br>0 – through SD<br>1 – direct            |
| 1           | ENCRYPT_XIP_EN<br>0 – Disabled<br>1 – Enabled                                                                                                                                      | Port Select:<br>0 – eSDHC1                                                          | Port Select:<br>1 – eSDHC2                                                                     |
| 0           | FLASH_AUTO_PROBE_EN<br>0 – Disabled<br>1 – Enabled                                                                                                                                 | Reserved                                                                            | Fast Boot:<br>0 – Regular<br>1 – Fast Boot                                                     |

The Boot\_CFG can be set on the MBa117xL via multiple 4-fold DIP switches. The boot mode eMMC via SDHC2 is not supported on the MBa117xL.

### 3.2.2 Memory

The RT117x CPU has these external memory interfaces and controllers:

- Smart External Memory Controller (SEMC)
- eSD/eMMC/SDIO Interface
- Flexible Serial Peripheral Interface (FlexSPI)

#### 3.2.2.1 LPSDRAM

The RT117x CPU has a "Smart External Memory Controller" (SEMC). The SEMC is a multi-standard memory controller optimized for both high-performance and low pin-count. It can support multiple external memories in the same application with shared address and data pins. The SEMC is used to connect SDRAM in 16 bit mode and supports memory region #0 as CS0 device.

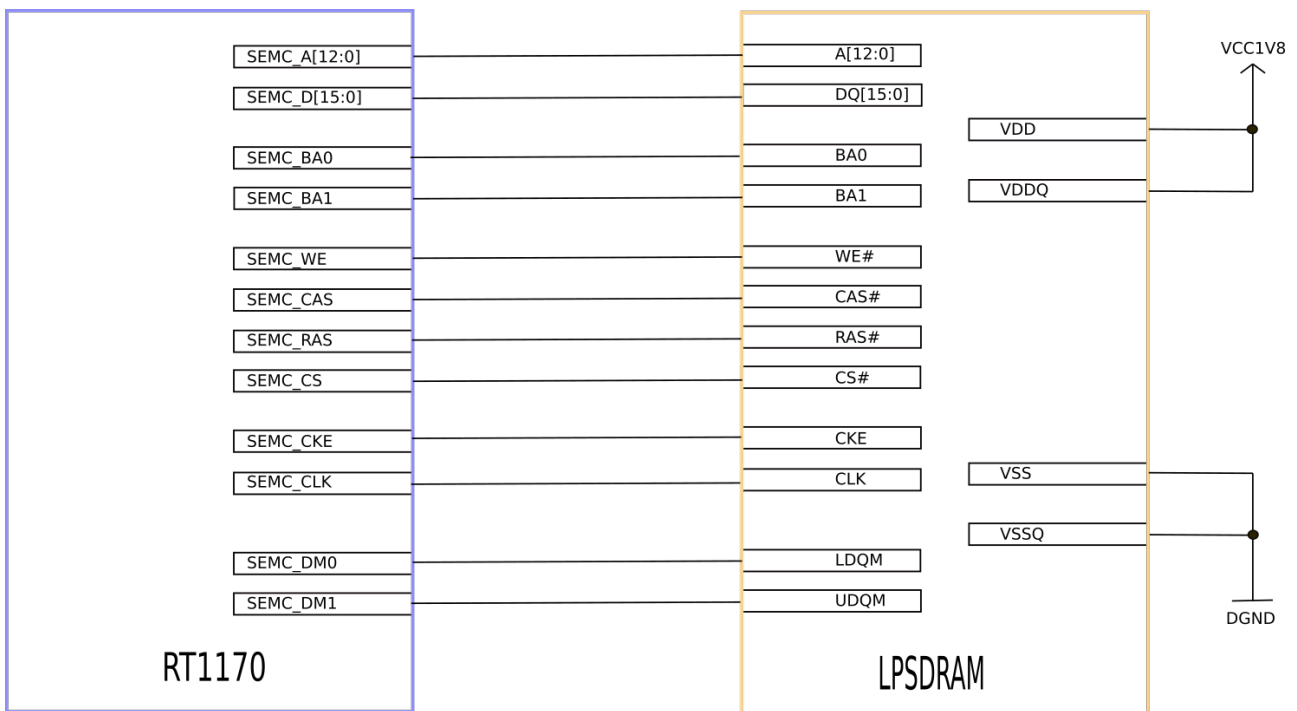


Figure 3: The LPSDRAM CPU connection

Minimum placement:

- 128 Mbit (16 MByte)
- Performance 133 MHz or 166 MHz

Maximum placement:

- 512 Mbit (64 MByte)
- Performance 133 MHz or 166 MHz

Note: Different memory manufacturers use different terms and notations for LPSDRAM:

- LP-SDRAM,
- Low Power SDRAM
- Mobile SDRAM

Table 9: Supported LPSDRAM

| Manufacturer | Part number  | Size     | Temperature range |
|--------------|--------------|----------|-------------------|
| Winbond      | W988D6FBGX6I | 256 Mbit | -40° C to +85° C  |
| Winbond      | W989D6DBGX6I | 512 Mbit | -40° C to +85° C  |

### 3.2.2.2 NOR Flash

A QSPI NOR flash is connected to FlexSPI1. It is bootable.

Maximum clock frequency = 133 MHz

Possible memory expansion:

- Standard variant: 16 MByte (128 MBit)
- Maximum expansion: 256 MByte (2 GBit)

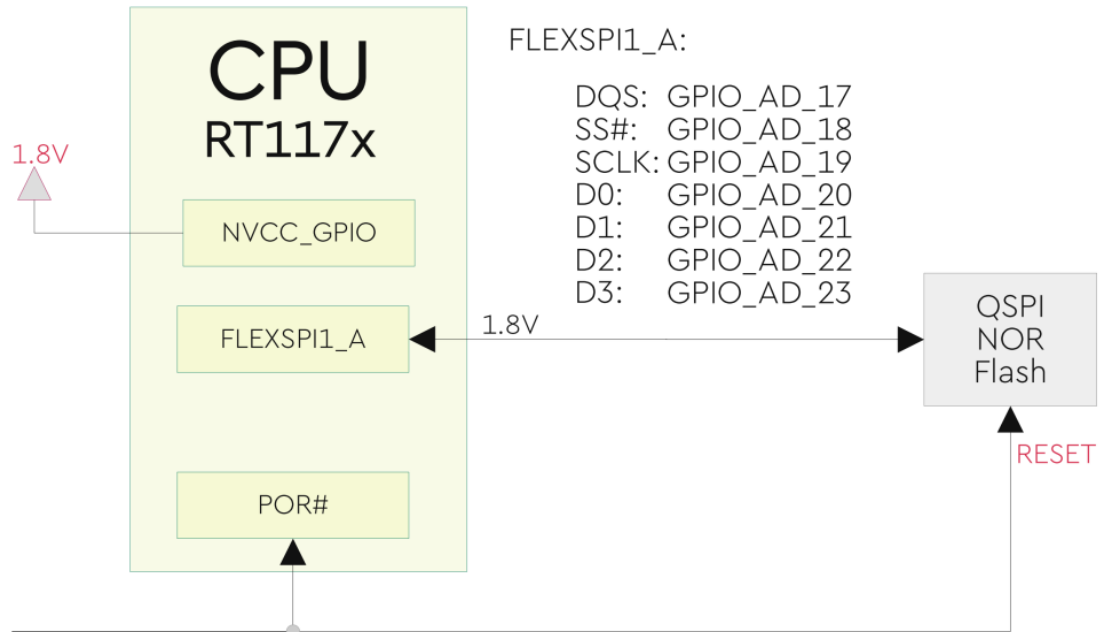


Figure 4: The NOR flash connection

The FLEXSPI1\_DQS signal is floating on the module. (Recommendation from NXP)

### 3.2.2.3 EEPROM

As usual with TQ modules, an I<sup>2</sup>C EEPROM is provided. Here it must be distinguished for whom this should typically be accessible.

- Customer data, freely accessible
- TQ production data (Serial number, MAC, ...)

The EEPROM is accessible via I2C\_6.

Table 10: EEPROM I<sup>2</sup>C addresses

| Part number    | Size              | Purpose       | I <sup>2</sup> C address (7 bit) |
|----------------|-------------------|---------------|----------------------------------|
| M24C64-DFMC6TG | 64 Kbit           | Customer data | 0x54                             |
|                | 32 Byte (ID Page) | TQ data       | 0x5C                             |

The write protection of the EEPROM for TQ data is accessible via LGA pad.

### 3.2.3 Trust Secure Element SE050

As an optional component, an NXP Trust Secure Element SE050 can be fitted on the TQMa117xL.

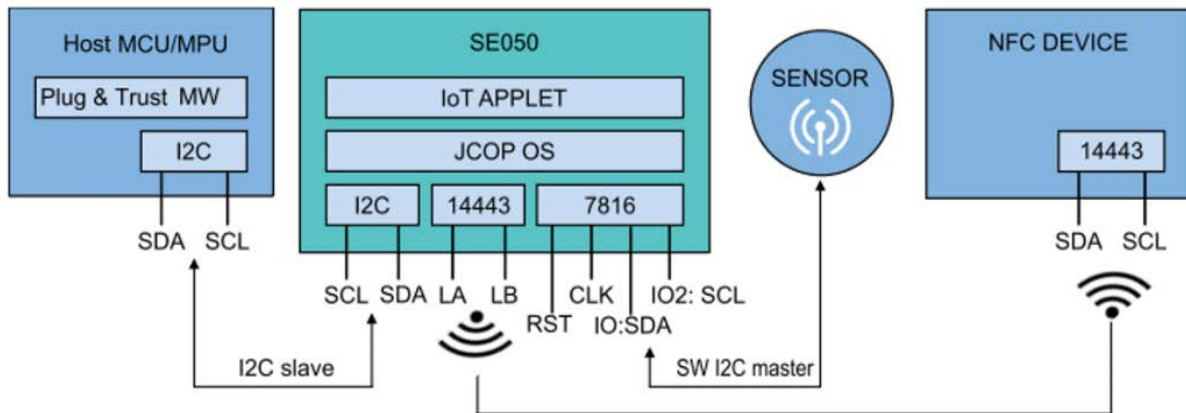


Figure 5: SEC connectivity (Source: NXP)

The Secure Element Chip (SEC) is fully accessible via LGA pads (see Table 3). The I<sup>2</sup>C slave address (7 bit) of the SEC is 0x48. All I<sup>2</sup>C slave addresses are summarised in chapter 3.2.6.1.

For more information about the SEC, see NXP EdgeLock SE050 Data Sheet (6) and User Guide (7).

### 3.2.4 RTC

For higher precision and more favourable power consumption, the external RTC PCF85063 is provided on the TQMa117xL. RTC\_INT# is implemented as open drain output and available via LGA pad. RTC\_CLKOUT is also available via LGA pad.

The specified voltage requires special attention: While VDD should be designed for operation with a battery via VBAT (typ. 3.0 V), the I<sup>2</sup>C IO voltage must be compatible for 1.8 V. To meet these constraints, a special RTC power supply is used on the TQMa117xL. It is comprised of an LDO, the NCP171. This LDO enables a distinction between normal operation and eco mode.

### 3.2.5 Temperature sensor with EEPROM

The RT117x CPU has an internal temperature sensor. The Reference Manual describes:

- Temperature Alarm Interrupts to indicate if temperature is beyond the programmed thresholds.
- Three tier alarms supported viz., Low, High and Panic.
- Single and Continuous Measurement Mode

The additional temperature sensor SE97BTP is assembled on the TQMa117xL and controlled by the I2C6 bus. The overtemperature output TEMP\_ALERT# of the SE97BTP is connected as open drain to TQMa117xL pad G8. The device is assembled on the top side of the TQMa117xL (component D6).

The SE97BTP provides also a serial EEPROM. The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write-Protected mode (PWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage.

- The device provides the following I2C6 addresses:
  - EEPROM (Read/Write): 0x53 / 101 0011b
  - EEPROM (Protection command): 0x33 / 011 0011b
  - Temperature sensor: 0x1B / 001 1011b

### 3.2.6 Interfaces

The i.MX RT1170 CPU has numerous interface modules, some of which are multiplexed and therefore not available simultaneously. For more information, see the i.MX RT1170 reference manual (1) and data sheet (2). The following interfaces are provided by the TQMa117xL as default:

Table 11: Interfaces

| Interface        | Number            | Purpose         | Note                                  |
|------------------|-------------------|-----------------|---------------------------------------|
| I <sup>2</sup> C | 1                 | General purpose | 2 to 5 slaves integrated on TQMa117xL |
| JTAG / SWD       | 1                 | Debug           |                                       |
| GPIO             | Depends on muxing | General purpose |                                       |
| MIPI CSI         | 1                 | Camera          |                                       |
| MIPI DSI         | 1                 | Display         |                                       |
| UART             | 1                 | Debug console   |                                       |
| USB              | 2                 | General purpose | Integrated PHYs                       |

#### 3.2.6.1 I<sup>2</sup>C

The accessible I<sup>2</sup>C buses depend on the pin multiplexing. I2C\_6 of the i.MX RT1170 CPU has relatively few alternative functions, so it is intended as a fixed I<sup>2</sup>C bus and on-module devices are connected to it. It is routed to the LGA pads J6 and H6 of the TQMa117xL.

The following figure shows the signals used by the I<sup>2</sup>C interfaces.

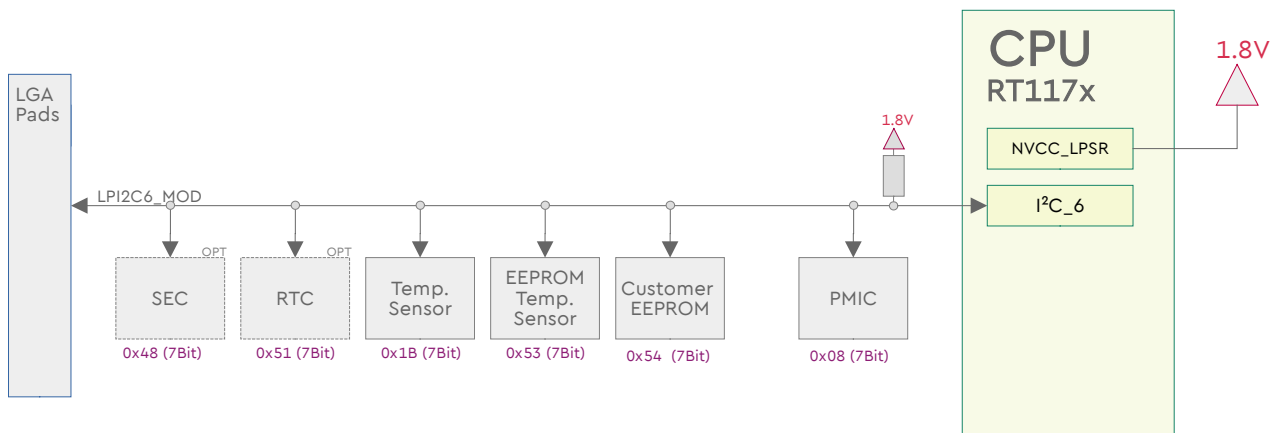


Figure 6: I<sup>2</sup>C bus structure

The following table shows the I<sup>2</sup>C devices controlled by the I2C\_6 bus on the TQMa117xL.

Table 12: Address assignment I2C\_6 bus

| Component      | Function                     | 7-bit address    |
|----------------|------------------------------|------------------|
| MPF5020AVNA0ES | PMIC                         | 0x08 / 000 1000b |
| SE050          | SEC (optional)               | 0x48 / 100 1000b |
| SE97BTP        | Temperature sensor           | 0x1B / 001 1011b |
|                | EEPROM TQ data (Read/Write)  | 0x53 / 101 0011b |
|                | EEPROM (Protection command)  | 0x33 / 011 0011b |
| PCF85063ATL    | RTC (optional)               | 0x51 / 101 0001b |
| M24C64-DFMC6TG | 64 Kbit EEPROM customer data | 0x54 / 101 0100b |

If more devices are connected to the I2C\_6 bus on the carrier board, the maximum capacitive bus load according to the I<sup>2</sup>C standard has to be taken note of. Optional external pullups should be provided to improve the rise/fall times.

LPI2C6\_MOD relates to NVCC\_LPSR, which is supplied with 1.8V.

### 3.2.6.2 JTAG /SWD

The CPU supports both the SWD and the JTAG interface. The double assignment is:

- SWD\_CLK = JTAG\_CLK
- SWD\_DIO = JTAG\_TMS

For the TQMa117xL module, the JTAG interface is mainly considered as a whole.

The following wiring is proposed here:

Table 13: JTAG interface termination

| JTAG signals | IO type        | On-chip termination | External termination                                     | i.MX RT1170 | TQMa117xL |
|--------------|----------------|---------------------|----------------------------------------------------------|-------------|-----------|
| JTAG_TCK     | Input          | 20-50 kΩ pull-down  | Not required                                             | T6          | F10       |
| JTAG_TMS     | Input          | 20-50 kΩ pull-up    | Not required, can use 10 kΩ pull-up                      | U7          | C10       |
| JTAG_TDI     | Input          | 20-50 kΩ pull-up    | Not required, can use 10 kΩ pull-up                      | U5          | C11       |
| JTAG_TDO     | 3-state output | None                | Do not use pull-up or pull-down                          | T5          | E11       |
| JTAG_TRST#   | Input          | 20-50 kΩ pull-up    | 4.7 kΩ pull-down is recommended for mass production      | R5          | F11       |
| JTAG_MOD     | Input          | 20-50 kΩ pull down  | 4.7 kΩ pull-down is already implemented on the TQMa117xL | U6          | D10       |

The JTAG interface of the RT1170 is subject to the NVCC\_LPSR bank supply. This is designed to be fixed at 1.8V.

For further JTAG design recommendation please refer to the Hardware Developer's Guide (3).

### 3.2.6.3 GPIO

Except for the dedicated differential signals, e.g., MIPI DSI/CSI, and USB, all CPU signals routed to the TQMa117xL LGA pads can be configured as GPIO. Please refer to Table 2 and Table 3.

The electrical characteristics of the GPIOs are to be taken from the i.MX RT1170 Data Sheet (2).

### 3.2.6.4 MIPI CSI

The i.MX RT1170 provides a MIPI-CSI camera interface with two data pairs. The maximum bit rate is 1.5 Gbps per lane (high speed mode). In addition there is low power mode with a 10 Mbps data rate.

The differential signals are length matched on the TQMa117xL and routed with a differential impedance of 100 Ω.

### 3.2.6.5 MIPI DSI

The i.MX RT1170 provides a DSI interface with two data pairs to output serial display data and supports High Speed and Low Power operation.

The differential signals are length matched on the TQMa117xL and routed with a differential impedance of 100 Ω.

### 3.2.6.6 UART

The TQMa117xL provides LPUART1 for a debug console. LPUART1\_TXD is routed to pad K7 and LPUART1\_RXD is routed to pad K6 of the TQMa117xL. (see Table 2 and Table 3)

In total the i.MX RT1170 CPU provides up to 12 UART interfaces (LPUART1...LPUART12). Each of the UART modules support the following serial data transmit/receive protocols and configurations:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)
- Programmable baud rates up to 20 Mbps.

The accessible UART interfaces and signals depend on the pin multiplexing. Therefore not all CPU interfaces and functions are available simultaneously.

### 3.2.6.7 USB

The i.MX RT1170 provides two USB 2.0 interfaces with integrated PHYs via USB1 and USB2. These support High-Speed (480 Mbit/s), Full-Speed (12 Mbit/s), as well as Low-Speed (1.5 Mbit/s) and offer host, device and OTG1 and OTG2 functionalities. The USB signals are provided via the LGA pads of the TQMa117xL.

### 3.2.7 Unspecific control und status signals

The following table lists all signals that are not assigned to a specific group.

ISO\_7816 and ISO\_14443 signals are only available with assembled Trust Secure Element, see chapter 3.2.3.

Table 14: Unspecific control and status signals

| Signal          | Direction | i.MX RT 1170 | TQMa117xL | Note                                    |
|-----------------|-----------|--------------|-----------|-----------------------------------------|
| PMIC_WDI        | I         | –            | K11       | 1.8 V                                   |
| MCU_Wakeup      | I         | T8           | H7        | 1.8 V                                   |
| DAC_OUT         | O         | H16          | L2        | 1.8 V                                   |
| TEMP_ALERT      | O         | –            | G8        | 1.8 V                                   |
| SE_ISO7816_IO1  | IO        | –            | A13       | Use with populated Trust Secure Element |
| SE_ISO7816_IO2  | IO        | –            | B14       |                                         |
| SE_ISO7816_CLK  | O         | –            | A15       |                                         |
| SE_ISO7816_RST# | I         | –            | C13       |                                         |
| SE_ISO14443_LA  | IO        | –            | C14       |                                         |
| SE_ISO14443_LB  | IO        | –            | B12       |                                         |
| SE_ENA          | I         | –            | D12       |                                         |
| TQMa117xL_PGOOD | O         | –            | G10       | TQMa117xL PGOOD Status                  |
| PMIC_WDI        | I         | –            | K11       | Optional PMIC Watchdog                  |

### 3.2.8 Reset / Enable

The TQMa117xL does not have a dedicated "Enable" pin. The module starts at

- Reset Release ( Hard\_Reset & Soft\_Reset)
- Automatically after VIN is valid
- via TQMa117xL\_PWR\_BTN# (Power Button) if the CPU was set in Standby Mode
- via MCU\_WAKEUP if configured correctly

The reset options are

- TQMa117xL\_HARD\_RESET#: Resets the TQMa117xL including Power Supply
- TQMa117xL\_SOFT\_RESET#: Resets only the RT1170 CPU via POR#

TQMa117xL\_RESET\_OUT# represents the RESET# condition of the TQMa117xL and is indicated by a red LED permanent on.

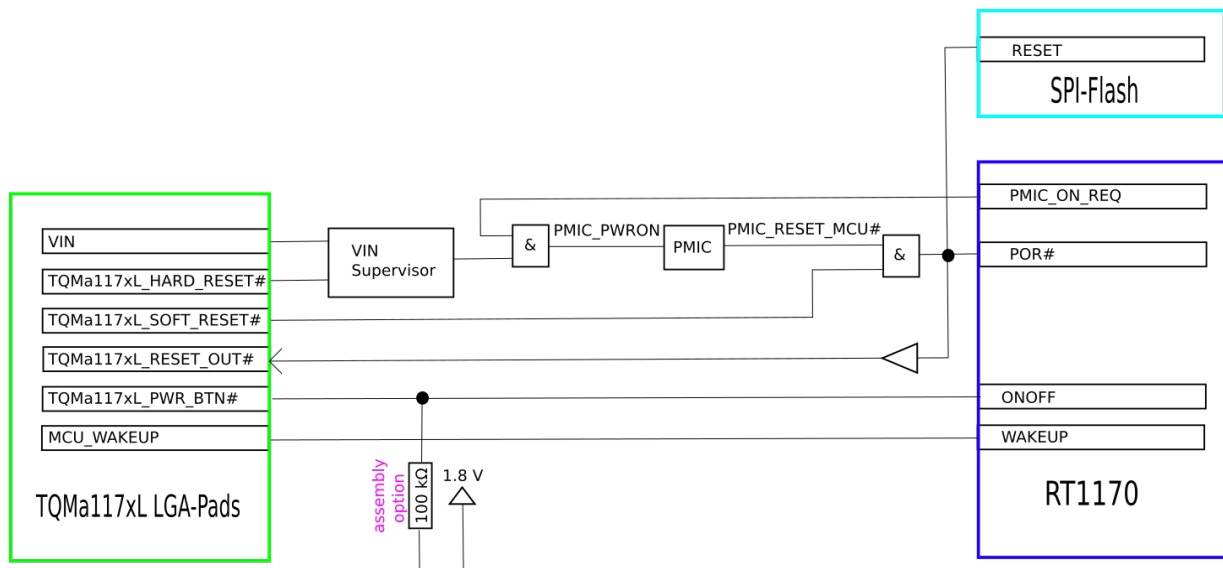


Figure 7: Reset structure

Table 15: Reset signals

| Signal                | Direction | i.MX RT 1170 | TQMa117xL               | Note                    |
|-----------------------|-----------|--------------|-------------------------|-------------------------|
| VIN                   | I         | –            | H16, H17, J16, J17, K17 | Module main power input |
| TQMa117xL_HARD_RESET# | I         | –            | A16                     | 4K7 pullup to VIN       |
| TQMa117xL_SOFT_RESET# | I         | T10          | F8                      | POR# to CPU             |
| TQMa117xL_RESET_OUT#  | O         | –            | U11                     | TQMa117xL reset status  |
| TQMa117xL_PWR_BTN#    | I         | U10          | E6                      | ONOFF control           |
| MCU_WAKEUP            | I         | T8           | H7                      | Wakeup form LP          |

### 3.2.9 Power

#### 3.2.9.1 Power supply

The TQMa117xL requires the supply voltage VIN of 5 V  $\pm$  5 %.

VBAT\_IN is an optional VDD\_SNVS supply of the MCU (2.8 V ... 3.6 V).

The SDIO supply voltage is switchable between 1.8 V and 3.3 V

The control signals are:

- PWR\_BTN: Connected directly to the MCU. Controls the ON\_OFF behaviour
- HARD\_RESET#: Low Active, triggers a reset of the module incl. power up sequencing.
- SOFT\_RESET#: Low Active, Triggers a reset of the CPU only.
- PGOOD: Status signal to the mainboard that all voltages on the module are valid.

#### 3.2.9.2 VBAT Power Supply

VBAT is an optional power supply input for the VDD\_SNVS Power Domain. It can be used if VIN is disabled in Low Power Modes. VBAT\_IN is specified: min. 2.8 V to max. 3.6 V.



Figure 8: VBAT

### 3.2.9.3 Power consumption

The TQMa117xL power consumption strongly depends on the application, the mode of operation and the operating system.

### 3.2.9.4 Supply outputs

The TQMa117xL provides three voltages that can be used on the carrier board.

Table 16: Power provided by TQMa117xL

| Power    | TQMa117xL             | Usage                             | Voltage        | Max. load | Note                                               |
|----------|-----------------------|-----------------------------------|----------------|-----------|----------------------------------------------------|
| VCC1V8   | M16, L16,<br>M17, N17 | General usage on<br>carrier board | 1.8 V $\pm$ 5% | 600 mA    | Maximum step<br>change in load<br>current is 0.5 A |
| NVCC_SD1 | P1                    | SD card supply                    | 1.8 V or 3.3 V | 20 mA     | Output Voltage<br>controlled by<br>CTRL_NVCC_SD1   |
| NVCC_SD2 | G5                    | SD card supply                    | 1.8 V or 3.3 V | 20 mA     | Output Voltage<br>controlled by<br>CTRL_NVCC_SD2   |

#### Attention: Destruction or malfunction, current exceedance



A load of up to 600 mA at VCC1V8, as well as up to 40 mA at NVCC\_SDx causes an increased power consumption of the TQMa117xL and thus a higher self-heating. These three voltages are outputs and must never be supplied from external sources! Furthermore the outputs are not short-circuit proof. Overloading the voltage outputs can damage the TQMa117xL.

### 3.2.9.5 Power-Up sequence TQMa117xL / carrier board

Since the TQMa117xL operates with 5 V and the I/O voltages of the CPU signals are generated on the TQMa117xL, there are timing requirements for the carrier board design with respect to the voltages generated on the carrier board:

After power up of the 5V supply for the TQMa117xL, the PMIC power-up sequence starts. External TQMa117xL inputs driven by the carrier board may only be switched on after the TQMa117xL provides the signal TQMa117xL\_PGOOD (LGA pad G10), indicating power good of all power rails on the TQMa117xL. It can be used to enable external power supply.

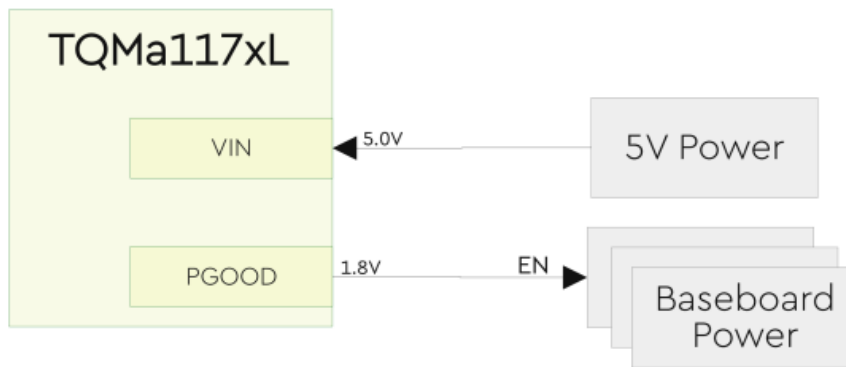


Figure 9: Block diagram power supply carrier board

**Attention: Destruction or malfunction, Power-Up sequence**

To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed.  
The end of the power-up sequence is indicated by a high level of signal TQMa117xL\_PGOOD (LGA pad G10).

**3.2.9.6 PMIC**

The properties and functions of all pins and signals can be found in the the i.MX RT1170 Reference Manual (1) and the PMIC Data Sheet (4). The PMIC is controlled by the I2C\_6 bus.

- The PMIC has the I<sup>2</sup>C address 0x08 / 000 1000b

**Attention: Destruction or malfunction, PMIC programming**

Improper programming of the PMIC may result in the i.MX RT1170 or periphery being operated outside its specification. This may lead to malfunctions, accelerated aging or destruction of the TQMa117xL.

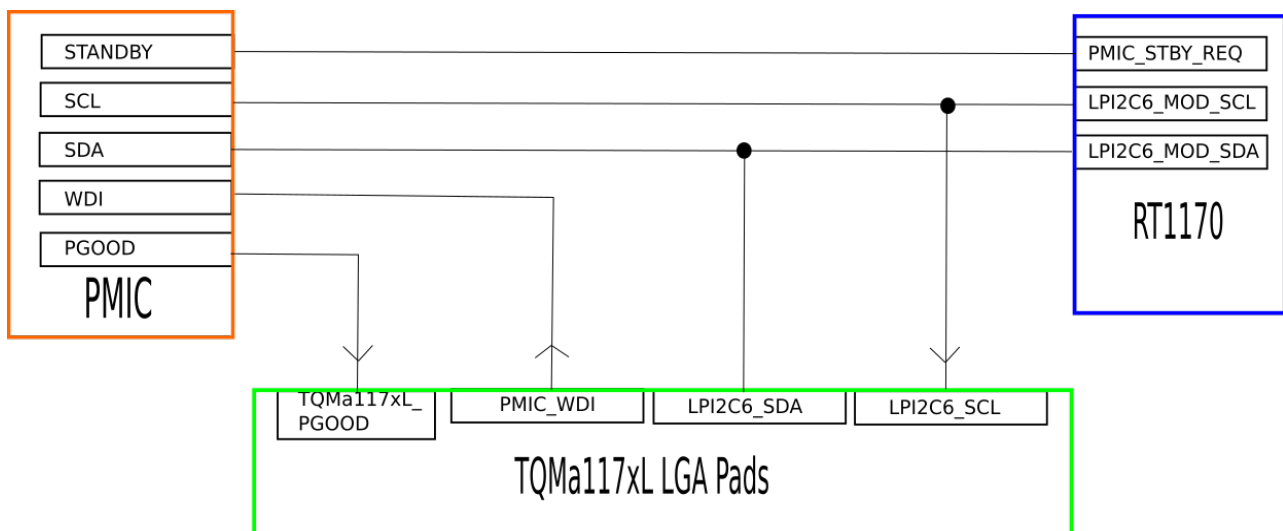


Figure 10: PMIC control structure

**3.2.10 Impedances**

Typically, all signals have a single-ended impedance of nominally 50 Ω or differentially 100 Ω with a tolerance of ±10 %.



## 4. SOFTWARE

The TQMa117xL is delivered with a preinstalled boot loader U-Boot.

The [BSP provided by](#) TQ-Systems GmbH is configured for the combination of TQMa117xL and MBa117xL.

The boot loader U-Boot provides TQMa117xL-specific as well as board-specific settings, e.g.:

- i.MX RT1170 configuration
- PMIC configuration
- Memory configuration
- Multiplexing
- Pin configuration

Further information can be found at <https://support.tq-group.com/TQMa117xL>.

If another bootloader is used, this data must be adapted. Contact [TQ-Support](#) for detailed information.

FreeRTOS is supported. More information on the operating system can be found at: <https://www.freertos.org/>

## 5. MECHANICS

### 5.1 Dimensions

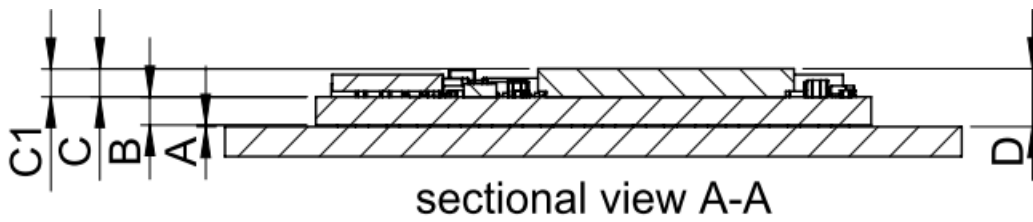


Figure 11: TQMa117xL dimensions, side view

Table 17: TQMa117xL heights

| Dim. | Value    | Tolerance | Remark                        |
|------|----------|-----------|-------------------------------|
| A    | 0.125 mm | +0.075 mm | Board to board distance       |
|      |          | -0.025 mm |                               |
| B    | 1.60 mm  | ±0.16 mm  | PCB thickness                 |
| C    | 1.47 mm  | ±0.16 mm  | Height CPU                    |
| C1   | 1.32 mm  | ±0.20 mm  | Capacitors                    |
| D    | 3.22 mm  | ±0.23 mm  | Overall height to CPU surface |

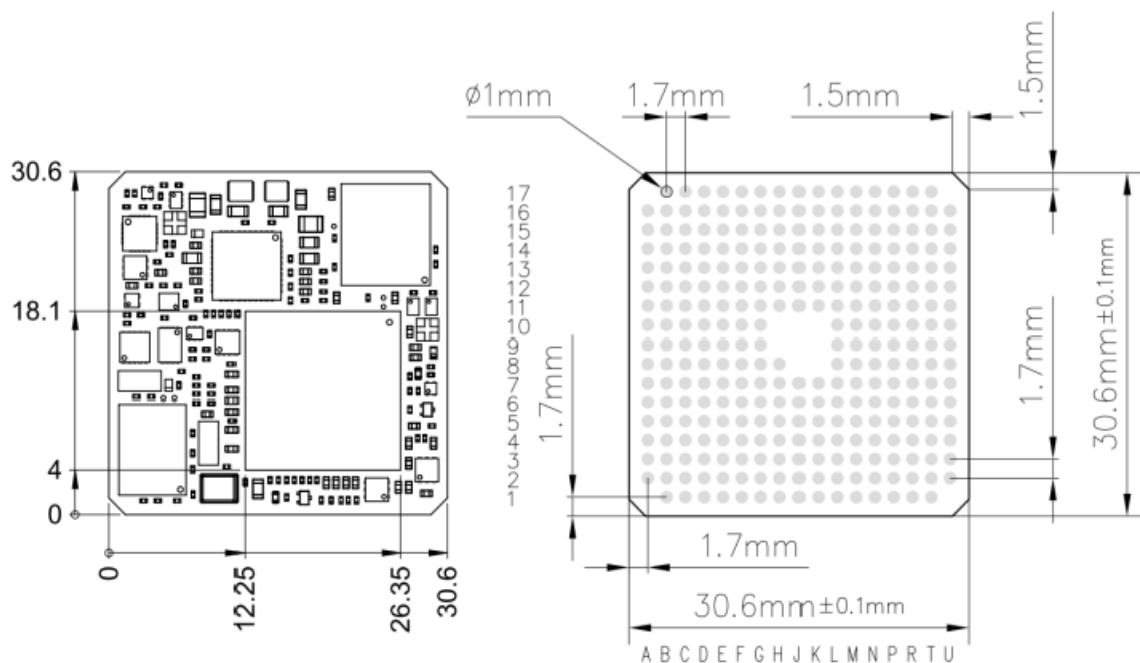


Figure 12: TQMa117xL dimensions, top view (left) and TQMa117xL dimensions, top through view

## 5.2 Component and label placement

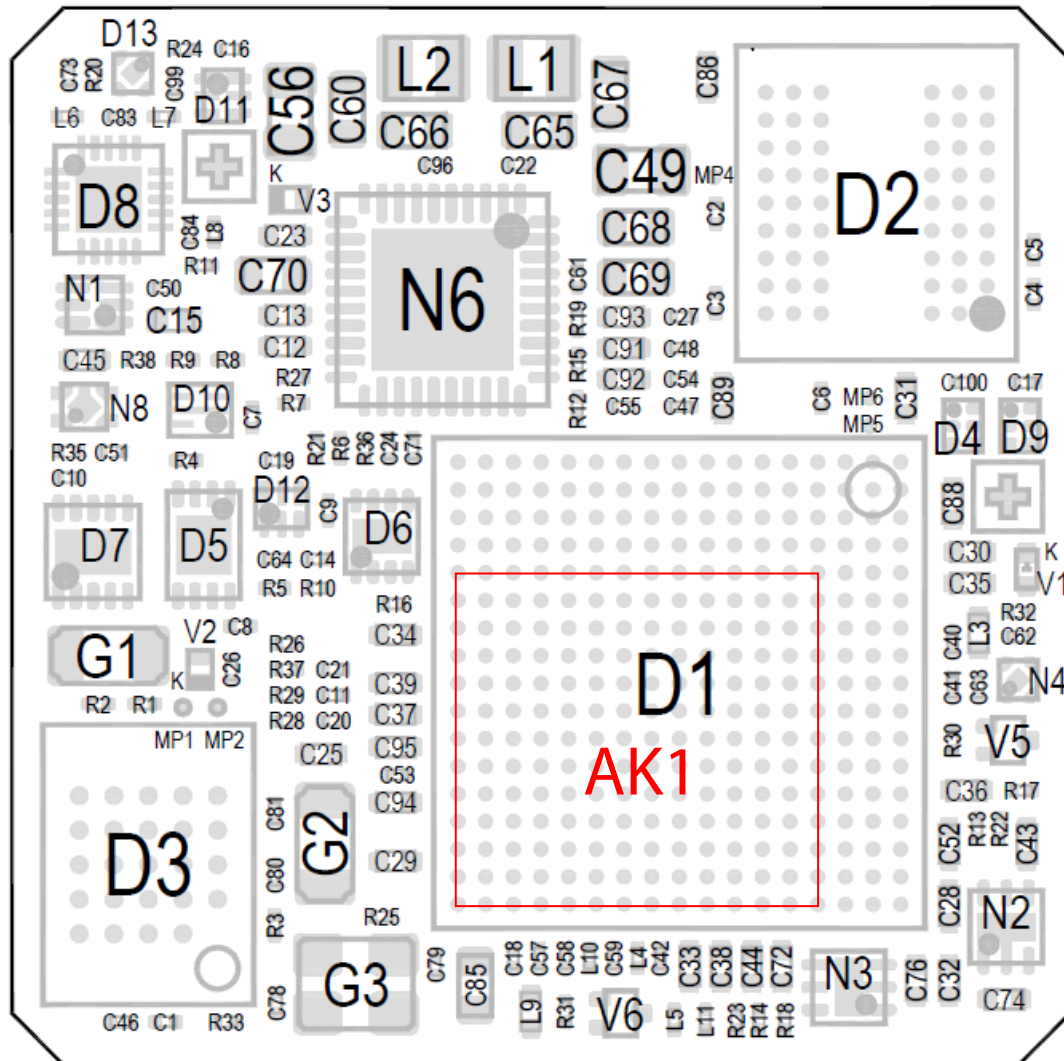


Figure 13: TQMa117xL, component and label placement top

The labels on the TQMa117xL show the following information:

Table 18: Labels on TQMa117xL

| Label | Content                                           |
|-------|---------------------------------------------------|
| AK1   | 2 x MAC addresses, TQMa117xL version and revision |

### 5.3 Adaptation to the environment

The TQMa117xL has overall dimensions (length × width) of 30.6 × 30.6 mm<sup>2</sup>.

The TQMa117xL has a maximum height above the carrier board of approximately 3.22 mm.

The TQMa117xL has 277 LGA pads with a diameter of 1.0 mm and a grid of 1.7 mm.

### 5.4 Protection against external effects

The TQMa117xL does not provide protection against dust, external impact and contact (IP00).

Adequate protection has to be guaranteed by the surrounding system.

### 5.5 Thermal management

No further cooling measures are required for the TQMa117xL at room temperature.

The customer is responsible for dissipating the power loss at higher temperatures in his application.

The power dissipation also depends on the software used and can vary according to the application.

#### Attention: Destruction or malfunction, TQMa117xL cooling



The i.MX RT1170 belongs to a performance category in which a cooling system is essential.

It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).

Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX RT1170 must be taken into consideration when connecting the heat sink. The i.MX RT1170 is not necessarily the highest component.

Inadequate cooling connections can lead to overheating of the TQMa117xL and thus malfunction, deterioration or destruction.

### 5.6 Structural requirements

The TQMa117xL has to be soldered on the carrier board. To ensure a high-quality connection of the LGA pads during reflow soldering of the TQMa117xL, the LGA pads must be free of grease and dirt.

Please contact [TQ-Support](#) for soldering instructions (10).



## 6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

### 6.1 EMC

The TQMa117xL was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short; avoid interference of other signals by distance and/or shielding, also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

### 6.2 ESD

In order to avoid interspersions on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa117xL.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

### 6.3 Operational safety and personal security

Due to the occurring voltages ( $\leq 5$  V DC), tests with respect to the operational and personal safety have not been carried out.

### 6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa117xL is only a sub-component of an overall system.

### 6.5 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ's invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

## 6.6 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

## 6.7 Climate and operational conditions

The operating temperature range for the TQMa117xL strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa117xL.

In general, a reliable operation is given when following conditions are met:

Table 19: Climate and operational conditions

| Parameter                               | Range              | Remark                |
|-----------------------------------------|--------------------|-----------------------|
| Ambient temperature TQMa117xL           | −40 °C ... +85 °C  | With suitable cooling |
| T <sub>J</sub> temperature i.MX RT1170  | −40 °C ... +105 °C | –                     |
| Case temperature other ICs              | −40 °C ... +85 °C  | –                     |
| Relative humidity (operating / storage) | 10 % ... 90 %      | Not condensing        |

### Attention: Destruction or malfunction, TQMa117xL cooling



The i.MX RT1170 belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).

Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX RT1170 must be taken into consideration when connecting the heat sink. The i.MX RT1170 is not necessarily the highest component.

Inadequate cooling connections can lead to overheating of the TQMa117xL and thus malfunction, deterioration or destruction.

## 6.8 Reliability and service life

The MTBF calculated for the TQMa117xL is 1.7 Million hours with a constant error rate @ +40 °C, Ground Benign.

The TQMa117xL is designed to be insensitive to shock and vibration.

The TQMa117xL must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.



## 7. ENVIRONMENT PROTECTION

### 7.1 RoHS

The TQMa117xL is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

### 7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa117xL was designed to be recyclable and easy to repair.

### 7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

### 7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa117xL always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa117xL on account of available Standby or Sleep-Modes of the components on the TQMa117xL.

### 7.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

### 7.6 Battery

No batteries are assembled on the TQMa117xL.

### 7.7 Packaging

The TQMa117xL is delivered in reusable packaging.

### 7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa117xL, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa117xL is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.



No PCB (polychlorinated biphenyls) containing capacitors and transformers are used.

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94  
(Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96  
(Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98  
(Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01  
(Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

## 8. APPENDIX

### 8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 20: Acronyms

| Acronym | Meaning                                             |
|---------|-----------------------------------------------------|
| ARM®    | Advanced RISC Machine                               |
| BGA     | Ball Grid Array                                     |
| BIOS    | Basic Input/Output System                           |
| BSP     | Board Support Package                               |
| CAN     | Controller Area Network                             |
| CAN-FD  | CAN with Flexible Data-Rate                         |
| CPU     | Central Processing Unit                             |
| CSI     | CMOS Sensor Interface                               |
| DDR     | Double Data Rate                                    |
| DIN     | Deutsche Industrienorm (German industry standard)   |
| DNC     | Do Not Connect                                      |
| DSI     | Display Serial Interface                            |
| EARC    | Enhanced Audio Return Channel                       |
| ECSPI   | Enhanced Configurable SPI                           |
| EEPROM  | Electrically Erasable Programmable Read-Only Memory |
| EMC     | Electromagnetic Compatibility                       |
| eMMC    | embedded Multimedia Card (Flash)                    |
| EN      | Europäische Norm (European standard)                |
| ESD     | Electrostatic Discharge                             |
| EuP     | Energy using Products                               |
| FR-4    | Flame Retardant 4                                   |
| Gbps    | Gigabit per second                                  |
| GPIO    | General Purpose Input/Output                        |
| GPT     | General-Purpose Timer                               |
| HDMI    | High-Definition Multimedia Interface                |
| I       | Input                                               |
| I/O     | Input/Output                                        |
| I2C     | Inter-Integrated Circuit                            |
| IP00    | Ingress Protection 00                               |
| IPU     | Input with Pull-Up                                  |
| JEDEC   | Joint Electronic Device Engineering Council         |
| JTAG®   | Joint Test Action Group                             |
| LGA     | Land Grid Array                                     |
| LPDDR4  | Low Power DDR4                                      |
| LVDS    | Low-Voltage Differential Signaling                  |
| MAC     | Media Access Control                                |
| MIPI    | Mobile Industry Processor Interface                 |
| ML/AI   | Machine Learning / Artificial Intelligence          |
| MMC     | Multimedia Card                                     |
| MTBF    | Mean operating Time Between Failures                |



## 8.1 Acronyms and definitions (continued)

Table 20: Acronyms (continued)

| Acronym | Meaning                                                                |
|---------|------------------------------------------------------------------------|
| NAND    | Not-And                                                                |
| NOR     | Not-Or                                                                 |
| O       | Output                                                                 |
| OD      | Open Drain                                                             |
| OOD     | Output with Open Drain                                                 |
| OTG     | On-The-Go                                                              |
| P       | Power                                                                  |
| PCB     | Printed Circuit Board                                                  |
| PCIe    | Peripheral Component Interconnect Express                              |
| PCMCIA  | People Can't Memorize Computer Industry Acronyms                       |
| PD      | Pull-Down (resistor)                                                   |
| PHY     | Physical (layer of the OSI model)                                      |
| PMIC    | Power Management Integrated Circuit                                    |
| PU      | Pull-Up (resistor)                                                     |
| PWM     | Pulse-Width Modulation                                                 |
| PWP     | Permanent Write Protected                                              |
| QSPI    | Quad Serial Peripheral Interface                                       |
| RAM     | Random Access Memory                                                   |
| RC      | Resistor-Capacitor                                                     |
| REACH®  | Registration, Evaluation, Authorisation (and restriction of) Chemicals |
| RF      | Radio Frequency                                                        |
| RGMII   | Reduced Gigabit Media Independent Interface                            |
| RMII    | Reduced Media Independent Interface                                    |
| RoHS    | Restriction of (the use of certain) Hazardous Substances               |
| ROM     | Read-Only Memory                                                       |
| RTC     | Real-Time Clock                                                        |
| RWP     | Reversible Write Protection                                            |
| SAI     | Serial Audio Interface                                                 |
| SCU     | System Control Unit                                                    |
| SD      | Secure Digital                                                         |
| SDRAM   | Synchronous Dynamic Random Access Memory                               |
| SNVS    | Secure Non-Volatile Storage                                            |
| SPDIF   | Sony-Philips Digital Interface Format                                  |
| SPI     | Serial Peripheral Interface                                            |
| SVHC    | Substances of Very High Concern                                        |
| TBD     | To Be Determined                                                       |
| UART    | Universal Asynchronous Receiver/Transmitter                            |
| UM      | User's Manual                                                          |
| USB     | Universal Serial Bus                                                   |
| uSDHC   | Ultra-Secured Digital Host Controller                                  |
| WEEE®   | Waste Electrical and Electronic Equipment                              |
| WP      | Write-Protection                                                       |



## 8.2 References

Table 21: Further applicable documents

| No.  | Name                                                                | Rev., Date         | Company             |
|------|---------------------------------------------------------------------|--------------------|---------------------|
| (1)  | i.MX RT1170 Processor Reference Manual                              | Rev. 2, Jul 2023   | <a href="#">NXP</a> |
| (2)  | i.MX RT1170 Crossover Processors Data Sheet for Industrial Products | Rev. 4, Jun 2023   | <a href="#">NXP</a> |
| (3)  | i.MX RT1170 Hardware Development Guide                              | Rev. 5, Jul 2023   | <a href="#">NXP</a> |
| (4)  | PMIC PF5020 Data Sheet                                              | Rev. 3, Sep 2021   | <a href="#">NXP</a> |
| (5)  | i.MX RT1170 Chip Errata                                             | Rev. 1.4, Apr 2023 | <a href="#">NXP</a> |
| (6)  | EdgeLock SE050 Data Sheet                                           | Rev 3.7, Oct 2022  | <a href="#">NXP</a> |
| (7)  | EdgeLock SE050 User Guide                                           | Rev 1.2, Aug 2022  | <a href="#">NXP</a> |
| (8)  | MBa117xL User's Manual                                              | – current –        | <a href="#">TQ</a>  |
| (9)  | TQMa117xL Support-Wiki                                              | – current –        | <a href="#">TQ</a>  |
| (10) | TQMa117xL Processing instructions                                   | – current –        | <a href="#">TQ</a>  |

