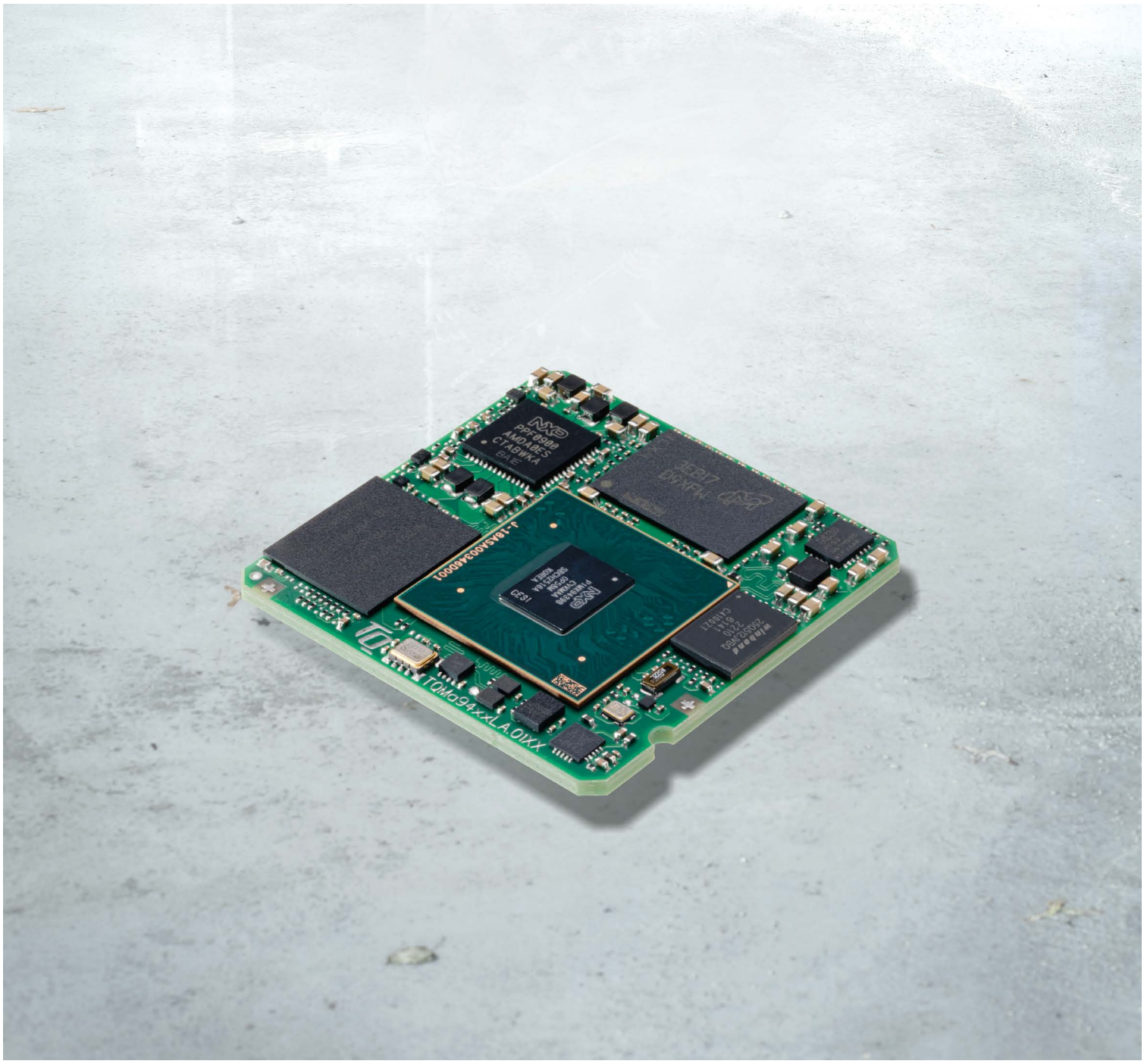
TQMa94xxLA
Preliminary User's Manual

TQMa94xxLA UM 0001
14.04.2026



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	14.04.2026	Kreuzer		Initial release

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa94xxLA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa94xxCA circuit diagram
- MBa94xxCA User's Manual
- i.MX 94 Data Sheet
- i.MX 94 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa94xxLA

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of TQMa94xxLA revision 01xx in combination with the MBa94xxCA and refers to some software settings. The MBa94xxCA serves as an evaluation board for the TQMa94xxLA. A certain TQMa94xxLA derivative does not necessarily provide all features described in this Preliminary User's Manual. This Preliminary User's Manual does also not replace the NXP i.MX 94 Reference Manual (2). The CPU derivatives provide up to four Arm Cortex-A55 cores, two Arm Cortex-M33 cores, two Arm Cortex-M7 cores and ML acceleration NPU.

The TQMa94xxLA is a universal minimodule, based on these NXP ARM® Cortex®-A55 i.MX 94 CPUs, see also Table 4.

An i.MX 94 Cortex®-A55 core typically operates up to 1.4 GHz.

2.1 Block diagram i.MX 94

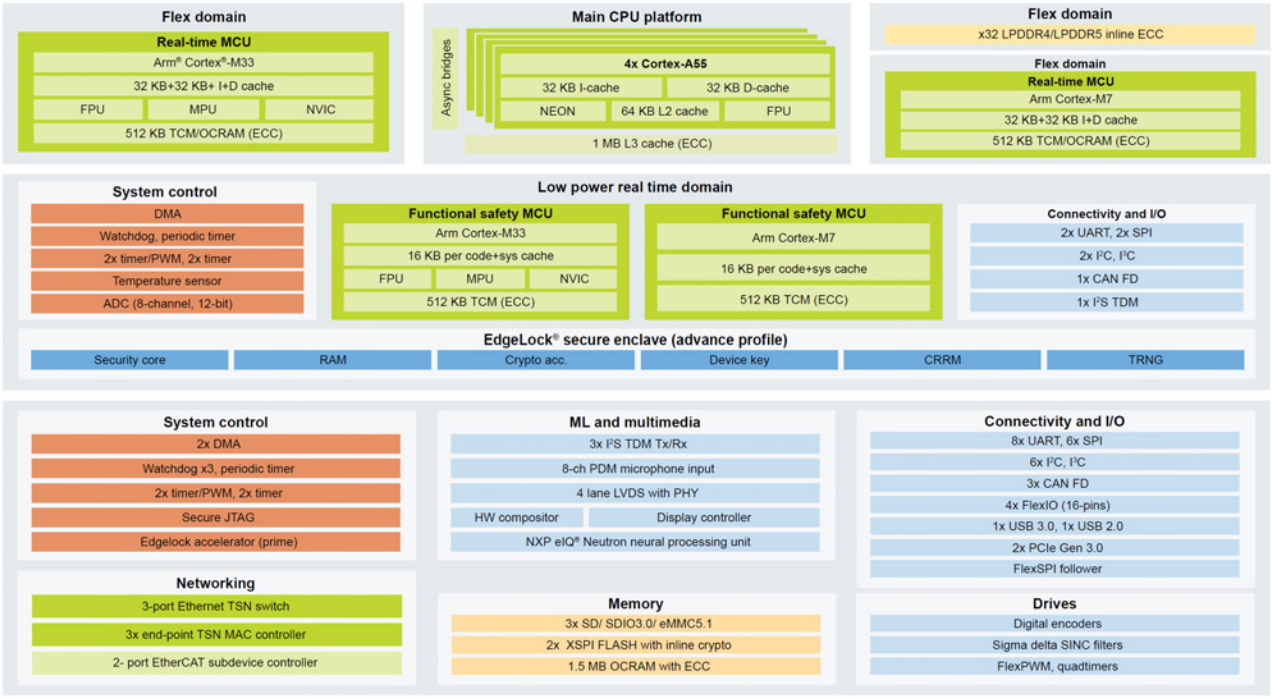

Figure 1: Block diagram i.MX 94 CPU
(Source: NXP)

2.2 Key functions and characteristics

The TQMa94xxLA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

A suitable i.MX 94 derivative can be selected for each requirement.

The signals are routed to solder pads. All essential components like CPU, LPDDR4 SDRAM and power management are already integrated on the TQMa94xxLA. The main features of the TQMa94xxLA are:

- 64-bit NXP i.MX 94 CPU with up to four ARM® Cortex®-A55
- x32 RAM in LPDDR4 version
- Quad-SPI NOR flash (optional)
- Customized EEPROM (optional)
- RTC (optional)
- Plug & Trust Secure Element (optional)
- Gyroscope (optional)

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa94xxLA and the BSP provided by TQ-Systems GmbH, see also section 5.

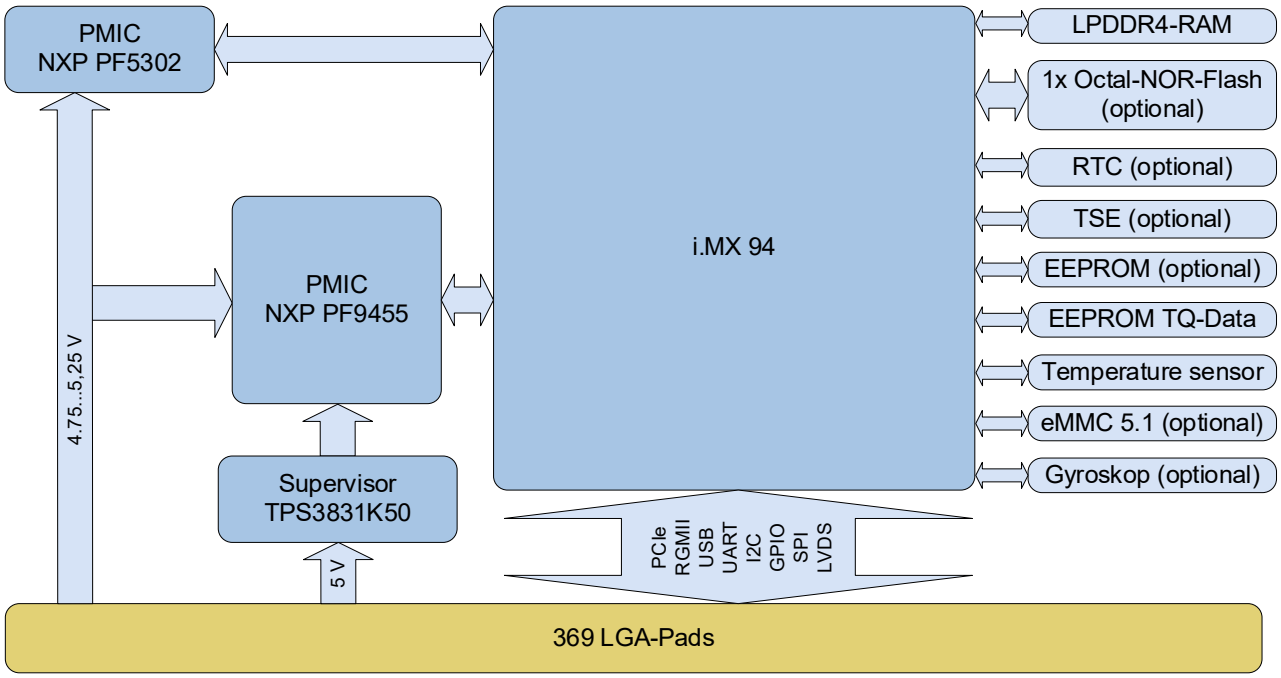

Figure 2: Block diagram TQMa94xxLA

3.1 Interfaces to other systems and devices

Except for the internal interfaces, all functional pins are routed on LGA balls. Each customer must check the suitability of the multiplexing in the respective project and adapt it if necessary.

The following table shows the possible primary interfaces of the TQMa94xxLA that can be muxed simultaneously:

Table 2: Interfaces TQMa94xxLA

i.MX 94 interface	Quantity	Remark
Internal interfaces		
DRAM	1	LPDDR4, x32
FlexSPI (NOR-Flash)	1	Default for QSPI use
USDHC1 (eMMC)	1	8 bit (HS400)
External interfaces		
ADC	1	8 x Inputs
GPIO	58	
I2C	2	1x for PMICs, 1x for other peripheries
JTAG	1	
LVDS	1	4 x diff. DATA, 1 x diff. CLK
RMII	2	
RGMII	3	
SGMII	1	
PCIe	2	1 Lane + CLK each
PDM	1	
SAI	1	
Smartcard ISO14443 / ISO7816	1	optionally provided by TSE
TAMPER	2	
UART	2	
USB	2	USB1 as USB 3.0 and USB2 as USB 2.0
SD-Card	1	4 bit

3.2 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of.
The pin assignment listed in Table 3 refers to the corresponding BSP provided by TQ-Systems GmbH in combination with the MBa94xxCA.
The electrical and pin characteristics are to be taken from the i.MX 94 Data Sheet (1), the i.MX 94 Reference Manual (2), and the PMIC Data Sheet (4) .

Attention: Destruction or malfunction	
	Depending on the configuration, many i.MX 94 balls can provide several different functions. Please take note of the information in the i.MX 94 Reference Manual (2), and the i.MX 94 Errata (3) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa94xxLA. The meanings given in the following tables must be observed: RFU: Reserved pins without function. To support future TQMa94xxLA versions, these pins must not be connected. DNC: These pins must not be connected, they have to be left open. A: Indicates an optional interface, implemented on pins shared with another use

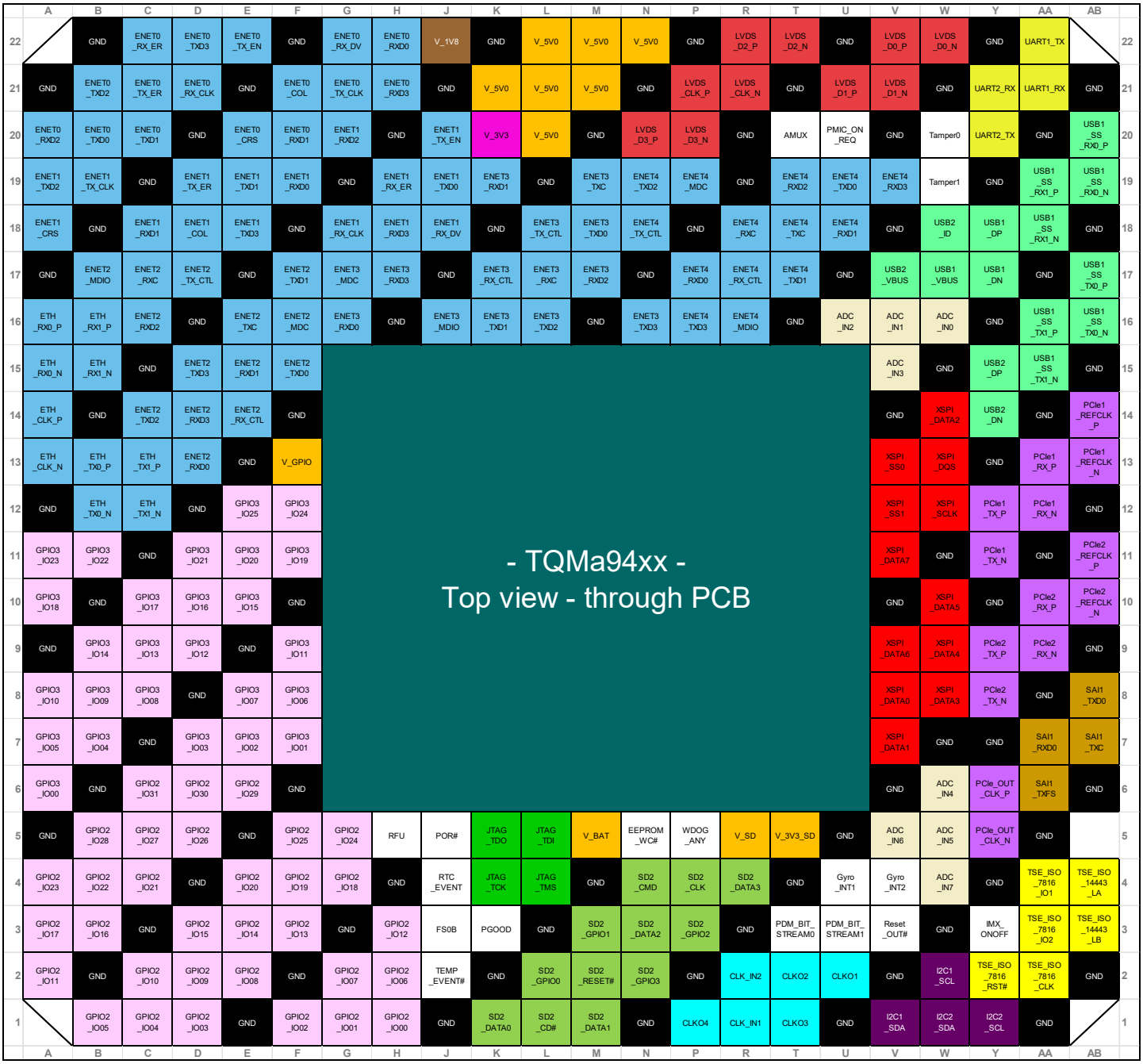

Figure 3: LGA pads layout (top view – through PCB)

3.3 LGA pads

Table 3: Pinout LGA pads

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
A1	-	Not available		-	-	
B1	GPIO2_IO05	GPIO	I/O	V_GPIO	J31	
C1	GPIO2_IO04	GPIO	I/O	V_GPIO	H30	
D1	GPIO2_IO03	GPIO	I/O	V_GPIO	K30	
E1	GND	Power	P	0 V	-	
F1	GPIO2_IO02	GPIO	I/O	V_GPIO	F32	
G1	GPIO2_IO01	GPIO	I/O	V_GPIO	J29	
H1	GPIO2_IO00	GPIO	I/O	V_GPIO	E33	
J1	GND	Power	P	0 V	-	
K1	SD2_DATA0	SD-Card	I/O	V_SD	AJ27	
L1	SD2_CD#	SD-Card	I	V_SD	AE23	
M1	SD2_DATA1	SD-Card	I/O	V_SD	AK28	
N1	GND	Power	P	0 V	-	
P1	CLKO4	CLK	O	1.8 V	AD28	
R1	CLK_IN1	CLK	I	1.8 V	H24	Already has a pull-down resistors on module
T1	CLKO3	CLK	O	1.8 V	AD30	
U1	GND	Power	P	0 V	-	
V1	I2C1_SDA	I2C	I/O	1.8 V	G25	Already has 1.8 V pull-up resistors on module
W1	I2C2_SDA	I2C	I/O	1.8 V	H26	Already has 1.8 V pull-up resistors on module
Y1	I2C2_SCL	I2C	O	1.8 V	F26	Already has 1.8 V pull-up resistors on module
AA1	GND	Power	P	0 V	-	
AB1	-	Not available		-	-	
A2	GPIO2_IO11	GPIO	I/O	V_GPIO	H32	
B2	GND	Power	P	0 V	-	
C2	GPIO2_IO10	GPIO	I/O	V_GPIO	N27	
D2	GPIO2_IO09	GPIO	I/O	V_GPIO	G33	
E2	GPIO2_IO08	GPIO	I/O	V_GPIO	D34	
F2	GND	Power	P	0 V	-	
G2	GPIO2_IO07	GPIO	I/O	V_GPIO	P26	
H2	GPIO2_IO06	GPIO	I/O	V_GPIO	F34	
J2	TEMP_EVENT#	Config	O	OD	-	Open-Drain (0.9 V to 3.6 V). External PU needed
K2	GND	Power	P	0 V	-	
L2	SD2_GPIO0	SD-Card	I/O	V_SD	AG25	
M2	SD2_RESET#	SD-Card	O	V_SD	AP28	
N2	SD2_GPIO3	SD-Card	I/O	V_SD	AM28	
P2	GND	Power	P	0 V	-	
R2	CLK_IN2	CLK	I	1.8 V	J25	Already has a pull-down resistors on module
T2	CLKO2	CLK	O	1.8 V	AC27	
U2	CLKO1	CLK	O	1.8 V	AD32	
V2	GND	Power	P	0 V	-	
W2	I2C1_SCL	I2C	O	1.8 V	K26	Already has 1.8 V pull-up resistors on module
Y2	TSE_ISO_7816_RST#	ISO_7816	I	1.8 V	-	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
AA2	TSE_ISO_7816_CLK	ISO_7816	I	1.8 V	-	
AB2	GND	Power	P	0 V	-	
A3	GPIO2_IO17	GPIO	I/O	V_GPIO	N29	
B3	GPIO2_IO16	GPIO	I/O	V_GPIO	H34	
C3	GND	Power	P	0 V	-	
D3	GPIO2_IO15	GPIO	I/O	V_GPIO	P28	
E3	GPIO2_IO14	GPIO	I/O	V_GPIO	L29	
F3	GPIO2_IO13	GPIO	I/O	V_GPIO	J33	
G3	GND	Power	P	0 V	-	
H3	GPIO2_IO12	GPIO	I/O	V_GPIO	L31	
J3	FS0B	Config	O	OD	-	Already has 1.8 V pull-up resistor on module
K3	PGOOD	Config	O	OD	-	Already has 1.8 V pull-up resistor on module
L3	GND	Power	P	0 V	-	
M3	SD2_GPIO1	SD-Card	I/O	V_SD	AN29	
N3	SD2_DATA2	SD-Card	I/O	V_SD	AL29	
P3	SD2_GPIO2	SD-Card	I/O	V_SD	AP30	
R3	GND	Power	P	0 V	-	
T3	PDM_BIT_STREAM0	PDM	I	1.8 V	D32	
U3	PDM_BIT_STREAM1	PDM	I	1.8 V	C33	Non maskable interrupt of M33 Coprocessor
V3	Reset_OUT#	Config	O	OD	F22	Open-Drain (up to 5.5 V). External PU needed
W3	GND	Power	P	0 V	-	
Y3	IMX_ONOFF	Config	I	1.8 V	K24	Already has 1.8 V pull-up resistor on module
AA3	TSE_ISO_7816_IO2	ISO_7816	I/O	1.8 V	-	
AB3	TSE_ISO_14443_LB	ISO_14443	I/O	1.8 V	-	
A4	GPIO2_IO23	GPIO	I/O	V_GPIO	N31	
B4	GPIO2_IO22	GPIO	I/O	V_GPIO	L33	
C4	GPIO2_IO21	GPIO	I/O	V_GPIO	T26	
D4	GND	Power	P	0 V	-	
E4	GPIO2_IO20	GPIO	I/O	V_GPIO	M30	
F4	GPIO2_IO19	GPIO	I/O	V_GPIO	R27	
G4	GPIO2_IO18	GPIO	I/O	V_GPIO	K34	
H4	GND	Power	P	0 V	-	
J4	RTC_EVENT	Config	O	OD	-	Open-Drain (0.7 V to 5.5 V). External PU needed
K4	JTAG_TCK	JTAG	I	1.8 V	AC29	
L4	JTAG_TMS	JTAG	I	1.8 V	AD34	
M4	GND	Power	P	0 V	-	
N4	SD2_CMD	SD-Card	I/O	V_SD	AF24	
P4	SD2_CLK	SD-Card	O	V_SD	AH26	
R4	SD2_DATA3	SD-Card	I/O	V_SD	AN31	
T4	GND	Power	P	0 V	-	
U4	Gyro_INT1	Config	O	OD / PP	-	Open-Drain or Push-Pull / active high or low
V4	Gyro_INT2	Config	O	OD / PP	-	Open-Drain or Push-Pull / active high or low
W4	ADC_IN7	ADC	I	1.8 V	A25	
Y4	GND	Power	P	0 V	-	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
AA4	TSE_ISO_7816_IO1	ISO_7816	I/O	1.8 V	-	
AB4	TSE_ISO_14443_LA	ISO_14443	I/O	1.8 V	-	
A5	GND	Power	P	0 V	-	
B5	GPIO2_IO28	GPIO	I/O	V_GPIO	N33	
C5	GPIO2_IO27	GPIO	I/O	V_GPIO	M34	
D5	GPIO2_IO26	GPIO	I/O	V_GPIO	R29	
E5	GND	Power	P	0 V	-	
F5	GPIO2_IO25	GPIO	I/O	V_GPIO	M32	
G5	GPIO2_IO24	GPIO	I/O	V_GPIO	P30	
H5	RFU	-	-	-	-	
J5	POR#	Config	I	OD	F22	Open-Drain (1.8 V or higher)
K5	JTAG_TDO	JTAG	O	1.8 V	AE33	
L5	JTAG_TDI	JTAG	I	1.8 V	AC31	
M5	V_BAT	Power	P	3 V	-	Power-Input
N5	EEPROM_WC#	Config	I	OD	-	Already has pull-up resistor on module. Keep floating
P5	WDOG_ANY	GPIO	I/O	1.8 V	E31	I/O behaviour dependent on PMIC model
R5	V_SD	Power	P	1.8 / 3.3 V	AC23, AD22	Power-Output (max. 75 mA)
T5	V_3V3_SD	Power	P	3.3 V	-	Power-Output (max. 400 mA)
U5	GND	Power	P	0 V	-	
V5	ADC_IN6	ADC	I	1.8 V	C25	
W5	ADC_IN5	ADC	I	1.8 V	F24	
Y5	PCIe_OUT_CLK_N	PCIe	O	1.8 V	B18	
AA5	GND	Power	P	0 V	-	
AB5	-	Not available		-	-	
A6	GPIO3_IO00	GPIO	I/O	V_GPIO	T30	
B6	GND	Power	P	0 V	-	
C6	GPIO2_IO31	GPIO	I/O	V_GPIO	T28	
D6	GPIO2_IO30	GPIO	I/O	V_GPIO	P34	
E6	GPIO2_IO29	GPIO	I/O	V_GPIO	R31	
F6	GND	Power	P	0 V	-	
G6, H6, J6, K6, L6, M6, N6, P6, R6, T6, U6		Not available		-	-	
V6	GND	Power	P	0 V	-	
W6	ADC_IN4	ADC	I	1.8 V	A27	
Y6	PCIe_OUT_CLK_P	PCIe	O	1.8 V	A17	
AA6	SAI1_TXC	SAI	O	1.8 V	D30	
AB6	GND	Power	P	0 V	-	
A7	GPIO3_IO05	GPIO	I/O	V_GPIO	T32	
B7	GPIO3_IO04	GPIO	I/O	V_GPIO	U31	
C7	GND	Power	P	0 V	-	
D7	GPIO3_IO03	GPIO	I/O	V_GPIO	T34	
E7	GPIO3_IO02	GPIO	I/O	V_GPIO	R33	
F7	GPIO3_IO01	GPIO	I/O	V_GPIO	U27	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
G7, H7, J7, K7, L7, M7, N7, P7, R7, T7, U7		Not available		-	-	
V7	XSPI_DATA1	XSPI	I/O	1.8 V	AL31	Not usable if module contains QSPI NOR-Flash
W7	GND	Power	P	0 V	-	
Y7	GND	Power	P	0 V	-	
AA7	SAI1_RXD0	SAI	I	1.8 V	D28	
AB7	SAI1_TXD0	SAI	O	1.8 V	F28	Used as BOOT_MODE3 at startup
A8	GPIO3_IO10	GPIO	I/O	V_GPIO	V34	
B8	GPIO3_IO09	GPIO	I/O	V_GPIO	W29	
C8	GPIO3_IO08	GPIO	I/O	V_GPIO	V30	
D8	GND	Power	P	0 V	-	
E8	GPIO3_IO07	GPIO	I/O	V_GPIO	U33	
F8	GPIO3_IO06	GPIO	I/O	V_GPIO	V28	
G8, H8, J8, K8, L8, M8, N8, P8, R8, T8, U8		Not available		-	-	
V8	XSPI_DATA0	XSPI	I/O	1.8 V	AH28	Not usable if module contains QSPI NOR-Flash
W8	XSPI_DATA3	XSPI	I/O	1.8 V	AG27	Not usable if module contains QSPI NOR-Flash
Y8	PCIe2_TX_N	PCIe	O	1.8 V	F20	
AA8	GND	Power	P	0 V	-	
AB8	SAI1_TXFS	SAI	O	1.8 V	F30	Used as BOOT_MODE2 at startup
A9	GND	Power	P	0 V	-	
B9	GPIO3_IO14	GPIO	I/O	V_GPIO	W33	
C9	GPIO3_IO13	GPIO	I/O	V_GPIO	Y34	
D9	GPIO3_IO12	GPIO	I/O	V_GPIO	W31	
E9	GND	Power	P	0 V	-	
F9	GPIO3_IO11	GPIO	I/O	V_GPIO	W27	
G9, H9, J9, K9, L9, M9, N9, P9, R9, T9, U9		Not available		-	-	
V9	XSPI_DATA6	XSPI	I/O	1.8 V	AL33	
W9	XSPI_DATA4	XSPI	I/O	1.8 V	AH30	
Y9	PCIe2_TX_P	PCIe	O	1.8 V	G21	
AA9	PCIe2_RX_N	PCIe	I	1.8 V	E21	
AB9	GND	Power	P	0 V	-	
A10	GPIO3_IO18	GPIO	I/O	V_GPIO	Y26	
B10	GND	Power	P	0 V	-	
C10	GPIO3_IO17	GPIO	I/O	V_GPIO	Y28	
D10	GPIO3_IO16	GPIO	I/O	V_GPIO	Y30	
E10	GPIO3_IO15	GPIO	I/O	V_GPIO	Y32	
F10	GND	Power	P	0 V	-	
G10, H10, J10, K10, L10, M10, N10, P10, R10, T10, U10		Not available		-	-	
V10	GND	Power	P	0 V	-	
W10	XSPI_DATA5	XSPI	I/O	1.8 V	AM32	
Y10	GND	Power	P	0 V	-	
AA10	PCIe2_RX_P	PCIe	I	1.8 V	D20	
AB10	PCIe2_REFCLK_N	PCIe	I	1.8 V	D22	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
A11	GPIO3_IO23	GPIO	I/O	V_GPIO	AC33	
B11	GPIO3_IO22	GPIO	I/O	V_GPIO	AA27	
C11	GND	Power	P	0 V	-	
D11	GPIO3_IO21	GPIO	I/O	V_GPIO	AB34	
E11	GPIO3_IO20	GPIO	I/O	V_GPIO	AA33	
F11	GPIO3_IO19	GPIO	I/O	V_GPIO	AA31	
G11, H11, J11, K11, L11, M11, N11, P11, R11, T11, U11		Not available		-	-	
V11	XSPI_DATA7	XSPI	I/O	1.8 V	AN33	
W11	GND	Power	P	0 V	-	
Y11	PCIe1_TX_N	PCIe	O	1.8 V	F18	
AA11	GND	Power	P	0 V	-	
AB11	PCIe2_REFCLK_P	PCIe	I	1.8 V	C21	
A12	GND	Power	P	0 V	-	
B12	ETH_TX0_N	ETH	O	0.8 V	AL5	
C12	ETH_TX1_N	ETH	O	0.8 V	AJ7	
D12	GND	Power	P	0 V	-	
E12	GPIO3_IO25	GPIO	I/O	V_GPIO	AB28	
F12	GPIO3_IO24	GPIO	I/O	V_GPIO	AB30	
G12, H12, J12, K12, L12, M12, N12, P12, R12, T12, U12		Not available		-	-	
V12	XSPI_SS1	XSPI	O	1.8 V	AE25	
W12	XSPI_SCLK	XSPI	O	1.8 V	AK30	
Y12	PCIe1_TX_P	PCIe	O	1.8 V	E19	
AA12	PCIe1_RX_N	PCIe	I	1.8 V	C19	
AB12	GND	Power	P	0 V	-	
A13	ETH_CLK_N	ETH	I/O	0.8 V	AL1	
B13	ETH_TX0_P	ETH	O	0.8 V	AK4	
C13	ETH_TX1_P	ETH	O	0.8 V	AK6	
D13	ENET2_RXD0	ENET	I	1.8 V	AM16	
E13	GND	Power	P	0 V	-	
F13	V_GPIO	Power	P	1.8 / 3.3 V	R25, U25, W25, V26	Power-Input
G13, H13, J13, K13, L13, M13, N13, P13, R13, T13, U13		Not available		-	-	
V13	XSPI_SS0	XSPI	O	1.8 V	AD24	Not usable if module contains QSPI NOR-Flash
W13	XSPI_DQS	XSPI	O	1.8 V	AF26	
Y13	GND	Power	P	0 V	-	
AA13	PCIe1_RX_P	PCIe	I	1.8 V	D18	
AB13	PCIe1_REFCLK_N	PCIe	I	1.8 V	B20	
A14	ETH_CLK_P	ETH	I/O	0.8 V	AM2	
B14	GND	Power	P	0 V	-	
C14	ENET2_TXD2	ENET	O	1.8 V	AH18	
D14	ENET2_RXD3	ENET	I	1.8 V	AP20	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
E14	ENET2_RX_CTL	ENET	I	1.8 V	AL17	
F14	GND	Power	P	0 V	-	
G14, H14, J14, K14, L14, M14, N14, P14, R14, T14, U14		Not available		-	-	
V14	GND	Power	P	0 V	-	
W14	XSPI_DATA2	XSPI	I/O	1.8 V	AJ31	Not usable if module contains QSPI NOR-Flash
Y14	USB2_DN	USB	I/O	3.3 V	F16	
AA14	GND	Power	P	0 V	-	
AB14	PCIe1_REFCLK_P	PCIe	I	1.8 V	A19	
A15	ETH_RX0_N	ETH	I	0.8 V	AP4	
B15	ETH_RX1_N	ETH	I	0.8 V	AP6	
C15	GND	Power	P	0 V	-	
D15	ENET2_TXD3	ENET	O	1.8 V	AK20	
E15	ENET2_RXD1	ENET	I	1.8 V	AP16	
F15	ENET2_TXD0	ENET	O	1.8 V	AE17	
G15, H15, J15, K15, L15, M15, N15, P15, R15, T15, U15		Not available		-	-	
V15	ADC_IN3	ADC	I	1.8 V	B26	
W15	GND	Power	P	0 V	-	
Y15	USB2_DP	USB	I/O	3.3 V	G17	
AA15	USB1_SS_TX1_N	USB	O	0.8 V	C13	
AB15	GND	Power	P	0 V	-	
A16	ETH_RX0_P	ETH	I	0.8 V	AN3	
B16	ETH_RX1_P	ETH	I	0.8 V	AN5	
C16	ENET2_RXD2	ENET	I	1.8 V	AP18	
D16	GND	Power	P	0 V	-	
E16	ENET2_TXC	ENET	O	1.8 V	AK18	
F16	ENET2_MDC	ENET	O	1.8 V	AN17	
G16	ENET3_RXD0	ENET	I	1.8 V	AL19	
H16	GND	Power	P	0 V	-	
J16	ENET3_MDIO	ENET	I/O	1.8 V	AL23	
K16	ENET3_TXD1	ENET	O	1.8 V	AF20	
L16	ENET3_TXD2	ENET	O	1.8 V	AG19	
M16	GND	Power	P	0 V	-	
N16	ENET3_TXD3	ENET	O	1.8 V	AH20	
P16	ENET4_TXD3	ENET	O	1.8 V	AH22	
R16	ENET4_MDIO	ENET	I/O	1.8 V	AH24	
T16	GND	Power	P	0 V	-	
U16	ADC_IN2	ADC	I	1.8 V	E25	
V16	ADC_IN1	ADC	I	1.8 V	B28	
W16	ADC_IN0	ADC	I	1.8 V	D26	
Y16	GND	Power	P	0 V	-	
AA16	USB1_SS_TX1_P	USB	O	0.8 V	B12	
AB16	USB1_SS_TX0_N	USB	O	0.8 V	B16	
A17	GND	Power	P	0 V	-	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
B17	ENET2_MDIO	ENET	I/O	1.8 V	AM18	
C17	ENET2_RXC	ENET	I	1.8 V	AK16	
D17	ENET2_TX_CTL	ENET	O	1.8 V	AJ17	
E17	GND	Power	P	0 V	-	
F17	ENET2_TXD1	ENET	O	1.8 V	AG17	
G17	ENET3_MDC	ENET	O	1.8 V	AM24	
H17	ENET3_RXD3	ENET	I	1.8 V	AN23	
J17	GND	Power	P	0 V	-	
K17	ENET3_RX_CTL	ENET	I	1.8 V	AL21	
L17	ENET3_RXC	ENET	I	1.8 V	AM20	
M17	ENET3_RXD2	ENET	I	1.8 V	AP22	
N17	GND	Power	P	0 V	-	
P17	ENET4_RXD0	ENET	I	1.8 V	AN25	
R17	ENET4_RX_CTL	ENET	I	1.8 V	AN27	
T17	ENET4_TXD1	ENET	O	1.8 V	AF22	
U17	GND	Power	P	0 V	-	
V17	USB2_VBUS	USB	P	5 V	H18	
W17	USB1_VBUS	USB	P	5 V	H14	
Y17	USB1_DN	USB	I/O	3.3 V	C15	
AA17	GND	Power	P	0 V	-	
AB17	USB1_SS_TX0_P	USB	O	0.8 V	A15	
A18	ENET1_CRS	ENET	I	1.8 V	AK12	
B18	GND	Power	P	0 V	-	
C18	ENET1_RXD1	ENET	I	1.8 V	AP12	
D18	ENET1_COL	ENET	I	1.8 V	AP14	
E18	ENET1_TXD3	ENET	O	1.8 V	AH16	
F18	GND	Power	P	0 V	-	
G18	ENET1_RX_CLK	ENET	I	1.8 V	AJ13	
H18	ENET1_RXD3	ENET	I	1.8 V	AM14	
J18	ENET1_RX_DV	ENET	I	1.8 V	AL13	
K18	GND	Power	P	0 V	-	
L18	ENET3_TX_CTL	ENET	O	1.8 V	AJ21	
M18	ENET3_TXD0	ENET	O	1.8 V	AE19	
N18	ENET4_TX_CTL	ENET	O	1.8 V	AK24	
P18	GND	Power	P	0 V	-	
R18	ENET4_RXC	ENET	I	1.8 V	AP24	
T18	ENET4_TXC	ENET	O	1.8 V	AJ23	
U18	ENET4_RXD1	ENET	I	1.8 V	AP26	
V18	GND	Power	P	0 V	-	
W18	USB2_ID	USB	I	1.8 V	J15	
Y18	USB1_DP	USB	I/O	3.3 V	D16	
AA18	USB1_SS_RX1_N	USB	I	0.8 V	B14	
AB18	GND	Power	P	0 V	-	
A19	ENET1_TXD2	ENET	O	1.8 V	AH14	
B19	ENET1_TX_CLK	ENET	O	1.8 V	AF14	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
C19	GND	Power	P	0 V	-	
D19	ENET1_TX_ER	ENET	O	1.8 V	AH12	
E19	ENET1_TXD1	ENET	O	1.8 V	AG15	
F19	ENET1_RXD0	ENET	I	1.8 V	AN11	
G19	GND	Power	P	0 V	-	
H19	ENET1_RX_ER	ENET	I	1.8 V	AM12	
J19	ENET1_TXD0	ENET	O	1.8 V	AF16	
K19	ENET3_RXD1	ENET	I	1.8 V	AP12	
L19	GND	Power	P	0 V	-	
M19	ENET3_TXC	ENET	O	1.8 V	AK22	
N19	ENET4_TXD2	ENET	O	1.8 V	AG21	
P19	ENET4_MDC	ENET	O	1.8 V	AK26	
R19	GND	Power	P	0 V	-	
T19	ENET4_RXD2	ENET	I	1.8 V	AL25	
U19	ENET4_TXD0	ENET	O	1.8 V	AE21	
V19	ENET4_RXD3	ENET	I	1.8 V	AL27	
W19	Tamper1	Tamper	I/O	1.8 V	H20	
Y19	GND	Power	P	0 V	-	
AA19	USB1_SS_RX1_P	USB	I	0.8 V	A13	
AB19	USB1_SS_RX0_N	USB	I	0.8 V	E15	
A20	ENET0_RXD2	ENET	I	1.8 V	AP10	
B20	ENET0_TXD0	ENET	O	1.8 V	AE13	
C20	ENET0_TXD1	ENET	O	1.8 V	AF12	
D20	GND	Power	P	0 V	-	
E20	ENET0_CRS	ENET	I	1.8 V	AK10	
F20	ENET0_RXD1	ENET	I	1.8 V	AN9	
G20	ENET1_RXD2	ENET	I	1.8 V	AL15	
H20	GND	Power	P	0 V	-	
J20	ENET1_TX_EN	ENET	O	1.8 V	AK14	
K20	V_3V3	Power	P	3.3 V	-	Power-Output (max. 500 mA)
L20	V_5V0	Power	P	5 V	-	Power-Input
M20	GND	Power	P	0 V	-	
N20	LVDS_D3_P	LVDS	O	1.8 V	A11	
P20	LVDS_D3_N	LVDS	O	1.8 V	B10	
R20	GND	Power	P	0 V	-	
T20	AMUX	Config	O	1.65 V	-	PMIC status pin - leave unconnected
U20	PMIC_ON_REQ	Config	I	1.8 V	E23	
V20	GND	Power	P	0 V	-	
W20	Tamper0	Tamper	I/O	1.8 V	J19	
Y20	UART2_TX	UART	O	1.8 V	K28	Used as BOOT_MODE1 at startup
AA20	GND	Power	P	0 V	-	
AB20	USB1_SS_RX0_P	USB	I	0.8 V	D14	
A21	GND	Power	P	0 V	-	
B21	ENET0_TXD2	ENET	O	1.8 V	AG11	

Table 3: LGA pads (continued)

Module pad	Pad name	Group	I/O	Level	CPU ball	Comment
C21	ENET0_TX_ER	ENET	O	1.8 V	AF10	
D21	ENET0_RX_CLK	ENET	I	1.8 V	AM8	
E21	GND	Power	P	0 V	-	
F21	ENET0_COL	ENET	I	1.8 V	AJ9	
G21	ENET0_TX_CLK	ENET	O	1.8 V	AJ11	
H21	ENET0_RXD3	ENET	I	1.8 V	AM10	
J21	GND	Power	P	0 V	-	
K21	V_5V0	Power	P	5 V	-	Power-Input
L21	V_5V0	Power	P	5 V	-	Power-Input
M21	V_5V0	Power	P	5 V	-	Power-Input
N21	GND	Power	P	0 V	-	
P21	LVDS_CLK_P	LVDS	O	1.8 V	G13	
R21	LVDS_CLK_N	LVDS	O	1.8 V	H12	
T21	GND	Power	P	0 V	-	
U21	LVDS_D1_P	LVDS	O	1.8 V	C11	
V21	LVDS_D1_N	LVDS	O	1.8 V	D10	
W21	GND	Power	P	0 V	-	
Y21	UART2_RX	UART	I	1.8 V	L27	
AA21	UART1_RX	UART	I	1.8 V	J27	
AB21	GND	Power	P	0 V	-	
A22	-	Not available		-	-	
B22	GND	Power	P	0 V	-	
C22	ENET0_RX_ER	ENET	I	1.8 V	AL9	
D22	ENET0_TXD3	ENET	O	1.8 V	AH10	
E22	ENET0_TX_EN	ENET	O	1.8 V	AG9	
F22	GND	Power	P	0 V	-	
G22	ENET0_RX_DV	ENET	I	1.8 V	AK8	
H22	ENET0_RXD0	ENET	I	1.8 V	AP8	
J22	V_1V8	Power	P	1.8 V	-	Power-Output (max. 500 mA)
K22	GND	Power	P	0 V	-	
L22	V_5V0	Power	P	5 V	-	Power-Input
M22	V_5V0	Power	P	5 V	-	Power-Input
N22	V_5V0	Power	P	5 V	-	Power-Input
P22	GND	Power	P	0 V	-	
R22	LVDS_D2_P	LVDS	O	1.8 V	E11	
T22	LVDS_D2_N	LVDS	O	1.8 V	F10	
U22	GND	Power	P	0 V	-	
V22	LVDS_D0_P	LVDS	O	1.8 V	F12	
W22	LVDS_D0_N	LVDS	O	1.8 V	G11	
Y22	GND	Power	P	0 V	-	
AA22	UART1_TX	UART	O	1.8 V	H28	Used as BOOT_MODE0 at startup
AB22	-	Not available		-	-	

The pin assignment listed in Table 3 refers to the corresponding BSP provided by TQ-Systems GmbH.

For information regarding I/O pins in Table 3 refer to the i.MX 94 Data Sheet (1).

3.4 i.MX 94 CPU

3.4.1 i.MX 94 derivatives

Depending on the TQMa94xxLA version, one of the following i.MX 94 derivatives is assembled.

Table 4: i.MX 94 derivatives

TQMa94xxLA variant	CPU derivative	Cortex®-A55 clock	Cortex®-M33 clock	Cortex®-M7 clock
TQMa9432LA-AA	i.MX9432	2 x 1.7 GHz	333 MHz	800 MHz
TQMa9434LA-AA	i.MX9434	4 x 1.7 GHz	333 MHz	800 MHz

3.4.2 i.MX 94 errata

Attention: Malfunction	
	Please take note of the current i.MX 94 errata (3).

3.4.3 Boot modes

Depending on the OPT fuses (eFuse) and the boot mode settings, the system boots from the selected boot source. The following interfaces are available as boot source:

- eMMC (SD1)
- QSPI-NOR Flash (FlexSPI)
- Serial downloader (USB1)
- SD card (SD2)

The i.MX 94 uses four boot signals to select the boot source, but these signals are not dedicated to this function. The levels of these signals are read in analogy to previous i.MX CPUs when the reset is disabled and must be set high or low depending on the desired boot source at read-in time.

Table 5: Boot signals

Signal (multiplexing)	CPU-Pin	Power-Group
UART1_TX (BOOT_MODE0)	[H28] UART1_TXD	NVCC_AON (1.8 V)
UART2_TX (BOOT_MODE1)	[K28] UART2_TXD	
SAI1_TXFS (BOOT_MODE2)	[F30] SAI1_TXFS	
SAI1_TXDO (BOOT_MODE3)	[F28] SAI1_TXD0	

The exact boot source configuration is shown in the following table. The i.MX 94 only supports Low Power Boot (LPB), i.e. start of the M33 core. The M33 acts as the system controller and starts the A55 cores.

Table 6: Boot source selection (boot core M33)

BOOT_MODE [3:0]	Functions
x000	LPB: Boot from Internal Fuses
x001	LPB: Serial Downloader (USB1)
x010	LPB: uSDHC1, 8-bit, 1.8 V, eMMC 5.1
x011	LPB: uSDHC2, 4-bit, SD 3.0
x100	LPB: Serial NOR (XSPI)
x101	LPB: Serial NAND (XSPI)
x110	Reserved
x111	Test Mode (for DFT ATE Test)

More information about boot interfaces and its configuration is to be taken from the i.MX 94 Data Sheet (1) and the i.MX 94 Reference Manual (2). Alternatively, an image can be loaded into the internal RAM via serial downloader.

Note: Field software updates	
	When designing a carrier board, it is recommended to have a redundant update concept for field software updates.

3.5 Memory

3.5.1 RAM

LPDDR4-RAM with a memory width of 32 bits is used on the TQMa94xxLA. The i.MX 943 supports Inline ECC.
The LPDDR memory interface has the following basic parameters:

Table 7: Parameter RAM interface

Parameter	i.MX 94
Memory type	LPDDR4
DDR timing	LPDDR4-4267
DDR clock frequenz	max. 2133 MHz
Bus width (data)	32 bit
Max. memory size	8 GByte

The standard memory size of the TQMa94xxLA is 2 GByte. Variants with 4 GByte and 8 GByte are available.

Attention: Malfunction	
	The TQMa94xxLA uses a specially developed RAM timing. Each memory expansion level requires its own RAM configuration.

3.5.2 eMMC

An eMMC is available on the TQMa94xxLA as non-volatile memory for programs and data (e.g. bootloader, operating system, application). The following figure shows the interface of the eMMC to the i.MX 94:

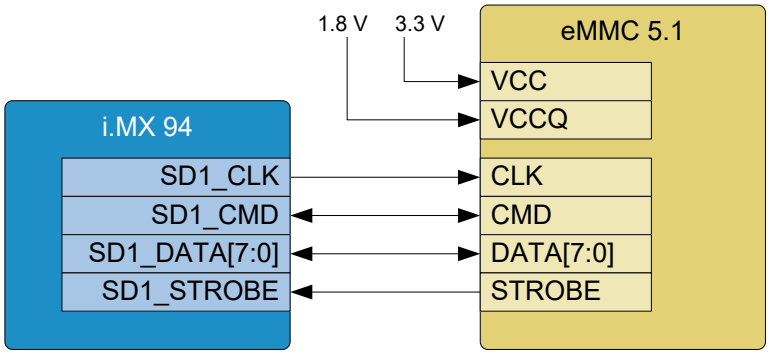

Figure 4: Block diagram eMMC

The eMMC is connected via the USDHC1 interface of the i.MX 94. A maximum transfer rate of 400 MB/s is supported, which corresponds to HS400 mode. Series resistors are provided for the CLK, DATA and CMD signals.
The standard eMMC is SanDisks SDINBDG4-16G-XI2 (16 GByte / MLC).

Table 8: Pin assignment eMMC via SD1

Signal (multiplexing)	CPU-Pin	Power-Group
SD1_CLK	[AH32] SD1_CLK	NVCC_WAKEUP (1.8 V)
SD1_CMD	[AE29] SD1_CMD	
SD1_DATA0	[AK34] SD1_DATA0	
SD1_DATA1	[AJ33] SD1_DATA1	
SD1_DATA2	[AF34] SD1_DATA2	
SD1_DATA3	[AF30] SD1_DATA3	
SD1_DATA4	[AG31] SD1_DATA4	
SD1_DATA5	[AG33] SD1_DATA5	
SD1_DATA6	[AH34] SD1_DATA6	
SD1_DATA7	[AF32] SD1_DATA7	
SD1_STROBE	[AG29] SD1_STROBE	

3.5.3 NOR Flash

With XSPI1, the CPU provides an 8-bit wide, bootable interface that can be used to connect an optional module-internal flash. QSPI NOR Flash is used here, which results in a restriction of the XSPI interface outside the TQMa94xxLA. For this reason, series resistors are provided in all data lanes.

If the NOR flash is not installed, all signals of the XSPI interface can be used outside the module. Alternatively, other memory types can be installed in the same package at this point in the module at the customer's request, for example MRAM or SRAM.

The supply voltage of the flash is 1.8 V. The standard NOR flash is Winbond W25Q512NWBIQ (64 MByte).

A second XSPI interface can be multiplexed onto the ETH4 pins, but does not serve as a boot source.

Table 9: Pin assignment NOR Flash

Signal (multiplexing)	CPU-Pin	Power-Group
XSPI1_DATA0	[AH28] XSPI1_DATA0	NVCC_WAKEUP (1.8 V)
XSPI1_DATA1	[AL31] XSPI1_DATA1	
XSPI1_DATA2	[AJ31] XSPI1_DATA2	
XSPI1_DATA3	[AG27] XSPI1_DATA3	
XSPI1_DATA4	[AH30] XSPI1_DATA4	
XSPI1_DATA5	[AM32] XSPI1_DATA5	
XSPI1_DATA6	[AL33] XSPI1_DATA6	
XSPI1_DATA7	[AN33] XSPI1_DATA7	
XSPI1_SCLK	[AK30] XSPI1_SCLK	
XSPI1_DQS	[AF26] XSPI1_DQS	
XSPI1_SS0_B	[AD24] XSPI1_SS0_B	
XSPI1_SS1_B	[AE25] XSPI1_SS0_B	

3.5.4 EEPROM

The TQMa94xxLA has an optional EEPROM for storing customer data that is connected via I2C2. It can be made read-only, allowing it to be used for storing sensitive data. The memory size can be adjusted by changing the components to meet customer requirements. Another EEPROM is used on the I2C1 bus to store TQ data.

The following table shows details of the default EEPROMs:

Table 10: EEPROMs

Manufacturer	Part number	Size	Temperature range
ST Microelectronics	M24C64-FMH6TG	64 Kbit (customer data)	–40 °C to +85 °C
ST Microelectronics	M24C02-FMH6TG	2 Kbit (TQ data)	–40 °C to +85 °C

3.5.5 SD Card

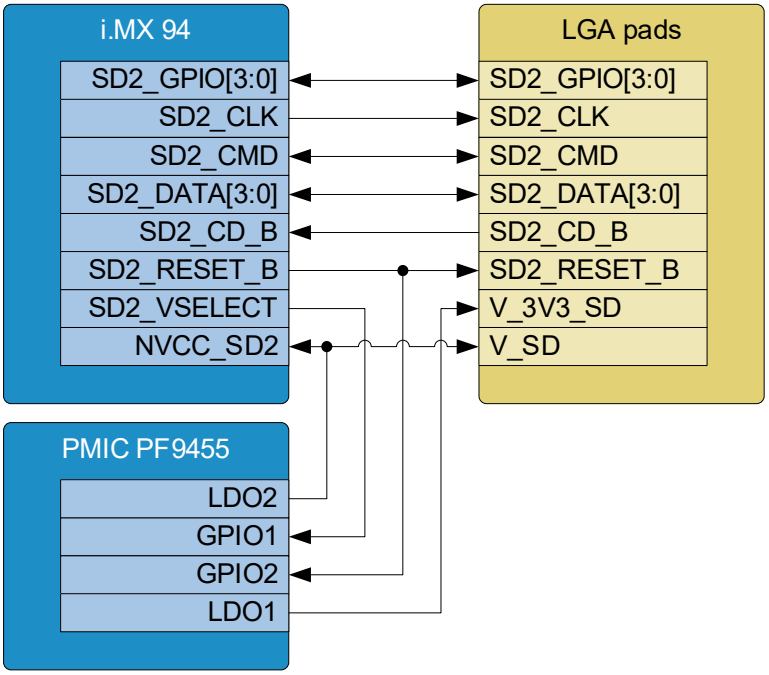

Figure 5: Block diagram SD Card

The i.MX 94 supports SD cards up to UHS-I in SDR104/DDR50 mode. This corresponds to the SD card specification v3.0 and a maximum data width of 4 bits.
To allow booting from SD cards, the SD2 interface is routed to the outside with the exception of SD2_VSELECT. SD2_RESET_B is routed outside but can remain unconnected because the module already implements the actual reset function of this signal.

The SD2 interface signals are supplied by a separate PMIC LDO whose IO voltage can be set to a range of 1.8 V or 3.3 V using the SD2_VSELECT signal. SD2_VSELECT is automatically toggled by the driver to use the fastest possible mode depending on the SD card used.

Table 11: LDO voltage control via SD2_VSELECT

Level SD2_VSELECT	PMIC voltage V_SD2
Low	typ. 3.3 V
High	typ. 1.8 V

The supply voltage V_SD2 is also provided externally by the module. In customer designs, this voltage can be used to connect the pull-up resistors of the SD card interface. Alternatively, the internal pull-up resistors of the CPU can be used.
The voltage V_3V3_SD is used to supply the SD card. The module-internal wiring allows to interrupt the SD card supply in case of a module reset, thus allowing a reset of the SD card.

The four additional GPIO pins on this interface are not required for SD card operation by default and can be used for other purposes. They are primarily relevant when RGMII4 is multiplexed on these pins instead of uSDHC2.

Table 12: Pin assignment SD2 (SD Card)

Signal (multiplexing)	CPU pin	Power group
SD2_CD#	[AE23] SD2_CD_B	NVCC_SD2 (1.8 V / 3.3 V)
SD2_CLK	[AH26] SD2_CLK	
SD2_CMD	[AF24] SD2_CMD	
SD2_DATA0	[AJ27] SD2_DATA0	
SD2_DATA1	[AK28] SD2_DATA1	
SD2_DATA2	[AL29] SD2_DATA2	
SD2_DATA3	[AN31] SD2_DATA3	
SD2_RST#	[AP28] SD2_RESEST_B	
SD2_GPIO0	[AG25] SD2_GPIO0	
SD2_GPIO1	[AN29] SD2_GPIO1	
SD2_GPIO2	[AP30] SD2_GPIO2	
SD2_GPIO3	[AM28] SD2_GPIO3	
SD2_VSELECT	[AE27] SD2_VSELECT	NVCC_WAKEUP (1.8 V)

3.6 Temperature sensor

The TI TMP1075DSGR temperature sensor is used for temperature measurement. The alarm output ALERT is routed to the outside and can be flexibly connected as an open-drain output. The sensor is controlled by the I2C1 bus (address: 0x4A).

3.7 i.MX 94 internal RTC

The i.MX 94 has an internal RTC. Its accuracy is primarily determined by the characteristics of the quartz used. The type FC-135 used on the TQMa94xxLA has a standard frequency tolerance of ±20 ppm at +25 °C. (Parabolic coefficient: max. -0.04 x 10^{-6} / °C^2)

3.8 Optional RTC RX8130CE

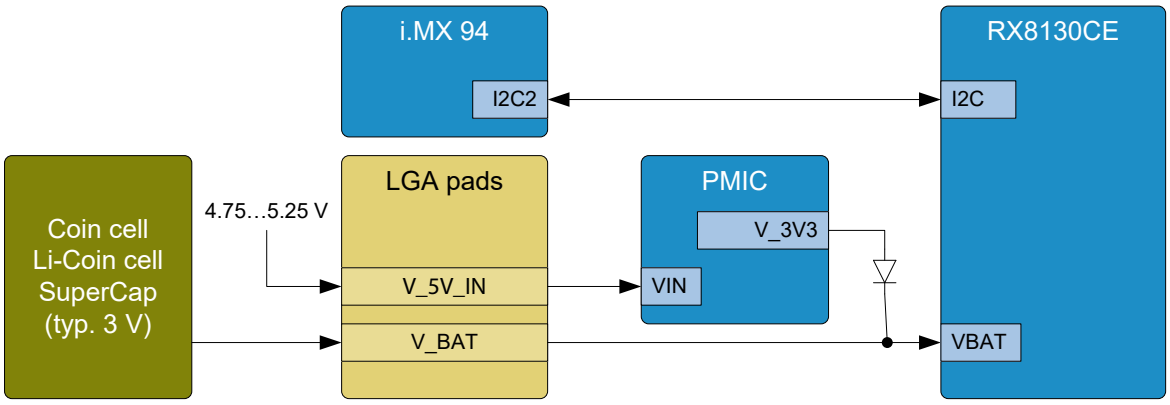

Figure 6: Block diagram RTC supply (TQMa94xxLA with discrete RTC)

In addition to the i.MX 94 internal RTC, TQMa94xxLA has optionally a discrete RTC at I2C2. It is recommended to use the RTC RX8130CE due to the lower current consumption during standby modes. The RTC_EVENT# signal is routed to the LGA pad and can be used as an open-drain signal in customer designs.

- The discrete RTC has I2C2 address `0x32 / 011 0010b`

3.9 Gyroscope

An optional gyroscope with I2C and SPI interfaces is provided on the TQMa94xxLA. It allows to determine the position of the TQMa94xxLA and provides two interrupts. These are routed to the outside and are available at two LGA pads. It is connected via I2C2 (address: `0x6B / 110 1011b`).

3.10 RMII (Ethernet/EtherCAT)

The i.MX 94 has two RMII interfaces, which also support EtherCAT as an option. Both interfaces are routed to the outside without any additional internal module circuits.

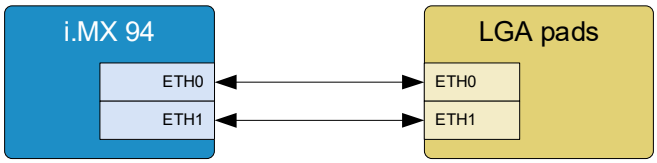

Figure 7: Block diagram RMII

The signal assignment can be found in the following table:

Table 13: Pin assignment RMII

Signal (multiplexing)	CPU pin	Power group
ETH0_RD0	[AP8] ETH0_RXD0	NVCC_ENET1 (1.8 V)
ETH0_RD1	[AN9] ETH0_RXD1	
ETH0_RD2	[AP10] ETH0_RXD2	
ETH0_RD3	[AM10] ETH0_RXD3	
ETH0_RX_CLK	[AM8] ETH0_RX_CLK	
ETH0_RX_DV	[AK8] ETH0_RX_DV	
ETH0_RX_ER	[AL9] ETH0_RX_ER	
ETH0_TD0	[AE13] ETH0_TXD0	
ETH0_TD1	[AF12] ETH0_TXD1	
ETH0_TD2	[AG11] ETH0_TXD2	
ETH0_TD3	[AH10] ETH0_TXD3	
ETH0_TX_CLK	[AJ11] ETH0_TX_CLK	
ETH0_TX_EN	[AG9] ETH0_TX_EN	
ETH0_TX_ER	[AF10] ETH0_TX_ER	
ETH0_CRS	[AK10] ETH0_CRS	
ETH0_COL	[AJ9] ETH0_COL	
ETH1_RD0	[AN11] ETH1_RXD0	
ETH1_RD1	[AP12] ETH1_RXD1	
ETH1_RD2	[AL15] ETH1_RXD2	
ETH1_RD3	[AM14] ETH1_RXD3	
ETH1_RX_CLK	[AJ13] ETH1_RX_CLK	
ETH1_RX_DV	[AL13] ETH1_RX_DV	
ETH1_RX_ER	[AM12] ETH1_RX_ER	
ETH1_TD0	[AF16] ETH1_TXD0	
ETH1_TD1	[AG15] ETH1_TXD1	
ETH1_TD2	[AH14] ETH1_TXD2	
ETH1_TD3	[AH16] ETH1_TXD3	
ETH1_TX_CLK	[AF14] ETH1_TX_CLK	
ETH1_TX_EN	[AK14] ETH1_TX_EN	
ETH1_TX_ER	[AH12] ETH1_TX_ER	
ETH1_CRS	[AK12] ETH1_CRS	
ETH1_COL	[AP14] ETH1_COL	

3.11 1G Ethernet (RGMII)

The i.MX 94 has three Ethernet MACs, each operating in maximum 1 Gigabit full-duplex mode. MII, RMII, or RGMII can be used as interface, with the latter being used for standard multiplexing. On the multiplexing side, only one common MDIO/SMI interface is available for all MACs.

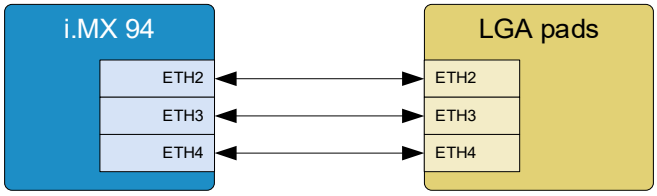

Figure 8: Block diagram 1G Ethernet (RGMII)

The following table shows the Ethernet interface signals:

Table 14: Pin assignment RGMII

Signal (multiplexing)	CPU pin	Power group
ETH2_RX_CTL	[AL17] ETH2_RX_CTL	NVCC_ENET (1.8 V)
ETH2_RXC	[AK16] ETH2_RXC	
ETH2_RD0	[AM16] ETH2_RXD0	
ETH2_RD1	[AP16] ETH2_RXD1	
ETH2_RD2	[AP18] ETH2_RXD2	
ETH2_RD3	[AP20] ETH2_RXD3	
ETH2_TX_CTL	[AJ17] ETH2_TX_CTL	
ETH2_TXC	[AK18] ETH2_TXC	
ETH2_TD0	[AE17] ETH2_TXD0	
ETH2_TD1	[AG17] ETH2_TXD1	
ETH2_TD2	[AH18] ETH2_TXD2	
ETH2_TD3	[AK20] ETH2_TXD3	
ETH2_MDC	[AN17] ETH2_MDC_GPIO1	
ETH2_MDIO	[AM18] ETH2_MDIO_GPIO2	
ETH3_RX_CTL	[AL21] ETH3_RX_CTL	
ETH3_RXC	[AM20] ETH3_RXC	
ETH3_RD0	[AL19] ETH3_RXD0	
ETH3_RD1	[AM22] ETH3_RXD1	
ETH3_RD2	[AP22] ETH3_RXD2	
ETH3_RD3	[AN23] ETH3_RXD3	
ETH3_TX_CTL	[AJ21] ETH3_TX_CTL	
ETH3_TXC	[AK22] ETH3_TXC	
ETH3_TD0	[AE19] ETH3_TXD0	
ETH3_TD1	[AF20] ETH3_TXD1	
ETH3_TD2	[AG19] ETH3_TXD2	
ETH3_TD3	[AH20] ETH3_TXD3	
ETH3_MDC	[AM24] ETH3_MDC_GPIO1	
ETH3_MDIO	[AL23] ETH3_MDIO_GPIO2	
ETH4_RX_CTL	[AN27] ETH4_RX_CTL	
ETH4_RXC	[AP24] ETH4_RXC	
ETH4_RD0	[AN25] ETH4_RXD0	
ETH4_RD1	[AP26] ETH4_RXD1	
ETH4_RD2	[AL25] ETH4_RXD2	
ETH4_RD3	[AL27] ETH4_RXD3	
ETH4_TX_CTL	[AK24] ETH4_TX_CTL	
ETH4_TXC	[AJ23] ETH4_TXC	
ETH4_TD0	[AE21] ETH4_TXD0	
ETH4_TD1	[AF22] ETH4_TXD1	
ETH4_TD2	[AG21] ETH4_TXD2	
ETH4_TD3	[AH22] ETH4_TXD3	
ETH4_MDC	[AK26] ETH4_MDC_GPIO1	
ETH4_MDIO	[AH24] ETH4_MDIO_GPIO2	

3.12 2.5G Ethernet (SGMII)

In addition to the 1G Ethernet interfaces, some i.MX 94 derivatives also have a 2.5G Ethernet SGMI interface with two lanes. The interface is routed directly to the outside without any further internal module circuitry.

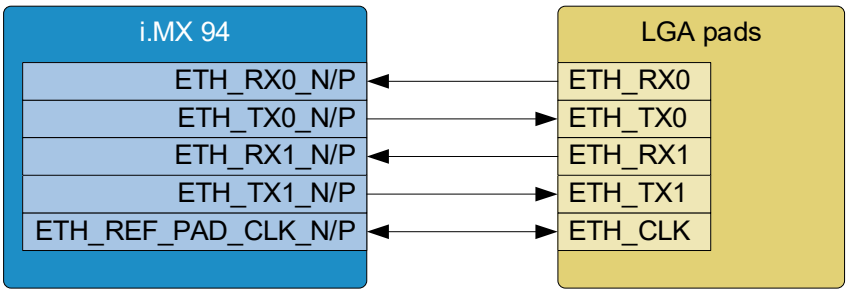

Figure 9: Block diagram 2.5G Ethernet (XGMII)

Table 15: Pin assignment SGMII

Signal (multiplexing)	CPU pin	Power group
ETH_RX0_N	[AP4] ETH_RX0_N	VDD_ETH_0P8 (0.8 V)
ETH_RX0_P	[AN3] ETH_RX0_P	
ETH_RX1_N	[AP6] ETH_RX1_N	
ETH_RX1_P	[AN5] ETH_RX1_P	
ETH_REF_CLK_N	[AL1] ETH_REF_PAD_CLK_N	
ETH_REF_CLK_P	[AM2] ETH_REF_PAD_CLK_P	
ETH_TX0_N	[AL5] ETH_TX0_N	
ETH_TX0_P	[AK4] ETH_TX0_P	
ETH_TX1_N	[AJ7] ETH_TX1_N	
ETH_TX1_P	[AK6] ETH_TX1_P	

3.13 USB

The i.MX 94 has a USB 2.0 controller (USB2) and a USB 3.0 controller (USB1). Both can be configured as host or device. The superspeed signals of the USB 3.0 controller can be connected directly to a USB-C connector as the controller provides two differential Tx and Rx pairs.

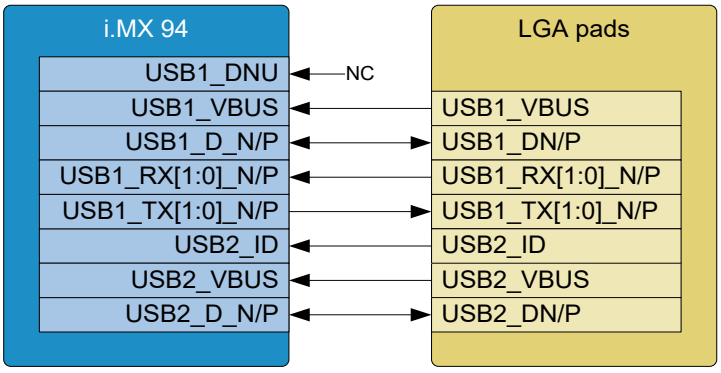

Figure 10: Block diagram USB

The USB1_ID signal has no function and is left unconnected. If necessary, use the USB1_OTG_ID signal instead. However, the OTG signals are only available to a limited extent because their multiplexing overlaps with the ENET2 interface.

The VBUS signals both have 30 kΩ series resistors on the module. According to NXP's i.MX 94 Hardware Developer's Guide, it is therefore possible to apply external 5V to these pins. The USB*_TXRTUNE pins are connected to GND with 200 Ohm resistors. The differential USB signals must have a differential impedance of 90 Ω.

Table 16: Pin assignment USB

Signal (multiplexing)	CPU pin	Power group
NC	[G15] USB1_DNU	Internal 1.8 V
USB2_ID	[J15] USB2_ID	VDD_USB_1P8 (1.8 V)
-	[K16] USB2_TXRTUNE	
USB1_DN USB1_DP	[C15] USB1_D_N [D16] USB1_D_P	VDD_USB_3P3 (3.3 V)
USB1_VBUS	[H14] USB1_VBUS	
-	[E13] USB1_TXRTUNE	
USB2_DN USB2_DP	[F16] USB2_D_N [G17] USB2_D_P	
USB2_VBUS	[H18] USB2_VBUS	
USB1_RX0_N USB1_RX0_P	[E15] USB1_RX0_N [D14] USB1_RX0_P	VDD_USB_0P8 (0.8 V)
USB1_RX1_N USB1_RX1_P	[B14] USB1_RX1_N [A13] USB1_RX1_P	
USB1_TX0_N USB1_TX0_P	[B16] USB1_TX0_N [A15] USB1_TX0_P	
USB1_TX1_N USB1_TX1_P	[C13] USB1_TX1_N [B12] USB1_TX1_P	

3.14 LVDS

The i.MX 94 has a LVDS controller with four differential data pairs for data transfer. The LVDS PHYs support outputs up to 1080p.

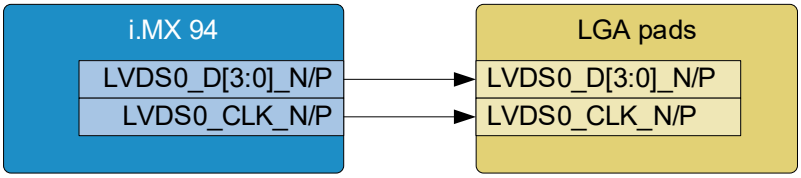

Figure 11: Block diagram LVDS

The differential signals have a differential impedance of 100 Ω. The interfaces are routed to the outside of the module without any internal circuitry.

Table 17: Pin assignment LVDS

Signal (multiplexing)	CPU pin	Power group
LVDS0_D0_N LVDS0_D0_P	[G11] LVDS0_D0_N [F12] LVDS0_D0_P	VDD_LVDS_1P8 (1.8 V)
LVDS0_D1_N LVDS0_D1_P	[D10] LVDS0_D1_N [C11] LVDS0_D1_P	
LVDS0_D2_N LVDS0_D2_P	[F10] LVDS0_D2_N [E11] LVDS0_D2_P	
LVDS0_D3_N LVDS0_D3_P	[B10] LVDS0_D3_N [A11] LVDS0_D3_P	
LVDS0_CLK_N LVDS0_CLK_P	[H12] LVDS0_CLK_N [G13] LVDS0_CLK_P	

3.15 Tamper

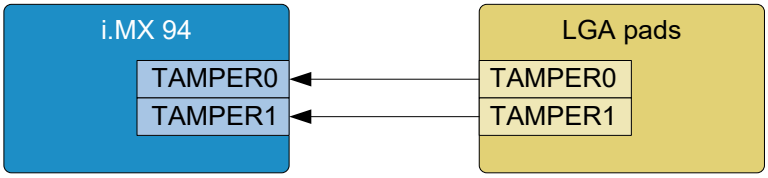

Figure 12: Block diagram Tamper

A total of two tamper signals are provided as one of the security features of the i.MX 94's BBSM unit. These are routed to LGA pads without any additional circuitry.

Table 18: Pin assignment TAMPER

Signal (multiplexing)	CPU pin	Power group
TAMPER0	[J19] TAMPER0	NVCC_BBSM (1.8 V)
TAMPER1	[H20] TAMPER1	

3.16 SAI

The i.MX 94 has several SAI interfaces with different data bus widths. All SAI interfaces support I2S, AC97, TDM and other Codec interfaces. The SAI1 pins of the AON domain are routed to the outside in their actual designation.

Table 19: Pin assignment SAI

Signal (multiplexing)	CPU pin	Power group
SAI1_TXC	[D30] SAI1_TXC	NVCC_AON (1.8 V)
SAI1_TXFS	[F30] SAI1_TXFS	
SAI1_TXD0	[F28] SAI1_TXD0	
SAI1_RXD0	[D28] SAI1_RXD0	

3.17 PDM

The i.MX 94 CPU provides a PDM interface that can be used as a microphone input. However, as the native CPU pins in the always-on domain only have two lanes and also allow the use of other functions, these pins are not intended for primary PDM use. If a PDM interface is required, it should be taken from the GPIO2 domain, as this offers more lanes for a more extensive interface. For example, the CPU pin PDM_CLK is used to connect the PMIC_INT# signal and is not routed to the outside. PDM_BIT_STREAM1 allows multiplexing as M33_NMI.

Table 20: Pin assignment PDM

Signal (multiplexing)	CPU pin	Power group
PDM_BIT0	[D32] PDM_BIT_STREAM0	NVCC_AON (1.8 V)
PDM_BIT1	[C33] PDM_BIT_STREAM1	

3.18 UART

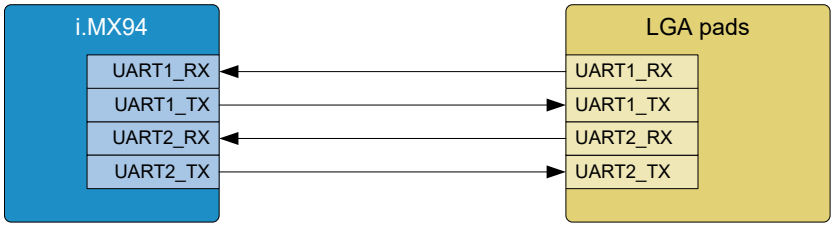

Figure 13: Block diagram UART

The CPU provides up to ten UARTs. Two of them are available by default. Both are in the AON domain and are therefore assigned to the Cortex M33 / system controller.

Table 21: Pin assignment UART

Signal (multiplexing)	CPU pin	Power group
UART1_RX	[J27] UART1_RXD	NVCC_AON (1.8 V)
UART1_TX	[H28] UART1_TXD	
UART2_RX	[L27] UART2_RXD	
UART2_TX	[K28] UART2_TXD	

3.19 PCI Express

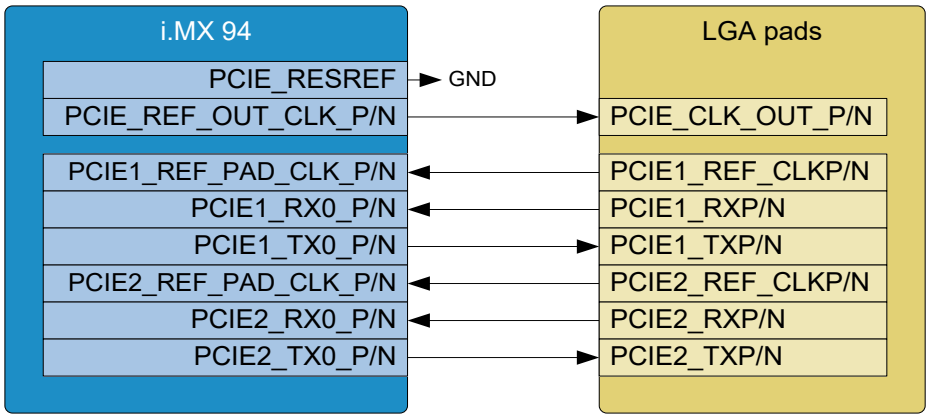

Figure 14: Block diagram PCI Express

The i.MX 94 has two PCIe 3.0 interfaces, each with one lane. A separate clock output is also provided. It is not possible to connect the clock output directly to the clock inputs because the technologies are not compatible (LVDS to HCSL). For this reason, a buffer or an external clock generator is always required to supply the clock inputs! Corresponding circuitry must always be implemented on the mainboard. The differential data lines must be the same length and have a differential impedance of 100 Ω. The differential clock lines, however, only require 85 Ω.

Table 22: Pin assignment PCIe

Signal (multiplexing)	CPU pin	Power group
PCIE1_REF_CLKN	[B20] PCIE1_REF_PAD_CLK_N	VDD_PCI_1P8 (1.8 V)
PCIE1_REF_CLKP	[A19] PCIE1_REF_PAD_CLK_P	
PCIE1_RXN	[C19] PCIE1_RX0_N	
PCIE1_RXP	[D18] PCIE1_RX0_P	
PCIE1_TXN	[F18] PCIE1_TX0_N	
PCIE1_TXP	[E19] PCIE1_TX0_P	
PCIE2_REF_CLKN	[D22] PCIE2_REF_PAD_CLK_N	
PCIE2_REF_CLKP	[C21] PCIE2_REF_PAD_CLK_P	
PCIE2_RXN	[E21] PCIE2_RX0_N	
PCIE2_RXP	[D20] PCIE2_RX0_P	
PCIE2_TXN	[F20] PCIE2_TX0_N	
PCIE2_TXP	[G21] PCIE2_TX0_P	
PCIE_CLK_OUT_N	[B18] PCIE_REF_OUT_CLK_N	VDD_ANAVDET_1P8 (1.8 V)
PCIE_CLK_OUT_P	[A17] PCIE_REF_OUT_CLK_P	

3.20 I²C

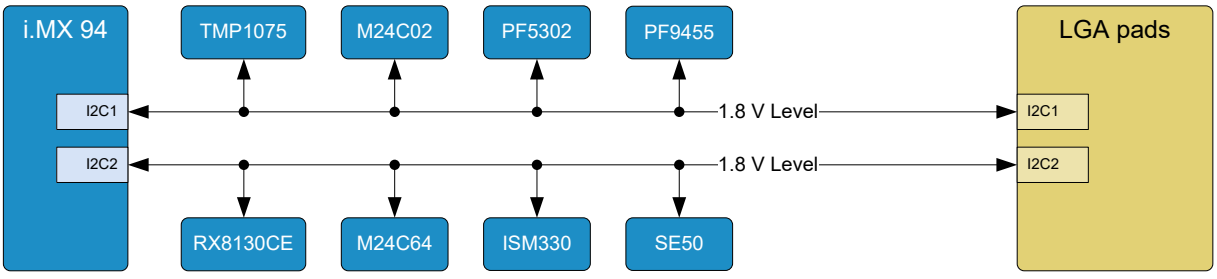

Figure 15: Block diagram I²C

The i.MX 94 provides up to eight I2C interfaces. I2C1 serves as the Cortex-M33 system bus for PMICs and temperature sensor, has pull-ups on the module and is also routed to LGA pads. The other internal components RTC, EEPROM, TSE and gyroscope are combined in the separate bus I2C2, which also operates at 1.8 V.

Other buses can be provided on the GPIO pins without wiring on the module. Their voltage level is defined by V_GPIO. In this case, pull-up resistors must be placed outside the module.

The internal components of the TQMa94xxLA with their corresponding addresses are listed in the following table:

Table 23: I²C addresses

Bus	I2C -Slave	Address	Remark
I2C1	Temperature Sensor TMP1075	0x4A	-
	EEPROM M24C02	0x50	Memory Array
	PMIC PF9455	0x08	-
	PMIC PF5302	0x29	-
I2C2	RTC RX8130CE	0x32	-
	Secure Element SE051	0x48	-
	Gyroskop ISM330	0x6B	-
	EEPROM M24C64	0x50	Memory Array

A list of the available I2C buses can be found in the following table:

Table 24: Pin assignment I2C

Signal (multiplexing)	CPU pin	Power group
I2C1_SCL	[K26] I2C1_SCL	NVCC_AON (1.8 V)
I2C1_SDA	[G25] I2C1_SDA	
I2C2_SCL	[F26] I2C2_SCL	
I2C2_SDA	[H26] I2C2_SDA	

3.21 GPIO

With the exception of dedicated differential signals (e.g. PCIe, LVDS), most of the CPU pins can be configured as GPIOs. GPIO1_IO08 is not routed to the outside and is used internally to connect the open-drain signal PMIC_INT#. As a freely configurable group, the signals of the NVCC_GPIO power domain can be used not only as GPIOs, but also as I2C, SPI or SAI interfaces, for example.

Table 25: Pin assignment GPIO

Signal (multiplexing)	CPU pin	Power group
GPIO2_IO00	[E33] GPIO2_IO00	NVCC_ GPIO (1,8 V / 3,3 V)
GPIO2_IO01	[J29] GPIO2_IO01	
GPIO2_IO02	[F32] GPIO2_IO02	
GPIO2_IO03	[K30] GPIO2_IO03	
GPIO2_IO04	[H30] GPIO2_IO04	
GPIO2_IO05	[J31] GPIO2_IO05	
GPIO2_IO06	[F34] GPIO2_IO06	
GPIO2_IO07	[P26] GPIO2_IO07	
GPIO2_IO08	[D34] GPIO2_IO08	
GPIO2_IO09	[G33] GPIO2_IO09	
GPIO2_IO10	[N27] GPIO2_IO10	
GPIO2_IO11	[H32] GPIO2_IO11	
GPIO2_IO12	[L31] GPIO2_IO12	
GPIO2_IO13	[J33] GPIO2_IO13	
GPIO2_IO14	[L29] GPIO2_IO14	
GPIO2_IO15	[P28] GPIO2_IO15	
GPIO2_IO16	[H34] GPIO2_IO16	
GPIO2_IO17	[N29] GPIO2_IO17	
GPIO2_IO18	[K34] GPIO2_IO18	
GPIO2_IO19	[R27] GPIO2_IO19	
GPIO2_IO20	[M30] GPIO2_IO20	
GPIO2_IO21	[T26] GPIO2_IO21	
GPIO2_IO22	[L33] GPIO2_IO22	
GPIO2_IO23	[N31] GPIO2_IO23	
GPIO2_IO24	[P30] GPIO2_IO24	
GPIO2_IO25	[M32] GPIO2_IO25	
GPIO2_IO26	[R29] GPIO2_IO26	
GPIO2_IO27	[M34] GPIO2_IO27	
GPIO2_IO28	[N33] GPIO2_IO28	
GPIO2_IO29	[R31] GPIO2_IO29	
GPIO2_IO30	[P34] GPIO2_IO30	
GPIO2_IO31	[T28] GPIO2_IO31	
GPIO3_IO00	[T30] GPIO3_IO00	
GPIO3_IO01	[U27] GPIO3_IO01	
GPIO3_IO02	[R33] GPIO3_IO02	
GPIO3_IO03	[T34] GPIO3_IO03	
GPIO3_IO04	[U31] GPIO3_IO04	
GPIO3_IO05	[T32] GPIO3_IO05	
GPIO3_IO06	[V28] GPIO3_IO06	
GPIO3_IO07	[U33] GPIO3_IO07	
GPIO3_IO08	[V30] GPIO3_IO08	
GPIO3_IO09	[W29] GPIO3_IO09	
GPIO3_IO10	[V34] GPIO3_IO10	
GPIO3_IO11	[W27] GPIO3_IO11	
GPIO3_IO12	[W31] GPIO3_IO12	
GPIO3_IO13	[Y34] GPIO3_IO13	
GPIO3_IO14	[W33] GPIO3_IO14	
GPIO3_IO15	[Y32] GPIO3_IO15	
GPIO3_IO16	[Y30] GPIO3_IO16	
GPIO3_IO17	[Y28] GPIO3_IO17	
GPIO3_IO18	[Y26] GPIO3_IO18	
GPIO3_IO19	[AA31] GPIO3_IO19	
GPIO3_IO20	[AA33] GPIO3_IO20	
GPIO3_IO21	[AB34] GPIO3_IO21	
GPIO3_IO22	[AA27] GPIO3_IO22	
GPIO3_IO23	[AC33] GPIO3_IO23	
GPIO3_IO24	[AB30] GPIO3_IO24	
GPIO3_IO25	[AB28] GPIO3_IO25	

3.22 Watchdog

The watchdog signal WDOG_ANY of the i.MX 94 is connected to the watchdog input of the PMIC and to the LGA pad.

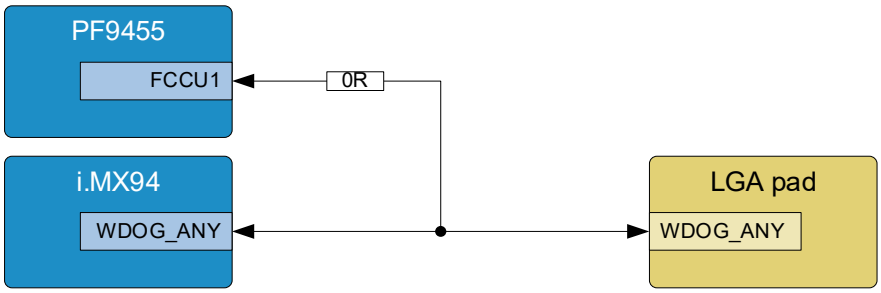

Figure 16: Block diagram Watchdog

3.23 ADC

Figure 17: Block diagram ADC

The i.MX 94 has a 12-bit analog-to-digital converter with a reference voltage of 1.8 V and a maximum of 8 channels. The module generates the reference voltage internally.

Table 26: Pin assignment ADC

Signal (multiplexing)	CPU pin	Power group
ADC_IN0	[D26] ADC_IN0	VDD_ANA_1P8 (1.8 V)
ADC_IN1	[B28] ADC_IN1	
ADC_IN2	[E25] ADC_IN2	
ADC_IN3	[B26] ADC_IN3	
ADC_IN4	[A27] ADC_IN4	
ADC_IN5	[F24] ADC_IN5	
ADC_IN6	[C25] ADC_IN6	
ADC_IN7	[A25] ADC_IN7	

3.24 JTAG

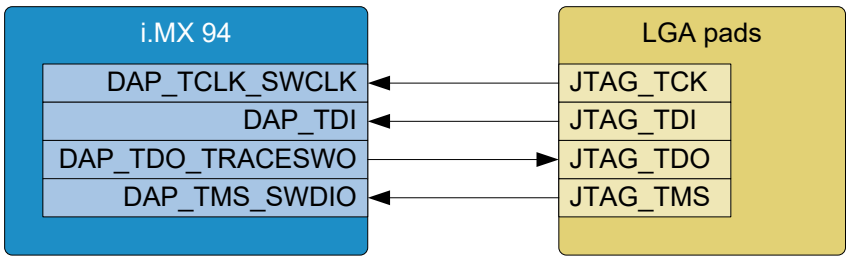

Figure 18: Block diagram JTAG

The JTAG signals are routed directly to LGA pads. Resistors for the pull circuits must be provided on the mainboard.

Table 27: Pin assignment JTAG

Signal (multiplexing)	CPU pin	Power group
JTAG_TCK	[AC29] DAP_TCLK_SWCLK	NVCC_CCM_DAP (1.8 V)
JTAG_TMS	[AD34] DAP_TMS_SWDIO	
JTAG_TDI	[AC31] DAP_TDI	
JTAG_TDO	[AE33] DAP_TDO_TRACESWO	

3.25 Trust Secure Element

Depending on the module variant, a Trust Secure Element (TSE) is available on the TQMa94xxLA. This is connected to the I2C2 bus (address: `0x48`). The selected chip SE051 from NXP provides additional smartcard interfaces according to ISO14443 and ISO7816 besides the I2C interface. The connection of the antenna for ISO 14443 or the sensor for ISO 7816 must be made on the base board.

3.26 Power

The TQMa94xxLA is designed for a voltage range of 4.75 V to 5.25 V. All supply voltages required by the CPU and the module components are generated by the TQMa94xxLA. To ensure the correct voltage sequence when powering the module, the individual controllers are enabled in a controlled manner by the PF9455 PMIC, which is controlled by a supervisor.

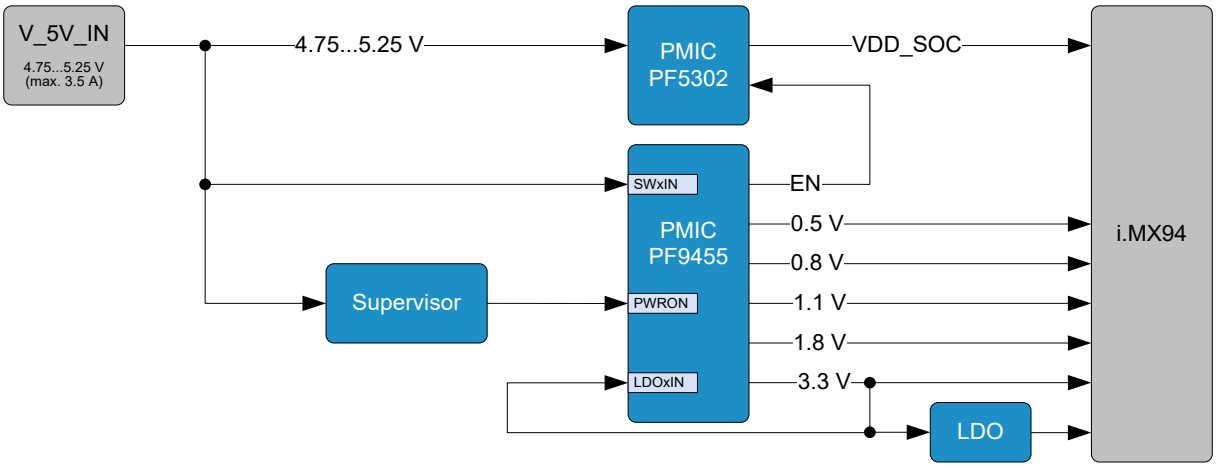

Figure 19: Block diagram module supply

3.26.1 Voltage monitoring

The supervisor of TQMa94xxLA monitors the input voltage and triggers a module reset via the PMIC_ON_REQ signal if the input voltage drops below 4.38 V.

Any protective measures beyond the component's internal protective mechanisms (e.g., overcurrent or reverse polarity protection) must be provided outside the module.

Attention: Malfunction or destruction	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. An excessively high supply voltage can lead to malfunctions, untimely aging or destruction of the TQMa94xxLA.

3.26.2 Power-up sequence TQMa94xxLA

The TQMa94xxLA can be operated with a supply voltage of 4.75 V to 5.25 V and all voltages for normal operation are generated on the module itself.

Attention: Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins should be driven by external components until the power-up sequence has been completed. The mainboard voltages are to be released by PGOOD.

3.26.3 PMICs

Two PMICs are responsible for powering the i.MX 94. The PF9455 is the primary PMIC that controls and monitors the other chip and communicates with it via I2C as needed. The PF9455 has a fixed pre-programmed power sequence in which the PF5302 is integrated. Enabling and PGOOD monitoring is done by the PF9455.

Attention: Malfunction or destruction	
	Improper PMIC programming may cause the i.MX 94 or other peripherals on the TQMa94xxLA to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa94xxLA.

3.27 Reset and Management Signals

Two reset options are provided on the module side:

1. A reset is made possible by the PMIC_ON_REQ signal. This signal between the CPU and PMIC is also routed to the outside, is low-active and has an internal CPU pull-up.
2. A second option is provided by the WDOG_ANY signal. This is a 1.8 V signal which has a pull-up on the module. The associated PMIC behavior can be configured via I2C.

The ONOFF pin of the CPU offers two reaction options. It has an internal pull-up and is low-active. If this signal is held low for longer than 5 s, the CPU switches to OFF mode. If the signal is briefly pulled low in OFF mode, the CPU switches back to ON mode. A short low pulse in ON mode triggers an interrupt according to (1). In addition, a reset is triggered by a module-internal supervisor when the module supply voltage drops.

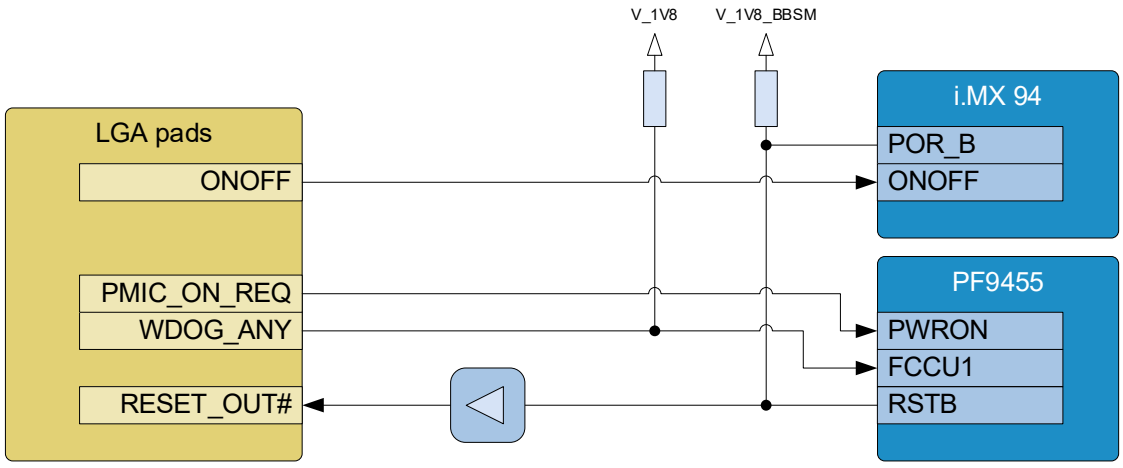

Figure 20: Block diagram Reset

RESET_OUT# is an open-drain output and available at an LGA pad. In customer applications, this ensures feedback to external components when the module is reset.

The FCCU0 signal is used as a fault counter and is only routed internally between the CPU and PMIC. The AMUX, PGOOD and FS0B signals are PMIC status signals, the use of which is up to the user. The function of FS0B differs depending on the application type of the PMIC (QM (Non-Safety Device), Industrial (SIL-2) or Automotive (ASIL-B/C/D)).

The following table lists the reset signals mentioned above, as well as other status signals that cannot be assigned to a more specific group:

Table 28: Reset and management signals

Signal (multiplexing)	CPU pin	Power group
PMIC_STBY_REQ	[G23] PMIC_STBY_REQ	NVCC_BBSM (1.8 V)
PMIC_ON_REQ	[E23] PMIC_ON_REQ	
IMX_ONOFF	[K24] ONOFF	
RESET_OUT#	[F22] POR_B	
PMIC_INT#	[A29] PDM_CLK	NVCC_AON (1.8 V)
FCCU_ERR0	[G29] FCCU_ERR0	
WDOG_ANY	[E31] WDOG_ANY	
AMUX	PMIC PF9455 - Pin 15	PMIC internal
PGOOD	PMIC PF9455 - Pin 44	Open Drain
FS0B	PMIC PF9455 - Pin 54	
RTC_EVENT#	-	
TEMP_EVENT#	-	
GYRO_INT1	-	
GYRO_INT2	-	

4. MECHANICS

4.1 Dimensions

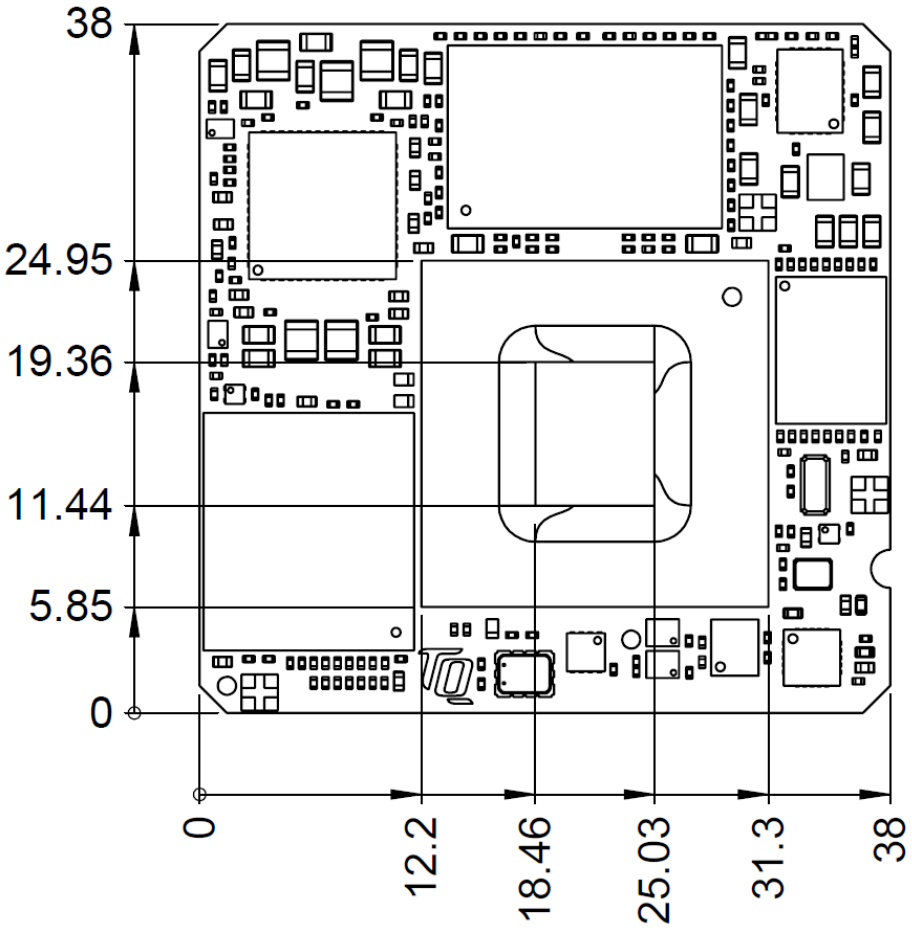

Figure 21: TQMa94xxLA dimensions (top view)

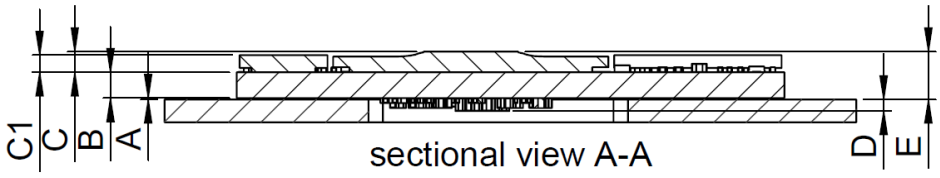

Figure 22: TQMa94xxLA heights

Table 29: Heights (in mm)

Dimension	Value	Tolerance	Comment
A	0.125	+0.075 / -0.025	Board to board distance
B	1.75	±0.18	PCB thickness
C	1.40	±0.16	CPU height
C1	1.20	±0.11	NOR Flash
D	0.57	±0.20	Component height below module
E	3.30	±0.24	Overall height to CPU surface

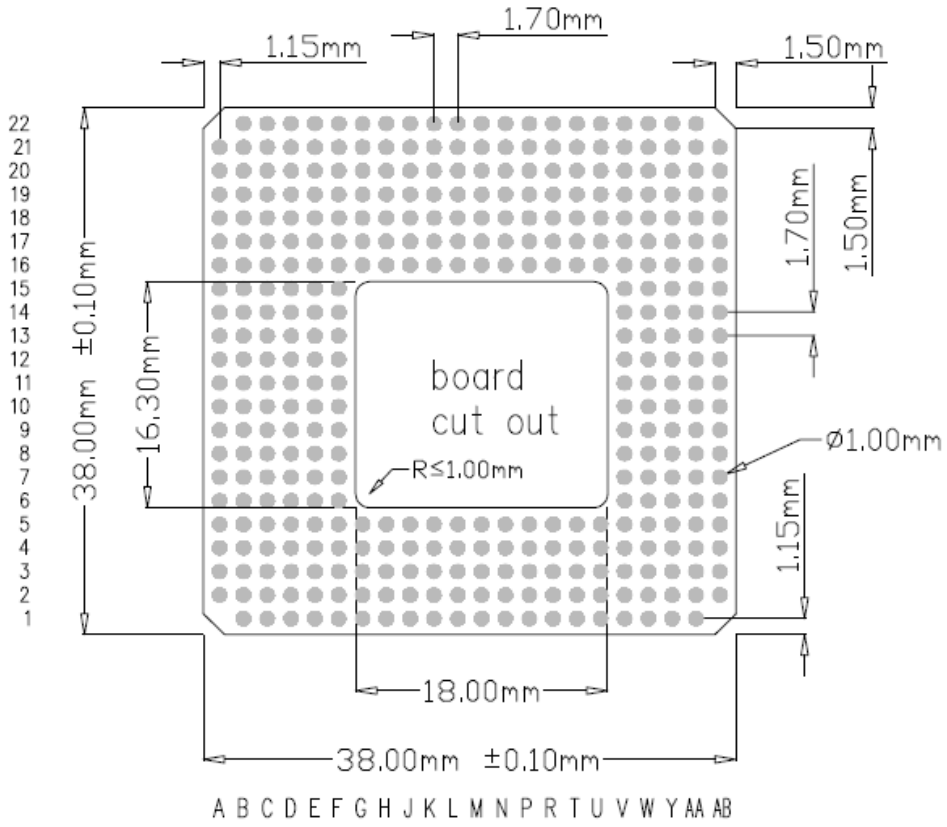

Figure 23: TQMa94xxLA dimensions (bottom view)

4.2 Component placement

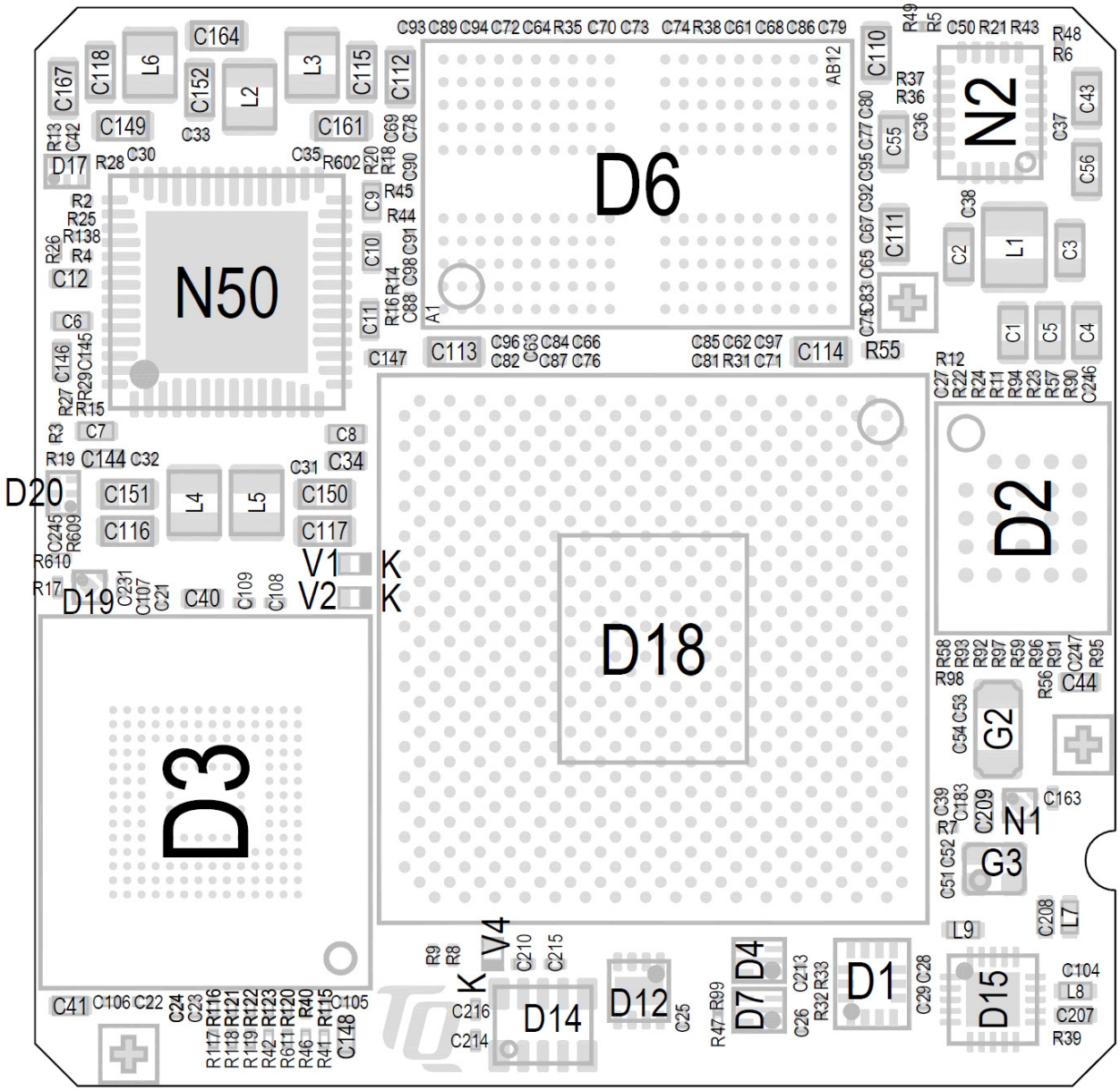

Figure 24: TQMa94xxLA, component placement top

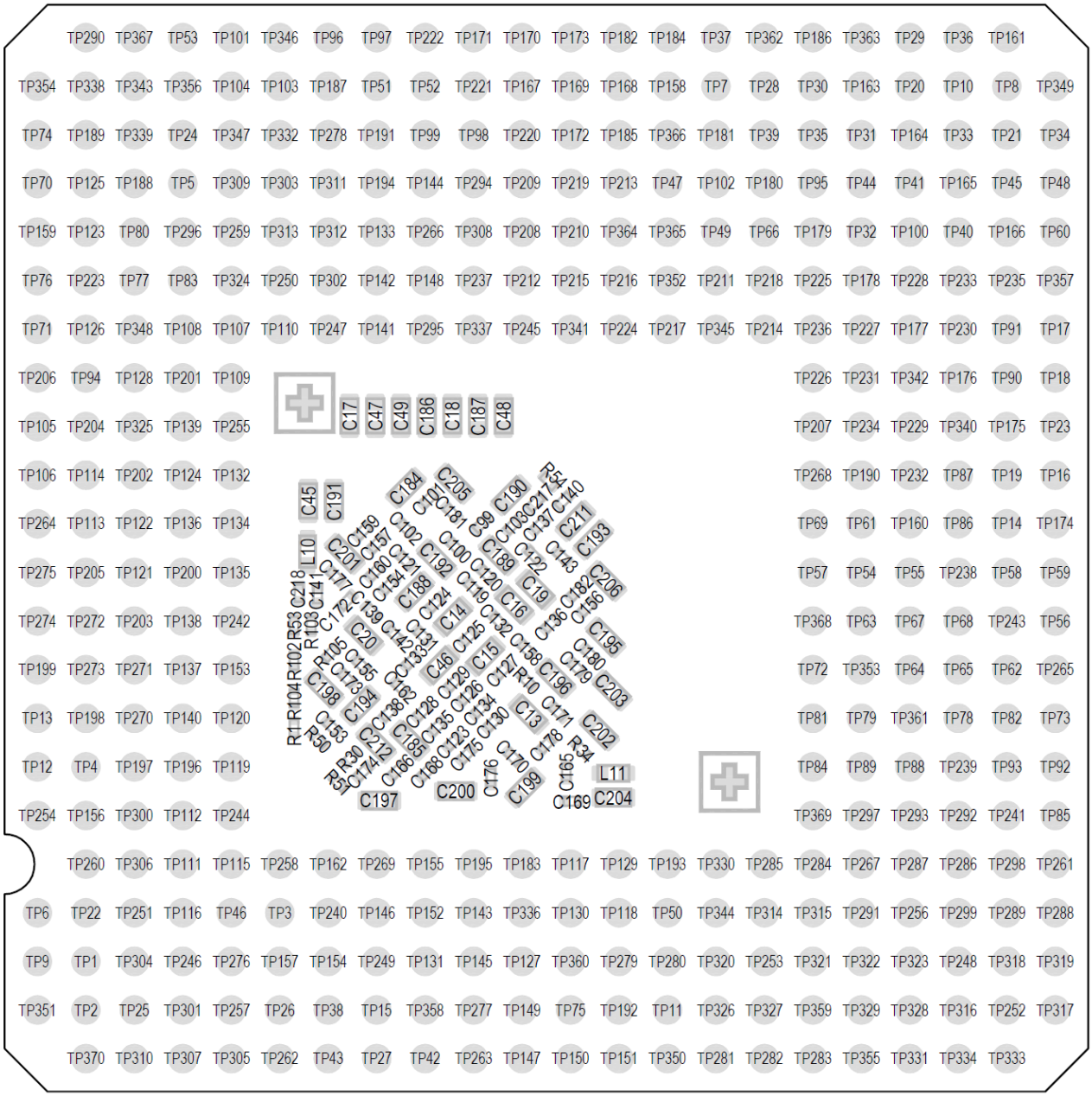

Figure 25: TQMa94xxLA, component placement bottom

The label on the TQMa94xxLA shows the following information:

Table 30: Label on TQMa94xxLA

Label	Content
AK1	MAC address, TQMa94xxLA version and revision, serial number

4.3 Adaptation to the environment

The TQMa94xxLA has overall dimensions (length × width) of 38 mm × 38 mm (± 0.1 mm).
The TQMa94xxLA (bare die version) has a minimum height above the carrier board of 3.30 mm (± 0.24 mm)
The TQMa94xxLA weighs approximately TBD.

4.4 Protection against external effects

As an embedded module, the TQMa94xxLA is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.5 Thermal management

To cool the TQMa94xxLA, a maximum of approximately TBD watts must be dissipated.
The cooling solution must be able to dissipate this power peak; it will never occur permanently in normal operation.
The power dissipation originates primarily in the i.MX 94, the SDRAM and the PMICs.
The power dissipation also depends on the software used and can vary according to the application. It is recommended to monitor critical temperatures and respond appropriately in the software. The CPU has an integrated temperature sensor that monitors the die temperature. In addition, a temperature sensor is implemented on the module.
See i.MX 94 Data Sheet (1) for further information.

Attention: Destruction or malfunction, TQMa94xxLA heat dissipation	
	The TQMa94xxLA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 94 must be taken into consideration when connecting the heat sink. The i.MX 94 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa94xxLA and thus malfunction, deterioration or destruction.

4.6 Structural requirements

The TQMa94xxLA has to be soldered on the carrier board. The TQMa94xxLA is held on the mainboard by the holding force of the solder connections from the LGA pads and requires no further fastening measures. If there are high requirements for vibration and shock resistance, a module holder must be provided in the final application to additionally hold the module in position. Since no heavy and large components are used, there are no further requirements.

Attention: Note on equipping the base board	
	To ensure a high-quality connection of the LGA pads when reflow soldering the TQMa94xxLA, the LGA pads must be free of grease and contamination. Please contact TQ-Support for soldering instructions (6).

5. SOFTWARE

The TQMa94xxLA is delivered with a preinstalled boot loader U-Boot and the BSP provided by TQ-Systems GmbH, which is tailored for the MBa94xxCA.

The boot loader U-Boot provides TQMa94xxLA-specific as well as board-specific settings, e.g.:

- i.MX 94 configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader is used.

More information can be found in the TQ-Support Wiki for the TQMa94xxLA.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa94xxLA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs for multi-pole interfaces (e.g. LC display).

As part of the development, an EMC test was performed with the starter kit MBa94xxCA in accordance with EN55022:2010 Class A limits.

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures are provided on the TQMa94xxLA.
The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The operating temperature range for the TQMa94xxLA strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa94xxLA.
The TQMa94xxLA is available in three different variants with different temperature ranges. In general, a reliable operation is given when following conditions are met:

Table 31: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Ambient temperature	–25 °C to +85 °C	–
Extended temperature	–40 °C to +85 °C	–
Storage temperature	-40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Attention: Destruction or malfunction, TQMa94xxLA heat dissipation	
	The TQMa94xxLA belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 94 must be taken into consideration when connecting the heat sink. The i.MX 94 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa94xxLA and thus malfunction, deterioration or destruction.

6.5 Reliability and service life

The calculated MTBF of the TQMa94xxLA is approximately 1107981 h @ +40 °C ambient temperature, Ground, Benign.
The TQMa94xxLA is designed to be insensitive to shock and vibration.

6.6 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa94xxLA is only a sub-component of an overall system.

6.7 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.8 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.
The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa94xxLA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of technical possibilities, the TQMa94xxLA was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7.5 EuP

The Eco Design Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa94xxLA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa94xxLA enable compliance with EuP requirements for the TQMa94xxLA.

7.6 Battery

No batteries are assembled on the TQMa94xxLA.

7.7 Packaging

The TQMa94xxLA is delivered in reusable packaging.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa94xxLA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa94xxLA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))

- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 32: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
ASIL	Automotive Safety Integrity Level
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR	Double Data Rate
DNC	Do Not Connect
DP	DisplayPort
DSI	Display Serial Interface
ECC	Error-Correcting Code
eDP	embedded DisplayPort
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card
ESD	Electrostatic Discharge
eSPI	enhanced Serial Peripheral Interface
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General-Purpose Input/Output
GPMC	General-Purpose Memory Controller
GPO	General-Purpose Output
GPU	Graphics Processing Unit
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IC	Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MIPI	Mobile Industry Processor Interface
MMC	Multimedia Card
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF	Mean (operating) Time Between Failures

8.1 Acronyms and definitions (continued)

Table 32: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
OD	Open-drain
OTG	On-The-Go
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
R/W	Read/Write
RAM	Random Access Memory
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SMBus	System Management Bus
SPI	Serial Peripheral Interface
TBD	To Be Determined
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
VPU	Video Processing Unit
WDT	Watchdog Timer
WEEE®	Waste Electrical and Electronic Equipment
WP	Write Protect

8.2 References

Table 33: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 943 Industrial Application Processors Data Sheet	Rev. 1, 04/2025	NXP
(2)	i.MX 94 Applications Processor Reference Manual	TBD	NXP
(3)	i.MX 94 Mask Set Errata	TBD	NXP
(4)	PF9455 - 9-channel Power Management IC	Rev. 0.21, 10.2024	NXP
(5)	i.MX 94x Preliminary Hardware Developer's Guide	Rev. X1, 01.2024	NXP
(6)	MBa94xxCA User's Manual	– current –	TQ-Systems
(7)	TQMa94xxLA Support-Wiki	– current –	TQ-Systems

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Technology in Quality