TQMa8MxML & TQMa8MxNL
User's Manual

TQMa8MxML UM 0103
04.07.2022

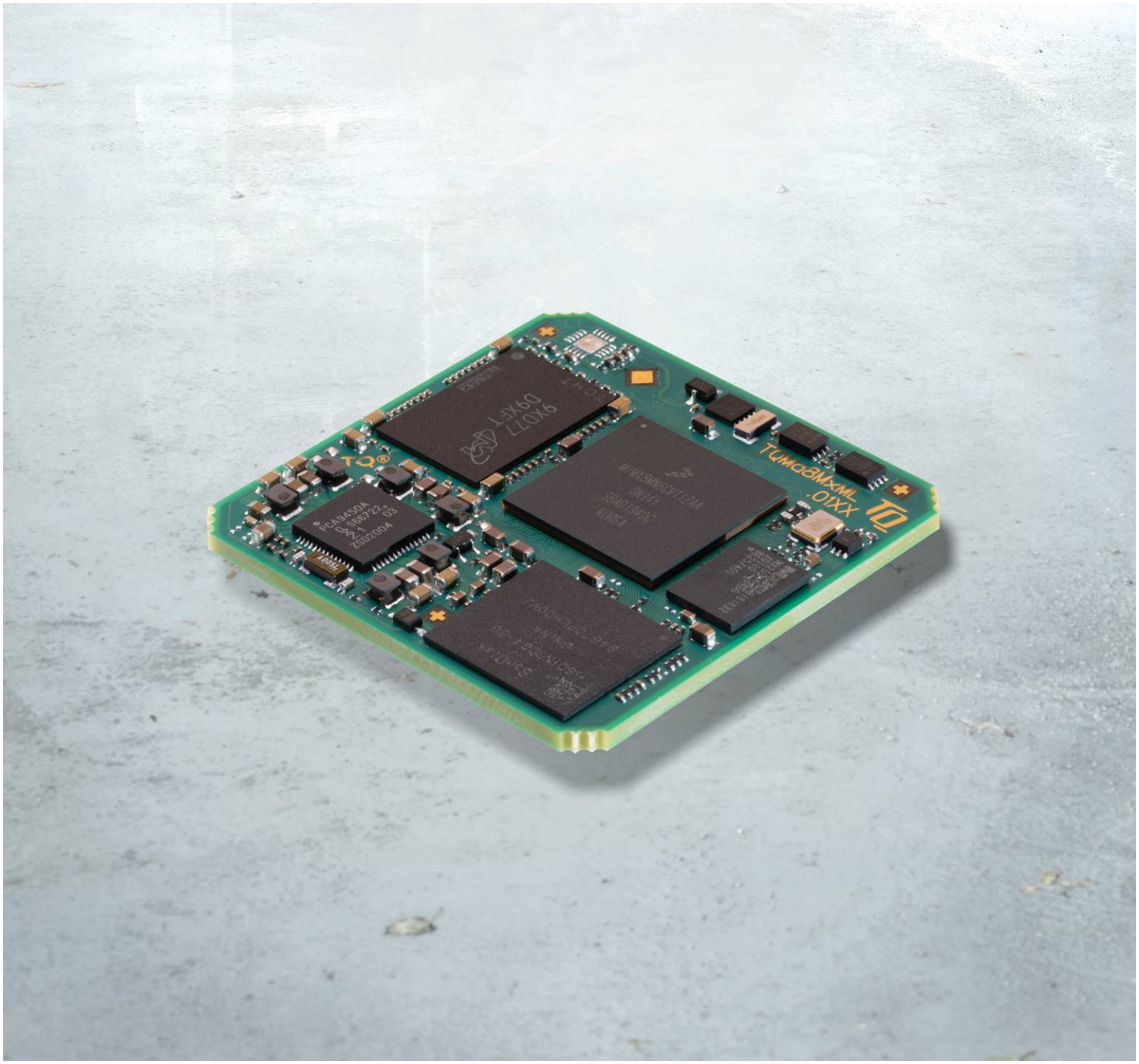

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	20.02.2021	Petz		First issue
0101	04.05.2021	Petz	All 3.2.5.15 Table 37	Non-functional changes, expressions, formatting Information regarding pull-ups added Values added
0102	27.10.2021	Kreuzer	Table 37	Values added
0104	01.07.2022	Kreuzer	Old Table 10 Table 12 Table 13	Old Table 10 removed and subsequent numbering adjusted Recommendations changed Recommendations changed

1. ABOUT THIS MANUAL

1.1 Copyright and license expenses

The drivers and utilities for the components used as well as the BIOS are subject to the copyrights of the respective manufacturers. The licence conditions of the respective manufacturer are to be adhered to.

Bootloader-licence expenses are paid by TQ-Systems GmbH and are included in the price.

Licence expenses for the operating system and applications are not taken into consideration and must be calculated / declared separately.

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Important Notice:

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa8MxML and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer’s advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8Mx circuit diagram
- MBa8Mx User’s Manual
- i.MX 8M Mini Data Sheet
- i.MX 8M Mini Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8MxML

2. BRIEF DESCRIPTION

This User's Manual describes the TQMa8MxML and the TQMa8MxNL each as of revision 0200 and refers to some software settings. This User's Manual does also not replace the NXP i.MX 8M Mini or i.MX 8M Nano documentation, see Table 47.

Note: Designations "TQMa8MxML" and "TQMa8MxNL", available features and interfaces	
	In order to facilitate the readability of this User's Manual, the designations "TQMa8MxML" and "i.MX 8M Mini" are used throughout. If technical aspects require a differentiation between "TQMa8MxML" and "TQMa8MxNL", or "i.MX 8M Mini" and "i.MX 8M Nano", the appropriate designation is used. This User's Manual describes all features and interfaces provided by the TQMa8MxML or TQMa8MxNL family. A certain TQMa8MxML or TQMa8MxNL derivative does not necessarily provide all features and interfaces described in this User's Manual.

The TQMa8MxML is a universal Minimodule based on the NXP ARM CPU i.MX 8M CPU family with ARM Cortex®-A53.
With a TQMa8MxML soldered on the adapter "TQMa8MxML-MB-ADAP", the TQMa8MxML can be operated on the MBa8Mx.

2.1 Key functions and characteristics

The TQMa8MxML extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
All essential i.MX 8M Mini pins are routed to the TQMa8MxML LGA pads. There are therefore no restrictions for customers using the TQMa8MxML with respect to an integrated customised design. All essential components like CPU, LPDDR4, eMMC, and PMIC are already integrated on the TQMa8MxML.

The main features of the TQMa8MxML are:

- 64 bit NXP i.MX 8M Mini CPU, up to 4 × ARM Cortex®-A53 and 1 × Cortex®-M4F
  - Mini Solo, Mini SoloLite, Mini Dual, Mini DualLite, Mini Quad, and Mini QuadLite
- Up to 4 Gbyte 32-bit LPDDR4-3000
- Up to 64 Gbyte eMMC NAND Flash, eMMC standard 5.1
- Up to 256 Mbyte QSPI NOR Flash
- 64 Kbit EEPROM
- Temperature sensor + EEPROM
- RTC
- NXP Power Management Integrated Circuit PCA9450
- All essential i.MX 8M Mini pins are routed to the TQMa8MxML LGA pads
- Plug & Trust Secure Element
- Single supply voltage 5 V

The main features of the TQMa8MxNL are:

- 64 bit NXP i.MX 8M Nano CPU, up to 4 × ARM Cortex®-A53 and 1 × Cortex®-M7
  - Nano Solo, Nano SoloLite, Nano Dual, Nano DualLite, Nano Quad, and Nano QuadLite
- Up to 2 Gbyte 16-bit LPDDR4-3200
- Up to 64 Gbyte eMMC NAND Flash, eMMC standard 5.1
- Up to 256 Mbyte QSPI NOR Flash
- 64 Kbit EEPROM
- Temperature sensor + EEPROM
- RTC
- NXP Power Management Integrated Circuit PCA9450
- All essential i.MX 8M Nano pins are routed to the TQMa8MxNL LGA pads
- Plug & Trust Secure Element
- Single supply voltage 5 V

2.2 CPU block diagrams

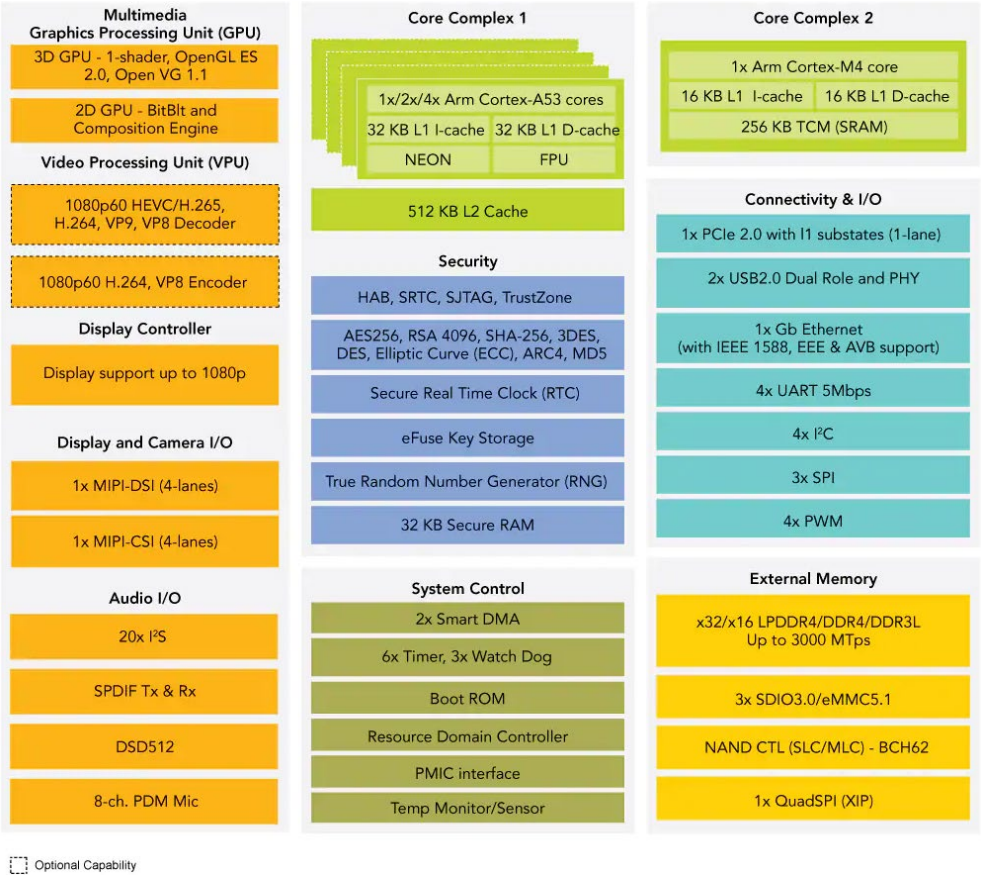

Figure 1: Block diagram i.MX 8M Mini
(Source: NXP)

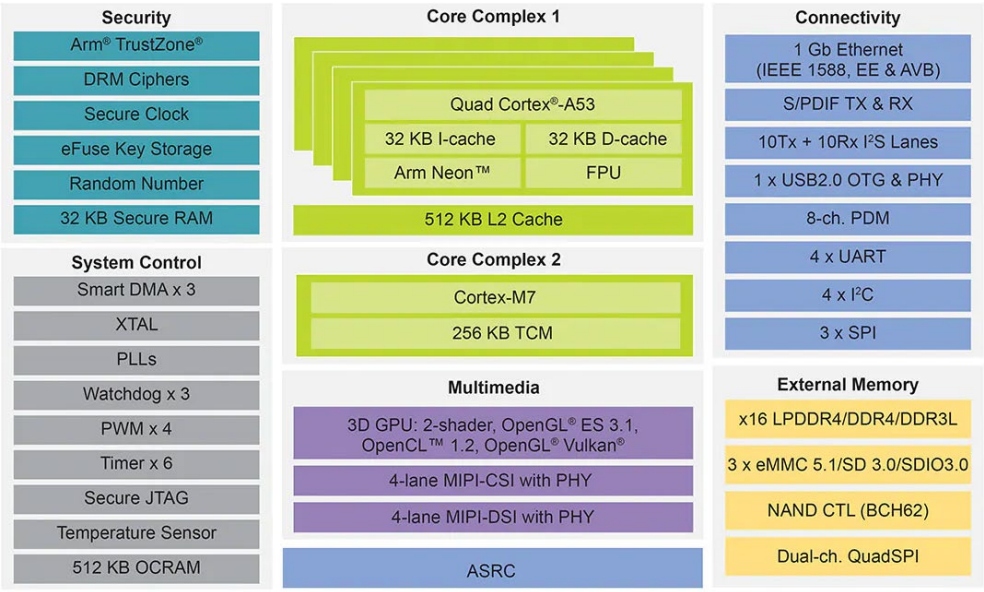

Figure 2: Block diagram i.MX 8M Nano
(Source: NXP)

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa8MxML, and the BSP provided by TQ-Systems GmbH, see also chapter 4.

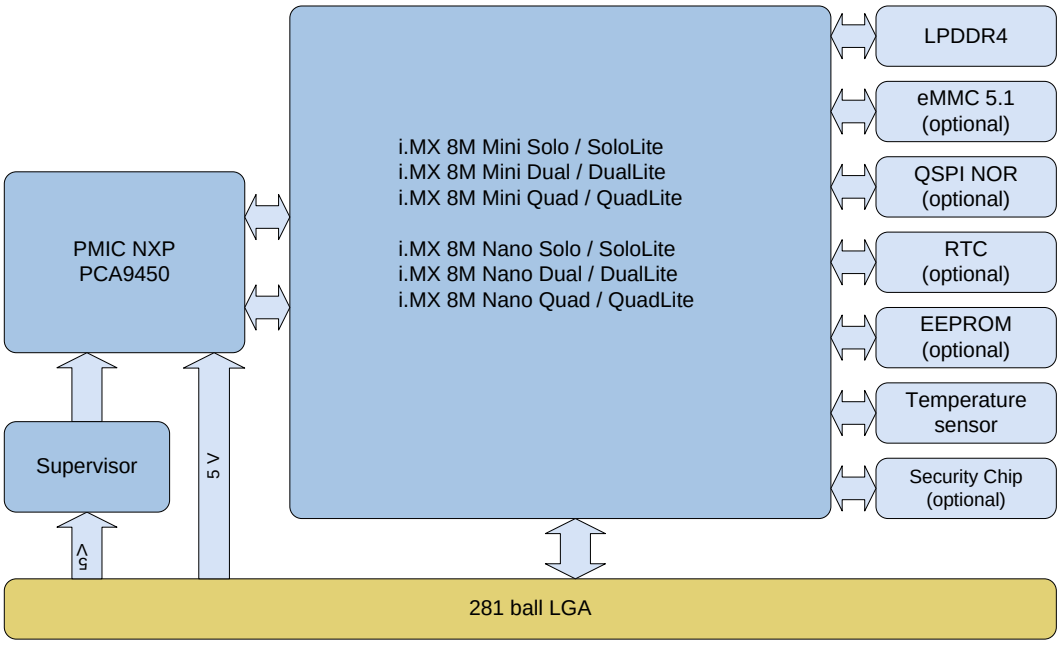

Figure 3: Block diagram TQMa8MxML / TQMa8MxNL (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX 8M Mini/Nano-internal function units must be taken note of.

The pin assignment in Table 3 refers to a TQMa8MxML with i.MX 8M Mini Quad CPU in combination with the Starterkit MBa8Mx.

The pin assignment in Table 5 refers to a TQMa8MxNL with i.MX 8M Nano Quad CPU in combination with the Starterkit MBa8Mx.

A certain i.MX 8M Mini or i.MX 8M Nano derivative listed in Table 7 and Table 8 does not necessarily provide all features described in Table 3 and Table 5. Details are to be taken from (3) and (4).

NXP provides a pin multiplexing tool, which simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).

The electrical and pin characteristics are to be taken from the i.MX 8M Mini and PMIC documentation, see Table 47.

Attention: Destruction or malfunction, pin multiplexing	
	Depending on the configuration, many i.MX 8M Mini pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX 8M Mini Reference Manual (1), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa8MxML. The descriptions given in the following tables should be taken note of: – DNC: These pins must never be connected and have to be left open. Please contact TQ-Support for details.

3.1.1.1 Pinout TQMa8MxML

The TQMa8MxML has a total of 281 LGA pads. The TQMa8MxML is soldered and thus permanently connected to the carrier board. It is not trivial and it is not recommended to remove the TQMa8MxML.
The following table shows the TQMa8MxML pad-out, top view **through** the TQMa8MxML.

Table 2: Pinout TQMa8MxML, top view **through** TQMa8MxML

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	
19		ECSPI2_SCLK	ECSPI2_MISO	ECSPI2_MOSI	GND	DSI_CLK_N	DSI_CLK_P	GND	CSI_D0_N	CSI_D0_P	GND	CSI_D2_N	CSI_D2_P	PCIE_TXN	PCIE_TXP	GND	USB1_DN	USB1_DP		19
18	ECSPI1_MISO	ECSPI1_MOSI	GND	DSI_D0_N	DSI_D0_P	GND	DSI_D2_N	DSI_D2_P	GND	CSI_D1_N	CSI_D1_P	GND	CSI_D3_N	CSI_D3_P	PCIE_RXN	PCIE_RXP	GND	USB2_DN	USB2_DP	18
17	ECSPI1_SCLK	GND	ECSPI2_SS0	GND	DSI_D1_N	DSI_D1_P	GND	DSI_D3_N	DSI_D3_P	GND	CSI_CLK_N	CSI_CLK_P	GND	USB2_ID	USB2_VBUS	PCIE_REF_CLKN	PCIE_REF_CLKP	GND	CLK1_OUT	17
16	GND	ECSPI1_SS0	GND	UART1_TXD	UART1_RXD	UART2_TXD	UART2_RXD	UART3_TXD	UART3_RXD	UART4_TXD	UART4_RXD	GND	USB1_ID	USB1_VBUS	GND	JTAG_TRST#	JTAG_TDI	CLK2_OUT	CLK1_IN	16
15	V_ECSPI	V_UART	GND	V_LICELL	GND	ISO_7816_CLK	GND									JTAG_TDO	JTAG_TMS	GND	CLK2_IN	15
14	GND	SAI3_TXD	I2C4_SCL	GND	RTC_EVENT#	ISO_7816_IO1										JTAG_TCK	GND	GPIO2_IO10	GND	14
13	SAI3_TXC	SAI3_TXFS	I2C3_SCL	I2C4_SDA	GND	ISO_7816_IO2										GND	GPIO2_IO02	GPIO2_IO09	GPIO2_IO07	13
12	SAI3_MCLK	SAI3_RXD	I2C3_SDA	GND	TEMP_EVENT#	ISO_7816_RST										GPIO3_IO14	QSPI_A_SCLK	GND	V_ENET	12
11	GND	SAI3_RXFS	GND	I2C2_SCL	TEST_MODE	GND										GPIO2_IO00	GND	GPIO2_IO11	GND	11
10	SAI3_RXC	GND	I2C1_SCL	I2C2_SDA	GND	BOOT_MODE1										GND	QSPI_A_SS0#	QSPI_A_DATA0	GPIO2_IO08	10
9	SAI5_RXD0	SAI5_RXD1	I2C1_SDA	GND	SPDIF_TX	BOOT_MODE0										GPIO2_IO01	QSPI_A_DATA1	QSPI_A_DATA2	QSPI_A_DATA3	9
8	GND	SAI5_RXD2	GND	SPDIF_EXT_CLK	GND	SPDIF_RX	GND									GPIO2_IO06	GPIO2_IO05	GPIO2_IO04	GPIO2_IO03	8
7	SAI5_MCLK	GND	SAI5_RXFS	GND	RESET_IN#	RESET_OUT#	ONOFF	GND							GND	SD2_RST#	GND	GND	GND	7
6	SAI5_RXC	SAI5_RXD3	GND	GND	PMIC_RST#	V_3V3_SD	USB2_OTG_OC	USB1_OTG_OC	USB2_OTG_ID	PMIC_WDOG#	GND	GPIO1_IO06	GPIO1_IO01	GPIO1_IO00	SD2_WP	GND	ENET_MDIO	ENET_MDC	ENET_RD3	6
5	GND	GND	GND	GND	GND	GND	USB2_OTG_PWR	USB1_OTG_PWR	USB1_OTG_ID	M4_NMI	GPIO1_IO09	GPIO1_IO07	GPIO1_IO03	SD2_CD#	GND	SD2_CMD	SD2_CLK	GND	ENET_RD2	5
4	V_5V_IN	V_5V_IN	V_5V_IN	GND	GND	GND	SAI1_RXFS	SAI1_RXD4	GND	SAI1_RXD7	SAI1_TXFS	GND	SAI1_TXD5	SAI1_TXD6	SD2_DATA3	SD2_DATA1	GND	ENET_RD1	GND	4
3	V_5V_IN	V_5V_IN	V_5V_IN	GND	GND	GND	GND	SAI1_RXD3	SAI1_RXD6	GND	SAI1_TXD1	SAI1_TXD3	GND	SAI1_TXD7	SD2_DATA2	GND	SD2_DATA0	ENET_RD0	ENET_RXC	3
2	V_5V_IN	GND	SAI2_RXD	SAI2_RXFS	GND	SAI2_TXFS	SAI1_RXD1	GND	SAI1_RXD5	SAI1_TXC	GND	SAI1_TXD2	SAI1_TXD4	GND	ENET_TX_CTL	ENET_TD3	ENET_TD1	GND	ENET_RX_CTL	2
1		SAI2_RXC	SAI2_MCLK	SAI2_TXC	SAI2_TXD	SAI1_RXC	SAI1_RXD0	SAI1_RXD2	GND	SAI1_MCLK	SAI1_TXD0	GND	V_1V8	V_3V3	GND	ENET_TXC	ENET_TD2	ENET_TD0		1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	

3.1.1.2 TQMa8MxML signals

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX 8M Mini documentation (1), (3), (5), as well as the PMIC Data Sheet (7).

Table 3: TQMa8MxML, signals

CPU ball	Signal	Group	Dir.	Level	TQMa8MxML pad
G26	BOOT_MODE0	Boot_Mode	I	3.3 V	F9
G27	BOOT_MODE1	Boot_Mode	I	3.3 V	F10
H27	CLK1_IN	CLK	I	1.8 V	W16
H26	CLK1_OUT	CLK	O	1.8 V	W17
J27	CLK2_IN	CLK	I	1.8 V	W15
J26	CLK2_OUT	CLK	O	1.8 V	V16
A7	ECSPI1_MISO	ECSPI	I	V_ECSPI	A18
B7	ECSPI1_MOSI	ECSPI	O	V_ECSPI	B18
D6	ECSPI1_SCLK	ECSPI	O	V_ECSPI	A17
B6	ECSPI1_SS0	ECSPI	O	V_ECSPI	B16
A8	ECSPI2_MISO	ECSPI	I	V_ECSPI	C19
B8	ECSPI2_MOSI	ECSPI	O	V_ECSPI	D19
E6	ECSPI2_SCLK	ECSPI	O	V_ECSPI	B19
A6	ECSPI2_SS0	ECSPI	O	V_ECSPI	C17
AC27	ENET_MDC	ENET	O	V_ENET	V6
AB27	ENET_MDIO	ENET	I/O	V_ENET	U6
AE27	ENET_RD0	ENET	I	V_ENET	V3
AD27	ENET_RD1	ENET	I	V_ENET	V4
AD26	ENET_RD2	ENET	I	V_ENET	W5
AC26	ENET_RD3	ENET	I	V_ENET	W6
AF27	ENET_RX_CTL	ENET	I	V_ENET	W2
AE26	ENET_RXC	ENET	I	V_ENET	W3
AG26	ENET_TD0	ENET	O	V_ENET	V1
AF26	ENET_TD1	ENET	O	V_ENET	U2
AG25	ENET_TD2	ENET	O	V_ENET	U1
AF25	ENET_TD3	ENET	O	V_ENET	T2
AF24	ENET_TX_CTL	ENET	O	V_ENET	R2
AG24	ENET_TXC	ENET	O	V_ENET	T1
–	RTC_EVENT#	Event	O	OD [1]	E14
–	TEMP_EVENT#	Event	O	OD [1]	E12

1: Requires PU to 3.3 V.

3.1.1.2 TQMa8MxML signals (continued)

Table 3: TQMa8MxML, signals (continued)

CPU ball	Signal	Group	Dir.	Level	TQMa8MxML pad
AG14	GPIO1_IO00	GPIO	I/O	3.3 V	P6
AF14	GPIO1_IO01	GPIO	I/O	3.3 V	N6
AF13	GPIO1_IO03	GPIO	I/O	3.3 V	N5
AG11	GPIO1_IO06	GPIO	I/O	3.3 V	M6
AF11	GPIO1_IO07	GPIO	I/O	3.3 V	M5
AF10	GPIO1_IO09	GPIO	I/O	3.3 V	L5
V26	GPIO2_IO00	GPIO	I/O	1.8 V	T11
V27	GPIO2_IO01	GPIO	I/O	1.8 V	T9
Y27	GPIO2_IO02	GPIO	I/O	1.8 V	U13
Y26	GPIO2_IO03	GPIO	I/O	1.8 V	W8
T27	GPIO2_IO04	GPIO	I/O	1.8 V	V8
T26	GPIO2_IO05	GPIO	I/O	1.8 V	U8
U27	GPIO2_IO06	GPIO	I/O	1.8 V	T8
U26	GPIO2_IO07	GPIO	I/O	1.8 V	W13
W27	GPIO2_IO08	GPIO	I/O	1.8 V	W10
W26	GPIO2_IO09	GPIO	I/O	1.8 V	V13
R23	GPIO2_IO10	GPIO	I/O	1.8 V	V14
R24	GPIO2_IO11	GPIO	I/O	1.8 V	V11
R22	GPIO3_IO14	GPIO	I/O	1.8 V	T12
E9	I2C1_SCL	I2C	O	3.3 V	C10
F9	I2C1_SDA	I2C	I/O	3.3 V	C9
D10	I2C2_SCL	I2C	O	3.3 V	D11
D9	I2C2_SDA	I2C	I/O	3.3 V	D10
E10	I2C3_SCL	I2C	O	3.3 V	C13
F10	I2C3_SDA	I2C	I/O	3.3 V	C12
D13	I2C4_SCL	I2C	O	3.3 V	C14
E13	I2C4_SDA	I2C	I/O	3.3 V	D13
–	ISO_7816_CLK	ISO_7816	I	3.3 V	F15
–	ISO_7816_IO1	ISO_7816	I/O	3.3 V	F14
–	ISO_7816_IO2	ISO_7816	I/O	3.3 V	F13
–	ISO_7816_RST	ISO_7816	I	3.3 V	F12
F26	JTAG_TCK	JTAG	I	3.3 V	T14
E27	JTAG_TDI	JTAG	I	3.3 V	U16
E26	JTAG_TDO	JTAG	O	3.3 V	T15
F27	JTAG_TMS	JTAG	I	3.3 V	U15
C27	JTAG_TRST#	JTAG	I	3.3 V	T16
AF12	M4_NMI	NMI	I	3.3 V	K5
AG13	PMIC_WDOG#	WDOG	O	3.3 V	K6

3.1.1.2 TQMa8MxML signals (continued)

Table 3: TQMa8MxML, signals (continued)

CPU ball	Signal	Group	Dir.	Level	TQMa8MxML pad
–	GND	A5, A8, A11, A14, A16, B2, B5, B7, B10, B17, C5, C6, C8, C11, C15, C16, C18, D3, D4, D5, D6, D7, D9, D12, D14, D17, E2, E3, E4, E5, E8, E10, E13, E15, E19, F3, F4, F5, F11, F18, G3, G8, G15, G17, H2, H7, H19, J1, J4, J18, K3, K17, L2, L6, L19, M1, M4, M16, M18, N3, N17, P2, R1, R5, R7, R16, T3, T6, T10, T13, T19, U4, U7, U11, U14, U18, V2, V5, V7, V12, V15, V17, W4, W7, W11, W14				
–	V_1V8	Power	P_{out}	1.8 V [2]	N1
–	V_3V3	Power	P_{out}	3.3 V [2]	P1
–	V_3V3_SD	Power	P_{out}	3.3 V [3]	F6
–	V_5V_IN	Power	P_{in}	5 V	A2, A3, A4, B3, B4, C3, C4
H10	V_ECSPI	Power	P_{in}	1.8 / 3.3 V	A15
W22	V_ENET	Power	P_{in}	1.8 / 2.5 / 3.3 V	W12
–	V_LICELL	Power	P_{in}	3 V	D15
J12	V_UART	Power	P_{in}	1.8 / 3.3 V	B15
A16	CSI_CLK_N	MIPI_CSI	I	1.8 V	L17
B16	CSI_CLK_P	MIPI_CSI	I	1.8 V	M17
A14	CSI_D0_N	MIPI_CSI	I	1.8 V	J19
B14	CSI_D0_P	MIPI_CSI	I	1.8 V	K19
A15	CSI_D1_N	MIPI_CSI	I	1.8 V	K18
B15	CSI_D1_P	MIPI_CSI	I	1.8 V	L18
A17	CSI_D2_N	MIPI_CSI	I	1.8 V	M19
B17	CSI_D2_P	MIPI_CSI	I	1.8 V	N19
A18	CSI_D3_N	MIPI_CSI	I	1.8 V	N18
B18	CSI_D3_P	MIPI_CSI	I	1.8 V	P18
A11	DSI_CLK_N	MIPI_DSI	O	1.8 V	F19
B11	DSI_CLK_P	MIPI_DSI	O	1.8 V	G19
A9	DSI_D0_N	MIPI_DSI	O	1.8 V	D18
B9	DSI_D0_P	MIPI_DSI	O	1.8 V	E18
A10	DSI_D1_N	MIPI_DSI	O	1.8 V	E17
B10	DSI_D1_P	MIPI_DSI	O	1.8 V	F17
A12	DSI_D2_N	MIPI_DSI	O	1.8 V	G18
B12	DSI_D2_P	MIPI_DSI	O	1.8 V	H18
A13	DSI_D3_N	MIPI_DSI	O	1.8 V	H17
B13	DSI_D3_P	MIPI_DSI	O	1.8 V	J17
A21	PCIE_REF_CLKN	PCIe	I/O	0.7 V	T17
B21	PCIE_REF_CLKP	PCIe	I/O	0.7 V	U17
A19	PCIE_RXN	PCIe	I	0.7 V	R18
B19	PCIE_RXP	PCIe	I	0.7 V	T18
A20	PCIE_TXN	PCIe	O	0.7 V	P19
B20	PCIE_TXP	PCIe	O	0.7 V	R19

2: Maximum load of 500 mA.
3: Maximum load of 400 mA.

3.1.1.2 TQMa8MxML signals (continued)

Table 3: TQMa8MxML, signals (continued)

CPU ball	Signal	Group	Dir.	Level	TQMa8MxML pad
AB18	SAI1_MCLK	SAI	I/O	3.3 V	K1
AF16	SAI1_RXC	SAI	I	3.3 V	F1
AG15	SAI1_RXD0	SAI	I	3.3 V	G1
AF15	SAI1_RXD1	SAI	I	3.3 V	G2
AG17	SAI1_RXD2	SAI	I	3.3 V	H1
AF17	SAI1_RXD3	SAI	I	3.3 V	H3
AG18	SAI1_RXD4	SAI	I	3.3 V	H4
AF18	SAI1_RXD5	SAI	I	3.3 V	J2
AG19	SAI1_RXD6	SAI	I	3.3 V	J3
AF19	SAI1_RXD7	SAI	I	3.3 V	K4
AG16	SAI1_RXFS	SAI	I	3.3 V	G4
AC18	SAI1_TXC	SAI	O	3.3 V	K2
AG20	SAI1_TXD0	SAI	O	3.3 V	L1
AF20	SAI1_TXD1	SAI	O	3.3 V	L3
AG21	SAI1_TXD2	SAI	O	3.3 V	M2
AF21	SAI1_TXD3	SAI	O	3.3 V	M3
AG22	SAI1_TXD4	SAI	O	3.3 V	N2
AF22	SAI1_TXD5	SAI	O	3.3 V	N4
AG23	SAI1_TXD6	SAI	O	3.3 V	P4
AF23	SAI1_TXD7	SAI	O	3.3 V	P3
AB19	SAI1_TXFS	SAI	O	3.3 V	L4
AD19	SAI2_MCLK	SAI	I/O	3.3 V	C1
AB22	SAI2_RXC	SAI	I	3.3 V	B1
AC24	SAI2_RXD	SAI	I	3.3 V	C2
AC19	SAI2_RXFS	SAI	I	3.3 V	D2
AD22	SAI2_TXC	SAI	O	3.3 V	D1
AC22	SAI2_TXD	SAI	O	3.3 V	E1
AD23	SAI2_TXFS	SAI	O	3.3 V	F2
AD6	SAI3_MCLK	SAI	I/O	3.3 V	A12
AG7	SAI3_RXC	SAI	I	3.3 V	A10
AF7	SAI3_RXD	SAI	I	3.3 V	B12
AG8	SAI3_RXFS	SAI	I	3.3 V	B11
AG6	SAI3_TXC	SAI	O	3.3 V	A13
AF6	SAI3_TXD	SAI	O	3.3 V	B14
AC6	SAI3_TXFS	SAI	O	3.3 V	B13
AD15	SAI5_MCLK	SAI	I/O	3.3 V	A7
AC15	SAI5_RXC	SAI	I	3.3 V	A6
AD18	SAI5_RXD0	SAI	I	3.3 V	A9
AC14	SAI5_RXD1	SAI	I	3.3 V	B9
AD13	SAI5_RXD2	SAI	I	3.3 V	B8
AC13	SAI5_RXD3	SAI	I	3.3 V	B6
AB15	SAI5_RXFS	SAI	I	3.3 V	C7

3.1.1.2 TQMa8MxML signals (continued)

Table 3: TQMa8MxML, signals (continued)

CPU ball	Signal	Group	Dir.	Level	TQMa8MxML pad
P23	QSPI_A_DATA0	QSPI	I/O	1.8 V	V10
K24	QSPI_A_DATA1	QSPI	I/O	1.8 V	U9
K23	QSPI_A_DATA2	QSPI	I/O	1.8 V	V9
N23	QSPI_A_DATA3	QSPI	I/O	1.8 V	W9
N22	QSPI_A_SCLK	QSPI	O	1.8 V	U12
N24	QSPI_A_SS0#	QSPI	O	1.8 V	U10
–	PMIC_RST#	Reset	I	1.8 V	E6
–	RESET_IN#	Reset	I	OD [4]	E7
–	RESET_OUT#	Reset	O	OD [4]	F7
AA26	SD2_CD#	SD	I	1.8 / 3.3 V	P5
W23	SD2_CLK	SD	O	1.8 / 3.3 V	U5
W24	SD2_CMD	SD	I/O	1.8 / 3.3 V	T5
AB23	SD2_DATA0	SD	I/O	1.8 / 3.3 V	U3
AB24	SD2_DATA1	SD	I/O	1.8 / 3.3 V	T4
V24	SD2_DATA2	SD	I/O	1.8 / 3.3 V	R3
V23	SD2_DATA3	SD	I/O	1.8 / 3.3 V	R4
AB26	SD2_RST#	SD	O	1.8 / 3.3 V	T7
AA27	SD2_WP	SD	I	1.8 / 3.3 V	R6
A25	ONOFF	SNVS	I	1.8 V	G7
AF8	SPDIF_EXT_CLK	SPDIF	I	3.3 V	D8
AG9	SPDIF_RX	SPDIF	I	3.3 V	F8
AF9	SPDIF_TX	SPDIF	O	3.3 V	E9
D26	TEST_MODE	TEST	I	3.3 V	E11
E14	UART1_RXD	UART	I	V_UART	E16
F13	UART1_TXD	UART	O	V_UART	D16
F15	UART2_RXD	UART	I	V_UART	G16
E15	UART2_TXD	UART	O	V_UART	F16
E18	UART3_RXD	UART	I	V_UART	J16
D18	UART3_TXD	UART	O	V_UART	H16
F19	UART4_RXD	UART	I	V_UART	L16
F18	UART4_TXD	UART	O	V_UART	K16
A22	USB1_DN	USB	I/O	3.3 V	U19
B22	USB1_DP	USB	I/O	3.3 V	V19
D22	USB1_ID	USB	I	1.8 V	N16
F22	USB1_VBUS	USB	P	5 V	P16
AD10	USB1_OTG_ID	USB	I	3.3 V	J5
AD9	USB1_OTG_OC	USB	I	3.3 V	H6
AB10	USB1_OTG_PWR	USB	O	3.3 V	H5
A23	USB2_DN	USB	I/O	3.3 V	V18
B23	USB2_DP	USB	I/O	3.3 V	W18
D23	USB2_ID	USB	I	1.8 V	P17
F23	USB2_VBUS	USB	P	5 V	R17
AC10	USB2_OTG_ID	USB	I	3.3 V	J6
AB9	USB2_OTG_OC	USB	I	3.3 V	G6
AC9	USB2_OTG_PWR	USB	O	3.3 V	G5

4: Requires PU to 1.8 V, max. 3.6 V.

3.1.1.3 Pinout TQMa8MxNL

The TQMa8MxNL has a total of 281 LGA pads. The TQMa8MxNL is soldered and thus permanently connected to the carrier board. It is not trivial and it is not recommended to remove the TQMa8MxNL.
The following table shows the TQMa8MxNL pad-out, top view **through** the TQMa8MxNL.

Table 4: Pinout TQMa8MxNL, top view **through** TQMa8MxNL

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	
19		ECSPI2_SCLK	ECSPI2_MISO	ECSPI2_MOSI	GND	DSI_CLK_N	DSI_CLK_P	GND	CSI_D0_N	CSI_D0_P	GND	CSI_D2_N	CSI_D2_P	(NC)	(NC)	GND	USB1_DN	USB1_DP		19
18	ECSPI1_MISO	ECSPI1_MOSI	GND	DSI_D0_N	DSI_D0_P	GND	DSI_D2_N	DSI_D2_P	GND	CSI_D1_N	CSI_D1_P	GND	CSI_D3_N	CSI_D3_P	(NC)	(NC)	GND	(NC)	(NC)	18
17	ECSPI1_SCLK	GND	ECSPI2_SS0	GND	DSI_D1_N	DSI_D1_P	GND	DSI_D3_N	DSI_D3_P	GND	CSI_CLK_N	CSI_CLK_P	GND	(NC)	(NC)	(NC)	(NC)	GND	CLK1_OUT	17
16	GND	ECSPI1_SS0	GND	UART1_TXD	UART1_RXD	UART2_TXD	UART2_RXD	UART3_TXD	UART3_RXD	UART4_TXD	UART4_RXD	GND	USB1_ID	USB1_VBUS	GND	BOOT_MODE2	JTAG_TDI	CLK2_OUT	CLK1_IN	16
15	V_ECSPI	V_UART	GND	V_LICELL	GND	ISO_7816_CLK	GND									JTAG_TDO	JTAG_TMS	GND	CLK2_IN	15
14	GND	SAI3_TXD	I2C4_SCL	GND	RTC_EVENT#	ISO_7816_IO1										JTAG_TCK	GND	GPIO2_IO10	GND	14
13	SAI3_TXC	SAI3_TXFS	I2C3_SCL	I2C4_SDA	GND	ISO_7816_IO2										GND	GPIO2_IO02	GPIO2_IO09	GPIO2_IO07	13
12	SAI3_MCLK	SAI3_RXD	I2C3_SDA	GND	TEMP_EVENT#	ISO_7816_RST										GPIO3_IO14	QSPI_A_SCLK	GND	V_ENET	12
11	GND	SAI3_RXFS	GND	I2C2_SCL	BOOT_MODE3	GND										GPIO2_IO00	GND	GPIO2_IO11	GND	11
10	SAI3_RXC	GND	I2C1_SCL	I2C2_SDA	GND	BOOT_MODE1										GND	QSPI_A_SS0#	QSPI_A_DATA0	GPIO2_IO08	10
9	SAI5_RXD0	SAI5_RXD1	I2C1_SDA	GND	SPDIF_TX	BOOT_MODE0										GPIO2_IO01	QSPI_A_DATA1	QSPI_A_DATA2	QSPI_A_DATA3	9
8	GND	SAI5_RXD2	GND	SPDIF_EXT_CLK	GND	SPDIF_RX	GND									GPIO2_IO06	GPIO2_IO05	GPIO2_IO04	GPIO2_IO03	8
7	SAI5_MCLK	GND	SAI5_RXFS	GND	RESET_IN#	RESET_OUT#	ONOFF	GND							GND	SD2_RST#	GND	GND	GND	7
6	SAI5_RXC	SAI5_RXD3	GND	GND	PMIC_RST#	V_3V3_SD	GPIO1_IO15	USB1_OTG_OC	GPIO1_IO11	PMIC_WDOG#	GND	GPIO1_IO06	GPIO1_IO01	GPIO1_IO00	SD2_WP	GND	ENET_MDIO	ENET_MDC	ENET_RD3	6
5	GND	GND	GND	GND	GND	GND	GPIO1_IO14	USB1_OTG_PWR	USB1_OTG_ID	M7_NMI	GPIO1_IO09	GPIO1_IO07	GPIO1_IO03	SD2_CD#	GND	SD2_CMD	SD2_CLK	GND	ENET_RD2	5
4	V_5V_IN	V_5V_IN	V_5V_IN	GND	GND	GND	(NC)	(NC)	GND	(NC)	(NC)	GND	(NC)	(NC)	SD2_DATA3	SD2_DATA1	GND	ENET_RD1	GND	4
3	V_5V_IN	V_5V_IN	V_5V_IN	GND	GND	GND	GND	(NC)	(NC)	GND	(NC)	(NC)	GND	(NC)	SD2_DATA2	GND	SD2_DATA0	ENET_RD0	ENET_RXC	3
2	V_5V_IN	GND	SAI2_RXD	SAI2_RXFS	GND	SAI2_TXFS	(NC)	GND	(NC)	(NC)	GND	(NC)	(NC)	GND	ENET_TX_CTL	ENET_TD3	ENET_TD1	GND	ENET_RX_CTL	2
1		SAI2_RXC	SAI2_MCLK	SAI2_TXC	SAI2_TXD	(NC)	(NC)	(NC)	GND	(NC)	(NC)	GND	V_1V8	V_3V3	GND	ENET_TXC	ENET_TD2	ENET_TD0		1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	

3.1.1.4 TQMa8MxNL signals

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX 8M Nano documentation (2), (4), (6), as well as the PMIC Data Sheet (7).

Table 5: TQMa8MxNL, signals

CPU ball	Signal	Group	Dir.	Level	TQMa8MxNL pad
G26	BOOT_MODE0	Boot_Mode	I	3.3 V	F9
G27	BOOT_MODE1	Boot_Mode	I	3.3 V	F10
C27	BOOT_MODE2	Boot_Mode	I	3.3 V	T16
D26	BOOT_MODE3	Boot_Mode	I	3.3 V	E11
H27	CLK1_IN	CLK	I	1.8 V	W16
H26	CLK1_OUT	CLK	O	1.8 V	W17
J27	CLK2_IN	CLK	I	1.8 V	W15
J26	CLK2_OUT	CLK	O	1.8 V	V16
A7	ECSPI1_MISO	ECSPI	I	V_ECSPI	A18
B7	ECSPI1_MOSI	ECSPI	O	V_ECSPI	B18
D6	ECSPI1_SCLK	ECSPI	O	V_ECSPI	A17
B6	ECSPI1_SS0	ECSPI	O	V_ECSPI	B16
A8	ECSPI2_MISO	ECSPI	I	V_ECSPI	C19
B8	ECSPI2_MOSI	ECSPI	O	V_ECSPI	D19
E6	ECSPI2_SCLK	ECSPI	O	V_ECSPI	B19
A6	ECSPI2_SS0	ECSPI	O	V_ECSPI	C17
AC27	ENET_MDC	ENET	O	V_ENET	V6
AB27	ENET_MDIO	ENET	I/O	V_ENET	U6
AE27	ENET_RD0	ENET	I	V_ENET	V3
AD27	ENET_RD1	ENET	I	V_ENET	V4
AD26	ENET_RD2	ENET	I	V_ENET	W5
AC26	ENET_RD3	ENET	I	V_ENET	W6
AF27	ENET_RX_CTL	ENET	I	V_ENET	W2
AE26	ENET_RXC	ENET	I	V_ENET	W3
AG26	ENET_TD0	ENET	O	V_ENET	V1
AF26	ENET_TD1	ENET	O	V_ENET	U2
AG25	ENET_TD2	ENET	O	V_ENET	U1
AF25	ENET_TD3	ENET	O	V_ENET	T2
AF24	ENET_TX_CTL	ENET	O	V_ENET	R2
AG24	ENET_TXC	ENET	O	V_ENET	T1
–	RTC_EVENT#	Event	O	OD [5]	E14
–	TEMP_EVENT#	Event	O	OD [5]	E12
E9	I2C1_SCL	I2C	O	3.3 V	C10
F9	I2C1_SDA	I2C	I/O	3.3 V	C9
D10	I2C2_SCL	I2C	O	3.3 V	D11
D9	I2C2_SDA	I2C	I/O	3.3 V	D10
E10	I2C3_SCL	I2C	O	3.3 V	C13
F10	I2C3_SDA	I2C	I/O	3.3 V	C12
D13	I2C4_SCL	I2C	O	3.3 V	C14
E13	I2C4_SDA	I2C	I/O	3.3 V	D13
AF12	M7_NMI	NMI	I	3.3 V	K5
AG13	PMIC_WDOG#	WDOG	O	3.3 V	K6

5: Requires PU to 3.3 V.

3.1.1.4 TQMa8MxNL signals (continued)

Table 5: TQMa8MxNL, signals (continued)

CPU ball	Signal	Group	Dir.	Level	TQMa8MxNL pad
AG14	GPIO1_IO00	GPIO	I/O	3.3 V	P6
AF14	GPIO1_IO01	GPIO	I/O	3.3 V	N6
AF13	GPIO1_IO03	GPIO	I/O	3.3 V	N5
AG11	GPIO1_IO06	GPIO	I/O	3.3 V	M6
AF11	GPIO1_IO07	GPIO	I/O	3.3 V	M5
AF10	GPIO1_IO09	GPIO	I/O	3.3 V	L5
AC10	GPIO1_IO11	GPIO	I/O	3.3 V	J6
AC9	GPIO1_IO14	GPIO	I/O	3.3 V	G5
AB9	GPIO1_IO15	GPIO	I/O	3.3 V	G6
V26	GPIO2_IO00	GPIO	I/O	1.8 V	T11
V27	GPIO2_IO01	GPIO	I/O	1.8 V	T9
Y27	GPIO2_IO02	GPIO	I/O	1.8 V	U13
Y26	GPIO2_IO03	GPIO	I/O	1.8 V	W8
T27	GPIO2_IO04	GPIO	I/O	1.8 V	V8
T26	GPIO2_IO05	GPIO	I/O	1.8 V	U8
U27	GPIO2_IO06	GPIO	I/O	1.8 V	T8
U26	GPIO2_IO07	GPIO	I/O	1.8 V	W13
W27	GPIO2_IO08	GPIO	I/O	1.8 V	W10
W26	GPIO2_IO09	GPIO	I/O	1.8 V	V13
R23	GPIO2_IO10	GPIO	I/O	1.8 V	V14
R24	GPIO2_IO11	GPIO	I/O	1.8 V	V11
R22	GPIO3_IO14	GPIO	I/O	1.8 V	T12
–	ISO_7816_CLK	ISO_7816	I	3.3 V	F15
–	ISO_7816_IO1	ISO_7816	I/O	3.3 V	F14
–	ISO_7816_IO2	ISO_7816	I/O	3.3 V	F13
–	ISO_7816_RST	ISO_7816	I	3.3 V	F12
F26	JTAG_TCK	JTAG	I	3.3 V	T14
E27	JTAG_TDI	JTAG	I	3.3 V	U16
E26	JTAG_TDO	JTAG	O	3.3 V	T15
F27	JTAG_TMS	JTAG	I	3.3 V	U15
A16	CSI_CLK_N	MIPI_CSI	I	1.8 V	L17
B16	CSI_CLK_P	MIPI_CSI	I	1.8 V	M17
A14	CSI_D0_N	MIPI_CSI	I	1.8 V	J19
B14	CSI_D0_P	MIPI_CSI	I	1.8 V	K19
A15	CSI_D1_N	MIPI_CSI	I	1.8 V	K18
B15	CSI_D1_P	MIPI_CSI	I	1.8 V	L18
A17	CSI_D2_N	MIPI_CSI	I	1.8 V	M19
B17	CSI_D2_P	MIPI_CSI	I	1.8 V	N19
A18	CSI_D3_N	MIPI_CSI	I	1.8 V	N18
B18	CSI_D3_P	MIPI_CSI	I	1.8 V	P18
A11	DSI_CLK_N	MIPI_DSI	O	1.8 V	F19
B11	DSI_CLK_P	MIPI_DSI	O	1.8 V	G19
A9	DSI_D0_N	MIPI_DSI	O	1.8 V	D18
B9	DSI_D0_P	MIPI_DSI	O	1.8 V	E18
A10	DSI_D1_N	MIPI_DSI	O	1.8 V	E17
B10	DSI_D1_P	MIPI_DSI	O	1.8 V	F17
A12	DSI_D2_N	MIPI_DSI	O	1.8 V	G18
B12	DSI_D2_P	MIPI_DSI	O	1.8 V	H18
A13	DSI_D3_N	MIPI_DSI	O	1.8 V	H17
B13	DSI_D3_P	MIPI_DSI	O	1.8 V	J17

3.1.1.4 TQMa8MxNL signals (continued)

Table 5: TQMa8MxNL, signals (continued)

CPU ball	Signal	Group	Dir.	Level	TQMa8MxNL pad
–	GND	A5, A8, A11, A14, A16, B2, B5, B7, B10, B17, C5, C6, C8, C11, C15, C16, C18, D3, D4, D5, D6, D7, D9, D12, D14, D17, E2, E3, E4, E5, E8, E10, E13, E15, E19, F3, F4, F5, F11, F18, G3, G8, G15, G17, H2, H7, H19, J1, J4, J18, K3, K17, L2, L6, L19, M1, M4, M16, M18, N3, N17, P2, R1, R5, R7, R16, T3, T6, T10, T13, T19, U4, U7, U11, U14, U18, V2, V5, V7, V12, V15, V17, W4, W7, W11, W14				
–	NC	F1, G1, G2, G4, G5, G6, H1, H3, H4, J2, J3, J6, K1, K2, K4, L1, L3, L4, M2, M3, N2, N4, P17, P19, P3, P4, R17, R18, R19, T17, T18, U17, V18, W18			
–	V_1V8	Power	P_{out}	1.8 V [6]	N1
–	V_3V3	Power	P_{out}	3.3 V [6]	P1
–	V_3V3_SD	Power	P_{out}	3.3 V [7]	F6
–	V_5V_IN	Power	P_{in}	5 V	A2, A3, A4, B3, B4, C3, C4
H10	V_ECSPI	Power	P_{in}	1.8 / 3.3 V	A15
W22	V_ENET	Power	P_{in}	1.8 / 2.5 / 3.3 V	W12
–	V_LICELL	Power	P_{in}	3 V	D15
J12	V_UART	Power	P_{in}	1.8 / 3.3 V	B15
P23	QSPI_A_DATA0	QSPI	I/O	1.8 V	V10
K24	QSPI_A_DATA1	QSPI	I/O	1.8 V	U9
K23	QSPI_A_DATA2	QSPI	I/O	1.8 V	V9
N23	QSPI_A_DATA3	QSPI	I/O	1.8 V	W9
N22	QSPI_A_SCLK	QSPI	O	1.8 V	U12
N24	QSPI_A_SS0#	QSPI	O	1.8 V	U10
–	PMIC_RST#	Reset	I	1.8 V	E6
–	RESET_IN#	Reset	I	OD [8]	E7
–	RESET_OUT#	Reset	O	OD [8]	F7
AD19	SAI2_MCLK	SAI	I/O	3.3 V	C1
AB22	SAI2_RXC	SAI	I	3.3 V	B1
AC24	SAI2_RXD	SAI	I	3.3 V	C2
AC19	SAI2_RXFS	SAI	I	3.3 V	D2
AD22	SAI2_TXC	SAI	O	3.3 V	D1
AC22	SAI2_TXD	SAI	O	3.3 V	E1
AD23	SAI2_TXFS	SAI	O	3.3 V	F2
AD6	SAI3_MCLK	SAI	I/O	3.3 V	A12
AG7	SAI3_RXC	SAI	I	3.3 V	A10
AF7	SAI3_RXD	SAI	I	3.3 V	B12
AG8	SAI3_RXFS	SAI	I	3.3 V	B11
AG6	SAI3_TXC	SAI	O	3.3 V	A13
AF6	SAI3_TXD	SAI	O	3.3 V	B14
AC6	SAI3_TXFS	SAI	O	3.3 V	B13
AD15	SAI5_MCLK	SAI	I/O	3.3 V	A7
AC15	SAI5_RXC	SAI	I	3.3 V	A6
AD18	SAI5_RXD0	SAI	I	3.3 V	A9
AC14	SAI5_RXD1	SAI	I	3.3 V	B9
AD13	SAI5_RXD2	SAI	I	3.3 V	B8
AC13	SAI5_RXD3	SAI	I	3.3 V	B6
AB15	SAI5_RXFS	SAI	I	3.3 V	C7

6: Maximum load of 500 mA.
7: Maximum load of 400 mA.
8: Requires PU to 1.8 V, max. 3.6 V.

3.1.1.4 TQMa8MxNL signals (continued)

Table 5: TQMa8MxNL, signals (continued)

CPU ball	Signal	Group	Dir.	Level	TQMa8MxNL pad
AA26	SD2_CD#	SD	I	1.8 / 3.3 V	P5
W23	SD2_CLK	SD	O	1.8 / 3.3 V	U5
W24	SD2_CMD	SD	I/O	1.8 / 3.3 V	T5
AB23	SD2_DATA0	SD	I/O	1.8 / 3.3 V	U3
AB24	SD2_DATA1	SD	I/O	1.8 / 3.3 V	T4
V24	SD2_DATA2	SD	I/O	1.8 / 3.3 V	R3
V23	SD2_DATA3	SD	I/O	1.8 / 3.3 V	R4
AB26	SD2_RST#	SD	O	1.8 / 3.3 V	T7
AA27	SD2_WP	SD	I	1.8 / 3.3 V	R6
A25	ONOFF	SNVS	I	1.8 V	G7
AF8	SPDIF_EXT_CLK	SPDIF	I	3.3 V	D8
AG9	SPDIF_RX	SPDIF	I	3.3 V	F8
AF9	SPDIF_TX	SPDIF	O	3.3 V	E9
E14	UART1_RXD	UART	I	V_UART	E16
F13	UART1_TXD	UART	O	V_UART	D16
F15	UART2_RXD	UART	I	V_UART	G16
E15	UART2_TXD	UART	O	V_UART	F16
E18	UART3_RXD	UART	I	V_UART	J16
D18	UART3_TXD	UART	O	V_UART	H16
F19	UART4_RXD	UART	I	V_UART	L16
F18	UART4_TXD	UART	O	V_UART	K16
A22	USB1_DN	USB	I/O	3.3 V	U19
B22	USB1_DP	USB	I/O	3.3 V	V19
D22	USB1_ID	USB	I	1.8 V	N16
AD10	USB1_OTG_ID	USB	I	3.3 V	J5
AD9	USB1_OTG_OC	USB	I	3.3 V	H6
AB10	USB1_OTG_PWR	USB	O	3.3 V	H5
F22	USB1_VBUS	USB	P	5 V	P16

3.1.1.5 Differences between TQMa8MxML and TQMa8MxNL

The following table shows the differences between TQMa8MxML and TQMa8MxNL.

Table 6: Differences between TQMa8MxML and TQMa8MxNL

CPU ball	Module pad	TQMa8MxML signal	TQMa8MxNL signal
C27	T16	JTAG_TRST#	BOOT_MODE2
D26	E11	TEST_MODE	BOOT_MODE3
A21	T17	PCIE_REF_CLKN	(NC)
B21	U17	PCIE_REF_CLKP	(NC)
A19	R18	PCIE_RXN	(NC)
B19	T18	PCIE_RXP	(NC)
A20	P19	PCIE_TXN	(NC)
B20	R19	PCIE_TXP	(NC)
AB18	K1	SAI1_MCLK	(NC)
AF16	F1	SAI1_RXC	(NC)
AG15	G1	SAI1_RXD0	(NC)
AF15	G2	SAI1_RXD1	(NC)
AG17	H1	SAI1_RXD2	(NC)
AF17	H3	SAI1_RXD3	(NC)
AG18	H4	SAI1_RXD4	(NC)
AF18	J2	SAI1_RXD5	(NC)
AG19	J3	SAI1_RXD6	(NC)
AF19	K4	SAI1_RXD7	(NC)
AG16	G4	SAI1_RXFS	(NC)
AC18	K2	SAI1_TXC	(NC)
AG20	L1	SAI1_TXD0	(NC)
AF20	L3	SAI1_TXD1	(NC)
AG21	M2	SAI1_TXD2	(NC)
AF21	M3	SAI1_TXD3	(NC)
AG22	N2	SAI1_TXD4	(NC)
AF22	N4	SAI1_TXD5	(NC)
AG23	P4	SAI1_TXD6	(NC)
AF23	P3	SAI1_TXD7	(NC)
AB19	L4	SAI1_TXFS	(NC)
A23	V18	USB2_DN	(NC)
B23	W18	USB2_DP	(NC)
D23	P17	USB2_ID	(NC)
F23	R17	USB2_VBUS	(NC)
AC10	J6	USB2_OTG_ID	GPIO1_IO11
AC9	G5	USB2_OTG_PWR	GPIO1_IO14
AB9	G6	USB2_OTG_OC	GPIO1_IO15

3.2 System components

3.2.1 i.MX 8M Mini and i.MX 8M Nano derivatives

3.2.1.1 i.MX 8M Mini derivatives

Depending on the TQMa8MxML version, one of the following i.MX 8M Mini derivatives is assembled.

Table 7: i.MX 8M Mini derivatives

TQMa8MxML version	i.MX 8M Mini derivative	i.MX 8M Mini clock	Temperature range
TQMa8MSML-XX	i.MX 8M Mini Solo	A53: 1.6 GHz, M4: 400 MHz	–40 °C … +105 °C
TQMa8MSMLL-XX	i.MX 8M Mini SoloLite	A53: 1.6 GHz, M4: 400 MHz	–40 °C … +105 °C
TQMa8MDML-XX	i.MX 8M Mini Dual	A53: 1.6 GHz, M4: 400 MHz	–40 °C … +105 °C
TQMa8MDMLL-XX	i.MX 8M Mini DualLite	A53: 1.6 GHz, M4: 400 MHz	–40 °C … +105 °C
TQMa8MQML-XX	i.MX 8M Mini Quad	A53: 1.6 GHz, M4: 400 MHz	–40 °C … +105 °C
TQMa8MQMLL-XX	i.MX 8M Mini QuadLite	A53: 1.6 GHz, M4: 400 MHz	–40 °C … +105 °C

3.2.1.2 i.MX 8M Nano derivatives

Depending on the TQMa8MxNL version, one of the following i.MX 8M Nano derivatives is assembled.

Table 8: i.MX 8M Nano derivatives

TQMa8MxNL version	i.MX 8M Nano derivative	i.MX 8M Nano clock	Temperature range
TQMa8MSNL-XX	i.MX 8M Nano Solo	A53: 1.4 GHz, M7: 600 MHz	–40 °C … +105 °C
TQMa8MSNLL-XX	i.MX 8M Nano SoloLite	A53: 1.4 GHz, M7: 600 MHz	–40 °C … +105 °C
TQMa8MDNL-XX	i.MX 8M Nano Dual	A53: 1.4 GHz, M7: 600 MHz	–40 °C … +105 °C
TQMa8MDNLL-XX	i.MX 8M Nano DualLite	A53: 1.4 GHz, M7: 600 MHz	–40 °C … +105 °C
TQMa8MQNL-XX	i.MX 8M Nano Quad	A53: 1.4 GHz, M7: 600 MHz	–40 °C … +105 °C
TQMa8MQNLL-XX	i.MX 8M Nano QuadLite	A53: 1.4 GHz, M7: 600 MHz	–40 °C … +105 °C

3.2.1.3 i.MX 8M Mini / i.MX 8M Nano, main differences

The following table lists the main differences between i.MX 8M Mini and i.MX 8M Nano.

Table 9: i.MX 8M Mini / i.MX 8M Nano, main differences

Function	i.MX 8M Mini	i.MX 8M Nano
Main CPU	4 × Cortex®-A53 @ 1.6 GHz	4 × Cortex®-A53 @ 1.4 GHz
Sub CPU	1 × Cortex®-M4F @ 400 MHz	1 × Cortex®-M7 @ 600 MHz
SDRAM	32-bit LPDDR4-3000	16-bit LPDDR4-3200
GPU	GC NanoUltra + GC520L	GC7000UL
VPU	1080p60	–
Interfaces	PCIe	–
	2 × USB 2.0	1 × USB 2.0

3.2.1.4 i.MX 8M Mini errata

Attention: Destruction or malfunction, i.MX 8M Mini errata, i.MX 8M Nano errata	
	Please take note of the current i.MX 8M Mini errata (8), and i.MX 8M Nano errata (9).

3.2.1.5 Boot Modes

The i.MX 8M Mini and i.MX 8M Nano CPUs boot in different ways. However, both have a ROM with integrated boot loader.

After the release of PMIC_POR# the System Controller (SCU) boots from the internal ROM and then loads the program image from the selected boot device. For example, the integrated eMMC or the SPI NOR Flash can be selected as the default boot device. The following boot sources are supported by TQMa8MxML and TQMa8MxNL:

- eMMC
- QSPI NOR
- USB OTG
- SD card

More information about the boot flow can be found in the Reference Manuals (1), (2), and the Data Sheets (3), (4) of i.MX 8M Mini and i.MX 8M Nano. Alternatively, an image can be loaded into the internal RAM using the serial downloader.

3.2.1.6 Boot configuration i.MX 8M Mini

The i.MX 8M Mini uses two BOOT_MODE pins, which are available on the TQMa8MxML's LGA pads. These require pull-up or pull-down wiring to 3.3 V and Ground. The pull-up voltage used must be stable before the release of IMX_POR.

It is strongly recommended to use V_3V3 as pull-up voltage to ensure a reliable boot behaviour.

The recommended settings of the config pins for the respective interface are highlighted in blue.

The exact boot behaviour depends on the BT_FUSE_SEL register value.

The following table shows the behaviour in dependence of BT_FUSE_SEL and selected Boot Mode:

Table 10: Boot Modes i.MX 8M Mini

BOOT_MODE[1:0]	Boot type	BT_FUSE_SEL	Usage
`00` (default)	Boot from eFuses	0: Boot using Serial Loader (default) 1: Boot Mode configuration is taken from eFuses	Series
`01`	Serial Downloader	Boot using Serial-Loader (USB OTG1)	Development / Testing
`10`	Internal Boot	0: Boot Mode configuration is taken from GPIOs (default) 1: Boot Mode configuration is taken from eFuses.	Development
`11`	(Reserved)	(n/a)	(n/a)

If Internal Boot is used, a detailed setting can be done with CFG Fuses. The CFG Fuses are multiplexed on the SAI1 interface pins and require pull-up or pull-down resistors. With BOOT_CFG15 a general setting can be made independent of the boot device:

Table 11: General boot configuration

Fuse	Signal	TQMa8MxML	Setting
BOOT_CFG15	SAI1_TXD7	P3	Infinite Loop (for debugging): 0: Disabled 1: Enabled

3.2.1.6.1 Boot device eMMC

Table 12: Boot configuration eMMC at USDHC3

Fuse	Signal	TQMa8MxML	Setting
BOOT_CFG14	SAI1_TXD6	P4	Boot Device: 010: MMC/eMMC
BOOT_CFG13	SAI1_TXD5	N4	
BOOT_CFG12	SAI1_TXD4	N2	
BOOT_CFG11	SAI1_TXD3	M3	Port Selection: 00: uSDHC1 01: uSDHC2 10: uSDHC3
BOOT_CFG10	SAI1_TXD2	M2	
BOOT_CFG9	SAI1_TXD1	L3	Power Cycle Enable: 0: No power cycle 1: Enabled
BOOT_CFG7	SAI1_RXD7	K4	Boot Speed: 0: Normal/Regular Boot 1: Fast Boot
BOOT_CFG6	SAI1_RXD6	J3	Bus Width: 000: 1 bit 001: 4 bit 010: 8 bit 101: 4 bit DDR (MMC 4.4) 110: 8 bit DDR (MMC 4.4)
BOOT_CFG5	SAI1_RXD5	J2	
BOOT_CFG4	SAI1_RXD4	H4	
BOOT_CFG3	SAI1_RXD3	H3	Speed Selection: 00: Normal Speed 01: High Speed 10: Reserved for HS200
BOOT_CFG2	SAI1_RXD2	H1	
BOOT_CFG1	SAI1_RXD1	G2	USDHC I/O Voltage (Normal Boot): 0: 3.3 V 1: 1.8 V
BOOT_CFG0	SAI1_RXD0	G1	USDHC I/O Voltage (Manufacture Mode): 0: 3.3 V 1: 1.8 V

3.2.1.6.2 Boot device SD card

Table 13: Boot configuration SD card at USDHC2

Fuse	Signal	TQMa8MxML	Setting
BOOT_CFG14	SAI1_TXD6	P4	Boot Device: 001: SD/eSD
BOOT_CFG13	SAI1_TXD5	N4	
BOOT_CFG12	SAI1_TXD4	N2	
BOOT_CFG11	SAI1_TXD3	M3	Port Selection: 00: uSDHC1 01: uSDHC2 10: uSDHC3
BOOT_CFG10	SAI1_TXD2	M2	
BOOT_CFG9	SAI1_TXD1	L3	Power Cycle Enable: 0: No power cycle 1: Enabled
BOOT_CFG8	SAI1_TXD0	L1	SD Loopback Clock Source: 0: Through SD pad 1: Direct
BOOT_CFG7	SAI1_RXD7	K4	Boot Speed: 0: Normal/Regular Boot 1: Fast Boot
BOOT_CFG4	SAI1_RXD4	H4	Bus Width: 0: 1 bit 1: 4 bit
BOOT_CFG3	SAI1_RXD3	H3	Speed Selection: 000: Normal / SDR12 001: High / SDR25 010: SDR50 011: SDR104 101: Reserved for DDR50
BOOT_CFG2	SAI1_RXD2	H1	
BOOT_CFG1	SAI1_RXD1	G2	

3.2.1.6.3 Boot device QSPI NOR

Table 14: Boot configuration QSPI NOR at QSPI_A

Fuse	Signal	TQMa8MxML	Setting
BOOT_CFG14	SAI1_TXD6	P4	Boot Device: 100: QSPI
BOOT_CFG13	SAI1_TXD5	N4	
BOOT_CFG12	SAI1_TXD4	N2	
BOOT_CFG10	SAI1_TXD2	M2	Flash Type: 000: 3B read 001: 4B read 010: Hyperflash 1V8 011: Hyperflash 3V3 100: MXIC Octal DDR
BOOT_CFG9	SAI1_TXD1	L3	
BOOT_CFG8	SAI1_TXD0	L1	
BOOT_CFG7	SAI1_RXD7	K4	Hold Time: 00: 500 µsec 01: 1 msec 10: 3 msec 11: 10 msec
BOOT_CFG6	SAI1_RXD6	J3	

3.2.1.7 Boot configuration i.MX 8M Nano

The i.MX 8M Nano uses four signals to select the boot source. The signals JTAG_TRST# and TEST_MODE are additionally used.
To use these pins as boot selection pins, they require a pull-up/pull-down wiring to 3.3 V or Ground.
It is strongly recommended to use V_3V3 as pull-up voltage to ensure a reliable boot behaviour.

Table 15: Boot configuration i.MX 8M Nano

Boot source	BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0
Boot from eFuse	0	0	0	0
Serial Downloader (USB OTG1)	0	0	0	1
Boot from USDHC3 (eMMC)	0	0	1	0
Boot from USDHC2 (SD card)	0	0	1	1
Boot from NAND (not supported)	0	1	0	x
Boot from QSPI (3 Byte Read)	0	1	1	0
Boot from QSPI (Hyperflash)	0	1	1	1
Boot from eCSPI (not supported)	1	0	0	0
(Reserved)	1	0	0	1

Booting from USDHC1 is only possible on the i.MX 8M Nano after burning the fuses and is therefore not used. DCD is not supported by the i.MX 8M Nano.

3.2.2 Memory

3.2.2.1 LPDDR4 SDRAM

An LPDDR4 SDRAM chip is assembled on the TQMa8MxML or TQMa8MxNL.
The following table shows details of the SDRAM assembled:

Table 16: LPDDR4 SDRAM on TQMa8MxML or TQMa8MxNL

Module	Interface width	Max. size	JEDEC standard	I/O clock
TQMa8MxML	32 bit	4 Gbyte	LPDDR4-3000	1500 MHz
TQMa8MxNL	16 bit	2 Gbyte	LPDDR4-3200	1600 MHz

3.2.2.2 eMMC NAND Flash

An eMMC NAND Flash is provided on the TQMa8MxML for boot loader and application software.
The eMMC is connected to the i.MX 8M Mini via USDHC3.
The i.MX 8M Mini and i.MX 8M Nano support transfer modes up to the current eMMC standard v5.1 according to JESD84-B51.
In DDR mode (HS400) data rates of up to 400 Mbyte/s can be achieved.
The boot configuration is described in chapter 3.2.1.5

3.2.2.3 QSPI NOR Flash

The i.MX 8M Mini has two QSPI interfaces, of which QSPI_A is occupied on the TQMa8MxML when QSPI NOR Flash is populated. If no QSPI NOR Flash is populated on the TQMa8MxML, the QSPI_A interface signals can be used on the carrier board.
The following block diagram shows how the QSPI NOR Flash is connected to the i.MX 8M Mini.

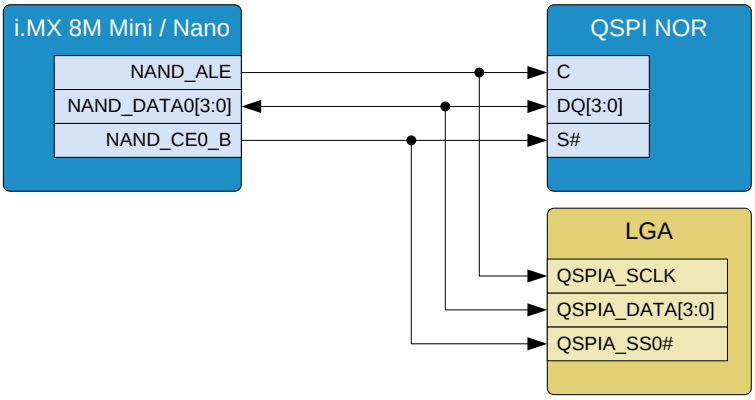

Figure 4: Block diagram QSPI NOR Flash interface

3.2.2.4 EEPROM 24LC64T

A serial EEPROM, controlled by the I2C1 bus, is assembled. Write-Protection (WP) is not supported by default but available as an assembly option. The following block diagram shows how the EEPROM is connected to the i.MX 8M Mini.

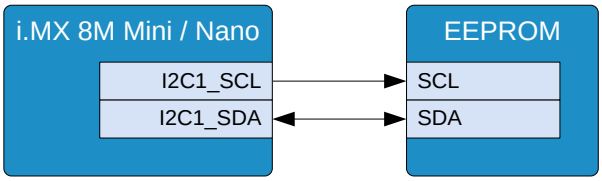

Figure 5: Block diagram EEPROM interface

A 64 Kbit EEPROM 24LC64T is assembled by default on the TQMa8MxML.

- The EEPROM has I²C address `0x57 / 101 0111b`

3.2.2.5 EEPROM with temperature sensor SE97BTP

A serial EEPROM including temperature sensor type SE97BTP, controlled by the I2C1 bus, is assembled on the TQMa8MxML.
The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write-Protected Mode (PWP) or to Reversible Write-Protected Mode (RWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage. The overtemperature output of the SE97BTP is connected as open drain to TQMa8MxML pad E12 (TEMP_EVENT#).
This requires a pull-up to 3.3 V on the carrier board.
The device is assembled on the top side of the TQMa8MxML, see component D12, Figure 28.

- The device provides the following I²C addresses:
  - EEPROM (Normal Mode): `0x53 / 101 0011b`
  - EEPROM (Protection Mode): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

3.2.3 Trust Secure Element SE050

As an option, a Trust Secure Element NXP SE050 can be assembled on the TQMa8MxML. The SE050 is connected to the I2C1 bus. The ISO14443 signals are routed to the I2C4 interface, which is no longer available in this case.

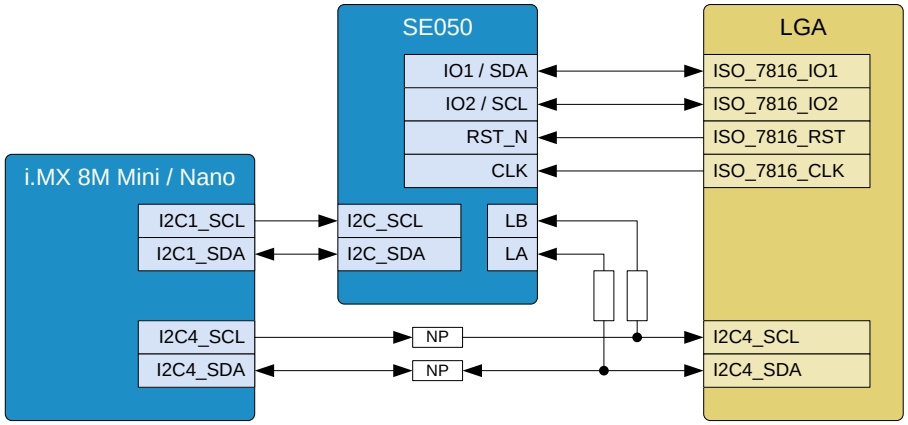

Figure 6: Block diagram Trust Secure Element

The antenna for ISO 14443, or the sensor for ISO 7816, must be connected on the carrier board.
The following TQMa8MxML signals are used to provide the smartcard interfaces.

Table 17: Trust Secure Element signals

Signal	ISO signal name	TQMa8MxML	Power group
ISO_7816_IO1	ISO 7816 IO1 / SDA	F14	V_3V3
ISO_7816_IO2	ISO 7816 IO2 / SCL	F13	
ISO_7816_RST	ISO 7816 RST#	F12	
ISO_7816_CLK	ISO 7816 CLK	F15	
I2C4_SCL	ISO 14443 LB	C14	ISO 14443 (Antenna)
I2C4_SDA	ISO 14443 LA	D13	

- The Trust Secure Element has I²C address `0x48 / 100 1000b`

Unused signals should be terminated as follows:

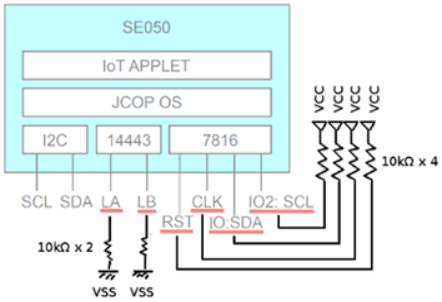

Figure 7: Termination of unused SE050 signals

Note: Signal availability I2C4	
	For TQMa8MxML variants with populated Trust Secure Element, the I2C4 signals listed in the above table are disconnected from the i.MX 8M Mini and thus no longer available.

3.2.4 RTC

The TQMa8MxML provides an i.MX 8M Mini-internal RTC or a discrete RTC PCF85063A.

3.2.4.1 i.MX 8M Mini-internal RTC

The i.MX 8M Mini provides an RTC, which has its own power domain (V_0V8_SNVS). The RTC power domain SNVS of the i.MX 8M Mini is supplied by the PMIC. The PMIC is supplied by the TQMa8MxML input voltage of V_5V_IN.
The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

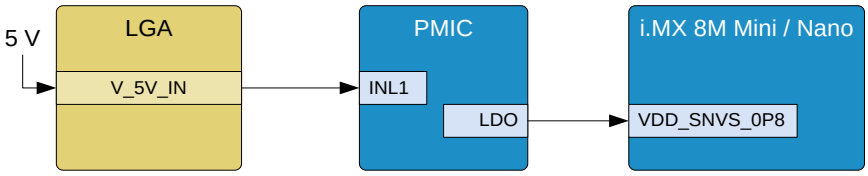

Figure 8: Block diagram RTC supply (TQMa8MxML without discrete RTC)

Note: RTC power supply	
	The CPU internal RTC can be used in regular operation. If the TQMa8MxML supply (5 V) fails, it is no longer available, since the i.MX 8M Mini's SNVS rail is no longer supplied.

3.2.4.2 Discrete RTC PCF85063A

In addition to the i.MX 8M Mini-internal RTC the TQMa8MxML provides a discrete RTC PCF85063A, which is connected to I2C1.
The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.
The discrete RTC has an interrupt output which provides the open-drain signal at LGA pad E14 (RTC_EVENT#).
This pad requires a pull-up to 3.3 V on the carrier board.
The RTC PCF85063A is only directly supplied by V_LICELL when the PMIC or the TQMa8MxML supply is switched off.
During normal operation of the TQMa8MxML, the PMIC supplies 3.3 V.

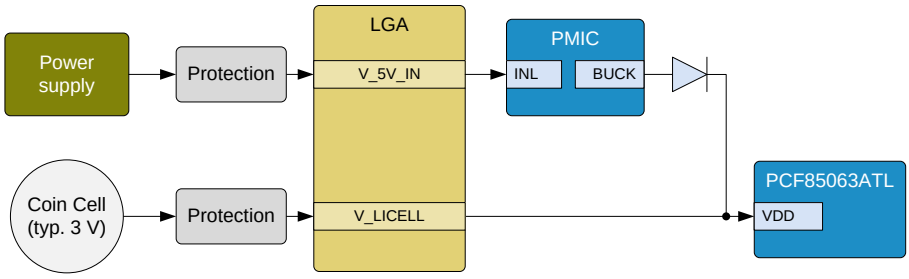

Figure 9: Block diagram RTC supply (TQMa8MxML with discrete RTC)

- The discrete RTC has I²C address `0x51 / 101 0001b`

Note: RTC power supply	
	The SNVS functions of the i.MX 8M Mini can only be used if the TQMa8MxML is supplied with 5 V. It is not possible to obtain these functions by a separate supply during a reset. Since the SNVS rail is not supplied when the TQMa8MxML is not powered-up, it is recommended to use the optional RTC PCF85063A.

3.2.5 Interfaces

3.2.5.1 Overview

The following interfaces or signals are not available on the TQMa8MxML LGA pads and are used on the TQMa8MxML.

Table 18: Internal interfaces

Interface	Chapter	Remark
USDHC3	3.2.2.2	eMMC, 8 bit
SDRAM	3.2.2.1	LPDDR4, 32 bit
GPIO1_IO04 / SD2_VSELECT	3.2.5.15	–
GPIO1_IO08 / IRQ#	–	PMIC Interrupt Request
RTC_RESET#	–	PMIC Reset output pin

3.2.5.2 ENET

The i.MX 8M Mini provides an Ethernet MAC which can operate in Gigabit full duplex mode.
RMII and RGMII can be used as interfaces, with RGMII being used for standard multiplexing.
The supply voltage must be set externally to 1.8 V, 2.5 V or 3.3 V via LGA pad V_ENET.
RMII is supported at 1.8 V and 3.3 V, RGMII at 1.8 V and 2.5 V. See also chapter 3.2.9.6.

The following table shows the signals used in RGMII mode.

Table 19: ENET signals in RGMII mode

Signal	Direction	CPU ball	TQMa8MxML	Power group
ENET_MDC	O	AC27	V6	V_ENET
ENET_MDIO	I/O	AB27	U6	
ENET_RD0	I	AE27	V3	
ENET_RD1	I	AD27	V4	
ENET_RD2	I	AD26	W5	
ENET_RD3	I	AC26	W6	
ENET_RX_CTL	I	AF27	W2	
ENET_RXC	I	AE26	W3	
ENET_TD0	O	AG26	V1	
ENET_TD1	O	AF26	U2	
ENET_TD2	O	AG25	U1	
ENET_TD3	O	AF25	T2	
ENET_TX_CTL	O	AF24	R2	
ENET_TXC	O	AG24	T1	

In RMII mode the following TQMa8MxML signals are omitted:

- ENET_TD3
- ENET_RD3
- ENET_RD2

3.2.5.3 GPIO

Except for the dedicated differential signals, e.g., MIPI DSI/CSI, and USB, all CPU signals routed to the TQMa8MxML LGA pads can be configured as GPIO.

The following table shows the GPIO signals primarily configured as GPIO.

Table 20: GPIO signals

Signal	CPU ball	TQMa8MxML	Power group
GPIO1_IO00	AG14	P6	V_3V3
GPIO1_IO01	AF14	N6	
GPIO1_IO03	AF13	N5	
GPIO1_IO06	AG11	M6	
GPIO1_IO07	AF11	M5	
GPIO1_IO09	AF10	L5	
GPIO2_IO00	V26	T11	V_1V8
GPIO2_IO01	V27	T9	
GPIO2_IO02	Y27	U13	
GPIO2_IO03	Y26	W8	
GPIO2_IO04	T27	V8	
GPIO2_IO05	T26	U8	
GPIO2_IO06	U27	T8	
GPIO2_IO07	U26	W13	
GPIO2_IO08	W27	W10	
GPIO2_IO09	W26	V13	
GPIO2_IO10	R23	V14	
GPIO2_IO11	R24	V11	
GPIO3_IO14	R22	T12	

The electrical characteristics of the GPIOs are to be taken from the i.MX 8M Mini Data Sheet (4).

3.2.5.4 I²C

All four I²C interfaces provided by the i.MX 8M Mini are routed to TQMa8MxML LGA pads.

All I²C devices on the TQMa8MxML are connected to I2C1. If more devices are connected to the I2C1 bus on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional pull-ups should be provided at the I²C bus on the carrier board, if required.

I2C4 is not available when Trust Secure Element SE050 is assembled.

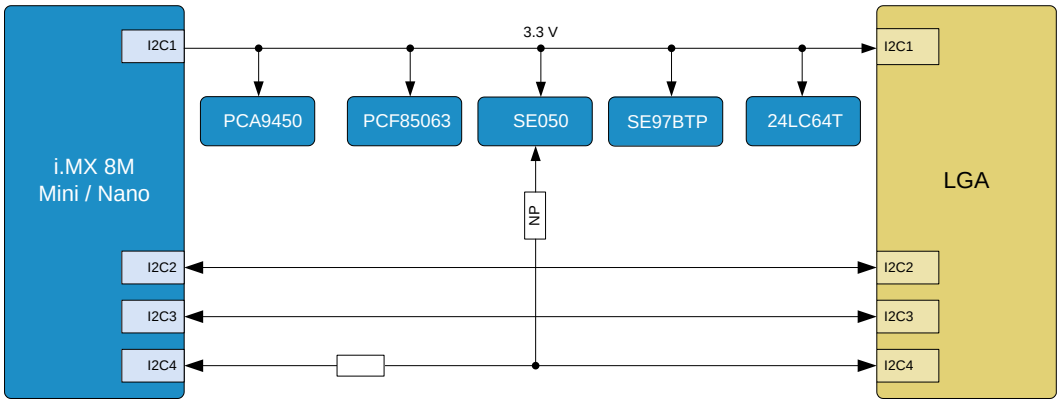

Figure 10: Block diagram I²C

The following table shows the signals used by the I²C interfaces.

Table 21: I²C signals

Signal	Direction	CPU ball	TQMa8MxML	Power group	Remark
I2C1_SCL	O	E9	C10	V_3V3	4.7 kΩ PU to 3.3 V on TQMa8MxML
I2C1_SDA	I/O	F9	C9		4.7 kΩ PU to 3.3 V on TQMa8MxML
I2C2_SCL	O	D10	D11		No PU on TQMa8MxML
I2C2_SDA	I/O	D9	D10		No PU on TQMa8MxML
I2C3_SCL	O	E10	C13		No PU on TQMa8MxML
I2C3_SDA	I/O	F10	C12		No PU on TQMa8MxML
I2C4_SCL [9]	O	D13	C14		No PU on TQMa8MxML
I2C4_SDA [9]	I/O	E13	D13		No PU on TQMa8MxML

The following table shows the I²C devices connected to the I2C1 bus on the TQMa8MxML.

Table 22: Address assignment I2C1 bus

Component	Function	7-bit address
PCA9450	PMIC	`0x25 / 010 0101b`
24LC64T	EEPROM (optional)	`0x57 / 101 0111b`
PCF85063A	RTC (optional)	`0x51 / 101 0001b`
SE97BTP	EEPROM (Normal Mode)	`0x53 / 101 0011b`
	EEPROM (Protection Mode)	`0x33 / 011 0011b`
	Temperature sensor in EEPROM	`0x1B / 001 1011b`
SE050	Trust Secure Element (optional)	`0x48 / 100 1000b`

9: I2C4 is not available when Trust Secure Element SE050 is assembled.

3.2.5.5 JTAG

On the TQMa8MxML JTAG_TRST# is available for the JTAG interface. On the TQMa8MxNL, JTAG_TRST# is used as BOOT_MODE2 and is therefore not available in the JTAG interface. In this case an external pull circuit must be provided on the carrier board for this signal to enable the setting of the different Boot Modes.

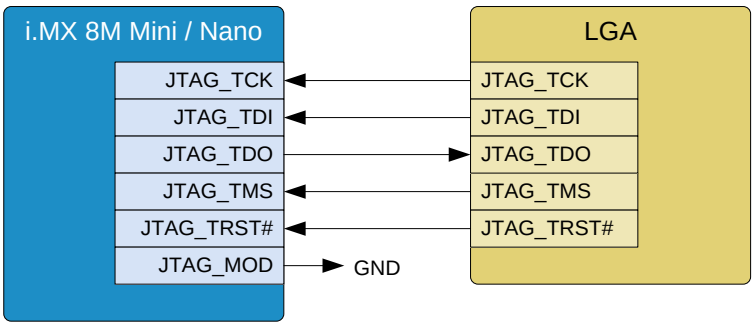

Figure 11: Block diagram JTAG interface

The following table shows the signals used by the JTAG interface.

Table 23: JTAG signals

Signal	Direction	CPU ball	TQMa8MxML	Power group	Remark
JTAG_TCK	I	F26	T14	V_3V3	10 kΩ PD on TQMa8MxML
JTAG_TDI	I	E27	U16		–
JTAG_TDO	O	E26	T15		–
JTAG_TMS	I	F27	U15		–
JTAG_TRST#	I	C27	T16		Not available with TQMa8MxNL

3.2.5.6 MIPI CSI

The i.MX 8M Mini provides a MIPI-CSI camera interface. Up to 1.5 Gbps are transmitted on four data pairs. Image formats up to 4K @ 30 fps are supported.

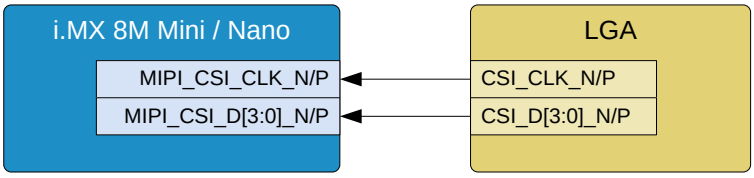

Figure 12: Block diagram MIPI CSI

The following table shows the signals used by the MIPI CSI interface.

Table 24: MIPI CSI signals

Signal	CPU ball	TQMa8MxML	Power group
CSI_CLK_N	A16	L17	V_1V8_ANA
CSI_CLK_P	B16	M17	
CSI_D0_N	A14	J19	
CSI_D0_P	B14	K19	
CSI_D1_N	A15	K18	
CSI_D1_P	B15	L18	
CSI_D2_N	A17	M19	
CSI_D2_P	B17	N19	
CSI_D3_N	A18	N18	
CSI_D3_P	B18	P18	

3.2.5.7 MIPI DSI

The i.MX 8M Mini provides a DSI interface to output serial display data.
The MIPI-DSI PHY supports resolutions up to 1080p @ 60 fps.

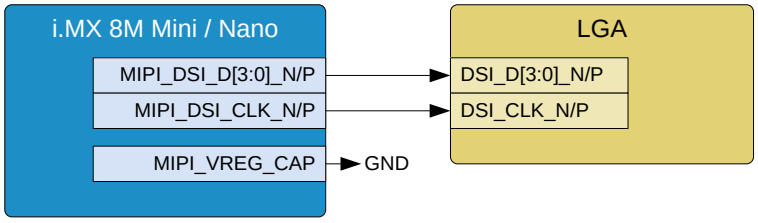

Figure 13: Block diagram MIPI DSI

The following table shows the signals used by the MIPI DSI interface.

Table 25: MIPI DSI signals

Signal	CPU ball	TQMa8MxML	Power group
DSI_CLK_N	A11	F19	V_1V8_ANA
DSI_CLK_P	B11	G19	
DSI_D0_N	A9	D18	
DSI_D0_P	B9	E18	
DSI_D1_N	A10	E17	
DSI_D1_P	B10	F17	
DSI_D2_N	A12	G18	
DSI_D2_P	B12	H18	
DSI_D3_N	A13	H17	
DSI_D3_P	B13	J17	

3.2.5.8 PCIe

The i.MX 8M Mini provides one PCIe 2.0 lane, the i.MX 8M Nano does not provide this feature.
The 100 MHz reference clock can be generated on the TQMa8MxML and output to PCIE_REF_CLKN/P for the PCIe card.
The 100 MHz reference clock can be generated internally and output to PCIE_REF_CLKN/P for the PCIe card.
Alternatively, the reference clock can be provided from an external source to PCIE_REF_CLKN/P.
The PCIe card must be supplied by the carrier board.
The series capacitors required by the PCIe standard must be provided on the carrier board.

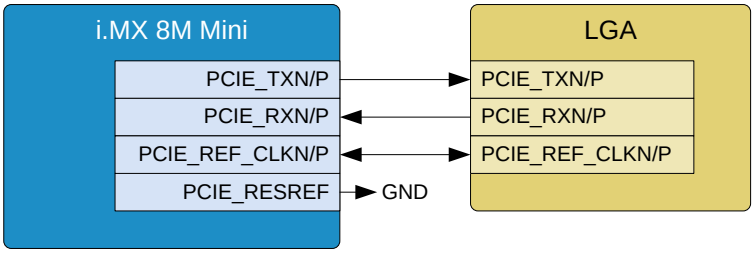

Figure 14: Block diagram PCIe

The following table shows the signals used by the PCIe interface.

Table 26: PCIe signals

Signal	Direction	CPU ball	TQMa8MxML	Power group
PCIE_REF_CLKN	I or O [10]	A21	T17	V_1V8_ANA
PCIE_REF_CLKP		B21	U17	
PCIE_RXN	I	A19	R18	
PCIE_RXP		B19	T18	
PCIE_TXN	O	A20	P19	
PCIE_TXP		B20	R19	

Note: TQMa8MxNL, termination of PCIe interface pins	
	The TQMa8MxNL does not offer a PCIe interface. The i.MX 8M Nano nevertheless features the pins, which are connected to the LGA pads of the TQMa8MxNL. Therefore, it is recommended to terminate the signals externally when using the TQMa8MxNL.

10: Direction depends on configuration.

3.2.5.9 SAI

Because of the focus on audio functions, i.MX 8M Mini and i.MX 8M Nano offer several SAI interfaces. These are partially full-duplex capable. I^2S, AC97, TDM and other codecs are supported, but they have to be implemented on the carrier board.
The supply voltage of all SAI interfaces is set to 3.3 V by the TQMa8MxML.

The i.MX 8M Nano does not provide the SAI1 interface. Therefore, external signal termination is required for TQMa8MxNL modules. 10 kΩ to Ground are recommended. Clock pins can be used as input or output.

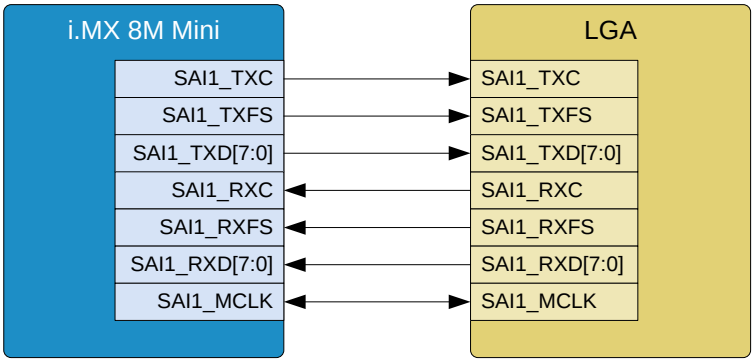

Figure 15: Block diagram SAI1

The signals of SAI2, SAI3 and SA5 are routed to the LGA pads in the same way, see Table 28.

Note: TQMa8MxNL, termination of SAI1 interface pins	
	The TQMa8MxNL does not offer the SAI1 interface. The i.MX 8M Nano nevertheless features the pins, which are connected to the LGA pads of the TQMa8MxNL. Therefore, it is recommended to terminate the signals externally when using the TQMa8MxNL. There is no exact specification, which is why 10 kΩ to Ground are recommended.

3.2.5.9 SAI (continued)

The following table shows the signals used by the SAI interface.

Table 27: SAI signals

Signal	Direction	CPU ball	TQMa8MxML	TQMa8MxNL	Power group
SAI1_MCLK	I/O	AB18	K1	(NC)	V_3V3
SAI1_RXC	I	AF16	F1	(NC)	
SAI1_RXD0	I	AG15	G1	(NC)	
SAI1_RXD1	I	AF15	G2	(NC)	
SAI1_RXD2	I	AG17	H1	(NC)	
SAI1_RXD3	I	AF17	H3	(NC)	
SAI1_RXD4	I	AG18	H4	(NC)	
SAI1_RXD5	I	AF18	J2	(NC)	
SAI1_RXD6	I	AG19	J3	(NC)	
SAI1_RXD7	I	AF19	K4	(NC)	
SAI1_RXFS	I	AG16	G4	(NC)	
SAI1_TXC	O	AC18	K2	(NC)	
SAI1_TXD0	O	AG20	L1	(NC)	
SAI1_TXD1	O	AF20	L3	(NC)	
SAI1_TXD2	O	AG21	M2	(NC)	
SAI1_TXD3	O	AF21	M3	(NC)	
SAI1_TXD4	O	AG22	N2	(NC)	
SAI1_TXD5	O	AF22	N4	(NC)	
SAI1_TXD6	O	AG23	P4	(NC)	
SAI1_TXD7	O	AF23	P3	(NC)	
SAI1_TXFS	O	AB19	L4	(NC)	
SAI2_MCLK	I/O	AD19	C1	C1	
SAI2_RXC	I	AB22	B1	B1	
SAI2_RXD	I	AC24	C2	C2	
SAI2_RXFS	I	AC19	D2	D2	
SAI2_TXC	O	AD22	D1	D1	
SAI2_TXD	O	AC22	E1	E1	
SAI2_TXFS	O	AD23	F2	F2	
SAI3_MCLK	I/O	AD6	A12	A12	
SAI3_RXC	I	AG7	A10	A10	
SAI3_RXD	I	AF7	B12	B12	
SAI3_RXFS	I	AG8	B11	B11	
SAI3_TXC	O	AG6	A13	A13	
SAI3_TXD	O	AF6	B14	B14	
SAI3_TXFS	O	AC6	B13	B13	
SAI5_MCLK	I/O	AD15	A7	A7	
SAI5_RXC	I	AC15	A6	A6	
SAI5_RXD0	I	AD18	A9	A9	
SAI5_RXD1	I	AC14	B9	B9	
SAI5_RXD2	I	AD13	B8	B8	
SAI5_RXD3	I	AC13	B6	B6	
SAI5_RXFS	I	AB15	C7	C7	

3.2.5.10 SPDIF

The i.MX 8M Mini provides an SPDIF interface, which is routed to the TQMa8MxML LGA pads.

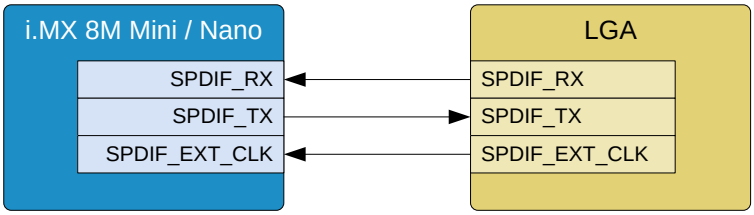

Figure 16: Block diagram SPDIF

The following table shows the signals used by the SPDIF interface.

Table 28: SPDIF signals

Signal	Direction	CPU ball	TQMa8MxML	Power group
SPDIF_EXT_CLK	I	AF8	D8	V_3V3
SPDIF_RX	I	AG9	F8	
SPDIF_TX	O	AF9	E9	

3.2.5.11 ECSPI

The SPI interfaces of the i.MX 8M Mini are full-duplex capable and support both master and slave modes.
As a primary function, the ECSPI1 and ECSPI2 interfaces each have a chip select on TQMa8MxML LGA pads.
ECSPI3 can be multiplexed to UART pads.
The voltage supply must be set to 1.8 V or 3.3 V via LGA pad V_ECSPI.

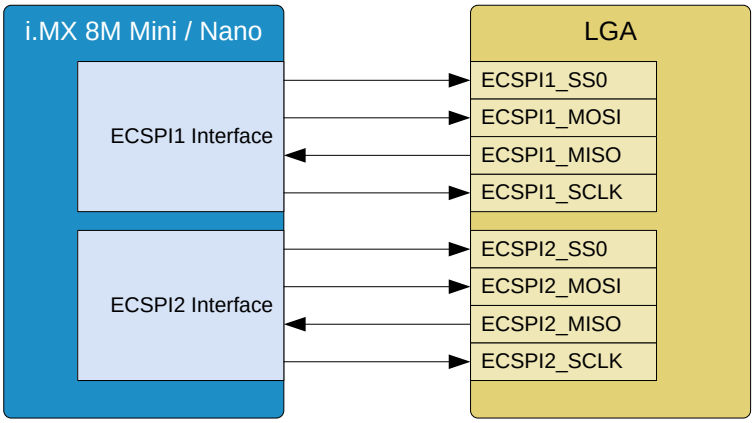

Figure 17: Block diagram ECSPI

The following table shows the signals used by the ECSPI interface.

Table 29: ECSPI signals

Signal	Direction	CPU ball	TQMa8MxML	Power group
ECSPI1_MISO	I	A7	A18	V_ECSPI
ECSPI1_MOSI	O	B7	B18	
ECSPI1_SCLK	O	D6	A17	
ECSPI1_SS0	O	B6	B16	
ECSPI2_MISO	I	A8	C19	
ECSPI2_MOSI	O	B8	D19	
ECSPI2_SCLK	O	E6	B19	
ECSPI2_SS0	O	A6	C17	

3.2.5.12 QSPI

(See chapter 3.2.2.3.)

3.2.5.13 UART

The i.MX 8M Mini provides four UART interfaces, which are all routed to TQMa8MxML LGA pads.
UART2 can be used to debug the A53 core, UART4 can be used to debug the M4 core.
The voltage supply must be set to 1.8 V or 3.3 V via LGA pad V_UART.

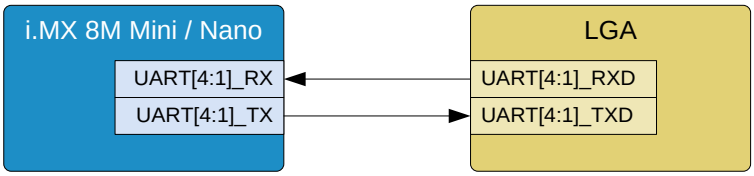

Figure 18: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces.

Table 30: UART signals

Signal	CPU ball	TQMa8MxML	Power group
UART1_RXD	E14	E16	V_UART
UART1_TXD	F13	D16	
UART2_RXD	F15	G16	
UART2_TXD	E15	F16	
UART3_RXD	E18	J16	
UART3_TXD	D18	H16	
UART4_RXD	F19	L16	
UART4_TXD	F18	K16	

3.2.5.14 USB

The i.MX 8M Mini provides two USB 2.0 controllers (including USB 2.0 OTG).
USB1 is configured as USB OTG by default. The OTG signals use GPIO1 pins as shown in the block diagram.
USB2 is configured in such a way that USB 2.0 is used without OTG functionality, although an OTG configuration is possible.
The LGA pads of the OTG signals are available as GPIO pins when not in use.
USB_ID pins may only be connected with 1.8 V! USB_VBUS pins on the other hand with up to 5 V.
The i.MX 8M Nano offers only one USB interface (USB1), which is implemented as USB-OTG on the TQMa8MxNL.
If the TQMa8MxNL is used, the LGA pads of the USB2 signals, except for the OTG pins, should be terminated with 10 kΩ.
When using USB-OTG, it is recommended to use the OTG_ID signal instead of the regular ID signal.
The regular ID signal is available as placement option.

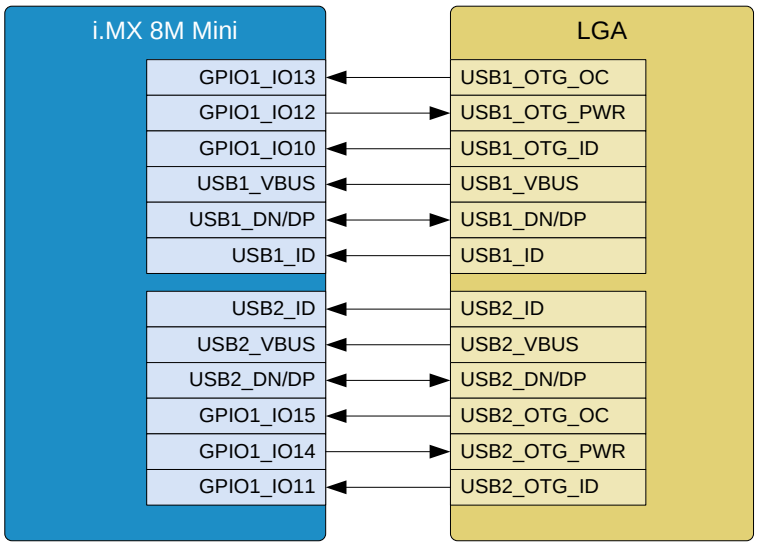

Figure 19: Block diagram USB interfaces

The following table shows the signals used by the USB_OTG interfaces:

Table 31: USB_OTG signals

Signal	Direction	CPU ball	TQMa8MxML	Power group
USB1_DN	I/O	A22	U19	V_3V3
USB1_DP		B22	V19	
USB1_VBUS	P	F22	P16	
USB1_ID	I	D22	N16	V_1V8_ANA
USB1_OTG_ID	I	AD10	J5	V_3V3
USB1_OTG_OC	I	AD9	H6	
USB1_OTG_PWR	O	AB10	H5	
USB2_DN	I/O	A23	V18	V_3V3
USB2_DP		B23	W18	
USB2_VBUS	P	F23	R17	
USB2_ID	I	D23	P17	V_1V8_ANA
USB2_OTG_ID	I	AC10	J6	V_3V3
USB2_OTG_OC	I	AB9	G6	
USB2_OTG_PWR	O	AC9	G5	

3.2.5.15 USDHC (SD card)

An SD card can be connected to the USDHC2 interface of the i.MX 8M Mini. All signals are routed from the i.MX 8M Mini to the TQMa8MxML LGA pads. The supply voltage V_3V3_SD provided at TQMa8MxML LGA pad F6 can be used to supply SD cards. V_3V3_SD can supply up to 400 mA.

The CPU internal pull resistors are used as pull-ups for the signal lines. External pull-up resistors are therefore not required.

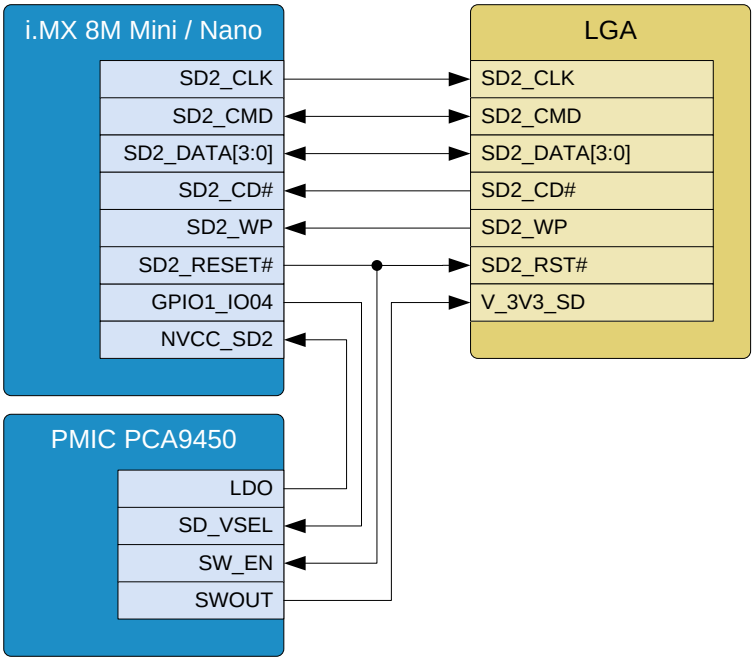

Figure 20: Block diagram SD card interface

Table 32: USDHC2 signals

Signal	Direction	CPU ball	TQMa8MxML	Power group
SD2_CD#	I	AA26	P5	V_SD2
SD2_CLK	O	W23	U5	
SD2_CMD	I/O	W24	T5	
SD2_DATA0	I/O	AB23	U3	
SD2_DATA1	I/O	AB24	T4	
SD2_DATA2	I/O	V24	R3	
SD2_DATA3	I/O	V23	R4	
SD2_RST#	O	AB26	T7	
SD2_WP	I	AA27	R6	
V_3V3_SD	O	–	F6	V_3V3_SD

The voltage level of the data signals between SD card and CPU is controlled by the signal SD2_VSELECT on the TQMa8MxML.

Table 33: SD2_VSELECT logic

SD2_VSELECT	SD card voltage
High	1.8 V
Low	3.3 V

3.2.5.16 External clock sources

The i.MX 8M Mini has the option to use two external oscillators as clock sources.
All four CPU balls provided for this purpose are connected to TQMa8MxML LGA pads.
The following table shows these clock signals.

Table 34: XTAL signals

Signal	CPU ball	TQMa8MxML	Power group
CLK1_IN	H27	W16	V_1V8
CLK1_OUT	H26	W17	
CLK2_IN	J27	W15	
CLK2_OUT	J26	V16	

3.2.6 Unspecific signals

The following table lists all signals that are not assigned to a specific group.

Table 35: Unspecific signals

Signal	Direction	CPU ball	TQMa8MxML	Power group
PMIC_WDOG#	O	AG13	K6	V_3V3
M4_NMI / M7_NMI [11]	I	AF12	K5	
ONOFF	I_{PU}	A25	G7	V_1V8_SNVS
TEST_MODE [12]	I	D26	E11	V_3V3

11: M4_NMI on the TQMa8MxML, M7_NMI on the TQMa8MxNL.
12: Signal is only available on the TQMa8MxML.

3.2.7 Reset

Reset inputs or outputs are available at the TQMa8MxML LGA pads.
The following block diagram shows the wiring of the reset signals.

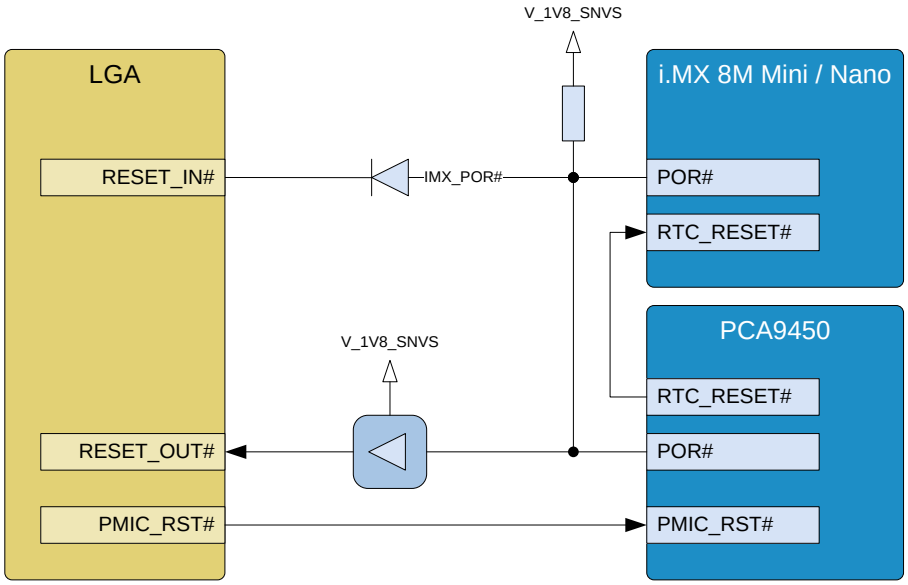

Figure 21: Block diagram Reset

The following table describes the reset signals available at the TQMa8MxML LGA pads:

Table 36: Reset signals

Signal	Direction	TQMa8MxML	Power group	Remark
RESET_IN#	I	E7	1.8 V	• Reset input of i.MX 8M Mini • Low-active signal • To deactivate: float or PU to 1.8 V
RESET_OUT#	O	F7	Defined externally	• Reset output of TQMa8MxML • Low-active signal • Activated by PMIC or RESET_IN# • Open Drain, requires PU to 3.3 V on carrier board
PMIC_RST#	I	E6	1.8 V	• Reset input of PMIC • Low-active signal • To deactivate: float

3.2.8 Differences between TQMa8MxML and TQMa8MxNL

The i.MX 8M Nano has some differences compared to the i.MX 8M Mini that must be taken into account when designing a carrier board.

3.2.8.1 CPU

- The i.MX 8M Nano has an integrated Cortex-M7, while the i.MX 8M Mini has a Cortex-M4.
- The i.MX 8M Nano does not have a VPU and therefore cannot support video processing.
  Due to the omission of the VPU, the TQMa8MxNL consumes less power than the TQMa8MxML.
- The "Non Maskable Interrupt" (NMI) can still be used on the TQMa8MxNL.
  The LGA pad "M4_NMI" is routed to the CPU ball [AF12] and is labelled "M7_NMI".

3.2.8.2 SDRAM

The i.MX 8M Nano only supports 16-bit wide SDRAM. Therefore, only 16-bit wide LPDDR4 RAM is populated.

3.2.8.3 Boot Mode

The Boot Mode of the i.MX 8M Nano is set using four Boot_Mode pins, while that of the i.MX 8M Mini is set using only two.
In addition to BOOT_MODE0 and BOOT_MODE1, JTAG_TRST# is used as BOOT_MODE2 and TEST_MODE as BOOT_MODE3 on the TQMa8MxNL.

3.2.8.4 SAI

The i.MX 8M Nano lacks the SAI1 interface. Some of these pins are used on the i.MX 8M Mini to set the boot source. Accordingly, the i.MX 8M Nano does not offer as many audio processing options, since SAI1 is the widest audio interface with 8 bits at the same time. On the other hand, the i.MX 8M Nano also has a second 1-bit wide audio interface, SAI7, which can be multiplexed if required.

3.2.8.5 PCIe

Compared to the i.MX 8M Mini, the i.MX 8M Nano does not have PCIe functionality. However, the corresponding pads are present on the TQMa8MxNL. It is recommended to terminate them with 10 kΩ to Ground.

3.2.8.6 USB

The i.MX 8M Nano provides only one USB 2.0 interface, which is also OTG-capable. However, the corresponding pads are present on the TQMa8MxNL. It is recommended to terminate the corresponding module pads (USB2_xx) with 10 kΩ to Ground.

3.2.9 Power

3.2.9.1 Power supply

The TQMa8MxML requires a supply voltage of 5 V ±5 %.
The following block diagram shows the TQMa8MxML power supply.

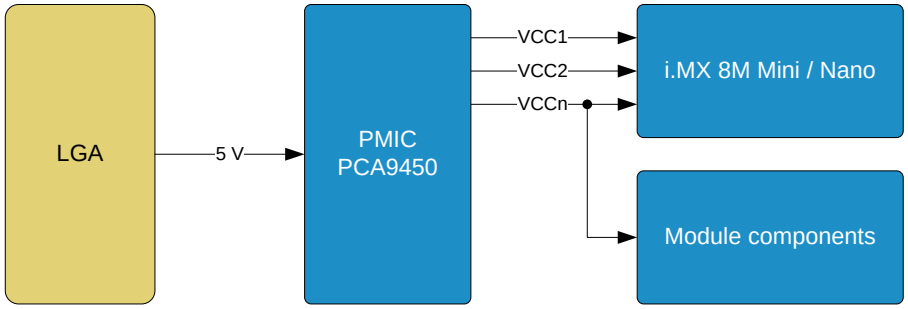

Figure 22: Block diagram TQMa8MxML power supply

The characteristics and functions of the single pins and signals are to be taken from the PMIC Data Sheet (7), and the i.MX 8M Mini Reference Manual (2).

3.2.9.2 Power consumption

The given power consumption has to be seen as an approximate value.
The power consumption strongly depends on the application, the mode of operation and the operating system.
For more information on power consumption and savings options, see NXP Application Note AN12410 (10) and AN12269 .

The following table shows the TQMa8MxML and TQMa8MxNL current and power consumptions at 5 V (±5 %) supply voltage:

Table 37: TQMa8MxML power consumption

Mode of operation	TQMa8MxML	TQMa8MxNL
U-Boot idle (prompt)	227 mA / 1,135 mW	163.3 mA / 816.5 mW
Linux idle (prompt)	159 mA / 795 mW	113.9 mA / 569,5 mW
Linux 100 % CPU load (stress test)	379 mA / 1,895 mW	301.9 mA / 1,509.5 mW
Off-Mode (PMIC_RST# = Low)	28.5 mA / 142.5 mW	9.7 mA / 48.5 mW
Current consumption theoretical worst case (design base for module supply)	3.25 A / 16.25 W	

3.2.9.3 Voltage monitoring

The TQMa8MxML features a supervisor which monitors the input voltage (V_{IN}).

If the input voltage drops below 4.38 V, a Reset is triggered and the TQMa8MxML is held in reset until the input voltage is in the permitted range again.

Attention: Destruction or malfunction, supply voltage exceedance	
	The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa8MxML.

3.2.9.4 Other supply voltages

USBx_VBUS:

The voltage inputs USB1_VBUS and USB2_VBUS are used to detect the USB-VBUS voltage and are usually connected to the VBUS voltage switched by USB[2:1]_PWR. Protective circuitry on the TQMa8MxML allows up to 5 V to be applied to these LGA pads.
It is recommended to provide one 220 nF capacitor (10 V) each between USBx_VBUS and Ground on the carrier board.

V_LICELL:

A coin cell can be connected to the TQMa8MxML LGA pad D15 (V_LICELL) to supply the optional discrete RTC.

See chapter 3.2.4.2 for information on the LICELL or RTC options.

Note: RTC power supply	
	If the supply voltage fails, the CPU-internal RTC is reset. In this case the system time can be maintained if the discrete RTC is supplied by a coin cell.

3.2.9.5 Supply outputs

The TQMa8MxML provides three voltages that can be used on the carrier board.

Table 38: Voltages provided by TQMa8MxML

Voltage	TQMa8MxML	Usage	Max. load
V_1V8	N1	General usage on carrier board	500 mA
V_3V3	P1	General usage on carrier board	500 mA
V_3V3_SD	F6	SD card supply	400 mA

The voltage V_3V3 can be used as Power-Good signal for the supply of circuitry on the carrier board.

Attention: Destruction or malfunction, current exceedance	
	A load of up to 500 mA at V_1V8 or V_3V3, as well as up to 400 mA at V_3V3_SD causes an increased power consumption of the TQMa8MxML and thus a higher self-heating. These three voltages are outputs and must never be supplied from external sources! Furthermore the outputs are not short-circuit proof. Overloading the voltage outputs can damage the TQMa8MxML.

3.2.9.6 I/O voltages

The TQMa8MxML provides three LGA pads that define the I/O voltages for specific rails of the CPU. They are listed in the following table and must be set on the carrier board. If not set, the corresponding TQMa8MxML I/O signals are not supplied with voltage. The TQMa8MxML supply outputs V_1V8 or V_3V3 can be used for this purpose. If 2.5 V is to be used, this voltage must be provided by the carrier board, since it cannot be provided by the TQMa8MxML.

Table 39: Configurable voltages

TQMa8MxML	Permitted voltages	Max. load	Remark
V_ECSPI	1.8 / 3.3 V	15 mA at 1.8 V; 27 mA at 3.3 V	–
V_ENET	1.8 / 2.5 / 3.3 V	32 mA at 1.8 V; 58 mA at 3.3 V	RGMII: 1.8 V or 2.5 V RMII: 1.8 V or 3.3 V
V_UART	1.8 / 3.3 V	15 mA at 1.8 V; 27 mA at 3.3 V	–

3.2.9.7 Power-Up sequence TQMa8MxML / carrier board

Since the TQMa8MxML operates with 5 V and the I/O voltages of the CPU signals are generated on the TQMa8MxML, there are timing requirements for the carrier board design with respect to the voltages generated on the carrier board:

After power up of the 5V supply for the TQMa8MxML, the PMIC power-up sequence starts. External TQMa8MxML inputs driven by the carrier board may only be switched on after the power-up of V_3V3. LGA pad P1 (V_3V3) can be used as feedback.

The following figure illustrates the recommended control of the voltage regulators on a carrier board.

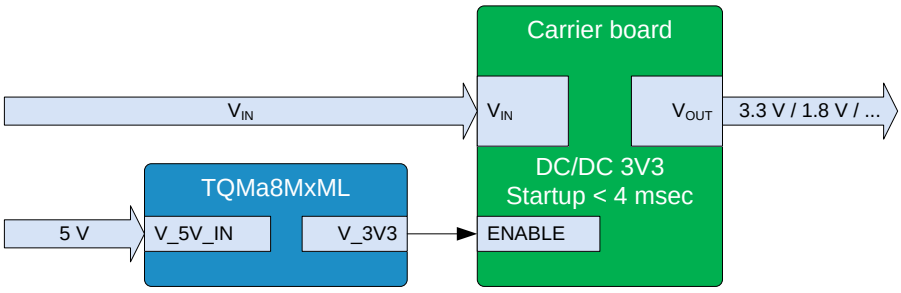

Figure 23: Block diagram power supply carrier board

Attention: Destruction or malfunction, Power-Up sequence	
⚠	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the power-up sequence is indicated by a high level of signal V_3V3, TQMa8MxML pad P1.

3.2.9.8 Standby and SNVS

In Standby Mode, several voltage controllers on the TQMa8MxML are switched off.

The rails V_1V8_SNVS and V_0V8_SNVS remain active, which ensures the correct function of the RTC.

3.2.9.9 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX 8M Mini Reference Manual (2) and the PMIC Data Sheet (7). The PMIC is connected to the I2C1 bus.
The following block diagram shows the connection between PMIC and i.MX 8M Mini:

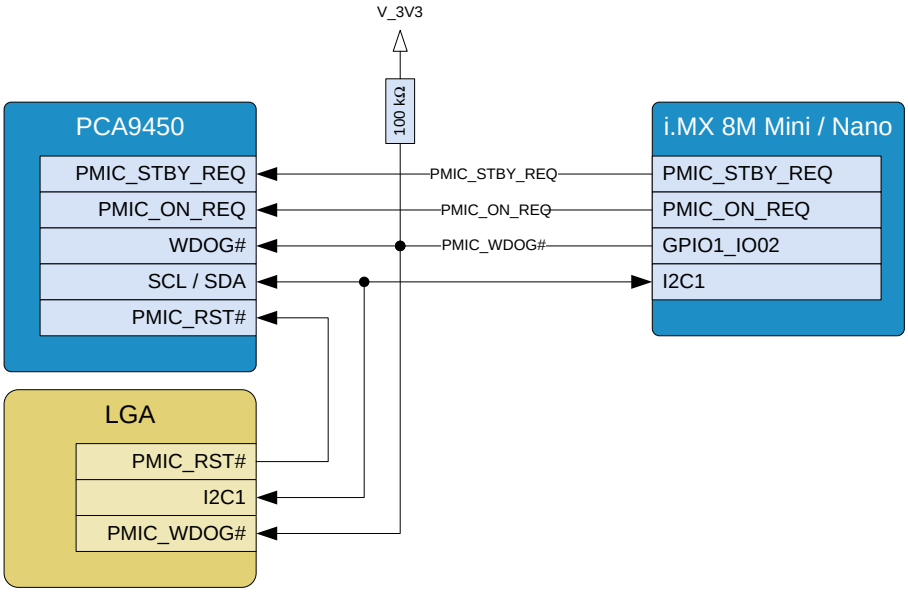

Figure 24: Block diagram PMIC interface

➢ The PMIC has I²C address `0x25 / 010 0101b`

The following PMIC and power management signals are available on the TQMa8MxML LGA pads

Table 40: PMIC signals

Signal	Direction	TQMa8MxML	Power group	Remark
PMIC_WDOG#	I_{PU}	AG13	V_3V3	• Watchdog Reset input of i.MX 8M Mini • Deactivated by default on the part of the PMIC, can therefore be used as GPIO1_IO02
PMIC_RST#	I_{PU}	E6	V_1V8_SNVS	• Low-active with internal PU • See PMIC Data Sheet (7)
I2C1_SCL	I/O	C10	V_3V3	• Can be used on carrier board, see chapter 3.2.5.4
I2C1_SDA	O	C9		

Attention: Destruction or malfunction, PMIC programming	
⚠	Improper programming of the PMIC may result in the i.MX 8M Mini or periphery being operated outside its specification. This may lead to malfunctions, accelerated aging or destruction of the TQMa8MxML.

3.2.10 Impedances

By default, all single-ended signals have a nominal impedance of 50 Ω ±10 %.
However, some interfaces on the TQMa8MxML are routed with different impedances, depending on the signal requirements.

The following table is taken from the Hardware Developer's Guide (6) and shows the respective interfaces:

Table 41: Impedances

Signal / Interface	Impedance on TQMa8MxML	Recommendation for carrier board
DDR DQS/CLK; PCIe TX/RX data pairs	85 Ω, differential	85 Ω ±10 %, differential
Differential USB signals	90 Ω, differential	90 Ω ±10 %, differential
Differential MIPI signals (CSI and DSI)	100 Ω, differential	100 Ω ±10 %, differential
Differential RGMII signals	100 Ω, differential	100 Ω ±10 %, differential

4. SOFTWARE

The TQMa8MxML is delivered with a preinstalled boot loader U-Boot.
The BSP provided by TQ-Systems GmbH is configured for the combination of TQMa8MxML and MBa8Mx.
The boot loader U-Boot provides TQMa8MxML-specific as well as board-specific settings, e.g.:

- i.MX 8M Mini configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

Further information can be found in the https://support.tq-group.com/TQMa8MxML.

If another bootloader is used, this data must be adapted. Contact TQ-Support for detailed information.

5. MECHANICS

5.1 Dimensions

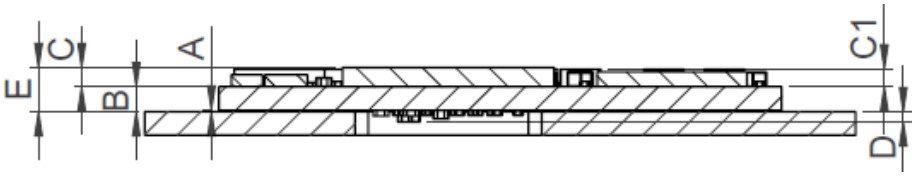

Figure 25: TQMa8MxML dimensions, side view

Table 42: TQMa8MxML heights

Dim.	Value	Tolerance	Remark
A	0.125 mm	+0.075 mm –0.025 mm	TQMa8MxML LGA pads height
B	1.6 mm	±0.16 mm	PCB without solder resist
C	1.25 mm	±0.11 mm	Height CPU soldered
C1	1.22 mm	±0.05 mm	Highest component, top side
D	0.57 mm	±0.2 mm	Highest component, bottom side
E	3 mm	±0.2 mm	Top edge CPU with soldered TQMa8MxML. Referenced to top edge of carrier board.

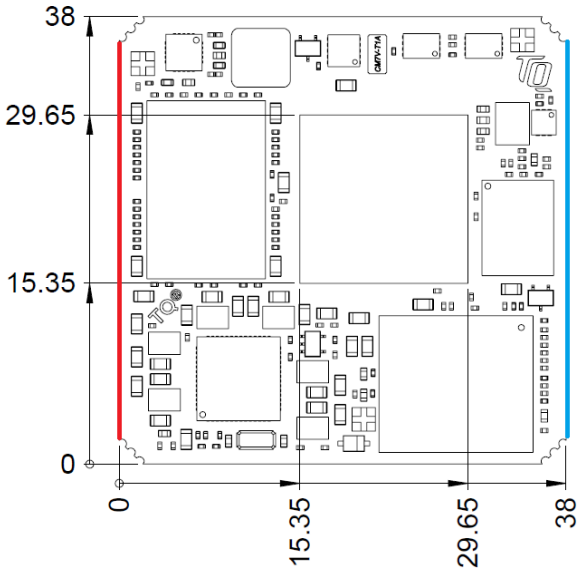

Figure 26: TQMa8MxML dimensions, top view

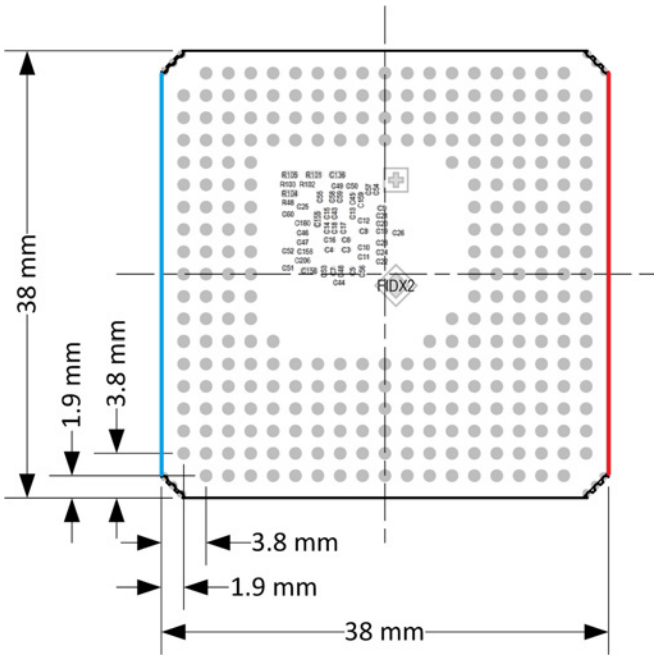

Figure 27: TQMa8MxML dimensions, bottom view

5.2 Component placement

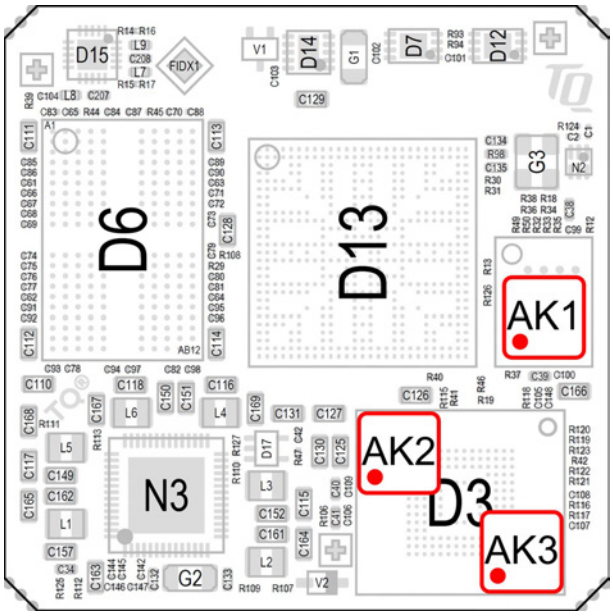

Figure 28: TQMa8MxML, component placement top

The labels on the TQMa8MxML show the following information:

Table 43: Labels on TQMa8MxML

Label	Content
AK1	TQMa8MxML version and revision
AK2	Serial number
AK3	MAC address

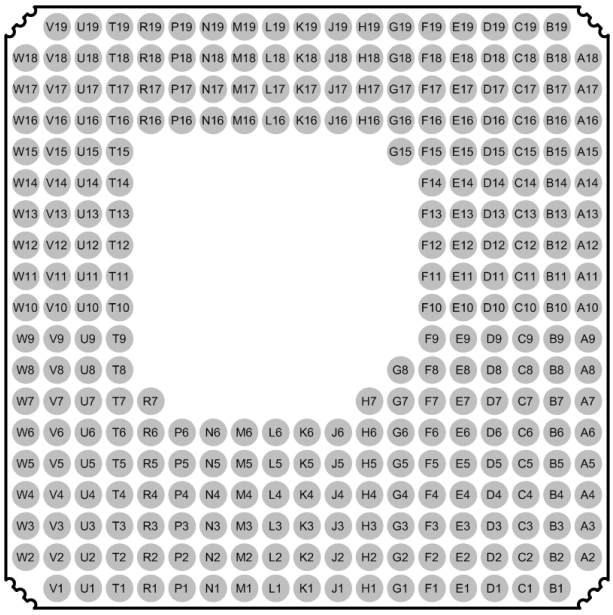

Figure 29: TQMa8MxML, LGA pad numbering scheme, **bottom** view

5.3 Adaptation to the environment

The TQMa8MxML has overall dimensions (length × width) of 38 × 38 mm^2.
The TQMa8MxML has a maximum height above the carrier board of approximately 3.0 mm.
The TQMa8MxML has 281 LGA pads with a diameter of 1.0 mm and a grid of 1.9 mm.
The TQMa8MxML weighs approximately 10 grams.

5.4 Protection against external effects

As an embedded module, the TQMa8MxML is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

To cool the TQMa8MxML, approximately 4 watts (TQMa8MxML) or 3 watts (TQMa8MxNL) have to be dissipated, see Table 37.
The power dissipation originates primarily in the i.MX 8M Mini/Nano, the LPDDR4 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (6) and (10) for further information.

Attention: Destruction or malfunction, TQMa8MxML cooling	
	The i.MX 8M Mini belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA pads, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M Mini must be taken into consideration when connecting the heat sink, see (10). The i.MX 8M Mini is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MxML and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMa8MxML has to be soldered on the carrier board. To ensure a high-quality connection of the LGA pads during reflow soldering of the TQMa8MxML, the LGA pads must be free of grease and dirt.
Please contact TQ-Support for soldering instructions (14).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa8MxML was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa8MxML.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.4 Climate and operational conditions

The operating temperature range for the TQMa8MxML strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa8MxML.

In general, a reliable operation is given when following conditions are met:

Table 44: Climate and operational conditions

Variant	Ambient temperature		Relative humidity not condensing (operational / storage)	Remark
	Operational	Storage		
C	0 °C to +85 °C	–40 °C to +85 °C	10 % to 90 %	Consumer
E	–25 °C to +85 °C			Extended (default)
I	–40 °C to +85 °C			Industrial

Table 45: Maximum operating temperatures

Parameter	Temp. range
T_J i.MX 8M Mini, i.MX 8M Nano	–40 °C to +105 °C
T_J PMIC	–40 °C to +105 °C
Case temperature SDRAM	–40 °C to +85 °C
Case temperature other ICs	Ambient temperature see Table 44

Detailed information concerning the i.MX 8M Mini thermal characteristics is to be taken from NXP documents (6).

Attention: Destruction or malfunction, TQMa8MxML cooling	
	The i.MX 8M Mini belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA pads, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M Mini must be taken into consideration when connecting the heat sink, see (10). The i.MX 8M Mini is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MxML and thus malfunction, deterioration or destruction.

6.5 Reliability and service life

The MTBF calculated for the TQMa8MxML is 1,270,405 hours with a constant error rate @ +40 °C, Ground Benign.

The TQMa8MxML is designed to be insensitive to shock and vibration.

The TQMa8MxML must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.

Detailed information concerning the i.MX 8M Mini service life under different operational conditions is to be taken from the NXP Application Note (11).

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa8MxML is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa8MxML was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa8MxML always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa8MxML on account of available Standby or Sleep-Modes of the components on the TQMa8MxML.

7.5 Battery

No batteries are assembled on the TQMa8MxML.

7.6 Packaging

The TQMa8MxML is delivered in reusable packaging.

7.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa8MxML, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures.

Since there is currently no technically equivalent alternative for PCBs with bromine-containing flame retardants (FR-4 material), such PCBs continue to be used. Components containing polychlorinated biphenyls are not used.

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 46: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DDR	Double Data Rate
DIN	Deutsche Industrie Norm (German industry standard)
DNC	Do Not Connect
DSI	Display Serial Interface
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
Gbps	Gigabit per second
GPIO	General Purpose Input/Output
HS	High-Speed
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Integrated Interchip Sound
IP00	Ingress Protection 00
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LGA	Land Grid Array
LPDDR4	Low Power DDR4
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
MTBF	Mean operating Time Between Failures
NAND	Not-And
NC	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go

8.1 Acronyms and definitions (continued)

Table 46: Acronyms (continued)

Acronym	Meaning
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protection
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
USDHC	Ultra-Secured Digital Host Controller
WDOG	Watchdog
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 47: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8M Mini Applications Processor Reference Manual	Rev. 3, 15 Jan 2021	NXP
(2)	i.MX 8M Nano Applications Processor Reference Manual	Rev. 1, 15 Jan 2021	NXP
(3)	i.MX 8M Mini Applications Processors Data Sheet for Industrial Products	Rev 1, 04 Aug 2020	NXP
(4)	i.MX 8M Nano Applications Processors Data Sheet for Industrial Products	Rev 3, Apr 2022	NXP
(5)	i.MX 8M Mini Hardware Developer's Guide	Rev 3.0, Dec 2021	NXP
(6)	i.MX 8M Nano Hardware Developer's Guide	Rev 2, Nov 2021	NXP
(7)	PMIC PCA9450 Data Sheet	Rev 2.2, 15 Sep 2021	NXP
(8)	i.MX 8M Mini Mask Set Errata for Mask 0N87W	Rev. 1, Oct 2021	NXP
(9)	i.MX 8M Nano Mask Set Errata for Mask 0N14Y	Rev.1, Apr 2021	NXP
(10)	i.MX 8M Mini Power Consumption Measurement, AN12269	Rev. 0, Oct 2018	NXP
(11)	i.MX 8M Mini Product Lifetime Usage, AN12468	Rev.0, 23 Jun 2019	NXP
(12)	MBa8Mx User's Manual	– current –	TQ-Systems
(13)	TQMa8MxML Support-Wiki	– current –	TQ-Systems
(14)	TQMa8MxML Processing instructions	– current –	TQ-Systems

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