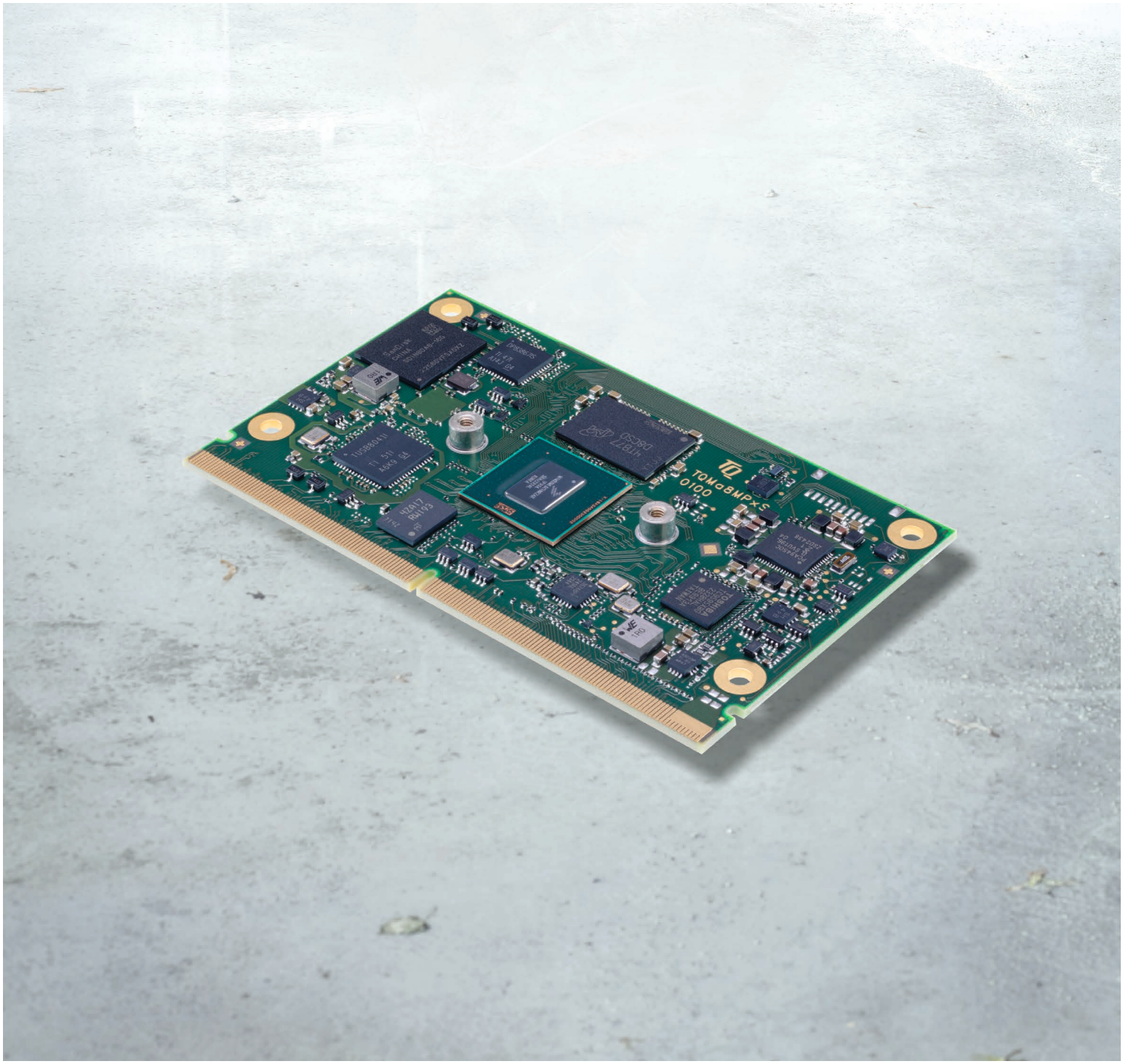
TQMa8MPxS
Preliminary User's Manual

TQMa8MPxS UM 0001
08.07.2025



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	08.07.2025	Kreuzer		First issue

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TQ-Systems GmbH
Gut Delling, Mühlstraße 2
D-82229 Seefeld

Tel: +49 8153 9308–0
Fax: +49 8153 9308–4223
E-Mail: Info@TQ-Group
Web: TQ-Group

1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa8MPxS and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MB-SMARC-2 circuit diagram
- MB-SMARC-2 User's Manual
- i.MX 8M Plus Data Sheet
- i.MX 8M Plus Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8MPxS

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of the TQMa8MPxS as of revision 0100, in combination with the MB-SMARC-2 as of revision 0100 and refers to some software settings. A certain TQMa8MPxS derivative does not necessarily provide all features described in this Preliminary User's Manual. This Preliminary User's Manual does neither replace the i.MX 8M Plus Reference Manual (1), nor the i.MX 8M Plus Data Sheet (2), nor any other documents from NXP.

The TQMa8MPxS is a universal Minimodule based on the NXP ARM® Cortex®-A53 based i.MX 8M CPU family.

2.1 Key functions and characteristics

The TQMa8MPxS extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

All essential i.MX 8M Plus signals are routed to the TQMa8MPxS SMARC pin strip. There are therefore no restrictions for customers using the TQMa8MPxS with respect to an integrated customised design. All essential components like CPU, LPDDR4, eMMC and PMIC are already integrated on the TQMa8MPxS.

The main features of the TQMa8MPxS are:

- 64 bit NXP i.MX 8M Plus CPU, up to 4 × ARM Cortex®-A53 and 1 × Cortex®-M7
- i.MX 8M Plus Dual, Plus Quad 4 Lite, Plus Quad 6 Video, Plus Quad 8 ML/AI
- Up to 8Gbyte 32-bit LPDDR4-4000
- Up to 256 Gbyte eMMC NAND Flash, eMMC standard 5.1
- Up to 256 Mbyte QSPI NOR Flash (optional)
- SMARC specific EEPROM
- Customer specific EEPROM (optional)
- Temperature sensor
- RTC (optinal)
- Trust Secure Element (optional)
- Gyroscope (optional)
- second Ethernet-PHY (optional)
- DisplayPort bridge (optional)
- NXP Power Management Integrated Circuit PCA9450
- Single supply voltage 5 V or wide range input 3.0 V to 5.25 V

2.2 CPU block diagram

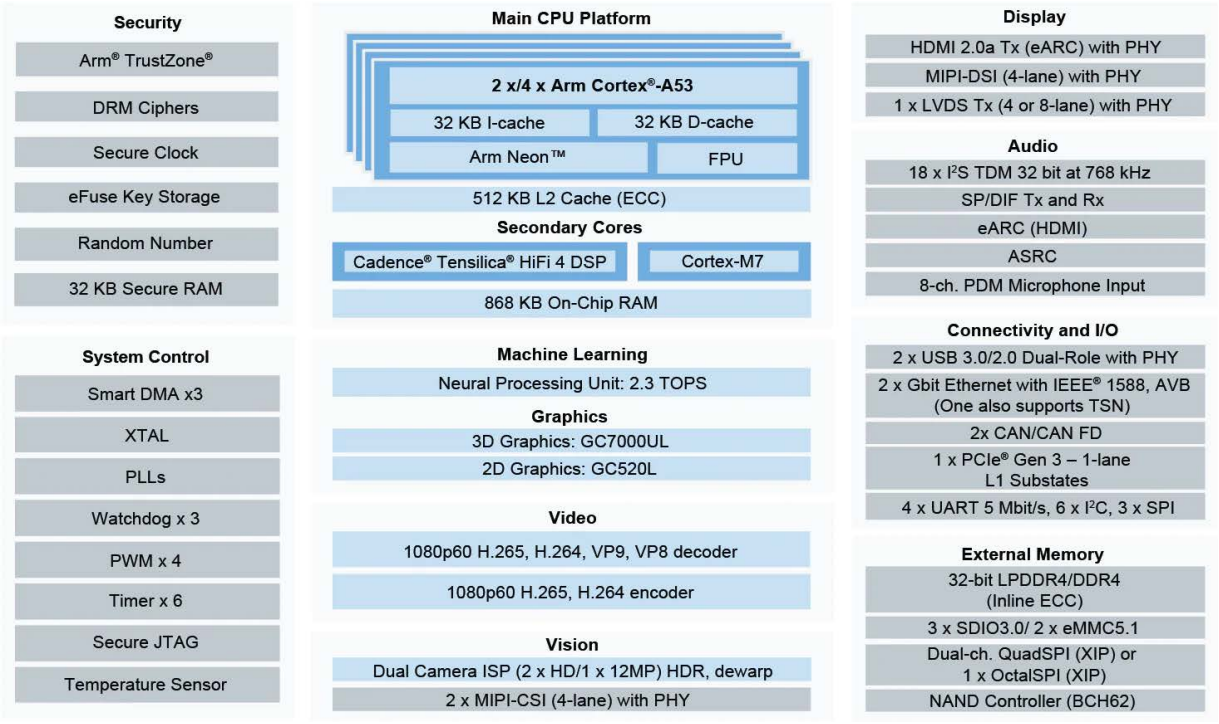

Figure 1: Block diagram i.MX 8M Plus
(Source: NXP)

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa8MPxS, and the BSP provided by TQ-Systems GmbH, see also chapter 4.

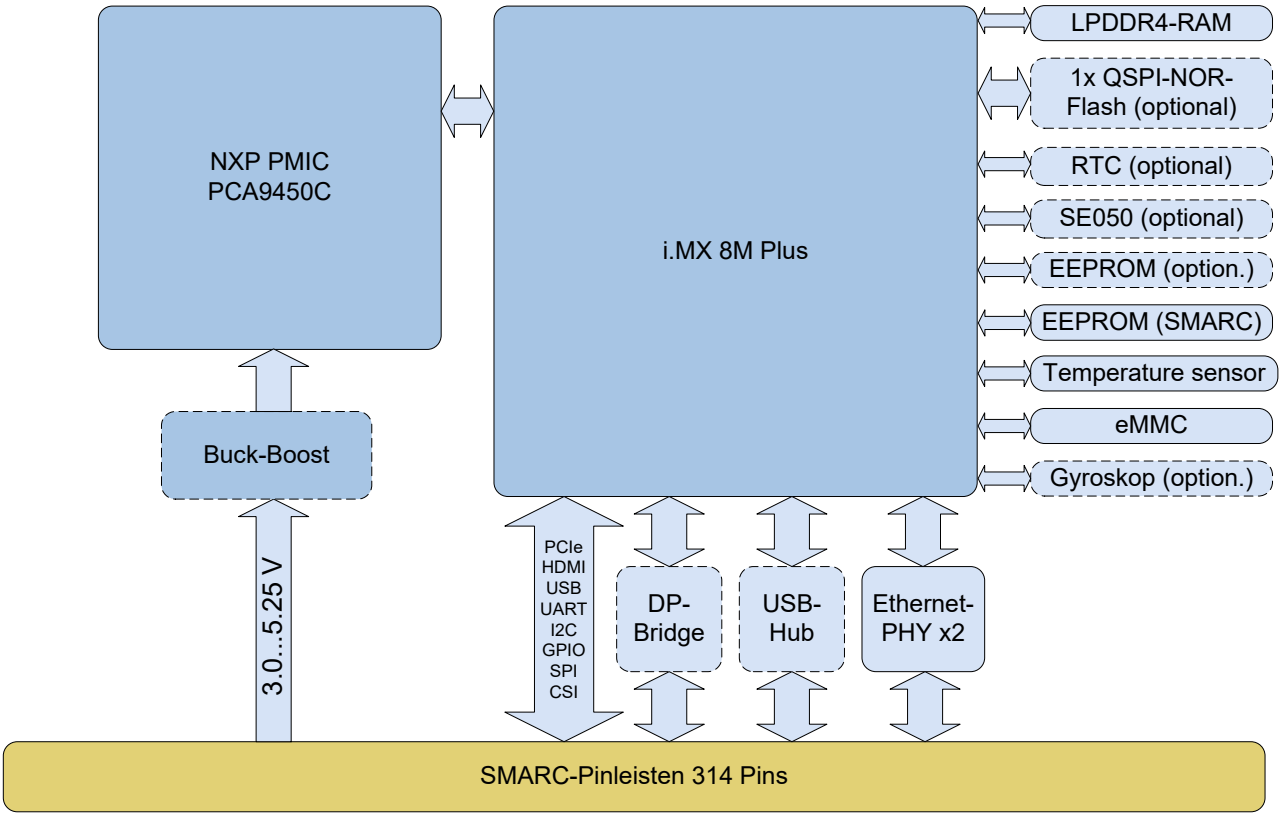

Figure 2: Block diagram TQMa8MPxS (simplified)

3.1 Interfaces to other systems and devices

The TQMa8MPxS has a SMARC pin strip with a total of 314 pins, divided between the top and bottom side of the board, via which it is connected to the baseboard. Furthermore, the module has four holes with which it can be fixed to the carrier board by means of screws.

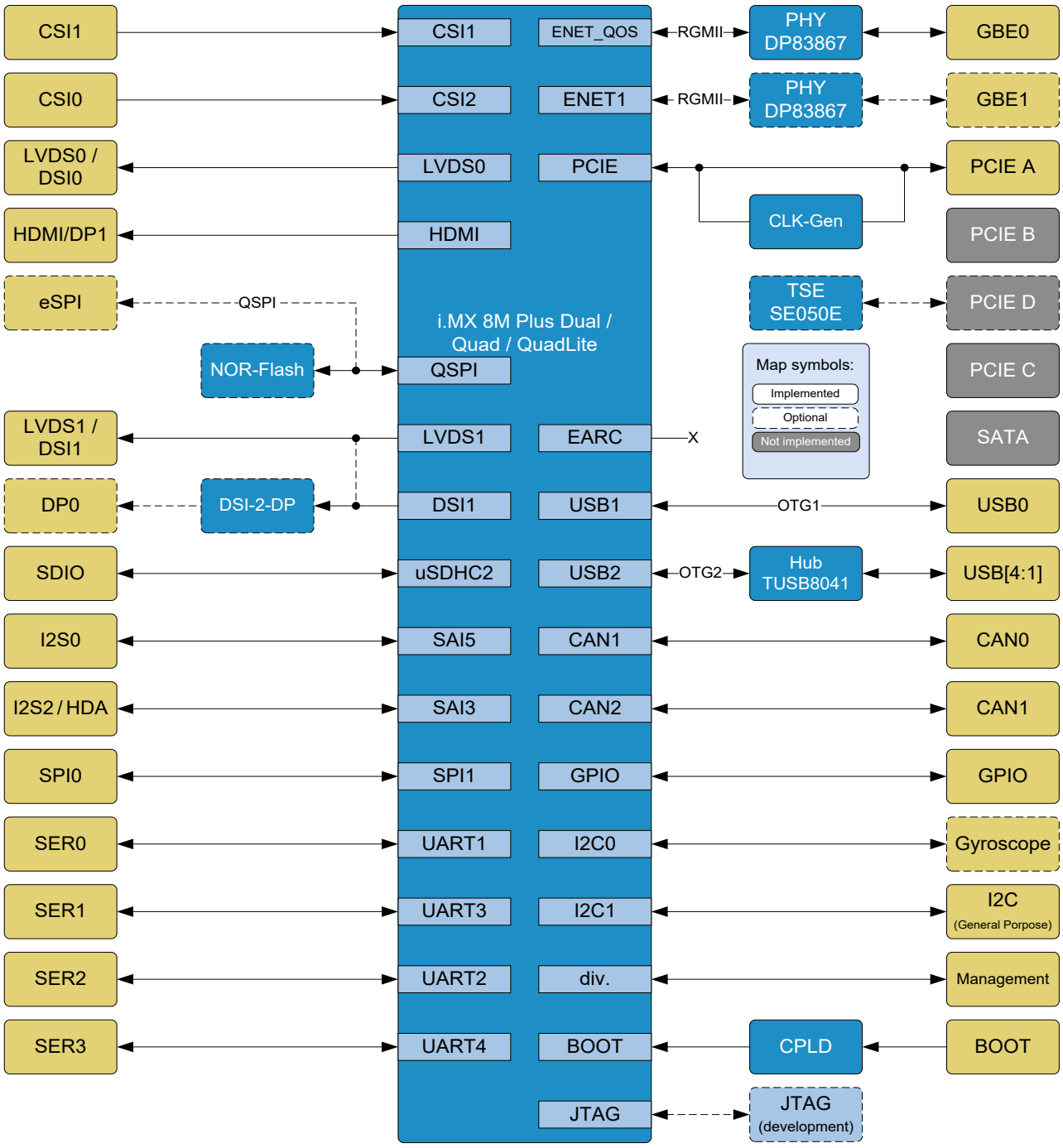

Figure 3: SMARC interface with i.MX 8M Plus

3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX 8M Plus-internal function units must be taken note of.

The pin assignment in Table 2 refers to a TQMa8MPxS with i.MX 8M Plus Quad 8 ML/AI CPU in combination with the carrier board MB-SMARC-2.

NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).

The electrical and pin characteristics are to be taken from the i.MX 8M Plus and PMIC documentation, see Table 31.

Attention: Destruction or malfunction, pin multiplexing	
	Depending on the configuration, many i.MX 8M Plus pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX 8M Plus Reference Manual (1), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa8MPxS. Please contact TQ-Support for details.

3.1.1.1 Pinout TQMa8MPxS

The TQMa8MPxS has a total of 314 SMARC pins. The following table shows the TQMa8MPxS pinout:

Table 2: Pinout TQMa8MPxS

i.MX 8M Plus pin name	I/O	Level	Group	SMARC signal	Pin		SMARC signal	Group	Level	I/O	i.MX 8M Plus pin name
-	-	-	-	-	-	S1	CSI1_TX+ / I2C_CAM1_CK	CSI1	1.8 V	O	SD1_DATA2
GPIO1_IO03	I	1.8 V	CONFIG	SMB_ALERT_1V8#	P1	S2	CSI1_TX- / I2C_CAM1_DAT	CSI1	1.8 V	I/O	SD1_DATA3
-	P	-	Power	GND	P2	S3	GND	Power	-	P	-
MIPI_CSI1_CLK_P	O	1.8 V	CSI1	CSI1_CK+	P3	S4	RSVD	-	-	-	-
MIPI_CSI1_CLK_N	O	1.8 V	CSI1	CSI1_CK-	P4	S5	CSI0_TX+ / I2C_CAM0_CK	CSI0	1.8 V	O	SD1_DATA0
SAI1_RXD0 / SAI1_RXD1	I/O	3.3 V	GBE1	GBE1_SDP	P5	S6	CAM_MCK	CSI1	1.8 V	O	CLKOUT1
SAI2_MCLK / SAI2_TXFS	I/O	3.3 V	GBE0	GBE0_SDP	P6	S7	CSI0_TX- / I2C_CAM0_DAT	CSI0	1.8 V	I/O	SD1_DATA1
MIPI_CSI1_D0_P	I	1.8 V	CSI1	CSI1_RX0+	P7	S8	CSI0_CK+	CSI0	1.8 V	O	MIPI_CSI2_CLK_P
MIPI_CSI1_D0_N	I	1.8 V	CSI1	CSI1_RX0-	P8	S9	CSI0_CK-	CSI0	1.8 V	O	MIPI_CSI2_CLK_N
-	P	-	Power	GND	P9	S10	GND	Power	-	P	-
MIPI_CSI1_D1_P	I	1.8 V	CSI1	CSI1_RX1+	P10	S11	CSI0_RX0+	CSI0	1.8 V	I	MIPI_CSI2_D0_P
MIPI_CSI1_D1_N	I	1.8 V	CSI1	CSI1_RX1-	P11	S12	CSI0_RX0-	CSI0	1.8 V	I	MIPI_CSI2_D0_N
-	P	-	Power	GND	P12	S13	GND	Power	-	P	-
MIPI_CSI1_D2_P	I	1.8 V	CSI1	CSI1_RX2+	P13	S14	CSI0_RX1+	CSI0	1.8 V	I	MIPI_CSI2_D1_P
MIPI_CSI1_D2_N	I	1.8 V	CSI1	CSI1_RX2-	P14	S15	CSI0_RX1-	CSI0	1.8 V	I	MIPI_CSI2_D1_N
-	P		Power	GND	P15	S16	GND	Power		P	-
MIPI_CSI1_D3_P	I	1.8 V	CSI1	CSI1_RX3+	P16	S17	GBE1_MDI0+	GBE1	-	A	-
MIPI_CSI1_D3_N	I	1.8 V	CSI1	CSI1_RX3-	P17	S18	GBE1_MDI0-	GBE1	-	A	-
-	P	-	Power	GND	P18	S19	GBE1_LINK100#	-	-	-	-
-	A	-	GBE0	GBE0_MDI3-	P19	S20	GBE1_MDI1+	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI3+	P20	S21	GBE1_MDI1-	GBE1	-	A	-
-	-	-	-	GBE0_LINK100#	P21	S22	GBE1_LINK1000#	GBE1	3.3 V	O	-
-	O	3.3 V	GBE0	GBE0_LINK1000#	P22	S23	GBE1_MDI2+	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI2-	P23	S24	GBE1_MDI2-	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI2+	P24	S25	GND	Power	-	P	-
-	O	3.3 V	GBE0	GBE0_LINK_ACT#	P25	S26	GBE1_MDI3+	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI1-	P26	S27	GBE1_MDI3-	GBE1	-	A	-
-	A	-	GBE0	GBE0_MDI1+	P27	S28	GBE1_CTREF	-	-	-	-
-	-	-	-	GBE0_CTREF	P28	S29	PCIE_D_TX+/SERDES_0_TX+	-	-	-	-
-	A	-	GBE0	GBE0_MDI0-	P29	S30	PCIE_D_TX-/SERDES_0_TX-	-	-	-	-
-	A	-	GBE0	GBE0_MDI0+	P30	S31	GBE1_LINK_ACT#	GBE1	3.3 V	O	-
ECSPI2_MISO	O	1.8 V	SPI0	SPI0_CS1#	P31	S32	PCIE_D_RX+/SERDES_0_RX+	-	-	-	-
-	P	-	Power	GND	P32	S33	PCIE_D_RX-/SERDES_0_RX-	-	-	-	-
SD2_WP	I	1.8 / 3.3 V	SDIO	SDIO_WP	P33	S34	GND	Power	-	P	-
SD2_CMD	I/O	1.8 / 3.3 V	SDIO	SDIO_CMD	P34	S35	USB4+	USB4	-	I/O	-
SD2_CD_B	I	1.8 / 3.3 V	SDIO	SDIO_CD#	P35	S36	USB4-	USB4	-	I/O	-
SD2_CLK	O	1.8 / 3.3 V	SDIO	SDIO_CK	P36	S37	USB3_VBUS_DET	USB3	5 V	I	USB2_VBUS
SD2_RESET_B	O	3.3 V	SDIO	SDIO_PWR_EN	P37	S38	AUDIO_MCK	I2S0	1.8 V	O	SAI3_MCLK
-	P	-	Power	GND	P38	S39	I2S0_LRCK	I2S0	1.8 V	O	SAI2_RXFS
SD2_DATA0	I/O	1.8 / 3.3 V	SDIO	SDIO_D0	P39	S40	I2S0_SDOUT	I2S0	1.8 V	O	SAI2_RXD0
SD2_DATA1	I/O	1.8 / 3.3 V	SDIO	SDIO_D1	P40	S41	I2S0_SDIN	I2S0	1.8 V	I	SAI5_RXD0
SD2_DATA2	I/O	1.8 / 3.3 V	SDIO	SDIO_D2	P41	S42	I2S0_CK	I2S0	1.8 V	O	SAI2_RXC

SD2_DATA3	I/O	1.8 / 3.3 V	SDIO	SDIO_D3	P42	S43	ESPI_ALERT0#	eSPI	1.8 V	I	GPIO1_IO09
ECSPI1_SS0	O	1.8 V	SPI0	SPI0_CS0#	P43	S44	ESPI_ALERT1#	eSPI	1.8 V	-	-
ECSPI1_SCLK	O	1.8 V	SPI0	SPI0_CK	P44	S45	MDIO_CLK	-	-	-	-
ECSPI1_MISO	I	1.8 V	SPI0	SPI0_DIN	P45	S46	MDIO_DAT	-	-	-	-
ECSPI1_MOSI	O	1.8 V	SPI0	SPI0_DO	P46	S47	GND	Power	-	P	-
-	P	-	Power	GND	P47	S48	I2C_GP_CK	I2C	1.8 V	O	I2C1_SCL
-	-	-	-	SATA_TX+	P48	S49	I2C_GP_DAT	I2C	1.8 V	I/O	I2C1_SDA
-	-	-	-	SATA_TX-	P49	S50	HDA_SYNC / I2S2_LRCK	I2S2	1.8 V	O	SAI3_TXFS
-	P	-	Power	GND	P50	S51	HDA_SDO / I2S2_SDOUT	I2S2	1.8 V	O	SAI3_TXD
-	-	-	-	SATA_RX+	P51	S52	HDA_SDI / I2S2_SDIN	I2S2	1.8 V	I	SAI3_RXD
-	-	-	-	SATA_RX-	P52	S53	HDA_CK / I2S2_CK	I2S2	1.8 V	O	SAI3_TXC
-	P	-	Power	GND	P53	S54	SATA_ACT#	-	-	-	-
NAND_CE0_B	O	1.8 V	eSPI	ESPI_CS0#	P54	S55	USB5_EN_OC#	-	-	-	-
GPIO1_IO09	O	1.8 V	eSPI	ESPI_CS1#	P55	S56	ESPI_IO_2	eSPI	1.8 V	I/O	NAND_DATA02
NAND_ALE	O	1.8 V	eSPI	ESPI_CK	P56	S57	ESPI_IO_3	eSPI	1.8 V	I/O	NAND_DATA03
NAND_DATA01	I/O	1.8 V	eSPI	ESPI_IO_1	P57	S58	ESPI_RESET#	eSPI	1.8 V	O	SAI1_RXD3
NAND_DATA00	I/O	1.8 V	eSPI	ESPI_IO_0	P58	S59	USB5+	-	-	-	-
-	P	-	Power	GND	P59	S60	USB5-	-	-	-	-
USB1_D_P	I/O	3.3 V	USB0	USB0+	P60	S61	GND	Power	-	P	-
USB1_D_N	I/O	3.3 V	USB0	USB0-	P61	S62	USB3_SSTX+	USB3	-	O	-
GPIO1_IO12	O	3.3 V	USB0	USB0_EN_OC#	P62	S63	USB3_SSTX-	USB3	-	O	-
USB1_VBUS	I	5 V	USB0	USB0_VBUS_DET	P63	S64	GND	Power	-	P	-
GPIO1_IO10	I	1.8 V	USB0	USB0_OTG_ID	P64	S65	USB3_SSRX+	USB3	-	I	-
-	I/O	-	USB1	USB1+	P65	S66	USB3_SSRX-	USB3	-	I	-
-	I/O	-	USB1	USB1-	P66	S67	GND	Power	-	P	-
-	I/O	3.3 V	USB1	USB1_EN_OC#	P67	S68	USB3+	USB3	-	I/O	-
-	P	-	Power	GND	P68	S69	USB3-	USB3	-	I/O	-
-	I/O	-	USB2	USB2+	P69	S70	GND	Power	-	P	-
-	I/O	-	USB2	USB2-	P70	S71	USB2_SSTX+	USB2	-	O	-
-	I/O	3.3 V	USB2	USB2_EN_OC#	P71	S72	USB2_SSTX-	USB2	-	O	-
-	-	-	-	RSVD	P72	S73	GND	Power	-	P	-
-	-	-	-	RSVD	P73	S74	USB2_SSRX+	USB2	-	I	-
	I/O	3.3 V	USB3	USB3_EN_OC#	P74	S75	USB2_SSRX-	USB2	-	I	-
-	-	-	-	-	Key		-	-	-	-	-
-	-	-	-	-			-	-	-	-	-
-	-	-	-	-			-	-	-	-	-
SD1_RESET_B	O	3.3 V	PCIE1	PCIE_A_RST#	P75	S76	PCIE_B_RST#	-	-	-	-
-	I/O	3.3 V	USB4	USB4_EN_OC#	P76	S77	PCIE_C_RST#	-	-	-	-
-	-	-	-	PCIE_B_CKREQ#	P77	S78	PCIE_C_RX+/SERDES_1_RX+	-	-	-	-
-	I	3.3 V	PCIE1	PCIE_A_CKREQ#	P78	S79	PCIE_C_RX-/SERDES_1_RX-	-	-	-	-
-	P	-	Power	GND	P79	S80	GND	Power	-	P	-
-	-	-	-	PCIE_C_REFCK+	P80	S81	PCIE_C_TX+/SERDES_1_TX+	-	-	-	-
-	-	-	-	PCIE_C_REFCK-	P81	S82	PCIE_C_TX-/SERDES_1_TX-	-	-	-	-
-	P	-	Power	GND	P82	S83	GND	Power	-	P	-
PCIE_CLK_P	O	1.0 V	PCIE1	PCIE_A_REFCK+	P83	S84	PCIE_B_REFCK+	-	-	-	-
PCIE_CLK_N	O	1.0 V	PCIE1	PCIE_A_REFCK-	P84	S85	PCIE_B_REFCK-	-	-	-	-
-	P	-	Power	GND	P85	S86	GND	Power	-	P	-
PCIE_RXN_P	I	1.0 V	PCIE1	PCIE_A_RX+	P86	S87	PCIE_B_RX+	-	-	-	-
PCIE_RXN_N	I	1.0 V	PCIE1	PCIE_A_RX-	P87	S88	PCIE_B_RX-	-	-	-	-
-	P	-	Power	GND	P88	S89	GND	Power	-	P	-
PCIE_TXN_P	O	1.0 V	PCIE1	PCIE_A_TX+	P89	S90	PCIE_B_TX+	-	-	-	-

PCIE_TXN_N	O	1.0 V	PCIE1	PCIE_A_TX-	P90	S91	PCIE_B_TX-	-	-	-	-
-	P	-	Power	GND	P91	S92	GND	Power	-	P	-
HDMI_TX2_P	O	1.8 V	HDMI	HDMI_D2+ / DP1_LANE0+	P92	S93	DP0_LANE0+	DP	-	O	-
HDMI_TX2_N	O	1.8 V	HDMI	HDMI_D2- / DP1_LANE0-	P93	S94	DP0_LANE0-	DP	-	O	-
-	P	-	Power	GND	P94	S95	DP0_AUX_SEL	DP	-	I	-
HDMI_TX1_P	O	1.8 V	HDMI	HDMI_D1+ / DP1_LANE1+	P95	S96	DP0_LANE1+	DP	-	O	
HDMI_TX1_N	O	1.8 V	HDMI	HDMI_D1- / DP1_LANE1-	P96	S97	DP0_LANE1-	DP	-	O	-
-	P	-	Power	GND	P97	S98	DP0_HPD	DP	-	I	-
HDMI_TX0_P	O	1.8 V	HDMI	HDMI_D0+ / DP1_LANE2+	P98	S99	DP0_LANE2+	-	-	-	-
HDMI_TX0_N	O	1.8 V	HDMI	HDMI_D0- / DP1_LANE2-	P99	S100	DP0_LANE2-	-	-	-	-
-	P	-	Power	GND	P100	S101	GND	Power	-	P	-
HDMI_TXC_P	O	1.8 V	HDMI	HDMI_CK+ / DP1_LANE3+	P101	S102	DP0_LANE3+	-	-	-	-
HDMI_TXC_N	O	1.8 V	HDMI	HDMI_CK- / DP1_LANE3-	P102	S103	DP0_LANE3-	-	-	-	-
-	P	-	Power	GND	P103	S104	USB3_OTG_ID	USB3	1.8 V	I	GPIO1_IO11
HDMI_HPD	I	1.8 V	HDMI	HDMI_HPD / DP1_HPD	P104	S105	DP0_AUX+	DP	3.3 V	I/O	-
HDMI_DDC_SCL	I/O	1.8 V	HDMI	HDMI_CTRL_CK / DP1_AUX+	P105	S106	DP0_AUX-	DP	3.3 V	I/O	-
HDMI_DDC_SDA	I/O	1.8 V	HDMI	HDMI_CTRL_DAT / DP1_AUX-	P106	S107	LCD1_BKLT_EN	LVDS1	1.8 V	O	-
-	-	-	-	DP1_AUX_SEL	P107	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1	1.8 V	O	LVDS1_CLK_P
SAI2_TXC	I/O	1.8 V	GPIO	GPIO0 / CAM0_PWR#	P108	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1	1.8 V	O	LVDS1_CLK_N
SAI2_TXD0	I/O	1.8 V	GPIO	GPIO1 / CAM1_PWR#	P109	S110	GND	Power	-	P	-
SAI3_RXFS	I/O	1.8 V	GPIO	GPIO2 / CAM0_RST#	P110	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1	1.8 V	I/O	LVDS1_D0_P
SAI5_RXC	I/O	1.8 V	GPIO	GPIO3 / CAM1_RST#	P111	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1	1.8 V	I/O	LVDS1_D0_N
SAI5_RXFS	I/O	1.8 V	GPIO	GPIO4 / HDA_RST#	P112	S113	eDP1_HPD	-	-	-	-
SPDIF_EXT_CLK	I/O	1.8 V	GPIO	GPIO5 / PWM_OUT	P113	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1	1.8 V	I/O	LVDS1_D1_P
SAI3_RXC	I/O	1.8 V	GPIO	GPIO6 / TACHIN	P114	S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1	1.8 V	I/O	LVDS1_D1_N
SAI1_MCLK	I/O	1.8 V	GPIO	GPIO7	P115	S116	LCD1_VDD_EN	LVDS1	1.8 V	O	-
SAI1_RXC	I/O	1.8 V	GPIO	GPIO8	P116	S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1	1.8 V	I/O	LVDS1_D2_P
SAI1_RXD2	I/O	1.8 V	GPIO	GPIO9	P117	S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1	1.8 V	I/O	LVDS1_D2_N
GPIO1_IO05	I/O	1.8 V	GPIO	GPIO10	P118	S119	GND	Power	-	P	-
ECSPI_MOSI	I/O	1.8 V	GPIO	GPIO11	P119	S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1	1.8 V	I/O	LVDS1_D3_P
-	P	-	Power	GND	P120	S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1	1.8 V	I/O	LVDS1_D3_N
I2C2_SCL	O	1.8 V	I2C	I2C_PM_CK	P121	S122	LCD1_BKLT_PWM	LVDS1	1.8 V	O	SPDIF_RX
I2C2_SDA	I/O	1.8 V	I2C	I2C_PM_DAT	P122	S123	GPIO13	GPIO	1.8 V	I/O	ECSPI_SS0
-	I	1.8 V	BOOT	BOOT_SEL0#	P123	S124	GND	Power	-	P	-
-	I	1.8 V	BOOT	BOOT_SEL1#	P124	S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0	1.8 V	O	LVDS0_D0_P
-	I	1.8 V	BOOT	BOOT_SEL2#	P125	S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0	1.8 V	O	LVDS0_D0_N
POR_B	O	1.8 V	CONFIG	RESET_OUT#	P126	S127	LCD0_BKLT_EN	LVDS0	1.8 V	O	-
POR_B	I	1.8 V	CONFIG	RESET_IN#	P127	S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0	1.8 V	O	LVDS0_D1_P

ONOFF	I	1.8 V	CONFIG	POWER_BTN#	P128	S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0	1.8 V	O	LVDS0_D1_N
UART1_TXD	O	1.8 V	SER	SER0_TX	P129	S130	GND	Power	-	P	-
UART1_RXD	I	1.8 V	SER	SER0_RX	P130	S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0	1.8 V	O	LVDS0_D2_P
UART3_RXD	O	1.8 V	SER	SER0_RTS#	P131	S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0	1.8 V	O	LVDS0_D2_N
UART3_TXD	I	1.8 V	SER	SER0_CTS#	P132	S133	LCD0_VDD_EN	LVDS0	1.8 V	O	-
-	P	-	Power	GND	P133	S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0	1.8 V	O	LVDS0_CLK_P
SD1_DATA6	O	1.8 V	SER	SER1_TX	P134	S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0	1.8 V	O	LVDS0_CLK_N
SD1_DATA7	I	1.8 V	SER	SER1_RX	P135	S136	GND	Power	-	P	-
UART2_TXD	O	1.8 V	SER	SER2_TX	P136	S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0	1.8 V	O	LVDS0_D3_P
UART2_RXD	I	1.8 V	SER	SER2_RX	P137	S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0	1.8 V	O	LVDS0_D3_N
SD1_DATA4	O	1.8 V	SER	SER2_RTS#	P138	S139	I2C_LCD_CK	I2C	1.8 V	I/O	I2C3_SCL
SD1_DATA5	I	1.8 V	SER	SER2_CTS#	P139	S140	I2C_LCD_DAT	I2C	1.8 V	I/O	I2C3_SDA
UART4_TXD	O	1.8 V	SER	SER3_TX	P140	S141	LCD0_BKLT_PWM	LVDS0	1.8 V	O	SPDIF_TX
UART4_RXD	I	1.8 V	SER	SER3_RX	P141	S142	GPIO12	GPIO	1.8 V	I/O	ECSPI2_SCLK
-	P	-	Power	GND	P142	S143	GND	Power	-	P	-
SAI5_RXD1	O	1.8 V	CAN	CAN0_TX	P143	S144	eDP0_HPD	-	-	-	-
SAI5_RXD2	I	1.8 V	CAN	CAN0_RX	P144	S145	WDT_TIME_OUT#	CONFIG	1.8 V	O	GPIO1_IO02
SAI5_RXD3	O	1.8 V	CAN	CAN1_TX	P145	S146	PCIE_WAKE#	PCIE1	3.3 V	I	SD1_STROBE
SAI5_MCLK	I	1.8 V	CAN	CAN1_RX	P146	S147	VDD_RTC	Power	3,0 V	P	-
-	P	3.0… 5.25 V	Power	VDD_IN	P147	S148	LID#	CONFIG	1.8 V	I	GPIO1_IO03
-	P	3.0… 5.25 V	Power	VDD_IN	P148	S149	SLEEP#	CONFIG	1.8 V	I	GPIO1_IO00
-	P	3.0… 5.25 V	Power	VDD_IN	P149	S150	VIN_PWR_BAD#	CONFIG	VDD_IN	I	-
-	P	3.0… 5.25 V	Power	VDD_IN	P150	S151	CHARGING#	CONFIG	1.8 V	I	GPIO1_IO06
-	P	3.0… 5.25 V	Power	VDD_IN	P151	S152	CHARGER_PRSNT#	CONFIG	1.8 V	I	GPIO1_IO07
-	P	3.0… 5.25 V	Power	VDD_IN	P152	S153	CARRIER_STBY#	CONFIG	1.8 V	O	PMIC_STBY_REQ
-	P	3.0… 5.25 V	Power	VDD_IN	P153	S154	CARRIER_PWR_ON	CONFIG	1.8 V	O	-
-	P	3.0… 5.25 V	Power	VDD_IN	P154	S155	FORCE_RECOV#	BOOT	1.8 V	I	-
-	P	3.0… 5.25 V	Power	VDD_IN	P155	S156	BATLOW#	CONFIG	1.8 V	I	GPIO1_IO01
-	P	3.0… 5.25 V	Power	VDD_IN	P156	S157	TEST#	CONFIG	1.8 V	-	-
-	-	-	-	-	-	S158	GND	Power	-	P	-

*not directly connected
NC = not connected
RSVD = reserved

3.2 System components

3.2.1 i.MX 8M Plus

3.2.1.1 i.MX 8M Plus derivatives

Depending on the TQMa8MPxS version, one of the following i.MX 8M Plus derivatives is assembled.

Table 3: i.MX 8M Plus derivatives

TQMa8MPxS version	i.MX 8M Plus derivative	i.MX 8M Plus clocks	Temperature range
TQMa8MPDS-AA	i.MX 8M Plus Dual 3 ML/AI	A53: 1.6 GHz, M7: 800 MHz	–25 °C … +85 °C
TQMa8MPQS-AA	i.MX 8M Plus Quad 6 Video	A53: 1.6 GHz, M7: 800 MHz	–25 °C … +85 °C
TQMa8MPQS-AB	i.MX 8M Plus Quad 8 ML/AI	A53: 1.6 GHz, M7: 800 MHz	–25 °C … +85 °C
TQMa8MPQS-AC	i.MX 8M Plus Quad 8 ML/AI	A53: 1.6 GHz, M7: 800 MHz	–25 °C … +85 °C

Other configurations on request.

3.2.1.2 i.MX 8M Plus errata

Attention: Destruction or malfunction, i.MX 8M Plus errata	
	Please take note of the current i.MX 8M Plus errata (5).

3.2.1.3 Boot modes

The i.MX 8M Plus has a ROM with integrated boot loader. After the release of PMIC_POR# the System Controller (SCU) boots from the internal ROM and then loads the program image from the selected boot device. For example, the integrated eMMC or the optional QSPI NOR Flash can be selected as the default boot device. The following boot sources are supported by TQMa8MPxS:

Table 4: Boot sources of the TQMa8MPxS according to SMARC standard

Boot source	Interface
eMMC	SD3
SD-Card	SD2
QSPI-NOR	QuadSPI
Serial downloader	USB1

Alternatively, an image can be loaded into the internal RAM using the serial downloader.
More information about the boot flow can be found in the Reference Manual (1), and the Data Sheet (2) of i.MX 8M Plus.

3.2.1.4 Boot mode pins

The SMARC standard requires a defined wiring of the SMARC pins BOOT_SEL[2:0]. These are converted to the boot mode pins BOOT_MODE[3:0] by a CPLD. The FORCE_RECOV# signal is used to switch to the “Force Recovery” or Serial Downloader mode.

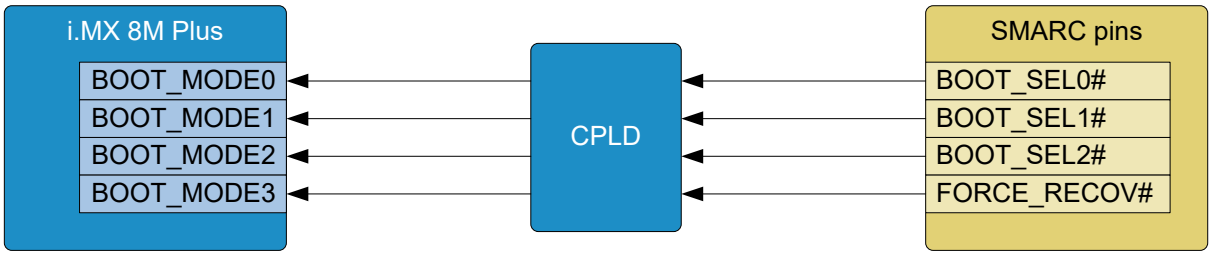

Figure 4: Boot mode circuitry

Table 5: Boot configuration

BOOT_MODE[3:0]	FORCE_RECOV#	BOOT_SEL[2:0]#	Boot media
0011	1	001	SD-Card
0110	1	100	QuadSPI 4k (QSPI-NOR-Flash)
0010	1	110	eMMC
0000	1	101	Remote boot (set to 'Boot from Fuses' as the i.MX 8M Plus does not support remote mode)
0001	0	xxx	Recovery mode / serial downloader

3.2.2 Memory

3.2.2.1 LPDDR4 SDRAM

The memory interface of the i.MX 8M Plus supports DDR4 and LPDDR4 memory (32 bit bus) with a maximum clock rate of 2.0 GHz, which meets JEDEC LPDDR4-4000 standard. The TQMa8MPxS exclusively uses LPDDR4. A maximum of 8 Gbyte of LPDDR4 SDRAM is supported.

3.2.2.2 eMMC

eMMC is connected via the USDHC3 interface of the i.MX 8M Plus. A maximum transfer rate of 400 MB/s is supported, which corresponds to HS400 mode. Series resistors are provided for the CLK, DATA and CMD signals.

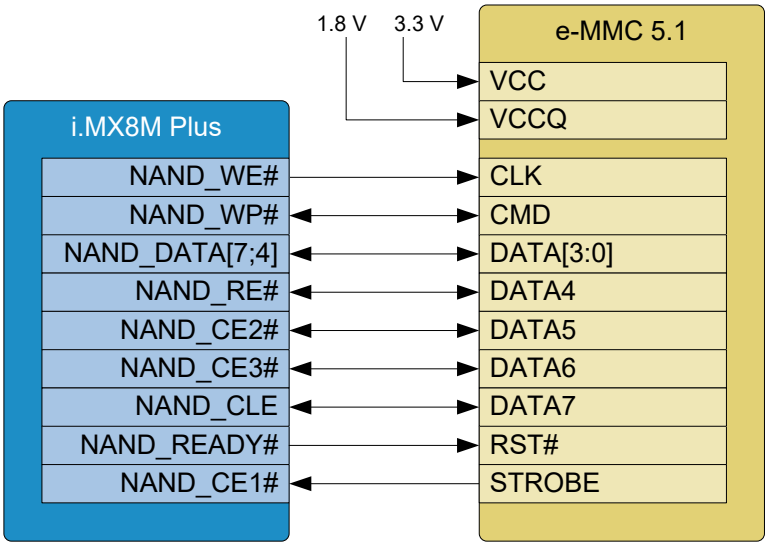

Figure 5: Block diagram eMMC

3.2.2.3 QSPI NOR Flash

QSPI NOR flash can optionally be assembled on the TQMa8MPxS.

33 Ω series resistors are provided in the data lines. The supply voltage of the flash is 1.8 V.

If a NOR flash is equipped, part of the ESPI interface on the SMARC connector is omitted. Therefore, ESPI is only fully available on the SMARC pins if no NOR flash is equipped.

3.2.2.4 EEPROM

Two EEPROMs are provided on the TQMa8MPxS, one customer-specific and one SMARC-specific. Both are connected to the I2C_GP bus (I2C1) of the TQMa8MPxS and supplied with 1.8 V.

The slave address of the SMARC-specific EEPROM is set to 0x50 in accordance with the specification. Information on the module configuration can be found at this address.

The second EEPROM is optional and can be used for customer-specific data.

3.2.3 Trust Secure Element

The NXP Trust Secure Element SE050 (alternatively SE051) is available on the TQMa8MPxS as an assembly option and connected to the I2C1-bus.

As the SMARC standard does not provide any pins for the smartcard interfaces, the signals for these interfaces in accordance with ISO14443 and ISO7816 are routed to the unused SMARC pins of the PCIe_D interface but are disconnected by default using 0R resistors.

Table 6: Connection of SE050 to SMARC connector

Signal SE050	SMARC-Pin
ISO_14443_LA	S46 – MDIO_DAT
ISO_14443_LB	S45 – MDIO_CLK
ISO_7816_IO1	S29 – PCIE_D_TX+
ISO_7816_IO2	S30 – PCIE_D_TX-
ISO_7816_CLK	S32 – PCIE_D_RX+
ISO_7816_RST	S33 – PCIE_D_RX-

3.2.4 RTC

The TQMa8MPxS provides an i.MX 8M Plus-internal RTC or an optional discrete RTC PCF85063A.

3.2.4.1 i.MX 8M Plus internal RTC

The i.MX 8M Plus provides an RTC, which has its own power domain (V_1V8_SNVS). The RTC power domain SNVS of the i.MX 8M Plus is supplied by the PMIC. The PMIC is supplied by the TQMa8MPxS input voltage of VDD_IN.

The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

Note: RTC power supply	
	The CPU internal RTC can be used in regular operation. If the TQMa8MPxS supply fails, it is no longer available, since the i.MX 8M Plus's SNVS rail is no longer supplied. We recommend using the optional RTC PCF85063A.

3.2.4.2 Discrete RTC PCF85063A

In addition to the i.MX 8M Plus internal RTC the TQMa8MPxS provides a discrete RTC PCF85063A as an assembly option, which is controlled by the I2C1 bus. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C. The RTC PCF85063A is supplied by VDD_RTC (SMARC pin S147) when the PMIC or the TQMa8MPxS supply is switched off.

- The discrete RTC has I2C address `0x51 / 101 0001b`

3.2.5 Temperature Sensor

The TMP1075DSGR temperature sensor from Texas Instruments is used for temperature measurement. The ALERT alarm output (TEMP_EVENT#) is routed internally to a GPIO pin (HDMI_CEC) of the i.MX 8M Plus.

3.2.6 Interfaces

3.2.6.1 CAN

The i.MX 8M Plus provides two CAN interfaces, CAN1 and CAN2, which are directly routed to the SMARC-Pins.

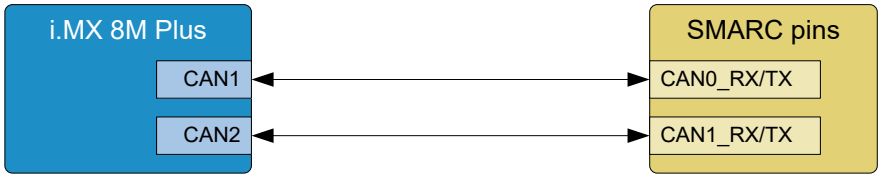

Figure 6: Block diagram CAN

3.2.6.2 Ethernet

Two Gigabit Ethernet interfaces (GBE0, GBE1) are made available on the SMARC pins of the TQMa8MPxS. In accordance with the SMARC standard, the Ethernet PHYs are part of the SMARC module, so that only the transformer is implemented on the carrier. Both PHYs are operated in “mirror mode”, i.e. the differential pairs between PHY and SMARC pins are inverted. Both PHYs are connected to the same SMI bus in order to have more GPIOs available.

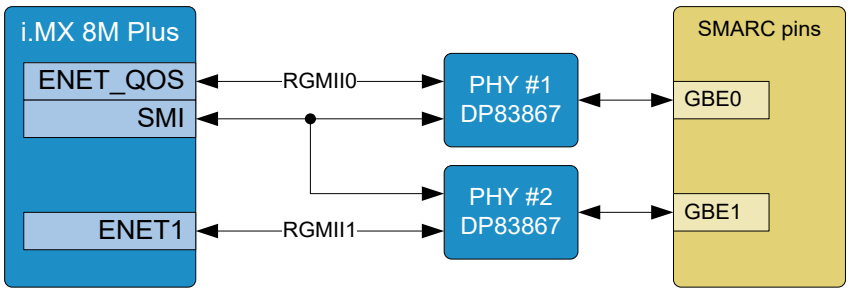

Figure 7: Block diagram Ethernet overview

The LED signals are defined in the SMARC specification as 3.3 V tolerant open-drain outputs for a current of at least 24 mA each. The IEEE1588 signals GBE[1:0]_SDP are implemented as EVENT_IN / EVENT_OUT. As these signals have an IO level of 3.3 V according to the SMARC standard, switchable level converters and analog switches are used. The data direction of these is controlled by GPIOs of the CPU.

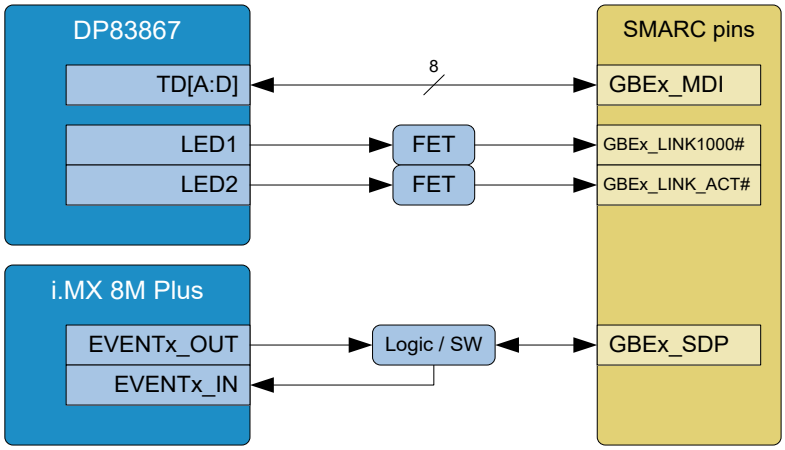

Figure 8: Block diagram of single Ethernet interface

3.2.6.3 I²C

The I²C interfaces on the SMARC pins are provided by the CPU as follows:

Table 7: I²C interfaces

SMARC pins	Interface i.MX 8M Plus
I2C_GP	I2C1
I2C_PM	I2C2
I2C_LCD	I2C3
I2C_CAM0	I2C4
I2C_CAM1	I2C6

Pull-up resistors are provided on the TQMa8MPxS for all I2C signals in accordance with the standard. In addition to several I2C devices, level converters are also used on the TQMa8MPxS.

The following table shows the addresses of the I2C components used on the TQMa8MPxS:

Table 8: I²C addresses

Bus	I2C-Slave	Address	Note
I2C1 (I2C_GP)	EEPROM	0x50	SMARC specific
	EEPROM ID-Page	0x58	SMARC specific
	EEPROM	0x54	Customer specific; optional
	EEPROM ID-Page	0x5C	Customer specific; optional
	RTC PCF85063	0x51	Optional
	TSE SE050	0x48	standard NP
	PCIE clock generator	0x6A	Optional
	USB hub	0x44	standard not connected
	Gyroscope ISM330 (optional)	0x6B	standard NP
I2C2 (I2C_PM)	PMIC PCA9450C	0x25	
	Port expander	0x73	
	Temperature sensor TMP1075	0x4A	
I2C3 (DSI0_I2C)	DisplayPort bridge	0x0F	Optional

3.2.6.4 JTAG

The JTAG interface of the i.MX 8M Plus is made available on a connector (JST SM10B-SRSS-TB) on the TQMa8MPxS that is not fitted as standard. Its position uses an area on the upper side of the board specified in the SMARC standard. The pin assignment of the connector and the model are defined in the SMARC standard.

The connector wiring can be found in the following table:

Table 9: JTAG signals

Pin	Name	DIR	CPU signal
1	VDD_JTAG_IO	P	V_1V8
2	JTAG_TRST#	-	n.c.
3	JTAG_TMS	I	JTAG_TMS
4	JTAG_TDO	O	JTAG_TDO
5	JTAG_TDI	I	JTAG_TDI
6	JTAG_TCK	I	JTAG_TCK
7	JTAG_RTCK	I	n.c.
8	JTAG_RESET_IN	I	POR# via buffer; NP
9	MFG_MODE#	I	n.c.
10	GND	P	GND

3.2.6.5 Watchdog

The watchdog signal WDOG_ANY of the i.MX 8M Plus is connected to the SMARC pin WDT_TIME_OUT# and to the WDOG# pin of the PMIC. Both can be disconnected via 0R bridges. The watchdog function of the PMIC is deactivated by default and must be activated via software.

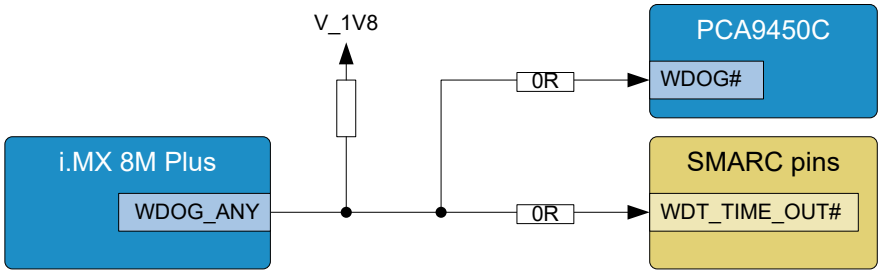

Figure 9: Block Diagram Watchdog

3.2.6.6 GPIO

The SMARC standard provides a total of 14 GPIO pins. According to the standard, GPIO0…5 are recommended for use as outputs and GPIO6…13 are recommended for use as inputs. However, the native GPIOs of the i.MX 8M Plus can be used in both directions. GPIO5 and GPIO6 can be used as a PWM output or tachometer input.

In accordance with the SMARC specification, all GPIOs are provided with discrete pull-up resistors.

Table 10: GPIO signals

SMARC pin	Origin	Processor pin	Preferred direction	Alternative function
GPIO0 / CAM0_PWR#	i.MX 8M Plus	SAI2_TXC	Output	GPIO4_IO25
GPIO1 / CAM1_PWR#	i.MX 8M Plus	SAI2_TXD0	Output	GPIO4_IO26
GPIO2 / CAM0_RST#	i.MX 8M Plus	SAI3_RXFS	Output	GPIO4_IO28
GPIO3 / CAM1_RST#	i.MX 8M Plus	SAI5_RXC	Output	GPIO3_IO20
GPIO4 / HDA_RST#	i.MX 8M Plus	SAI5_RXFS	Output	GPIO3_IO19
GPIO5 / PWM_OUT	i.MX 8M Plus	SPDIF_EXT_CLK	Output	PWM1 / GPIO5_IO05
GPIO6 / TACHIN	i.MX 8M Plus	SAI3_RXC	Input	GPT1_CLK / GPIO4_IO29
GPIO7	i.MX 8M Plus	SAI1_MCLK	Input	GPIO4_IO20
GPIO8	i.MX 8M Plus	SAI1_RXC	Input	GPIO4_IO01
GPIO9	i.MX 8M Plus	SAI1_RXD2	Input	GPIO4_IO04
GPIO10	i.MX 8M Plus	GPIO1_IO05	Input	M7_NMI / GPIO1_IO05
GPIO11	i.MX 8M Plus	ECSPI2_MOSI	Input	GPIO5_IO11
GPIO12	i.MX 8M Plus	ECSPI2_SCLK	Input	GPIO5_IO10
GPIO13	i.MX 8M Plus	ECSPI2_SS0	Input	GPIO5_IO13

3.2.6.7 Camera Interfaces (CSI)

The i.MX 8M Plus provides two CSI camera interfaces. The CSI0 pins of the SMARC connector are connected to CSI2 of the i.MX 8M Plus. The CSI1 interface of the i.MX 8M Plus is connected to the CSI1 pins of the SMARC connector.

CSI1 uses all four differential data pairs of the CPU, whereas CSI0 only uses two. Both camera interfaces have independent I2C buses, which are always connected directly to the SMARC pins.

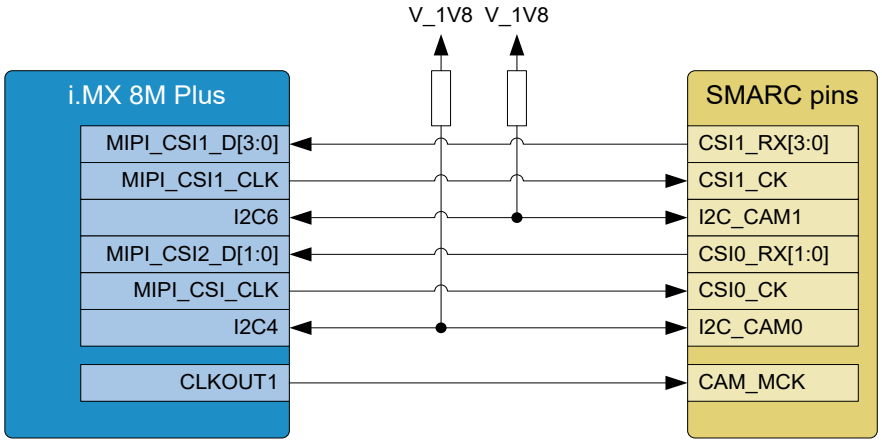

Figure 10: Block diagram MIPI CSI

3.2.6.8 LVDS

The CPU has two four-channel LVDS interfaces. These interfaces are connected directly to the corresponding SMARC pins, eliminating the need for additional wiring. The LVDS control signals, BKLT_EN and VDD_EN, are provided by the port expander outputs and the PWM signals, BKLT_PWM, are provided by the processors PWM-capable pins, for which SPDIF_TX and SPDIF_RX are used.

I2C3 is used as the I2C bus for communicating with the displays.

The LVDS1 pins can optionally be mapped to DSI signals.

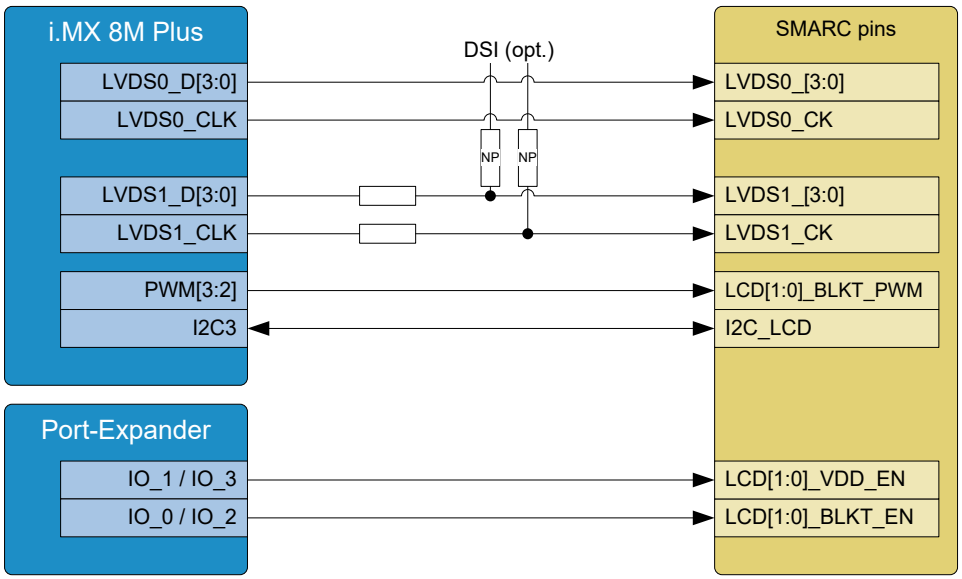

Figure 11: Block diagram LVDS

3.2.6.9 DisplayPort

In addition to LVDS, the SMARC standard also specifies HDMI and DisplayPort as display interfaces. To enable practical use of the DSI signals from the CPU, a DisplayPort bridge is used to convert the MIPI DSI signals. It should be noted that the bridge only allows two-channel DisplayPort. The other channels remain unconnected.

If the DisplayPort bridge is not populated, the DSI signals can be routed to the LVDS1 pins of the SMARC connector via a placement option. Termination is not necessary according to (3).

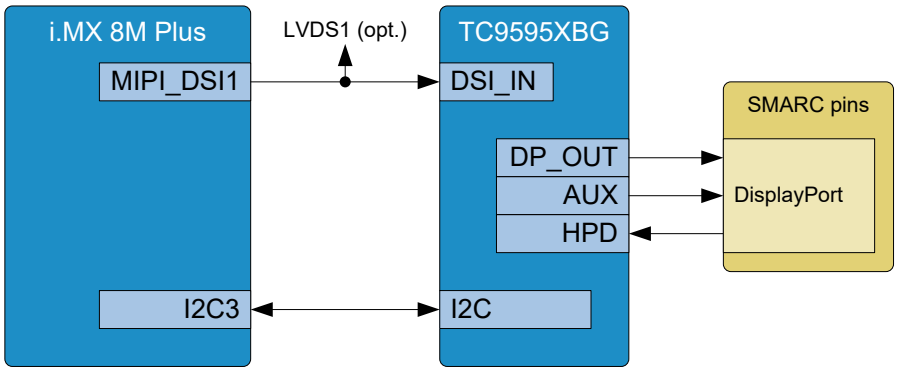

Figure 12: Block diagram DisplayPort

3.2.6.10 HDMI

The i.MX 8M Plus provides an HDMI interface according to the display specification "HDMI 2.0a".

The maximum resolutions are 3840x2160 @ 30 fps or 1920x1080 @ 120 fps.

As there are no eARC signals in the SMARC standard, these are left unconnected. Correct wiring in accordance with the HDMI specification is required on the mainboard. Corresponding signal conditioning is not implemented on the module.

Control signals such as CEC are not provided by the SMARC standard and can therefore not be used.

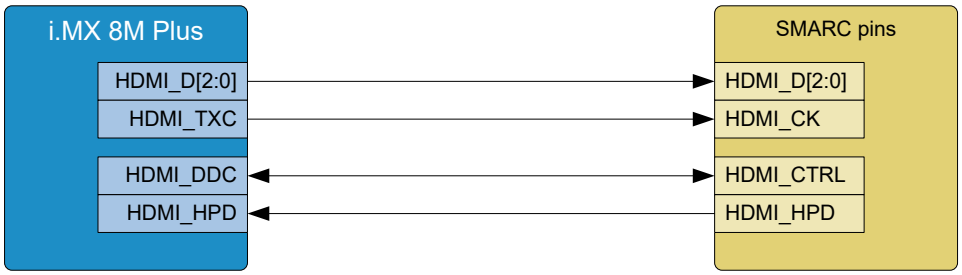

Figure 13: Block diagram HDMI

3.2.6.11 Audio (I2S)

The I2S0 interface on the SMARC pins is provided by the SAI5 interface of the i.MX 8M Plus. The SAI5 interface is also connected to the DisplayPort bridge as an assembly option, but is not connected to it by default.

The I2S2 interface is also connected to the CPU via SAI3.

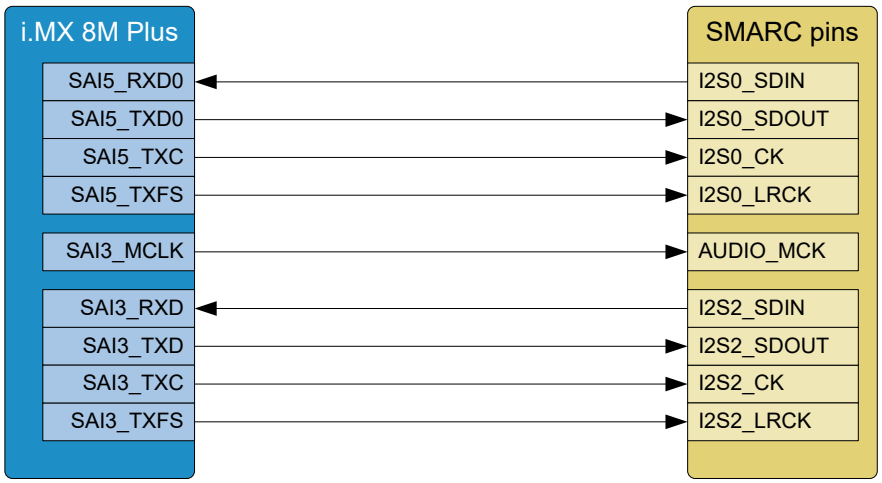

Figure 14: Block diagram I2S

3.2.6.12 PCIe

A total of four PCIe interfaces are defined in the SMARC standard. However, the i.MX 8M Plus can only provide one PCIe 3.0 lane. It is connected to the PCIE_A pins; the PCIE_[D:B] pins are not provided.

Based on experience with jitter requirements of previous i.MX processors, the TQMa8MPxS provides an external clock source for the i.MX 8M Plus and the PCIe interface. As SMARC defines the clock pins as outputs, the clock driver cannot be provided on the mainboard but can be implemented on the TQMa8MPxS. To reduce costs in sensitive designs, 0R resistors are provided to bypass the clock generator. Compliance with the jitter requirements must be specifically checked for this use case.

The internal clock must be deactivated via software because the internally generated clock would otherwise conflict with the external clock source. The PCIe clock generator is connected via I2C. The control signals of its two channels are connected and can be activated by the CPU or the CLKREQ# signal on the SMARC connector via OR linking.

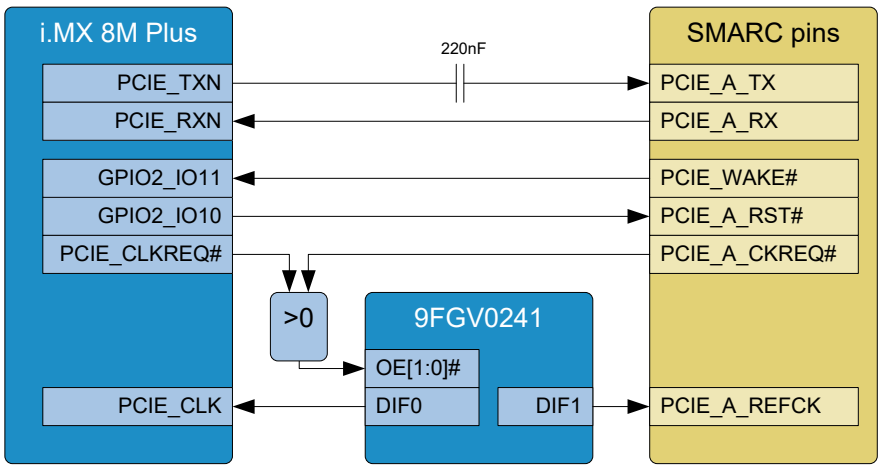

Figure 15: Block Diagram PCI Express

3.2.6.13 SPI

The SPI0 interface connects to ECSPI1 of the i.MX 8M Plus. The second chip select signal is provided as a GPIO.

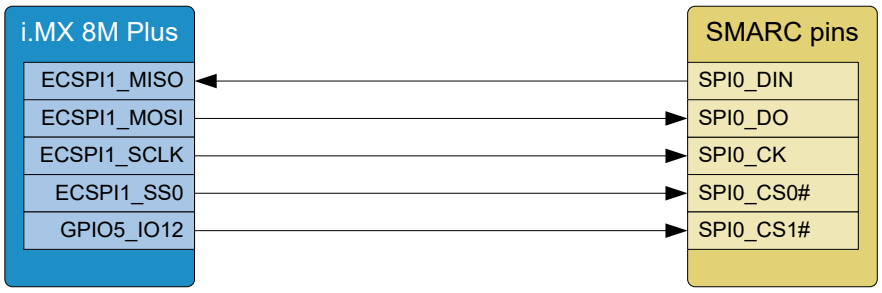

Figure 16: Block diagram SPI

3.2.6.14 eSPI

The eSPI pins are only optionally wired and connected to the QSPI interface of the i.MX 8M Plus: The signals are only routed to the outside if the optional NOR flash is not installed. As this is a memory interface and not an eSPI interface according to the Intel-standard, functional restrictions may occur if components other than QSPI memory are connected.

ESPI_RESET# is provided as an output function of a GPIO that is logically ORed with the POR_B signal of the i.MX 8M Plus. This means that an external reset can be performed either by the system when the CPU reboots or alternatively by means of defined CPU control.

The ESPI_ALERT0# signal is connected to the ECSPI_CS1# signal via a 0R resistor and is realized as a common GPIO of the CPU. This means that either an additional chip select or an alarm input is available. Due to the QSPI design, the chip select is provided as default. ESPI_ALERT1# is not used.

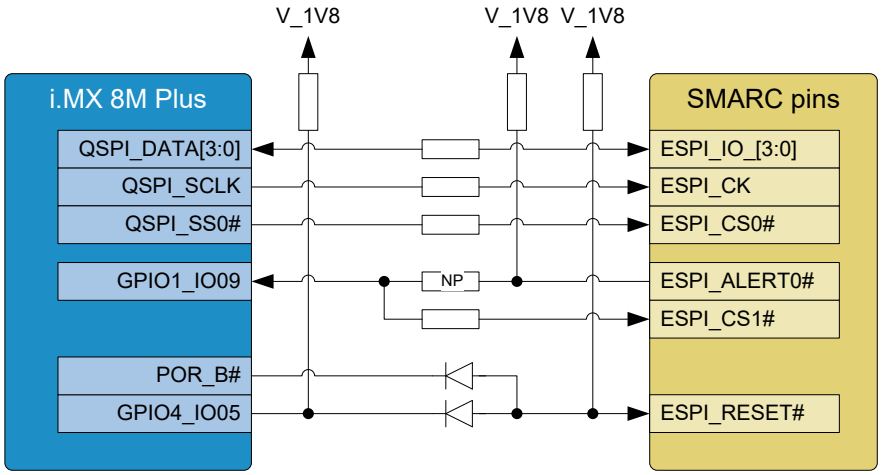

Figure 17: Block diagram eSPI

3.2.6.15 Serial ports

The i.MX 8M Plus provides up to four UART interfaces, which are all routed directly to the SMARC pins SER3…0 of the TQMa8MPxS. Due to the different signal scopes with two or four signals, part of the SD1 interface is also used in the multiplexing.

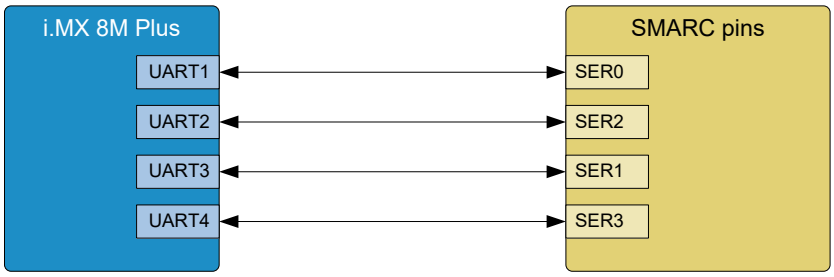

Figure 18: Block diagram Serial Ports

3.2.6.16 USB

A USB 3.0 hub is used to operate the majority of the USB interfaces provided in the SMARC standard. The hub is connected to the USB2 interface of the i.MX 8M Plus and is a placement option. To save on the USB hub in cost-sensitive designs, 0R resistors are provided with which the hub can be bridged. If the hub is not populated, the signals of the CPU interface can be made available directly on the SMARC pins of USB3.
The SMARC USB[5:0]_EN_OC# pins are bidirectional multifunction signals. In the absence of USB ports on the processor and the USB hub, the USB5 interface of the SMARC standard is not connected.

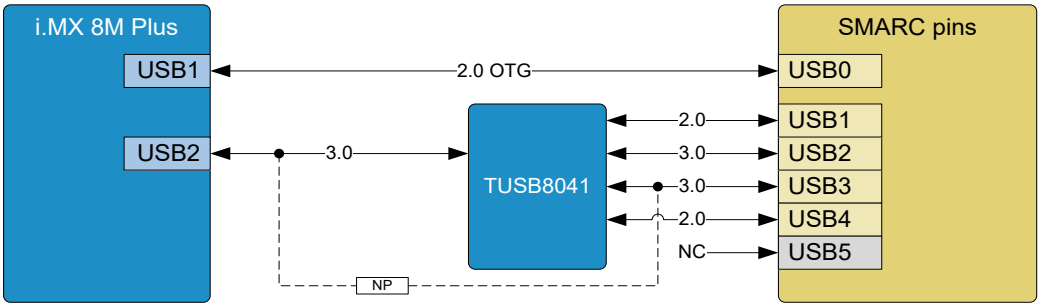

Figure 19: Block diagram USB interfaces

3.2.6.17 SD-Card

The SD card interface is provided by uSDHC2 of the i.MX 8M Plus. The SMARC signal SDIO_PWR_EN is used to enable the SD supply voltage on the carrier. uSDHC2 provides a 4-bit wide interface.

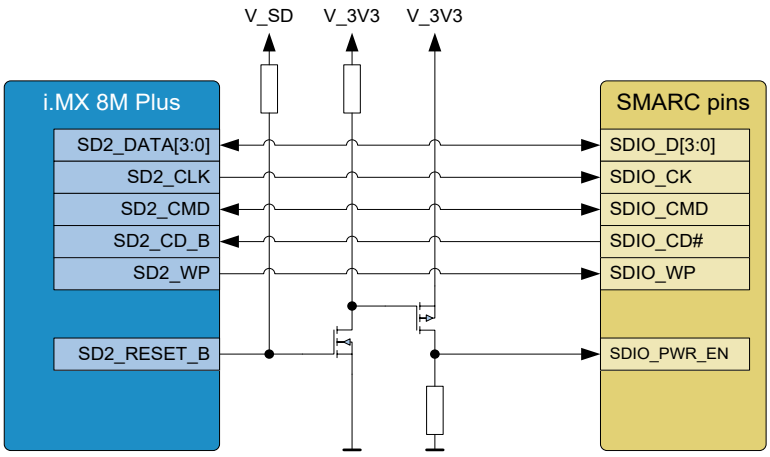

Figure 20: Block diagram SD card interface

3.2.7 Gyroscope

The TQMa8MPxS has an optional gyroscope with an I2C and SPI interface. This enables the TQMa8MPxS's position to be determined. The connection is made via I2C1.

3.2.8 Management signals

The following table shows an overview of the management pins used in accordance with the SMARC standard:

Table 11: Overview and wiring of the management pins

Signal	Type	Level	Description	Target
VIN_PWR_BAD#	I	VDD_IN	Status module voltage supply from carrier	Enable signals for PMIC and buck-boost controller
CARRIER_PWR_ON	O	1.8 V	Enable signals of the voltage supply on carrier	Generated via voltage divider from buck 4 and routed to buffer
CARRIER_STBY#	O	1.8 V	Status standby	PMIC_STBY_REQ from CPU to PMIC, linked to CARRIER_PWR_ON (Figure 26)
RESET_OUT#	O	1.8 V	Reset output of the PMIC	Generated from IMX_POR#; buffer with push-pull stage
RESET_IN#	I	1.8 V	Reset input	Routed to IMX_POR# via diode; pulled to 1.8 V
POWER_BTN#	I	1.8 V	Activation / deactivation of the CPU or the system	i.MX 8M Plus ON_OFF_BUTTON
SLEEP#	I	1.8 V	Carrier sleep status	i.MX 8M Plus GPIO1_IO00 (debouncing via RC element and Schmitt trigger)
LID#	I	1.8 V	Housing status	i.MX 8M Plus GPIO1_IO03 (equipped by default; debouncing via RC element and Schmitt trigger)
SMB_ALERT#	I	1.8 V	SM-Bus interrupt	i.MX 8M Plus GPIO1_IO03 (NP by default)
I2C_PM_DAT/CK	I/O	1.8 V	Power management I2C bus	See I2C interfaces (chapter 3.2.5.6)
BATLOW#	I	1.8 V	Low battery voltage	i.MX 8M Plus GPIO1_IO01
CHARGING#	I	1.8 V	Status charging process	i.MX 8M Plus GPIO1_IO06
CHARGER_PRSNT#	I	1.8 V	Status charging voltage	i.MX 8M Plus GPIO1_IO07
TEST#	I	1.8 V	Test function	Not used on module

To ensure that the CARRIER_STBY# signal corresponds to the SMARC power sequencing specification, it is logically linked to the CARRIER_PWRON signal. In sequencing, the high edge at CARRIER_STBY# must not occur before the high edge at CARRIER_PWRON. As the PMIC does not have a separate PGOOD signal, CARRIER_PWRON is generated using a buffer from the PMIC's 3.3 V, as this voltage represents the second-to-last step in the power sequence.

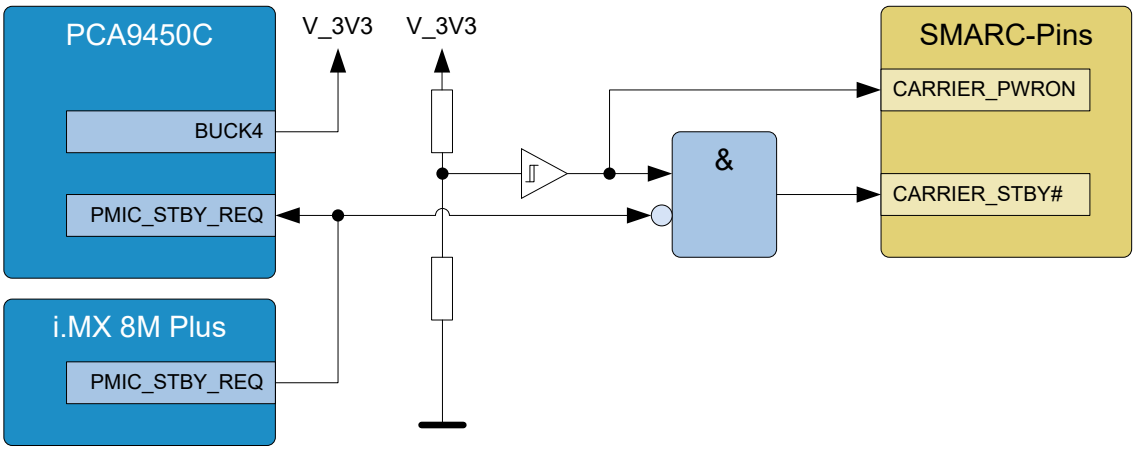

Figure 21: Block diagram CARRIER_STBY#

3.2.9 Unused CPU signals

CPU signals that cannot be mapped by the SMARC standard are either terminated directly on the module or left unconnected. These are primarily signals of the function groups EARC and CLK_IN.

According to the pinout of the CPU, the associated CPU pins have no alternative functions and therefore cannot be used as GPIOs or similar, which is why connecting them does not provide any added value.

3.2.10 Power

3.2.10.1 Power supply

In accordance with the SMARC specification, the TQMa8MPxS supports an input voltage range of 3.0 V to 5.25 V.
As the supply of the module is defined in the SMARC standard with a fixed pin assignment, no measures are provided with regard to reverse polarity protection or inrush currents. Measures against ESD and overvoltage, e.g. TVS diodes, are not implemented on the TQMa8MPxS itself. Appropriate solutions must always be provided on the mainboards (carriers).

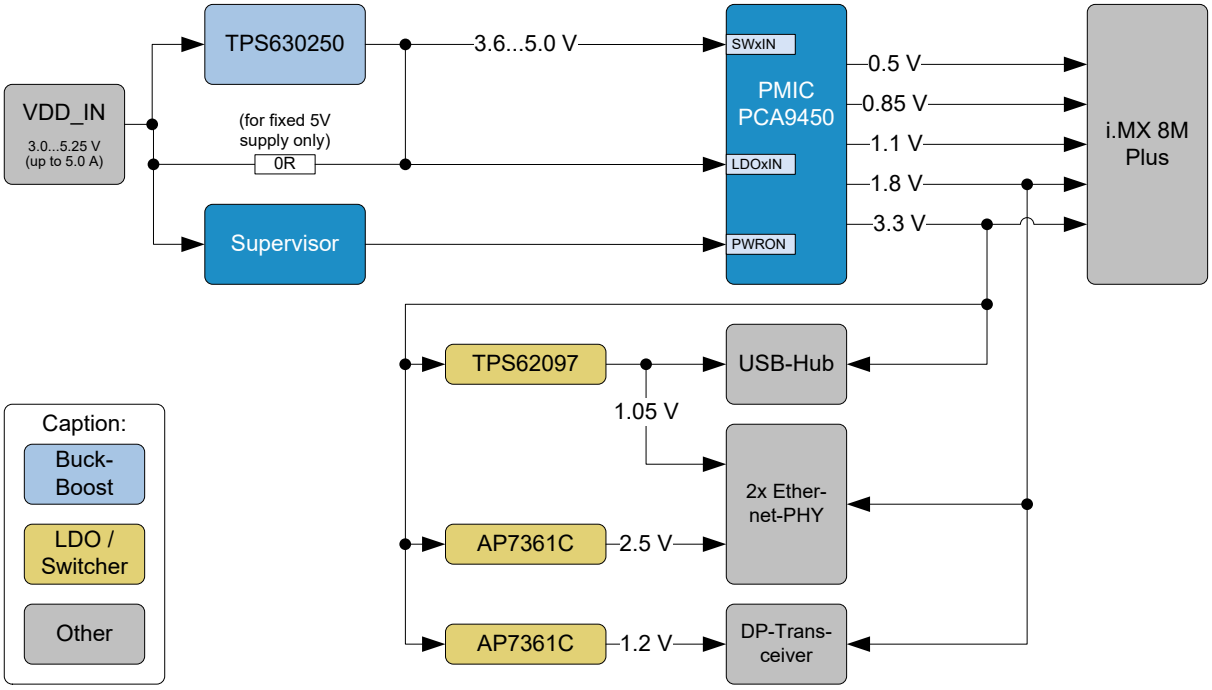

Figure 22: Block diagram Power Supply

3.2.10.2 Power consumption

The given power consumption has to be seen as an approximate value.
The TQMa8MPxS power consumption strongly depends on the application, the mode of operation and the operating system.
For more information on power consumption and savings options, see NXP Application Note AN12410 (6).

The following table shows TQMa8MPxS (with i.MX 8M Plus Quad) with 5 V power supply and power consumption parameters:

Table 12: Power consumption

Mode of operation	Current @ 5 V	Power consumption @ 5 V
Theoretical calculated peak (worst case)	TBD	TBD
U-Boot prompt	TBD	TBD
Linux-Idle	TBD	TBD
Linux with 100 % CPU load	TBD	TBD
Reset	TBD	TBD
Suspend to RAM mode	TBD	TBD

3.2.10.3 Voltage monitoring

A supervisor is provided to ensure that the module only starts after the supply voltage is within the valid range.

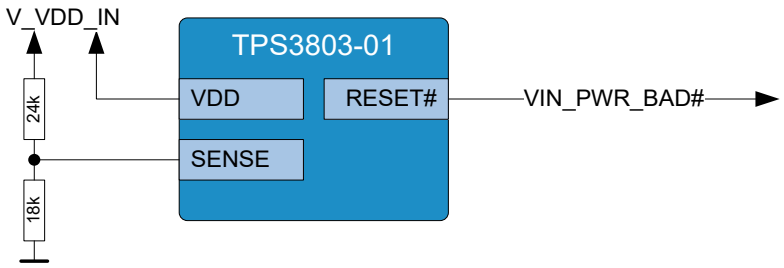

Figure 23: Block diagram Supervisior

Attention: Destruction or malfunction, supply voltage exceedance	
	The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa8MPxS.

3.2.11 Impedances

By default, all single-ended signals have a nominal impedance of 50 Ω ±10 %.
However, some interfaces on the TQMa8MPxS are routed with different impedances, depending on the signal requirements.

The following table is taken from the Hardware Developer's Guide (3) and shows the respective interfaces:

Table 13: Impedances

Signal / Interface	Impedance on TQMa8MPxS	Recommendation for carrier board
DDR DQS/CLK; PCIe CLK, TX/RX data pairs	85 Ω, differential	85 Ω ±10 %, differential
Differential USB signals	90 Ω, differential	90 Ω ±10 %, differential
Differential MIPI (CSI, DSI), HDMI, EARC, LVDS signals	100 Ω, differential	100 Ω ±10 %, differential
Differential RGMII signals	100 Ω, differential	100 Ω ±10 %, differential

4. SOFTWARE

The TQMa8MPxS is delivered with a preinstalled boot loader U-Boot.
The BSP provided by TQ-Systems GmbH is configured for the combination of TQMa8MPxS and MB-SMARC-2.
The boot loader U-Boot provides TQMa8MPxS-specific as well as board-specific settings, e.g.:

- i.MX 8M Plus configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

Further information can be found at https://support.tq-group.com/TQMa8MPxS.

If another bootloader is used, this data must be adapted. Contact TQ-Support for detailed information.

5. MECHANICS

5.1 Dimensions

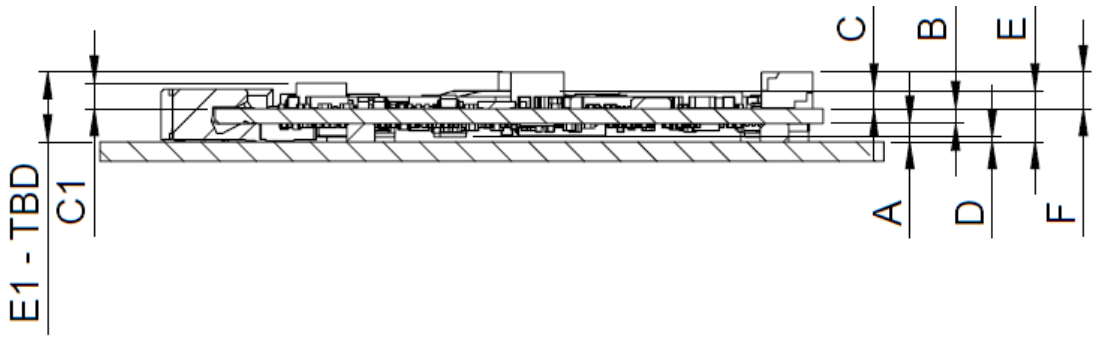

Figure 24: TQMa8MPxS dimensions, side view

Table 14: TQMa8MPxS heights

Dim.	Value	Tolerance	Remark
A	1.55 mm	±0.15 mm	Board to TQMa8MPxS distance[1,2]
B	1.172 mm	±0.117 mm	PCB thickness
C	1.43 mm	±0.16 mm	Processor height
C1	2.07 mm	±0.10 mm	Inductors height
D	0.535 mm	±0.16 mm	Space below module[1]
E	4.15 mm	±0.25 mm	Overall height to processor surface[1]
E1	TBD	TBD	Overall height to heatspreader[1]
F	3.02	±0.05 mm	JTAG connector (optional) height

[1]Tolerance defined by connector. Screw fastening not considered.

[2]Height based on connector low profile version; other heights possible by choosing connector type.

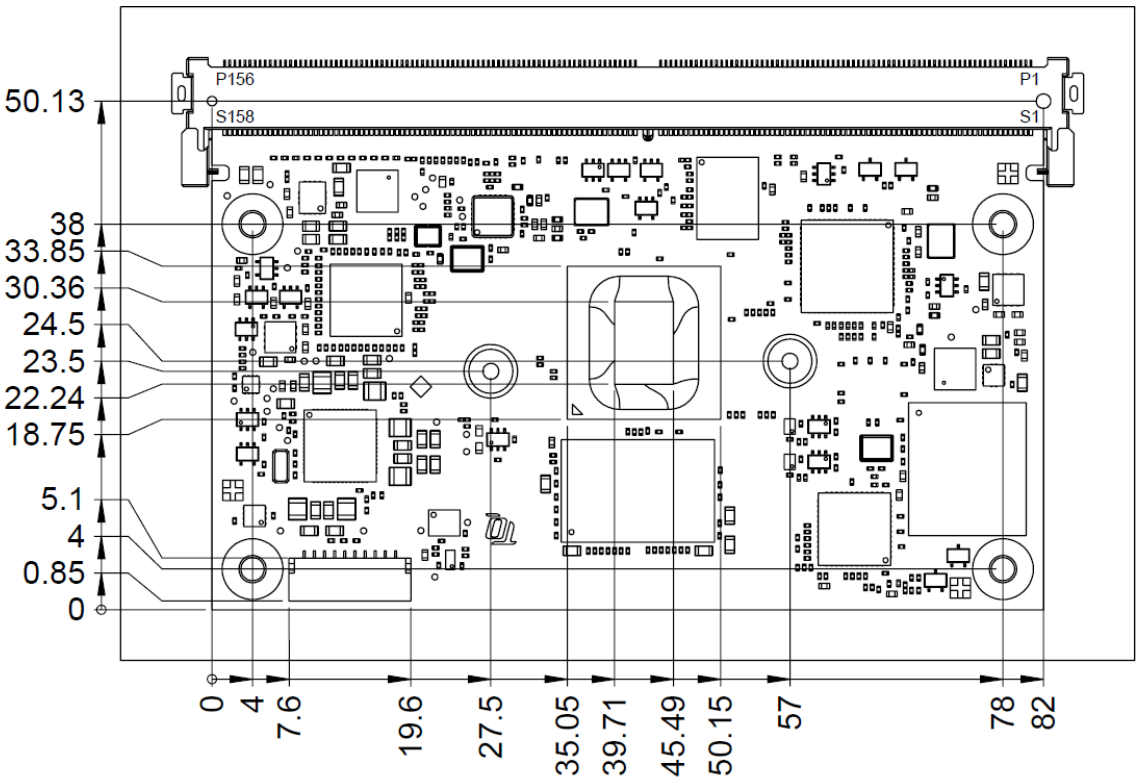

Figure 25: TQMa8MPxS dimensions (without heatspreader)

5.2 Component placement

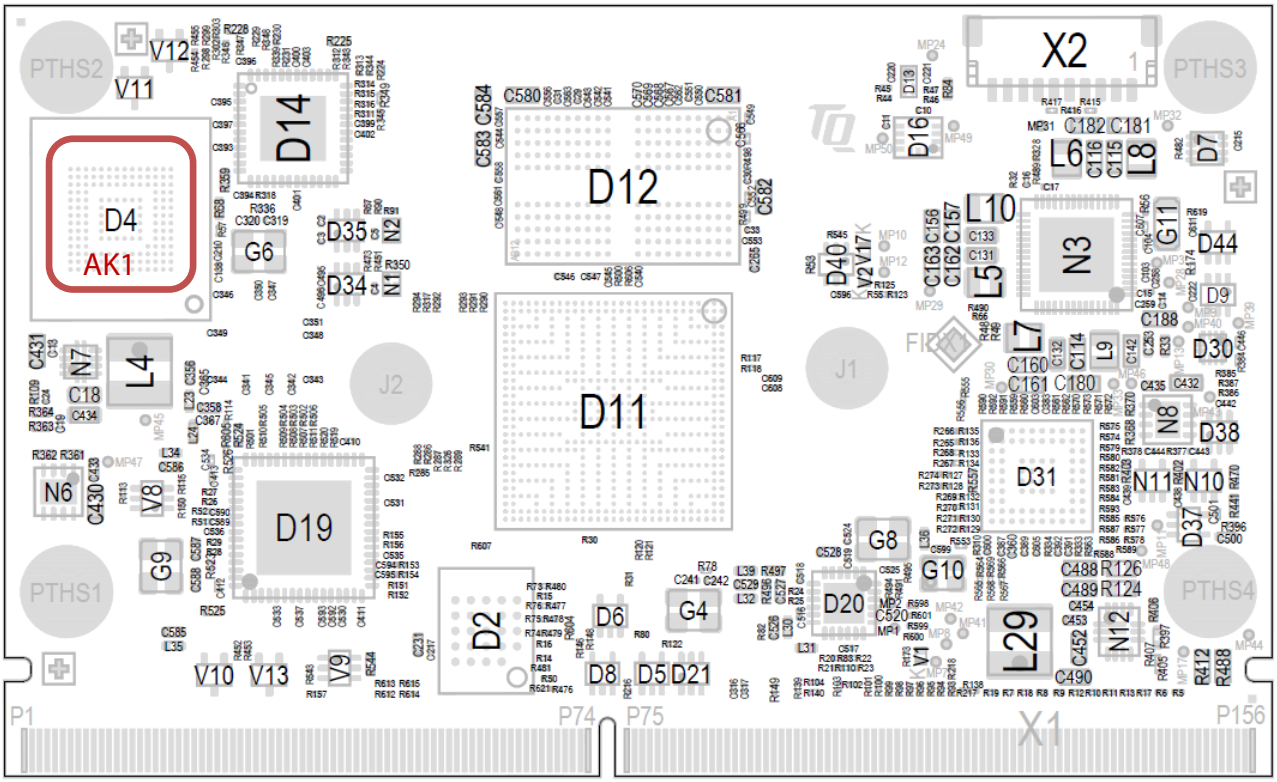

Figure 26: TQMa8MPxS, component placement top

The label AK1 on the TQMa8MPxS has the following information: MAC address, TQMa95xxSA version and revision, serial number

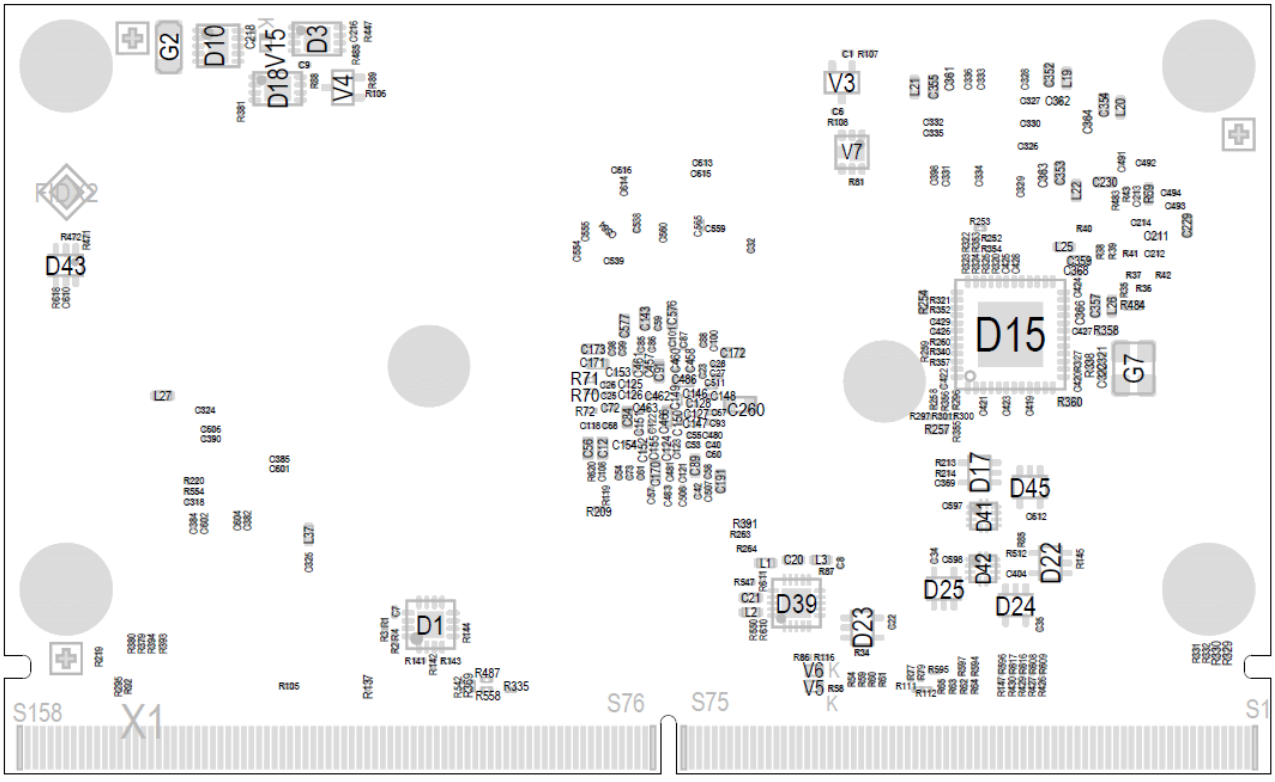

Figure 27: TQMa8MPxS, bottom view

5.3 Adaptation to the environment

The TQMa8MPxS has overall dimensions (length × width) of 82 mm × 50 mm (± 0,1 mm).
The TQMa8MPxS has a maximum height (heatspreader) above the carrier board of approximately TBD mm.
The TQMa8MPxS has 314 SMARC pins.
The TQMa8MPxS weighs approximately 20 g.

5.4 Protection against external effects

The TQMa8MPxS does not provide protection against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

To cool the TQMa8MPxS, note Table 12. The power dissipation originates primarily in the i.MX 8M Plus, the LPDDR4 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (6) and (7) for further information.

Attention: Destruction or malfunction, TQMa8MPxS cooling	
	The i.MX 8M Plus belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M Plus must be taken into consideration when connecting the heat sink, see (6). The i.MX 8M Plus is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MPxS and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMa8MPxS has a low retention force and has to be mounted / secured according to customer requirements.
The superior system is defined by the customer depending on the usage of the TQMa8MPxS.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa8MPxS was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa8MPxS.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Climate and operational conditions

The TQMa8MPxS is available in two different variants (Standard and Extended) with different temperature ranges. The operating temperature range for the TQMa8MPxS strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa8MPxS.

In general, a reliable operation is given when following conditions are met:

Table 15: Climate and operational conditions

Parameter		Range	Remark
Temperature range	Standard	–25 °C to 85 °C	–
	Extended	–40 °C to 85 °C	–
Storage temperature TQMa8MPxS		–40 °C to 100 °C	–
Relative humidity (operating / storage)		10 % to 90 %	Not condensing
IP code		IP00	

Detailed information concerning the i.MX 8M Plus thermal characteristics is to be taken from NXP documents (6) and (7).

Attention: Destruction or malfunction, TQMa8MPxS cooling	
	The i.MX 8M Plus belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8M Plus must be taken into consideration when connecting the heat sink, see (6). The i.MX 8M Plus is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8MPxS and thus malfunction, deterioration or destruction.

6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa8MPxS is only a sub-component of an overall system.

6.5 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.6 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.7 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.8 Reliability and service life

The MTBF calculated for the TQMa8MPxS is 681,662 hours with a constant error rate @ +40 °C, Ground Benign.

The TQMa8MPxS is designed to be insensitive to shock and vibration.

The TQMa8MPxS must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.

Detailed information concerning the i.MX 8M Plus service life under different operational conditions is to be taken from the NXP Application Note (7).

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa8MPxS is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMa8MPxS was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7.5 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa8MPxS always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa8MPxS on account of available Standby or Sleep-Modes of the components on the TQMa8MPxS.

7.6 Battery

No batteries are assembled on the TQMa8MPxS.

7.7 Packaging

The TQMa8MPxS is delivered in reusable packaging.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa8MPxS, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa8MPxS is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

There is no use of capacitors or transformers containing polychlorinated biphenyls (PCBs).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)

- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 16: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CAN-FD	CAN with Flexible Data-Rate
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DDR	Double Data Rate
DIN	Deutsche Industrienorm (German industry standard)
DNC	Do Not Connect
DSI	Display Serial Interface
EARC	Enhanced Audio Return Channel
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
Gbps	Gigabit per second
GPIO	General Purpose Input/Output
GPT	General-Purpose Timer
HDMI	High-Definition Multimedia Interface
I	Input
I/O	Input/Output
I2C	Inter-Integrated Circuit
IP00	Ingress Protection 00
IPU	Input with Pull-Up
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LGA	Land Grid Array
LPDDR4	Low Power DDR4
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
ML/AI	Machine Learning / Artificial Intelligence
MMC	Multimedia Card
MTBF	Mean operating Time Between Failures

8.1 Acronyms and definitions (continued)

Table 16: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
O	Output
OD	Open Drain
OOD	Output with Open Drain
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PD	Pull-down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protection
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TBD	To Be Determined
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 17: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 8M Plus Applications Processor Reference Manual	Rev. 3, Aug 2024	NXP
(2)	i.MX 8M Plus Applications Processors Data Sheet for Industrial Products	Rev. 2.2, Sep 2024	NXP
(3)	i.MX 8M Plus Hardware Developer's Guide	Rev. 1, Mar 2024	NXP
(4)	PMIC PCA9450 Data Sheet	Rev 2.3, Jul 2024	NXP
(5)	i.MX 8M Plus Mask Set Errata for Mask 1P33A	Rev. 2.1, Oct 2024	NXP
(6)	i.MX 8M Plus Power Consumption Measurement, AN12410	Rev. 0, 14 Apr 2019	NXP
(7)	i.MX 8M Plus Product Lifetime Usage, AN12468	Rev.0, 23 Jun 2019	NXP
(8)	SE050 Trust Secure Element Data Sheet	Rev. 3.8, Oct 2023	NXP
(9)	MB-SMARC-2 User's Manual	– current –	TQ-Systems
(10)	TQMa8MPxS Support-Wiki	– current –	TQ-Systems
(11)	TQMa8MPxS Processing instructions	– current –	TQ-Systems

TQ-Systems GmbH
Mühlstraße 2 I Gut Delling I 82229 Seefeld
Info@TQ-Group | TQ-Group

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