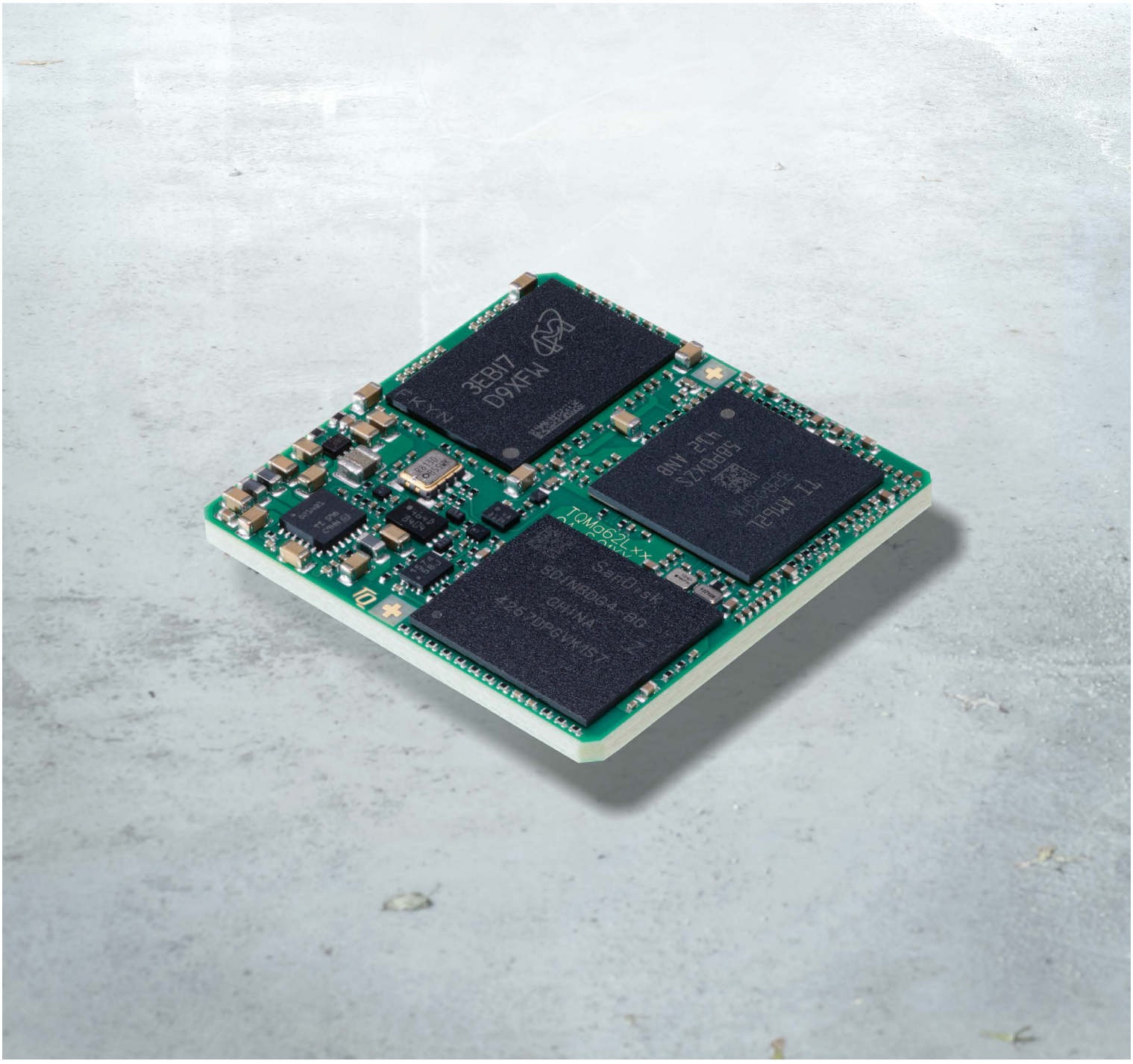
TQMa62LxxOA-S
Preliminary User's Manual

TQMa62LxxOA-S UM 0001
25.08.2026



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Rev.	Date	Name	Pos.	Modification
0001	25.08.2026	M. Kreuzer	All	Initial release

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive devices and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa62LxxOA-S and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you power up the TQMa62LxxOA-S or the Starterkit, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manuals of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa62xx circuit diagram
- MBa62xx Preliminary User's Manual
- Sitara™ AM62Lx Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- TQ-Support Wiki: support.tq-group.com/doku.php?id=en:arm:tqma62lxxoa

2. BRIEF DESCRIPTION

The TQMa62LxxOA-S is a universal OSM module from TQ based on the TI Sitara family AM62Lx with ARM Cortex A53 cores.

This Preliminary User's Manual describes the hardware of the TQMa62LxxOA-S Rev.010x and refers to some software settings. It does not replace the AM62Lx Reference Manual (2).

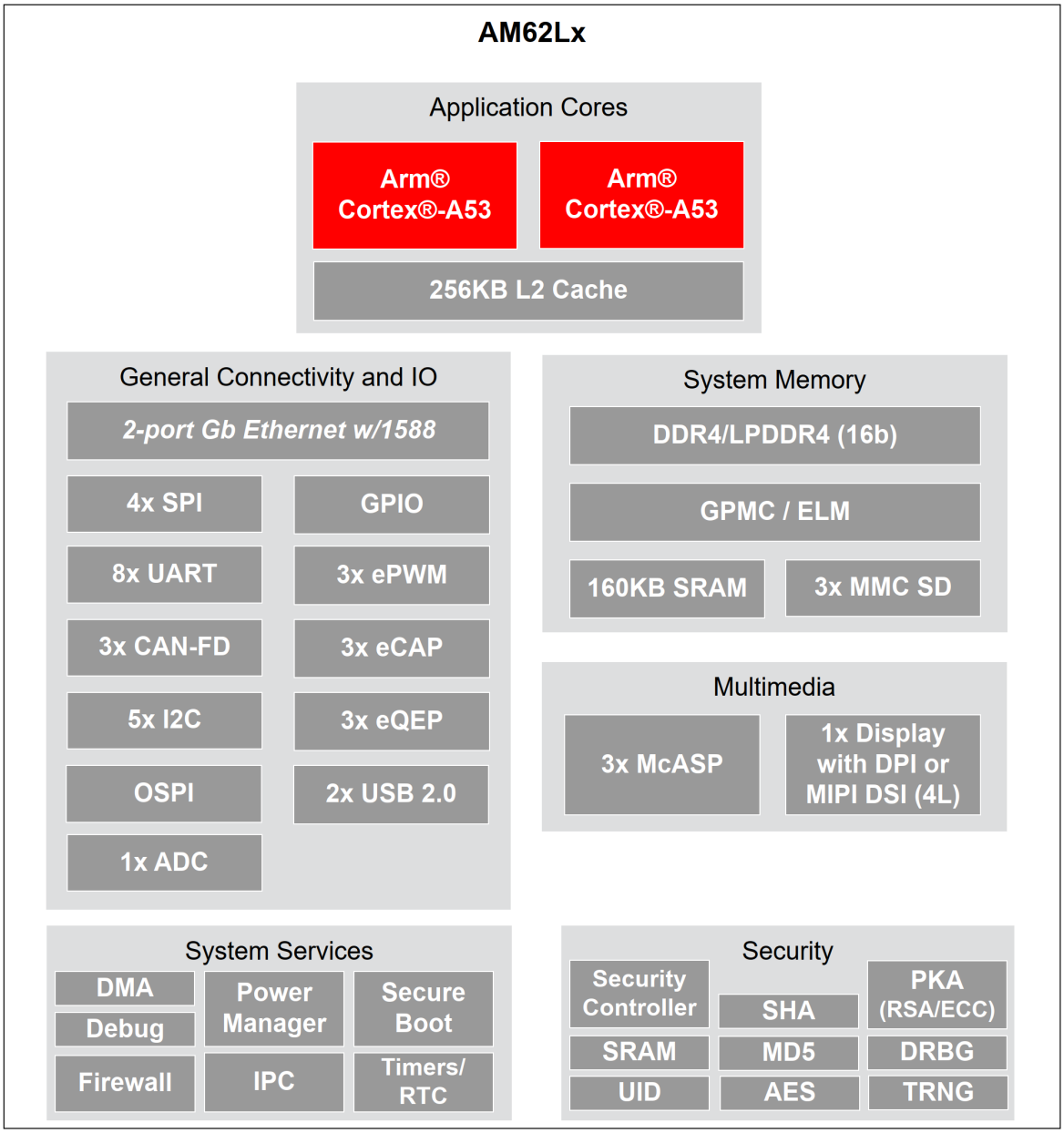

Figure 1: Block diagram AM62Lx

(Source: Texas Instruments)

All useful AM62Lx signals are routed to the TQMa62LxxOA-S LGA pads. There are no restrictions for customers using the TQMa62LxxOA-S with respect to an integrated customised design.

Please take note of that not all interfaces can be used simultaneously.

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa62LxxOA-S, and the BSP provided by TQ-Systems GmbH, see also section 4.

3.1 System overview

3.1.1 System architecture / block diagram

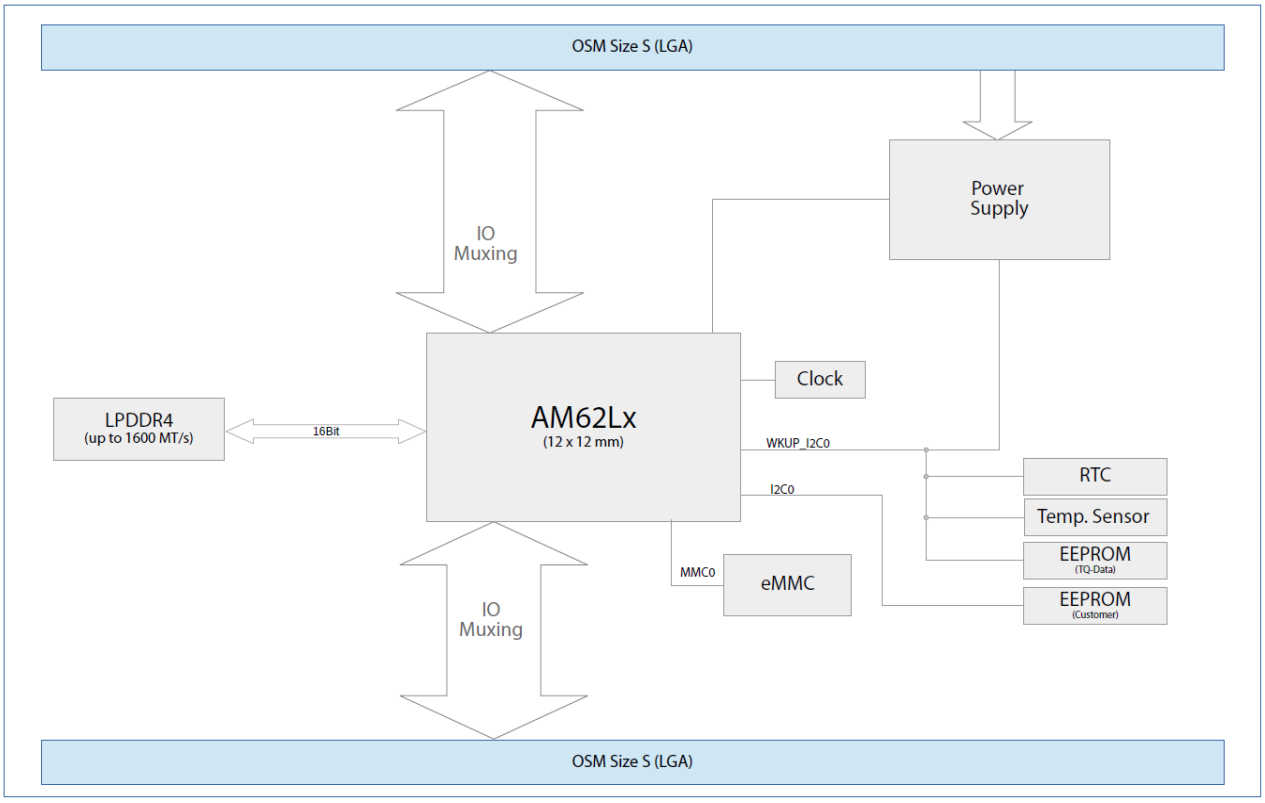

Figure 2: Block diagram TQMa62LxxOA-S

3.1.2 Functionality

The following key functions are implemented on the TQMa62LxxOA-S:

- OSM S module (30 mm x 30 mm)
- AM62Lx processor (up to 2 x A53 Cores)
- Up to 2 GB LPDDR4 memory with optional in-line ECC
- Up to 128 GB eMMC NAND-Flash 5.1 (default: 8 GB)
- Up to 64 kBit EEPROM (optional)
- 2kBit EEPROM (TQ-Data)
- Clock supply
- Real-time clock (optional)
- Temperature sensor (optional)
- Supervisor
- Availability of all essential signals of the processor at the 322 LGA pads of the OSM-S form factor
- Single Power Supply 5 V

3.1.3 Pin multiplexing

The pin multiplexing of the AM62Lx permits to use many pins for different interfaces.
The information provided in this Preliminary User's Manual is based on the BSP provided by TQ-Systems GmbH.

Attention: Destruction or malfunction	
	Many AM62Lx pins can be configured as different function. Please take note of the information in the AM62Lx data sheet (1) concerning the configuration of these pins before integration / start-up of your carrier board / Starter kit. Please also take note of the latest AM62Lx errata (3).

3.2 System components

3.2.1 Processor derivatives

Depending on the TQMa62LxxOA-S version, one of the following AM62Lx derivatives is assembled:
AM62L32 / AM62L31

Table 2: AM62Lx derivatives

Features	Reference Name	AM62L32	AM62L31
Arm Cortex-A53 Microprocessor Subsystem	A53SS	Dual Core	Single Core
Security Controller	Security Controller	Yes	
Crypto Accelerators	Security	Yes	
On-Chip Shared Memory (RAM)	OCSRAM in MAIN Domain	96 KB	
	OCSRAM in WKUP Domain	64 KB	
DDR Subsystem	DDRSS with DDR4	16-bit data; up to 4 GB	
	DDRSS with LPDDR4	16-bit data; up to 2 GB	
General-Purpose Memory Controller	GPMC	16-bit (GPMC, Raw NAND, Muxed-NOR)	
Display Subsystem	DSS	1 x DPI	
		1 x DSI	
Modular Controller Area Network with Full CAN-FD Support	MCAN	3	
General-Purpose I/O	GPIO	133	
Inter-Integrated Circuit Interface	I2C	5	
Analog-to-Digital Converter	ADC	Yes	
Multichannel Audio Serial Port	MCASP	3 (4/6/16 bits)	
Multichannel Serial Peripheral Interface	MCSPI	4	
Multi-Media Card/Secure Digital Interface	MMC/SD	1 x eMMC (8 bits)	
		2 x SD/SDIO (4 bits)	
Flash Subsystem (FSS)(2)	OSPI/QSPI	Yes	
Gigabit Ethernet Interface	CPSW3G	Yes	
General-Purpose Timers	TIMER	6	
Global Timer Counter	GTC	1	
Real Time Clock	RTC	Yes	
Enhanced Pulse-Width Modulator Module	EPWM	3	
Enhanced Capture Module	ECAP	3	
Enhanced Quadrature Encoder Pulse Module	EQEP	3	
Universal Asynchronous Receiver and Transmitter	UART	8	
USB2.0 Controller with PHY	USB 2.0	2	

3.2.2 Booting

3.2.2.1 Boot source

The boot source is selected via the boot strapping pins of the AM62Lx. The signals are directly routed to the module connectors and will be available again as GPIO after reading the boot configuration.

After the release of RESET_IN# (PORz) the boot configuration is read in at the BOOTMODE[15:0] pins. Independent of the boot device, the ROM bootloader is executed first, which assists in reading and executing the application code. The data can be read and loaded either directly from the memory device or by a peripheral.

The following figure shows the implementation of boot strapping on the module:

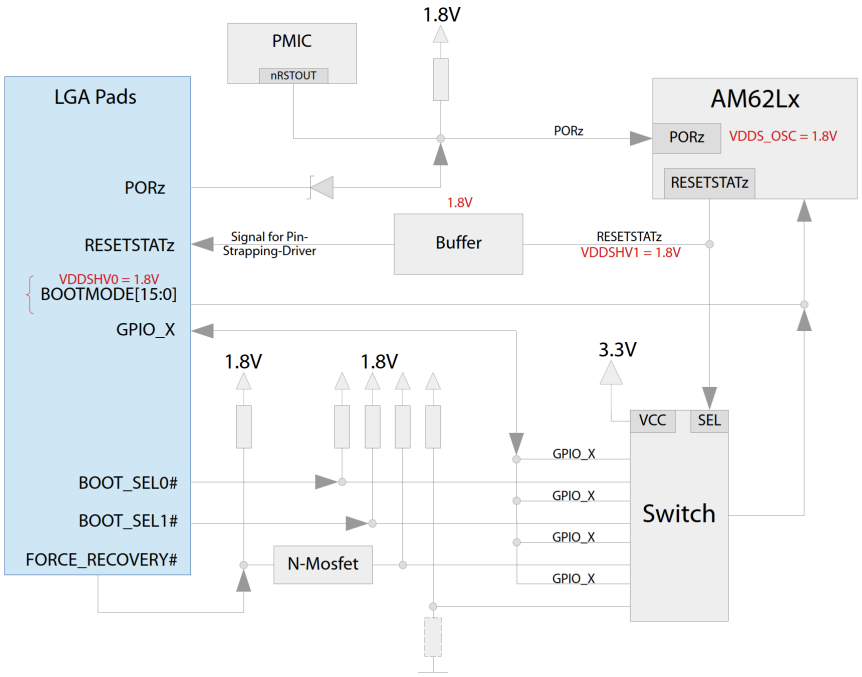

Figure 3: Block diagram boot strapping

According to the Reference Manual (2) the general boot configuration of the AM62Lx supports two different BOOTMODE pin mapping options:

- Reduced Pincount - Using only 4 of the bootstrap pins BOOTMODE[15:12]
- Full Pincount - Using all 16 of the bootstrap pins BOOTMODE[15:0].

Table 3: Boot-Strapping Reduced vs Full

BOOTMODE[15:14]	Bootmode Mapping
00	Full Pincount
01, 10, or 11	Reduced Pincount

The Reduced Pincount option is implemented in hardware and is transparent to the ROM code. Its implementation is a lookup table that uses four pins to select from either the Full Pincount option, or a set of commonly used boot modes selected as Reduced Pincount options. The selection determines what value is loaded into the Device Status register WKUP_CTRL_MMR_CFG1_DEVSTAT[15:0] on a POR.

Table 4: Selecting the General Boot Configuration of the Reduced Pincount

Boot configuration pin	Configuration	TQMa62LxxOA-S
BOOTMODE[15]	Reserved, fixed to 1 via Pullup on module	1
BOOTMODE[14]	via FORCE_RECOVERY# (Pullup on module)	0
BOOTMODE[13]	Signal BOOT_SEL1# (Pullup on module)	1
BOOTMODE[12]	Signal BOOT_SEL0# (Pullup on module)	1

All of the Reduced Pincount options are expanded to a full 16-bit option by a lookup table and the expanded 16-bit value is loaded into the Device Status register.

Table 5: Lookup table of the Reduced Pincount

PIN VALUE BOOTMODE				WKUP_CTRL_MMR_CFG1_DEVSTAT[15:0] VALUEROM USES		
15	14	13	12	Source	Primary	Backup
0	0	x	x	Selects the Full Pincount option, BOOTMODE[15:0] input buffers are enabled and all pins are captured in WKUP_CTRL_MMR_CFG1_DEVSTAT[15:0] on POR.		
0	1	0	0	Reserved for future definition, Do Not Use		
0	1	0	1	Reserved for future definition, Do Not Use		
0	1	1	0	Efuse Bootmode1	DEVBOOT	None
0	1	1	1	Efuse Bootmode2	USB0 Host MSC	UART
1	0	0	0	Fixed 1	MMC0 eMMC Boot Partition	USB DFU
1	0	0	1	Fixed 2	FSS0 QSPI CS0	UART
1	0	1	0	Fixed 3	MMC1 4 BIT UDA Filesystem	UART
1	0	1	1	Fixed 4	MMC0 eMMC Boot Partition	MMC1
1	1	0	0	Fixed 5	FSS0 Serial NAND OSPI 1-1-4	UART
1	1	0	1	Fixed 6	FSS0 xSPI SFDP Enabled (Discoverable)	UART
1	1	1	0	Fixed 7	EXT. HOST UART0	MMC1
1	1	1	1	Fixed 8	EXT. HOST USB0 DFU	MMC1

Attention: Malfunction

When the Full Pincount bootmode option is selected, all BOOTMODE[15:0] pins must be pulled up or down. They must not be left floating. When the Reduced Pincount option is selected, this applies only to BOOTMODE[15:12] pins.

3.2.2.2 Boot device eMMc

Table 6: Boot device selection eMMC

Boot configuration pin	Setting	TQMa62LxxOA-S
BOOTMODE[14]	FORCE_RECOVERY# This bit should be left open	000
BOOTMODE[13]	0	
BOOTMODE[12]	0	

3.2.2.3 FORCE_RECOVERY#

Table 7: Selection of the FORCE_RECOVERY# Boot-Mode

Boot configuration pin	Setting	TQMa62LxxOA-S
BOOTMODE[14]	FORCE_RECOVERY# This bit must be LOW	111
BOOTMODE[13]	1	
BOOTMODE[12]	1	

Further boot configurations can be found in the Reference Manual (2).

Besides the mentioned boot configurations above, it is recommended to consider an alternative boot source during development, e.g. USB boot.

Note: Update

When designing a mainboard, it is recommended to plan a redundant update concept for software updates in the field. Furthermore, it is recommended to switch the conversion of the boot strap pins to high impedance after reading in.

3.2.3 Memory

3.2.3.1 LPDDR4 SDRAM

The TQMa62LxxOA-S has a LPDDR4 memory with the use of in-line ECC:

- 16-bit bus width with optional ECC (8-bit data + 8-bit ECC)
- Up to 1600 Mbps = 800 MHz
- 1 GByte (=8 Gbit) / 1.5 GByte (=12 Gbit) / 2 GByte (=16 Gbit)

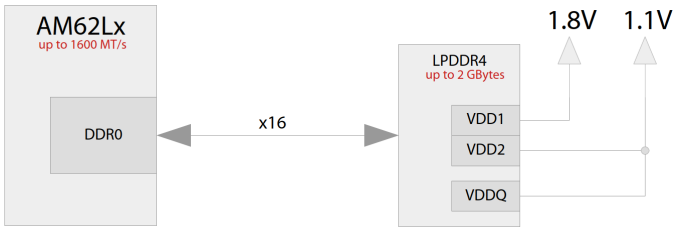

Figure 4: Block diagram LPDDR4 interface

3.2.3.2 eMMC

An eMMC is available to the TQMa62LxxOA-S as non-volatile data memory for programs and data (e.g. boot loader, operating system). The used MMC0 signals are not available to the Pinout.

- MMC0 Interface is connected to the eMMC Flash
- 8 / 16 / 32 / 64 / 128 GByte

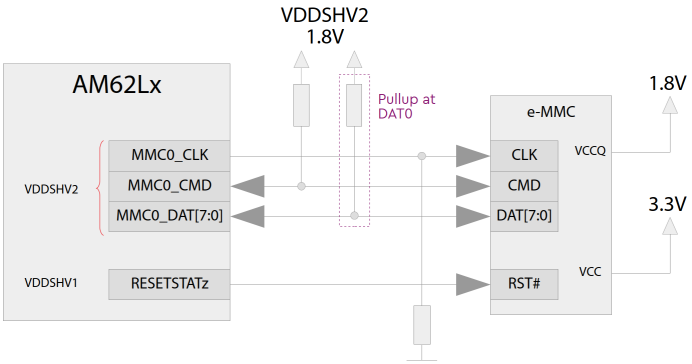

Figure 5: Block diagram eMMC flash interface

The TQMa62LxxOA-S supports the following transmission modes:

Table 8: eMMC Flash modes

Mode	1-bit	4-bit	8-bit	Note
Default Speed	n/a	n/a	n/a	
High Speed	n/a	n/a	Yes	Boot process
HS200	n/a	n/a	Yes	U-boot / Linux (default)

3.2.3.3 EEPROMs

I²C EEPROMs are provided on the TQMa62LxxOA-S for non-volatile storage. A distinction is made here between:

- Customer data, freely accessible
- TQ manufacturing data (Serial Number, MAC, ...)

All I²C slave address and bus structure are summarized in chapter 3.2.8.3.

3.2.4 Clock supply

The clock supply of the TQMa62LxxOA-S is represented as follows:

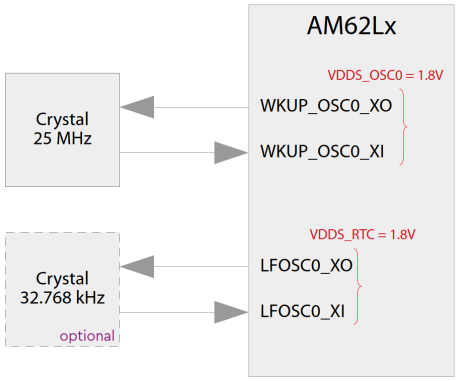

Figure 6: Block diagram clock supply

To get the OSM module executable only with a 5 V supply, LFOSC_XO / XI and WKUP_OSC0_XO / XI were implemented as clock on the module. The remaining clock inputs can either be derived from the system clock or fed externally via the module connectors, as an example the following clocks can be fed externally:

- EXT_REFCLK1
- WKUP_EXT_REFCLK0
- AUDIO_EXT_REFCLK0/1
- …

Further information can be obtained from the associated data sheets (1).

3.2.5 RTC

An optional RTC (Epson RX8130CE) can be equipped on the TQMa62LxxOA-S. The connection is realized as follows:

- The RTC can be supplied from the base board via V_RTC_IN. V_RTC_IN = 2.0 V to 5.5V
- RTC_INT# is accessible at the module pad AA2.
- I2C is connected via WKUP_I2C0 (I^2C addresses are described in chapter 3.2.8.3)

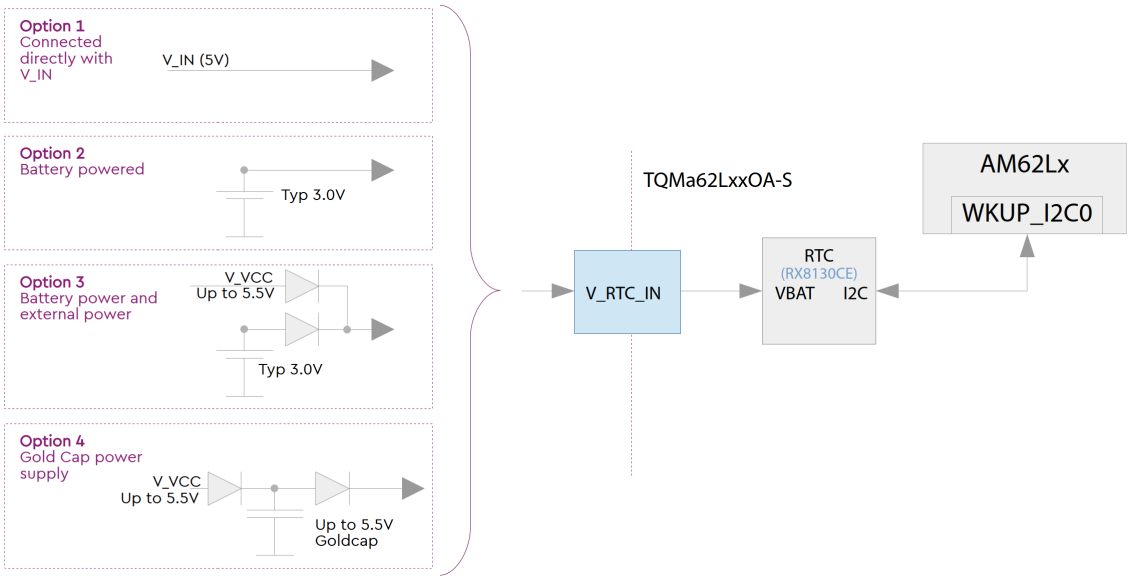

Figure 7: Block diagram RTC

Note: Equipping the base board	
	The RTC is supplied directly via V_RTC_IN. This allows the user an easy use of Gold-Caps or coin cells on the mainboard.

3.2.6 Temperature sensor

A temperature sensor (TI TMP110D0IDPWR) is placed on the TQMa62LxxOA-S to monitor the module temperature.
The over temperature output (TEMP_ALERT) of the sensor is available at the module pad AA13 as an open drain output.
The I²C addresses are described in chapter 3.2.8.3.

3.2.7 Interfaces

In general, except for the memory connection, all IO pins of the processor are provided at the module connectors.
For further information about the interfaces and the pin multiplexing refer to the Processor Reference Manual (2).

3.2.7.1 GPIO

Besides their interface function, most AM62Lx pins can also be used as GPIOs. Details are to be taken from the AM62Lx Data Sheet (1).

3.2.7.2 I²Cs (I2C0, WKUP_I2C0)

The accessible I²C buses depend on the pin multiplexing. To use the internal I²C devices, the WKUP_I2C0 bus is permanently provided on the TQMa62LxxOA-S. The following devices are connected to the module:

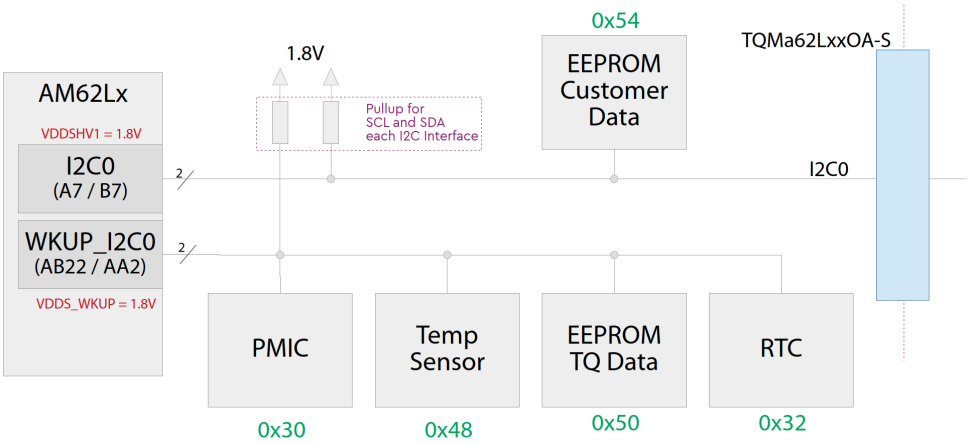

Figure 8: Block diagram I2C bus on the TQMa62LxxOA-S

Table 9: I2C address assignment on the module

Bus	Component	Address	Note
WKUP_I2C0	Temperature sensor TMP110D0	0x48 / 0b100 1000	Optional
	EEPROM M24C02	0x50 / 0b101 0000	TQ-Data
	RTC RX8130CE	0x32 / 0b011 0010	Optional
	PMIC TPS65214	0x30 / 0b011 0000	
I2C0	EEPROM M24C64	0x54 / 0b101 0100	Customer EEPROM (optional)

3.2.8 Reset

The following figure describes the implementation of the reset structure of the TQMa62LxxOA-S:

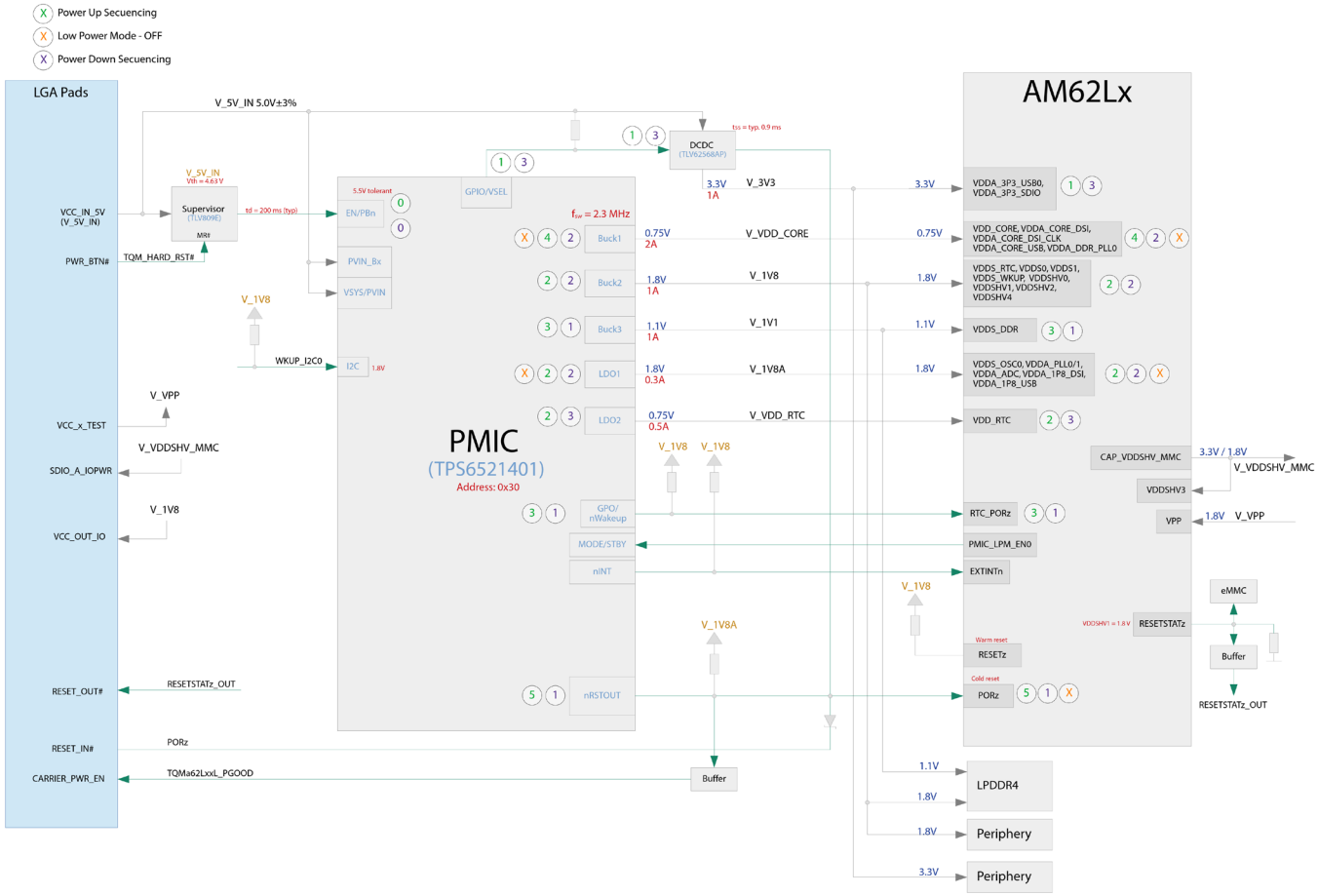

Figure 9: Block diagram Reset

3.2.8.1 Reset Options (Input)

3.2.8.1.1 TQM_HARD_RST# (PWR_BTN#)

The input signal TQM_HARD_RST# is used to control the entire module. Coming from the module pad a reset with power cycle of the module is executed. As soon as the signal becomes HIGH, the power-up sequencing takes place after a delay of approx. 200 ms.

Per default the signal is connected with a pullup to V_5V_IN (5 V), therefore only a LOW can reset the module with power cycle.

3.2.8.1.2 PORz (RESET_IN#)

The RESET_IN# signal is used to trigger a cold reset. A Schottky diode and a PMIC are connected between the RESET_IN# signal and PORz; the PMIC holds the signal at LOW during power sequencing and then switches it to HIGH.
By default, the PORz signal is connected to a pull-up to 1.8V (V_1V8A), so only a LOW level can trigger a cold reset on the module. The status of PORz is buffered and visible via the TQMa62LxxL_PGOOD signal.

3.2.8.1.3 EXT_WAKEUP0/1

The input signal is used to control the RTC mode. A signal is sent from the LGA balls to the processor (EXT_WAKEUP0/1).
There is no pull-up or pull-down resistor on the OSM module; the customer must provide one on the motherboard/base board.

3.2.8.2 Reset Status (Output)

3.2.8.2.1 RESETSTATz (RESET_OUT#)

The RESETSTATz signal serves as a status signal for a warm reset of the main domain.
By default, the signal is connected to ground via a pull-down resistor.

3.2.8.3 Control signals

3.2.8.3.1 TQMa62LxxL_PGOOD

TQMa62LxxL_PGOOD serves as a status signal to the base board that the voltages on the mainboard can now be switched on. Power GOOD (PGOOD) is only active when the power sequencing on the module has been successfully completed.

3.2.9 Power supply

3.2.9.1 Overview TQMa62LxxOA-S supply

The main supply of the TQMa62LxxOA-S is defined to typ. 5 V ± 5 %. By applying the 5 V voltage the module generates all required voltages.
The following table shows all relevant supply voltages of the TQMa62LxxOA-S.

Table 10: Supply voltages

Module pin / Signal	Voltage	Current	Use
V_5V_IN (VCC_5V_IN)	4.75…5.25 V	see Table 13	Input: module supply
V_3V3 (VCC_2_TEST)	3.289…3.366 V	max. 100 mA	Output
V_1V8 (VCC_OUT_IO)	1.746…1.854 V	max. 100 mA	Output
V_VDDSHV_MMC (SDIO_A_IOPWR)	1.8 V / 3.3 V	< 20 mA	Output: MMC1 IO-Bank supply
V_1V8 / (SDIO_B_IOPWR)	1.8 V	max. 100 mA	Output: MMC2 IO-Bank supply
V_RTC_IN (RTC_PWR)	2.0…5.5 V	see 3.2.5	Input: supply for module RTC
V_VPP (Ball B22)	1.8 V	max. 400 mA	Input: supply for eFuse programming
USB0_VBUS	typ. 5 V	< 1 mA	Input: Used to detect the USB-VBUS voltage and is usually supplied with the VBUS voltage switched by the USB host. External circuitry is required – see (2).
USB1_VBUS			

Attention: Malfunction	
	If the absolute maximum voltages of the processor are exceeded, malfunctions and component failures may occur. The mentioned outputs may not be supplied externally under any circumstances.

3.2.9.2 Power sequencing

After switching on the module supply V_5V_IN and TQM_HARD_RST# to HIGH the power-up sequence starts. With completion of the power sequencing the supply of the external mainboard components is signaled via TQM62LxxL_PGOOD (CARRIER_PWR_EN). The following figure shows the chronological sequence of the signals involved.

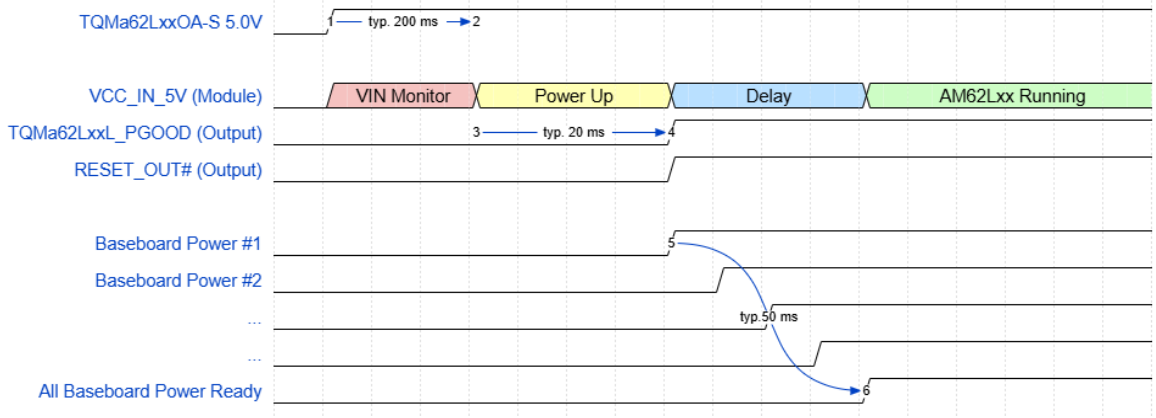

Figure 10: Recommended power up sequence

Attention: Malfunction	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence is completed. The end of the power-up sequence is signaled by a high level of the TQMa62LxxL_PGOOD signal.

3.2.9.3 Power modes

The TQMa62LxxOA-S has the following power modes:

- Active Mode - The module is powered and everything is active.

Depending of the processor, the following low power modes can be provided:

- Deep Sleep Mode
  - Module is completely powered
  - All power domains that can be switched off can be turned off
  - HFOSC0 is OFF
  - DDR interface in self-refresh
- RTC only + IO +DDR
  - The SoC is OFF except for RTC, IO, and DDR.
  - DDR in self-refresh mode is specified in IDD6; typical current consumption at an ambient temperature of 25 °C is approximately 0.4 mA … 2.7 mA
- Standby
  - Module is completely supplied
  - State change: triggered by every SOC interrupt
  - DDR interface in self-refresh

More information can be found in the AM62Lx Reference Manual (2).

Independent of the processor, the following low power modes can be provided:

- I2C-RTC Mode
  - The module is no longer powered via V_5V_IN
  - Only the RTC remains powered and active
  - The current consumption is then determined solely by the RTC's current consumption and is typically in the range of 300 nA (backup mode)

3.2.9.4 Power consumption

The following table lists some technical parameters of the module supply. The specified current consumptions are to be regarded as a guide value. Since the current consumption of the TQMa62LxxOA-S can differ greatly depending on the application, modes and operating system, the values listed here should only be used for a performance estimate.

Table 11: Current consumption TQMa62LxxOA-S

TQMa62L32OA-S (1 Gbit LPDDR4, 8 GByte eMMC-Flash)		
Current consumption Power OFF	TBD mA	TQM_HARD_RST# = LOW
Current consumption Reset mode	TBD mA	RESET_IN# = LOW
Current consumption RTC + IO + DDR	TBD mA	RTC + IO + DDR Mode
Current consumption theoretical worst case	1.15 A	Current consumption @ 5 V
Current consumption U-Boot prompt	TBD mA	U-Boot Idle
Current consumption Linux prompt	TBD mA	Linux Idle
Current consumption Linux (stressapptest -W -s 31536000 -M 256 -m 2 -C 2 -i 2 stress-ng --cpu-load 100 --cpu 2 --timeout 31536000)	TBD mA	Higher current consumption must be expected when using additional interfaces in parallel

3.3 TQMa62LxxOA-S interface

3.3.1 Pin assignment

The TQMa62LxxOA-S has a total of 322 LGA pads. By using the OSM-S design, the module is soldered on once and thus has a permanent, stable connection to its peripherals. Removing the module from its soldered-on position is not possible without further ado, is not recommended and can lead to a reduction in service life or to its destruction.

The electrical and pin characteristics are to be taken from the AM62Lx datasheet / manual (1)(2)

Attention: Destruction or malfunction	
	The multiple pin configurations of all AM62Lx internal function units must be taken note of. The pin assignment shown in Figure 15 refers to the corresponding BSP provided by TQ-Systems GmbH. Table 12 shows all pin multiplexing options.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A		CSI_A_DATA1_N	CSI_A_DATA1_P	GND	CSI_A_DATA2_N	CSI_A_DATA2_P	GND	USB_C_SSTX_P	USB_C_SSTX_N	GND				UART_A_RX	COM_AREA_01	COM_AREA_02	COM_AREA_03	COM_AREA_04	COM_AREA_05	COM_AREA_06	COM_AREA_07	UART_C_RX	
B	CSI_A_DATA0_P	GND	CSI_A_CLOCK_N	CSI_A_CLOCK_P	GND	CSI_A_DATA3_N	CSI_A_DATA3_P	GND	GND	USB_C_SSRX_P	USB_C_SSRX_N		UART_A_TX		COM_AREA_08	COM_AREA_09	COM_AREA_10	COM_AREA_11	COM_AREA_12	COM_AREA_13	COM_AREA_14	Vendor Defined	UART_C_TX
C	CSI_A_DATA0_N	CAM_MCK	CAM_A_SDA/ CSI_A_TX_N	CAM_A_SCL/ CSI_A_TX_P	VCC_6_TEST	ETH_B_MDC	ETH_B_MDIO	USB_C_OC#	USB_C_VBUS	USB_C_EN	GND		UART_A_RTS	UART_A_CTS	COM_AREA_15	Vendor Defined	COM_AREA_16	TEST_GENERIC	COM_AREA_17	SDIO_A_IOPWR	COM_AREA_18	UART_D_RX	UART_D_TX
D	GND	ETH_B_(R)(G)MII_CRS	GPIO_C_0	GPIO_C_1	GND	Vendor Defined	Vendor Defined	GND	USB_C_ID	USB_C_D_P	USB_C_D_N		UART_B_TX	UART_B_RX	UART_B_RTS	UART_B_CTS	GPIO_A_0	GND	GPIO_B_0	SDIO_A_WP	SDIO_A_PWR_EN	UART_CON_RX	UART_CON_TX
E	ETH_B_(R)(G)MII_COL	GND	GPIO_C_2/ CAM_B_PWR	GPIO_C_3/ CAM_B_RST#											GND	ETH_A_(R)(G)MII_CRS	GPIO_A_1	PWM_0/ DISP_BL_PWM	GPIO_B_1	SDIO_A_CMD	GND		
F	ETH_B_(S)(R)(G)MII_TXD1	ETH_B_(S)(R)(G)MII_TXD3	GPIO_C_4/ DISP_VDD_EN	GPIO_C_5/ DISP_BL_EN											ETH_A_(R)(G)MII_COL	GND	GPIO_A_2	PWM_1	GPIO_B_2	GND	SDIO_A_CLK		
G	ETH_B_(S)(R)(G)MII_TXD0	ETH_B_(S)(R)(G)MII_TXD2	GPIO_C_6/ CAM_A_PWR	GPIO_C_7/ CAM_A_RST#											ETH_A_(S)(R)(G)MII_TXD1	ETH_A_(S)(R)(G)MII_TXD3	GPIO_A_3	PWM_2	GPIO_B_3	SDIO_A_D0	SDIO_A_D1		
H	ETH_B_(R)(G)MII_TX_CLK	GND	RGB_CS#	GND											ETH_A_(S)(R)(G)MII_TXD0	ETH_A_(S)(R)(G)MII_TXD2	GPIO_A_4	PWM_3	GPIO_B_4	SDIO_A_D2	SDIO_A_D3		
J	ETH_B_(S)(R)(G)MII_RXD0	ETH_B_(R)(G)MII_TX_EN(_ER)	RGB_RESET#	RGB_DE											ETH_A_(R)(G)MII_TX_CLK	GND	GPIO_A_5	PWM_4	GPIO_B_5	GND	SDIO_A_CD#		
K	ETH_B_(S)(R)(G)MII_RXD1	ETH_B_(R)(G)MII_RX_ER	RGB_HSYNC	RGB_DISP											ETH_A_(S)(R)(G)MII_RXD0	ETH_A_(R)(G)MII_TX_EN(_ER)	GPIO_A_6/ SPI_A_CS1#	PWM_5	GPIO_B_6	SDIO_B_CLK	SDIO_B_CMD		
L	ETH_B_(R)(G)MII_RX_DV(_ER)	GND	RGB_VSYNC	GND											ETH_A_(S)(R)(G)MII_RXD1	ETH_A_(R)(G)MII_RX_ER	GPIO_A_7/ SPI_B_CS1#	GND	GPIO_B_7	SDIO_B_D0	SDIO_B_D1		
M	ETH_B_(R)(G)MII_RXD2	ETH_B_SDP	RGB_B5	RGB_(PIXEL)CLK											ETH_A_(R)(G)MII_RX_DV(_ER)	GND	ETH_IOPWR	ADC_0	VCC_2_TEST	GND	SDIO_B_D2		
N	ETH_B_(R)(G)MII_RXD3	RESERVED	RGB_B3	RGB_B4											ETH_A_(R)(G)MII_RXD2	ETH_A_SDP	JTAG_TCK(SWCLK)	ADC_1	JTAG_TMS(SWDIO)	SDIO_B_D3	SDIO_B_D4		
P	ETH_B_(R)(G)MII_RX_CLK	GND	RGB_B2	GND											ETH_A_(R)(G)MII_RXD3	Vendor Defined	JTAG_TDI	GND	JTAG_RTCK	SDIO_B_D5	SDIO_B_D6		
R	GND	PCIe_SM_ALERT#	RGB_B1	RGB_B0											ETH_A_(R)(G)MII_RX_CLK	GND	JTAG_TDO(SWO)	BOOT_SEL1#	JTAG_nTRST	GND	SDIO_B_D7		
T	PCIe_SMCLK	PCIe_WAKE#	RGB_G4	RGB_G5											ETH_MDIO	ETH_MDC	FORCE_RECOVERY#	I2S_B_LRCLK	I2S_B_BITCLK	SDIO_B_IOPWR	SDIO_B_CD#		
U	PCIe_SMDAT	GND	RGB_G3	GND											SPI_A_SDI_(IO1)	SPI_A_SCK	RESET_IN#	VCC_OUT_IO	BOOT_SEL0#	SDIO_B_WP	SDIO_B_PWR_EN		
V	GND	PCIe_A_PERST#	RGB_G1	RGB_G2											SPI_A_SDO_(IO0)	GND	Carrier_PWR_EN	I2S_MCLK	I2S_B_DATA_IN	GND	I2S_A_DATA_IN		
W	PCIe_REFCLK_P	PCIe_CLKREQ#	GND	RGB_G0											SPI_A_HOLD_(IO3)	SPI_A_WP_(IO2)	RTC_PWR	I2S_A_LRCLK	I2S_B_DATA_OUT	I2S_A_BITCLK	I2S_A_DATA_OUT		
Y	PCIe_REFCLK_N	GND	VCC_5_TEST	RGB_R5	RGB_R4	RGB_R2	RGB_R0	VCC_IN_5V	VCC_IN_5V	VCC_IN_5V	VCC_IN_5V		CARRIER_STBY#	RESET_OUT#	SPI_A_CS0#	VCC_3_TEST	VCC_IN_5V	GND	VCC_IN_3V3	VCC_4_TEST	SPI_B_SCK	SPI_B_SDI	SPI_B_SDO
AA	GND	RESERVED	DSI_TE	GND	RGB_R3	RGB_R1	GND	GND	PWR_BTN#	GND	GND		RESERVED	GND	I2C_A_SCL	I2C_A_SDA	GND	V_BAT	GND	I2C_B_SCL	I2C_B_SDA	GND	SPI_B_CS0#
AB	PCIe_A_HSI0_P	PCIe_A_HSI0_N	GND	DSI_DATA3_P / LVDS_A_LANE3_P	DSI_DATA3_N / LVDS_A_LANE3_N	GND	DSI_CLOCK_P / LVDS_A_CLK_P	DSI_CLOCK_N / LVDS_A_CLK_N	GND	DSI_DATA0_P / LVDS_A_LANE0_P	DSI_DATA0_N / LVDS_A_LANE0_N		USB_A_D_N	USB_A_ID	GND	USB_A_VBUS	CAN_A_RX	V_BAT	CAN_B_RX	USB_B_VBUS	GND	USB_B_ID	USB_B_D_N
AC		PCIe_A_HSO0_P	PCIe_A_HSO0_N	GND	DSI_DATA2_P / LVDS_A_LANE2_P	DSI_DATA2_N / LVDS_A_LANE2_N	GND	DSI_DATA1_P / LVDS_A_LANE1_P	DSI_DATA1_N / LVDS_A_LANE1_N	GND				USB_A_D_P	USB_A_OC#	USB_A_EN	CAN_A_TX	DEBUG_EN	CAN_B_TX	USB_B_EN	USB_B_OC#	USB_B_D_P	

Figure 11: TQMa62LxxOA-S – Pinout (top view)

3.3.2 Pinout TQMa62LxxOA-S

Table 12: Pinout

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
VCC_2_TEST	M19	V_3V3		Module power voltage testpoint	PO			Factory Test Only
VCC_3_TEST	Y16	V_VDD_CORE			PO			
VCC_4_TEST	Y20	V_1V1			PO			
VCC_IN_5V	Y17	V_5V_IN		Module power input voltage of 5 V - Primary voltage rail	P			Tolerance: 5 V +- 5%
VCC_IN_3V3	Y19	NC						
V_BAT	AA18, AB18	NC						
GND	D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21	DGND		Module signal and power return and GND reference	P			
RESET_IN#	U17	RESET_IN	AB18	Reset input from carrier board. Carrier drives low to force a module reset, floats the line otherwise	I OD CMOS	1.8 V	PU 1K	Connected to PORz
RESET_OUT#	Y14	RESETSTATz_OUT	C16	Reset output from CPU to reset peripherals on Carrier	O CMOS	1.8 V		Connected to RESETSTATz
CARRIER_PWR_EN	V17	TQMa62LxxL_PGOOD		Carrier board circuits should not be powered up until the module asserts the CARRIER_PWR_EN signal	O CMOS	1.8 V		
CARRIER_STBY#	Y13	NC						
VCC_OUT_IO	U18	V_1V8		Provides IO voltage level for several interfaces to connect	PO	1.8 V		max. current 100 mA
RTC_PWR	W17	V_RTC_IN		Low current RTC circuit backup power - 3.0 V nominal. May be sourced from a carrier based Lithium cell or Super Cap	P			2.0 V…5.5 V
BOOT_SEL0#	U19	BOOT_SEL0#		Boot select line 0	I OD CMOS	1.8 V	PU 10k	Reduced Pin Mapping BOOTMODE12
BOOT_SEL1#	R18	BOOT_SEL1#		Boot select line 1	I OD CMOS	1.8 V	PU 10k	Reduced Pin Mapping BOOTMODE13
FORCE_RECOVERY#	T17	FORCE_RECOVERY#		If low on carrier board module enters recovery mode	I OD CMOS	1.8 V	PU 10k	Reduced Pin Mapping BOOTMODE14
JTAG_TCK(SWCLK)	N17	TCK	AB14	Test Clock	I CMOS	1.8 V		
JTAG_TMS(SWDIO)	N19	TMS	Y17	Test Mode Select	I CMOS	1.8 V		
JTAG_TDI	P17	TDI	AC16	Test Data Input	I CMOS	1.8 V		
JTAG_RTCK	P19	NC						
JTAG_TDO(SWO)	R17	TDO	AB15	Test Data Output	O CMOS	1.8 V		
JTAG_nTRST	R19	TRST#	AB16	Test Reset, Active Low	I CMOS	1.8 V		
DEBUG_EN	AC18	NC						
TEST_GENERIC	C18	TQ_EEPROM_WC#		General purpose for testing	I/O CMOS	1.8 V		for testing only
UART_A_RX	A14	WKUP_UART0_RXD	Y22	Asynchronous serial data input port A	I CMOS	1.8 V		

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
UART_A_TX	B13	WKUP_UART0_TXD	AA23	Asynchronous serial data output port A	O CMOS	1.8 V		
UART_A_RTS	C13	WKUP_UART0_RTS#	W22	Request to Send handshake line for port A	O CMOS	1.8 V		
UART_A_CTS	C14	WKUP_UART0_CTS#	W23	Clear to Send handshake line for port A	I CMOS	1.8 V		
UART_B_RX	D14	OSPI0_CS2#	D18	Asynchronous serial data input port B	I CMOS	1.8 V		
UART_B_TX	D13	OSPI0_CS3#	C23	Asynchronous serial data output port B	O CMOS	1.8 V		
UART_B_RTS	D15	OSPI0_LBCLKO	E18	Request to Send handshake line for port B	O CMOS	1.8 V		
UART_B_CTS	D16	OSPI0_DQS	E22	Clear to Send handshake line for port B	I CMOS	1.8 V		
UART_C_RX	A22	OSPI0_D6	G20	Asynchronous serial data input port C	I CMOS	1.8 V		
UART_C_TX	B23	OSPI0_D7	F20	Asynchronous serial data output port C	O CMOS	1.8 V		
UART_D_RX	C22	OSPI0_D4	F21	Asynchronous serial data input port D	I CMOS	1.8 V		
UART_D_TX	C23	OSPI0_D5	F19	Asynchronous serial data output port D	O CMOS	1.8 V		
UART_CON_RX	D22	UART0_RXD	D13	Asynchronous serial data input port console	I CMOS	1.8 V		
UART_CON_TX	D23	UART0_TXD	C13	Asynchronous serial data output port console	O CMOS	1.8 V		
ETH_A_(R)(G)MII_CRS	E16	NC						
ETH_A_(R)(G)MII_COL	F15	NC						
ETH_A_(S)(R)(G)MII_TXD0	H15	RGMII1_TD0	AC10	Transmit data bit 0 (transmitted first) port A	O CMOS	1.8 V		
ETH_A_(S)(R)(G)MII_TXD1	G15	RGMII1_TD1	W13	Transmit data bit 1 port A	O CMOS	1.8 V		
ETH_A_(S)(R)(G)MII_TXD2	H16	RGMII1_TD2	Y11	Transmit data bit 2 port A	O CMOS	1.8 V		
ETH_A_(S)(R)(G)MII_TXD3	G16	RGMII1_TD3	AA11	Transmit data bit 3 port A	O CMOS	1.8 V		
ETH_A_(R)(G)MII_TX_EN(_ER)	K16	RGMII1_TX_CTL	AB11	Transmit enable (Error) port A	O CMOS	1.8 V		
ETH_A_(R)(G)MII_TX_CLK	J15	RGMII1_TXC	W11	Transmit clock port A	I/O CMOS	1.8 V		
ETH_A_(S)(R)(G)MII_RXD0	K15	RGMII1_RD0	Y8	Receive data bit 0 (received first) port A	I CMOS	1.8 V		
ETH_A_(S)(R)(G)MII_RXD1	L15	RGMII1_RD1	AA6	Receive data bit 1 port A	I CMOS	1.8 V		
ETH_A_(R)(G)MII_RXD2	N15	RGMII1_RD2	AA8	Receive data bit 2 port A	I CMOS	1.8 V		
ETH_A_(R)(G)MII_RXD3	P15	RGMII1_RD3	W8	Receive data bit 3 port A	I CMOS	1.8 V		
ETH_A_(R)(G)MII_RX_ER	L16	NC						
ETH_A_(R)(G)MII_RX_DV(_ER)	M15	RGMII1_RX_CTL	Y6	Receive data valid port A	I CMOS	1.8 V		
ETH_A_(R)(G)MII_RX_CLK	R15	RGMII1_RXC	Y7	Receive clock port A	I/O CMOS	1.8 V		
ETH_A_SDP	N16	NC						
ETH_MDIO	T15	MDIO0_MDIO	AC13	Management bus data signal for Ethernet	I/O CMOS	1.8 V		Can be used for all ETH ports
ETH_MDC	T16	MDIO0_MDC	AC15	Management bus clock signal for Ethernet	O CMOS	1.8 V		Can be used for all ETH ports
ETH_IOPWR	M17	V_1V8		ETH voltage. IO Voltage Level for all Ethernet interfaces	PO	1.8 V		max. current 100 mA
GPIO_A_0	D17	GPMC0_AD0	L22	General purpose I/O Contact A0	I/O CMOS	1.8 V		BOOTMODE00
GPIO_A_1	E17	GPMC0_AD1	L23	General purpose I/O Contact A1	I/O CMOS	1.8 V		BOOTMODE01
GPIO_A_2	F17	GPMC0_AD2	K22	General purpose I/O Contact A2	I/O CMOS	1.8 V		BOOTMODE02
GPIO_A_3	G17	GPMC0_AD3	J23	General purpose I/O Contact A3	I/O CMOS	1.8 V		BOOTMODE03

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
GPIO_A_4	H17	GPMC0_AD4	K23	General purpose I/O Contact A4	I/O CMOS	1.8 V		BOOTMODE04
GPIO_A_5	J17	GPMC0_AD5	H22	General purpose I/O Contact A5	I/O CMOS	1.8 V		BOOTMODE05
GPIO_A_6	K17	GPMC0_ADV#_ALE	N19	General purpose I/O Contact A6	I/O CMOS	1.8 V		Dual function: SPI_A_CS1#
GPIO_A_7	L17	GPMC0_WP#	N21	General purpose I/O Contact A7	I/O CMOS	1.8 V		Dual function: SPI_B_CS1#
GPIO_B_0	D19	GPMC0_AD6	H23	General purpose I/O Contact B0	I/O CMOS	1.8 V		BOOTMODE06
GPIO_B_1	E19	GPMC0_AD7	J22	General purpose I/O Contact B1	I/O CMOS	1.8 V		BOOTMODE07
GPIO_B_2	F19	GPMC0_AD8	H19	General purpose I/O Contact B2	I/O CMOS	1.8 V		BOOTMODE08
GPIO_B_3	G19	GPMC0_AD9	H20	General purpose I/O Contact B3	I/O CMOS	1.8 V		BOOTMODE09
GPIO_B_4	H19	GPMC0_AD10	H21	General purpose I/O Contact B4	I/O CMOS	1.8 V		BOOTMODE10
GPIO_B_5	J19	GPMC0_AD11	H18	General purpose I/O Contact B5	I/O CMOS	1.8 V		BOOTMODE11
GPIO_B_6	K19	GPMC0_AD12	G23	General purpose I/O Contact B6	I/O CMOS	1.8 V		
GPIO_B_7	L19	GPMC0_AD13	G22	General purpose I/O Contact B7	I/O CMOS	1.8 V		
SDIO_A_CMD	E20	MMC1_CMD	Y3	SDIO A Command/Response. Card initialization and command transfers	I/O CMOS	1.8 V or 3.3 V		
SDIO_A_CLK	F21	MMC1_CLK	Y2	SDIO A Clock	O CMOS	1.8 V or 3.3 V		
SDIO_A_D0	G20	MMC1_DAT0	AA1	SDIO A Data lines. Push-pull mode	I/O CMOS	1.8 V or 3.3 V		
SDIO_A_D1	G21	MMC1_DAT1	Y4	SDIO A Data lines. Push-pull mode	I/O CMOS	1.8 V or 3.3 V		
SDIO_A_D2	H20	MMC1_DAT2	AA2	SDIO A Data lines. Push-pull mode	I/O CMOS	1.8 V or 3.3 V		
SDIO_A_D3	H21	MMC1_DAT3	AB2	SDIO A Data lines. Push-pull mode	I/O CMOS	1.8 V or 3.3 V		
SDIO_A_CD#	J21	MMC1_SDCD	B6	SDIO A Card Detect	I OD CMOS	1.8 V	PU 10k	
SDIO_A_WP	D20	MMC1_SDWP	D6	SDIO A Write Protect	I OD CMOS	1.8 V	PU 10k	Tie to GND on carrier, if not used
SDIO_A_PWR_EN	D21	EXT_REFCLK1	D16	SDIO A Power Enable	O CMOS	1.8 V		
SDIO_A_IOPWR	C20	V_VDDSHV_MMC	T16	SDIO A Voltage.	PO	1.8 V or 3.3 V		max. current 20 mA
SDIO_B_CLK	K20	MMC2_CLK	R23	SDIO B Clock	O CMOS	1.8 V		
SDIO_B_CMD	K21	MMC2_CMD	U23	SDIO B Command/Response	I/O CMOS	1.8 V		
SDIO_B_D0	L20	MMC2_DAT0	U22	SDIO B Data lines.	I/O CMOS	1.8 V		
SDIO_B_D1	L21	MMC2_DAT1	T22	SDIO B Data lines.	I/O CMOS	1.8 V		
SDIO_B_D2	M21	MMC2_DAT2	T23	SDIO B Data lines.	I/O CMOS	1.8 V		
SDIO_B_D3	N20	MMC2_DAT3	R22	SDIO B Data lines.	I/O CMOS	1.8 V		
SDIO_B_D4	N21	NC						
SDIO_B_D5	P20	NC						
SDIO_B_D6	P21	NC						
SDIO_B_D7	R21	NC						
SDIO_B_CD#	T21	MMC2_SDCD	T20	SDIO B Card Detect	I OD CMOS	1.8 V	PU 10k	

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
SDIO_B_WP	U20	MMC2_SDWP	T21	SDIO B Write Protect	I OD CMOS	1.8 V	PU 10k	Tie to GND on carrier, if not used
SDIO_B_PWR_EN	U21	WKUP_CLKOUT0	Y23	SDIO B Power Enable.	O CMOS	1.8 V		
SDIO_B_IOPWR	T20	V_1V8		SDIO B Voltage.	PO	1.8 V		max. current 100 mA
PWM_0	E18	MCASP0_AFSR	C11	Pulse width modulation 0	O CMOS	1.8 V		Dual function: DISP_BL_PWM
PWM_1	F18	MCASP0_ACLKR	A12	Pulse width modulation 1	O CMOS	1.8 V		
PWM_2	G18	I2C1_SCL	D7	Pulse width modulation 2	O CMOS	1.8 V		
PWM_3	H18	GPMC0_CLK	L21	Pulse width modulation 3	O CMOS	1.8 V		
PWM_4	J18	SPI0_CS1	D11	Pulse width modulation 4	O CMOS	1.8 V		
PWM_5	K18	ADC0_AIN3	V21	Pulse width modulation 5	O CMOS	1.8 V		Default: not connected
ADC_0	M18	ADC0_AIN0	V20	Analog Digital Converter 0	Analog	0 V…1.8 V		
ADC_1	N18	ADC0_AIN1	V22	Analog Digital Converter 1	Analog	0 V…1.8 V		
SPI_A_SDI_(IO1)	U15	OSPI0_D1	D21	SPI A Serial Data Input	I/O CMOS	1.8 V		Alternate use: QuadSPI IO1
SPI_A_SDO_(IO0)	V15	OSPI0_D0	C22	SPI A Serial Data Output	I/O CMOS	1.8 V		Alternate use: QuadSPI IO0
SPI_A_WP_(IO2)	W16	OSPI0_D2	E23	SPI A Write Protect	I/O CMOS	1.8 V		Alternate use: QuadSPI IO2
SPI_A_HOLD_(IO3)	W15	OSPI0_D3	D23	SPI A Suspends Serial Input	I/O CMOS	1.8 V		Alternate use: QuadSPI IO3
SPI_A_CS0#	Y15	OSPI0_CS0#	C20	SPI A Master Chip Select 0	O CMOS	1.8 V		
SPI_A_SCK	U16	OSPI0_CLK	D22	SPI A Serial Data Clock	O CMOS	1.8 V		
SPI_B_SDI	Y22	SPI0_D1	B12	SPI B Serial Data Input	I CMOS	1.8 V		
SPI_B_SDO	Y23	SPI0_D0	E12	SPI B Serial Data Output	O CMOS	1.8 V		
SPI_B_CS0#	AA23	SPI0_CS0#	E11	SPI B Master Chip Select 0	O CMOS	1.8 V		
SPI_B_SCK	Y21	SPI0_CLK	E13	SPI B Serial Data Clock	O CMOS	1.8 V		
I2S_A_DATA_IN	V21	MCASP0_AXR0	B9	I2S A Digital audio Input	I/O CMOS	1.8 V		
I2S_A_DATA_OUT	W21	MCASP0_AXR1	A9	I2S A Digital audio Output	I/O CMOS	1.8 V		
I2S_B_DATA_IN	V19	GPMC0_WE#	M19	I2S B Digital audio Input	I/O CMOS	1.8 V		
I2S_B_DATA_OUT	W19	GPMC0_OE#_RE#	N20	I2S B Digital audio Output	I/O CMOS	1.8 V		
I2S_MCLK	V18	NC						
I2S_A_LRCLK	W18	MCASP0_AFSX	B11	I2S Left & Right synchronization clock	I/O CMOS	1.8 V		Module Output if CPU Master, Input if Slave
I2S_A_BITCLK	W20	MCASP0_ACLKX	A11	I2S Digital audio clock	I/O CMOS	1.8 V		
I2S_B_LRCLK	T18	GPMC0_WAIT0	N23	I2S Left & Right synchronization clock	I/O CMOS	1.8 V		
I2S_B_BITCLK	T19	GPMC0_BE0#_CLE	P23	I2S Digital audio clock	I/O CMOS	1.8 V		
CAN_A_TX	AC17	MCAN0_TX	B16	CAN port A Transmit output	O CMOS	1.8 V		
CAN_A_RX	AB17	MCAN0_RX	B15	CAN port A Receive input	I CMOS	1.8 V		
CAN_B_TX	AC19	UART0_RTS#	B13	CAN port B Transmit output	O CMOS	1.8 V		
CAN_B_RX	AB19	UART0_CTS#	B14	CAN port B Receive input	I CMOS	1.8 V		
USB_A_D_N	AB13	USB0_DM	AC4	USB differential data pairs for port A	I/O USB	USB		
USB_A_D_P	AC14	USB0_DP	AB4	USB differential data pairs for port A	I/O USB	USB		

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
USB_A_ID	AB14	MCASP0_AXR2	B10	Input Contact to announce OTG device insertion on USB 2.0 port	I OD CMOS	1.8 V	PU 10k	
USB_A_OC#	AC15	MCASP0_AXR3	A8	USB over-current for port A	I OD CMOS	1.8 V	PU 10k	
USB_A_VBUS	AB16	USB0_VBUS	AC3	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V		
USB_A_EN	AC16	USB0_DRVVBUS	C6	Power enable for USB VBUS voltage	O CMOS	1.8 V		
USB_B_D_N	AB23	USB1_DM	AC5	USB differential data pairs for port B	I/O USB	USB		
USB_B_D_P	AC22	USB1_DP	AB5	USB differential data pairs for port B	I/O USB	USB		
USB_B_ID	AB22	GPMC0_CS1#	L19	Input Contact to announce OTG device insertion on USB 2.0 port	I OD CMOS	1.8 V	PU 10k	
USB_B_OC#	AC21	I2C1_SDA	A6	USB over-current for port B	I OD CMOS	1.8 V	PU 10k	
USB_B_VBUS	AB20	USB1_VBUS	AB6	USB port 0 port power detection	I USB VBUS 5V	USB VBUS 5V		
USB_B_EN	AC20	USB1_DRVVBUS	A5	Power enable for USB VBUS voltage	O CMOS	1.8 V		
I2C_A_SCL	AA15	I2C0_SCL	B7	I2C Port A Clock Signal	I/O OD CMOS	1.8 V	PU 2k2	
I2C_A_SDA	AA16	I2C0_SDA	A7	I2C Port A Data Signal	I/O OD CMOS	1.8 V	PU 2k2	
I2C_B_SCL	AA20	I2C2_SCL	B8	I2C Port B Clock Signal	I/O OD CMOS	1.8 V	PU 2k2	
I2C_B_SDA	AA21	I2C2_SDA	D8	I2C Port B Data Signal	I/O OD CMOS	1.8 V	PU 2k2	
COM_AREA_01	A15	DGND						
COM_AREA_02	A16	NC						
COM_AREA_03	A17	DGND						
COM_AREA_04	A18	DGND						
COM_AREA_05	A19	DGND						
COM_AREA_06	A20	NC						
COM_AREA_07	A21	DGND						
COM_AREA_08	B15	DGND						
COM_AREA_09	B16	DGND						
COM_AREA_10	B17	DGND						
COM_AREA_11	B18	DGND						
COM_AREA_12	B19	DGND						
COM_AREA_13	B20	DGND						
COM_AREA_14	B21	DGND						
COM_AREA_15	C15	NC						
COM_AREA_16	C17	NC						
COM_AREA_17	C19	NC						
COM_AREA_18	C21	NC						
RESERVED	AA13	TEMP_ALERT		Reserved for future use				
Vendor Defined	B22	V_VPP	N18	Defined by module manufacturer				
Vendor Defined	C16	EMU0	Y16					
Vendor Defined	P16	EMU1	AA16					
VCC_5_TEST	Y3	V_1V8A		Module power voltage test point	PO			Factory Test Only
VCC_6_TEST	C5	V_VDD_RTC			PO			

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
VCC_IN_5V	Y8, Y9, Y10, Y11	V_5V_IN		Module power input voltage of 5 V	P			Tolerance: 5 V +- 5%
GND	A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10	DGND		Module Signal and power return and GND reference	P			
PWR_BTN#	AA9	TQM_HARD_RST#		Power-button input from Carrier board. Active low	I OD CMOS	1.8 V…5 V	PU 10K	
ETH_B_(R)(G)MII_CRS	D2	NC						
ETH_B_(R)(G)MII_COL	E1	NC						
ETH_B_(S)(R)(G)MII_TXD0	G1	RGMII2_TD0	AC12	Transmit data bit 0 (transmitted first) port B	O CMOS	1.8 V		
ETH_B_(S)(R)(G)MII_TXD1	F1	RGMII2_TD1	AB13	Transmit data bit 1 port B	O CMOS	1.8 V		
ETH_B_(S)(R)(G)MII_TXD2	G2	RGMII2_TD2	AA12	Transmit data bit 2 port B	O CMOS	1.8 V		
ETH_B_(S)(R)(G)MII_TXD3	F2	RGMII2_TD3	AA13	Transmit data bit 3 port B	O CMOS	1.8 V		
ETH_B_(R)(G)MII_TX_EN(_ER)	J2	RGMII2_TX_CTL	AB12	Transmit enable (Error) port B	O CMOS	1.8 V		
ETH_B_(R)(G)MII_TX_CLK	H1	RGMII2_TXC	Y13	Transmit clock port B	I/O CMOS	1.8 V		
ETH_B_(S)(R)(G)MII_RXD0	J1	RGMII2_RD0	AB9	Receive data bit 0 (received first) port B	I CMOS	1.8 V		
ETH_B_(S)(R)(G)MII_RXD1	K1	RGMII2_RD1	AC9	Receive data bit 1 port B	I CMOS	1.8 V		
ETH_B_(R)(G)MII_RXD2	M1	RGMII2_RD2	AB10	Receive data bit 2 port B	I CMOS	1.8 V		
ETH_B_(R)(G)MII_RXD3	N1	RGMII2_RD3	AB8	Receive data bit 3 port B	I CMOS	1.8 V		
ETH_B_(R)(G)MII_RX_ER	K2	NC						
ETH_B_(R)(G)MII_RX_DV(_ER)	L1	RGMII2_RX_CTL	AC8	Receive data valid (Error) port B	I CMOS	1.8 V		
ETH_B_(R)(G)MII_RX_CLK	P1	RGMII2_RXC	AC7	Receive clock port B	I/O CMOS	1.8 V		
ETH_B_SDP	M2	NC						
ETH_B_MDIO	C7	NC						
ETH_B_MDC	C6	NC						
GPIO_C_0	D3	GPMC0_AD14	F22	General purpose I/O Contact C0	I/O CMOS	1.8 V		
GPIO_C_1	D4	GPMC0_AD15	F23	General purpose I/O Contact C1	I/O CMOS	1.8 V		BOOTMODE15 Default '1' for Reduced Pin Mapping
GPIO_C_2	E3	GPMC0_CS0#	L20	General purpose I/O Contact C2	I/O CMOS	1.8 V		Dual function: CAM_B_PWR
GPIO_C_3	E4	GPMC0_BE1#	P22	General purpose I/O Contact C3	I/O CMOS	1.8 V		Dual function: CAM_B_RST#
GPIO_C_4	F3	GPMC0_CS2#	M23	General purpose I/O Contact C4	I/O CMOS	1.8 V		Dual function: DISP_VDD_EN
GPIO_C_5	F4	GPMC0_CS3#	M22	General purpose I/O Contact C5	I/O CMOS	1.8 V		Dual function: DISP_BL_EN
GPIO_C_6	G3	GPMC0_DIR	M21	General purpose I/O Contact C6	I/O CMOS	1.8 V		Dual function: CAM_A_PWR
GPIO_C_7	G4	GPMC0_WAIT1	N22	General purpose I/O Contact C7	I/O CMOS	1.8 V		Dual function: CAM_A_RST#
DSI_DATA0_N/LVDS_A_LANE0_N	AB11	DSI0_TXN0	B19	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
DSI_DATA0_P/LVDS_A_LANE0_P	AB10	DSI0_TXP0	B18	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA1_N/LVDS_A_LANE1_N	AC9	DSI0_TXN1	A18	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA1_P/LVDS_A_LANE1_P	AC8	DSI0_TXP1	A17	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA2_N/LVDS_A_LANE2_N	AC6	DSI0_TXN2	A20	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA2_P/LVDS_A_LANE2_P	AC5	DSI0_TXP2	A21	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA3_N/LVDS_A_LANE3_N	AB5	DSI0_TXN3	B22	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA3_P/LVDS_A_LANE3_P	AB4	DSI0_TXP3	B21	DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_CLOCK_N/LVDS_A_CLK_N	AB8	DSI0_TXCLKN	A15	DSI differential clock / LVDS channel A clock	O LVDS D-PHY / O LVDS LCD			
DSI_CLOCK_P/LVDS_A_CLK_P	AB7	DSI0_TXCLKP	A14	DSI differential clock / LVDS channel A clock	O LVDS D-PHY / O LVDS LCD			
DSI_TE	AA3	OSPI0_CS1#	D20	DSI panel tearing effect signal	I CMOS	1.8 V		
DSI_DATA0_N/LVDS_A_LANE0_N	AB11	DSI0_TXN0		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA0_P/LVDS_A_LANE0_P	AB10	DSI0_TXP0		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA1_N/LVDS_A_LANE1_N	AC9	DSI0_TXN1		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA1_P/LVDS_A_LANE1_P	AC8	DSI0_TXP1		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA2_N/LVDS_A_LANE2_N	AC6	DSI0_TXN2		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA2_P/LVDS_A_LANE2_P	AC5	DSI0_TXP2		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_DATA3_N/LVDS_A_LANE3_N	AB5	DSI0_TXN3		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
DSI_DATA3_P/LVDS_A_LANE3_P	AB4	DSI0_TXP3		DSI differential output / LVDS channel A data	O LVDS D-PHY / O LVDS LCD			
DSI_CLOCK_N/LVDS_A_CLK_N	AB8	DSI0_TXCLKN		DSI differential clock / LVDS channel A clock	O LVDS D-PHY / O LVDS LCD			
DSI_CLOCK_P/LVDS_A_CLK_P	AB7	DSI0_TXCLKP		DSI differential clock / LVDS channel A clock	O LVDS D-PHY / O LVDS LCD			
DSI_TE	AA3	OSPI0_CS1#		DSI panel tearing effect signal	I CMOS	1.8 V		
CSI_A_DATA0_N	C1	NC						
CSI_A_DATA0_P	B1	NC						
CSI_A_DATA1_N	A2	NC						
CSI_A_DATA1_P	A3	NC						
CSI_A_DATA2_N	A5	NC						
CSI_A_DATA2_P	A6	NC						
CSI_A_DATA3_N	B6	NC						
CSI_A_DATA3_P	B7	NC						
CSI_A_CLOCK_N	B3	NC						
CSI_A_CLOCK_P	B4	NC						
CAM_MCK	C2	NC						
CAM_A_SDA/CSI_A_TX_N	C3	NC						
CAM_A_SCL/CSI_A_TX_P	C4	NC						
RGB_R0	Y7	NC						
RGB_R1	AA6	NC						
RGB_R2	Y6	NC						
RGB_R3	AA5	NC						
RGB_R4	Y5	NC						
RGB_R5	Y4	NC						
RGB_G0	W4	NC						
RGB_G1	V3	NC						
RGB_G2	V4	NC						
RGB_G3	U3	NC						
RGB_G4	T3	NC						
RGB_G5	T4	NC						
RGB_B0	R4	NC						
RGB_B1	R3	NC						
RGB_B2	P3	NC						
RGB_B3	N3	NC						
RGB_B4	N4	NC						
RGB_B5	M3	NC						
RGB_(PIXEL)CLK	M4	NC						
RGB_VSYNC	L3	NC						
RGB_HSYNC	K3	NC						

Contact Name	Pad	Signal Name	AM62L Ball	Functional Description	I/O Type	I/O Level	PU/PD	Comments
RGB_DISP	K4	NC						
RGB_DE	J4	NC						
RGB_RESET#	J3	NC						
RGB_CS#	H3	NC						
USB_C_D_N	D11	NC						
USB_C_D_P	D10	NC						
USB_C_ID	D9	NC						
USB_C_OC#	C8	NC						
USB_C_VBUS	C9	NC						
USB_C_EN	C10	NC						
USB_C_SSTX_N	A9	NC						
USB_C_SSTX_P	A8	NC						
USB_C_SSRX_N	B11	NC						
USB_C_SSRX_P	B10	NC						
PCIe_A_HSI0_P	AB1	NC						
PCIe_A_HSI0_N	AB2	NC						
PCIe_A_HSO0_P	AC2	NC						
PCIe_A_HSO0_N	AC3	NC						
PCIe_CLKREQ#	W2	NC						
PCIe_A_PERST#	V2	NC						
PCIe_REFCLK_P	W1	NC						
PCIe_REFCLK_N	Y1	NC						
PCIe_WAKE#	T2	NC						
PCIe_SMDAT	U1	NC						
PCIe_SMCLK	T1	NC						
PCIe_SM_ALERT#	R2	NC						
RESERVED	N2	ADC0_AIN2	V23	Reserved for future use				
RESERVED	AA2	RTC_INT#						
Vendor Defined	D6	EXT_WAKEUP0	AB19	Defined by module manufacturer				
Vendor Defined	D7	EXT_WAKEUP1	AB20					

4. SOFTWARE

The TQMa62LxxOA-S is shipped with a specially adapted bootloader, which is configured for use on a TQMA62LXXO-S-ADAP RK REV.0100 and a MBa62xx.

This bootloader contains module specific as well as board specific adjustments like e.g.

- Processor configuration
- RAM configuration / timing
- Muxing
- Clocks
- Driver strengths

When using a different bootloader this data has to be adapted. Details can be requested from TQ support. More information can be found in the Support Wiki for the TQMa62LxxOA-S.

5. MECHANICS

5.1 TQMa62LxxOA-S dimensions and footprint

The overall dimensions (length × width) of the TQMa62LxxOA-S are 30.0 mm × 30.0 mm (± 0.1 mm).
The mass of TQMa62LxxOA-S is TBD g (± TBD g).

TBD

Figure 12: Dimensions TQMa62LxxOA-S

5.2 LGA pads of the OSM

Thanks to its OSM-S form factor, the TQMa62LxxOA-S features a total of 332 pins in the form of LGA balls. Because it uses the LGA package, the module is soldered in place once, ensuring a permanent, stable connection to its peripherals. Removing the module from its soldered position is not easily possible, is not recommended, and may result in a reduction in service life or even damage to the module.

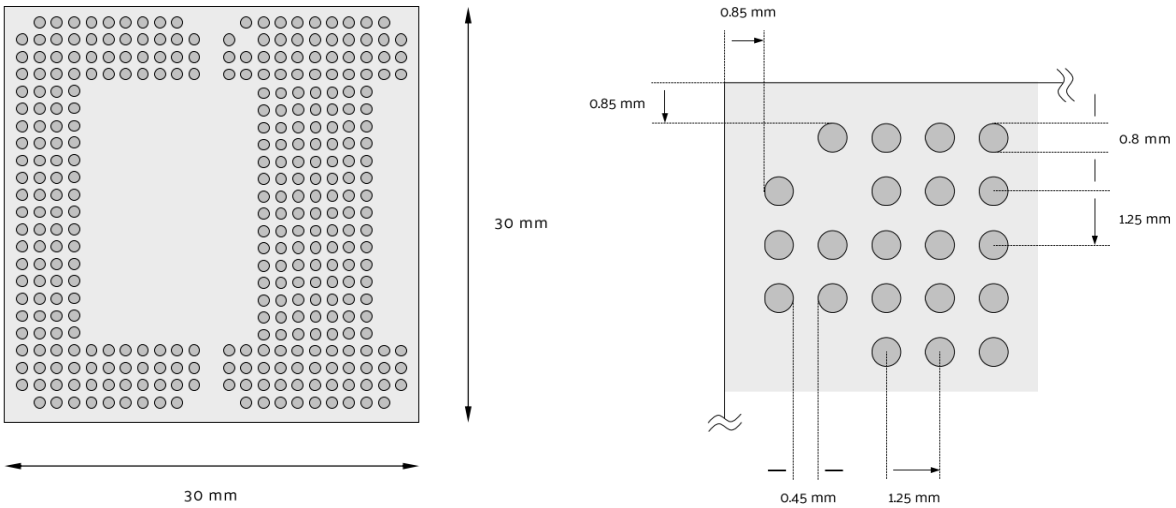

Figure 13: TQMa62LxxOA-S - view from Top through module

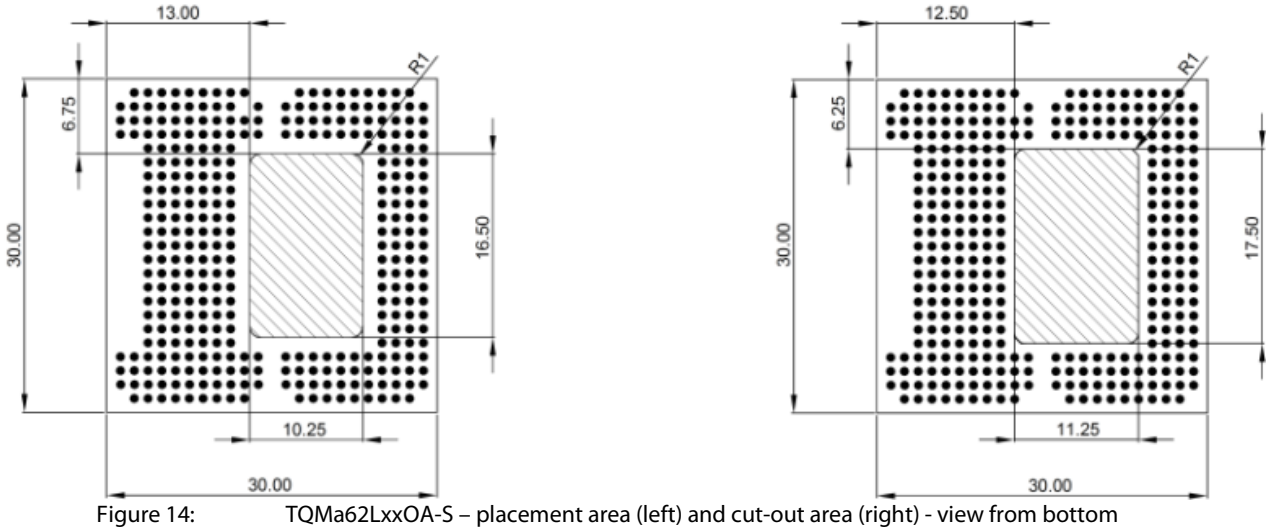

Figure 14: TQMa62LxxOA-S – placement area (left) and cut-out area (right) - view from bottom

5.3 TQMa62LxxOA-S component placement and labeling

The label AK1 includes TQ serial number, MAC address, and product name.

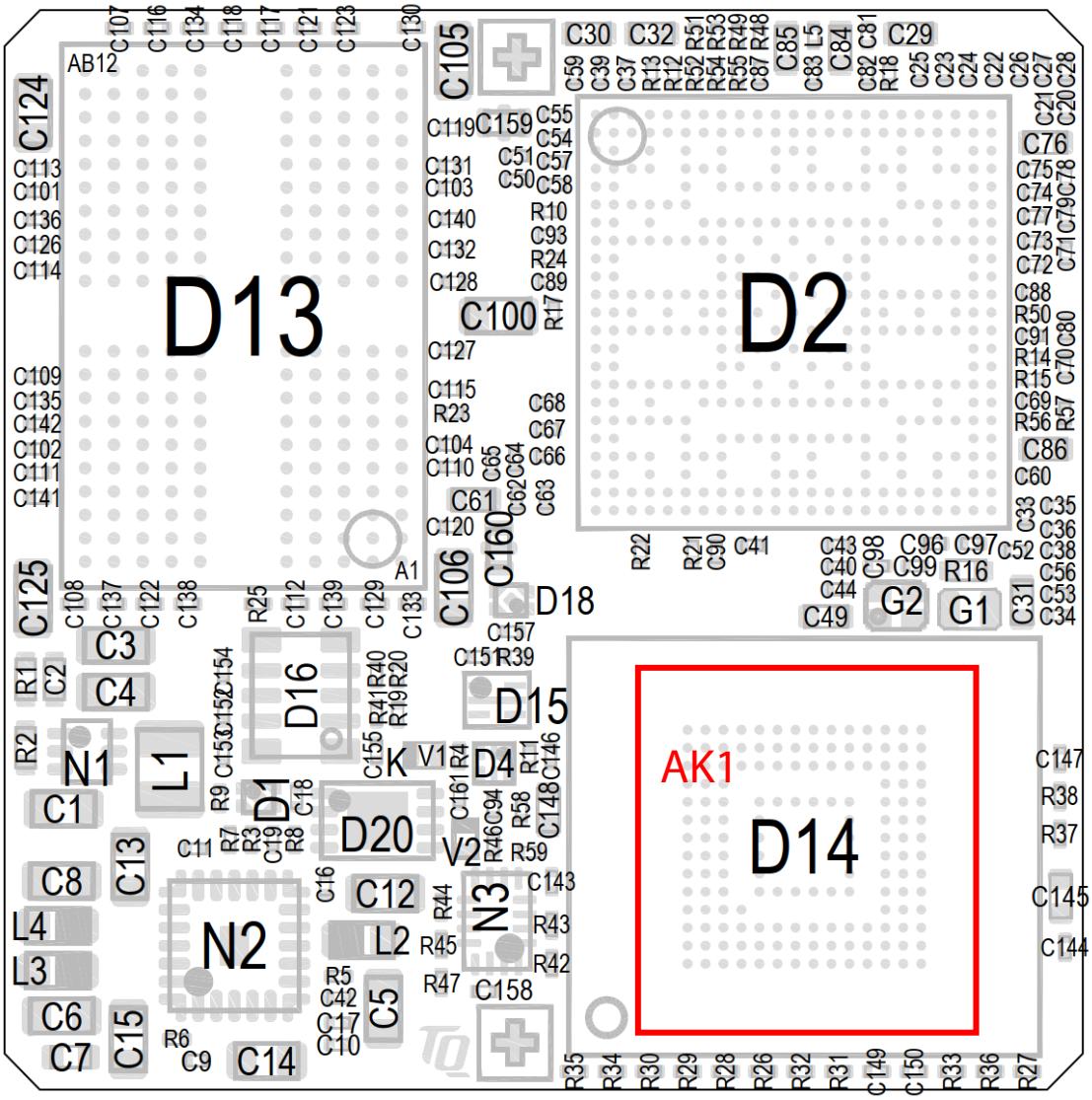

Figure 15: TQMa62LxxOA-S top view

5.4 Protection against external effects

As an embedded module the TQMa62LxxOA-S is not protected against dust, external impact and contact (IP00). Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

The power dissipation mainly depends on the software used and can vary according to the application. The power dissipation mainly arises at the processor, the switching regulators and the LPDDR4 devices. It is the customer's responsibility to define a suitable cooling method for his use case.

Attention: Destruction or malfunction, TQMa62LxxOA-S cooling	
	The AM62Lx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM62Lx must be taken into consideration when connecting the heat sink. The AM62Lx is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa62LxxOA-S and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMa62LxxOA-S has to be soldered on the carrier board. The TQMa62LxxOA-S is held on the mainboard by the holding force of the solder connections from the LGA pads and requires no further fastening measures. If there are high requirements for vibration and shock resistance, a module holder must be provided in the final application to additionally hold the module in position. Since no heavy and large components are used, there are no further requirements.

Attention: Note on equipping the base board	
	To ensure a high-quality connection of the LGA pads when reflow soldering the TQMa62LxxOA-S, the LGA pads must be free of grease and contamination. Please contact TQ-Support for soldering instructions (6).

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa62LxxOA-S was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding besides, take note of not only the frequency, but also the signal rise times
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.
As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa62LxxOA-S.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, Zener diode(s)
- Fast signal lines: Integrated protective devices (e.g., suppressor diode arrays)

6.3 Operational safety and personal security

Due to the occurring voltages (≤ 5 V DC), tests with respect to the operational and personal safety haven't been carried out.

6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the TQMa62LxxOA-S is only a sub-component of an overall system.

6.5 Climatic and operational conditions

The temperature range, in which the TQMa62LxxOA-S works reliably, strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 13: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Environmental temperature	–40 °C to +85 °C	With appropriate cooling
Permitted storage temperature	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

6.6 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.7 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.8 Reliability and service life

For the TQMa62LxxOA-S, a constant error rate results in an MTBF of approximately TBD hours.

Attention must be paid to a construction that is insensitive to vibration and shock.

Service life-limiting components such as electrolytic capacitors were not used.

6.9 Environment protection

6.9.1 RoHS

The TQMa62LxxOA-S is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

6.9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa62LxxOA-S was designed to be recyclable and easy to repair.

6.10 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

6.11 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa62LxxOA-S must therefore always be seen in conjunction with the complete device.

The available standby and sleep modes of the components on the TQMa62LxxOA-S enable compliance with EuP requirements for the TQMa62LxxOA-S.

6.12 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

6.13 Battery

No batteries are used on the TQMa62LxxOA-S.

6.14 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa62LxxOA-S, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The TQMa62LxxOA-S is delivered in reusable packaging.

6.15 Other entries

The energy consumption of this subassembly is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

7. APPENDIX

7.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 14: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AIN	Analog In
ARM®	Advanced RISC Machine
AVS	Adaptive Voltage Scaling
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
DC	Direct Current
DDR3L	Double Data Rate Type three Low voltage
DIN	Deutsche Industrie Norm
DVS	Dynamic Voltage Scaling
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electro-Magnetic Compatibility
eMMC	embedded Multi-Media Card
EN	Europäische Norm
ESD	Electro-Static Discharge
EU	European Union
EuP	Energy using Products
FR-4	Flame Retardant 4
GMII	Gigabit Media Independent Interface
GPIO	General Purpose Input/Output
GPMC	General Purpose Memory Controller
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IP	Ingress Protection
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MAC	Media Access Control
MCASP	Multichannel Audio Serial Port
MCSPI	Multichannel Serial Port Interface
MD	Management Data
MII	Media-Independent Interface
MMC	Multi-Media Card
MTBF	Mean operating Time Between Failures

7.1 Acronyms and definitions (continued)

Table 14: Acronyms (continued)

Acronym	Meaning
n.a.	Not Available
NC	Not Connected
PCB	Printed Circuit Board
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PRCM	Power and Clock Management
PU	Pull-Up
PWM	Pulse-Width Modulation
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection
WXGA	Wide Extended Graphics Array

7.2 References

Table 15: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	AM62Lx Sitara Processors Datasheet	B / Nov. 2025	Texas Instruments
(2)	AM62Lx Processors Silicon Revision 1.0 Technical Reference Manual	A / Sep. 2025	Texas Instruments
(3)	AM62Lx Processor Errata	B / Oct. 2025	Texas Instruments
(4)	MBa62xx User's Manual	– current –	TQ-Systems
(5)	Support-Wiki for the TQMa62LxxOA-S	– current –	TQ-Systems
(6)	Processing instructions for TQMa62LxxOA-S	– current –	TQ-Systems

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