MBa94xxCA
Preliminary User's Manual

MBa94xxCA UM 0001
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TABLE OF CONTENTS

1. ABOUT THIS MANUAL ... 1
1.1 Copyright and license expenses ... 1
1.2 Registered trademarks ... 1
1.3 Disclaimer ... 1
1.4 Intended Use ... 1
1.5 Imprint ... 2
1.6 Tips on safety ... 2
1.7 Symbols and typographic conventions ... 2
1.8 Handling and ESD tips ... 3
1.9 Naming of signals ... 3
1.10 Further applicable documents / presumed knowledge ... 3
2. BRIEF DESCRIPTION ... 5
2.1 MBa94xxCA block diagram ... 5
2.2 MBa94xxCA interfaces ... 6
3. ELECTRONICS ... 7
3.1 TQMa94xxLA ... 7
3.1.1 TQMa94xxLA connectors on MBa94xxCA ... 7
3.1.2 MBa94xxCA pinout ... 8
3.2 Boot Mode configuration ... 10
3.3 I²C Mapping ... 11
3.4 GPIO port expander ... 12
3.5 Temperature sensor and EEPROM ... 13
3.6 RTC backup ... 13
3.7 USB hub ... 14
3.8 CAN-FD ... 14
3.9 Debug USB / UART ... 15
3.10 Ethernet ... 15
3.10.1 1Gb Ethernet ... 17
3.10.2 2.5Gb Ethernet ... 17
3.10.3 Single Pair Ethernet (SPE) ... 17
3.10.4 EtherCAT ... 18
3.11 WiFi ... 18
3.12 LVDS ... 18
3.13 M.2 interfaces ... 20
3.14 SIM card ... 21
3.15 USB Host ... 21
3.16 USB Type-C ... 21
3.17 Micro-SD card ... 22
3.18 RS485 ... 22
3.19 MBa94xxCA Extension Headers (X4, X5, X6) ... 23
3.20 IO Header X25 ... 24
3.21 JTAG ... 25
3.22 Fan ... 25
3.23 Status LEDs ... 26
3.24 User Buttons ... 26
3.25 Power supply ... 27
3.25.1 Input protection ... 27
3.25.2 Power sequencing ... 29
3.25.3 V_5V and V_3V3 ... 30
3.25.4 V_5V_MB ... 30
3.25.5 V_1V8 ... 30
3.25.6 V_3V3A ... 31
3.25.7 V_1V0_ETH ... 31
3.25.8 V_1V1 ... 31
3.25.9 V_12V ... 31
3.25.10 V_2V5_ETH ... 32
3.25.11 Power consumption ... 32
3.26 Reset & Configuration ... 33
4. SOFTWARE ... 34
5. MECHANICS ... 34
5.1 MBa94xxCA dimensions ... 34

5.2 Embedding in the target system ... 34
5.3 Housing ... 34
5.4 Thermal management ... 34
5.5 Assembly & Labels ... 35
6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS ... 37
6.1 EMC ... 37
6.2 ESD ... 37
6.3 Operational safety and personal security ... 37
6.4 Cyber Security ... 37
7. CLIMATIC AND OPERATIONAL CONDITIONS ... 38
7.1 Protection against external effects ... 38
7.2 Reliability and service life ... 38
7.3 Export Control and Sanctions Compliance ... 38
7.4 Warranty ... 39
8. ENVIRONMENT PROTECTION ... 40
8.1 RoHS ... 40
8.2 WEEE® ... 40
8.3 REACH® ... 40
8.4 EuP ... 40
8.5 Statement on California Proposition 65 ... 40
8.6 Packaging ... 40
8.7 Batteries ... 40
8.7.1 General notes ... 40
8.7.2 Lithium batteries ... 40
8.8 Other entries ... 41
9. APPENDIX ... 42
9.1 Acronyms and definitions ... 42
9.2 References ... 44

TABLE DIRECTORY

Table 1: Terms and Conventions 2
Table 2: Data interfaces & power connectors 6
Table 3: Diagnostic and user interfaces 6
Table 4: Pinout MBa94xxCA connector X1 8
Table 5: Pinout MBa94xxCA connector X2 9
Table 6: Pinout MBa94xxCA connector X3 10
Table 7: Boot Mode configuration 11
Table 8: I^2C mapping 11
Table 9: Pinout RTC backup (X32 & X34) 13
Table 10: CAN termination with S6/S7 15
Table 11: Pinout CAN1 / 2 (X13, X14) 15
Table 12: Address mapping of the Ethernet PHYs 15
Table 13: Pinout LVDS Data (X19) 19
Table 14: Pinout LVDS CMD (X20) 20
Table 15: Logic USB Type-C port 22
Table 16: Pinout RS485 (X15) 22
Table 17: Termination switch S8 22
Table 18: Power consumption headers 23
Table 19: Pinout extension header X4 23
Table 20: Pinout extension header X5 24
Table 21: Pinout extension header X6 24
Table 22: Threshold digital inputs 24
Table 23: Pinout IO header X25 25
Table 24: Pinout JTAG (X20) 25
Table 25: Pinout fan header 26
Table 26: Supply voltage V_24V_IN at Power-In (X28, X29) 28
Table 27: Pinout power-in (X28, X29) 28
Table 28: Power sequencing 30
Table 29: Specifications V_5V and V_3V3 30
Table 30: Specification V_1V8 30
Table 31: Specification V_3V3A 31
Table 32: Specification V_1V0_ETH 31
Table 33: Specification V_1V1 31
Table 34: Specification V_12V 32
Table 35: Specification V_2V5_ETH 32
Table 36: Current consumption MBa94xxCA 32
Table 37: Reset signals 33
Table 38: Labels on MBa94xxCA 35
Table 39: Climatic and operational conditions MBa94xxCA 38
Table 40: Acronyms 42
Table 41: Further applicable documents 44

FIGURE DIRECTORY

Figure 1: Block diagram MBa94xxCA 5
Figure 2: Block diagram TQMa94xxLA 7
Figure 3: Block diagram boot mode 10
Figure 4: Block diagram GPIO expander 12
Figure 5: Block diagram temperature sensor 13
Figure 6: Block diagram RTC backup 13
Figure 7: Block diagram USB hub 14
Figure 8: Block diagram CAN 14
Figure 9: Block diagram USB debug 15
Figure 10: Block diagram Ethernet 16
Figure 11: Block diagram 1G Ethernet 17
Figure 12: Block diagram 2.5G Ethernet 17
Figure 13: Block diagram SPE 17
Figure 14: Block diagram EtherCAT 18
Figure 15: Block diagram WiFi 18
Figure 16: Block diagram LVDS 18
Figure 17: Block diagram M.2 20
Figure 18: Block diagram USB Host 21
Figure 19: Block diagram USB Type-C 21
Figure 20: Block diagram Micro-SD card 22
Figure 21: Block diagram RS485 22
Figure 22: Block diagram JTAG 25
Figure 23: Block diagram Status LEDs 26
Figure 24: Block diagram User Buttons 26
Figure 25: Block diagram MBa94xxCA power supply 27
Figure 26: Block diagram Power-In 28
Figure 27: Pinout DC socket 2.5 mm/6.5 mm 28
Figure 28: Power sequencing MBa94xxCA 29
Figure 29: Block diagram Reset & Configuration 33
Figure 30: MBa94xxCA top view 35
Figure 31: MBa94xxCA bottom view 36

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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.7 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa94xxCA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa94xxCA schematics
- TQMa94xxLA User's Manual
- i.MX 94 Data Sheet
- i.MX 94 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa94xxLA

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of the MBa94xxCA as of revision 02xx. The MBa94xxCA is designed as a carrier board for the TQMa94xxLA on the adapter TQMa94xxLA-ADAP.

Core of the MBa94xxCA is the TQMa94xxLA with an NXP i.MX 94 CPU.

The TQMa94xxLA connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, etc., all other available signals of the TQMa94xxLA are routed on 100 mil standard pin headers on the MBa94xxCA.

CPU features and interfaces can be evaluated, software development for a TQMa94xxLA based project can start immediately.

2.1 MBa94xxCA block diagram

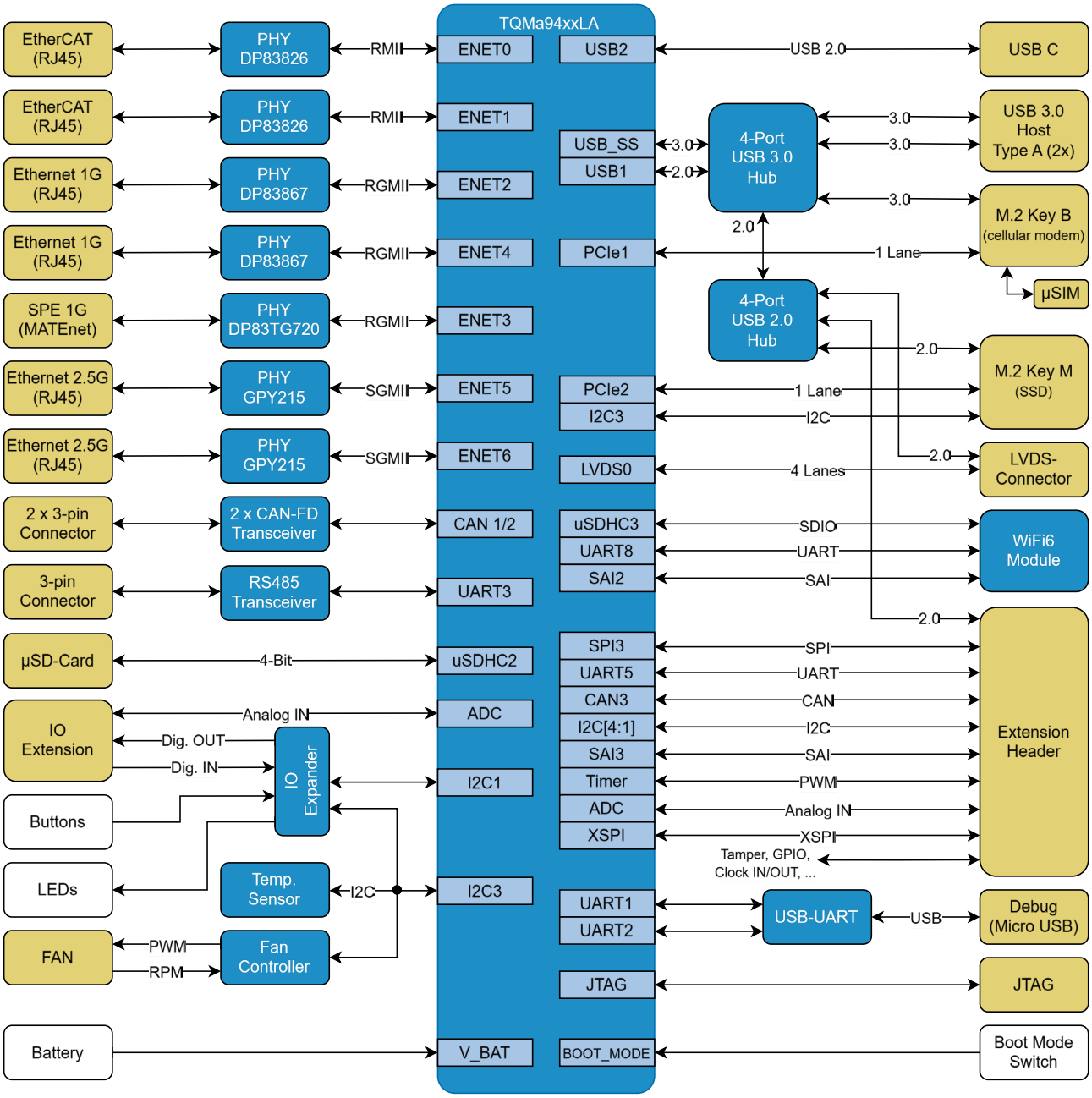

Figure 1: Block diagram MBa94xxCA

2.2 MBa94xxCA interfaces

The following interfaces/functions and user interfaces are available on the MBa94xxCA:

Table 2: Data interfaces & power connectors

Interface	Connector	Type
CAN-FD	X13, X14	3-pin Phoenix
Coin cell	X34	CR2032 holder
EtherCAT, 10Base-TE/100Base-TX	X21	Dual-RJ-45, integrated magnetics
Ethernet, 1000Base-T	X10, X11	RJ-45, integrated magnetics
Ethernet, 2.5GBase-T	X23, X12	RJ-45, integrated magnetics
Ethernet, 1000Base-T1/10Base-T1S	X24	MATEnet
Extension headers	X4, X5, X6	100 mil header, 2 × 40-pin, 1 x 10-pin
External battery	X32	2-pin header
Fan	X30	4-pin header
IO (digital / analog)	X25	30-pin terminal block
ISO 14443	X33	2-pin header for antenna
LVDS	X19	30-pin, DF19G
LVDS CMD	X20	20-pin, DF19G
M.2	X16	M.2 Socket Key M
	X17	M.2 Socket Key B
	X18	Micro-SIM card holder
Power In	X28	DC jack (2.5 mm / 5.5 mm)
	X29	2-pin screw terminal block
RS485	X15	3-pin Phoenix
SD card, UHS-I	X7	Push-Pull
USB 3.0 Host	X8	USB, stacked Type A
USB Type C	X9	USB, Type C
USB debug	X26	USB, Micro AB

The MBa94xxCA provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	7 × green LED	Power LEDs
	6 × green LED	USB hub, Type-C, VBUS
	1 × green LED	Debug LED for USB debug interface
	1 × green LED	User LED1
	1 × orange LED	User LED2
	2 × green LED	M.2
	1 × red LED	Reset LED
	6 × green / 6 x yellow LED	Ethernet LEDs (Activity / Speed)
	1 x green / 1 x orange	SPE (Activity / Speed)
	1 x green LED	SD card
Temperature sensor	1 × SE97BTP	Digital I^2C temperature sensor
Power / Reset button	2 × Push button	ONOFF (S3), WDOG_ANY (S2)
General Purpose button	2 × Push button	GP push button at port expander (S4, S5)
Boot Mode configuration	1 × 4-fold DIP switch	S1
CAN termination	2 × 2-fold DIP switch	S6, S7
JTAG	1 × 10-pin, 100 mil header	X27
RS485 termination	1 x 2-fold DIP switch	S8

3. ELECTRONICS

The following chapters describe the interfaces of the MBa94xxCA as of revision 02xx in connection with a TQMa94xxLA with maximum configuration. In any case the TQMa94xxLA User's Manual must be complied with.

3.1 TQMa94xxLA

The TQMa94xxLA is the central system on the MBa94xxCA. It provides LPDDR4 SDRAM, eMMC, temperature sensor with EEPROM, power supply and power management functionality. Further functionalities are optionally available (see Figure 2).

All TQMa94xxLA internal voltages are derived from the 5 V supply voltage. All functionally relevant pins of the CPU are routed to the TQMa94xxLA pads. This enables the user to use the TQMa94xxLA with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa94xxLA User's Manual.

On the MBa94xxCA the standard interfaces like USB, Ethernet, etc., provided by the TQMa94xxLA are routed to industry standard connectors. All other signals and buses provided by the TQMa94xxLA are routed to 100 mil headers. The boot behaviour of the TQMa94xxLA can be configured. The Boot Mode configuration is set by a DIP switch on the MBa94xxCA, see chapter 3.2.

Furthermore, the MBa94xxCA provides all power supplies and configurations required for the operation of the TQMa94xxLA.

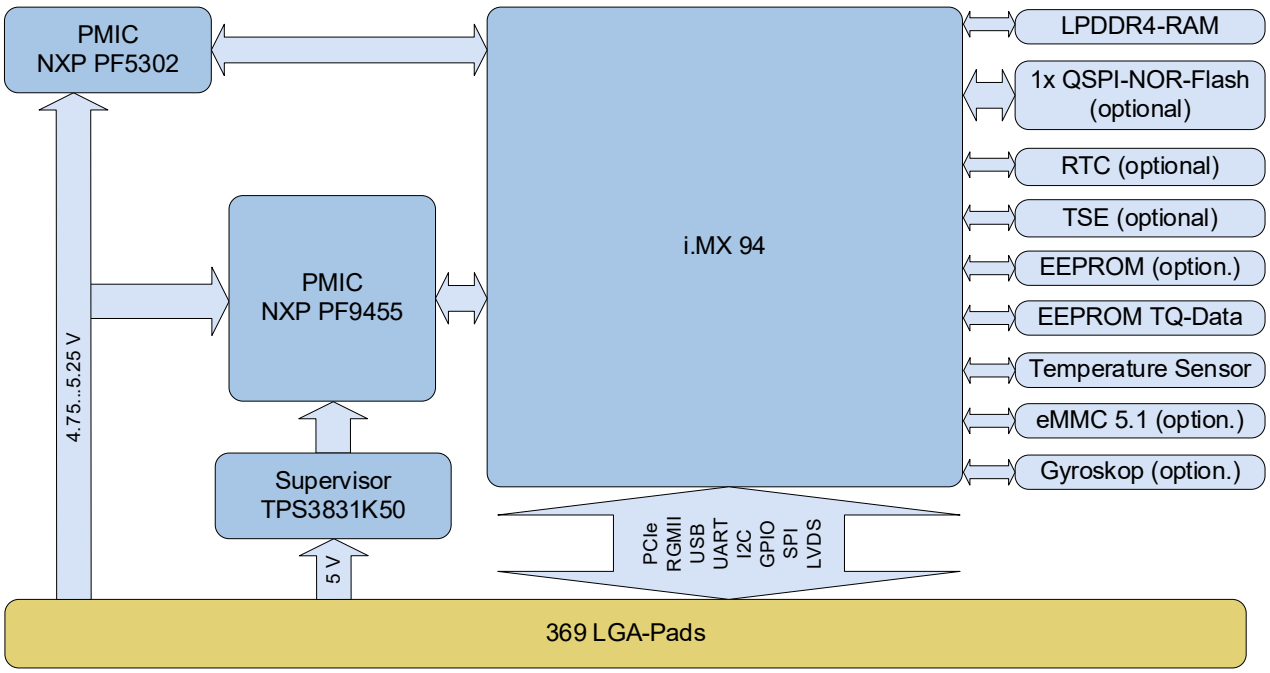

Figure 2: Block diagram TQMa94xxLA

3.1.1 TQMa94xxLA connectors on MBa94xxCA

The TQMa94xxLA is connected to the MBa94xxCA with 360 pins on three connectors (2 x EPT 401-51301-51, 1 x EPT 401-51701-51). Connector samples are available from: https://www.ept.de/index.php?tq-colibri-lp

The TQMa94xxLA is held in the mating connectors on the MBa94xxCA by 360 pins with a considerable retention force. To avoid damaging the connectors of the MBa94xxCA or the TQMa94xxLA while removing the TQMa94xxLA adapter, the use of the extraction tool TBD is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa94xxLA adapter for the extraction tool TBD.

The pins assignment listed in Table 4, Table 5, and Table 6 refer to the corresponding BSP provided by TQ-Systems.

For information regarding I/O pins in Table 4, Table 5, and Table 6 refer to the i.MX 94 documentation see Table 40.

3.1.2 MBa94xxCA pinout

All available TQMa94xxLA signals are available at the three connectors X1, X2, and X3 on the MBa94xxCA.
Further information like pull-ups or pull-downs on the TQMa94xxLA can be taken from the TQMa94xxLA User's Manual (6).

Table 4: Pinout MBa94xxCA connector X1

GPIO use	Muxing	TQ-Muxing	Pin	Pin	TQ-Muxing	Muxing	GPIO use
	PCIe_OUT_CLK_N	PCIe_OUT_CLK_N	A1	B1	GND	-	
	PCIe_OUT_CLK_P	PCIe_OUT_CLK_P	A2	B2	CAN1_RX	gpio1.IO[11] / ccmsrcgpcmix.BOOT_MODE[2]	RTC_Event + BM2
	GND	GND	A3	B3	PEX1_INT#	gpio1.IO[14]	Expander INT (wakeup)
	PCIe2_TX_N	PCIe2_TX_N	A4	B4	BM2_RTC_EVENT_MOD#	can1.TX	
	PCIe2_TX_P	PCIe2_TX_P	A5	B5	BM3_CAN1_TX	can1.RX	
	GND(FIXED)	GND (FIXED)	A6	B6	GND (FIXED)		
	PCIe2_RX_N	PCIe2_RX_N	A7	B7	ADC_IN7	ADC_IN7	
	PCIe2_RX_P	PCIe2_RX_P	A8	B8	ADC_IN6	ADC_IN6	
	GND	GND	A9	B9	ADC_IN5	ADC_IN5	
	PCIe2_REFCLK_N	PCIe2_REFCLK_N	A10	B10	ADC_IN4	ADC_IN4	
	PCIe2_REFCLK_P	PCIe2_REFCLK_P	A11	B11	GND		
	GND	GND	A12	B12	ADC_IN3	ADC_IN3	
	GND	GND	A13	B13	ADC_IN2	ADC_IN2	
	PCIe1_TX_N	PCIe1_TX_N	A14	B14	ADC_IN1	ADC_IN1	
	PCIe1_TX_P	PCIe1_TX_P	A15	B15	ADC_IN0	ADC_IN0	
	GND(FIXED)	GND (FIXED)	A16	B16	GND (FIXED)		
	PCIe1_RX_N	PCIe1_RX_N	A17	B17	I2C1_SCL	i2c1.SCL	
	PCIe1_RX_P	PCIe1_RX_P	A18	B18	I2C1_SDA	i2c1.SDA	
	GND	GND	A19	B19	GND		
	PCIe1_REFCLK_N	PCIe1_REFCLK_N	A20	B20	XSPI1_DATA1	XSPI1_DATA1	
	PCIe1_REFCLK_P	PCIe1_REFCLK_P	A21	B21	XSPI1_DATA0	XSPI1_DATA0	
	GND	GND	A22	B22	XSPI1_DATA3	XSPI1_DATA3	
	RFU	RFU	A23	B23	XSPI1_DATA4	XSPI1_DATA4	
	i2c2.SCL	I2C2_SCL	A24	B24	XSPI1_DATA6	XSPI1_DATA6	
	i2c2.SDA	I2C2_SDA	A25	B25	XSPI1_DATA5	XSPI1_DATA5	
		GND (FIXED)	A26	B26	GND(FIXED)	GND(FIXED)	
	USB1_SS_TX1_N	USB1_SS_TX1_N	A27	B27	XSPI1_SCLK	XSPI1_SCLK	
	USB1_SS_TX1_P	USB1_SS_TX1_P	A28	B28	XSPI1_DATA7	XSPI1_DATA7	
	GND	GND	A29	B29	XSPI1_DATA2	XSPI1_DATA2	
	USB1_SS_TX0_N	USB1_SS_TX0_N	A30	B30	XSPI1_DQS	XSPI1_DQS	
	USB1_SS_TX0_P	USB1_SS_TX0_P	A31	B31	XSPI1_SS0_B	XSPI1_SS0_B	
		GND	A32	B32	XSPI1_SS1_B	XSPI1_SS1_B	
	USB1_VBUS	USB1_VBUS	A33	B33	GND		
	USB1_DN	USB1_DN	A34	B34	PDM_BIT_STREAM0	gpio1.IO[9]	Gyro INT
	USB1_DP	USB1_DP	A35	B35	PDM_BIT_STREAM1	m33.NMI	
		GND (FIXED)	A36	B36	GND (FIXED)		
	USB1_SS_RX1_N	USB1_SS_RX1_N	A37	B37	USB2_DN	USB2_DN	
	USB1_SS_RX1_P	USB1_SS_RX1_P	A38	B38	USB2_DP	USB2_DP	
	GND	GND	A39	B39	GND		
	USB1_SS_RX0_N	USB1_SS_RX0_N	A40	B40	USB2_VBUS	USB2_VBUS	
	USB1_SS_RX0_P	USB1_SS_RX0_P	A41	B41	USB2_ID	USB2_ID	
		GND	A42	B42	GND		
	uart1.RX	UART1_RXD	A43	B43	UART2_TXD	uart2.TX	
	uart1.TX	UART1_TXD	A44	B44	UART2_RXD	uart2.RX	
		GND (FIXED)	A45	B45	GND (FIXED)		
	netc_pinmux.ETH3_TXD[3]	ETH3_TXD3	A46	B46	ETH3_RXD3	netc_pinmux.ETH3_RXD[3]	
	netc_pinmux.ETH3_TXD[2]	ETH3_TXD2	A47	B47	ETH3_RXD2	netc_pinmux.ETH3_RXD[2]	
	netc_pinmux.ETH3_TXD[1]	ETH3_TXD1	A48	B48	ETH3_RXD1	netc_pinmux.ETH3_RXD[1]	
	netc_pinmux.ETH3_TXD[0]	ETH3_TXD0	A49	B49	ETH3_RXD0	netc_pinmux.ETH3_RXD[0]	
		GND	A50	B50	GND		
	netc_pinmux.ETH3_TX_CLK	ETH3_TX_CLK	A51	B51	ETH3_RX_CLK	netc_pinmux.ETH3_RX_CLK	
	netc_pinmux.ETH3_TX_CTL	ETH3_TX_CTL	A52	B52	ETH3_RX_CTL	netc_pinmux.ETH3_RX_CTL	
		GND	A53	B53	GND		
1G Phy #2 - RESET	gpio6.IO[14]	ETH3_MDC_GPIO1	A54	B54	ETH3_MDIO_GPIO2	gpio6.IO[15]	1G Phy #2 - INT
		GND (FIXED)	A55	B55	GND (FIXED)		
	netc.EMDC	ETH4_MDC_GPIO1	A56	B56	ETH4_MDIO_GPIO2	netc.EMDIO	
		GND	A57	B57	GND		
	netc_pinmux.ETH4_TX_CTL	ETH4_TX_CTL	A58	B58	ETH4_RX_CTL	netc_pinmux.ETH4_RX_CTL	
	netc_pinmux.ETH4_TX_CLK	ETH4_TX_CLK	A59	B59	ETH4_RX_CLK	netc_pinmux.ETH4_RX_CLK	
		GND	A60	B60	GND		
	netc_pinmux.ETH4_TXD[0]	ETH4_TXD0	A61	B61	ETH4_RXD0	netc_pinmux.ETH4_RXD[0]	
	netc_pinmux.ETH4_TXD[1]	ETH4_TXD1	A62	B62	ETH4_RXD1	netc_pinmux.ETH4_RXD[1]	
	netc_pinmux.ETH4_TXD[2]	ETH4_TXD2	A63	B63	ETH4_RXD2	netc_pinmux.ETH4_RXD[2]	
	netc_pinmux.ETH4_TXD[3]	ETH4_TXD3	A64	B64	ETH4_RXD3	netc_pinmux.ETH4_RXD[3]	
		GND(FIXED)	A65	B65	GND (FIXED)		
		AMUX	A66	B66	Tamper1	bbsmmix.TAMPER1	
	LVDS0_D0_N	LVDS0_D0_N	A67	B67	Tamper0	bbsmmix.TAMPER0	
	LVDS0_D0_P	LVDS0_D0_P	A68	B68	PMIC_ON_REQ	PMIC_ON_REQ	
		GND	A69	B69	GND		
	LVDS0_D1_N	LVDS0_D1_N	A70	B70	V_3V3		
	LVDS0_D1_P	LVDS0_D1_P	A71	B71	V_1V8		
		GND	A72	B72	GND		
	LVDS0_D2_N	LVDS0_D2_N	A73	B73	V_5V0		
	LVDS0_D2_P	LVDS0_D2_P	A74	B74	V_5V0		
		GND (FIXED)	A75	B75	GND (FIXED)		
	LVDS0_CLK_N	LVDS0_CLK_N	A76	B76	V_5V0		
	LVDS0_CLK_P	LVDS0_CLK_P	A77	B77	V_5V0		
		GND	A78	B78	V_5V0		
	LVDS0_D3_N	LVDS0_D3_N	A79	B79	V_5V0		
	LVDS0_D3_P	LVDS0_D3_P	A80	B80	V_5V0		

3.1.2 MBa94xxCA pinout (continued)

Table 5: Pinout MBa94xxCA connector X2

GPIO use	Muxing	TQ-Muxing	Pin	Pin	TQ-Muxing	Muxing	GPIO use
	ccmsrcgpcmix.CLKO4	CCM_CLKO4	A1	B1	CLKIN2	CLKIN2	
	ccmsrcgpcmix.CLKO3	CCM_CLKO3	A2	B2	CLKIN1	CLKIN1	
		GND	A3	B3	GND		
I2C-Switch Reset	gpio4.IO[1]	CCM_CLKO2	A4	B4	GPIO2_IO21	sai2.TX_BCLK	
	ccmsrcgpcmix.CLKO1	CCM_CLKO1	A5	B5	GPIO2_IO22	gpio2.IO[22]	PortEXP INT
		GND(FIXED)	A6	B6	GND(FIXED)		
IO State 1/2	gpio2.IO[4]	GPIO2_IO4	A7	B7	GPIO2_IO24	flexpwm4.PWMX[0]	
IO State 3/4	gpio2.IO[5]	GPIO2_IO5	A8	B8	GPIO2_IO23	pcie2.CLKREQ_B	
ETH T1S Interrupt	gpio2.IO[6]	GPIO2_IO6	A9	B9	GPIO2_IO20	pcie1.CLKREQ_B	
	spi3.PCS1	GPIO2_IO7	A10	B10	GPIO2_IO25	gpio2.IO[25]	Temp Event MB
		GND	A11	B11	GND		
	spi3.PCS0	GPIO2_IO8	A12	B12	GPIO2_IO12	uart8.TX	
	spi3.SIN	GPIO2_IO9	A13	B13	GPIO2_IO13	uart8.RX	
	spi3.SOUT	GPIO2_IO10	A14	B14	GPIO2_IO14	uart8.CTS_B	
	spi3.SCK	GPIO2_IO11	A15	B15	GPIO2_IO15	uart8.RTS_B	
		GND(FIXED)	A16	B16	GND(FIXED)		
	uart5.RTS_B	GPIO2_IO3	A17	B17	GPIO2_IO26	sai2.RX_DATA[0]	
	uart5.CTS_B	GPIO2_IO2	A18	B18	GPIO2_IO27	sai2.TX_DATA[0]	
	uart5.RX	GPIO2_IO1	A19	B19	GPIO2_IO28	sai2.TX_SYNC	
	uart5.TX	GPIO2_IO0	A20	B20	GPIO2_IO29	gpio2.IO[29]	Gyro INT 2
		FS0B	A21	B21	PGOOD		
	i2c3.SDA	GPIO2_IO16	A22	B22	GPIO2_IO30	uart3.TX	
	i2c3.SCL	GPIO2_IO17	A23	B23	GPIO2_IO31	uart3.RX	
	i2c4.SDA	GPIO2_IO18	A24	B24	GPIO3_IO0	gpio3.IO[0]	M.2 B Reset
	i2c4.SCL	GPIO2_IO19	A25	B25	GPIO3_IO1	gpio3.IO[1]	M.2 B DPR
		GND(FIXED)	A26	B26	GND(FIXED)		
	flexpwm3.PWMX[0]	GPIO3_IO6	A27	B27	GPIO3_IO5	gpio3.IO[5]	M.2 B Full Card Off
	uart3.RTS_B	GPIO3_IO7	A28	B28	GPIO3_IO4	gpio3.IO[4]	M.2 B W_Disable2
WiFi - DEV_WAKE_BT	gpio3.IO[8]	GPIO3_IO8	A29	B29	GPIO3_IO3	can2.RX	
WiFi - DEV_WAKE_WiFi	gpio3.IO[9]	GPIO3_IO9	A30	B30	GPIO3_IO2	can2.TX	
		GND	A31	B31	GND		
	sai3.TX_BCLK	GPIO3_IO10	A32	B32	GPIO3_IO16	usdhc3.CLK	
	sai3.RX_DATA[0]	GPIO3_IO14	A33	B33	GPIO3_IO17	usdhc3.CMD	
	sai3.RX_SYNC	GPIO3_IO13	A34	B34	GPIO3_IO18	usdhc3.DATA0	
	sai3.MCLK	GPIO3_IO11	A35	B35	GPIO3_IO19	usdhc3.DATA1	
		GND(FIXED)	A36	B36	GND(FIXED)		
	sai3.RX_BCLK	GPIO3_IO12	A37	B37	GPIO3_IO20	usdhc3.DATA2	
	sai3.TX_DATA[0]	GPIO3_IO15	A38	B38	GPIO3_IO21	usdhc3.DATA3	
		GND	A39	B39	GND		
	ETH5_RX0_N	ENET5_RX0-	A40	B40	ENET5_TX0-	ETH5_TX0_N	
	ETH5_RX0_P	ENET5_RX0+	A41	B41	ENET5_TX0+	ETH5_TX0_P	
		GND	A42	B42	GND		
	ETH6_RX1_N	ENET6_RX1-	A43	B43	ENET6_TX1-	ETH6_TX1_N	
	ETH6_RX1_P	ENET6_RX1+	A44	B44	ENET6_TX1+	ETH6_TX1_P	
		GND(FIXED)	A45	B45	GND(FIXED)		
WiFi - W_Disable1	gpio3.IO[22]	GPIO3_IO22	A46	B46	ETH_REF_PAD_CLK_P	ETH_REF_PAD_CLK_P	
WiFi - W_Disable2	gpio3.IO[23]	GPIO3_IO23	A47	B47	ETH_REF_PAD_CLK_N	ETH_REF_PAD_CLK_N	
	sai3.TX_SYNC	GPIO3_IO24	A48	B48	GND		
WiFi - PD	gpio3.IO[25]	GPIO3_IO25	A49	B49	V_GPIO	V_GPIO	
	usb1.OTG_PWR	ETH2_MDIO_GPIO2	A50	B50	Gyro_INT1	Gyro_INT1	
Button B	gpio6.IO[0]	ETH2_MDC_GPIO1	A51	B51	Gyro_INT2	Gyro_INT2	
		GND	A52	B52	GND		
	netc_pinmux.ETH2_RX_CLK	ETH2_RX_CLK	A53	B53	ETH2_TX_CLK	netc_pinmux.ETH2_TX_CLK	
	netc_pinmux.ETH2_RX_CTL	ETH2_RX_CTL	A54	B54	ETH2_TX_CTL	netc_pinmux.ETH2_TX_CTL	
		GND(FIXED)	A55	B55	GND(FIXED)		
	netc_pinmux.ETH2_RXD[3]	ETH2_RXD3	A56	B56	ETH2_TXD3	netc_pinmux.ETH2_TXD[3]	
	netc_pinmux.ETH2_RXD[2]	ETH2_RXD2	A57	B57	ETH2_TXD2	netc_pinmux.ETH2_TXD[2]	
	netc_pinmux.ETH2_RXD[1]	ETH2_RXD1	A58	B58	ETH2_TXD1	netc_pinmux.ETH2_TXD[1]	
	netc_pinmux.ETH2_RXD[0]	ETH2_RXD0	A59	B59	ETH2_TXD0	netc_pinmux.ETH2_TXD[0]	
		GND	A60	B60	GND		
FAN Alert	gpio5.IO[31]	ETH1_COL	A61	B61	ETH1_CRS	gpio5.IO[30]	FAN Enable
	netc_pinmux.ETH1_RX_DV	ETH1_RX_DV	A62	B62	ETH1_TX_EN	netc_pinmux.ETH1_TX_EN	
	netc_pinmux.ETH1_RX_ER	ETH1_RX_ER	A63	B63	ETH1_TX_ER	gpio5.IO[29]	M.2 M Alert
USB C Alert	gpio5.IO[27]	ETH1_RX_CLK	A64	B64	ETH1_TX_CLK	netc_pinmux.ETH1_TX_CLK	
		GND(FIXED)	A65	B65	GND(FIXED)		
	netc_pinmux.ETH1_RXD[0]	ETH1_RXD0	A66	B66	ETH1_TXD0	netc_pinmux.ETH1_TXD[0]	
	netc_pinmux.ETH1_RXD[1]	ETH1_RXD1	A67	B67	ETH1_TXD1	netc_pinmux.ETH1_TXD[1]	
	gpio5.IO[25]	GPIO5_IO25	A68	B68	ETH1_TXD2	gpio5.IO[23]	ECAT Phy #2 - RESET
	gpio5.IO[26]	ENET5_INT#	A69	B69	ETH1_TXD3	gpio5.IO[24]	ECAT Phy #2 - INT
		GND	A70	B70	GND		
12 V Enable	gpio5.IO[15]	ETH0_COL	A71	B71	ETH0_CRS	gpio5.IO[14]	2.5G Phy - INT
	netc_pinmux.ETH0_RX_DV	ETH0_RX_DV	A72	B72	ETH0_TX_EN	netc_pinmux.ETH0_TX_EN	
	netc_pinmux.ETH0_RX_ER	ETH0_RX_ER	A73	B73	ETH0_TX_ER	gpio5.IO[13]	SPE 1G Phy - INT
SPE 1G Phy - RESET	gpio5.IO[11]	ETH0_RX_CLK	A74	B74	ETH0_TX_CLK	netc_pinmux.ETH0_TX_CLK	
		GND(FIXED)	A75	B75	GND(FIXED)		
	netc_pinmux.ETH0_RXD[0]	ETH0_RXD0	A76	B76	ETH0_TXD0	netc_pinmux.ETH0_TXD[0]	
	netc_pinmux.ETH0_RXD[1]	ETH0_RXD1	A77	B77	ETH0_TXD1	netc_pinmux.ETH0_TXD[1]	
1G Phy #1 - RESET	gpio5.IO[9]	ETH0_RXD2	A78	B78	ETH0_TXD2	gpio5.IO[7]	ECAT Phy #1 - RESET
1G Phy #1 - INT	gpio5.IO[10]	ETH0_RXD3	A79	B79	ETH0_TXD3	gpio5.IO[8]	ECAT Phy #1 - INT
		GND	A80	B80	GND		

3.1.2 MBa94xxCA pinout (continued)

Table 6: Pinout MBa94xxCA connector X3

GPIO use	Muxing	TQ-Muxing	Pin	Pin	TQ-Muxing	Muxing	GPIO use
	TSE_ISO_14443_LA	TSE_ISO_14443_LA	A1	B1	V_BAT		
	TSE_ISO_14443_LB	TSE_ISO_14443_LB	A2	B2	GND		
		GND	A3	B3	SD2_CD_B	usdhc2.CD_B	
	TSE_ISO_7816_RST#	TSE_ISO_7816_RST#	A4	B4	SD2_RESET_B	Intern! + Pad	
	TSE_ISO_7816_CLK	TSE_ISO_7816_CLK	A5	B5	SD2_GPIO0	gpio4.IO[28]	LED1 / Attention V_SD!
		GND(FIXED)	A6	B6	GND(FIXED)		
	TSE_ISO_7816_IO2	TSE_ISO_7816_IO2	A7	B7	SD2_GPIO3	gpio4.IO[31]	M.2 M PEDET / Attention V_SD!
	TSE_ISO_7816_IO1	TSE_ISO_7816_IO1	A8	B8	SD2_GPIO2	gpio4.IO[30]	SFP MOD ABS / Attention V_SD!
	TEMP_EVENT#	TEMP_EVENT#	A9	B9	SD2_GPIO1	gpio4.IO[29]	LED2 / Attention V_SD!
	RTC_EVENT#	RTC_EVENT#	A10	B10	GND		
	IMX_ONOFF	IMX_ONOFF	A11	B11	SD2_DATA0	usdhc2.DATA0	
	Reset_OUT#	Reset_OUT#	A12	B12	SD2_DATA1	usdhc2.DATA1	
	wdog1.WDOG_ANY	WDOG_ANY	A13	B13	SD2_DATA2	usdhc2.DATA2	
	EEPROM_WC#	EEPROM_WC#	A14	B14	SD2_DATA3	usdhc2.DATA3	
	GND(FIXED)	GND(FIXED)	A15	B15	GND(FIXED)		
	POR#	POR#	A16	B16	SD2_CMD	usdhc2.CMD	
	JTAG_TDO	JTAG_TDO	A17	B17	SD2_CLK	usdhc2.CLK	
	JTAG_TDI	JTAG_TDI	A18	B18	GND		
	JTAG_TMS	JTAG_TMS	A19	B19	V_SD		
	JTAG_TCK	JTAG_TCK	A20	B20	V_3V3_SD		

3.2 Boot Mode configuration

The TQMa94xxLA can boot from different boot sources. The boot source is selected on the MBa94xxCA via DIP switches (S1). The following table shows the possible boot configurations of the i.MX 94, where Serial NAND is not supported by the TQMa94xxLA.

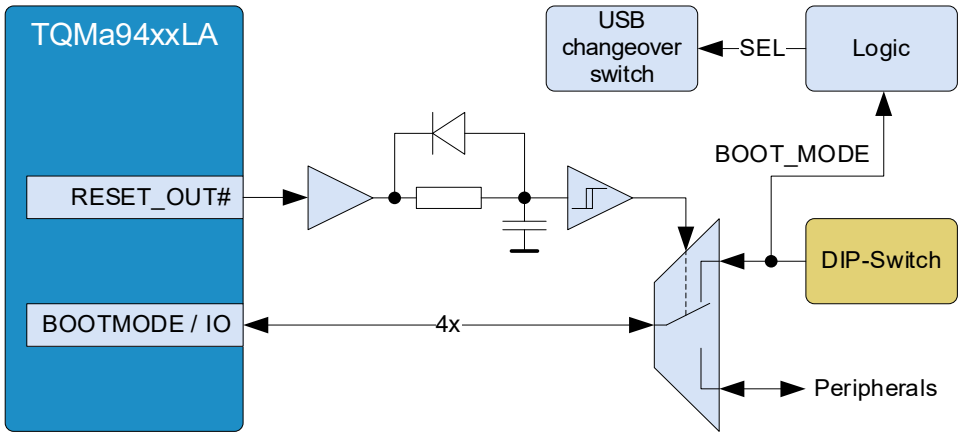

Figure 3: Block diagram boot mode

The four BOOT_MODE pins of the CPU are not dedicated pins but are multiplexed with functional IO pins. So that neither connected periphery influences the boot mode nor the boot configuration influences the connected periphery, the pins are switched via analog switch. The RESET_OUT# signal is used for toggling, which triggers the switch with a delay (approx. 5 ms) after RESET_OUT# has been released by the logic and RC element. The switch back to the DIP switch is done almost without delay at a low edge at RESET_OUT#.

At the BOOT_MODE signals 100 kΩ pull-down resistors are provided. The 1.8 V provided by the module are used as pull-up voltage for the switchable 4.7 kΩ resistors.

The BOOT_MODE signals are also used for the logic to switch from the USB1 interface to the USB Type-C interface.

Table 7: Boot Mode configuration

Boot-Mode	S1-4 (BM3)		S1-3 (BM2)		S1-2 (BM1)		S1-1 (BM0)		Remark
	Pos.	Level	Pos.	Level	Pos.	Level	Pos.	Level	
Boot from eFuses	OFF	0	OFF	0	OFF	0	OFF	0	–
Serial Downloader (USB 1)	OFF	0	OFF	0	OFF	0	ON	1	–
eMMC (uSDHC1)	OFF	0	OFF	0	ON	1	OFF	0	–
SD card (uSDHC2)	OFF	0	OFF	0	ON	1	ON	1	–
QSPI (FlexSPI Serial NOR)	OFF	0	ON	1	OFF	0	OFF	0	–

Note: Boot from NAND	
	Booting from NAND is not supported on the MBa94xxCA.

3.3 I²C Mapping

Due to the large number of I²C devices connected to the TQMa94xxLA, special attention must be paid to the I²C addresses already in use. Depending on the application and software load the number of used I2C devices may limit the data throughput or block the bus.

The following table shows the default I²C device addresses on the MBa94xxCA and the TQMa94xxLA.

For some devices the address can be changed by assembly options. The options are described in detail in the given chapter.

Table 8: I²C mapping

Bus	Assembly	Device	Address	Note
I2C1	TQMa94xxLA	PMIC PF9455	0x08	available on the pin header
		PMIC PF5302	0x29	
		Temperature sensor	0x4A	
		TQ-EEPROM	0x50	
	MBa94xxCA	Port expander (Wake-up)	0x70	
		Starter kit pin header	NA	
I2C2	TQMa94xxLA	EEPROM	0x50	available on the pin header
		RTC	0x32	
		TSE	0x48	
		Gyroscope	0x6B	
	MBa94xxCA	Starter kit pin header	NA	
I2C3	MBa94xxCA	[Allg] I²C switch	0x77	available on the pin header
		[CH0] SMBUS alert response	0x0C	
		[CH0] USB-C PD-Controller	0x53	
		[CH0] Temperature sensor (temperature)	0x1E	
		[CH0] Temperature sensor (EEPROM)	0x56	
		[CH0] Temperature sensor (software protection)	0x36	
		[CH0] Port expander #1	0x70	
		[CH0] Port expander #2	0x71	
		[CH0] Port expander #3	0x72	
		[CH0] PCIE clock generator	0x68	
		[CH0] USB hub TUSB8041 (SMBus)	0x44 [1]	
		[CH0] USB hub USB2514 (SMbus)	0x2C	
		[CH0] Fan controller	0x2F	
		[CH1] M.2 Key M socket	NA	
		[CH1] Starter kit pin header	NA	
I2C4	MBa94xxCA	Starter kit pin header	NA	available on the pin header

[1] Depending on how the strap pins are configured for other options, addresses 0x45…0x47 may also be in use.

Note: I²C address conflicts	
	When changing the address due to assembly options or when connecting further I²C components, it must be ensured that no address conflicts occur. Otherwise malfunctions may occur. The addresses preassigned by the TQMa94xxLA must also be observed (depending on the TQMa94xxLA variant used).

3.4 GPIO port expander

Due to the limited number of GPIO pins available on the TQMa94xxLA IO expanders are required to provide the necessary signals. A total of four I2C IO expanders are used on the MBa94xxCA. Only IO signals that need to be processed directly by the CPU (e.g. Interrupts, Timer IOs, PWM signals) are connected to the TQMa94xxLA. All other control signals are connected to the IO expanders.

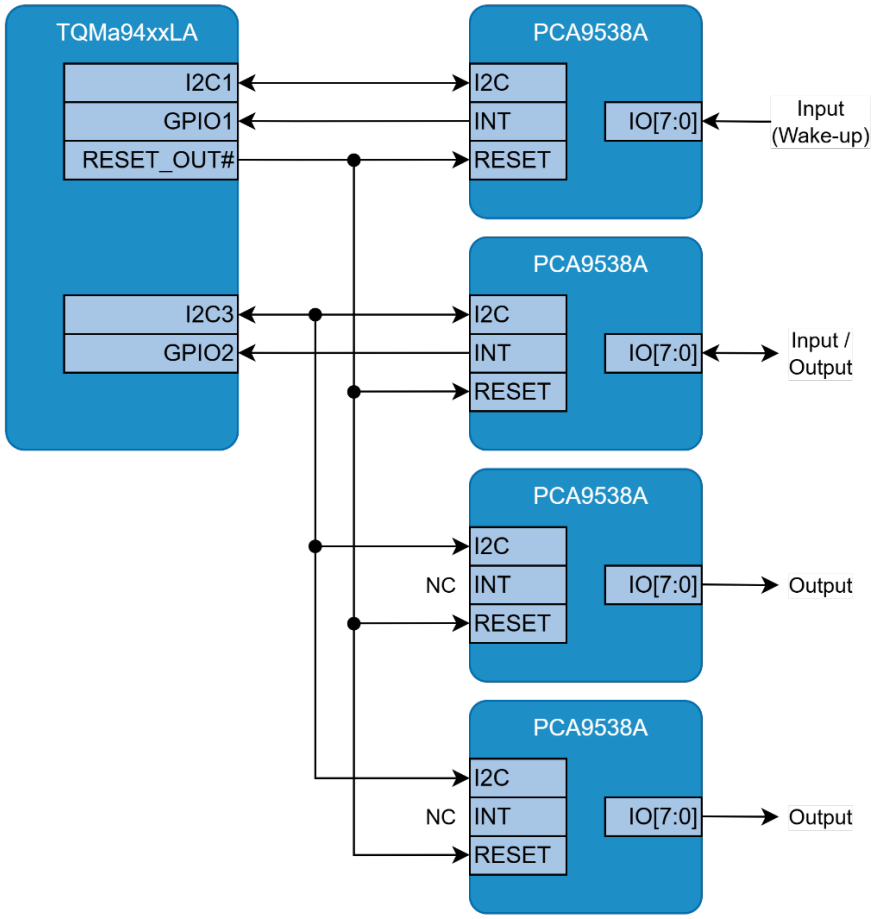

Figure 4: Block diagram GPIO expander

Signals that can be used to wake up the CPU are connected to an 8-port expander. This is connected to I2C1. The interrupt signal from the expander is connected to a CPU input of the GPIO1 group. This group, which also includes the I2C1 signals, is in the always-on domain, which remains active when the i.MX94 is in low-power mode. This allows the system to be reactivated with the wake-up signals.

Three further expanders on I2C3, each with 8 ports, are used for outputs and non-critical inputs. The input signals are connected to only one of the expanders and its interrupt signal is connected to a CPU input of the GPIO2 group. The other two expanders are used for outputs only. The interrupt pin of these two expanders is not connected to the CPU.

The IO expanders used have a reset input connected to RESET_OUT#. This resets all signals when the CPU is reset (High-Z).

3.5 Temperature sensor and EEPROM

A temperature sensor SE97BTP is populated on the MBa94xxCA to monitor the temperature. The sensor is read out via I2C3 and operates at 3.3 V.

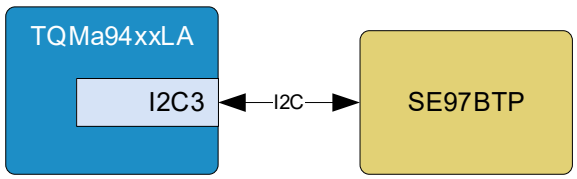

Figure 5: Block diagram temperature sensor

The sensor address on the MBa94xxCA can be changed by reassembling resistors (default `0b100`). When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 8. The assembly options are documented in the MBa94xxCA schematics.
The SE97BTP has an additional EEPROM to store revision data and/or data regarding the motherboard components . Further specifications of the SE97BTP can be found in the data sheet.

The sensor's EVENT# output is connected to a GPIO pin on the TQMa94xxLA.

3.6 RTC backup

The TQMa94xxLA has an optional RTC. It is supplied via pin V_BAT.
On the MBa94xxCA there are two possibilities to supply the V_BAT input [1]:

- CR2032-Battery holder (X34)
- 2-pin header (X32) for alternative connection of an external voltage or batteries

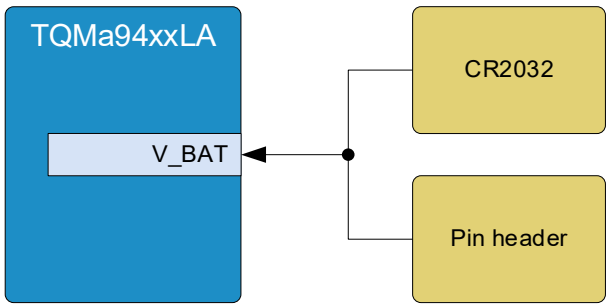

Figure 6: Block diagram RTC backup

Table 9: Pinout RTC backup (X32 & X34)

Pin	Signal	Level	Remark
1	V_BAT	3 V	Supply voltage for RTC on TQMa94xxLA
2	GND	0 V	Ground

To meet regulatory requirements for protection against accidental battery charging, a 1 kΩ resistor and diode is connected in series between X32/X34 and the V_BAT input of the TQMa94xxLA.

1: Only one of the two options may be used at a time!

The diode has a very low forward voltage (<0.1 V) in order not to unnecessarily reduce the battery runtime and a very low reverse current to keep residual charging currents as low as possible.

3.7 USB hub

The USB interfaces are implemented by cascading two USB hubs. The 4-port USB 3.0 hub TUSB8041 provides the USB 3.0 interfaces for the two USB host sockets and the M.2 Key B interface. Downstream, the USB2514 4-port USB 2.0 hub provides the USB 2.0 interfaces for the M.2 Key M interface, the LVDS-CMD connector and the starter kit pin header.

The USB 3.0 hub is connected to the USB1 port and the USB_SS signals of the CPU. The USB 2.0 signals of the CPU's USB1 port are also switched to the USB Type-C interface to enable booting from the Serial Downloader.

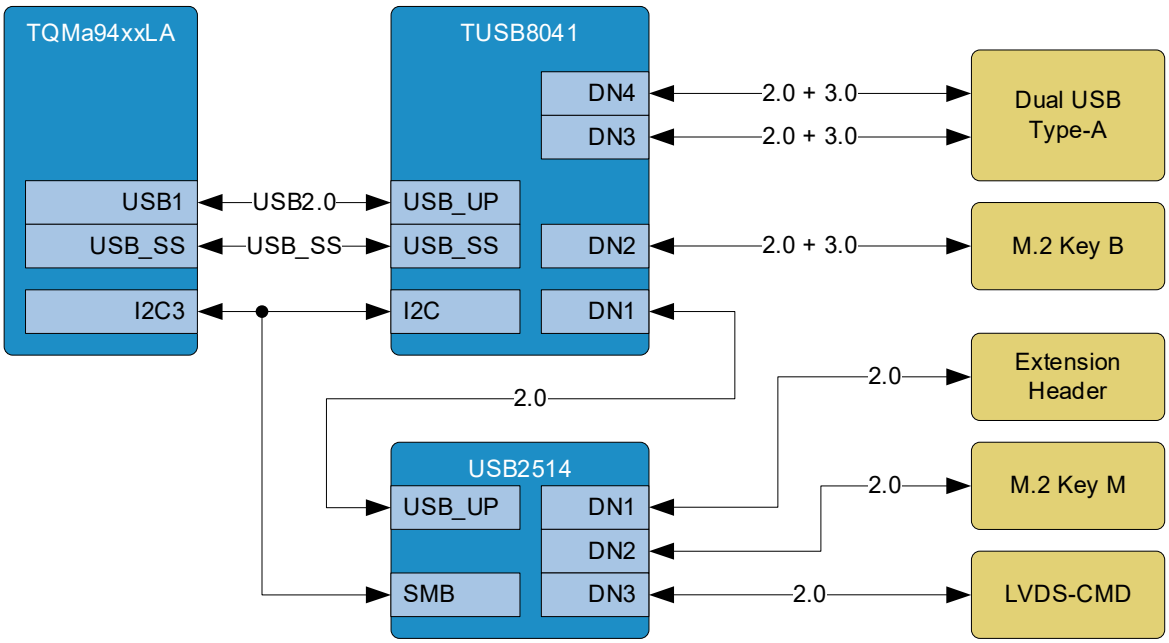

Figure 7: Block diagram USB hub

As the USB 2.0 signals of the USB1 port are switched to the Type C interface when using the Serial Downloader, the voltage on USB1_VBUS must also be controlled by this interface in this case. For this purpose, the processed VBUS signal from USB Type C is linked by logic with the SEL_USB signal, which switches the USB signals in Serial Downloader mode, and used for control. The detection signal on USB2_VBUS is deactivated in this case.

3.8 CAN-FD

The MBa94xxCA features two CAN interfaces that comply with the ISO 11898 standard. The signals are provided via a 3-pin connector in each case.

The interfaces are electrically isolated with an isolation voltage of 1 kV. The two CAN interfaces are not isolated from each other. CAN termination is configured via a DIP switch.

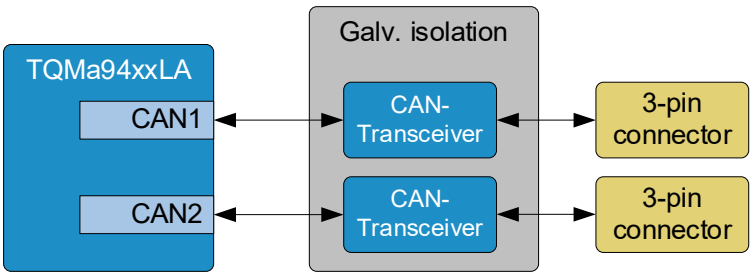

Figure 8: Block diagram CAN

The CAN signals can be terminated with DIP switches S6 (CAN1) and S7 (CAN2).

Table 10: CAN termination with S6/S7

Sx-1	Sx-2	Mode
OFF	OFF	No termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Termination with 120 Ω

Table 11: Pinout CAN1 / 2 (X13, X14)

CAN	Pin	Signal	Dir.	Level	Remark
CAN0	1	CAN0_H	I/O	Spec. (1)	CAN High-Level I/O from CAN0 / galvanically isolated
	2	CAN0_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN0 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated
CAN1	1	CAN1_H	I/O	Spec. (1)	CAN High-Level I/O from CAN1 / galvanically isolated
	2	CAN1_L	I/O	Spec. (1)	CAN Low-Level I/O from CAN1 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated

3.9 Debug USB / UART

For debug purposes, two UARTs of the i.MX94 CPU are made available at USB socket X26 by using an UART-USB-Bridge. UART1 and UART2 are used for this purpose. Both are in the NVCC_AON power domain.

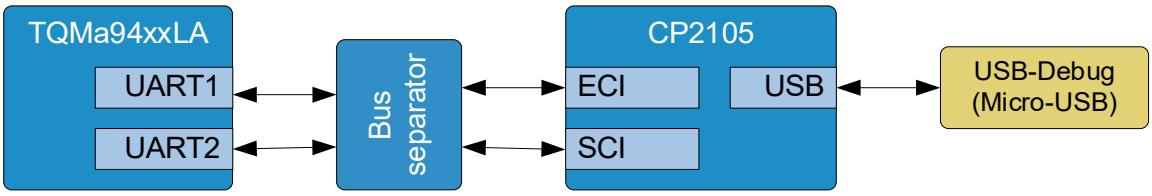

Figure 9: Block diagram USB debug

3.10 Ethernet

The i.MX 94 CPU provides a total of seven physical Ethernet ports; however, not all of them can be used simultaneously within the CPU. Since the ports have different functionalities and support different data rates, all seven are provided as separate interfaces on the MBa94xxCA. All ports are TSN-capable.

All the PHYs in use are connected to the same management interface. The following table shows the address mapping for each PHY.

Table 12: Address mapping of the Ethernet PHYs

Bus	Device	Address	Note
ETHx_SLV_MDIO/MDC	DP83867 #1	0x02	1Gb (ETH4)
	DP83867 #2	0x01	1Gb (ETH2)
	DP83826 #1	0x03	EtherCAT (ETH0)
	DP83826 #2	0x07	EtherCAT (ETH1)
	DP83TG721	0x05	SPE (ETH3)
	GPY215 #1	0x04	2.5Gb (SGMII, ETH6)
	GPY215 #2	0x06	2.5Gb (SGMII, ETH5)

1: According to CAN standard.

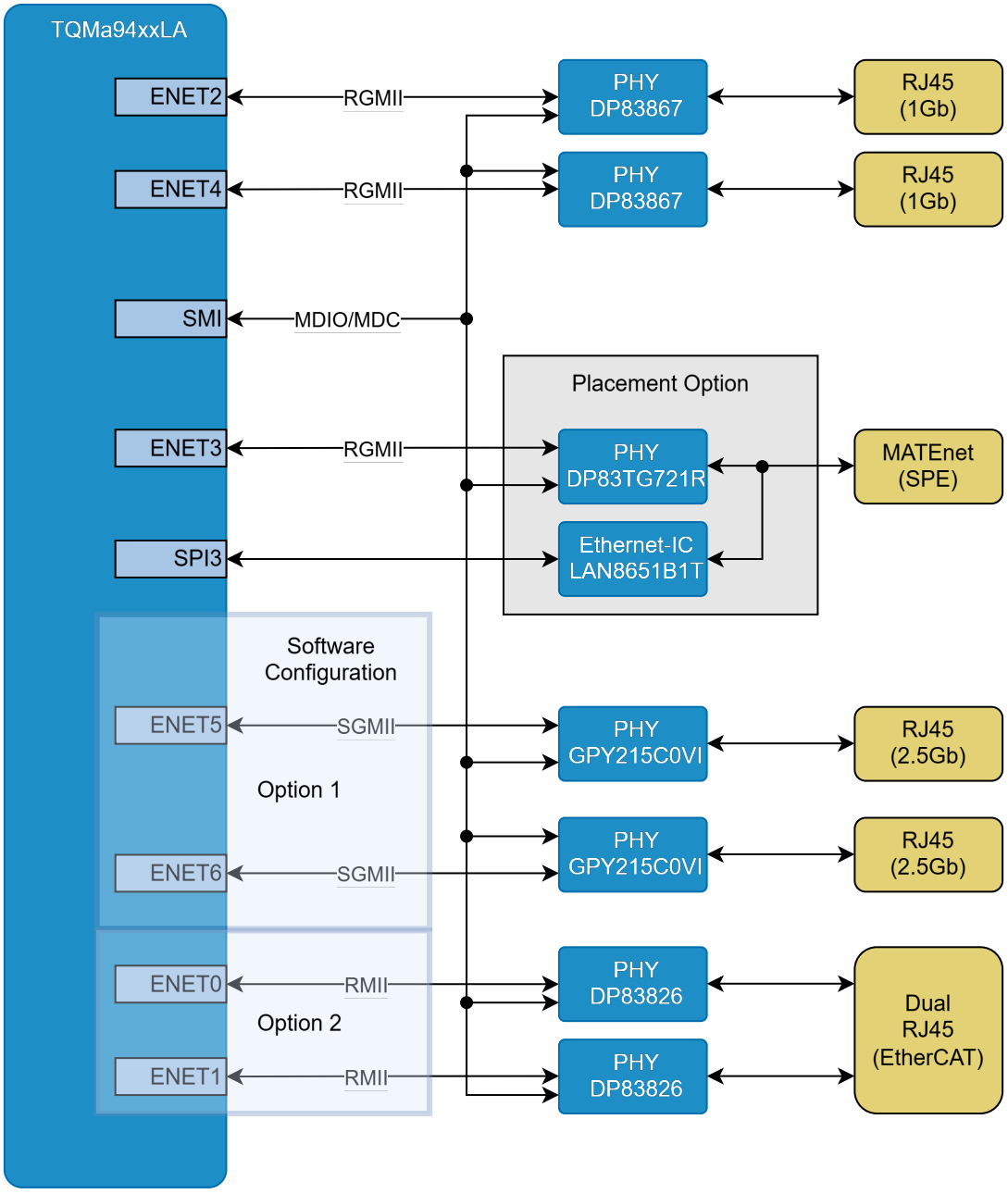

Figure 10: Block diagram Ethernet

3.10.1 1Gb Ethernet

Two of the i.MX 94 processor's RGMII interfaces are provided as 1 Gb interfaces on RJ45 sockets with Time Sensitive Network (TSN) features.

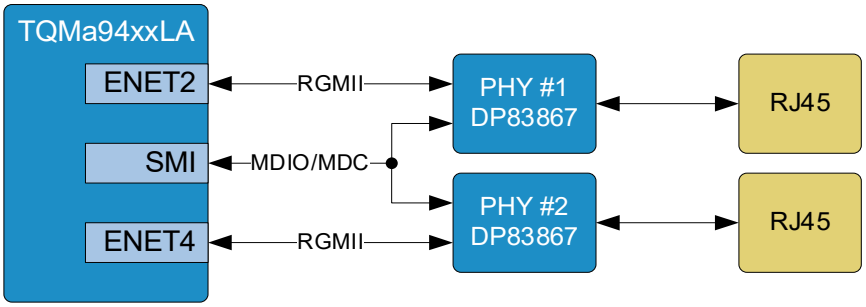

Figure 11: Block diagram 1G Ethernet

The used PHY DP83867 is TSN compliant. However, the required TSN features are mainly on the MAC and application level. The DP83867 has configurable GPIO signals that can be used as SFD (Start of Frame) detection outputs for debugging purposes. For Ethernet1 interface, these signals are provided on solder pads (X31) on the MBa94xxCA.

3.10.2 2.5Gb Ethernet

The CPU's 2.5 Gb Ethernet interfaces are implemented as SGMII and are wired identically.

Both interfaces use RJ45 sockets.

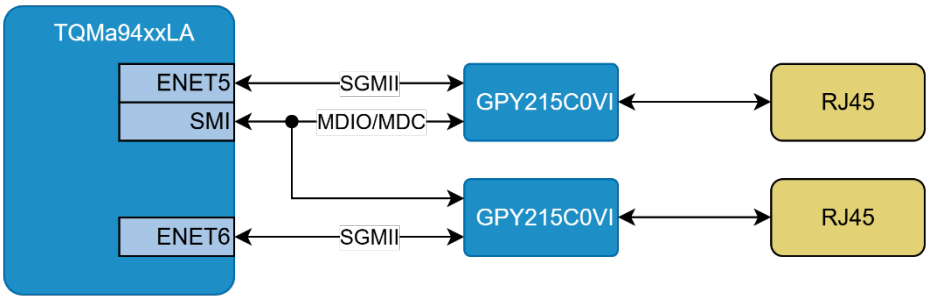

Figure 12: Block diagram 2.5G Ethernet

3.10.3 Single Pair Ethernet (SPE)

The SPE interface's default configuration is a 1000BASE-T1 interface without multidrop capability. The PHY connects to the CPU via RGMII.

To provide a 10BASE-T1S connection with multidrop capability, an optional Ethernet controller with an integrated MAC and PHY for 10BASE-T1S can be connected to a SPI interface of the i.MX 94. This replaces the 1000BASE-T1 interface.

Currently, the 10BASE-T1S SPE standard is the only one that provides multidrop capability. This facilitates, for instance, the communication of multiple sensors within a bus structure with a singular master. However, the data rate is comparatively low at a maximum of 10 Mbit/s.

Both SPE interfaces use a common MATEnet connector via an optional placement configuration.

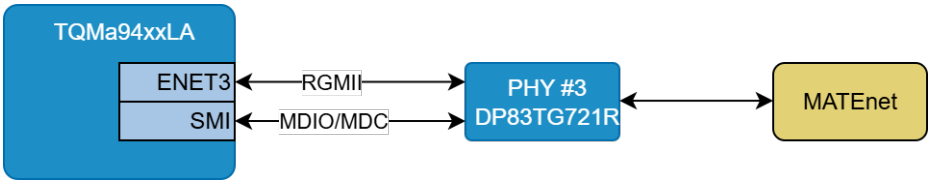

Figure 13: Block diagram SPE

3.10.4 EtherCAT

The i.MX 94 provides up to two EtherCAT-capable Ethernet ports. EtherCAT-capable PHYs are connected to these ports via RMII. The interfaces are provided via RJ45 sockets.

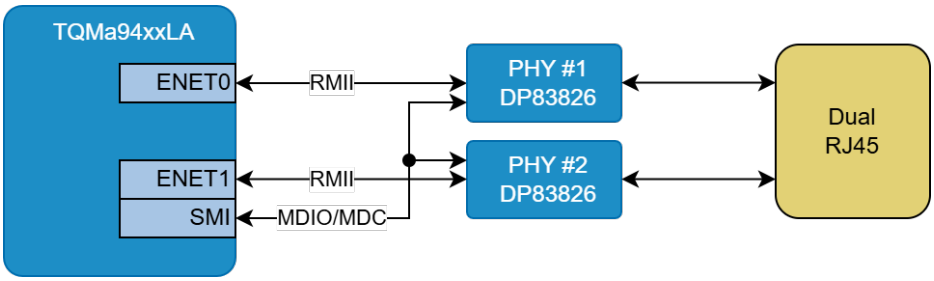

Figure 14: Block diagram EtherCAT

3.11 WiFi

The JODY-W377 solder-in module from u-blox is used to implement the Wi-Fi 6 interface. The module is connected to the TQMa94 via SDIO for Wi-Fi and UART for PAN. Additionally, I2S is used for PAN. For various control signals, GPIO signals are used, either from the CPU or from an IO expander. Three U.FL sockets are provided for connecting antennas.

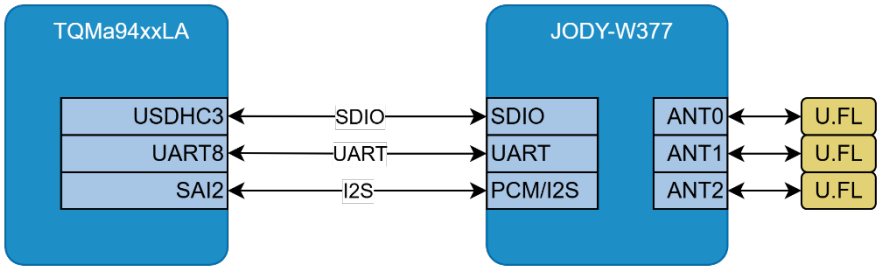

Figure 15: Block diagram WiFi

3.12 LVDS

The i.MX 94 processor has one LVDS interfaces with four lanes on one connector (X19). The MBa94xxCA also has an additional CMD connector (X20) which provides power, USB, and display/backlight control signals.

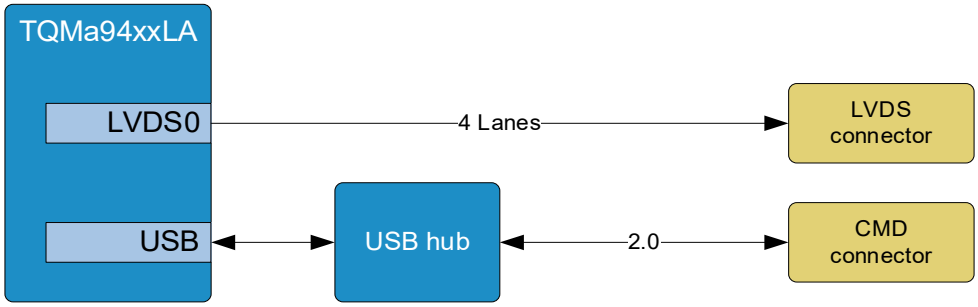

Figure 16: Block diagram LVDS

Table 13: Pinout LVDS Data (X19)

Pin	Signal	Dir.	Level	Remark
1	LVDS0_DATA0–	O	1.8 V	LVDS0 interface (Lane 0)
2	LVDS0_DATA0+	O	1.8 V	
3	LVDS0_DATA1–	O	1.8 V	LVDS0 interface (Lane 1)
4	LVDS0_DATA1+	O	1.8 V	
5	LVDS0_DATA2–	O	1.8 V	LVDS0 interface (Lane 2)
6	LVDS0_DATA2+	O	1.8 V	
7	GND	P	0 V	Ground
8	LVDS0_CLOCK–	O	1.8 V	LVDS0 interface (Clock)
9	LVDS0_CLOCK+	O	1.8 V	
10	LVDS0_DATA3–	O	1.8 V	LVDS0 interface (Lane 3)
11	LVDS0_DATA3+	O	1.8 V	
12	NC			
13				
14	GND	P	0 V	Ground
15	NC			
16				
17	GND	P	0 V	Ground
18	NC			
19				
20				
21				
22				
23				
24	GND	P	0 V	Ground
25	V_5V_LVDS	P	5 V	5 V supply voltage (1.0 A max. output)
26				
27				
28	V_3V3_LVDS	P	3.3 V	3.3 V supply voltage (1.0 A max. output)
29				
30				
M1, M2	GND	P	0 V	Ground

Table 14: Pinout LVDS CMD (X20)

Pin	Signal	Dir.	Level	Remark
1	V_12V	P	12 V	12 V supply voltage (2.5 A max.)
2				
3				
4	GND	P	0 V	Ground
5				
6				
7	V_5V_MB	P	5 V	5 V supply voltage (1.0 A max.)
8				
9	GND	P	0 V	Ground
10				
11	V_VBUS_H7	P	5 V	VBUS USB Host 7 (0.8 A max.)
12	GND	P	0 V	Ground
13	USBH7_D–	I/O	3.3 V	Data USB Host 7
14	USBH7_D+	I/O	3.3 V	
15	GND	P	0 V	Ground
16	LCD_RESET#	O_{PD}	3.3 V	Reset
17	LCD_BLT_EN	O_{PD}	3.3 V	Backlight-Enable
18	LCD_PWR_EN	O_{PD}	3.3 V	Power-Enable
19	LCD_PWM	O	3.3 V	PWM Contrast-/ Brightness
20	GND	P	0 V	Ground
M1, M2				

3.13 M.2 interfaces

Two M.2 slots with PCIe are provided. One is intended for cellular connectivity, and the other for storage solutions. Key B is required for cellular connectivity. NVMe SSDs that use Key M are suitable as storage solutions with a PCIe interface.

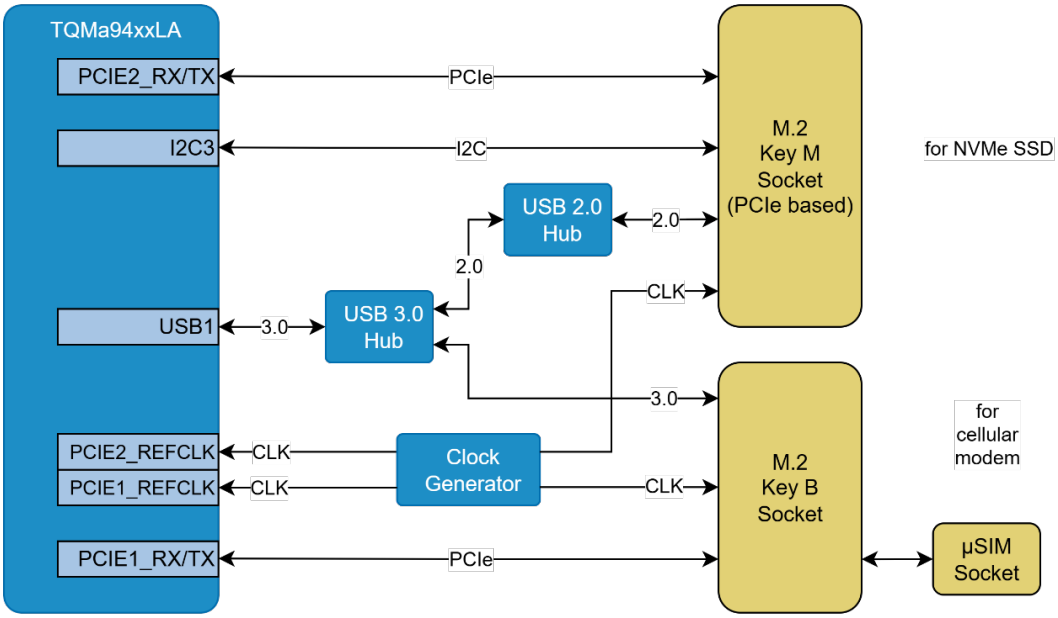

Figure 17: Block diagram M.2

3.14 SIM card

A Micro-SIM card holder (X18) is available on the MBa94xxCA for the use of a SIM card, which is directly connected to the M.2 Key B slot.

3.15 USB Host

The required USB interfaces for the host ports are provided by the USB hub (see chapter 3.7). VBUS with max. 900 mA each is provided at the double-decker USB type A host connector. The current limit is internally set to typ. 1.5 A, the recommended maximum continuous current is 1 A.

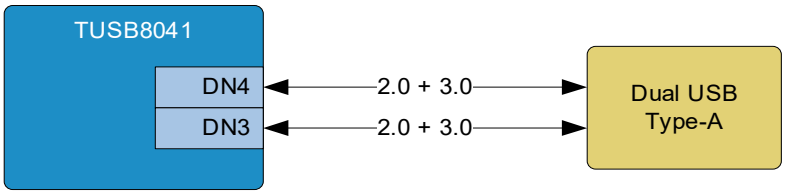

Figure 18: Block diagram USB Host

3.16 USB Type-C

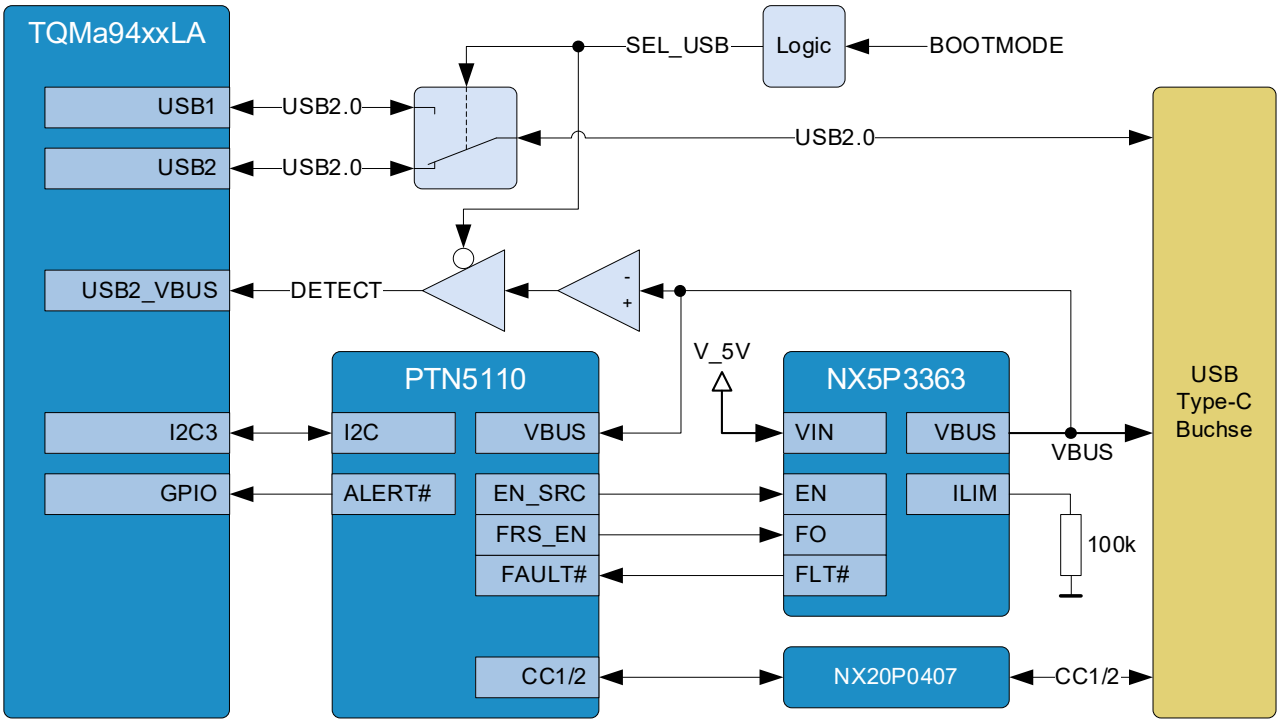

Figure 19: Block diagram USB Type-C

The USB Type-C interface is connected to the USB2 interface of the CPU by default. This means that the connector X9 is used for USB 2.0 signals only. However, as this interface should also be available for the serial downloader, the USB 2.0 signals of the USB1 interface of the CPU are routed to the socket via an analog switch in serial downloader mode. USB2 is not supported by the serial downloader. To switch over, the BOOTMODE signals are logically linked and sent to the analog switch as a control signal.

Table 15: Logic USB Type-C port

BOOT_MODE[3:0]	USB Port	Boot Device
x001	USB1	Serial Downloader
xxx0	USB2	other Boot Devices
x011		
x101		
x111		

3.17 Micro-SD card

The micro SD card connector (X7) is directly connected to the uSDHC2 interface of the TQMa94xxLA. A 4-bit wide data interface is used. The uSDHC controller in the i.MX94 supports UHS-I mode.

The switching of the IO voltage is performed by the module-internal signal SD2_VSELECT. The SD card is supplied with V_3V3_SD, which is provided by the TQMa94xxLA.

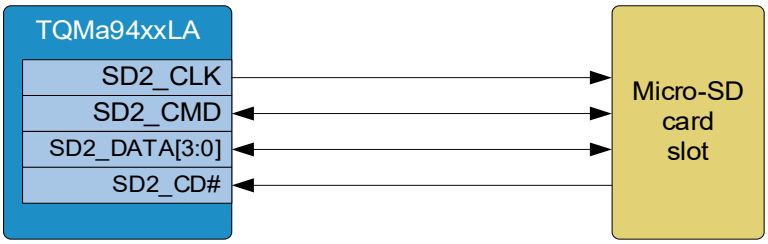

Figure 20: Block diagram Micro-SD card

3.18 RS485

On the MBa94xxCA, a RS485 interface (halfduplex) is realized. This interface is not galvanically isolated. It is connected to the UART3 interface of the TQMa94xxLA. The RTS signal of the UART interface (possibly used as GPIO) is used for automatic direction switching.

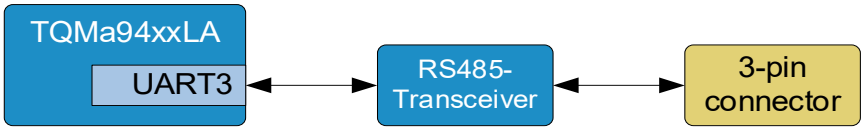

Figure 21: Block diagram RS485

The bus termination for RS485 is done via DIP switch S8. By default the termination (120 Ω) components are equiped to use it for RS485 bus. There is an assembly option to use a Profibus compliant termination (220 Ω). The assembly option is documented in the MBa94xxCA schematic.

The RS485 Bus is provided at a 3-pin connector.

Table 16: Pinout RS485 (X15)

Pin	Signal
1	RS485_A
2	RS485_B
3	GND

Table 17: Termination switch S8

S8-1	S8-2	Modus
OFF	OFF	No bus termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Bus terminated

3.19 MBa94xxCA Extension Headers (X4, X5, X6)

The MBa94xxCA provides three 100 mil headers. In addition to the signals, 1.8 V, 3.3 V, 5 V and 12 V are available on the headers. The maximum current is divided among all pin headers as well as the connectors of LVDS and analog input. In total, no more than the specified maximum current may be drawn at the following interfaces:

Table 18: Power consumption headers

Rail	I_{max}	Remark
V_12V	2.5 A	Sum of currents at X4, X5, X20, X30
V_5V_MB	1.5 A	Sum of currents at X4, X5, X19, X20, (X30)
V_3V3	1.5 A	Sum of currents at X4, X5, X19
V_1V8	250 mA	Sum of currents at X4, X5, X6

Note: Observe power consumption with regard to the overall system



The supply voltages (1.8 V, 12 V, etc.) provided at the MBa94xxCA headers are not individually fused. Technically, an overload of the fuse at the 24 V supply input is therefore possible, see also chapter 3.25.

Please note the resulting total current consumption of the MBa94xxCA, which must be less than 5 A!

Table 19: Pinout extension header X4

Level	Signal	Pin		Signal	Level
12 V	V_12V	1	2	V_3V3_MB	3.3 V
5 V	V_5V_MB	3	4	V_1V8	1.8 V
0 V	GND	5	6	GND	0 V
1.8 V	XSPI_DATA4	7	8	XSPI_DATA0	1.8 V
1.8 V	XSPI_DATA5	9	10	XSPI_DATA1	1.8 V
1.8 V	XSPI_DATA6	11	12	XSPI_DATA2	1.8 V
1.8 V	XSPI_DATA7	13	14	XSPI_DATA3	1.8 V
1.8 V	XSPI_SS1#	15	16	XSPI_DQS	1.8 V
1.8 V	XSPI_SS0#	17	18	XSPI_SCLK	1.8 V
0 V	GND	19	20	GND	0 V
1.8 V	I2C1_1V8_SDA	21	22	TSE_ISO_7816_CLK	1.8 V
1.8 V	I2C1_1V8_SCL	23	24	TSE_ISO_7816_IO2	1.8 V
1.8 V	I2C2_1V8_SDA	25	26	TSE_ISO_7816_IO1	1.8 V
1.8 V	I2C2_1V8_SCL	27	28	TSE_ISO_7816_RST#	1.8 V
0 V	GND	29	30	TAMPER0	1.8 V
3.3 V	RESET_OUT#	31	32	TAMPER1	1.8 V
1.8 V	WDOG_ANY	33	34	GND	0 V
1.8 V	IMX_ONOFF	35	36	USB_H5_D+	V_VBUS_H5
1.8 V	EEPROM_WC_MOD#	37	38	USB_H5_D-	V_VBUS_H5
V_SD	SD2_GPIO2	39	40	V_VBUS_H5	V_VBUS_H5

Table 20: Pinout extension header X5

Level	Signal	Pin		Signal	Level
12 V	V_12V	1	2	V_3V3	3.3 V
5 V	V_5V_MB	3	4	V_1V8	1.8 V
0 V	GND	5	6	GND	0 V
1.8 V	CLKO1	7	8	CLK_IN1	1.8 V
1.8 V	CLKO3	9	10	CLK_IN2	1.8 V
1.8 V	CLKO4	11	12	GND	0 V
-	RFU	13	14	SPI3_PCS0#	1.8 V
0 V	GND	15	16	SPI3_PCS1#	1.8 V
1.8 V	UART5_TX	17	18	SPI3_SIN	1.8 V
1.8 V	UART5_RX	19	20	SPI3_SOUT	1.8 V
1.8 V	UART5_CTS#	21	22	SPI3_SCLK	1.8 V
1.8 V	UART5_RTS#	23	24	GND	0 V
0 V	GND	25	26	I2C4_SCL	1.8 V
1.8 V	SAI3_MCLK	27	28	I2C4_SDA	1.8 V
1.8 V	SAI3_TX_BCLK	29	30	I2C3_1V8_SCL	1.8 V
1.8 V	SAI3_TXD0	31	32	I2C3_1V8_SDA	1.8 V
1.8 V	SAI3_TX_SYNC	33	34	HEADER_PWM	1.8 V
1.8 V	SAI3_RX_SYNC	35	36	GND	0 V
1.8 V	SAI3_RXD0	37	38	GPIO5_IO25	1.8 V
1.8 V	SAI3_RX_BCLK	39	40	M33_NMI	1.8 V

Table 21: Pinout extension header X6

Level	Signal	Pin		Signal	Level
1.8 V	V_1V8_A	1	2	V_1V8_A	1.8 V
1.8 V	ADC_IN2	3	4	ADC_IN5	1.8 V
1.8 V	ADC_IN3	5	6	ADC_IN6	1.8 V
1.8 V	ADC_IN4	7	8	ADC_IN7	1.8 V
0 V	GND	9	10	GND	0 V

3.20 IO Header X25

The X25 pin header provides an IO extension with four digital inputs, four digital outputs, and two analog inputs designed for higher voltages (up to 32 V).

Table 22: Threshold digital inputs

Threshold	min.	typ.	max.
Positive	-	11.25 V	13.86 V
Negative	3.35 V	6.19 V	-

Table 23: Pinout IO header X25

Level	Signal	Pin		Signal	Level
U = 16…32 V I = 2 A (max.)	V_24V_OUT	B1	A1	GND	0 V
		B2	A2		
U = 16…32 V I = 2 A (max.)	V_HSS_IN	B3	A3		
		B4	A4		
0 V	GND	B5	A5		
V_HSS_IN (max. 500 mA per channel)	DIG_OUT_1	B6	A6		
	DIG_OUT_2	B7	A7		
	DIG_OUT_3	B8	A8		
	DIG_OUT_4	B9	A9		
max. 32 V	DIG_IN_1	B10	A10		
	DIG_IN_2	B11	A11		
	DIG_IN_3	B12	A12		
	DIG_IN_4	B13	A13		
0…V_24V_IN (16…32 V)	ANA_IN1	B14	A14		
	ANA_IN2	B15	A15		

3.21 JTAG

The JTAG interface is routed to a 10-pin header (X27). All signal lines use 1.8 V as reference voltage. The JTAG interface is not ESD protected.

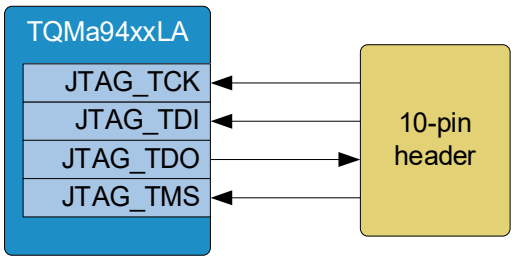

Figure 22: Block diagram JTAG

Table 24: Pinout JTAG (X20)

Remark	Level	Dir.	Signal	Pin	Pin	Signal	Dir.	Level	Remark
Test Mode Select	1.8 V	I_{PU}	JTAG_TMS	2	1	V_1V8	P	1.8 V	1.8 V
Test Clock	1.8 V	I_{PD}	JTAG_TCK	4	3	GND	P	0 V	Ground
Test Data Out	1.8 V	O	JTAG_TDO	6	5	GND	P	0 V	Ground
Test Data In	1.8 V	I_{PU}	JTAG_TDI	8	7	(NC)	–	–	Not used
Not used	-	-	(NC)	10	9	GND	P	0 V	Pulled to ground

3.22 Fan

If active cooling of the TQ module is required, a fan connector is provided. The fan is controlled by a fan controller. The fan connector has both a PWM and a tacho signal. The fan is connected to a 4-pin Molex connector and is supplied with 12 V as standard. Optionally, 5 V can be used via placement option. The fan is mounted on the optional heat sink of the TQMa94xxLA. Mounting holes are provided on the mainboard.

Table 25: Pinout fan header

Signal	Pin
GND	1
V_FAN	2
RPM	3
PWM	4

3.23 Status LEDs

Several LEDs are provided on the MBa94xxCA. In addition to an LED for RESET_OUT# and LEDs on the M.2 sockets, there are two user LEDs that can be controlled via IO expanders. Furthermore, one LED is provided on each of the main voltage rails and the VBUS voltages of all USB ports. These LEDs signal to the user that the voltages have reached the typical end value and facilitate development on the MBa94xxCA as well as troubleshooting.

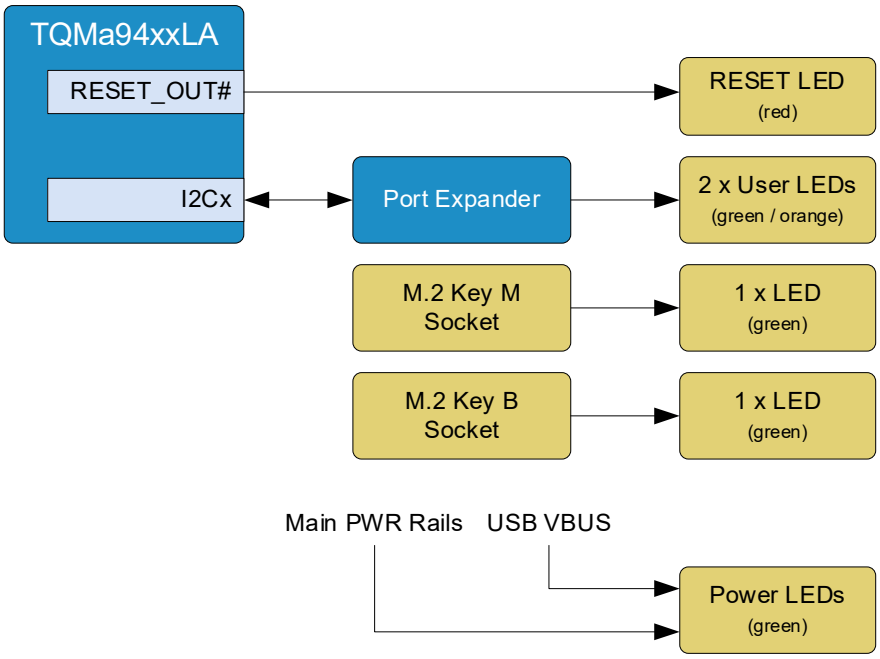

Figure 23: Block diagram Status LEDs

3.24 User Buttons

Two short-stroke keys are provided for simple user input. One of the buttons is connected to the IO expander for the wake-up signals, and the other button is connected to a GPIO pin on the TQMa94xxLA.

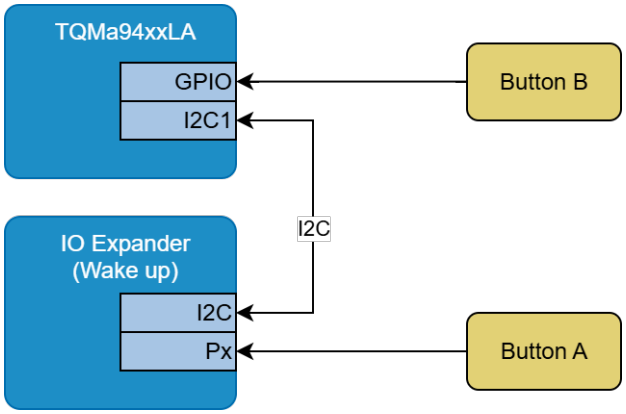

Figure 24: Block diagram User Buttons

3.25 Power supply

The MBa94xxCA must be supplied with 24 V DC (typ.) via one of the two connections X28 and X29, which can be used alternatively.

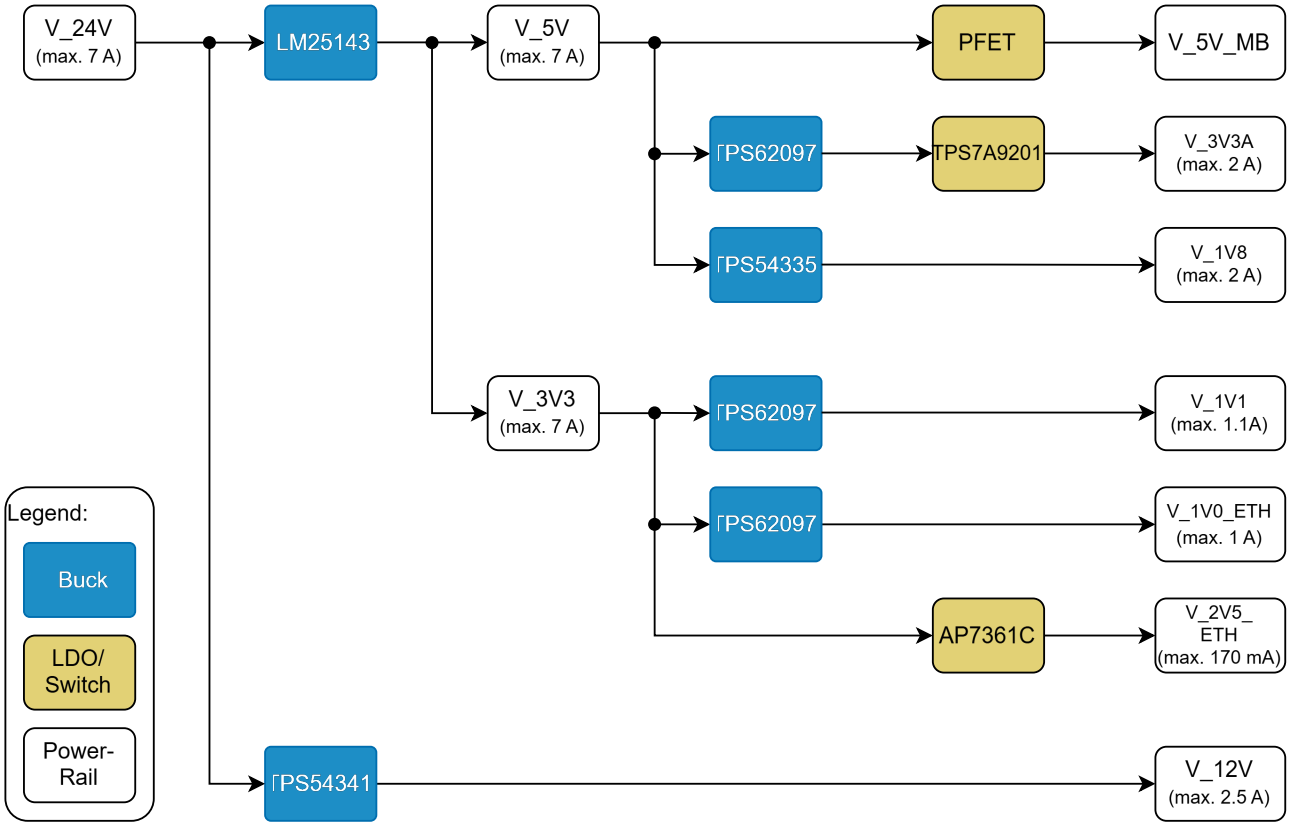

Figure 25: Block diagram MBa94xxCA power supply

Figure 25 shows all voltages (rails) on the MBa94xxCA, which are divided into two main paths consisting of a LM25143 and a TPS54341. These supply the largest loads (TQMa94xxLA, USB supply, 12 V, display supply and M.2 modules).

The design also allows power sequencing of all voltage levels used. With the exception of V_5V, all voltages are switched on after the TQMa94xxLA boots.

3.25.1 Input protection

The following protective circuits are provided for the input voltage V_24V (16…32 V) of the MBa94xxCA:

- Fuse 7 A, slow blow
- Overvoltage protection
- PI Filter (CLC element)
- Reverse polarity protection
- Voltage stabilization

Attention: Voltages at headers	
	The internal voltages (1.8 V, 12 V, etc.) provided at the MBa94xxCA headers are not separately fused. Technically an overload of the fuse is therefore possible. The resulting total current consumption of the MBa94xxCA should be kept below 7 A in total.

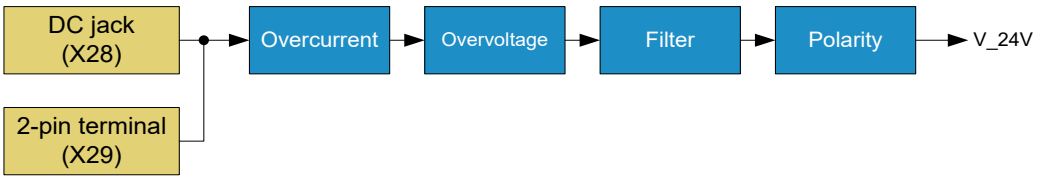

Figure 26: Block diagram Power-In

Table 26: Supply voltage V_24V_IN at Power-In (X28, X29)

Parameter	Min.	Typ.	Max.	Remark
Input voltage	16 V	24 V	32 V	–
Power consumption	–	TBD (1)	TBD (2)	–
Rated current of the fuse	–	7 A	–	–
Voltage limitation in case of overvoltage	TBD	–	TBD	Note: The MBa94xxCA may be damaged in case of permanent overvoltage!

Table 27: Pinout power-in (X28, X29)

Pin	Pin	Signal	Type	Level	Remark
X28	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground
	3	(NC)	–	–	Not connected
X29	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground

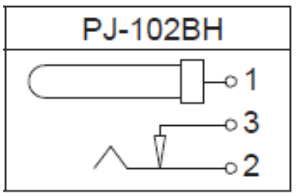

Figure 27: Pinout DC socket 2.5 mm/6.5 mm

1: Typical scenario is not defined.
2: Theoretical full load. All supply voltages are loaded with maximum current, e.g. by connecting additional load to the pin headers, and all system components have maximum power consumption.

3.25.2 Power sequencing

The following figure shows the power-on sequences of the different voltage levels of the main board, without taking into account the rise times of the voltages:

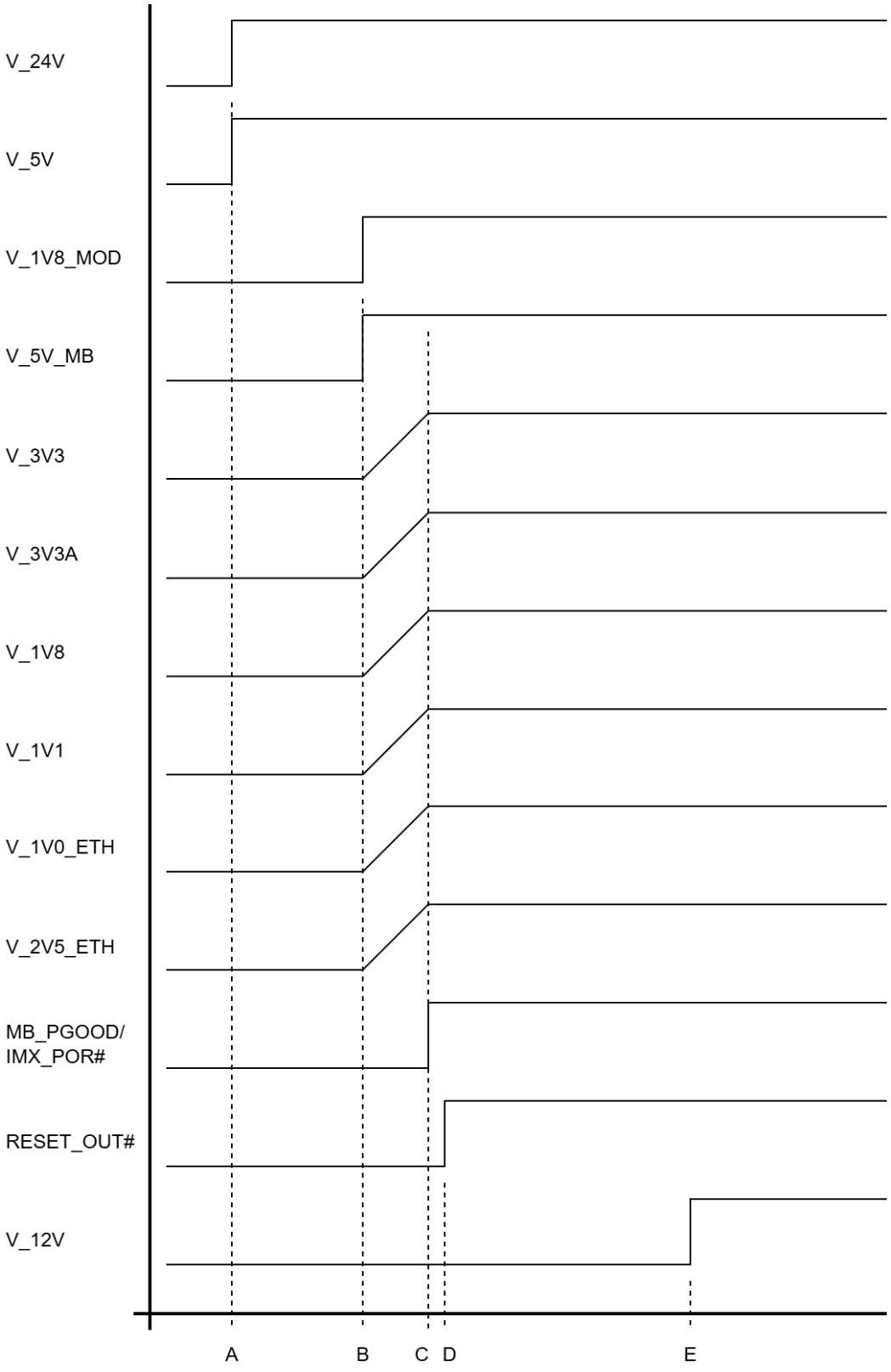

Figure 28: Power sequencing MBa94xxCA

The following table shows the sequence steps from Figure 28:

Table 28: Power sequencing

Sequence	Time	Description
A	t_A	Start point: Power-up MBa94xxCA supplies
B	t_B	Release MBa94xxCA supplies by V_1V8_MOD as last part of the internal power sequence of the TQMa94xxLA
C	t_B + 2 ms	MBa94xxCA supply stable (Softstart Time V_1V8 = 2 ms) Release IMX_POR# by MBa94xxCA (IMX_POR# may still be active on TQMa94xxLA at that time)
D	t_D	Release RESET_OUT# after completion of TQMa94xxLA power sequencing
E	Software dependent	Switching on of additional supply by software driver with 12V_EN

V_1V8_MOD uses the supervisor to control the second regulator of the LM25143 (V_3V3), as well as the power MOSFET for V_5V_MB and the DC-DC converter for V_3V3A. This automatically activates the regulators for V_1V0_ETH, V_2V5_ETH, and V_1V1 as well.

3.25.3 V_5V and V_3V3

3.3 V and 5 V are required to supply the TQMa94xxLA, some components on MBa94xxCA and the USB voltage. The dual regulator LM25143 is used for this purpose, which generates the two voltages from the 16...32 V input voltage.
Voltage V_5V is automatically activated when the mainboard supply is switched on, supplying the TQMa94xxLA. V_3V3 is activated after the module's internal power sequencing is complete, using the V_1V8_MOD provided by the module via the supervisor (LM25119 pin EN2). The designs have the following specification:

Table 29: Specifications V_5V and V_3V3

Voltage	Parameter	Value	Remark
V_5V	V_{IN}	16…32 V	V_24V
	V_{OUT}	4.95…5.05 V	V_5V
	I_{OUT}	7 A	Load: max. 6.86 A (realistic use case)
V_3V3	V_{IN}	16…32 V	V_24V
	V_{OUT}	3.267…3.335 V	V_3V3
	I_{OUT}	7 A	Load: max. 6.95 A (realistic use case)

3.25.4 V_5V_MB

V_5V_MB supplies components whose power is not switched via separate enable signals. The power distribution switches for USB are powered directly from V_5V. The same applies to the DC-DC regulators on V_5V, which are not activated until power sequencing begins.

3.25.5 V_1V8

Various components on the motherboard require a supply voltage of 1.8 V. This is generated from V_5V using the TPS335A DC-DC regulator. The switching regulator is activated by MB_EN (see 4.4.4).
The design has the following specifications:

Table 30: Specification V_1V8

Voltage	Parameter	Value	Remark
V_1V8	V_{IN}	4.5…5.5 V	V_5V
	V_{OUT}	1.769…1.864 V	V_1V8
	I_{OUT}	2 A	Load: max. 1.84 A
	f_sw	520 kHz (±20 %)	TPS54335A
	Output ripple	max. 30 mV_{pp}	Requirement WiFi module

3.25.6 V_3V3A

Due to the noise requirements for the Wi-Fi module, this component is powered by 3.3 V from a separate low-noise LDO. To minimize power loss, an additional DC-DC regulator is connected upstream to generate an intermediate voltage.
The design has the following specification:

Table 31: Specification V_3V3A

Voltage	Parameter	Value	Remark
V_3V6A	V_{IN}	typ. 5 V	V_5V
	V_{OUT}	3.57…3.75 V	V_3V6A
	I_{OUT}	max. 2 A	peak
	f_sw	1.5 MHz	TPS62097
V_3V3A	V_{IN}	3.57…3.75 V	V_3V6A
	V_{OUT}	3.262…3.338 V	V_3V3A
	I_{OUT}	max. 0,8 A	peak
		max. 0,75 A	average
	Ripple	max. 30 mV_{pp}	requirement Wi-Fi module

3.25.7 V_1V0_ETH

The 1 Gbit and 2.5 Gbit Ethernet PHYs require a voltage of 1.0 V. The voltage V_1V0_ETH is generated from V_3V3 using the TPS62097 switching regulator.

Table 32: Specification V_1V0_ETH

Voltage	Parameter	Value	Remark
V_1V0_ETH	V_{IN}	3.2…3.4 V	V_3V3
	V_{OUT}	0.988…1.012 V	V_1V05
	I_{OUT}	2 A	Load: max. 909 mA
	f_sw	1.5 MHz	TPS62097

3.25.8 V_1V1

The USB 3.0 hub and the SPE PHY require a voltage of 1.1 V. The voltage V_1V1 is generated from V_3V3 using the TPS62097 switching regulator.

Table 33: Specification V_1V1

Voltage	Parameter	Value	Remark
V_1V1	V_{IN}	3.2…3.4 V	V_3V3
	V_{OUT}	1.086…1.114 V	V_1V1
	I_{OUT}	1.1 A	Load: max. 1016 mA
	f_sw	1.75 MHz	TPS62097

3.25.9 V_12V

A voltage of 12 V is required for the backlight supply at the LVDS, the fan as well as the starter kit pin header, which is specified with 2.5 A in total. The voltage is generated from V_24V by a step-down converter. The controller can be switched on or off via GPIO signal by software.
The design has the following specification:

Table 34: Specification V_12V

Voltage	Parameter	Value	Remark
V_12V	V_{IN}	16…32 V	V_24V
	V_{OUT}	11.660…12.471 V	V_12V
	I_{OUT}	2.5 A	
	f_sw	1.75 MHz	TPS62097

3.25.10 V_2V5_ETH

The DP83867 Ethernet PHYs require a 2.5 V power supply. It is generated from V_3V3 using the AP7361 linear regulator. Power to the PHYs is thus automatically supplied after the boot process.

Table 35: Specification V_2V5_ETH

Voltage	Parameter	Value	Remark
V_2V5_ETH	V_{IN}	3.25…3.35 V	V_3V3
	V_{OUT}	2.44…2.56 V	V_2V5_ETH
	I_{OUT}	250 mA	Load: max. 170 mA

3.25.11 Power consumption

The following table lists some technical parameters of the board supply. The specified current consumptions are to be regarded as a guide value. Since the current consumption of the MBa94xxCA can differ greatly depending on the application, modes and operating system, the values listed here should only be used for a performance estimate.

Table 36: Current consumption MBa94xxCA

Status	Current	Power
Theoretical calculated peak (worst case)	TBD mA	TBD mW
Linux prompt	TBD mA	TBD mW
Linux Stressapptest	TBD mA	TBD mW
Linux 100% CPU Load	TBD mA	TBD mW
Suspend-to-RAM	TBD mA	TBD mW

3.26 Reset & Configuration

Figure 29 shows the reset structure on the MBa94xxCA.

In addition to the reset signals of the TQMa94xxLA, the MBa94xxCA also provides further software-controlled reset signals for individual function blocks, e.g. ENET reset for the Ethernet transceivers.

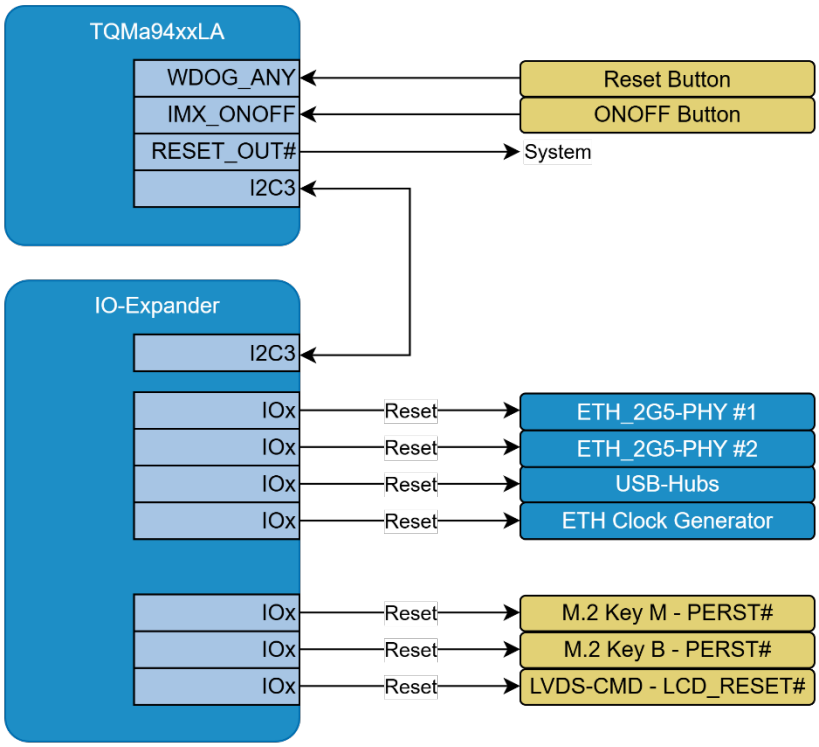

Figure 29: Block diagram Reset & Configuration

The following signals from the TQMa94xxLA are used on the MBa94xxCA:

Table 37: Reset signals

Signal	Type	Level	Remark
WDOG_ANY#	I	1.8 V	• activates RESET of the PMIC (low-active) • no pull-up on mainboard necessary • to activate, connect to GND via a 1 kΩ resistor (push button)
RESET_OUT#	O	-	• open drain output (low-active) • activates RESET of mainboard components • requires pull-up on mainboard (max. 5.5 V)
IMX_ONOFF	I	1.8 V	• ON/OFF function of the i.MX94 (see data sheet) • no pull-up on mainboard necessary • connect to GND to activate (push button)

Push buttons are connected to WDOG_ANY# and IMX_ONOFF.

RESET_OUT is connected with a pull-up to V_3V3 and resets followed blocks:

- IO Expander
- Analog switch for boot mode signals
- External components at starter kit headers

The reset signal is linked to an LED.

4. SOFTWARE

No software is required for the MBa94xxCA.

Suitable software is only required for the TQMa94xxLA and is not a part of this User's Manual.

More information can be found in the TQ-Support Wiki for the TQMa94xxLA.

5. MECHANICS

5.1 MBa94xxCA dimensions

The MBa94xxCA has overall dimensions (length × width × height) of 170 mm × 170 mm × TBD mm.

The MBa94xxCA has six 4.2 mm mounting holes for the housing.

The MBa94xxCA weighs approximately TBD grams without TQMa94xxLA.

5.2 Embedding in the target system

The MBa94xxCA serves as a design base for customer products, as well as a reference platform during development.

5.3 Housing

The form factor and the mounting holes of the MBa94xxCA are designed for installation in a standard Mini-ITX housing.

5.4 Thermal management

The largest power dissipation on the MBa94xxCA is caused by the voltage regulators. In addition, the TQMa94xxLA is a heat source that acts indirectly on the MBa94xxCA. Depending on the application, further power dissipation can occur, mainly at additional external loads on the pin headers on the MBa94xxCA, the M.2 slots, etc.

For evaluation of the TQMa94xxLA under high load conditions an optional heat sink is provided. Four holes are provided on the MBa94xxCA for this purpose. A connector is available on the MBa94xxCA for connecting an optional fan.

Attention: TQMa94xxLA heat dissipation	
	The i.MX 94 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa94xxLA and the TQMa94xxLA-ADAP must be taken into consideration when connecting the heat sink. The TQMa94xxLA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa94xxLA or the MBa94xxCA and thus malfunction, deterioration or destruction.

5.5 Assembly & Labels

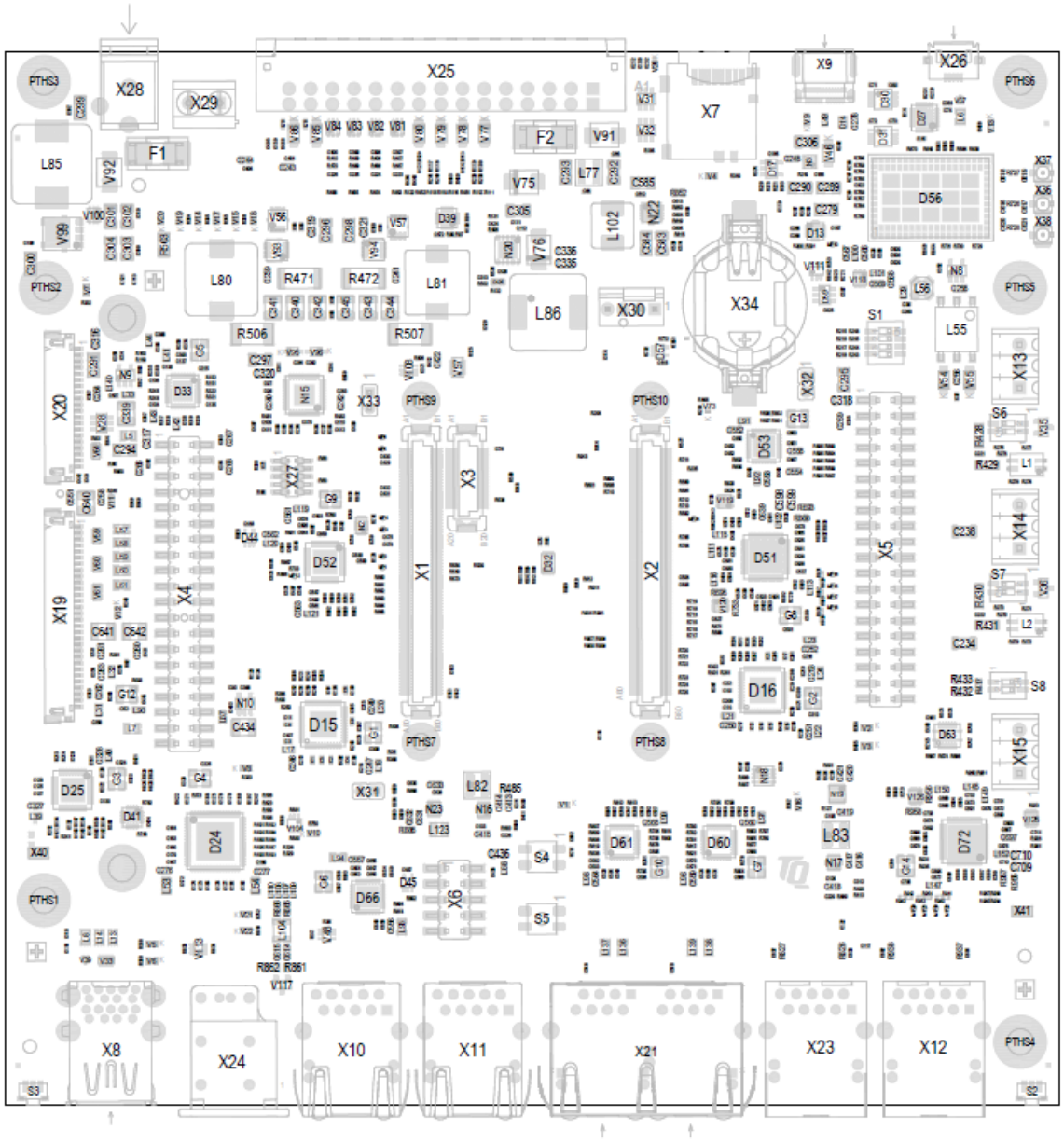

Figure 30: MBa94xxCA top view

The label (TBD) on the MBa94xxCA shows the following information:

Table 38: Labels on MBa94xxCA

Label	Content
AK1	MAC addresses; product name; serial number TQ

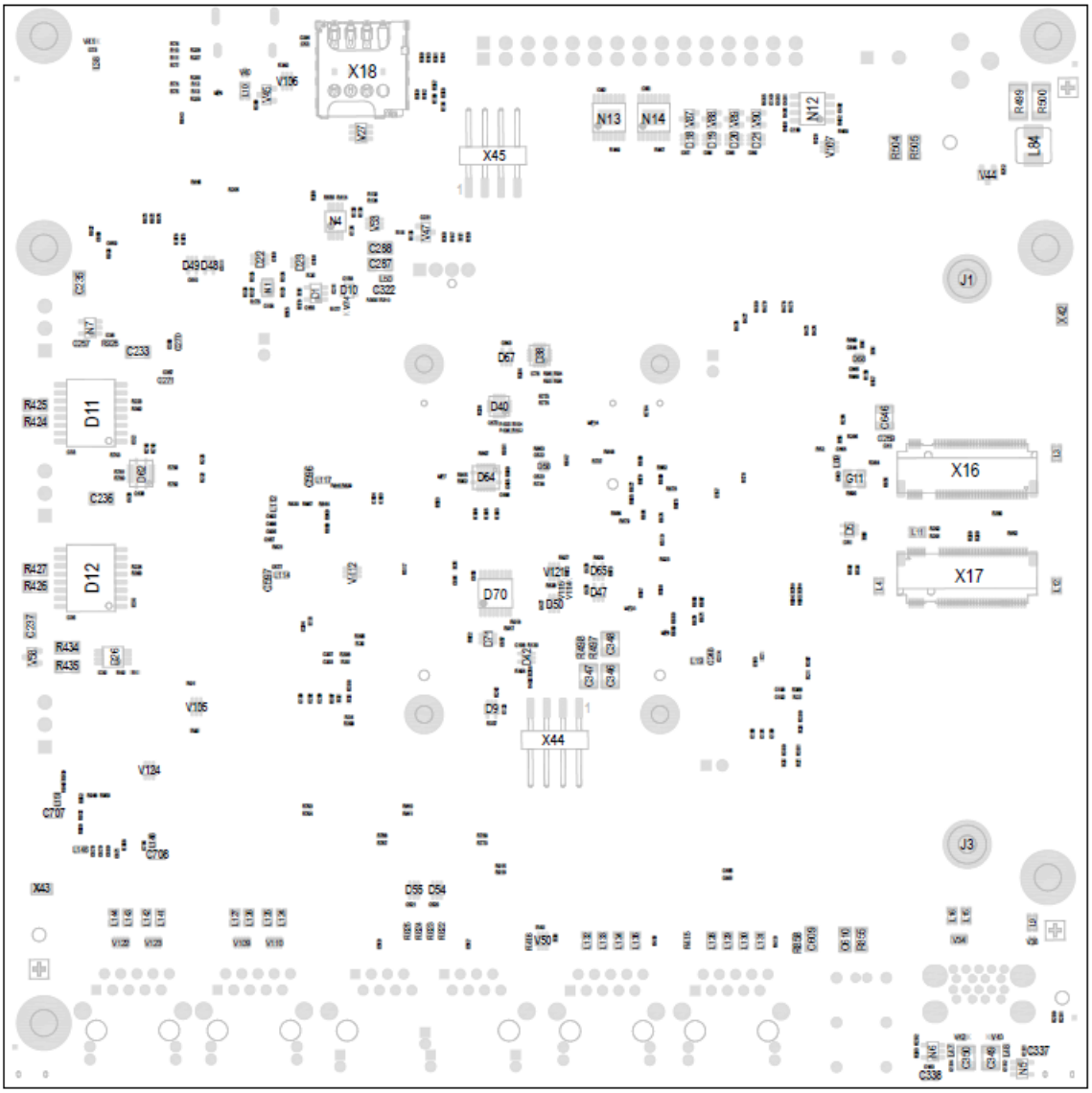

Figure 31: MBa94xxCA bottom view

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBa94xxCA is a development platform, no EMC tests have been performed.
During the development of the MBa94xxCA the standard DIN EN 55022:2010 limit class A was taken into account.

6.2 ESD

ESD protection is provided on most interfaces of the MBa94xxCA.
The MBa94xxCA schematics show, which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the MBa94xxCA is only a sub-component of an overall system.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 39: Climatic and operational conditions MBa94xxCA

Parameter	Range	Remark
Temperature range	–25 °C to +85 °C	
Storage temperature	–40 °C to +100 °C	
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa94xxLA heat dissipation	
	The i.MX 94 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa94xxLA must be taken into consideration when connecting the heat sink. The TQMa94xxLA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa94xxLA and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa94xxCA. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa94xxCA.

The MBa94xxCA is designed to be insensitive to vibration and impact.

7.3 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

7.4 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa94xxCA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa94xxCA was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa94xxCA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa94xxCA enable compliance with EuP requirements for the MBa94xxCA.

8.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.
The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.
Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.
TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

8.6 Packaging

The MBa94xxCA is delivered in reusable packaging.

8.7 Batteries

8.7.1 General notes

For technical reasons a battery is necessary for the MBa94xxCA. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets. During disposal, the device must not be exposed to fire or mechanical crushing while the battery is still installed.

8.7.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa94xxCA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa94xxCA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 40: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AI	Analog Input
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CLC	Capacitor-Inductor-Capacitor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR3L	Double Data Rate 3 Low voltage
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communication
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
I_{PD}	Input with Pull-Down
I_{PU}	Input with Pull-Up
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures

9.1 Acronyms and definitions (continued)

Table 39: Acronyms (continued)

Acronym	Meaning
NAND	Not-And (flash memory)
(NC)	Not Connected
NOR	Not-Or
NP	Not Placed
O_{OD}	Open-Drain Output
O_{PD}	Output with Pull-Down
O_{PU}	Output with Pull-Up
OTG	On-The-Go
PAN	Personal Area Network
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PD	Pull-Down
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media-Independent Interface
SIM	Subscriber Identification Module
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 41: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 943 Industrial Application Processors Data Sheet	Rev. 2, Jul. 2026	NXP
(2)	i.MX94 Hardware Developer's Guide	Rev. 2, Feb. 2026	NXP
(3)	i.MX 94 – Reference Manual	Rev.1, Jul. 2025	NXP
(4)	i.MX 94 – Mask Set Errata	Rev. A0, Jul. 2025	NXP
(5)	TQMa94xxLA User's Manual	– current –	TQ-Systems
(6)	TQMa94xxLA Support Wiki	– current –	TQ-Systems

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