



MBa91xxCA Preliminary User's Manual

MBa91xxCA UM 0002
30.10.2024





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REVISION HISTORY

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0001	30.11.2023	Kreuzer		First edition
0002	30.10.2024	Kreuzer	1.4 3.1.1	Chapter moved Connector source added



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1.6 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.


1.7 Symbols and typographic conventions

Table 1: Terms and Conventions


Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Command	A font with fixed-width is used to denote commands, file names, or menu items.

1.8 Handling and ESD tips

General handling of your TQ-products

	<p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off.</p> <p>Violation of this guideline may result in damage / destruction of the MBa91xxCA and be dangerous to your health.</p> <p>Improper handling of your TQ-product would render the guarantee invalid.</p>
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Proper ESD handling

	<p>The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).</p> <p>Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.</p>
---	--

1.9 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring. The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.10 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.



The following documents are required to fully comprehend the following contents:

- MBa91xxCA schematics
- TQMa91xxCA User's Manual
- i.MX 91 Data Sheet
- i.MX 91 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/Support-Wiki-TQMa91xxCA
- TQ-Support Wiki: [Support-Wiki TQMa91xxCA](http://www.yoctoproject.org/docs/Support-Wiki-TQMa91xxCA)

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of the MBa91xxCA as of revision 01xx. The MBa91xxCA is designed as a carrier board for the TQ modules TQMa91xxCA and TQMa91xxLA with LGA adapter. If not described differently, all descriptions apply to both TQMa91xxCA and TQMa91xxCA.

For better readability, the TQMa91xxCA is therefore named for both, the TQMa91xxCA and the TQMa91xxCA.

Core of the MBa91xxCA is the TQMa91xxCA with an NXP i.MX 91 CPU.

The TQMa91xxCA connects all peripheral components. In addition to the standard communication interfaces such as USB, Ethernet, etc., all other available signals of the TQMa91xxCA are routed on 100 mil standard pin headers on the MBa91xxCA.

CPU features and interfaces can be evaluated; software development for a TQMa91xxCA based project can start immediately.

Currently one i.MX 91 derivative is supported:

1. i.MX 91x1 (1 x Cortex®-A55)

2.1 MBa91xxCA block diagram

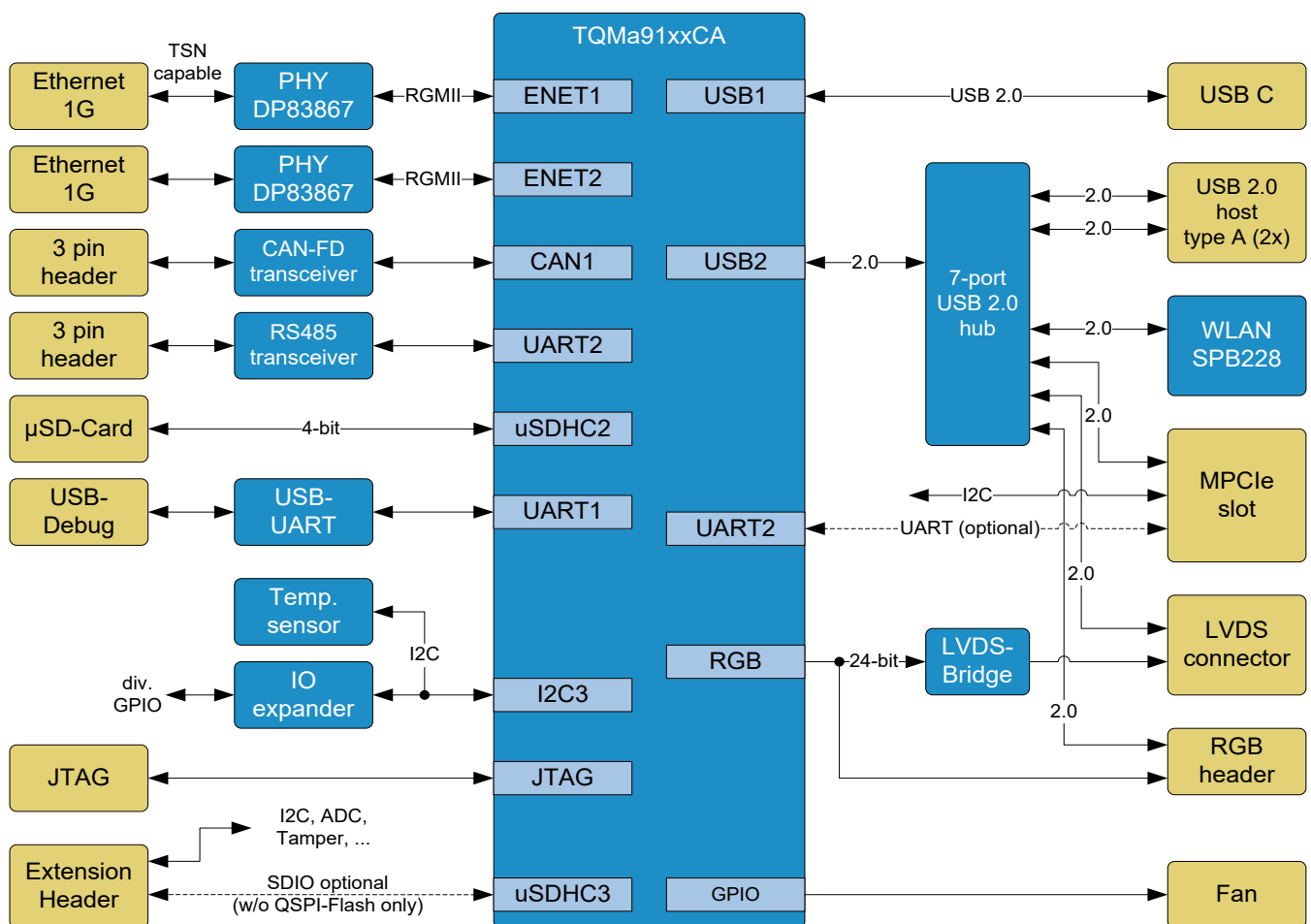


Figure 1: Block diagram MBa91xxCA

2.2 MBa91xxCA data interfaces

The following interfaces/functions and user interfaces are available on the MBa91xxCA:

Table 2: Data interfaces & power connectors

Interface	Connector	Type
CAN-FD	X8	3-pin Phoenix
Coin cell	X14	CR2032 holder
Ethernet, 1000 Base-T	X6, X7	RJ-45, integrated magnetics
Extension headers	X1, X2	100 mil header, 1 × 40-pin, 1 × 10-pin
External battery	X13	2-pin header
Fan	X25	4-pin header
ISO 14443	X4	2-pin header for antenna
LVDS	X12	30-pin, DF19G
LVDS CMD	X11	20-pin, DF19G
Mini PCIe	X16	Mini PCIe socket
	X18	SIM card holder
Power In	X23	DC jack (2.5 mm / 5.5 mm)
	X24	2-pin screw terminal block
RGB	X3	100 mil header, 2 × 30-pin
RS485	X10	3-pin Phoenix
SD card, UHS-I	X15	Push-Pull
USB 2.0 Host	X19	USB, stacked Type A
USB Type C	X17	USB, Type C
USB debug	X22	USB, Micro AB
WLAN	D6-A, D6-B	MHF4

The MBa91xxCA provides the following diagnostic and user interfaces:

Table 3: Diagnostic and user interfaces

Interface	Component	Remark
Status LEDs	8 × Green LED	Power LEDs
	4 × Green LED	3 × USB Host, 1 × USB Type-C
	1 × Green LED	Debug LED for USB debug interface
	1 × Green LED	User LED1
	1 × Orange LED	User LED2
	3 × Green LED	Mini PCIe: WWAN, WLAN, WPAN
	1 × Red LED	Reset LED
	2 × Green / 2 × Yellow LED	Ethernet LEDs (Activity / Speed)
	2 × Green LED	WLAN / Mobile Network
	1 × Green LED	SD card
Temperature sensor	1 × SE97BTP	Digital I ² C temperature sensor
Power / Reset button	2 × Push button	PMIC_RST, ONOFF
General Purpose button	2 × Push button	GP push button at port expander
Boot Mode configuration	1 × 4-fold DIP switch	Boot Mode configuration
CAN termination	1 × 2-fold DIP switch	S4
JTAG	1 × 10-pin, 100 mil header	X20
RS485 termination	1 × 2-fold DIP switch	S6

3. ELECTRONICS

The following chapters describe the interfaces of the MBa91xxCA as of revision 01xx in connection with a TQMa91xxCA or TQMa91xxCA with maximum configuration. If not described differently, all descriptions apply to both TQMa91xxCA and TQMa91xxLA.

For better readability, the TQMa91xxCA is therefore named for both, the TQMa91xxCA and the TQMa91xxLA.

In any case the TQMa91xxCA User's Manual must be complied with.

3.1 TQMa91xxCA

The TQMa91xxCA is the central system on the MBa91xxCA. It provides LPDDR4 SDRAM, eMMC, NOR flash, RTC, EEPROM, power supply and power management functionality.

All TQMa91xxCA internal voltages are derived from the 5 V supply voltage. All functionally relevant pins of the CPU are routed to the TQMa91xxCA connectors. This enables the user to use the TQMa91xxCA with all the freedom that comes with a customer-specific design-in solution. Further information can be found in the TQMa91xxCA User's Manual.

On the MBa91xxCA the standard interfaces like USB, Ethernet, etc., provided by the TQMa91xxCA are routed to industry standard connectors. All other signals and buses provided by the TQMa91xxCA are routed to 100 mil headers.

The boot behaviour of the TQMa91xxCA can be configured.

The Boot Mode configuration is set by a DIP switch on the MBa91xxCA, see chapter 3.2.

Furthermore, the MBa91xxCA provides all power supplies and configurations required for the operation of the TQMa91xxCA.

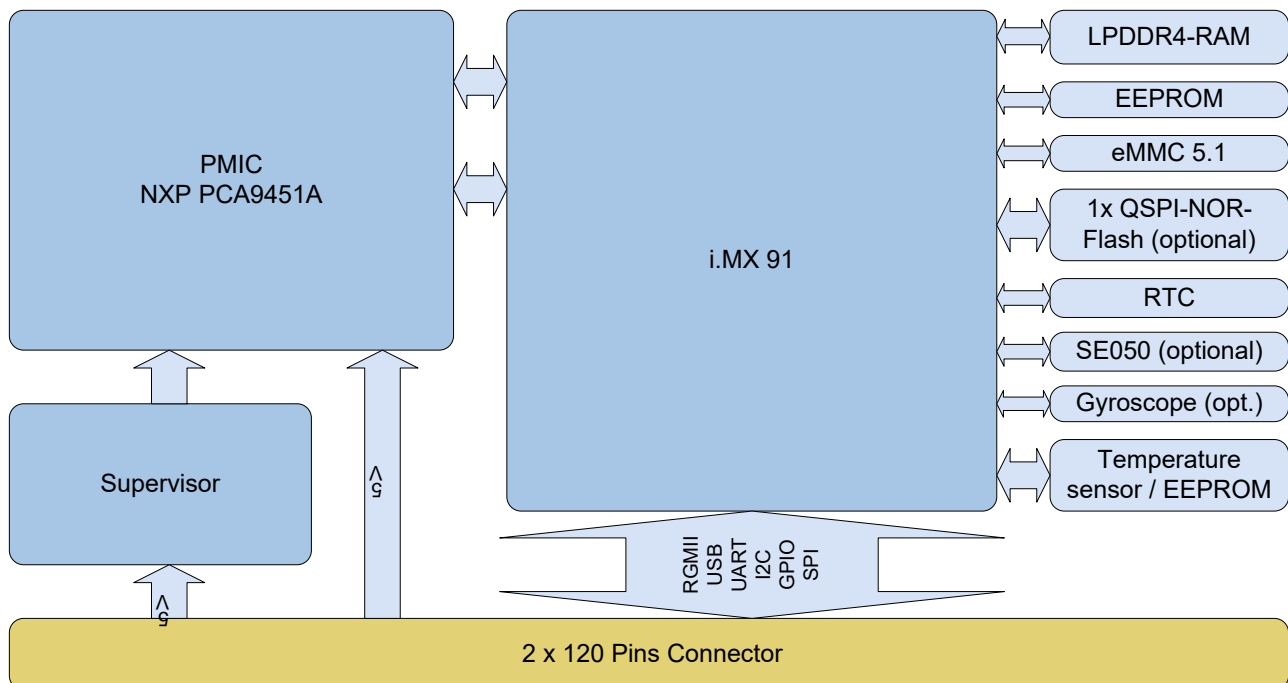


Figure 2: Block diagram TQMa91xxCA

3.1.1 TQMa91xxCA connectors on MBa91xxCA

The TQMa91xxCA is connected to the MBa91xxCA with 240 pins on two connectors (ept Colibri Plug 120, 5mm 401-51401-51). Connector samples are available from: <https://www.ept.de/index.php?tq-colibri-lp>

The TQMa91xxCA is held in the mating connectors on the MBa91xxCA by 240 pins with a considerable retention force. To avoid damaging the connectors of the MBa91xxCA or the TQMa91xxCA while removing the TQMa91xxCA, the use of the extraction tool MOZI6UL REV.0100 is strongly recommended.

Note: Component placement on carrier board



2.5 mm should be kept free on the carrier board, on both long sides of the MBa91xxCA for the extraction tool MOZIA6UL REV.0100.

The pins assignment listed in Table 4 to Table 5 refer to the corresponding [BSP provided by TQ-Systems](#). For information regarding I/O pins in Table 4 to Table 5 refer to the i.MX 91 documentation, see Table 45.

3.1.2 TQMa91xxCA pinout

All available TQMa91xxCA signals are available at the two connectors D1-X1 and D1-X2 on the MBa91xxCA.

The direction of the signals in Table 4 to Table 5 is shown from the perspective of the TQMa91xxCA.

Further information like pull-ups or pull-downs on the TQMa91xxCA can be taken from the TQMa91xxCA User's Manual (6).

3.1.2 TQMa91xxCA pinout (continued)

Table 4: Pinout TQMa91xxCA connector, D1-X1

Cpu ball	Dir.	Level	TQ Multiplexing	Pin		TQ Multiplexing	Level	Dir.	CPU ball
-	P	5 V	V_5V_IN	X1-A1	X1-B1	V_5V_IN	5 V	P	-
-	P		V_5V_IN	X1-A2	X1-B2	V_5V_IN		P	-
-	P		V_5V_IN	X1-A3	X1-B3	V_5V_IN		P	-
-	-	0V	GND	X1-A4	X1-B4	GND	0V	-	-
AA2	O	1.8 V	GPIO3_IO26	X1-A5	X1-B5	ENET1_TXC	1.8 V	O	U10
-	-	0V	GND	X1-A6	X1-B6	GND	0V	-	-
Y3	O	1.8 V	GPIO3_IO27	X1-A7	X1-B7	ENET1_TX_CTL	1.8 V	O	V10
U4	O		CLK3_OUT	X1-A8	X1-B8	ENET1_TXD0		O	W11
V4	O		GPIO4_IO29	X1-A9	X1-B9	ENET1_TXD1		O	T12
-	-	0V	GND	X1-A10	X1-B10	ENET1_TXD2	-	O	U12
-	I/O	3.3 V	PMIC_SCLH	X1-A11	X1-B11	ENET1_TXD3	-	O	V12
-	I/O		PMIC_SDAH	X1-A12	X1-B12	GND	0V	-	-
-	-	0V	GND	X1-A13	X1-B13	ENET1_RXC	1.8 V	I	AA7
-	I/O	1.8 V	PMIC_SDAL	X1-A14	X1-B14	GND	0V	-	-
-	I/O		PMIC_SCLL	X1-A15	X1-B15	ENET1_RX_CTL	1.8 V	I	Y8
-	-	0V	GND	X1-A16	X1-B16	GND	0V	-	-
AA19	O	V_SD2	SD2_CLK	X1-A17	X1-B17	ENET1_RXD0	1.8 V	I	AA8
-	-	0V	GND	X1-A18	X1-B18	ENET1_RXD1		I	Y9
Y19	I/O	V_SD2	SD2_CMD	X1-A19	X1-B19	ENET1_RXD2		I	AA9
Y17	I		SD2_CD#	X1-A20	X1-B20	ENET1_RXD3	I	Y10	
-	-	0V	GND	X1-A21	X1-B21	GND	0V	-	-
Y18	I/O	V_SD2	SD2_DATA0	X1-A22	X1-B22	ENET1_MDC	1.8 V	O	AA11
AA18	I/O		SD2_DATA1	X1-A23	X1-B23	ENET1_MDIO		I/O	AA10
Y20	I/O		SD2_DATA2	X1-A24	X1-B24	GND	0V	-	-
AA20	I/O		SD2_DATA3	X1-A25	X1-B25	QSPI_SCLK ¹	1.8 V	O	V16
-	-	0V	GND	X1-A26	X1-B26	GND	0V	-	-
AA17	O	V_SD2	SD2_RST#	X1-A27	X1-B27	QSPI_SS0# ¹	1.8 V	O	U16
-	-	0V	GND	X1-A28	X1-B28	QSPI_DATA0 ¹		I/O	T16
-	P	1.8 V / 3.3V	V_SD2	X1-A29	X1-B29	QSPI_DATA1 ¹		I/O	V14
-	-	0V	GND	X1-A30	X1-B30	QSPI_DATA2 ¹		I/O	U14
-	P	3.3 V	V_3V3_SD ²	X1-A31	X1-B31	QSPI_DATA3 ¹	-	I/O	T14
-	-	0V	GND	X1-A32	X1-B32	GND	0V	-	-
-	P	3.3 V	V_3V3 ³	X1-A33	X1-B33	RFU	-	-	-
-	P	1.8 V	V_1V8 ³	X1-A34	X1-B34	RFU	-	-	-
-	-	0V	GND	X1-A35	X1-B35	GND	0V	-	-
R20	I/O	V_GPIO	SAI3_MCLK	X1-A36	X1-B36	PMIC_RST#	1.8 V	I	-
-	-	0V	GND	X1-A37	X1-B37	RESET_OUT#	open drain, needs external pull-up		
T21	I/O	V_GPIO	SAI3_TXD0	X1-A38	X1-B38	GPIO1_IO02	3.3 V	I/O	D20
V20	I/O		SAI3_TXFS	X1-A39	X1-B39	GND	0V	-	-
R21	I/O		SAI3_TXC	X1-A40	X1-B40	UART6_RXD	V_GPIO	I/O	L18
-	-	0V	GND	X1-A41	X1-B41	UART6_TXD		I/O	L17
T20	I/O	V_GPIO	SAI3_RXD0	X1-A42	X1-B42	GND	0V	-	-
R17	I/O		SAI3_RXFS	X1-A43	X1-B43	TPM5_CH0	V_GPIO	I/O	L20
R18	I/O		SAI3_RXC	X1-A44	X1-B44	GPIO2_IO07		I/O	L21
-	-	0V	GND	X1-A45	X1-B45	GND	0V	-	-
N20	I/O	V_GPIO	UART8_TXD	X1-A46	X1-B46	SPI6_PCS0#	V_GPIO	I/O	J21
N21	I/O		UART8_RXD	X1-A47	X1-B47	SPI6_SIN		I/O	J20
-	-	0V	GND	X1-A48	X1-B48	SPI6_SOUT		I/O	K20
P20	I/O	V_GPIO	UART3_TXD	X1-A49	X1-B49	SPI6_SCK		I/O	K21
P21	I/O		UART3_RXD	X1-A50	X1-B50	GND	0V	-	-
-	-	0V	GND	X1-A51	X1-B51	GPIO2_IO10	V_GPIO	I/O	N17
U21	I/O	V_GPIO	GPIO2_IO24	X1-A52	X1-B52	TPM3_EXTCLK		I/O	M21
U20	I/O		I2C5_SCL	X1-A53	X1-B53	TPM6_CH0		I/O	M20
U18	I/O		I2C5_SDA	X1-A54	X1-B54	GPIO2_IO11		I/O	N18
-	-	0V	GND	X1-A55	X1-B55	GND	0V	-	-
W21	I/O	V_GPIO	CAN2_RX	X1-A56	X1-B56	GPIO1_IO14	3.3 V	O	H20
V21	I/O		CAN2_TX	X1-A57	X1-B57	GPIO1_IO12		I	G20
-	-	0V	GND	X1-A58	X1-B58	GPIO1_IO11		O	G21
Y21	I/O	V_GPIO	I2C3_SCL	X1-A59	X1-B59	UART2_RTS#		O	H21
W20	I/O		I2C3_SDA	X1-A60	X1-B60	GND	0V	-	-

¹ NC if NOR-Flash is placed

² Power-Output (max. 400 mA)

³ Power-Output (max. 500 mA)



3.1.2 TQMa91xxCA pinout (continued)

Table 5: Pinout TQMa91xxCA connector, D1-X2

CPU ball	Dir.	Level	TQ Multiplexing	Pin		TQ Multiplexing	Level	Dir.	CPU ball
-	I/O	3.3 V	ISO_14443_LA	X2-A1	X2-B1	DNC	1.8 V	O	C1
-	I/O		ISO_14443_LB	X2-A2	X2-B2	DNC		O	B1
-	-	0 V	GND	X2-A3	X2-B3	GND	0 V	-	-
-	I	3.3 V	ISO_7816_CLK	X2-A4	X2-B4	DNC	1.8 V	O	B3
-	I/O		ISO_7816_IO1	X2-A5	X2-B5	DNC		O	A3
-	-	0 V	GND	X2-A6	X2-B6	GND	0 V	-	-
-	I/O	3.3 V	ISO_7816_IO2	X2-A7	X2-B7	DNC	1.8 V	O	B2
-	I	3.3 V	ISO_7816_RST	X2-A8	X2-B8	DNC		O	A2
-	-	0 V	GND	X2-A9	X2-B9	GND	0 V	-	-
W1	I	1.8 V	JTAG_TDI	X2-A10	X2-B10	DNC	1.8 V	O	B4
Y2	O		JTAG_TDO	X2-A11	X2-B11	DNC		O	A4
Y1	O		JTAG_TCK	X2-A12	X2-B12	GND	0 V	-	-
W2	I/O		JTAG_TMS	X2-A13	X2-B13	DNC	1.8 V	O	B5
-	-	0 V	GND	X2-A14	X2-B14	DNC		O	A5
-	P	0.9...5.5 V	V_LICELL	X2-A15	X2-B15	RTC_EVENT#	open drain, needs external pull-up		
-	-	0 V	GND	X2-A16	X2-B16	GND	0 V	-	-
U6	O	1.8 V	ENET2_TXC	X2-A17	X2-B17	TEMP_EVENT#	open drain, needs external pull-up		
-	-	0 V	GND	X2-A18	X2-B18	DNC	1.8 V	O	A6
V6	O	1.8 V	ENET2_TX_CTL	X2-A19	X2-B19	DNC		O	B6
T8	O		ENET2_TXD0	X2-A20	X2-B20	GND	0 V	-	-
U8	O		ENET2_TXD1	X2-A21	X2-B21	DNC	1.8 V	O	A7
V8	O		ENET2_TXD2	X2-A22	X2-B22	DNC		O	B7
T10	O		ENET2_TXD3	X2-A23	X2-B23	GND	0 V	-	-
-	-	0 V	GND	X2-A24	X2-B24	DNC	1.8 V	O	D6
AA3	I	1.8 V	ENET2_RXC	X2-A25	X2-B25	DNC		O	E6
-	-	0 V	GND	X2-A26	X2-B26	GND	0 V	-	-
Y4	I	1.8 V	ENET2_RX_CTL	X2-A27	X2-B27	DNC	1.8 V	O	A8
AA4	I		ENET2_RXD0	X2-A28	X2-B28	DNC		O	B8
Y5	I		ENET2_RXD1	X2-A29	X2-B29	GND	0 V	-	-
AA5	I		ENET2_RXD2	X2-A30	X2-B30	DNC	1.8 V	O	A9
Y6	I		ENET2_RXD3	X2-A31	X2-B31	DNC		O	B9
-	-	0 V	GND	X2-A32	X2-B32	GND	0 V	-	-
AA6	I/O	1.8 V	ENET2_MDIO	X2-A33	X2-B33	DNC	1.8 V	I	A11
Y7	O		ENET2_MDC	X2-A34	X2-B34	DNC		I	B11
-	-	0 V	GND	X2-A35	X2-B35	GND	0 V	-	-
C20	O	3.3 V	I2C1_SCL	X2-A36	X2-B36	DNC	1.8 V	I	D10
C21	I/O		I2C1_SDA	X2-A37	X2-B37	DNC		I	E10
-	-	0 V	GND	X2-A38	X2-B38	GND	0 V	-	-
J17	I	3.3 V	CAN1_RX	X2-A39	X2-B39	DNC	1.8 V	I	A10
G17	O		CAN1_TX	X2-A40	X2-B40	DNC		I	B10
-	-	0 V	GND	X2-A41	X2-B41	GND	0 V	-	-
G18	I	3.3 V	GPIO1_IO10	X2-A42	X2-B42	ONOFF	1.8 V	I	A19
B16	I/O	1.8 V	TAMPER0	X2-A43	X2-B43	USB1_ID	1.8 V	I	C11
F14	I/O		TAMPER1	X2-A44	X2-B44	USB2_ID		I	E12
-	-	0 V	GND	X2-A45	X2-B45	GND	0 V	-	-
B17	I	1.8 V	CLK1_IN	X2-A46	X2-B46	V_GPIO ¹	1.8 V / 3.3 V	P	N15
A18	I		CLK2_IN	X2-A47	X2-B47	USB1_VBUS		P	F12
J18	O	3.3 V	WDOG_ANY	X2-A48	X2-B48	USB2_VBUS	(5 V tolerant)	P	E14
-	I	3.3 V	PMIC_WDOG_IN#	X2-A49	X2-B49	GND		-	-
-	-	0 V	GND	X2-A50	X2-B50	DNC	-	-	B12
B19	I	1.8 V	ADC_IN0	X2-A51	X2-B51	DNC	0 V	-	A12
A20	I		ADC_IN1	X2-A52	X2-B52	GND		-	-
B20	I		ADC_IN2	X2-A53	X2-B53	DNC	-	-	B13
B21	I		ADC_IN3	X2-A54	X2-B54	DNC		-	A13
-	-	0 V	GND	X2-A55	X2-B55	GND	0 V	-	-
E20	I	3.3 V	UART1_RXD	X2-A56	X2-B56	USB1_DP	3.3 V	I/O	B14
E21	O	3.3 V	UART1_TXD	X2-A57	X2-B57	USB1_DN		I/O	A14
F20	I	3.3 V	UART2_RXD	X2-A58	X2-B58	GND	0 V	-	-
F21	O	3.3 V	UART2_TXD	X2-A59	X2-B59	USB2_DP	3.3 V	I/O	B15
-	-	0 V	GND	X2-A60	X2-B60	USB2_DN		I/O	A15

¹ Power-Input for NVCC_GPIO

3.2 Boot Mode configuration

The TQMa91xxCA can boot from different boot sources. The boot source is selected on the MBa91xxCA via DIP switches (S1). The following table shows the possible boot configurations of the i.MX91, where Serial NAND is not supported by the MBa91xxCA.

The four BOOT_MODE pins of the CPU are not dedicated pins, but are multiplexed with functional IO pins. So that neither connected periphery influences the boot mode nor the boot configuration influences the connected periphery, the pins are switched via analog switch. The RESET_OUT# signal is used for toggling, which triggers the switch with a delay (approx. 5 ms) after RESET_OUT# has been released by the logic and RC element. The switch back to the DIP switch is done almost without delay at a low edge at RESET_OUT#.

At the BOOT_MODE signals 100 kΩ pull-down resistors are provided. The 3.3 V provided by the module are used as pull-up voltage for the switchable 4.7 kΩ resistors.

Table 6: Boot Mode configuration

Boot-Mode	S1-4 (BM3)		S1-3 (BM2)		S1-2 (BM1)		S1-1 (BM0)		Remark
	Pos.	Level	Pos.	Level	Pos.	Level	Pos.	Level	
Boot from eFuses	OFF	0	OFF	0	OFF	0	OFF	0	–
Serial Downloader (USB 1)	OFF	0	OFF	0	OFF	0	ON	1	–
eMMC (USDCH1)	OFF	0	OFF	0	ON	1	OFF	0	–
SD card (USDHC2)	OFF	0	OFF	0	ON	1	ON	1	–
FlexSPI Serial NOR	OFF	0	ON	1	OFF	0	OFF	0	–

Note: Boot from NAND



Booting from NAND is not supported on the MBa91xxCA.

3.3 I²C devices

Due to the large number of I²C devices on the TQMa91xxCA, special attention must be paid to the I2C1 addresses already in use. Depending on the application and software load the number of used I2C devices may limit the data throughput or block the bus. For this reason several devices used on the MBa91xxCA are connected to I2C3.

Table 7: I²C signals

Signal	MBa91xxCA pin
I2C1_SDA	D1-X2-A37
I2C1_SCL	D1-X2-A36
I2C3_SDA	D1-X1-A60
I2C3_SCL	D1-X1-A59

The following table shows the default I²C device addresses on the MBa91xxCA and the TQMa91xxCA. For some devices the address can be changed by assembly options. The options are described in detail in the given chapter.

Table 8: I²C devices, address mapping on TQMa91xxCACA and MBa91xxCA

Location	Bus	Device	Function	7-bit address	Remark
TQMa91xxCA	I2C1	PCA9451	PMIC	0x25 / 010 0101b	
		SE97BTP	Temperature sensor in EEPROM	0x1B / 001 1011b	
			EEPROM Read / Write	0x53 / 101 0011b	
			Protection command	0x33 / 011 0011b	
		SE050 (opt.)	Trust Secure Element	0x48 / 100 1000b	
		PCF85063A	RTC	0x51 / 101 0001b	
		M24C64	EEPROM Memory array	0x57 / 101 0111b	
			Identification page (32 Byte)	0x5F / 101 1111b	
		ISM330 (opt.)	Gyroscope	0x6A / 110 1010b	
MBa91xxCA	I2C1	X2	Pin header	NA	
	I2C3	X16/X2	Mini-PCle	NA	available at pin header
		PTN5110	USB-C PD-Controller	0x50 / 101 0000b	
		SE97BTP	Temperature sensor in EEPROM	0x1C / 001 1100b	
			EEPROM Read / Write	0x54 / 101 0100b	
			Protection command	0x34 / 011 0100b	
		PCA9538	Port expander #1	0x70 / 111 0000b	
		PCA9538	Port expander #2	0x71 / 111 0001b	
		PCA9538	Port expander #3	0x72 / 111 0010b	

Note: I²C address conflicts

When changing the address due to assembly options or when connecting further I²C components, it must be ensured that no address conflicts occur. Otherwise malfunctions may occur. The addresses preassigned by the TQMa91xxCA must also be observed (depending on the TQMa91xxCA variant used).

3.4 GPIO port expander

Three I2C IO expanders with eight ports each are used on the MBa91xxCA.

The port expanders are controlled via I2C3. The addresses of the port expanders can be altered by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 8.

The assembly options are documented in the schematic of the MBa91xxCA.

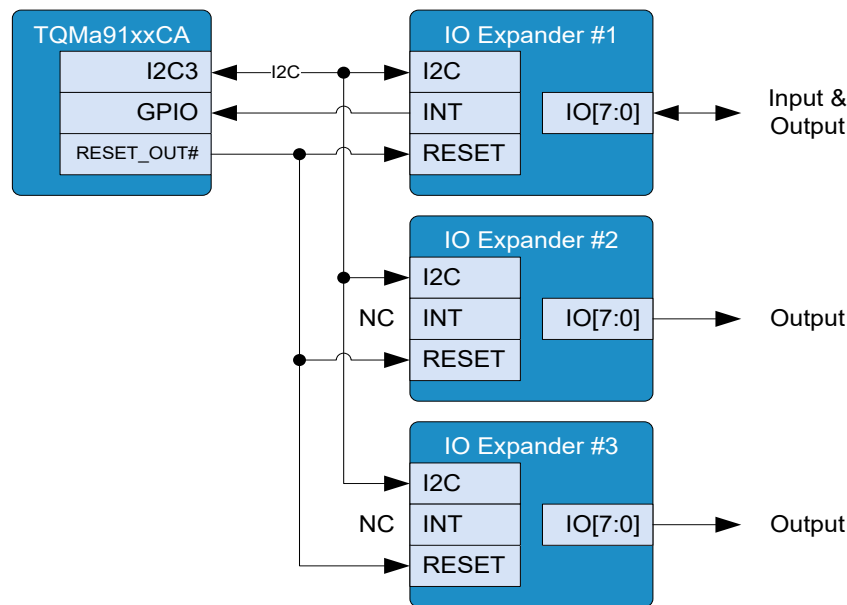


Figure 3: Block diagram GPIO expanders

The IO expanders are supplied with V_3V3. Due to the lack of GPIO pins at the TQMa91xxCA, only one IO expander, to which input signals are connected, sends the interrupt signal to the CPU. The other expanders only contain output signals. The interrupt signal is not necessary for this. The used IO expanders have a reset input that is connected to RESET_OUT#. This resets all signals at a reset of the CPU (High-Z).

Table 9: Port expander functions

Expander	I ² C device address	Port	Signal	Dir.
1	0x70	IO_0	TEMP_EVENT_MOD#	O
		IO_1	MPCIE_WAKE#	I
		IO_2	MPCIE_1V5_EN	O
		IO_3	MPCIE_3V3_EN	O
		IO_4	MPCIE_PERST#	O
		IO_5	MPCIE_WDISABLE#	O
		IO_6	BUTTON_A#	I
		IO_7	BUTTON_B#	I
2	0x71	IO_0	ENET1_RESET#	O
		IO_1	ENET2_RESET#	
		IO_2	USB_RESET#	O
		IO_3	NC	
		IO_4	WLAN_PD#	O
		IO_5	WLAN_W_DISABLE#	
		IO_6	WLAN_PERST#	
		IO_7	12V_EN	
3	0x72	IO_0	LCD_RESET#	O
		IO_1	LCD_PWR_EN	
		IO_2	LCD_BLT_EN	
		IO_3	LVDS_SHDN#	
		IO_4	FAN_PWR_EN	
		IO_5	NC	
		IO_6	USER_LED1	
		IO_7	USER_LED2	

3.5 Temperature sensor and EEPROM

A temperature sensor SE97BTP is populated on the MBa91xxCA to monitor the temperature. The same type of sensor is also used on the TQMa91xxCA. The sensor of MBa91xxCA is read out via I2C3, the sensor of TQMa91xxCA is read out via I2C1, see Table 8.

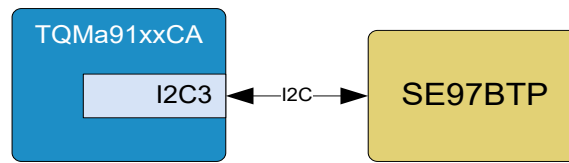


Figure 4: Block diagram temperature sensor

The sensor address on the MBa91xxCA can be changed by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices, see Table 8. The assembly options are documented in the MBa91xxCA schematics.

The SE97BTP has an additional EEPROM. Further specifications of the SE97BTP can be found in the data sheet.

The alarm output Temp_EVENT_MB# of the SE97BTP is available on the pin header X2.

3.6 RTC backup

The TQMa91xxCA has an optional RTC and a voltage rail for standby functions. This is supplied via pin V_LICELL. On the MBa91xxCA there are two possibilities to supply the LICELL input ¹:

- CR2032-Battery holder
- 2-pin header (X13) for alternative connection of an external voltage or batteries

The maximum input voltage at X13 is described in the TQMa91xxCA User's Manual.

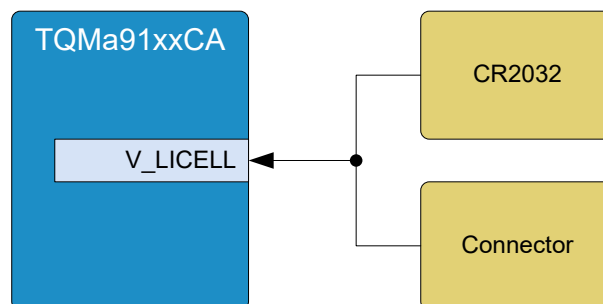


Figure 5: Block diagram RTC backup

Table 10: Pinout RTC backup (X13)

Pin	Signal	Level	Remark
1	V_LICELL	3 V	Supply voltage for RTC on TQMa91xxCA
2	GND	0 V	Ground

To meet regulatory requirements for protection against accidental battery charging, a 1 kΩ resistor and diode is connected in series between X13/X14 and the V_LICELL input of the TQMa91xxCA.

The diode has a very low forward voltage (<0.1V) to not unnecessarily reduce battery runtime, and a very low reverse current to keep residual charge currents as low as possible.

If it is necessary to reduce the forward voltage to 0 V for test purposes, the protective diode can be removed according to Table 11 and a corresponding resistor can be fitted.

¹: Only one of the two options may be used at a time!

Table 11: Assembly option RTC-Backup

Reverse current protection	V56	R216	Remark
Active	BAS70	NP	Default
Not active	NP	0 Ω	Note: 1 k Ω in series is still present in this case

Attention: Loss of reverse current protection



The reverse current protection is lost when the protective diode is replaced with a resistor! This is especially critical for TQMa91xxCACA with external RTC, since here the 3.3 V supply of the TQMa91xxCA in ON mode¹ drives directly into the RTC backup battery!

3.7 USB hub

The 7-port USB 2.0 hub USB2517 is used to provide the USB interfaces on the USB host sockets as well as for the WLAN module, Mini PCIe, RGB pin header, and LVDS connectors. The USB hub is connected to the CPU at the USB2 port.

VBUS with max. 500 mA each port is provided at the USB type A double jack.

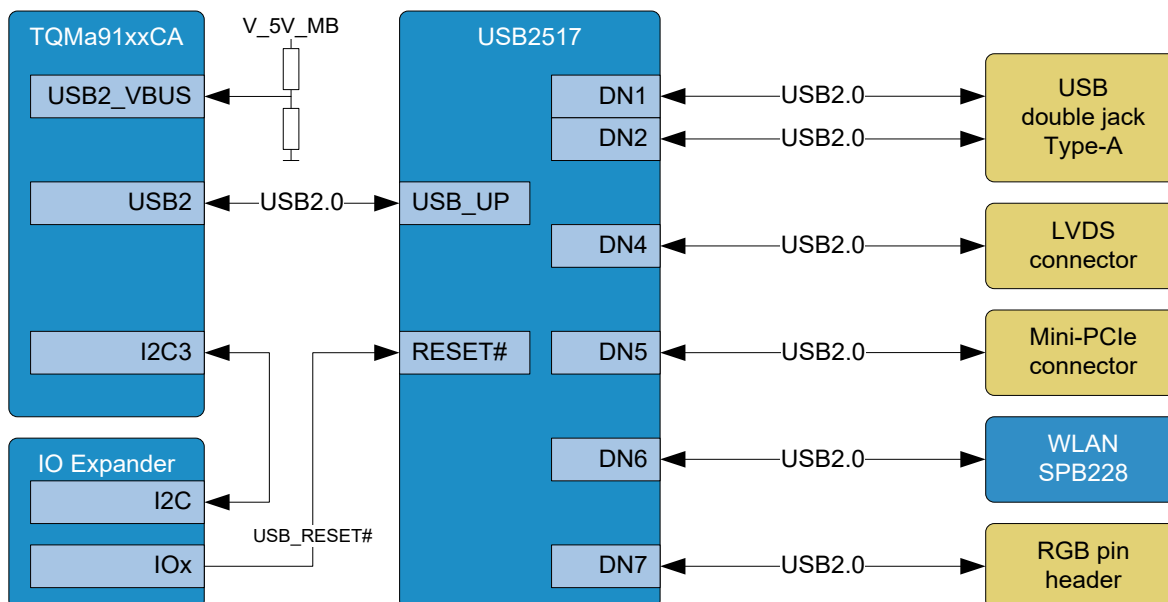


Figure 6: Block diagram USB hub

3.8 Data interfaces

3.8.1 CAN-FD

The CAN interface of the MBa91xxCA is available at the 3-pin connector X8. The interface is galvanically isolated with 1 kV.

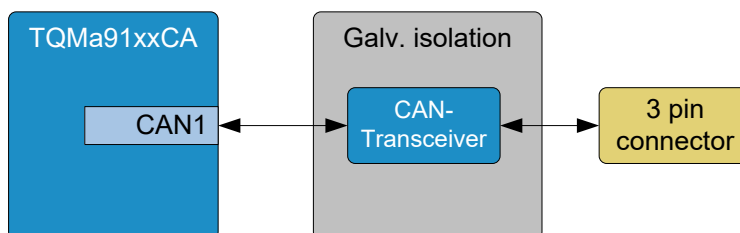


Figure 7: Block diagram CAN

1: TQMa91xxCACA is supplied at V_3V3_IN.

The CAN signals can be terminated with 120 Ω via DIP switches S4 (CAN1).

Table 12: CAN termination

Sx-1	Sx-2	Modus
OFF	OFF	No termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Termination with 120 Ω

Table 13: Pinout CAN1 (X8)

CAN	Pin	Signal	Dir.	Level	Remark
CAN1	1	CAN1_H	I/O	Spec. ⁽¹⁾	CAN High-Level I/O from CAN1 / galvanically isolated
	2	CAN1_L	I/O	Spec. ⁽¹⁾	CAN Low-Level I/O from CAN1 / galvanically isolated
	3	GND_CAN	P	0 V	Ground / galvanically isolated

3.8.2 Debug USB / UART

For debug purposes, a UART of the i.MX91 CPU is made available at USB socket X22 by using an FTDI USB bridge. UART1 is used for this purpose.

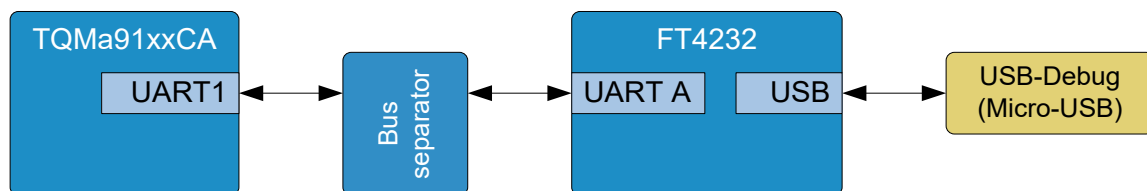


Figure 8: Block diagram USB debug

Note: Connection to the host cannot be established



If no connection to the host can be established, the host may require drivers:
<https://ftdichip.com/Drivers/vcp-drivers/>

3.8.3 Ethernet

The i.MX91 processor has two independent RGMII interfaces. On the MBa91xxCA, both interfaces are used to provide two Gigabit Ethernet ports. The ENET1 interface (ENET QOS) of the CPU provides Time Sensitive Network (TSN) features and is therefore used for the TSN-capable interface. The 1588_EVENT signals of the CPU can only be multiplexed to balls of the SD2 interface. As the SD card already occupies this, the EVENT signals cannot be used by default. Placement options are provided on the MBa91xxCA to make the EVENT signals of the ENET1 optionally available at the starter kit header. When using these signals, the SD Card cannot be used.

The ENET2 interface does not support TSN. The Ethernet ports are provided on two RJ45 jacks.

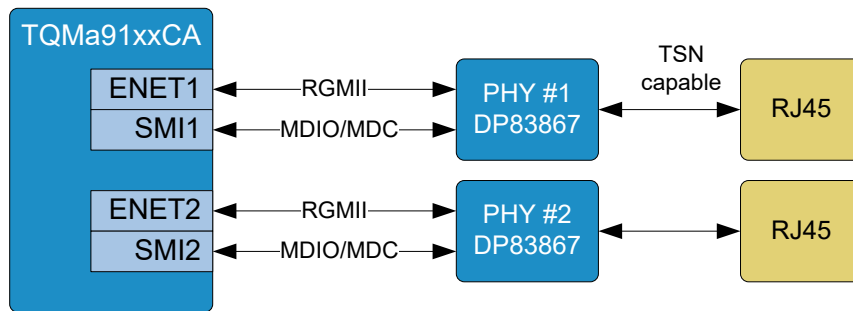


Figure 9: Block diagram Ethernet

The PHY DP83867 has configurable GPIO signals, which can be used for SFD (Start of Frame) detection outputs for debug purposes, among other things. For the TSN-enabled Ethernet interface, these pins are provided on pin header X5 on the MBa91xxCA.

Both transceivers are each connected with their own reset and interrupt signals. For the interrupt signals two GPIO signals of the TQMa91xxCA are used. For the reset signals two IO-Signals of the I2C3 port expander of the MBa91xxCA are used. The following table shows the signals used.

Table 14: Ethernet reset and interrupt signals

Ethernet port	Transceiver function	MBa91xxCA signal	TQMa91xxCA signal	MBa91xxCA I2C3 address	Remark
Ethernet 1	Interrupt output (Pin: INT)	ENET1_INT#	GPIO3_IO26	–	Low-active / pulled-up to V_1V8
	Reset input (Pin: RESET#)	ENET1_RESET#	–	0x71, IO_0	Low-active
Ethernet 2	Interrupt output (Pin: INT)	ENET2_INT#	GPIO3_IO27	–	Low-active / pulled-up to V_1V8
	Reset input (Pin: RESET#)	ENET2_RESET#	–	0x71, IO_1	Low-active

The Transceiver DP83867 has boot straps to start with configurable default values.

The standard configuration on the MBa91xxCA is shown in the following table, alternatively, these can be changed via register settings or via placement options.

Table 15: Standard configuration of Ethernet transceivers (boot straps)

Config-Pin on Ethernet-Transceiver ⁽¹⁾	Default MBa91xxCA Mode ⁽²⁾	Description
RX_D0	1	Addresses for Management Interface (SMI): Transceiver #1 - 0b0000 Transceiver #2 - 0b0000
RX_D2	1	
RX_CTRL	3	Autonegotiation enabled
GPIO_0	1	RGMII RX CLOCK SKEW = 2.0 ns
GPIO_1	1	
LED_2	1	RGMII TX CLOCK SKEW = 2.0 ns
LED_1	1	Mode 10/100/1000 Mbit/s available (ANEG_SEL = 0)
LED_0	1	
		Port Mirroring disabled, SGMII Mode disabled

1: Identical for both transceivers unless explicitly stated.

2: A detailed description of the modes and their configuration can be found in data sheet (5)

The activity status of the respective Ethernet port is indicated by the LEDs in the RJ45 sockets. The table shows the default configuration. This can be adapted via register settings in the transceivers. The status messages are identical for both Ethernet ports.

Table 16: Ethernet-LEDs

LED	Colour	Function / Indication
LED left	Green	Connection is established
LED right	Yellow	Send and receive activity

3.8.4 WLAN

A WLAN module is available on the MBa91xxCA in the M.2 Type 1216 form factor (solder module). It supports IEEE 802.11 ac/a/b/g/n and offers a dual-band RF interface (2.4 / 5 GHz). The antennas have to be connected separately to the MHF4 sockets of the module and are not part of the MBa91xxCA.

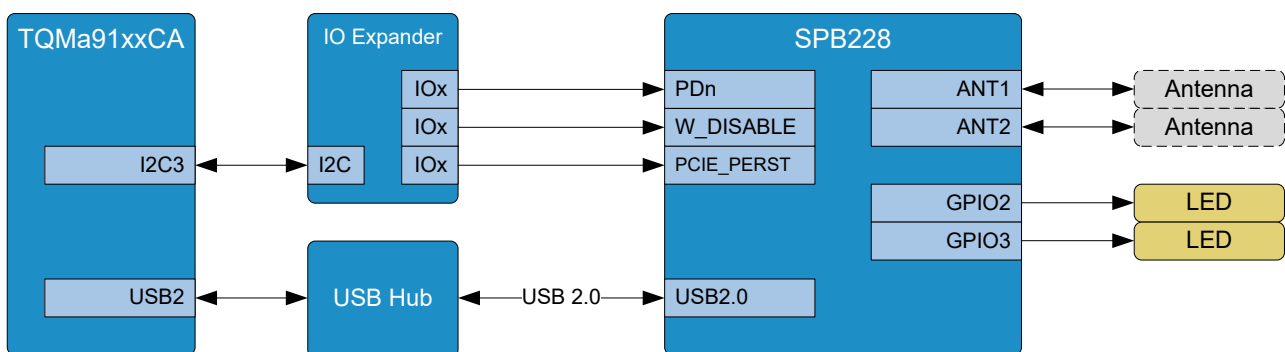


Figure 10: Block diagram WLAN

The module is connected via USB 2.0. However, the theoretically achievable maximum data rate of the SPB228 of 866 Mbit/s is reduced due to the connection via USB2.0. The host interface configuration of the SPB228 must be done for USB 2.0 as follows:

Table 17: SPB288 host interface configuration

CONFIG_HOST[2:0]	WLAN interface	Mobile Network Interface	Driver Name
101	USB 2.0	USB 2.0	linux-usb-driver-228

3.8.5 LVDS / RGB

The i.MX91 processor has no LVDS interface. To provide a display interface on the MBa91xxCA, the LVDS connector (X12) of the MBa91xxCA is connected to the 24-bit RGB interface of the i.MX91 via a LVDS bridge. An additional CMD connector (X11) is also provided on the MBa91xxCA to provide supply voltages, a USB interface as well as display and backlight control signals. In addition, the RGB signals are available at pin header X3.

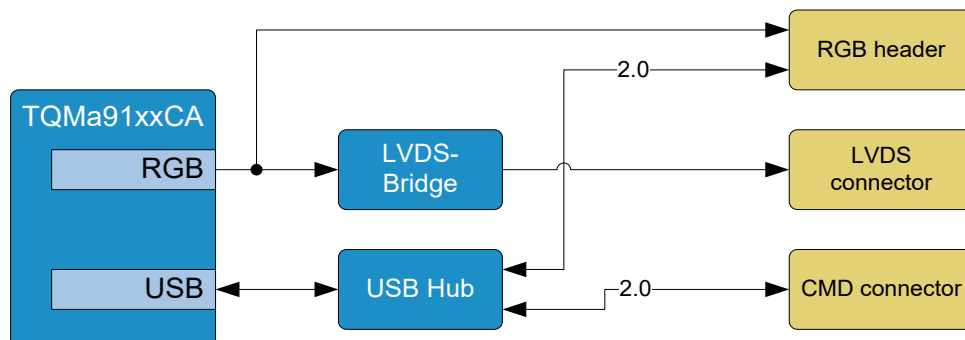


Figure 11: Block diagram LVDS / RGB

Table 18: Pinout LVDS (X12)

Pin	Signal	Dir.	Level	Remark
1	LVDS_DATA0-	O	1.8 V	LVDS interface (Lane 0)
2	LVDS_DATA0+	O	1.8 V	
3	LVDS_DATA1-	O	1.8 V	LVDS interface (Lane 1)
4	LVDS_DATA1+	O	1.8 V	
5	LVDS_DATA2-	O	1.8 V	LVDS interface (Lane 2)
6	LVDS_DATA2+	O	1.8 V	
7	GND	P	0 V	Ground
8	LVDS_CLOCK-	O	1.8 V	LVDS interface (Clock)
9	LVDS_CLOCK+	O	1.8 V	
10	LVDS_DATA3-	O	1.8 V	LVDS interface (Lane 3)
11	LVDS_DATA3+	O	1.8 V	
12	(NC)	O	1.8 V	-
13	(NC)	O	1.8 V	
14	GND	P	0 V	Ground
15	(NC)	O	1.8 V	-
16	(NC)	O	1.8 V	
17	GND	P	0 V	Ground
18	(NC)	O	1.8 V	-
19	(NC)	O	1.8 V	
20	(NC)	O	1.8 V	-
21	(NC)	O	1.8 V	
22	(NC)	O	1.8 V	-
23	(NC)	O	1.8 V	
24	GND	P	0 V	Ground
25	V_5V_LVDS	P	5 V	5 V supply voltage (1 A max. output)
26	V_5V_LVDS	P	5 V	
27	V_5V_LVDS	P	5 V	
28	V_3V3_LVDS	P	3.3 V	3.3 V supply voltage (1 A max. output)
29	V_3V3_LVDS	P	3.3 V	
30	V_3V3_LVDS	P	3.3 V	
M1, M2	GND	P	0 V	Ground

Table 19: Pinout CMD (X11)

Pin	Signal	Dir.	Level	Remark
1	V_12V	P	12 V	12 V supply voltage (1 A max.)
2	V_12V	P	12 V	
3	V_12V	P	12 V	
4	GND	P	0 V	Ground
5	GND	P	0 V	
6	GND	P	0 V	
7	V_5V	P	5 V	5 V supply voltage (1 A max.)
8	V_5V	P	5 V	
9	GND	P	0 V	Ground
10	GND	P	0 V	
11	V_USB_H4_VBUS	P	5 V	VBUS USB Host 4 (0.5 A max.)
12	GND	P	0 V	Ground
13	USBH4_D-	I/O	3.3 V	Data USB Host 4
14	USBH4_D+	I/O	3.3 V	
15	GND	P	0 V	Ground
16	LCD_RESET#	O _{PD}	3.3 V	Reset
17	LCD_BLT_EN	O _{PD}	3.3 V	Backlight-Enable
18	LCD_PWR_EN	O _{PD}	3.3 V	Power-Enable
19	LCD_PWM	O	3.3 V	PWM Contrast-/ Brightness
20	GND	P	0 V	Ground
M1, M2	GND	P	0 V	Ground

Table 20: Pinout RGB (X3)

Signal	Pin	Pin	Signal
V_12V	1	2	V_3V3
V_5V_MB	3	4	
GND	5	6	GND
LCD_PCLK	7	8	LCD_DE
LCD_HSYNC	9	10	LCD_D01
LCD_VSYNC	11	12	LCD_D03
LCD_D00	13	14	LCD_D05
LCD_D02	15	16	LCD_D07
LCD_D04	17	18	LCD_D09
LCD_D06	19	20	LCD_D11
LCD_D08	21	22	LCD_D13
LCD_D10	23	24	LCD_D15
LCD_D12	25	26	LCD_D17
LCD_D14	27	28	LCD_D19
LCD_D16	29	30	LCD_D21
LCD_D18	31	32	LCD_D23
LCD_D20	33	34	V_VBUS_H7
LCD_D22	35	36	USBH7_D-
GND	37	38	USBH7_D+
I2C3_SCL	39	40	GND
I2C3_SDA	41	42	NC
NC	43	44	NC
NC	45	46	NC
LCD_INT#	47	48	GND
LCD_PWR_EN	49	50	LCD_BLT_EN
LCD_RESET#	51	52	LCD_PWM
GND	53	54	GND
NC	55	56	NC
NC	57	58	NC
GND	59	60	GND

3.8.6 Mini PCIe

The pinout of the Mini PCIe connector is implemented according to the standard. A USB 2.0 interface of the USB hub is used as host interface. PCIe is not connected, since this is not available with the i.MX91 CPU. As a placement option, the UART interface can also be used, for example, for the IoT (LTE) plug-in card "BG95-M3 Mini PCIe" from Quectel.

As the I²C interface is not specified in conformity with the standard for many LTE cards available on the market, the I²C signals are separated from the connector by OR bridges. A micro SIM card slot is provided for wireless cards.

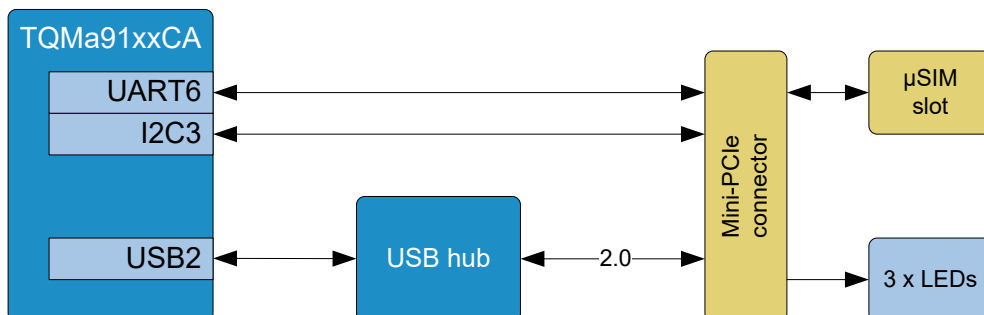


Figure 12: Block diagram Mini PCIe

Table 21: Pinout Mini PCIe (X16)

Pin	Signal	Dir.	Level	Remark
1	PCIE_WAKE#	I	3.3 V	Wake-Up-Signal of Mini PCIe card
2	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
3	(NC)	–	–	Not connected / reserved
4	GND	P	0 V	Ground
5	(NC)	–	–	Not connected / reserved
6	V_1V5_MPCIE	P	1.5 V	1.5 V supply voltage
7	(NC)	–	–	Not connected / reserved
8	UIM_PWR	O	– ⁽¹⁾	Supply voltage for SIM card
9	GND	P	0 V	Ground
10	UIM_DATA	I/O	– ⁽¹⁾	Bidirectional data line for SIM card
11	MPCIE_UART_TX	O	3.3 V	optional UART for use of BG95-M3 Mini-PCIe card
12	UIM_CLK	O	– ⁽¹⁾	Clock output for SIM card
13	MPCIE_UART_RX	I	3.3 V	optional UART for use of BG95-M3 Mini-PCIe card
14	UIM_RST	O	– ⁽¹⁾	Reset output for SIM card
15	GND	P	0 V	Ground
16	UIM_VPP	O	– ⁽¹⁾	Programming voltage for SIM card
17	(NC)	–	–	Not connected / reserved
18	GND	P	0 V	Ground
19	(NC)	–	–	Not connected / reserved
20	MPCIE_WDISABLE#	O	3.3 V	Disable signal for Mini PCIe card
21	GND	P	0 V	Ground
22	MPCIE_PERST#	O	3.3 V	Power-Good of Mini PCIe card
23	(NC)	–	–	Not connected / reserved
24	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
25	(NC)	–	–	Not connected / reserved
26	GND	P	0 V	Ground
27	GND	P	0 V	Ground
28	V_1V5_MPCIE	P	1.5 V	1.5 V supply voltage
29	GND	P	0 V	Ground
30	I2C3_SCL_3V3	O _{PU}	3.3 V	I ² C clock (I2C3_SCL level shifted)
31	(NC)	–	–	Not connected / reserved
32	I2C3_SDA_3V3	I/O _{PU}	3.3 V	I ² C data (I2C3_SDA level shifted)
33	(NC)	–	–	Not connected / reserved
34	GND	P	0 V	Ground
35	GND	P	0 V	Ground
36	USBH5_D–	I/O	3.3 V	Data USB Host 1
37	GND	P	0 V	Ground
38	USBH5_D+	I/O	3.3 V	Data USB Host 1
39	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
40	GND	P	0 V	Ground
41	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage
42	LED_WWAN#	I	3.3 V	Status input WWAN# (see chapter 3.9.4)
43	GND	P	0 V	Ground
44	LED_WLAN#	I	3.3 V	Status input WLAN# (see chapter 3.9.4)
45	(NC)	–	–	Not connected / reserved
46	LED_WPAN#	I	3.3 V	Status input WPAN# (see chapter 3.9.4)
47	(NC)	–	–	Not connected / reserved
48	V_1V5_MPCIE	P	1.5 V	1.5 V supply voltage
49	(NC)	–	–	Not connected / reserved
50	GND	P	0 V	Ground
51	(NC)	–	–	Not connected / reserved
52	V_3V3_MPCIE	P	3.3 V	3.3 V supply voltage

3.8.7 SIM card

A Micro-SIM card holder (X18) is available on the MBa91xxCA for the use of a SIM card, which is directly connected to the Mini PCIe interface.

1: Depending on the Mini PCIe card used.

3.8.8 USB Type-C

TQMa91xxCA has a USB Type-C interface. A corresponding USB Power Delivery Controller controls the VBUS switch. VBUS is used on the MBa91xxCA only as source (supply of an external device), not as sink (supply of mainboard from VBUS). The current limitation is fixed at approx. 500 mA.

This interface is connected to the USB1 port of the i.MX91. The Serial Download Mode is possible.

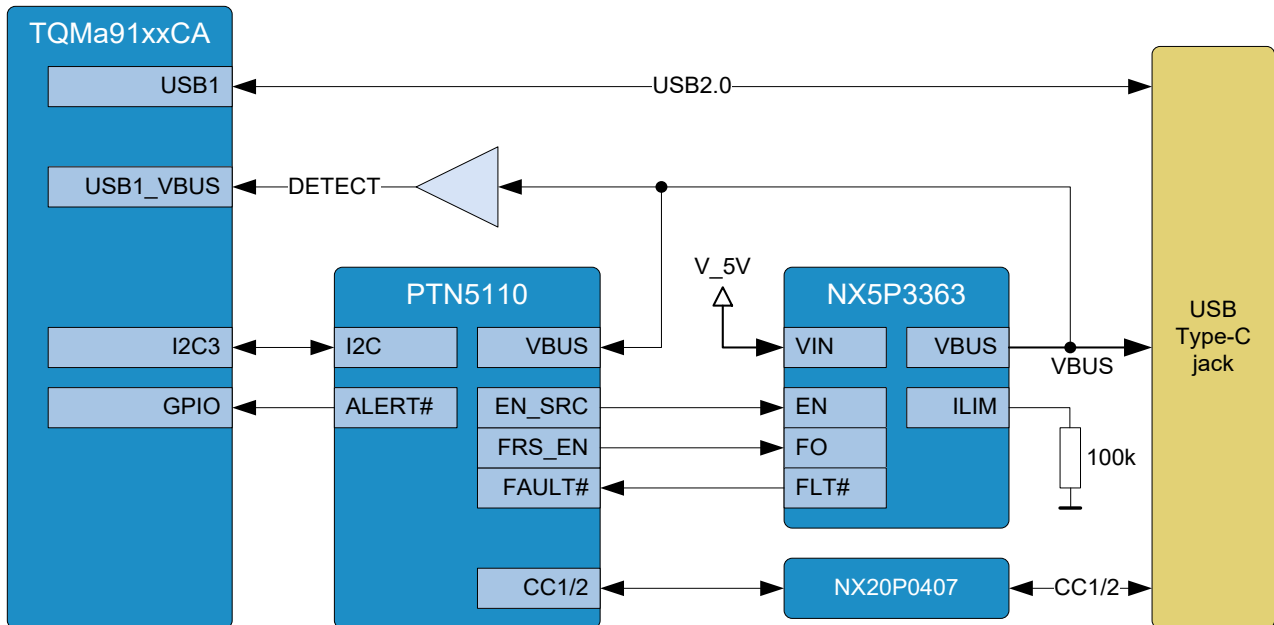


Figure 13: Block diagram USB Type-C

3.8.9 Micro-SD card

The micro SD card connector is directly connected to the uSDHC2 interface of the TQMa91xxCA. A 4-bit wide data interface is used. The uSDHC controller in the i.MX91 supports UHS-I mode.

The switching of the IO voltage is performed by the module-internal signal SD2_VSELECT. No measures are necessary on the mainboard for this. The SD card is supplied with V_3V3_SD, which is provided by the TQMa91xxCA.

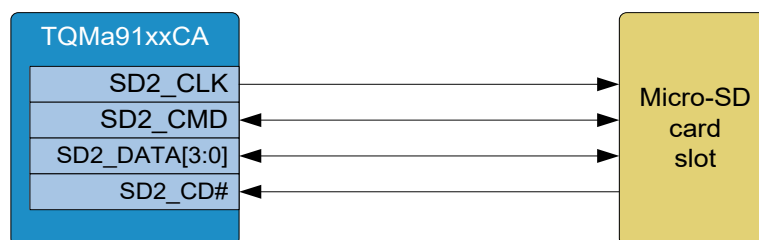


Figure 14: Block diagram Micor-SD card

3.8.10 RS485

On the MBa91xxCA a RS485 interface (halfduplex) is realized. This interface is not galvanically isolated. It is connected to the UART2 interface of the TQMa91xxCA. The RTS signal of the UART interface (possibly used as GPIO) is used for automatic direction switching.

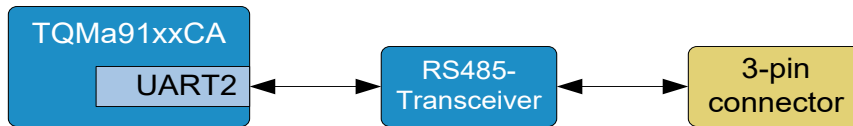


Figure 15: Block diagram RS485

The bus termination for RS485 is done via DIP switch S6. By default the termination components are equipped to use it for RS485 bus. There is a assembly option to use a Profibus compliant termination. The assembly option is documented in the MBa91xxCA schematic.

The RS485 Bus is provided at a 3-pin connector.

Table 22: Pinout RS485 (X10)

Pin	Signal
1	RS485_A
2	RS485_B
3	GND

Table 23: Termination switch S6

S6-1	S6-2	Modus
OFF	OFF	No bus termination
OFF	ON	Not defined (irregular state)
ON	OFF	Not defined (irregular state)
ON	ON	Bus terminated

3.8.11 MBa91xxCA headers (X1, X2)

The MBa91xxCA provides a 100 mil extension header (X2) and optionally a 50 mil header (X1).

Besides the signals, 1.8 V, 3.3 V, 5 V and 12 V are available at X2. The maximum current is divided among all pin headers as well as the connectors of LVDS and for the fan. In total, no more than the specified maximum current may be drawn at the following interfaces:

Table 24: Power consumption headers

Rail	I _{max}	Remark
V_12V	2 A	Sum of currents at X2, X3, X11 and X25
V_5V_MB	2 A	Sum of currents at X2, X3, X11, X12 and X25
V_3V3	2 A	Sum of currents at X2, X3 and X12
V_1V8	250 mA	Sum of currents at X2

Note: Observe power consumption with regard to the overall system



The supply voltages (1.8 V, 12 V, etc.) provided at the MBa91xxCA headers are not individually fused. Technically, an overload of the fuse at the 24 V supply input is therefore possible, see also chapter 3.10.

Please note the resulting total current consumption of the MBa91xxCA, which must be less than 5 A!

Table 25: Pinout extension header X1

Level	Signal	Pin		Signal	Level
3.3 V	ISO_7816_RST	1	2	V_3V3	3.3 V
3.3 V	ISO_7816_IO1	3	4	CLK3_OUT	1.8 V
3.3 V	ISO_7816_IO2	5	6	CLK4_OUT	1.8 V
0 V	GND	7	8	GND	0 V
3.3 V	ISO_7816_CLK	9	10	NC	-

Table 26: Pinout extension header X2

Level	Signal	Pin		Signal	Level
12 V	V_12V	1	2	V_3V3	3.3 V
5 V	V_5V_MB	3	4	V_1V8	1.8 V
0 V	GND	5	6	GND	0 V
3.3 V	RESET_OUT#	7	8	ADC_IN0	1.8 V
1.8 V	PMIC_RST#	9	10	ADC_IN1	1.8 V
3.3 V	PMIC_WDOG_IN#	11	12	ADC_IN2	1.8 V
3.3 V	WD0G_ANY	13	14	ADC_IN3	1.8 V
0 V	GND	15	16	GND	0 V
1.8 V	SD3_CMD	17	18	I2C1_SDA	3.3 V
1.8 V	SD3_DATA3	19	20	I2C1_SCL	3.3 V
1.8 V	SD3_DATA2	21	22	GND	0 V
1.8 V	SD3_DATA1	23	24	I2C3_SDA	3.3 V
1.8 V	SD3_DATA0	25	26	I2C3_SCL	3.3 V
0 V	GND	27	28	ENET1_EVENT0_IN	V_SD2
1.8 V	SD3_CLK	29	30	ENET1_EVENT0_OUT	V_SD2
0 V	GND	31	32	TEMP_EVENT_MOD#	3.3 V
1.8 V	TAMPER0	33	34	TEMP_EVENT_MB#	3.3 V
1.8 V	TAMPER1	35	36	RTC_EVENT#	3.3 V
0 V	GND	37	38	GND	0 V
1.8 V	CLK2_IN	39	40	CLK1_IN	1.8 V

3.8.12 JTAG

The JTAG interface is routed to a 10-pin header (X20). The required pull-ups of the lines TDI, TMS, and SRST# are available on the MBa91xxCA. All signal lines use 1.8 V as reference voltage. The JTAG interface is not ESD protected.

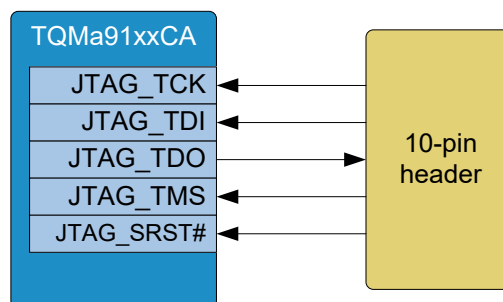


Figure 16: Block diagram JTAG

Table 27: Pinout JTAG (X20)

Remark	Level	Dir.	Signal	Pin	Pin	Signal	Dir.	Level	Remark
Test Mode Select	1.8 V	I _{PU}	JTAG_TMS	2	1	V_1V8	P	1.8 V	1.8 V
Test Clock	1.8 V	I _{PD}	JTAG_TCK	4	3	GND	P	0 V	Ground
Test Data Out	1.8 V	O	JTAG_TDO	6	5	GND	P	0 V	Ground
Test Data In	1.8 V	I _{PU}	JTAG_TDI	8	7	(NC)	–	–	Not used
System Reset	1.8 V	I/O _{PU}	JTAG_SRST#	10	9	GND	P	0 V	Pulled to ground

3.8.13 Fan

If active cooling is required, a fan connection is provided. The fan is controlled by external signals at header X9. The fan is connected to a 4-pin Molex connector and is supplied with 12 V as standard. Optionally, 5 V can be used via placement option. The fan is attached to the optional heat sink of the TQMa91xxCA. Mounting holes are provided on the mainboard identical to the module.

Table 28: Pinout fan header (X25)

Signal	Pin
GND	1
V_FAN	2
RPM	3
PWM	4

Table 29: Pinout external fan control (X9)

Signal	Pin
RPM	1
PWM	2

3.9 User interfaces

3.9.1 Reset button

Reset button S2 resets the PMIC and CPU on the TQMa91xxCA. The generated reset signal simultaneously activates the RESET_OUT# signal, which also resets various components on the MBa91xxCA.

3.9.2 On/Off button

Button S3 is directly connected to pin ONOFF of the TQMa91xxCA. Pressing the button triggers the ON/OFF function of the i.MX 91.

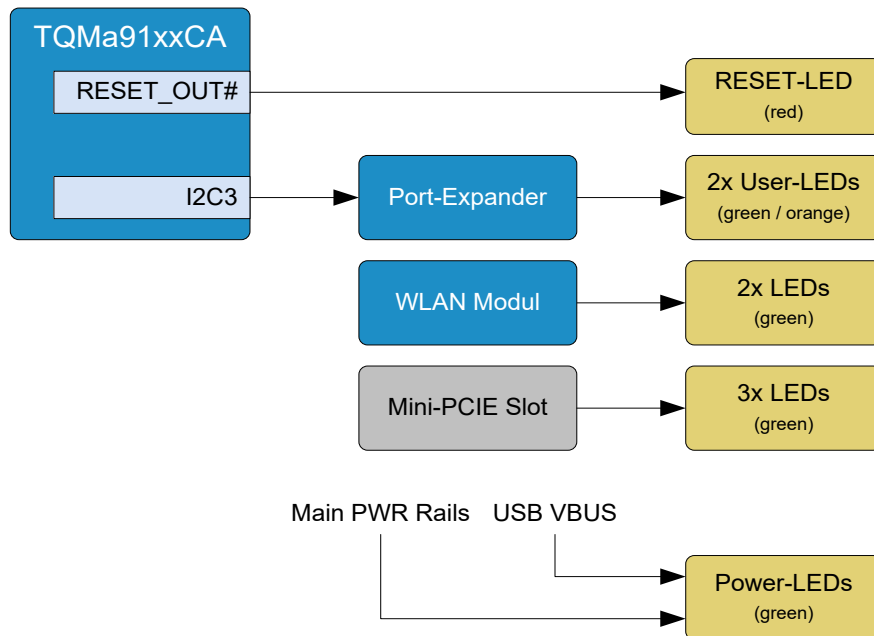
3.9.3 GPI buttons

Two buttons (S8, S9) are available on the MBa91xxCA for user-specific use. They are connected to the IO expander.

Table 30: General Purpose buttons

Button	Signal
S8	Button_A#
S9	Button_B#

3.9.4 Status LEDs



In addition to the status LEDs of the two Ethernet sockets, the MBa91xxCA provides more indicator LEDs:

Table 31: Status-LEDs

Function group	LED	Colour	Indication
Reset	V1	Red	Indicates the reset status of the des TQMa91xxCA (at signal RESET_OUT#)
USB	V5	Green	Indicates the presence of VBUS for USB Host 1
	V6	Green	Indicates the presence of VBUS for USB Host 2
	V22	Green	Indicates the presence of VBUS for USB Host 4 (LVDS-CMD)
	V27	Green	Indicates the presence of VBUS for USB Host 7 (RGB pin header)
	V7	Green	Indicates the presence of VBUS for USB Type C
Ethernet	X6	Green/yellow	Shows the status of Link/Activity
	X7	Green/yellow	Shows the status of Link/Activity
WLAN	V8	Green	Shows the status of the WLAN# signal on the WLAN module
Mobile Network	V9	Green	Shows the status of the BT# signal on the WLAN module
Mini PCIe	V10	Green	Shows the status of the WWAN# signal on the Mini-PCIE interface
	V11	Green	Shows the status of the WLAN# signal on the Mini-PCIE interface
	V12	Green	Shows the status of the WPAN# signal on the Mini-PCIE interface
User LEDs	V2	Green	Programmable LED (User LED1) on I ² C GPIO Expander ⁽¹⁾
	V3	Orange	Programmable LED (User LED2) on I ² C GPIO Expander ⁽¹⁾
SD Card	V4	Green	Indicates the presence of the internal 3.3 V supply voltage (V_3V3_SD)
Power ⁽²⁾	V14	Green	Indicates the presence of the external 24 V supply voltage (V_24V)
	V15	Green	Indicates the presence of the internal 12 V supply voltage (V_12V)
	V16	Green	Indicates the presence of the internal 5 V supply voltage (V_5V)
	V17	Green	Indicates the presence of the internal 5 V supply voltage (V_5V_MB)
	V18	Green	Indicates the presence of the internal 3.3 V supply voltage (V_3V3)
	V19	Green	Indicates the presence of the internal 1.8 V supply voltage (V_1V8)
	V20	Green	Indicates the presence of the internal 5 V supply voltage (V_5V_MPCIE)
Debug	V21	Green	Indicates the presence of the internal 1.5 V supply voltage (V_1V5_MPCIE)
	V13	Green	Indicates the presence of an external USB supply voltage on X22

1: For further information, see chapter 3.4.

2: For details on the supply concept and the distribution of the internal supply voltages, refer to chapter 3.10.

3.10 Power supply

The MBa91xxCA must be supplied with 24 V DC (typ.) via one of the two connections X23 and X24, which can be used alternatively.

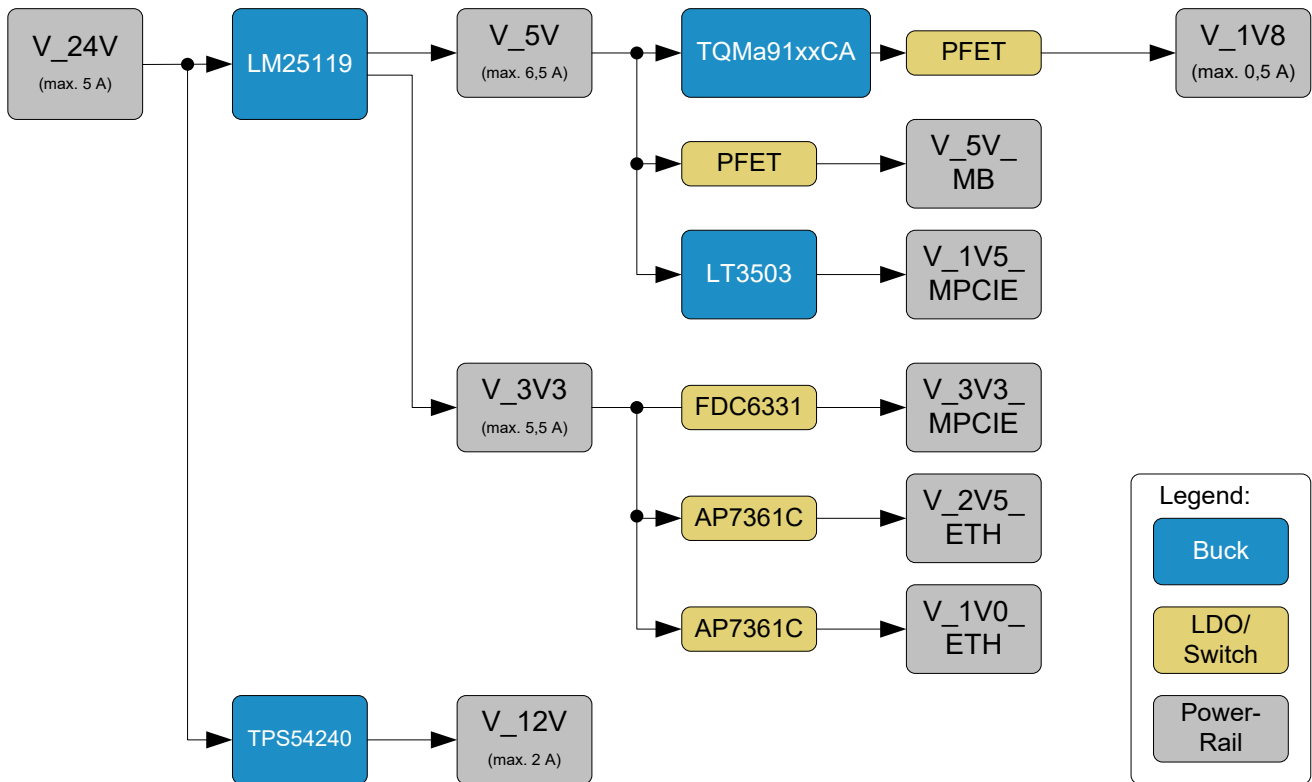


Figure 17: Block diagram MBa91xxCA power supply

Figure 19 shows all voltages (rails) on the MBa91xxCA, which are divided into three main paths consisting of two LM25119 and one TPS54240. These supply the largest loads (TQMa91xxCA, USB supply, 12 V display supply)

The design also allows power sequencing of all voltage levels used. With the exception of V_5V, all voltages are switched on after the TQMa91xxCA boots. A 1.8 V supply is already provided by the TQMa91xxCA and delivers up to 500 mA.

3.10.1 Input protection

The following protective circuits are provided for the input voltage V_24V of the MBa91xxCA:

- Fuse 5 A, slow blow
- Overvoltage protection
- PI Filter (CLC element)
- Reverse polarity protection
- Voltage stabilization

Attention: Voltages at headers



The internal voltages (1.8 V, 12 V, etc.) provided at the MBa91xxCA headers are not separately fused. Technically an overload of the fuse is therefore possible. The resulting total current consumption of the MBa91xxCA should be kept below 5 A in total.

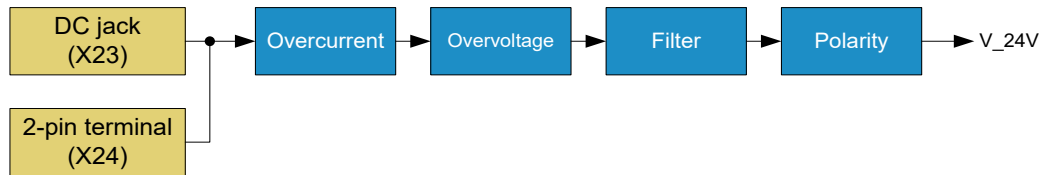


Figure 18: Block diagram Power-In

Table 32: Supply voltage V_24V_IN at Power-In (X23, X24)

Parameter	Min.	Typ.	Max.	Remark
Input voltage	16 V	24 V	30 V	–
Power consumption	–	TBD ⁽¹⁾	TBD ⁽²⁾	–
Rated current of the fuse	–	5 A	–	–
Voltage limitation in case of overvoltage	TBD	–	TBD	Note: The MBa91xxCA may be damaged in case of permanent overvoltage!

Table 33: Pinout Power-In (X23, X24)

Pin	Pin	Signal	Type	Level	Remark
X23	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground
	3	(NC)	–	–	Not connected
X24	1	V_24V_IN	P	24 V	24 V supply voltage
	2	GND	P	0 V	Ground

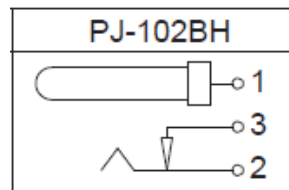


Figure 19: Pinout DC socket 2.5 mm/6.5 mm

1: Typical scenario is not defined.

2: Theoretical full load. All supply voltages are loaded with maximum current, e.g. by connecting additional load to the pin headers, and all system components have maximum power consumption.

3.10.2 Power sequencing

The following figure shows the power-on sequences of the different voltage levels of the mainboard, without taking into account the rise times of the voltages:

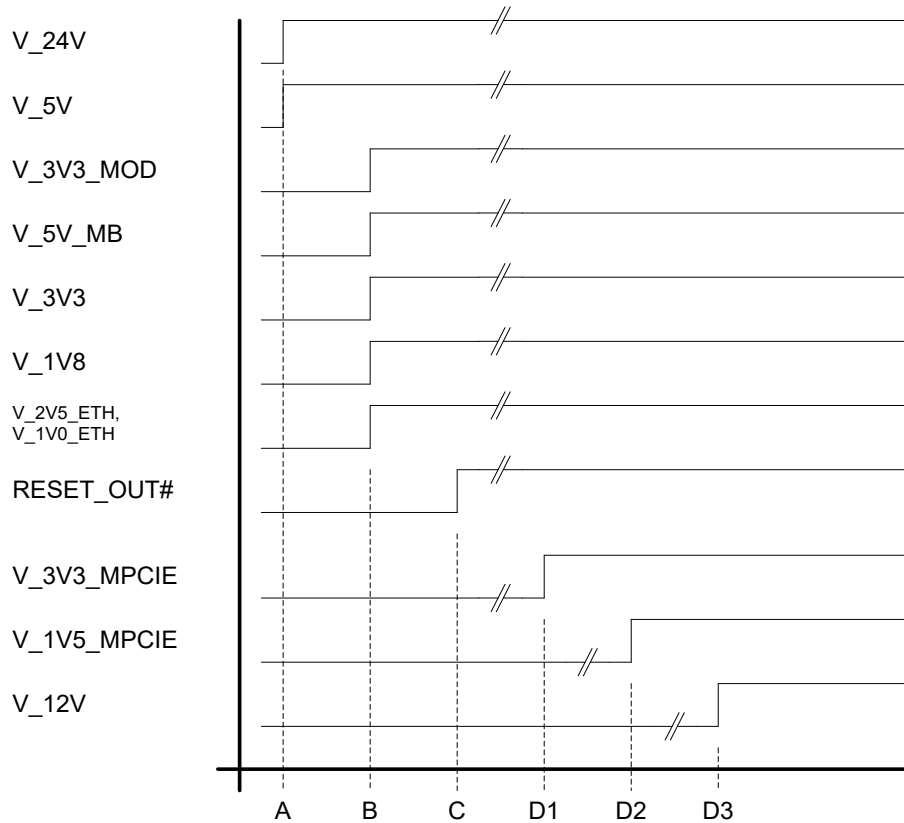


Figure 20: Power sequencing MBa91xxCA

The following table shows the sequence steps from Figure 22:

Table 34: Power sequencing

Sequence	Time	Description
A	–	Start point: Power-up MBa91xxCA supplies.
B	174...494 ms (t_B)	Release MBa91xxCA supplies by V_3V3_MOD as last part of the internal power sequence of the TQMa91xxCA.
C	$t_B + 22$ ms	Release RESET_OUT# after completion of TQMa91xxCA power sequencing plus preconfigured delay.
D1, D2, D3	Software dependent	Switching on of additional supply by software driver with signals MPCIE_3V3_EN, MPCIE_1V5_EN und 12V_EN.

V_3V3_MOD controls the second regulator of the LM25119 (V_3V3) as well as the power FET for V_5V_MB and V_1V8 by means of supervisor. Automatically the two AP7361 for V_1V0_ETH and V_2V5_ETH are activated.

Determined by the internal power sequence of the TQMa91xxCA, RESET_OUT# is only released with a corresponding time offset (22 ms) after the last voltage level V_3V3_MOD (TQMa91xxCA internal V_3V3) is switched on. Thus, all necessary voltages on the TQMa91xxCA and the carrier board are stable when the system starts.

3.10.3 V_5V and V_3V3

3.3 V and 5 V are required to supply the TQMa91xxCA, some components on the mainboard and the USB voltage. The dual regulator LM25119 is used for this purpose, which generates the two voltages from the 16...30 V input voltage.

The voltage V_5V is automatically activated when the mainboard supply is switched on and supplies the TQMa91xxCA. V_3V3 is activated after completion of the module-internal power sequencing with the V_3V3_MOD provided by the module by means of supervisor (LM25119 pin EN2). The designs have the following specification:

Table 35: Specifications V_5V and V_3V3

Voltage	Parameter	Value	Remark
V_5V	V _{IN}	16...30 V	V_24V
	V _{OUT}	4.91...5.08 V	V_5V
	I _{OUT}	6.5 A	Load: 5.45 A (realistic use case)
V_3V3	V _{IN}	16...30 V	V_24V
	V _{OUT}	3.25...3.35 V	V_3V3
	I _{OUT}	5.5 A	Load: max. 4.74 A (realistic use case)

3.10.4 V_5V_MB

Besides the module, the mainboard needs a 5 V supply for some components. This voltage V_5V_MB is switched on after completion of the module-internal power sequencing.

Components whose power is not switched via separate enable signals are supplied from V_5V_MB. The power distribution switches for USB and the DCDC for V1V5_MPCIE are powered directly from V_5V.

3.10.5 V_1V8

Because the power requirement by the components on the mainboard for 1.8 V is very low, the 1.8 V provided by the TQMa91xxCA is used for V_1V8. The module supplies up to 500 mA. A maximum of 250 mA of this remains for the starter kit header. As the 1.8 V are switched on by the module at an early stage in sequencing, they must be activated with a delay for the mainboard components. Otherwise, the power timing of the Ethernet PHYs will be violated. The supervisor, similar to V_5V_MB, switches on V_1V8.

3.10.6 V_3V3_MPCIE

The 3.3 V of the Mini-PCIe interface is switchable via a loadswitch. This is necessary because the Mini PCIe standard has certain power sequencing requirements. The switch can be enabled by software using a GPIO signal.

The design has the following specification:

Table 36: Specification V_3V3_MPCIE

Voltage	Parameter	Value	Remark
V_3V3_MPCIE	V _{IN}	3.25...3.35 V	V_3V3
	V _{OUT}	3.12...3.35 V	V_3V3_MPCIE
	I _{OUT}	max. 1.1 A	

3.10.7 V_1V5_MPCIE

1.5 V are required for the Mini PCIe interface. A switching regulator provides these from V_5V. It can supply a maximum of 750 mA. The regulator can be switched by software using GPIO signal.

The design has the following specification:

Table 37: Specification V_1V5_MPCIE

Voltage	Parameter	Value	Remark
V_1V5_MPCIE	V _{IN}	4.91...5.08 V	V_5V
	V _{OUT}	1.46...1.55 V	V_1V5_MPCIE
	I _{OUT}	max. 0.75 A	Load: max. 375 mA

3.10.8 V_1V0_ETH

The voltage of 1.0 V required for the Ethernet PHYs is generated from V_3V3.

Table 38: Specification V_1V0_ETH

Voltage	Parameter	Value	Remark
V_1V0_ETH	V _{IN}	3.25...3.35 V	V_3V3
	V _{OUT}	0.97...1.03 V	V_1V0_ETH
	I _{OUT}	250 mA	

3.10.9 V_2V5_ETH

Among other things, the Ethernet PHYs require a supply voltage of 2.5 V, which is generated from V_3V3 for both PHYs. The supply of the PHYs is thus automatically started after the boot process.

Table 39: Specification V_2V5_ETH

Voltage	Parameter	Value	Remark
V_1V2_DP	V _{IN}	3.25...3.35 V	V_3V3
	V _{OUT}	2.44...2.56 V	V_2V5_ETH
	I _{OUT}	320 mA	Load: max. 170 mA

3.10.10 V_12V

A voltage of 12 V is required for the backlight supply at the LVDS, the fan as well as the pin header of the starter kit, which is specified with 2 A in total. The voltage is generated from V_24V by a step-down converter. The controller can be switched on or off via GPIO signal by software.

The design has the following specification:

Table 40: Specification V_12V

Voltage	Parameter	Value	Remark
V_12V	V _{IN}	16...30 V	V_24V
	V _{OUT}	11.660...12.471 V	V_12V
	I _{OUT}	2 A	

3.11 Reset & Configuration

Figure 23 shows the reset structure on the MBa91xxCA.

In addition to the reset signals of the TQMa91xxCA, the MBa91xxCA also provides further software-controlled reset signals for individual function blocks, e.g. ENET reset for the Ethernet transceivers. These are implemented by GPIO signals and named accordingly in the respective chapters when applicable.

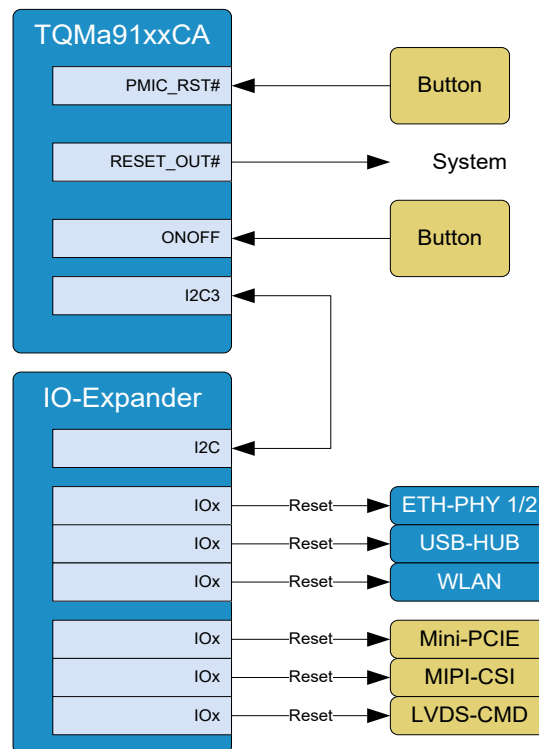


Figure 21: Block diagram Reset & Configuration

The following signals from the TQMa91xxCA are used on the MBa91xxCA:

Table 41: Reset signals

Signal	Type	Level	Remark
PMIC_RST#	I	1.8 V	<ul style="list-style-type: none"> • activates RESET of the PMIC (low-active) • reset behavior of PMIC configurable (see data sheet) • no pull-up on mainboard necessary • connect to GND for activation (push button)
RESET_OUT#	O	-	<ul style="list-style-type: none"> • open drain output (low-active) • activates RESET of mainboard components • requires pull-up on mainboard (max. 5.5 V)
ONOFF	I	1.8 V	<ul style="list-style-type: none"> • ON/OFF function of the i.MX91 (see data sheet) • no pull-up on mainboard necessary • connect to GND to activate (push button)

Pushbuttons are connected to PMIC_RST# and ONOFF.

RESET_OUT is connected with a pull-up to V_3V3 and resets followed blocks:

- IO Expander
- Analog switch for boot mode signals
- External components at starter kit headers

The reset signal is linked to an LED.

4. SOFTWARE

No software is required for the MBa91xxCA.

Suitable software is only required on the TQMa91xxCA and is not a part of this Preliminary User's Manual.

More information can be found in the [TQ-Support Wiki for the TQMa91xx](#).

5. MECHANICS

5.1 MBa91xxCA dimensions

The MBa91xxCA has overall dimensions (length × width × height) of 170 mm × 170 mm × TBD mm.

The MBa91xxCA has six 4.2 mm mounting holes for the housing, and four 2.7 mm mounting holes for a heat sink.

The MBa91xxCA weighs approximately TBD grams without TQMa91xxCA.

5.2 Notes of treatment

The TQMa91xxCA is held in the mating connectors with a retention force of >24 N.

To avoid damaging the TQMa91xxCA connectors as well as the carrier board connectors while removing the TQMa91xxCA the use of the extraction tool MOZIA6UL REV.0100 is strongly recommended.

Note: Component placement on carrier board



2.5 mm should be kept free on the carrier board, on both long sides of the MBa91xxCA for the extraction tool MOZIA6UL REV.0100.

5.3 Embedding in the target system

The MBa91xxCA serves as a design base for customer products, as well as a reference platform during development.

5.4 Housing

The form factor and the mounting holes of the MBa91xxCA are designed for installation in a standard Mini-ITX housing.

5.5 Thermal management

The largest power dissipation on the MBa91xxCA is caused by the voltage regulators. In addition, the TQMa91xxCA is a heat source that acts indirectly on the MBa91xxCA. Depending on the application, further power dissipation can occur, mainly at additional external loads on the pin headers on the MBa91xxCA, the Mini PCIe slot, etc.

For evaluation of the TQMa91xxCA under high load conditions an optional heat sink is provided. Four holes are provided on the MBa91xxCA for this purpose. A connector is available on the MBa91xxCA for connecting an optional fan.

Attention: TQMa91xxCA heat dissipation



The i.MX 91 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa91xxCA must be taken into consideration when connecting the heat sink. The TQMa91xxCA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa91xxCA or the MBa91xxCA and thus malfunction, deterioration or destruction.

5.6 Assembly & Labels

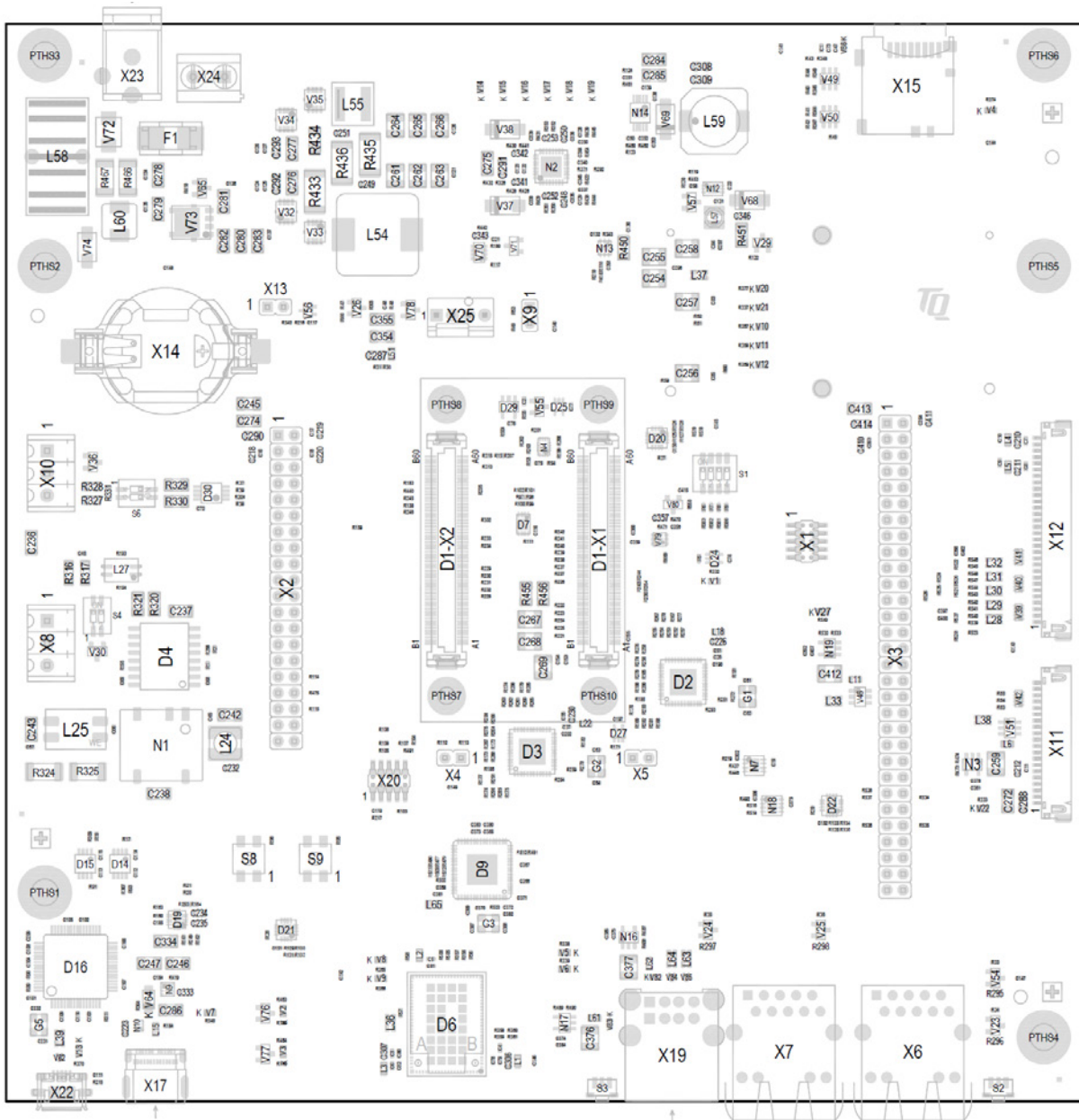


Figure 22: MBa91xxCA top view and label position

The labels on the MBa91xxCA show the following information:

Table 42: Labels on MBa91xxCA

Label	Content
AK1	Serial number
AK2	MBa91xxCA version and revision, tests performed

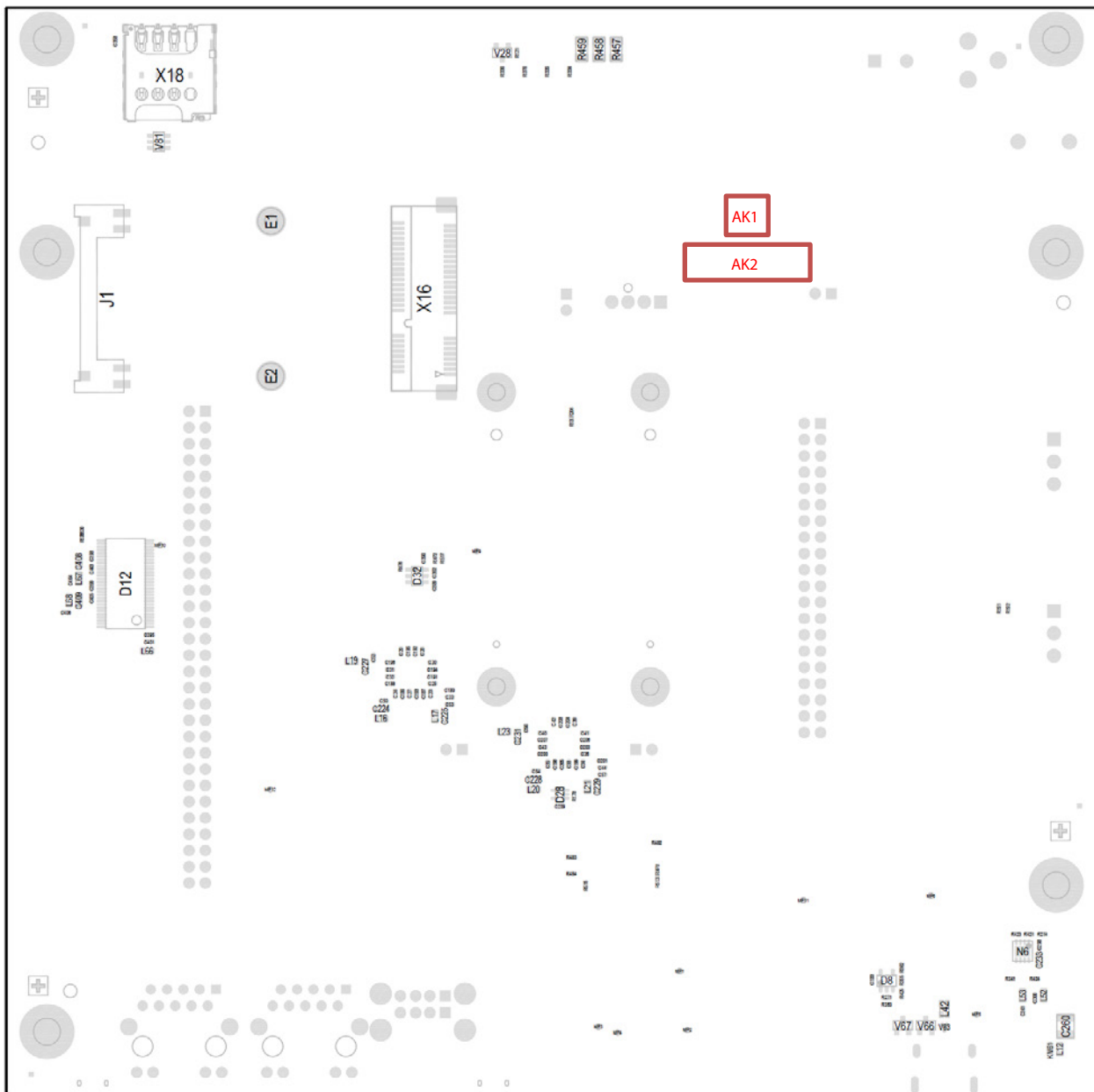


Figure 23: MBa91xxCA bottom view



6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Since the MBa91xxCA is a development platform, no EMC tests have been performed.

During the development of the MBa91xxCA the standard DIN EN 55022:2010 limit class A was taken into account.

6.2 ESD

ESD protection is provided on most interfaces of the MBa91xxCA.

The MBa91xxCA schematics show, which interfaces provide ESD protection.

6.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤ 30 V DC.

6.4 Cyber Security

A Threat Analysis and Risk Assessment (TARA) must always be performed by the customer for their individual end application, as the MBa91xxCA is only a sub-component of an overall system.

6.5 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship, irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ's invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.6 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfils the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general, reliable operation is given when the following conditions are met:

Table 43: Climatic and operational conditions MBa91xxCA

Parameter	Range	Remark
Ambient temperature	–20 °C to +70 °C	With Lithium battery
	–25 °C to +85 °C	Without Lithium battery
Storage temperature	–40 °C to +70 °C	With Lithium battery
	–40 °C to +100 °C	Without Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMa91xxCA heat dissipation



The i.MX 91 CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMa91xxCA must be taken into consideration when connecting the heat sink. The TQMa91xxCA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMa91xxCA and thus malfunction, deterioration or destruction.

7.1 Protection against external effects

Protection class IP00 was defined for the MBa91xxCA. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa91xxCA.

The MBa91xxCA is designed to be insensitive to vibration and impact.



8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa91xxCA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the MBa91xxCA was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBa91xxCA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBa91xxCA enable compliance with EuP requirements for the MBa91xxCA.

8.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers.

Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

8.6 Packaging

The MBa91xxCA is delivered in reusable packaging.

8.7 Batteries

8.7.1 General notes

For technical reasons a battery is necessary for the MBa91xxCA. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used. If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.

To allow a separate disposal, batteries are generally only mounted in sockets.

8.7.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.

There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa91xxCA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa91xxCA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).



These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
(Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof removal as at 1.9.96
(Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
(Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
(Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 44: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
AI	Analog Input
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CLC	Capacitor-Inductor-Capacitor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DIN	Deutsche Industrienorm (German industry standard)
DIP	Dual In-line Package
DSI	Display Serial Interface
eCSPI	enhanced Capability Serial Peripheral Interface
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European Standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FET	Field Effect Transistor
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communication
I ² C	Inter-Integrated Circuit
I ² S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IO	Input Output
IP00	Ingress Protection 00
I _{PD}	Input with Pull-Down
I _{PU}	Input with Pull-Up
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LGA	Land Grid Array
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean (operating) Time Between Failures

9.1 Acronyms and definitions (continued)

Table 44: Acronyms (continued)

Acronym	Meaning
NAND	Not-And (flash memory)
(NC)	Not Connected
NOR	Not-Or
NP	Not Placed
O _{OD}	Open-Drain Output
O _{PD}	Output with Pull-Down
O _{PU}	Output with Pull-Up
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PD	Pull-Down
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RTC	Real-Time Clock
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SGMII	Serial Gigabit Media-Independent Interface
SIM	Subscriber Identification Module
SMI	Serial Management Interface
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver/Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UIM	User Identity Module
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network



9.2 References

Table 45: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 91 Application Processors Data Sheet	Rev. 1 Draft F, Sep 2023	NXP
(2)	i.MX 91 Hardware Developer's Guide	TBD	NXP
(3)	i.MX 91 – Reference Manual	TBD	NXP
(4)	i.MX 91 – Mask Set Errata	TBD	NXP
(5)	Ethernet Transceiver DP83867– Data Sheet	December 2019	TI
(6)	TQMa91xxCA User's Manual	– current –	TQ-Systems
(7)	TQMa91xxLA User's Manual	– current –	TQ-Systems
(8)	TQMa91xxCA Support Wiki	– current –	TQ-Systems

