MBa57xx
User's Manual

MBa57xx UM 0101
08.02.2021

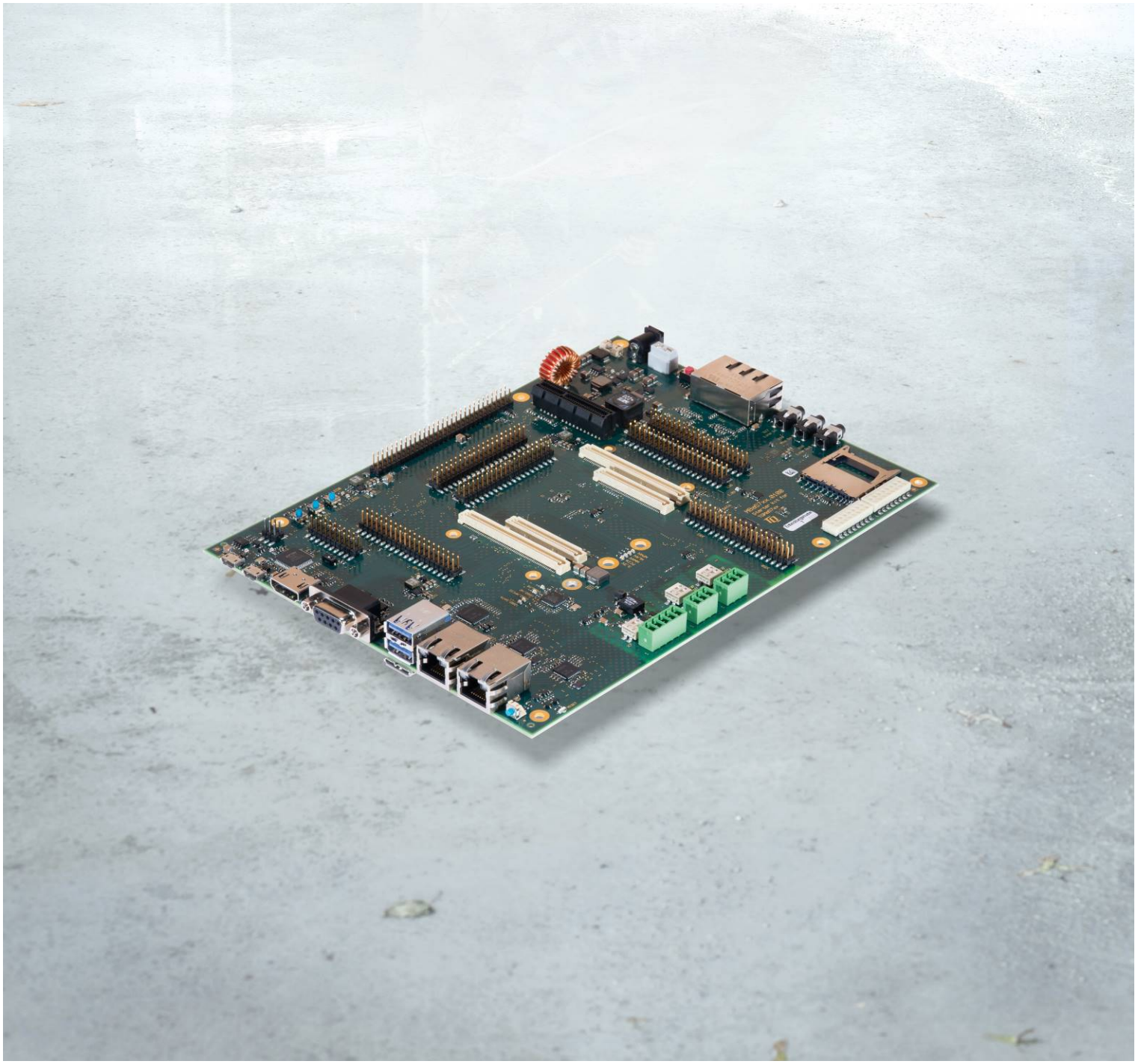

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Revision	Date	Name	Pos.	Modification
0100	15.04.2020	Petz		First edition
0101	08.02.2021	Petz	All 3.2.11	Non-functional changes, formatting, structure, expression Note regarding PCIe clock added

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBa57xx and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa57xx schematics
- TQMa57xx User's Manual
- AM57xx Reference Manuals
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa57xx

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBa57xx Revision 02xx. The MBa57xx is designed as a carrier board for the TQMa57xx. The illustrations in this User's Manual refer to the TQMa57xx. All interfaces provided by the TQMa57xx are available on the MBa57xx. The function of the AM57xx can be evaluated, and therefore the software development for a TQMa57xx project can start immediately. The MBa57xx supports all TQMa57xx modules with AM5718, AM5728, and AM5748 Single or Dual Cortex®-A15 CPUs. More details may be taken from the AM57xx documentation, see Table 60.

2.1 MBa57xx block diagram

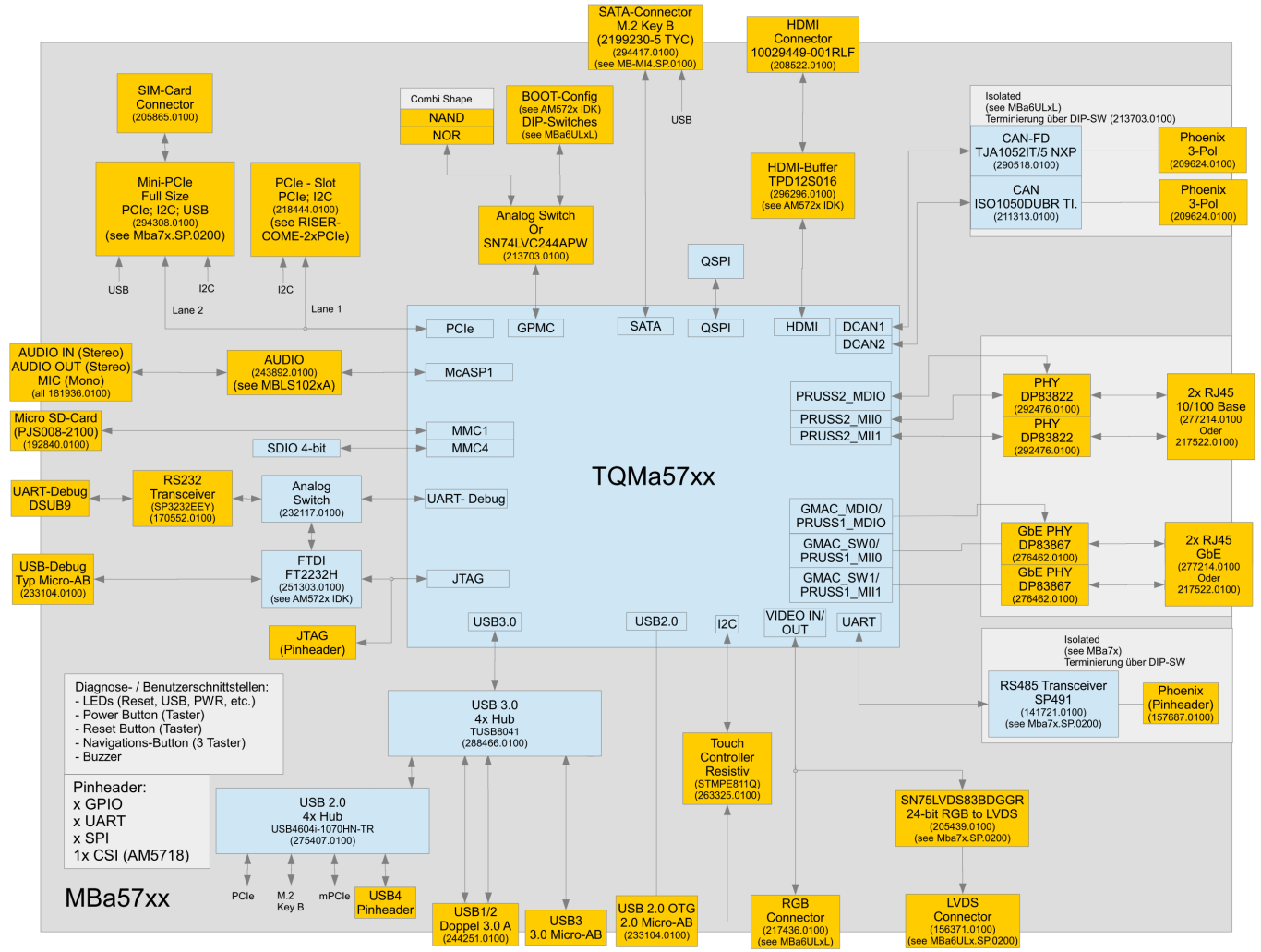

Figure 1: Block diagram MBa57xx with TQMa57xx

2.2 MBa57xx interfaces and functionality

Core of the system is the TQMa57xx with a TI AM57xx CPU. In addition to the standard communication interfaces like USB, Ethernet, RS-232, RS-485, etc. all other available signals of the TQMa57xx are routed to 100 mil standard headers.

The MBa57xx provides the following interfaces and functions:

Table 2: Overview MBa57xx interfaces

Interface	Connector	Type	Remark
USB 3.0 Super-Speed Host1&2	X31	USB, Type A	Stacked
USB 3.0 Super-Speed Host3	X32	USB, Micro B	–
USB 2.0 Hi-Speed Host1	X55	DF19, 20-pin	LCD, LVDS
USB 2.0 Hi-Speed Host2	X56	100 mil header	LCD, parallel, RGB
USB 2.0 Hi-Speed Host3	X26	M.2 Key-B	SATA
USB 2.0 Hi-Speed Host4	X29	Mini PCIe	–
USB 2.0 Hi-Speed OTG	X9	USB, Micro AB	–
USB Debug	X10	USB, Micro AB	–
Ethernet, Gbit	X52, X53	RJ45	2 × with integrated magnetics
Ethernet, 10/100 Base-T	X21	RJ45	Double, with integrated magnetics
CAN	X5, X6	Phoenix, 3-pin	Galvanically separated
RS-485	X7	Phoenix, 5-pin	Galvanically separated
RS-232	X8	D-Sub9	Debug UART
LVDS	X54	DF19, 30-pin	LVDS data
LCD	X56	100 mil header	LCD control signals, USB2.0, resistive touch controller signals
HDMI 1.4	X27	HDMI	–
Audio	X16	3.5 mm jacks	1 × Line-Out (stereo)
	X17		1 × Line-In (stereo)
	X18		1 × Mic (mono)
SD card	X14	Push-Pull	–
SATA	X26	M.2 Key-B	–
PCIe	X41	PCIe	–
	X29	Mini PCIe	–
	X25	SIM Card holder	–
Headers	X12/X13 X36/X37 X44/X45 X46/X47 X48/X49 X50/X51 X56	100 mil headers	Power-Out (12 V, 5 V, 3.3 V) LCD interface (parallel) Resistive Touch Controller 2× 10/100 Mbit Eth MII/MDIO I2C, SPI, QSPI, GPIO, SDIO, GPMC bus
Power In	X23	DC jack (2.5 mm / 5.5 mm)	V_{IN} = 24 V DC ±5 %
	X24	2-pin screw terminal block	
Coin cell	X20	CR2032 holder	Backup battery for RTC on TQMa57xx

2.2 MBa57xx interfaces and functionality (continued)

Table 3: Overview MBa57xx diagnostic and user's interfaces

Interface	Component	Remark
Status-LEDs	8 × Green LED	3 × VBUS USB3.0 1 × VBUS USB OTG 1 × VBUS (LVDS) 1 × VBUS (RGB) 1 × VBUS (SATA) 1 × VBUS (Mini PCIe)
	3 × Green LED	Mini PCIe WWAN, WLAN, WPAN
	2 × Green LED	GPIO LEDs at Port Expander II
	1 × Green LED	SATA status
	8 × Green LED	Power LEDs (24V, 12V, 5V, 3.3V, 3.3V-mPCIe, 1.8V, 1.5V, 1.1V)
	1 × Green LED	Debug LEDs for USB debug interface
	1 × Green / red LED	Reset LED
	8 × Green / yellow LED	Ethernet-LEDs (Activity / Speed)
Power / Reset buttons	2 × Push button	CPU / PMIC reset, CPU-ONOFF
GP push buttons	3 × Push button	GP buttons at I^2C Port Expander I
Boot Mode configuration	2 × DIP switch	2 × 8-fold Boot Device configuration
CAN and RS-485 termination	3 × DIP switch	3 × 2-fold
Debug USB / RS-232	1 × DIP switch	1 × single
Signal generator	1 × Buzzer	Connected to I^2C Port Expander II
JTAG	1 × 20-pin header	100 mil

3. ELECTRONICS

3.1 MBa57xx functional groups

3.1.1 TQMa57xx

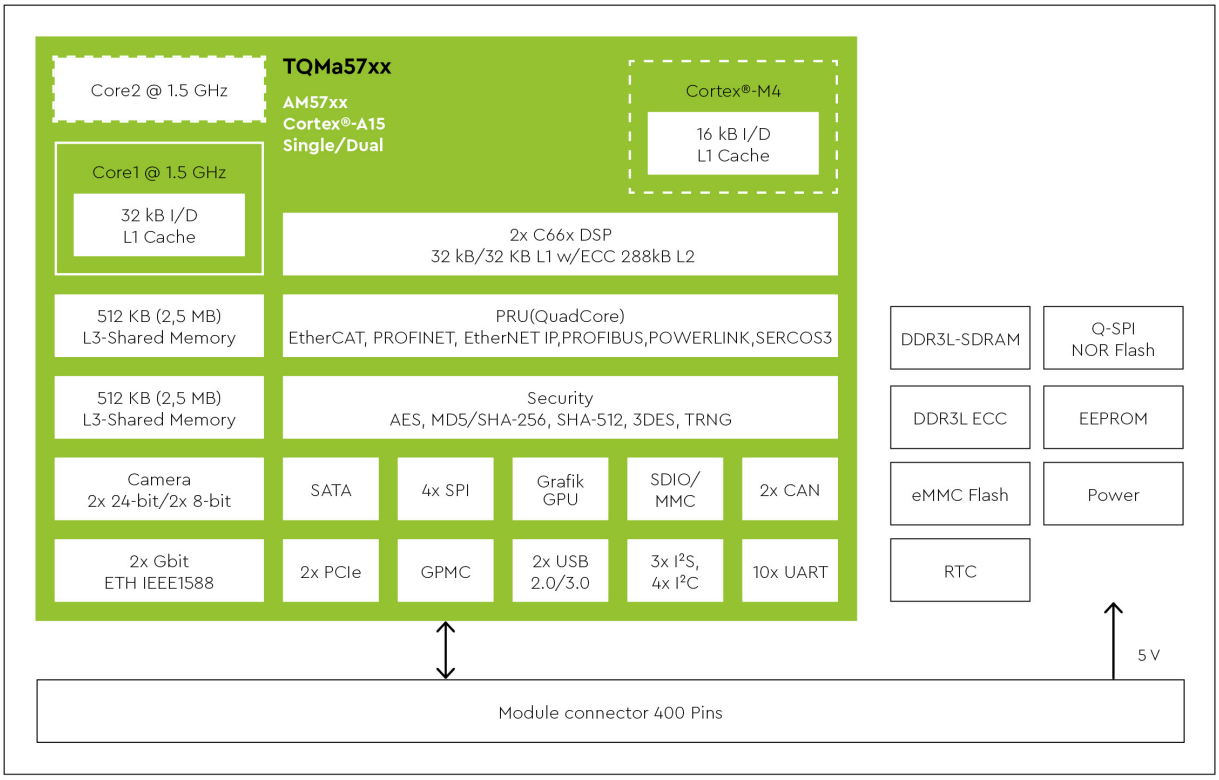

Figure 2: Block diagram TQMa57xx

Depending on the variant, the TQMa57xx features a Single or Dual Core Cortex®-A15 CPU with two Cortex®-M4 Image Processing Units (IPU) and one or two C66x Digital Signal Processor (DSP) subsystems. It can be used for all three variants AM5718, AM5728 and AM5748. The maximum clock rate of the CPUs is 1.5 GHz, the DSPs can be clocked with up to 750 MHz. The AM574x supports ECC and Secure Boot. More detailed information can be found in the TQMa57xx User's Manual (12).

3.1.1.1 TQMa57xx connectors

The available signals are routed to four connectors on the MBa57xx.

Note: TQMa57xx interfaces	
	Depending on the selected TQMa57xx, not all interfaces are available. Available interfaces are to be taken from the TQMa57xx User's Manual or the pinout tables in chapter 3.1.1.2.

The pin assignments listed in Table 4 to Table 7 refer to the BSP provided by TQ-Systems GmbH.

3.1.1.2 TQMa57xx pinout

Table 4: Pinout connector X1, (TQMa57xx: X1)

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
–	P	0 V	GND	DGND	1	2	DGND	GND	0 V	P	–
C9	O	1.8 V	LCD	VOUT1_D[20]	3	4	UART10_RTS#	UART	3.3 V	O	F4
A7	O	1.8 V	LCD	VOUT1_D[18]	5	6	UART10_RXD	UART	3.3 V	I	D1
B7	O	1.8 V	LCD	VOUT1_D[16]	7	8	UART10_TXD	UART	3.3 V	O	E2
C8	O	1.8 V	LCD	VOUT1_D[14]	9	10	DGND	GND	0 V	P	–
A5	O	1.8 V	LCD	VOUT1_D[12]	11	12	VOUT1_D[23]	LCD	1.8 V	O	A10
D7	O	1.8 V	LCD	VOUT1_D[10]	13	14	VOUT1_D[22]	LCD	1.8 V	O	B9
E8	O	1.8 V	LCD	VOUT1_D[8]	15	16	VOUT1_D[21]	LCD	1.8 V	O	A9
–	P	0 V	GND	DGND	17	18	VOUT1_D[19]	LCD	1.8 V	O	A8
F8	O	1.8 V	LCD	VOUT1_D[6]	19	20	VOUT1_D[17]	LCD	1.8 V	O	B8
G11	O	1.8 V	LCD	VOUT1_D[3]	21	22	VOUT1_D[15]	LCD	1.8 V	O	C7
F10	O	1.8 V	LCD	VOUT1_D[2]	23	24	VOUT1_D[13]	LCD	1.8 V	O	C6
G10	O	1.8 V	LCD	VOUT1_D[1]	25	26	DGND	GND	0 V	P	–
F11	O	1.8 V	LCD	VOUT1_D[0]	27	28	VOUT1_D[11]	LCD	1.8 V	O	D8
B11	I/O	1.8 V	GPIO	VOUT1_FLD (GPIO4_21)	29	30	VOUT1_D[9]	LCD	1.8 V	O	D9
B10	O	1.8 V	LCD	VOUT1_DE	31	32	VOUT1_D[7]	LCD	1.8 V	O	E7
–	P	0 V	GND	DGND	33	34	VOUT1_D[5]	LCD	1.8 V	O	F9
D11	O	1.8 V	LCD	VOUT1_CLK	35	36	VOUT1_D[4]	LCD	1.8 V	O	E9
–	I	3.3 V	Config	RST_FROM_MB#	37	38	VOUT1_VSYNC	LCD	1.8 V	O	E11
–	O	3.3 V	Config	RST_TO_MB#	39	40	VOUT1_HSYNC	LCD	1.8 V	O	C11
D20	I	3.3 V	JTAG	JTAG_TRSTN	41	42	DGND	GND	0 V	P	–
F18	I	3.3 V	JTAG	JTAG_TMS	43	44	GPIO4_0_G6	GPIO	3.3 V	I/O	G6
F19	O	3.3 V	JTAG	JTAG_TDO	45	46	GPIO4_1_F2 (PMIC_INT)	Config	3.3 V	I	F2
D23	I	3.3 V	JTAG	JTAG_TDI	47	48	GPIO4_2_F3 (TEMP_INT#)	Config	3.3 V	I	F3
–	P	0 V	GND	DGND	49	50	GPIO4_5_D2	GPIO	3.3 V	I/O	D2
E20	I	3.3 V	JTAG	JTAG_TCLK	51	52	GPIO5_1_J14	GPIO	3.3 V	I/O	J14
E18	O	3.3 V	JTAG	JTAG_RTCK	53	54	USB2.0_OTG_OC#	USB	3.3 V	I	G13
D24	I/O	3.3 V	JTAG	JTAG_EMU1	55	56	GPIO5_5_J11	GPIO	3.3 V	I/O	J11
G21	I/O	3.3 V	JTAG	JTAG_EMU0	57	58	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	59	60	MCASP8_ACLKX	AUDIO	3.3 V	I/O	B17
E12	I/O	3.3 V	GPIO	GPIO5_6_E12	61	62	MCASP8_FSX	AUDIO	3.3 V	I/O	A17
F13	I/O	3.3 V	GPIO	GPIO5_7_F13	63	64	MCASP8_AXR[0]	AUDIO	3.3 V	I/O	D15
C12	I/O	3.3 V	GPIO	GPIO5_8_C12	65	66	MCASP8_AXR[1]	AUDIO	3.3 V	I/O	B16
D12	I/O	3.3 V	GPIO	GPIO5_9_D12	67	68	MCASP8_AXR[2]	AUDIO	3.3 V	I/O	E15
–	P	0 V	GND	DGND	69	70	MCASP8_AXR[3]	AUDIO	3.3 V	I/O	A20
C18	I/O	3.3 V	AUDIO	MCASP4_C18	71	72	MCASP8_AHCLKX	AUDIO	3.3 V	O	C23
A15	I/O	3.3 V	AUDIO	MCASP2_A15	73	74	DGND	GND	0 V	P	–
F22	I	3.3 V	Config	AM57XX_PORZ#	75	76	DCAN1_RX	CAN	3.3 V	I	G19
F23	O	3.3 V	Config	RSTOUT#	77	78	DCAN1_TX	CAN	3.3 V	O	G20
E23	I	3.3 V	Config	RESET#	79	80	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	81	82	DCAN2_RX	CAN	3.3 V	I	F20
A22	O	3.3 V	SATA	SATA1_LED	83	84	DCAN2_TX	CAN	3.3 V	O	E21
B15	I/O	3.3 V	AUDIO	MCASP2_B15	85	86	DGND	GND	0 V	P	–
–	O	5 V	Config	PMIC_REGEN1	87	88	I2C4_SDA	I2C	3.3 V	I/O	B14
B20	I/O	3.3 V	HDMI	HDMI1_CEC	89	90	I2C4_SCL	I2C	3.3 V	O	A21
B21	I	3.3 V	HDMI	HDMI1_HPD	91	92	DGND	GND	0 V	P	–
F17	I/O	3.3 V	HDMI	HDMI1_DDC_SDA	93	94	I2C5_SDA	I2C	3.3 V	I/O	AA3
C25	O	3.3 V	HDMI	HDMI1_DDC_SCL	95	96	I2C5_SCL	I2C	3.3 V	O	AB9
–	P	0 V	GND	DGND	97	98	DGND	GND	0 V	P	–
G17	I/O	3.3 V	GPIO	GPIO7_16_G17	99	100	UART3_RXD	UART	3.3 V	I	A26
B24	I/O	3.3 V	GPIO	GPIO7_17_B24	101	102	UART3_TXD	UART	3.3 V	O	B22
D28	I/O	3.3 V	SDIO	MMC4_DAT[0]	103	104	DGND	GND	0 V	P	–
D26	I/O	3.3 V	SDIO	MMC4_DAT[1]	105	106	UART4_RXD	UART	3.3 V	I	G16
D27	I/O	3.3 V	SDIO	MMC4_DAT[2]	107	108	UART4_TXD	UART	3.3 V	O	D17
C28	I/O	3.3 V	SDIO	MMC4_DAT[3]	109	110	DGND	GND	0 V	P	–
C26	I	3.3 V	SDIO	MMC4_SDWP	111	112	UART8_RTS#	UART	3.3 V	O	AH6
–	P	0 V	GND	DGND	113	114	UART8_RXD	UART	3.3 V	I	AE8
E25	O	3.3 V	SDIO	MMC4_CLK	115	116	UART8_TXD	UART	3.3 V	O	AD8
C27	I/O	3.3 V	SDIO	MMC4_CMD	117	118	GPIO3_28_E1	GPIO	3.3 V	I/O	E1
B27	I	3.3 V	SDIO	MMC4_SDCD	119	120	DGND	GND	0 V	P	–

3.1.1.2 TQMa57xx pinout (continued)

Table 5: Pinout connector X2, (TQMa57xx: X2)

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
–	P	5 V	Power	VDD5V	1	2	VDD5V	Power	5 V	P	–
–	P	5 V	Power	VDD5V	3	4	VDD5V	Power	5 V	P	–
–	P	5 V	Power	VDD5V	5	6	VDD5V	Power	5 V	P	–
–	P	5 V	Power	VDD5V	7	8	VDD5V	Power	5 V	P	–
–	P	0 V	GND	DGND	9	10	VDD5V	Power	5 V	P	–
–	P	0 V	GND	DGND	11	12	DGND	GND	0 V	P	–
–	P	3.3 V	BAT	V_BAT	13	14	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	15	16	DGND	GND	0 V	P	–
F6	I/O	3.3 V	ENET	PR1_MDIO_DATA / GMAC_MDIO_DATA	17	18	WAKEUP0	Config	3.3 V	I	AD17
D3	O	3.3 V	ENET	PR1_MDIO_MDCLK / GMAC_MDIO_MCLK	19	20	GPIO3_29_G2	GPIO	3.3 V	I/O	G2
–	P	0 V	GND	DGND	21	22	PR1_MII1_TXEN	ENET	3.3 V	O	E4
A4	I	3.3 V	ENET	PR1_MII1_CRS / RGMII1_RXD0	23	24	PR1_MII1_MT_CLK	ENET	3.3 V	I	C1
B5	I	3.3 V	ENET	PR1_MII1_COL / RGMII1_RXD1	25	26	DGND	GND	0 V	P	–
B4	I	3.3 V	ENET	PR1_MII1_RXLINK / RGMII1_RXD2	27	28	PR1_MII1_TXD1 / RGMII1_TXC	ENET	3.3 V	O	D5
B3	I	3.3 V	ENET	PR1_MII1_RXER / RGMII1_RXD3	29	30	PR1_MII1_TXD0 / RGMII1_TXCTL	ENET	3.3 V	O	C2
–	P	0 V	GND	DGND	31	32	PR1_MII1_TXD2	ENET	3.3 V	O	E6
D6	I/O	3.3 V	ENET	PR1_MII1_RXD2 / RGMII1_TXD0	33	34	PR1_MII1_TXD3	ENET	3.3 V	O	F5
B2	I/O	3.3 V	ENET	PR1_MII1_RXD3 / RGMII1_TXD1	35	36	PR1_MII1_RXD0 / RGMII1_RXCTL	ENET	3.3 V	I	A3
C4	I/O	3.3 V	ENET	PR1_MII1_RXDV / RGMII1_TXD2	37	38	PR1_MII1_RXD1 / RGMII1_RXC	ENET	3.3 V	I	C5
C3	I/O	3.3 V	ENET	PR1_MII1_MR_CLK / RGMII1_TXD3	39	40	DGND	GND	0 V	P	–
–	I	5 V	USB	VUSB_VBUS2	41	42	GPIO3_30_H7	GPIO	3.3 V	I/O	H7
–	I	5 V	Config	PMIC_PWRON#	43	44	PR2_MDIO_DATA	ENET	3.3 V	I/O	D14
K14	I	1.8 V	Config	E–FUSE_1V8	45	46	PR2_MDIO_MDCLK	ENET	3.3 V	O	C14
–	P	0 V	GND	DGND	47	48	DGND	GND	0 V	P	–
A13	I	3.3 V	ENET	PR2_MII0_MR_CLK	49	50	PR2_MII0_MT_CLK	ENET	3.3 V	I	F12
G12	I	3.3 V	ENET	PR2_MII0_RXER	51	52	PR2_MII0_TXEN	ENET	3.3 V	O	B12
C15	I	3.3 V	ENET	PR2_MII0_RXD[0]	53	54	PR2_MII0_TXD[0]	ENET	3.3 V	O	E14
A18	I	3.3 V	ENET	PR2_MII0_RXD[1]	55	56	DGND	GND	0 V	P	–
A19	I	3.3 V	ENET	PR2_MII0_RXD[2]	57	58	PR2_MII0_TXD[1]	ENET	3.3 V	O	A12
F14	I	3.3 V	ENET	PR2_MII0_RXD[3]	59	60	PR2_MII0_TXD[2]	ENET	3.3 V	O	B13
–	P	0 V	GND	DGND	61	62	PR2_MII0_TXD[3]	ENET	3.3 V	O	A11
G14	I	3.3 V	ENET	PR2_MII0_RXDV	63	64	PR2_MII0_COL	ENET	3.3 V	I	F15
A16	I	3.3 V	ENET	PR2_MII0_RXLINK	65	66	PR2_MII0_CRS	ENET	3.3 V	I	B18
F21	I/O	3.3 V	GPIO	GPIO6_16_F21	67	68	DGND	GND	0 V	P	–
B26	I/O	3.3 V	GPIO	GPIO6_19_B26	69	70	PR2_MII1_RXLINK	ENET	3.3 V	I	C17
B25	I/O	3.3 V	SPI	SPI1_D0	71	72	PR2_MII1_CRS	ENET	3.3 V	I	E17
F16	I/O	3.3 V	SPI	SPI1_D1	73	74	PR2_MII1_COL	ENET	3.3 V	I	D18
–	P	0 V	GND	DGND	75	76	GPIO3_1_AF9	GPIO	3.3 V	I/O	AF9
A25	O	3.3 V	SPI	SPI1_SCLK	77	78	NMIN_DSP	Config	3.3 V	I	D21
A24	O	3.3 V	SPI	SPI1_CS0	79	80	DGND	GND	0 V	P	–

3.1.1.2 TQMa57xx pinout (continued)

Table 6: Pinout connector X3, (TQMa57xx: X3)

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
N6	O	1.8 V	GPMC	GPMC_BE#[0] (GPIO2_26)	1	2	DGND	GND	0 V	P	–
M4	O	1.8 V	GPMC	GPMC_BE#[1] (GPIO2_27)	3	4	GPMC_CLK (GPIO2_22)	GPMC	1.8 V	O	P7
M6	I/O	1.8 V	Boot/GPMC	GPMC_AD[0] (GPIO1_6)	5	6	GPMC_CS0 (GPIO2_19)	GPMC	1.8 V	O	T1
M2	I/O	1.8 V	Boot/GPMC	GPMC_AD[1] (GPIO1_7)	7	8	GPMC_OE#_RE# (GPIO2_24)	GPMC	1.8 V	O	M5
–	P	0 V	GND	DGND	9	10	GPMC_WE# (GPIO2_25)	GPMC	1.8 V	O	M3
L5	I/O	1.8 V	Boot/GPMC	GPMC_AD[2] (GPIO1_8)	11	12	GPMC_ADV#_ALE (GPIO2_23)	GPMC	1.8 V	O	N1
M1	I/O	1.8 V	Boot/GPMC	GPMC_AD[3] (GPIO1_9)	13	14	GPMC_A[1] (GPIO7_4)	GPMC	1.8 V	O	T9
L6	I/O	1.8 V	Boot/GPMC	GPMC_AD[4] (GPIO1_10)	15	16	GPMC_A[2] (GPIO7_5)	GPMC	1.8 V	O	T6
L4	I/O	1.8 V	Boot/GPMC	GPMC_AD[5] (GPIO1_11)	17	18	DGND	GND	0 V	P	–
L3	I/O	1.8 V	Boot/GPMC	GPMC_AD[6] (GPIO1_12)	19	20	GPMC_A[3] (GPIO7_6)	GPMC	1.8 V	O	T7
L2	I/O	1.8 V	Boot/GPMC	GPMC_AD[7] (GPIO1_13)	21	22	GPMC_A[4] (GPIO1_26)	GPMC	1.8 V	O	P6
L1	I/O	1.8 V	Boot/GPMC	GPMC_AD[8] (GPIO7_18)	23	24	GPMC_A[5] (GPIO1_27)	GPMC	1.8 V	O	R9
–	P	0 V	GND	DGND	25	26	GPMC_A[6] (GPIO1_28)	GPMC	1.8 V	O	R5
K2	I/O	1.8 V	Boot/GPMC	GPMC_AD[9] (GPIO7_19)	27	28	GPMC_A[7] (GPIO1_29)	GPMC	1.8 V	O	P5
J1	I/O	1.8 V	Boot/GPMC	GPMC_AD[10] (GPIO7_28)	29	30	GPMC_A[8] (GPIO1_30)	GPMC	1.8 V	O	N7
J2	I/O	1.8 V	Boot/GPMC	GPMC_AD[11] (GPIO7_29)	31	32	GPMC_A[9] (GPIO1_31)	GPMC	1.8 V	O	R4
H1	I/O	1.8 V	Boot/GPMC	GPMC_AD[12] (GPIO1_18)	33	34	DGND	GND	0 V	P	–
J3	I/O	1.8 V	Boot/GPMC	GPMC_AD[13] (GPIO1_19)	35	36	GPMC_A[10] (GPIO2_0)	GPMC	1.8 V	O	N9
H2	I/O	1.8 V	Boot/GPMC	GPMC_AD[14] (GPIO1_20)	37	38	GPMC_A27_AF4 (GPIO3_19)	GPMC	3.3 V	O	AF4
H3	I/O	1.8 V	Boot/GPMC	GPMC_AD[15] (GPIO1_21)	39	40	GPMC_A27_G1 (GPIO3_31)	GPMC	3.3 V	O	G1
AD9	I/O	3.3 V	GPIO	GPIO3_0_AD9	41	42	DGND	GND	0 V	P	–
B19	I	3.3 V	ENET	PR2_MII1_RXER	43	44	PR1_MII0_MT_CLK / RGMII0_RXC	ENET	3.3 V	I	U5
–	P	0 V	GND	DGND	45	46	PR1_MII0_COL (GPIO5_15)	ENET	3.3 V	I	V1
Y1	I	3.3 V	ENET	PR1_MII0_MR_CLK (GPIO5_19)	47	48	PR1_MII0_TXD3 / RGMII0_RXCTL	ENET	3.3 V	I/O	V5
V2	I	3.3 V	ENET	PR1_MII0_RXDV (GPIO5_18)	49	50	DGND	GND	0 V	P	–
U7	I/O	3.3 V	ENET	PR1_MII0_RXER / RGMII0_TXD2	51	52	PR1_MII0_TXD0 / RGMII0_RXD0	ENET	3.3 V	I/O	W2
V7	I/O	3.3 V	ENET	PR1_MII0_CRS / RGMII0_TXD3	53	54	PR1_MII0_TXD1 / RGMII0_RXD1	ENET	3.3 V	I/O	Y2
U6	I/O	3.3 V	ENET	PR1_MII0_RXD0 / RGMII0_TXD0	55	56	PR1_MII0_TXD2 / RGMII0_RXD3	ENET	3.3 V	I/O	V4
V6	I/O	3.3 V	ENET	PR1_MII0_RXD1 / RGMII0_TXD1	57	58	PR1_MII0_TXEN / RGMII0_RXD2	ENET	3.3 V	I/O	V3
–	P	0 V	GND	DGND	59	60	DGND	GND	0 V	P	–
W9	I/O	3.3 V	ENET	PR1_MII0_RXD3 / RGMII0_TXC	61	62	PR2_MII1_RXD[0]	ENET	3.3 V	I	AB5
V9	I/O	3.3 V	ENET	PR1_MII0_RXD2 / RGMII0_TXCTL	63	64	PR2_MII1_RXD[1]	ENET	3.3 V	I	AB8
U4	I	3.3 V	ENET	PR1_MII0_RXLINK (GPIO5_16)	65	66	PR2_MII1_RXD[2]	ENET	3.3 V	I	AD6
–	P	0 V	GND	DGND	67	68	PR2_MII1_RXD[3]	ENET	3.3 V	I	AC8
U3	I/O	3.3 V	ENET	RMII_MHZ_50_CLK	69	70	PR2_MII1_TXEN	ENET	3.3 V	O	AB4
–	P	0 V	GND	DGND	71	72	PR2_MII1_TXD[0]	ENET	3.3 V	O	AC6
AC9	I	3.3 V	ENET	PR2_MII1_MR_CLK	73	74	PR2_MII1_TXD[1]	ENET	3.3 V	O	AC7
AC3	I	3.3 V	ENET	PR2_MII1_RXDV	75	76	PR2_MII1_TXD[2]	ENET	3.3 V	O	AC4
AC5	I	3.3 V	ENET	PR2_MII1_MT_CLK	77	78	PR2_MII1_TXD[3]	ENET	3.3 V	O	AD4
–	P	0 V	GND	DGND	79	80	DGND	GND	0 V	P	–

3.1.1.2 TQMa57xx pinout (continued)

Table 7: Pinout connector X4, (TQMa57xx: X4)

Ball	Type	Level	Group	Signal	Pin		Signal	Group	Level	Type	Ball
–	P	0 V	GND	DGND	1	2	USB3.0_DRVVBUS	USB	3.3 V	O	AB10
AC12	I/O	3.3 V	USB	USB3.0_DM	3	4	DGND	GND	0 V	P	–
AD12	I/O	3.3 V	USB	USB3.0_DP	5	6	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	7	8	DGND	GND	0 V	P	–
AC11	O	1.8 V	USB	USB3.0_TXN0	9	10	USB3.0_RXP0	USB	1.8 V	I	AE12
AD11	O	1.8 V	USB	USB3.0_TXP0	11	12	USB3.0_RXN0	USB	1.8 V	I	AF12
–	P	0 V	GND	DGND	13	14	DGND	GND	0 V	P	–
AE11	I/O	3.3 V	USB	USB2.0_DP	15	16	USB2.0_DM	USB	3.3 V	I/O	AF11
AC16	I	3.3 V	USB	USB2.0_OTG_ID	17	18	USB2.0_DRVVBUS	USB	3.3 V	O	AC10
–	P	0 V	GND	DGND	19	20	DGND	GND	0 V	P	–
AH9	I	1.8 V	SATA	SATA1_RXN0	21	22	SATA1_TXN0	SATA	1.8 V	O	AG10
AG9	I	1.8 V	SATA	SATA1_RXP0	23	24	SATA1_TXP0	SATA	1.8 V	O	AH10
–	P	0 V	GND	DGND	25	26	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	27	28	PCIE_RXN1	PCIE	1.8 V	I	AG11
–	P	0 V	GND	DGND	29	30	PCIE_RXP1	PCIE	1.8 V	I	AH11
AG13	I	1.8 V	PCIE	PCIE_RXN0	31	32	DGND	GND	0 V	P	–
AH13	I	1.8 V	PCIE	PCIE_RXP0	33	34	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	35	36	PCIE_TXN1	PCIE	1.8 V	O	AG12
–	P	0 V	GND	DGND	37	38	PCIE_TXP1	PCIE	1.8 V	O	AH12
AG15	I	1.8 V	PCIE	PCIE_CLKP	39	40	DGND	GND	0 V	P	–
AH15	I	1.8 V	PCIE	PCIE_CLKN	41	42	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	43	44	PCIE_TXN0	PCIE	1.8 V	O	AG14
–	P	0 V	GND	DGND	45	46	PCIE_TXP0	PCIE	1.8 V	O	AH14
AG16	O	1.8 V	HDMI	HDMI1_CLOCKX	47	48	DGND	GND	0 V	P	–
AH16	O	1.8 V	HDMI	HDMI1_CLOCKY	49	50	DGND	GND	0 V	P	–
–	P	0 V	GND	DGND	51	52	DGND	GND	0 V	P	–
AG18	O	1.8 V	HDMI	HDMI1_DATA1X	53	54	HDMI1_DATA0X	HDMI	1.8 V	O	AG17
AH18	O	1.8 V	HDMI	HDMI1_DATA1Y	55	56	HDMI1_DATA0Y	HDMI	1.8 V	O	AH17
–	P	0 V	GND	DGND	57	58	DGND	GND	0 V	P	–
AH19	O	1.8 V	HDMI	HDMI1_DATA2Y	59	60	HDMI1_DATA2X	HDMI	1.8 V	O	AG19
–	P	0 V	GND	DGND	61	62	DGND	GND	0 V	P	–
R6	I/O	1.8 V	GPIO	GPIO7_3_R6	63	64	QSPI_SCK	QSPI	1.8 V	O	R2
Y9	I	3.3 V	SD	MMC1_SDWP	65	66	QSPI_RTCLK	QSPI	1.8 V	I	R3
–	P	0 V	GND	DGND	67	68	QSPI_SS1#	QSPI	1.8 V	O	P1
W6	O	3.3 V	SD	MMC1_CLK	69	70	DGND	GND	0 V	P	–
Y6	I/O	3.3 V	SD	MMC1_CMD	71	72	QSPI_DATA0	QSPI	1.8 V	I/O	U1
AA6	I/O	3.3 V	SD	MMC1_DAT[0]	73	74	QSPI_DATA1	QSPI	1.8 V	I/O	P3
Y4	I/O	3.3 V	SD	MMC1_DAT[1]	75	76	QSPI_DATA2	QSPI	1.8 V	I/O	U2
AA5	I/O	3.3 V	SD	MMC1_DAT[2]	77	78	QSPI_DATA3	QSPI	1.8 V	I/O	T2
Y3	I/O	3.3 V	SD	MMC1_DAT[3]	79	80	DGND	GND	0 V	P	–
W7	I	3.3 V	SD	MMC1_SDCD	81	82	QSPI_SS0#	QSPI	1.8 V	O	P2
–	P	0 V	GND	DGND	83	84	GPIO3_22_AE5	GPIO	3.3 V	I/O	AE5
AE9	I/O	3.3 V	GPIO	GPIO3_2_AE9	85	86	GPIO3_23_AE1	GPIO	3.3 V	I/O	AE1
AF8	I/O	3.3 V	GPIO	GPIO3_3_AF8	87	88	GPIO3_24_AE2	GPIO	3.3 V	I/O	AE2
–	P	0 V	GND	DGND	89	90	GPIO3_25_AE6	GPIO	3.3 V	I/O	AE6
AF6	I/O	3.3 V	GPIO	GPIO3_17_AF6	91	92	GPIO3_26_AD2	GPIO	3.3 V	I/O	AD2
AF3	I/O	3.3 V	GPIO	GPIO3_18_AF3	93	94	GPIO3_27_AD3	GPIO	3.3 V	I/O	AD3
AF1	I/O	3.3 V	GPIO	GPIO3_20_AF1	95	96	PR1_PRU0_GPO5_AG4	ENET	3.3 V	O	AG4
AE3	I/O	3.3 V	GPIO	GPIO3_21_AE3	97	98	DGND	GND	0 V	P	–
AG7	I/O	3.3 V	GPIO	GPIO3_6_AG7	99	100	PR1_PRU0_GPO6_AG2	ENET	3.3 V	O	AG2
AH3	I	3.3 V	ENET	PR1_PRU0_GPI1_AH3	101	102	PR1_PRU0_GPO7_AG3	ENET	3.3 V	O	AG3
AH5	I	3.3 V	ENET	PR1_PRU0_GPI2_AH5	103	104	PR1_PRU0_GPO8_AG5	ENET	3.3 V	O	AG5
–	P	0 V	GND	DGND	105	106	PR1_PRU0_GPO9_AF2	ENET	3.3 V	O	AF2
AG6	I	3.3 V	ENET	PR1_PRU0_GPI3_AG6	107	108	GPIO2_28_N2	GPIO	1.8 V	I/O	N2
AH4	I	3.3 V	ENET	PR1_PRU0_GPI4_AH4	109	110	GPIO2_30_AG8	GPIO	3.3 V	I/O	AG8
AC17	I/O	3.3 V	GPIO	GPIO1_1_AC17	111	112	GPIO2_31_AH7	GPIO	3.3 V	I/O	AH7
AB16	I/O	3.3 V	GPIO	GPIO1_2_AB16	113	114	DGND	GND	0 V	P	–
P9	I/O	1.8 V	GPIO	GPIO2_1_P9	115	116	MCASP5_AA4 (PR2_PRU1_GPO4)	AUDIO	3.3 V	I/O	AA4
P4	I/O	1.8 V	GPIO	GPIO2_2_P4	117	118	MCASP5_AB3 (PR2_PRU1_GPO3)	AUDIO	3.3 V	I/O	AB3
–	P	0 V	GND	DGND	119	120	DGND	GND	0 V	P	–

3.1.2 I2C address mapping

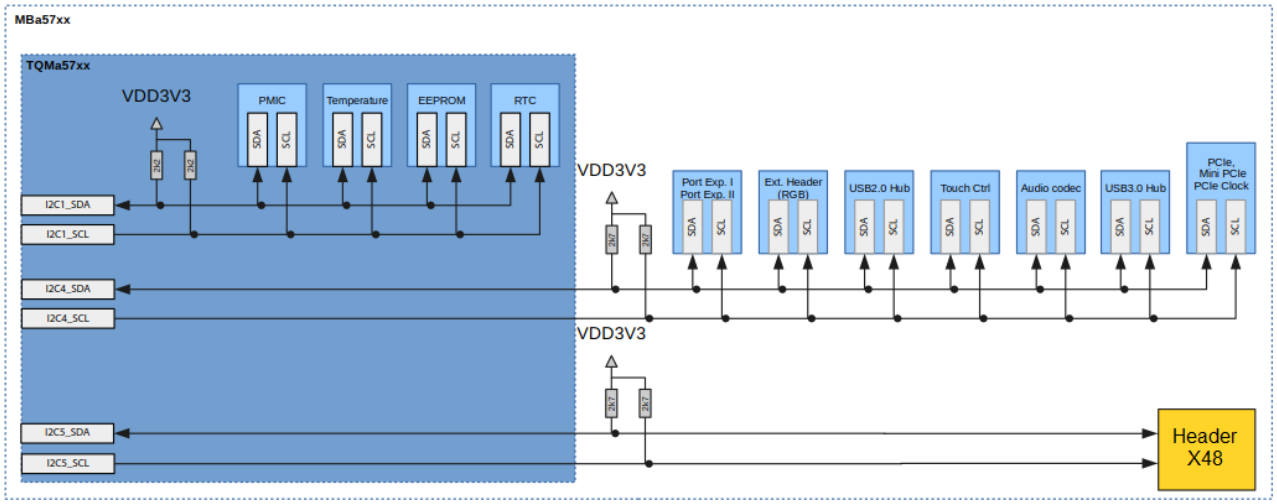

Figure 3: Block diagram I²C buses on TQMa57xx and MBa57xx

The TQMa57xx offers two I²C interfaces, which are available on the TQMa57xx connectors as primary function.
I2C1 is a TQMa57xx internal I²C bus, which is exclusively used for the I²C devices on the TQMa57xx. This bus is not available.
The corresponding addresses can be taken from the User's Manual of the TQMa57xx (12).
I2C5 is routed to header X48 on the MBa57xx, no I²C devices are connected.
Further I²C interfaces can be provided by an adapted pin multiplexing.
The following table shows the signals used on the two I²C interfaces:

Table 8: I²C signals

Signal	Direction	MBa57xx	Remark
I2C4_SDA	I/O	X1-88	2.7 kΩ PU to 3.3 V on MBa57xx
I2C4_SCL	O	X1-90	2.7 kΩ PU to 3.3 V on MBa57xx
I2C5_SDA	I/O	X1-94	2.7 kΩ PU to 3.3 V on MBa57xx
I2C5_SCL	O	X1-96	2.7 kΩ PU to 3.3 V on MBa57xx

The following table shows the I2C4 addresses used on the MBa57xx.

Table 9: I2C4 address assignment

Reference	Device	Usage	7-bit address
D22	PCA9555PW	GPIO expander	0x20 / 010 0000b
D23	PCA9555PW	GPIO expander	0x21 / 010 0001b
D18	USB4604	USB Hub	0x2D / 010 1101b
D9	STMPE811Q	Touch Controller	0x41 / 100 0001b
N9	TLV320AIC3204	Audio Codec	0x18 / 001 1000b
D35	9FGV0441AKILFT	PCIe Clock	0x34 / 011 0100b
D21	TUSB8041	USB3.0 Hub	0x44 / 100 0100b
X41	PCIe	Lane 0	–
X29	mPCIe	Lane 1	–
X56	Header	RGB	–

3.1.3 Temperature sensor

The MBa57xx does not provide a temperature sensor. However, on the top side of the TQMa57xx is a temperature sensor SE97BTP with integrated EEPROM.

3.1.4 RTC backup

The TQMa57xx provides a DS1339U-33 RTC, which is connected to the I2C1 bus.
To supply the RTC on the TQMa57xx, a 3V lithium battery type CR2032 with very low self-discharge is mounted on the MBa57xx.

The following tables show details of the RTC backup supply.

Table 10: RTC backup supply

Parameter	Value	Remark
Coin cell voltage	2.1 V to 3.7 V	3.0 V typical
Current consumption discrete RTC DS1339U-33	440 nA typical	0.7 µA maximal @ T_{amb} = +25 °C

3.1.5 Port Expander

Two PCA9555PW port expanders with 16 ports each are used to control several components on the MBa57xx.
These include the buzzer, user LEDs, user GPIOs, configuration signals for mPCIe and general purpose push buttons.

The port expanders are configured via I2C4. The expander addresses can be changed by rearranging resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices. The assembly options are documented in the MBa57xx schematics. In the initial state after power-on all ports are set as input.

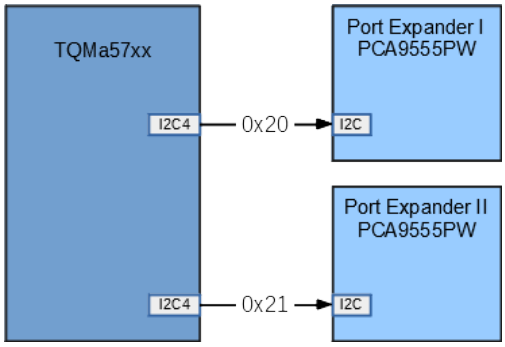

Figure 4: Block diagram port expander D22 and D23

The following tables show details of port expanders.

Table 11: Functions of port expanders

Port Expander	Port	Signal	Dir.	Remark
Port Expander I, D22 0x20 / 010 0000b	IO0_0	BOOT_CFG_EN#	O	Enable Boot Config on carrier board
	IO0_1	BUTTON_1#	I	General purpose push button
	IO0_2	BUTTON_2#	I	General purpose push button
	IO0_3	BUTTON_3#	I	General purpose push button
	IO0_4	LCD_EN	O	Enable LCD (X56)
	IO0_5	USB3.0_H3_OTG_ID	I	USB-ID for OTG
	IO0_6	PR2_MII0_RST	O	10/100 Base Ethernet reset
	IO0_7	PR2_MII1_RST	O	10/100 Base Ethernet reset
	IO1_0	RGMII0_INT#	I	Gbit Ethernet INT/PWDN
	IO1_1	RGMII1_INT#	I	Gbit Ethernet INT/PWDN
	IO1_2	PCIE_WAKE#	O	Wake signal for PCIe and mPCIe
	IO1_3	PCIE_DIS#	O	Disable signal for PCIe and mPCIe
	IO1_4	LCD_PWR_EN	O	LCD Power Enable
	IO1_5	LCD_BLT_EN	O	LCD Backlight Enable
	IO1_6	PWR_EN_3V3_DISPLAY	O	Enable 3.3 V display supply
	IO1_7	LVDS_EN	O	Enable LCD (X54)
Port Expander II, D23 0x21 / 010 0001b	IO0_0	BUZZER_PWM	O	Unused – GPIO6_19_B26 of TQMa57xx is used
	IO0_1	PWR_EN_1V5	O	–
	IO0_2	PWR_EN_1V1	O	–
	IO0_3	LED0	O	–
	IO0_4	LED1	O	–
	IO0_5	GPIO_EXP_IO5	O	Optional: audio reset
	IO0_6	GPIO_EXP_IO6	O	Optional: mPCIe reset
	IO0_7	GPIO_EXP_IO7	O	Optional: LCD reset
	IO1_0	PR2_MII0_INT#	I	10/100 Base Ethernet Interrupt
	IO1_1	PR2_MII1_INT#	I	10/100 Base Ethernet Interrupt
	IO1_2	RGMII0_RST#	O	Gbit Ethernet reset
	IO1_3	RGMII1_RST#	O	Gbit Ethernet reset
	IO1_4	USB2.0_HUB_RST#	O	–
	IO1_5	USB3.0_HUB_RST#	O	–
	IO1_6	PCIE_RST#	O	PCIe reset
	IO1_7	SATA_M2_RST#	O	SATA reset

3.1.6 Power Management and Reset

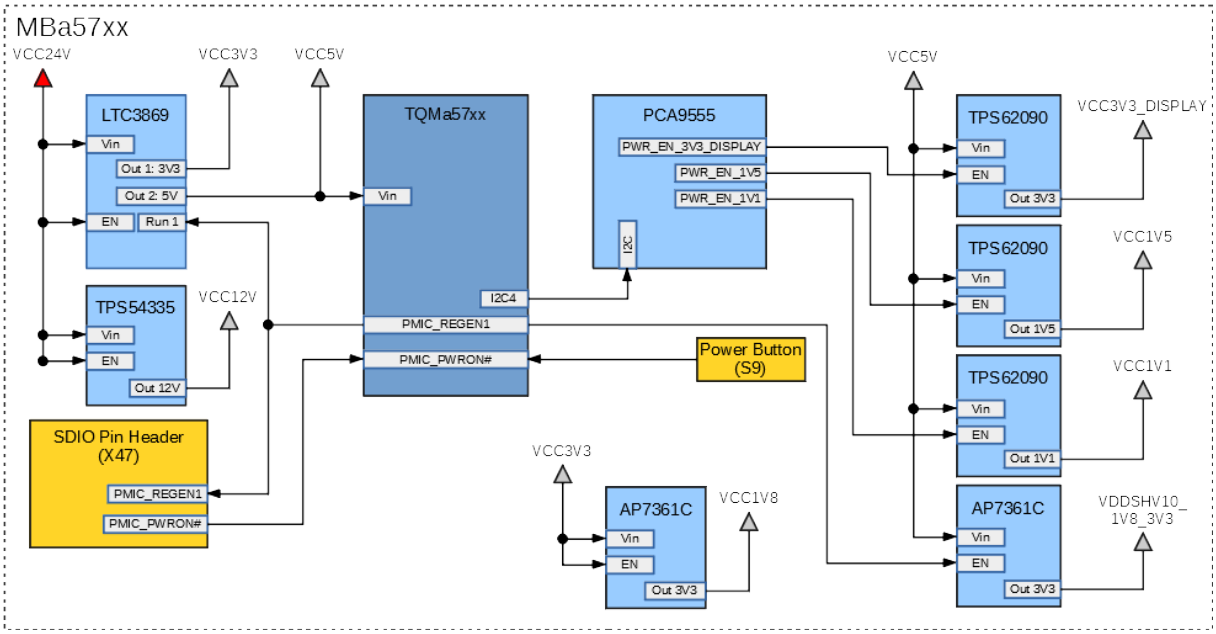

Figure 5: Block diagram Power

The following table shows the signals used for power management.

Table 12: Functions of power signals

Signal	Source	Dir.	Default	Remark
PMIC_REGEN1	TQMa57xx PMIC	O	Low	Is activated by the TQMa57xx during power sequencing and switches on the carrier board controller for 3.3 V.
PWR_EN_3V3_DISPLAY	Port-Expanders PCA9555PW	O	Low	Enable for display power supply (X54)
PWR_EN_1V5		O	Low	Enable for 1.5 V supply
PWR_EN_1V1		O	Low	Enable for 1.1 V supply
PMIC_PWRON#	Power Button / SDIO extension header	I	High	See TQMa57xx User's Manual. Can be used with push button S9 and SDIO extension header.

3.1.6 Power Management and Reset (continued)

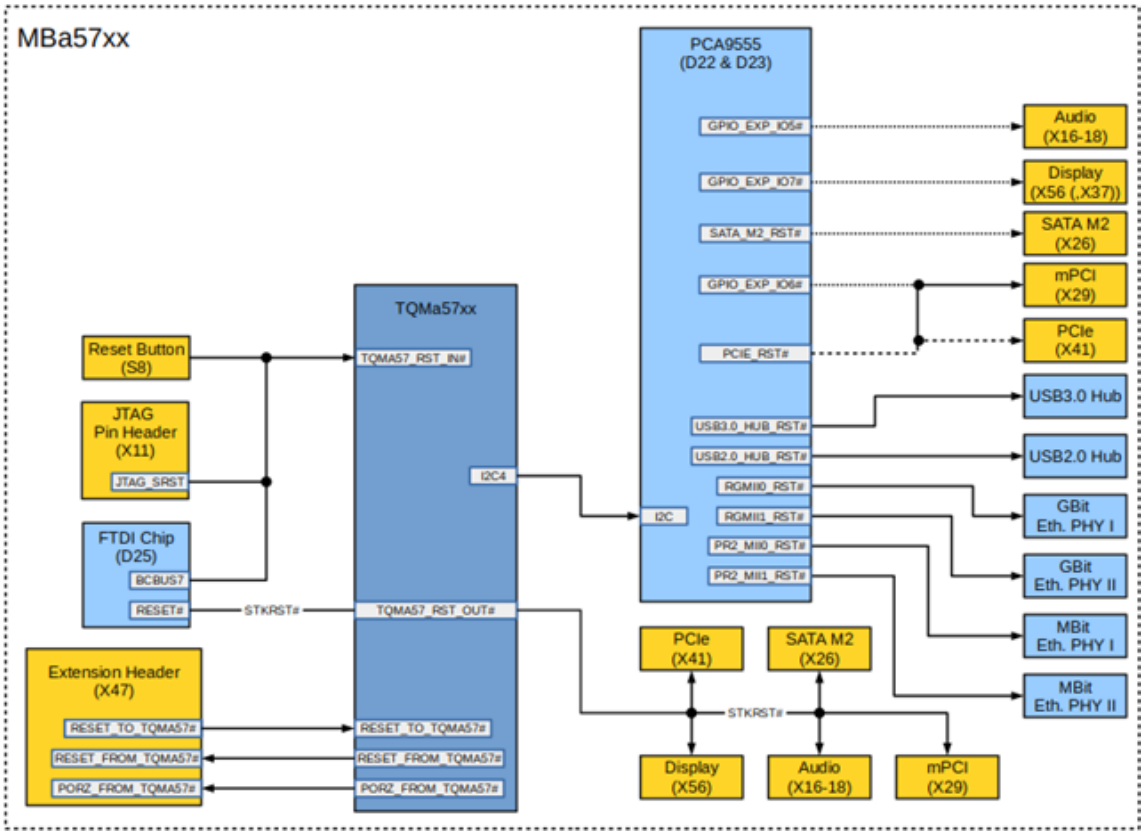

Figure 6: Block diagram Reset

The MBa57xx provides various options for a complete or partial reset of the assembly.
The following table shows the signals used.

Table 13: Functions of Reset signals

Signal	Source	Dir.	Default	Remark
RESET_TO_TQMA57#	Extension header	I	High	CPU reset
RESET_FROM_TQMA57#	TQMa57xx CPU	O	High	Reset signal from CPU (as indicator)
PORZ_FROM_TQMA57#	TQMa57xx reset	O	High	CPU hard reset signal (as indicator)
TQMA57_RST_IN#		I	High	See TQMa57xx User's Manual, push button S8 / FTDI / JTAG
TQMA57_RST_OUT#	TQMa57xx	O	High	See TQMa57xx User's Manual Active when AM57 reset is active (Open drain, PU required) Reset for periphery on carrier board (STKRST#)
USB3.0_HUB_RST#	Port Expander II, D23 PCA9555PW	O	High	Reset for USB3.0 Hub
USB2.0_HUB_RST#		O	High	Reset for USB2.0 Hub
RGMII0_RST#		O	High	Reset for Gbit Ethernet PHY I
RGMII1_RST#		O	High	Reset for Gbit Ethernet PHY II
PR2_MII0_RST#		O	High	Reset for Mbit Ethernet PHY I
PR2_MII1_RST#		O	High	Reset for Mbit Ethernet PHY II
PCIE_RST#		O	High	Reset for PCIe card at X41
SATA_M2_RST#		O	High	Reset for SATA interface at X26

3.1.7 Power supply

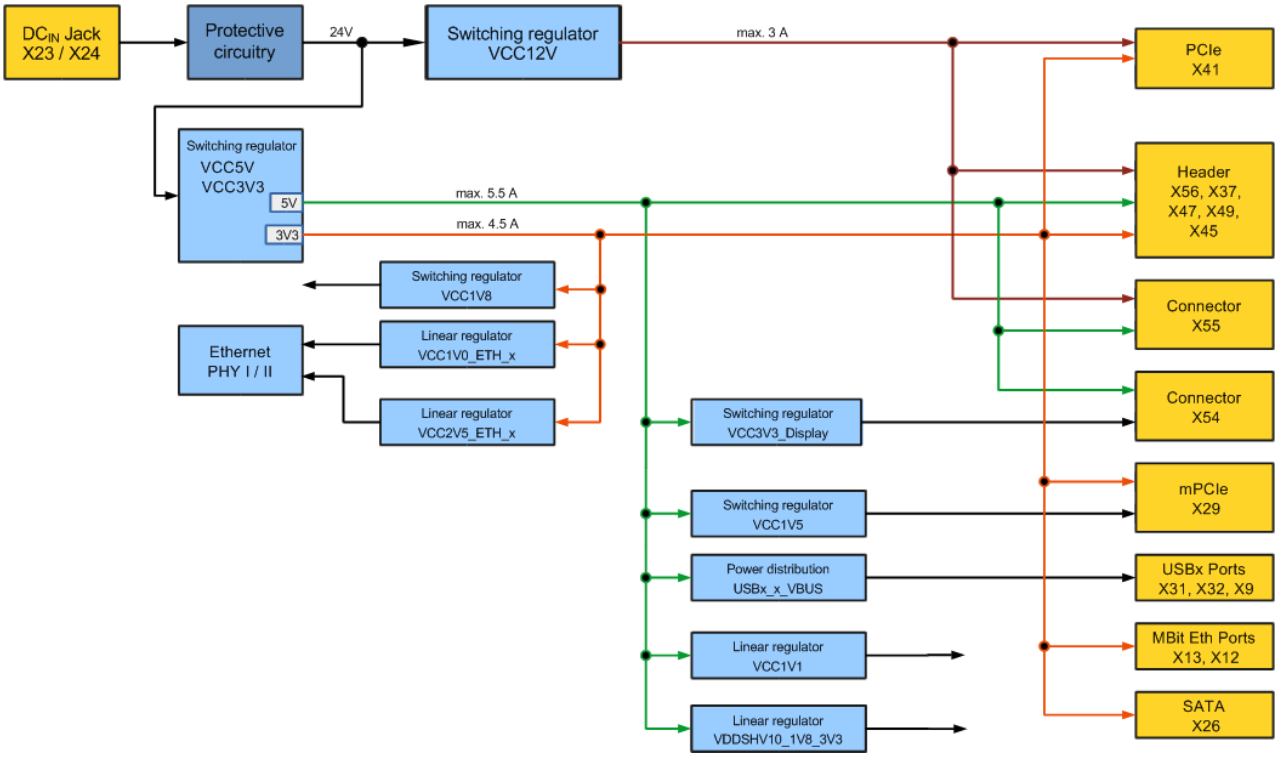

Figure 7: Block diagram power supply

The MBa57xx is supplied with 24 V via X23 or X24. From this voltage 1.0 V, 1.5 V, 2.5 V, 3.3 V, 5 V and 12 V are generated on the MBa57xx. These voltages are used to supply the components on the MBa57xx. All connectors share the available power.

The following table shows the voltages at the interfaces and headers on the MBa57xx.

Table 14: Voltages at MBa57xx headers

Connector	1.5 V	3.3 V	5 V	12 V
X11 (JTAG), X12, X13 (100 Mbit Eth), X14 (SD card), X26 (SATA)	–	Yes	–	–
X29 (mPCIe)	Yes	Yes	–	–
X37, X45, X47, X49, X56 (RGB)	–	Yes	Yes	Yes
X41 (PCIe)	–	Yes	–	Yes
X54 (LVDS)	–	Yes [1]	Yes	–
X55 (LVDS CMD)	–	–	Yes	Yes

Attention: Usage of PMIC_REGEN1	
	VCC3V3 and VDDSHV10_1V8_3V3 on the carrier board should be switched with signal PMIC_REGEN1 by the TQMa57xx, to avoid cross supply and errors in the power-up/down sequence.

1: Supplied by VCC3V3_DISPLAY.

3.1.7.1 Protective circuitry

V_{IN} of the MBa57xx also supplies the 3.3 V / 5 V and the 12 V switching regulators on the MBa57xx.
The protective circuit (Figure 8) has the following characteristics:

- Fuse, 4 A, slow blow
- Excess voltage protection diode
- PI filter
- Inverse-polarity protection
- Capacitors for voltage smoothing

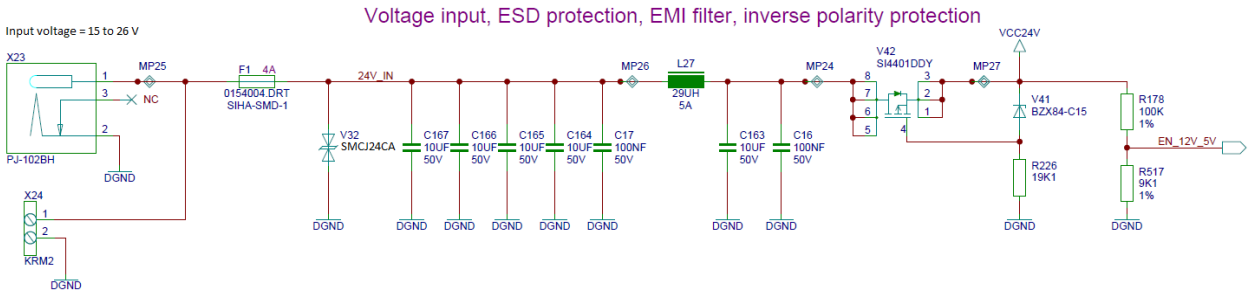

Figure 8: Protective circuit for V_{IN}

Table 15: Characteristics of protective circuit

Parameter	Min.	Typ.	Max.
Overcurrent limitation by fuse (slow blow)	–	4 A	–
Excess voltage limitation by SMBJ24CA	26.7 V	–	29.5 V

3.1.7.2 Power consumption

The MBa57xx, including a TQMa57xx, consumes 85 W under full load (all supply voltages are loaded with maximum current, e.g. by connecting devices at the pin headers). The power supply used must be specified accordingly. In most applications, however, the power consumption will be significantly lower.

3.1.7.3 Power supply connectors

Table 16: Power supply connectors

Connector	Manufacturer / Number	Description
X23	Cui Stack / PJ-102BH	DC jack 2.5 mm / 5.5 mm, nominal: 5 A / 24 V
X24	Lumberg / KRM2	2-pin screw terminal, 250 V / 15 A

3.2 Communication interfaces

3.2.1 USB 3.0 Super-Speed Host

The TQMa57xx connects via USB3.0 to the USB3.0 hub on the MBa57xx and configures the hub via the I2C4 bus.

The TUSB8041I USB hub provides three USB 3.0 super-speed Host interfaces and one USB2.0 hub interface.

The hub has one upstream port and four downstream ports. The USB connectors are supplied with 5 V via power distribution switches type TPS2561DRC. The switches have current monitoring and can switch off the bus voltage in case of overload and/or overheating. Please refer to the data sheets of the switch for detailed information.

USB3.0 Host1&2 are connected to a dual USB Type A socket (X31). USB Host3 is available at USB type Micro B socket X32.

The fourth interface is connected to the USB2.0 hub USB4604I.

The USB Host port of the TQMa57xx offers a theoretical data rate of 5 Gbit/s. This is shared among the connected ports.

Depending on the hardware and software used, the achievable read and write rates of the ports can vary.

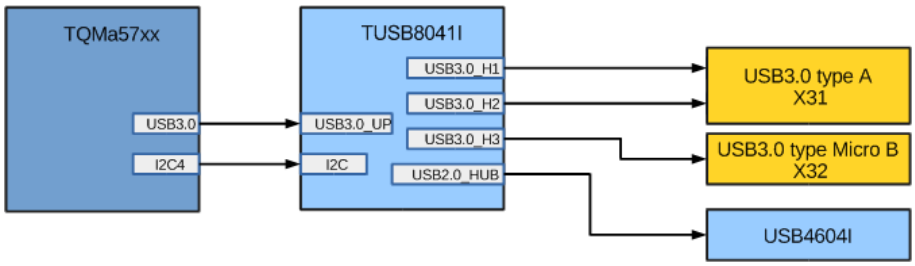

Figure 9: Block diagram USB 3.0 Hosts

3.2.1 USB 3.0 Super-Speed Host (continued)

Table 17: Pinout X31, USB 3.0 Host1&2, Type A

Pin	Pin name	Signal	Dir.	Remark
1	VBUS	USB3.0_H2_VBUS	P	200 µF to DGND + EMI Filter
2	D–	USB3.0_H2_DM_L	I/O	Common Mode Choke in series
3	D+	USB3.0_H2_DP_L	I/O	Common Mode Choke in series
4	DGND	DGND	P	–
5	SSRX–	USB3.0_H2_RXN_L	I/O	Common Mode Choke in series
6	SSRX+	USB3.0_H2_RXP_L	I/O	Common Mode Choke in series
7	DGND	DGND	P	–
8	SSTX–	USB3.0_H2_TXN_L	I/O	Common Mode Choke + AC coupling capacitor in series
9	SSTX+	USB3.0_H2_TXP_L	I/O	Common Mode Choke + AC coupling capacitor in series
10	VBUS	USB3.0_H1_VBUS	P	200 µF to DGND + EMI Filter
11	D–	USB3.0_H1_DM_L	I/O	Common Mode Choke in series
12	D+	USB3.0_H1_DP_L	I/O	Common Mode Choke in series
13	DGND	DGND	P	–
14	SSRX–	USB3.0_H1_RXN_L	I/O	Common Mode Choke in series
15	SSRX+	USB3.0_H1_RXP_L	I/O	Common Mode Choke in series
16	DGND	DGND	P	–
17	SSTX–	USB3.0_H1_TXN_L	I/O	Common Mode Choke + AC coupling capacitor in series
18	SSTX+	USB3.0_H1_TXP_L	I/O	Common Mode Choke + AC coupling capacitor in series
M1 – M4	–	DGND	P	–

Table 18: Pinout X32, USB 3.0 Host3, Micro B

Pin	Pin name	Signal	Dir.	Remark
1	VBUS	USB3.0_H3_VBUS	P	200 µF to DGND + EMI Filter
2	D–	USB3.0_H3_DM_L	I/O	Common Mode Choke in series
3	D+	USB3.0_H3_DP_L	I/O	Common Mode Choke in series
4	ID	USB3.0_H3_OTG_ID	I	Connected to I^2C Port Expander I (D22)
5	DGND	DGND	P	–
6	SSRX–	USB3.0_H3_RXN_L	I/O	Common Mode Choke in series
7	SSRX+	USB3.0_H3_RXP_L	I/O	Common Mode Choke in series
8	DGND	DGND	P	–
9	SSTX–	USB3.0_H3_TXN_L	I/O	Common Mode Choke + AC coupling capacitor in series
10	SSTX+	USB3.0_H3_TXP_L	I/O	Common Mode Choke + AC coupling capacitor in series
M1 – M6	–	DGND	P	–

3.2.2 USB 2.0 Hi-Speed Host

The TUSB8041I provides a chip-to-chip connection via USB2.0 to the USB2.0 hub, which is configured via the I2C4 bus.

The USB hub USB4604I provides four USB 2.0 Hi-Speed Host interfaces. The hub has one upstream port and four downstream ports. USB Host1&2 are routed to display connectors X55 and X56. Host3 is available at the SATA M.2 connector X26, and Host4 is available at the mPCIe connector X29.

The USB Host port of the TQMa57xx provides a theoretical data rate of 480 Mbit/s. The data rate is shared amongst the connected ports. The data rates of the ports can significantly deviate depending on the hardware and software used.

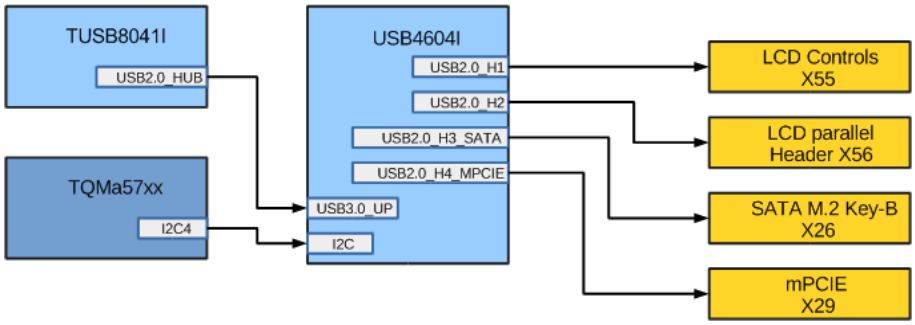

Figure 10: Block diagram USB 2.0 Hosts

The following tables show the pin assignment of the connectors used.

Table 19: Pinout X55, USB 2.0 Host1

Pin	Pin name	Signal	Dir.	Remark
13	D–	USB2.0_H1_D_N	I/O	Common Mode Choke in series
14	D+	USB2.0_H1_D_P	I/O	Common Mode Choke in series

Table 20: Pinout X56, USB 2.0 Host2

Pin	Pin name	Signal	Dir.	Remark
36	D–	USB2.0_H2_D_N	I/O	Common Mode Choke in series
38	D+	USB2.0_H2_D_P	I/O	Common Mode Choke in series

Table 21: Pinout X26, USB 2.0 Host3

Pin	Pin name	Signal	Dir.	Remark
9	D–	USB2.0_H3_SATA_N	I/O	Common Mode Choke in series
7	D+	USB2.0_H3_SATA_P	I/O	Common Mode Choke in series

Table 22: Pinout X29, USB 2.0 Host4

Pin	Pin name	Signal	Dir.	Remark
36	D–	USB2.0_H4_MPCIE_N	I/O	Common Mode Choke in series
38	D+	USB2.0_H4_MPCIE_P	I/O	Common Mode Choke in series

3.2.3 USB 2.0 Hi-Speed OTG

Both USB OTG interfaces of the TQMa57xx are provided on the MBa57xx.
OTG1 is available with all TQMa57xx variants as 5-pin Micro AB socket.
The OTG port of the TQMa57xx provides a theoretical data rate of 480 Mbit/s.
The data rate can significantly deviate depending on the hardware and software used.

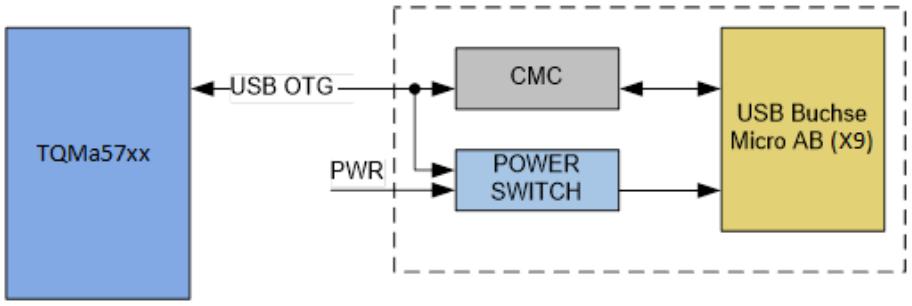

Figure 11: Block diagram USB 2.0 Hi-Speed OTG

The USB OTG interface of the TQMa57xx is connected on the MBa57xx to the USB2.0 Micro AB connector X9.
The following table shows the pin assignment.

Table 23: Pinout USB OTG, USB Micro AB, X9

Pin	Pin name	Signal	Dir.	Remark
1	VBUS	USB2_OTG_VBUS	P	100 µF to DGND; EMI filter
2	D–	USB2_OTG_N	I/O	Common Mode Choke in series
3	D+	USB2_OTG_P	I/O	Common Mode Choke in series
4	ID	USB2_OTG_ID	I	–
5	DGND	DGND	P	–
M1 – M6	DGND	DGND	P	–

3.2.4 Ethernet 10/100/1000BASE-T

All four Ethernet MACs of the TQMa57xx are connected to TI PHYs DP83867 on the MBa57xx via one MII interface each.
The Ethernet interfaces have their own PHY reset and interrupt signals.
The PHY DP83867 has boot straps to start with adjustable default values.
All boot straps can be adapted by means of assembly options. Further information is available in the MBa57xx schematics.
In addition to the sockets and PHYs, the PRU2 signals are routed to pin headers X13 and X12, see Table 46.

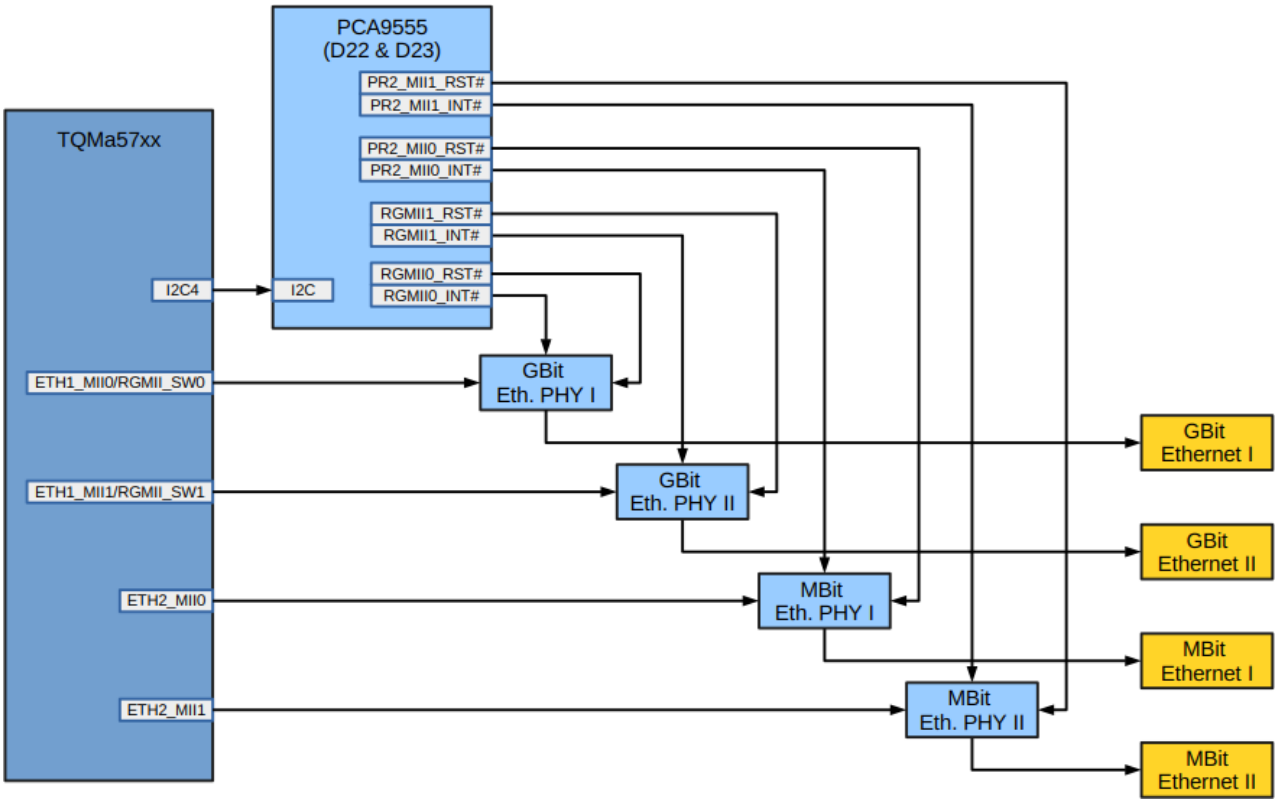

Figure 12: Block diagram Ethernet 10/100/1000BASE-T

3.2.5 CAN

The two CAN interfaces are designed differently. Depending on the processor version, CAN I can be connected as MCAN and a maximum of 5 Mbit/s can be transmitted. At the CAN II interface a maximum of 1 Mbit/s can be transmitted.

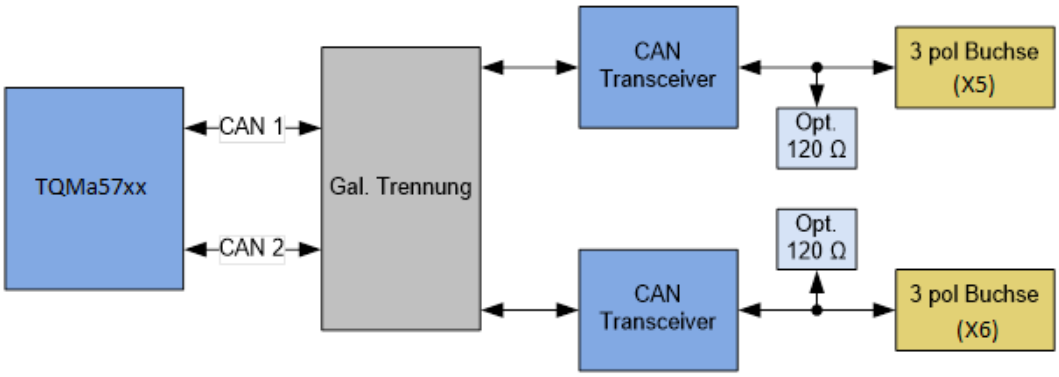

Figure 13: Block diagram CAN

Both TQMa57xx CAN interfaces are connected to CAN transceivers on the MBa57xx and routed to 3-pin connectors X5 and X6. Both interfaces are galvanically isolated with 1 kV. The CAN interfaces are not galvanically isolated from each other.
The CAN signals can be terminated with 120 Ω using DIP switches S3 and S7.

Table 24: Pinout CAN1, CAN2

CAN bus	Connector	Pin	Signal	Dir.	Remark
CAN1 CAN2	X5 X6	1	MCAN_HI	I/O	Galvanically isolated
		2	MCAN_LO	I/O	Galvanically isolated
		3	GND_CAN	P	Galvanically isolated

Table 25: CAN termination, DIP switches S3, S7

Switch	Signal	ON	OFF
S3-1	MCAN_HI	Terminated with 120 Ω	Not terminated
S3-2	MCAN_LO	Terminated with 120 Ω	Not terminated
S7-1	DCAN2_H	Terminated with 120 Ω	Not terminated
S7-2	DCAN2_L	Terminated with 120 Ω	Not terminated

3.2.6 RS-485

The TQMa57xx UART10 interface is routed to an RS-485 transceiver (SP491E), which provides the signals at the 9-pin D-Sub connector X7. The RS-485 interface is galvanically isolated with 500 V.

The interface is configured for full duplex operation by default, but can be switched to half duplex by an assembly option. In this case, the receiver is controlled by UART10_RTS#. The assembly option is shown in the MBa57xx schematics.

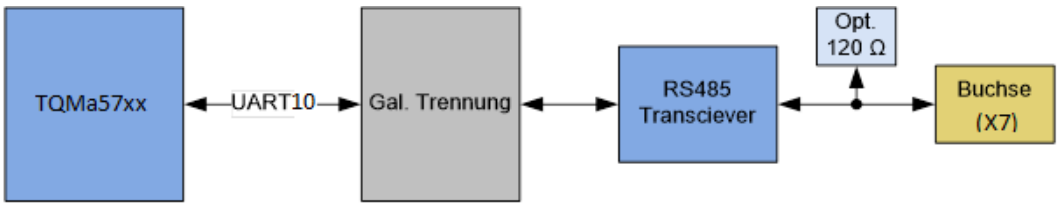

Figure 14: Block diagram RS-485

Table 26: Pinout RS-485, X7

Pin	Pin name	Signal	Dir.	Remark
1	A	RS485_A	I	Galvanically isolated
2	B	RS485_B	I	Galvanically isolated
3	Y	RS485_Y	O	Galvanically isolated
4	Z	RS485_Z	O	Galvanically isolated
5	GND	GND_RS485	P	Galvanically isolated

The RS-485 signals can be terminated with 120 Ω using DIP switch S5.

Table 27: RS-485 termination, DIP switch S5

Switch	ON	OFF
S5-1	Transmit path terminated with 120 Ω	Transmit path not terminated
S5-2	Receive path terminated with 120 Ω	Receive path not terminated

3.2.7 Debug interfaces

The debug interface is implemented on the MBa57xx as RS-232 and USB device interface. In both cases the TQMa57xx UART3 interface is used. No software configuration is required.

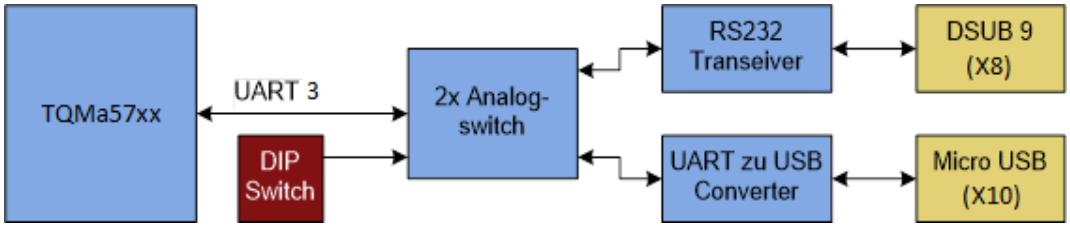

Figure 15: Block diagram RS-232 / Debug

Table 28 Pinout Debug RS-232, X8

Pin	Signal
1, 4, 6, 7, 8, 9	NC
2	RS232_RX
3	RS232_TX
5	DGND
M1, M2	DGND

Table 29 Pinout Debug USB, X10

Pin	Signal
1	USB_DBG_VBUS
2	USB_DBG_DM
3	USB_DBG_DP
4	NC
5	DGND
M1…M6	DGND

The debug interface can be set to RS-232 or USB with DIP switch S6.

Table 30: Debug interface, DIP switch S6

Switch	ON	OFF
S6	Debug-Interface USB-Device at X10	Debug-Interface RS-232 at X8

3.2.8 LVDS

An LVDS display can be connected to the MBa57xx (4× TX pairs). Since the AM57xx processor does not have a native LVDS interface, the LVDS signals are generated by an SN75LVDS83B transceiver connected to the parallel LCD interface.

The LVDS interface is routed to two DF19 connectors.

The first connector (30-pin, X54) provides the LVDS data signals as well as 3.3 V and 5 V.

The second connector (20-pin, X55) provides control lines and USB signals as well as 12 V and 5 V.

A High level at LVDS_SHDN# switches the LVDS transceiver on, a Low level at LVDS_SHDN# switches the LVDS transceiver off.

The LVDS transceiver is configured for 8-bit FORMAT-1 mode and operates at 65 MHz [2].

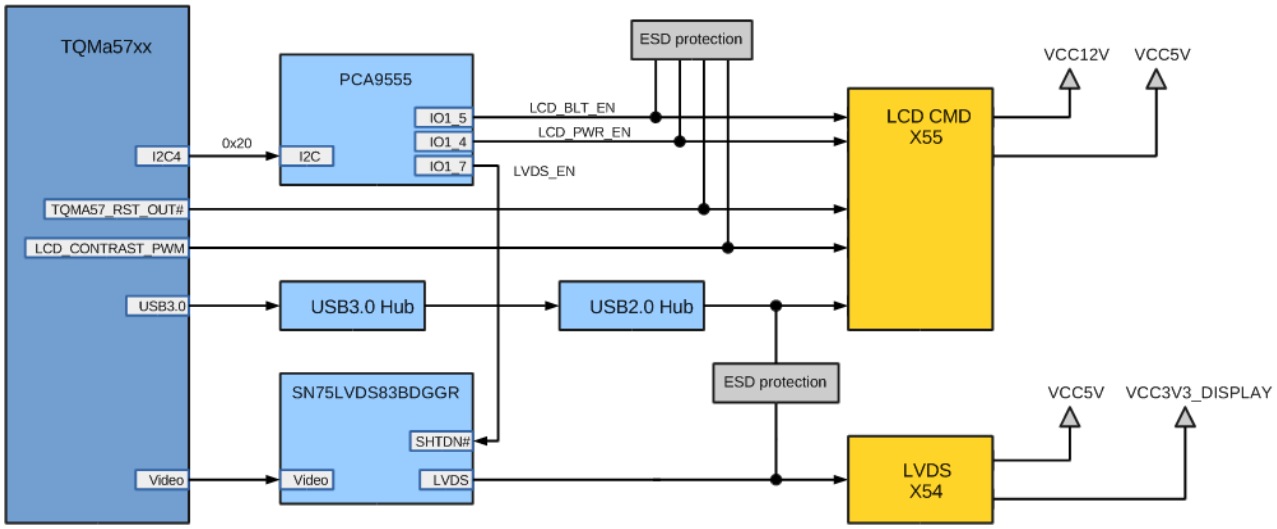

Figure 16: Block diagram LVDS

Table 31: Type of LVDS connectors

Connector	Manufacturer / Number	Description
X54	Hirose / DF19G-30P-1H	Board-to-Cable FFC connector, 30-pin, 1 mm pitch
X55	Hirose / DF19G-20P-1H	Board-to-Cable FFC connector, 20-pin, 1 mm pitch

2: See Texas Instruments Data Sheet SN75LVDS83B.

3.2.8 LVDS (continued)

Table 32: Pinout LVDS, X54

Pin	Signal	Remark
1	LVDS_TX0_N	ESD protected
2	LVDS_TX0_P	ESD protected
3	LVDS_TX1_N	ESD protected
4	LVDS_TX1_P	ESD protected
5	LVDS_TX2_N	ESD protected
6	LVDS_TX2_P	ESD protected
7	DGND	–
8	LVDS_CLK_N	ESD protected
9	LVDS_CLK_P	ESD protected
10	LVDS_TX3_N	ESD protected
11	LVDS_TX3_P	ESD protected
12	NC	–
13	NC	–
14	DGND	–
15	NC	–
16	NC	–
17	DGND	–
18	NC	–
19	NC	–
20	NC	–
21	NC	–
22	NC	–
23	NC	–
24	DGND	–
25	5 V	–
26	5 V	–
27	5 V	–
28	3.3 V	–
29	3.3 V	–
30	3.3 V	–
M1, M2	DGND	–

3.2.8 LVDS (continued)

Table 33: Pinout LVDS CMD, X55

Pin	Signal	Remark
1	12 V	–
2	12 V	–
3	12 V	–
4	DGND	–
5	DGND	–
6	DGND	–
7	5 V	–
8	5 V	–
9	DGND	–
10	DGND	–
11	USB2_H1_VBUS	ESD protected
12	DGND	–
13	USB_H2.0_H1_N	ESD protection + Common Mode Choke in series
14	USB_H2.0_H1_P	ESD protection + Common Mode Choke in series
15	DGND	–
16	DISPLAY_RST#	ESD protected
17	LCD_BLT_EN	ESD protected
18	LCD_PWR_EN	ESD protected
19	LCD_CONTRAST_PWM	ESD protected
20	DGND	–
M1, M2	DGND	–

3.2.9 Audio

Audio input and outputs are provided by the audio codec TLV320AIC3204. It is connected to the TQMa57xx via SAI (configured as I²S) and I²C. The audio codec provides microphone, line in and line out signals. The signals are routed to 3.5 mm jacks.

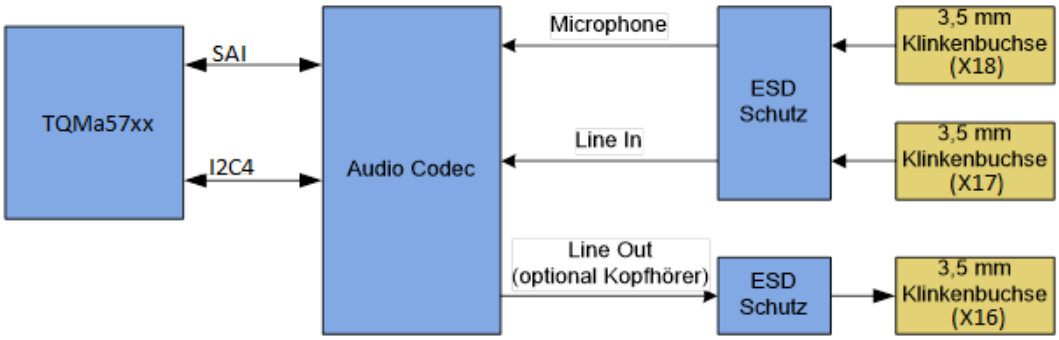

Figure 17: Block diagram Audio

An assembly option selects between line-out and headphone. The following table shows the possible configuration.

Table 34: Configuration Line-Out / headphone

Mode	R12	R13	R14	R15
Line-Out (default)	NP	NP	0 Ω	0 Ω
Headphone (optional)	0 Ω	0 Ω	NP	NP

Table 35: Pinout Line-Out, X16

Pin	Signal	Remark
1	GND_AUDIO	–
2A,2B	AUDIO_OUT_L	1 µF and 100 Ω in series; 47 nF to GND_AUDIO; ESD protection. Optional connection to HP_L
3	AUDIO_OUT_R	1 µF and 100 Ω in series; 47 nF to GND_AUDIO; ESD protection. Optional connection to HP_R

Table 36: Pinout Line-In, X17

Pin	Signal	Remark
1	GND_AUDIO	–
2A,2B	LINE_IN_L	470 nF in series; ESD protection
3	LINE_IN_R	470 nF in series; ESD protection

Table 37: Pinout Microphone, X18

Pin	Signal	Remark
1	GND_AUDIO	–
2A,2B	MIC_IN	2.2 kΩ in series to MIC_BIAS; ESD protection
3	GND_AUDIO	10 kΩ to GND_AUDIO, right channel not used

3.2.10 SD card

The SD card slot is directly with a 4-bit interface connected to the TQMa57xx SDHC controller.
The SDHC controller in the TQMa57xx supports the UHS-I mode, which is not used on the MBa57xx.
The maximum available mode is High-Speed. Booting from SD card is possible, see chapter 3.3.6.
All data lines are ESD protected.

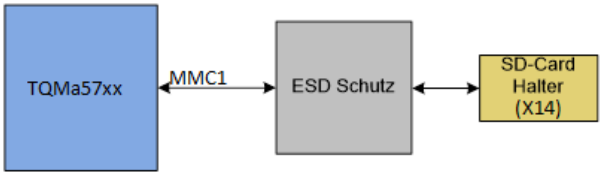

Figure 18: Block diagram SD card

Table 38: Pinout SD card, X14

Pin	Pin name	Signal	Remark
1	CD/DAT3/CS	MMC1_DAT3	10 kΩ PU to 3.3 V + ESD protection
2	CMD/DI	MMC1_CMD	10 kΩ PU to 3.3 V + ESD protection
3	VSS1	DGND	–
4	VDD	VCC3V3_SDCARD	3.3 V
5	CLK	MMC1_CLK	ESD protection
6	VSS2	DGND	–
7	DAT0/DO	MMC1_DAT0	10 kΩ PU to 3.3 V + ESD protection
8	DAT1	MMC1_DAT1	10 kΩ PU to 3.3 V + ESD protection
9	DAT2	MMC1_DAT2	10 kΩ PU to 3.3 V + ESD protection
CDS	CARD_DETECT	MMC1_CD#	10 kΩ PU to 3.3 V + ESD protection
COM	COMMON	DGND	–
WP	WRITE_PROTECT	MMC1_WP	10 kΩ PU to 3.3 V + ESD protection
M1, M2	SHIELD	DGND	SHIELD

3.2.11 PCIe

A PCIe slot (PCIe ×4) is available on the MBa57xx. One lane is routed to the PCIe connector, see pin assignment Table 40.

Every standard compliant PCIe card can be used.

The AM57xx internal clock is not PCIe compliant. For this reason, a PCIe compliant clock is generated on the MBa57xx with a dedicated clock generator. Detailed information can be found in the MBa57xx schematics.

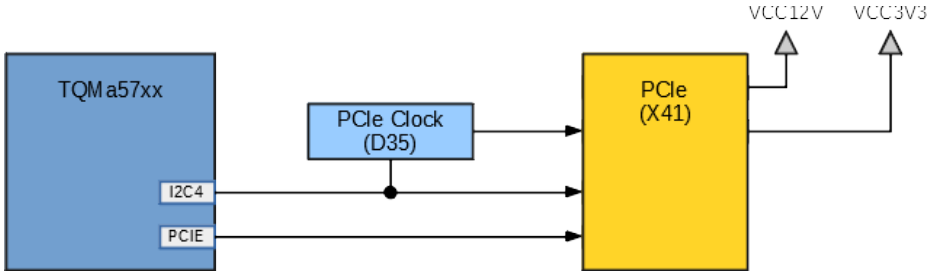

Figure 19: Block diagram PCIe

Table 39: Maximum currents, PCIe

Parameter	Min.	Typ.	Max.
Current @ 12 V	0	–	0.5 A
Current @ 3.3 V	0	–	3 A

Attention: PCIe card, maximum current	
	The voltages provided for the PCIe card may be loaded with the maximum currents specified in Table 39.

Note: PCIe clock	
	Since the PCIe clock provided by the AM57xx does not meet the PCIe specification, a dedicated clock generator is assembled on the MBa57xx. Further information can be found in the MBa57xx schematics.

3.2.11 PCIe (continued)

Table 40: Pinout PCIe, X41

Pin	Signal	Remark
A1	NC	–
A2	VCC12V_PCIE	See Table 39
A3	VCC12V_PCIE	See Table 39
A4	DGND	–
A5	NC	–
A6	NC	–
A7	NC	–
A8	NC	–
A9	VCC3V3_PCIE	See Table 39
A10	VCC3V3_PCIE	See Table 39
A11	PERST#	Connected to STKRST#. Connection to PCIE_RST# (from I^2C port expander) as assembly option.
A12	DGND	–
A13	MPCIE_SLOT_CLKP	PCIE clock from clock generator
A14	MPCIE_SLOT_CLKN	PCIE clock from clock generator
A15	DGND	–
A16	PCIE_RXP0	100 nF in series
A17	PCIE_RXN0	100 nF in series
A18	DGND	–
A19	NC	–
A20	DGND	–
A21	NC	–
A22	NC	–
A23	DGND	–
A24	DGND	–
A25	NC	–
A26	NC	–
A27	DGND	–
A28	DGND	–
A29	NC	–
A30	NC	–
A31	DGND	–
A32	NC	–
B1	VCC12V_PCIE	See Table 39
B2	VCC12V_PCIE	See Table 39
B3	VCC12V_PCIE	See Table 39
B4	DGND	–
B5	I2C4_SCL	–
B6	I2C4_SDA	–
B7	DGND	–
B8	VCC3V3_PCIE	See Table 39
B9	NC	–
B10	VCC3V3_PCIE	See Table 39
B11	PCIE_WAKE#	Assembly option: 10 kΩ PU to 3.3 V or GND. Default: none.
B12	NC	–
B13	DGND	–
B14	PCIE_TXP0	100 nF in series on TQMa57xx
B15	PCIE_TXN0	100 nF in series on TQMa57xx
B16	DGND	–
B17	NC	–
B18	DGND	–
B19	NC	–
B20	NC	–
B21	DGND	–
B22	DGND	–
B23	NC	–
B24	NC	–
B25	DGND	–
B26	DGND	–
B27	NC	–
B28	NC	–
B29	DGND	–
B30	NC	–
B31	NC	–
B32	DGND	–

3.2.12 Mini PCIe

A Mini PCIe slot (PCIe ×1) for full-size cards is available on the MBa57xx. Pin assignment see Table 40.

A Mini PCIe card (50.95 × 30 mm²) can be used. An additional SIM card holder is available, see chapter 3.2.11.

The AM57xx internal clock is not PCIe compliant. For this reason, a PCIe compliant clock is generated on the MBa57xx with a 9FGV0241AKILF clock generator. Detailed information can be found in the MBa57xx schematics.

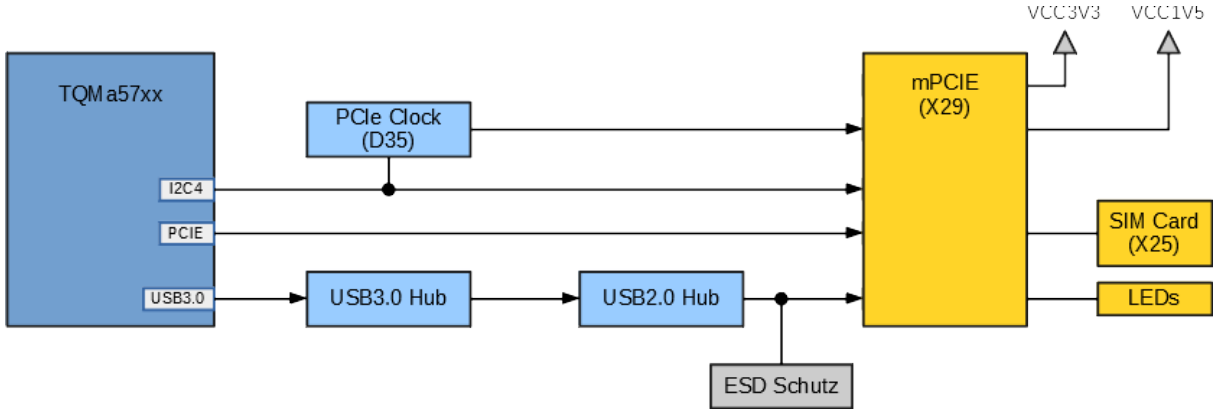

Figure 20: Block diagram Mini PCIe

Table 41: Maximum currents, Mini PCIe

Parameter	Min.	Typ.	Max.
Current @ 3.3 V	0	–	1.1 A
Current @ 1.5 V	0	–	0.375 A

Attention: Mini PCIe card, dimensions, maximum current	
	When using mPCIe cards, the distance between the board and the card must be taken into account. The connector for the card is located 3.7 mm above the board. With a heat sink screw connection with a maximum protrusion of 2 mm, the space defined in the PCIe specification is available. The voltages provided for the Mini PCIe card may be loaded with the maximum currents specified in Table 41.

3.2.12 Mini PCIe (continued)

Table 42: Pinout Mini PCIe, X29

Pin	Signal	Remark
1	PCIE_WAKE#	–
2	VCC3V3_MPCIE	See Table 41
3	NC	–
4	DGND	–
5	NC	–
6	VCC1V5_MPCIE	See Table 41
7	NC	–
8	SIM_PWR	SIM card signal, see Table 43
9	DGND	–
10	SIM_DATA	SIM card signal, see Table 43
11	MPCIE_CLKN	PCIE clock from clock generator
12	SIM_CLK	SIM card signal, see Table 43
13	MPCIE_CLKP	PCIE clock from clock generator
14	SIM_RST	SIM card signal, see Table 43
15	DGND	–
16	SIM_VPP	SIM card signal, see Table 43
17	NC	–
18	DGND	–
19	NC	–
20	PCIE_DIS#	Assembly option: 10 kΩ PU to 3.3 V or PD. Default: none
21	DGND	–
22	PCIE_RST#	Assembly option: 10 kΩ PU to 3.3 V or PD, 0 Ω to GPIO_EXP_IO6. Default: none
23	PCIE_RXN1	100 nF in series
24	VCC3V3_MPCIE	See Table 41
25	PCIE_RXP1	100 nF in series
26	DGND	–
27	DGND	–
28	VCC1V5_MPCIE	See Table 41
29	DGND	–
30	I2C4_SCL	I2C4 address mapping see Table 9
31	PCIE_TXN1	100 nF in series on TQMa57xx
32	I2C4_SDA	I2C4 address mapping see Table 9
33	PCIE_TXP1	100 nF in series on TQMa57xx
34	DGND	–
35	DGND	–
36	USB2.0_MPCIE_N_L	Common Mode Choke in series
37	DGND	–
38	USB2.0_MPCIE_P_L	Common Mode Choke in series
39	VCC3V3_MPCIE	See Table 41
40	DGND	–
41	VCC3V3_MPCIE	See Table 41
42	LED_WWAN#	Connected to VCC3V3_MPCIE with 270 Ω and green LED
43	DGND	–
44	LED_WLAN#	Connected to VCC3V3_MPCIE with 270 Ω and green LED
45	NC	–
46	LED_WPAN#	Connected to VCC3V3_MPCIE with 270 Ω and green LED
47	NC	–
48	VCC1V5_MPCIE	See Table 41
49	NC	–
50	DGND	–
51	NC	–
52	VCC3V3_MPCIE	See Table 41

3.2.13 SIM card

Table 43: Pinout SIM card, X25

Pin	Pin name	Signal
C1	PWR	SIM_PWR
C2	RST	SIM_RST
C3	CLK	SIM_CLK
C4	(NA)	–
C5	DGND	DGND
C6	VPP	SIM_VPP
C7	DATA	SIM_DATA
SW1-2	–	–

3.2.14 SATA

The MBa57xx provides an M.2 interface for M.2 SATA cards sizes 2242, 2260, or 2280.

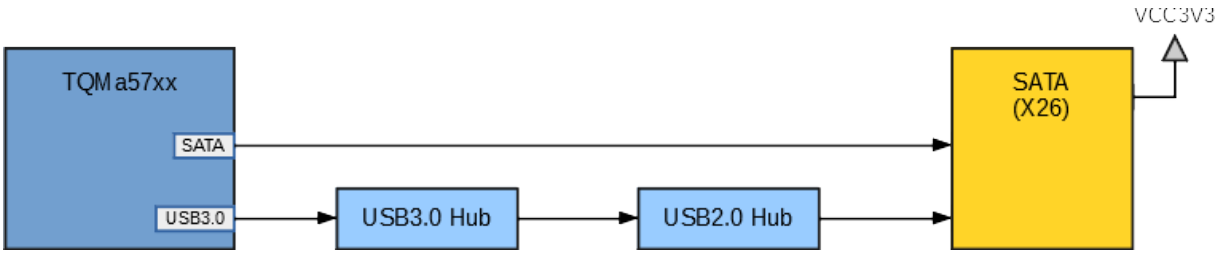

Figure 21: Block diagram SATA

Attention: Space between MBa57xx and M.2 card	
	When selecting a SATA card, the distance of 2.48 mm between the MBa57xx and the M.2 card, as defined by the M.2 connector X26, must be observed.

3.2.14 SATA (continued)

Table 44: Pinout SATA, X26

Pin	Signal	Remark
1	M2_CONFIG3	10 kΩ PU to 3.3 V
2	VCC3V3	–
3	DGND	–
4	VCC3V3	–
5	DGND	–
6	FULL_CARD_POWER_OFF#	Assembly option: 10 kΩ PU to 3.3 V
7	USB2.0_SATA_D+	Common mode choke in series
8	NC	–
9	USB2.0_SATA_D–	Common mode choke in series
10	LED1#	LED and 270 Ω to 3.3 V. Optional: 270 Ohm Ω to SATA1_LED from TQMa57xx.
11	DGND	–
20	NC	–
21	M2_CONFIG0	10 kΩ PU to 3.3 V
22 – 26	NC	–
27	DGND	–
28 – 32	NC	–
33	DGND	–
34 – 37	NC	–
38	DEVSLEEP	Assembly option: 100 kΩ PU to 3.3 V or 0 Ω to DGND. Default: none
39	DGND	–
40	NC	–
41	SATA1_RXP0	10 nF in series
42	NC	–
43	SATA1_RXN0	10 nF in series
44	NC	–
45	DGND	–
46	NC	–
47	SATA1_TXN0	10 nF in series on TQMa57xx
48	NC	–
49	SATA1_TXP0	10 nF in series on TQMa57xx
50	PERST#	10 kΩ PU to 3.3V. Connected to STKRST#, optional to SATA_M2_RST#, IO1_7
51	DGND	–
52 – 56	NC	–
57	DGND	–
58 – 66	NC	–
67	RESET	1.8 V, only for WWAN
68	SUSCLK	Assembly option: 100 kΩ PU to 3.3 V or 0 Ω to DGND. Default: none
69	M2_CONFIG1	10 kΩ PU to 3.3 V
70	VCC3V3	–
71	DGND	–
72	VCC3V3	–
73	DGND	–
74	VCC3V3	–
75	M2_CONFIG2	10 kΩ PU to 3.3 V
M1, M2	DGND	–

3.2.15 HDMI

The HDMI 1.4a interface of the AM57xx is connected to a standard HDMI port on the MBa57xx.

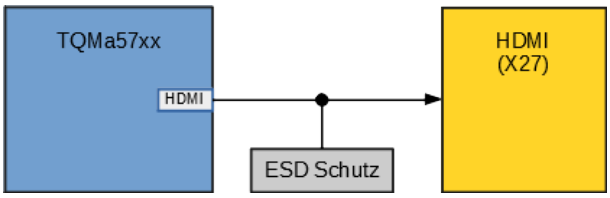

Figure 22: Block diagram HDMI

The following table shows the pinout of the HDMI interface.

Table 45: Pinout HDMI, X27

Pin	Signal	Remark
P1	CON_HDMI_TX2–	–
P2	DGND	–
P3	CON_HDMI_TX2+	–
P4	CON_HDMI_TX1–	–
P5	DGND	–
P6	CON_HDMI_TX1+	–
P7	CON_HDMI_TX0–	–
P8	DGND	–
P9	CON_HDMI_TX0+	–
P10	CON_HDMI_CLK–	–
P11	DGND	–
P12	CON_HDMI_CLK+	–
P13	CON_HDMI_CEC	–
P14	NC	Reserved for HDMI Ethernet and Audio
P15	CON_HDMI_SCL	–
P16	CON_HDMI_SDA	–
P17	DGND	–
P18	CON_HDMI_5V_OUT	55 mA max, 5V_OUT of TPD12S016RKT
P19	CON_HDMI_HPD	–
M1 – M4	DGND	–

3.2.16 100 mil headers

All signals not used on the TQMa57xx are routed to headers X12, X13, X36, X37, X44 ~ X51, and X56 on the MBa57xx.
Furthermore, some of the signals used are also routed to headers for reference and measurement purposes.
All headers have a 100 mil pitch.
The headers are positioned in such a way that adapter boards with customer-specific circuitry can easily be plugged in.

Figure 23: Block diagram headers X12, X13, X36, X37, X44 ~ X51, X56

The double grouping of the tables corresponds to the mechanical header arrangement on the MBa57xx.

Table 46: Pinout 10/100 Mbit Ethernet ports, header X13, X12

Group	Signal	Pin		Pin	Signal	Group
Power	VCC3V3	1	X13	2	PR2_MII0_RXD[0]	ETH2_MII0
ETH2_MDIO	PR2_MDIO_DATA	3		4	PR2_MII0_RXD[1]	ETH2_MII0
ETH2_MDIO	PR2_MDIO_MDCLK	5		6	PR2_MII0_RXD[2]	ETH2_MII0
ETH2_MII0	PR2_MII0_COL	7		8	PR2_MII0_RXD[3]	ETH2_MII0
ETH2_MII0	PR2_MII0_CRS	9		10	PR2_MII0_MT_CLK	ETH2_MII0
ETH2_MII0	PR2_MII0_MR_CLK	11		12	PR2_MII0_TXD[0]	ETH2_MII0
ETH2_MII0	PR2_MII0_RXDV	13		14	PR2_MII0_TXD[1]	ETH2_MII0
ETH2_MII0	PR2_MII0_RXER	15		16	PR2_MII0_TXD[2]	ETH2_MII0
ETH2_MII0	PR2_MII0_RXLINK	17		18	PR2_MII0_TXD[3]	ETH2_MII0
Power	DGND	19		20	PR2_MII0_TXEN	ETH2_MII0
Group	Signal	Pin		Pin	Signal	Group
Power	VCC3V3	1	X12	2	PR2_MII1_RXD[0]	ETH2_MII0
ETH2_MDIO	PR2_MDIO_DATA	3		4	PR2_MII1_RXD[1]	ETH2_MII0
ETH2_MDIO	PR2_MDIO_MDCLK	5		6	PR2_MII1_RXD[2]	ETH2_MII0
ETH2_MII1	PR2_MII1_COL	7		8	PR2_MII1_RXD[3]	ETH2_MII0
ETH2_MII1	PR2_MII1_CRS	9		10	PR2_MII1_MT_CLK	ETH2_MII0
ETH2_MII1	PR2_MII1_MR_CLK	11		12	PR2_MII1_TXD[0]	ETH2_MII0
ETH2_MII1	PR2_MII1_RXDV	13		14	PR2_MII1_TXD[1]	ETH2_MII0
ETH2_MII1	PR2_MII1_RXER	15		16	PR2_MII1_TXD[2]	ETH2_MII0
ETH2_MII1	PR2_MII1_RXLINK	17		18	PR2_MII1_TXD[3]	ETH2_MII0
Power	DGND	19		20	PR2_MII1_TXEN	ETH2_MII0

3.2.16 100 mil headers (continued)

Table 47: Pinout header X37, X36

Group	Signal	Pin		Pin	Signal	Group
Power	DGND	1	X37	2	DGND	Power
Power	VCC12V	3		4	VCC3V3	Power
Power	VCC5V	5		6	VCC3V3	Power
Power	DGND	7		8	DGND	Power
PR1_PRU0	PR1_PRU0_GPI1_AH3	9		10	PR1_PRU0_GPO5_AG4	PR1_PRU0
PR1_PRU0	PR1_PRU0_GPI2_AH5	11		12	PR1_PRU0_GPO6_AG2	PR1_PRU0
PR1_PRU0	PR1_PRU0_GPI3_AG6	13		14	PR1_PRU0_GPO7_AG3	PR1_PRU0
PR1_PRU0	PR1_PRU0_GPI4_AH4	15		16	PR1_PRU0_GPO8_AG5	PR1_PRU0
I²C Expander	GPIO_EXP_IO5 [3]	17		18	PR1_PRU0_GPO9_AF2	PR1_PRU0
I²C Expander	GPIO_EXP_IO6 [4]	19		20	GPIO2_1_P9	GPIO2
Group	Signal	Pin		Pin	Signal	Group
I²C Expander	GPIO_EXP_IO7 [5]	1	X36	2	GPIO2_2_P4	GPIO2
Power	DGND	3		4	DGND	Power
GPIO3	GPIO3_25_AE6	5		6	GPIO2_28_N2	GPIO2
GPIO3	GPIO3_26_AD2	7		8	GPIO2_30_AG8	GPIO2
GPIO3	GPIO3_27_AD3	9		10	GPIO2_31_AH7	GPIO2
GPIO1	GPIO1_1_AC17	11		12	MCASP5_AA4	MCASP5
GPIO1	GPIO1_2_AB16	13		14	MCASP5_AB3	MCASP5
GPIO7	GPIO7_3_R6	15		16	GPIO7_17_B24	GPIO7
GPIO7	GPIO7_16_G17	17		18	DGND	Power
Power	DGND	19		20	DGND	Power

3: Optional AUDIO_RST#.
4: Optional PCIE_RST#.
5: Optional DISPLAY_RST#.

3.2.16 100 mil headers (continued)

Table 48: Pinout header X45, X44

Group	Signal	Pin		Pin	Signal	Group
Power	DGND	1	X45	2	DGND	Power
Power	VCC12V	3		4	VCC3V3	Power
Power	VCC5V	5		6	VCC3V3	Power
Power	DGND	7		8	DGND	Power
GPIO5	GPIO5_6_E12	9		10	GPIO4_0_G6	GPIO4
GPIO5	GPIO5_7_F12	11		12	GPIO4_1_F2 [6]	GPIO4
GPIO5	GPIO5_8_C12	13		14	GPIO4_2_F3 [7]	GPIO4
GPIO5	GPIO5_9_D12	15		16	GPIO4_5_D2	GPIO4
MCASP4	MCASP4_C18	17		18	GPIO5_1_J14	GPIO5
MCASP2	MCASP2_A15	19		20	GPIO5_5_J11	GPIO5
Group	Signal	Pin		Pin	Signal	Group
MCASP2	MCASP2_B15	1	X44	2	GPIO3_28_E1	GPIO3
Power	DGND	3		4	DGND	Power
GPIO6	GPIO6_16_F21	5		6	GPIO3_3_AF8	GPIO3
GPIO6	GPIO6_19_B26	7		8	GPIO3_6_AG7	GPIO3
GPIO3	GPIO3_29_G2	9		10	GPIO3_17_AF6	GPIO3
GPIO3	GPIO3_30_H7	11		12	GPIO3_18_AF3	GPIO3
GPIO3	GPIO3_0_AD9	13		14	GPIO3_20_AF1	GPIO3
GPIO3	GPIO3_1_AF9	15		16	GPIO3_21_AE3	GPIO3
GPIO3	GPIO3_2_AE9	17		18	GPIO3_22_AE5	GPIO3
Power	DGND	19		20	DGND	Power

6: PMIC_INT on TQMa57xx.
7: TEMP_INT# on TQMa57xx.

3.2.16 100 mil headers (continued)

Table 49: Pinout header X47, X46

Group	Signal	Pin		Pin	Signal	Group
Power	DGND	1	X47	2	DGND	Power
Power	VCC12V	3		4	VCC3V3	Power
Power	VCC5V	5		6	VCC3V3	Power
Power	DGND	7		8	DGND	Power
Power	PMIC_PWRON#	9		10	RMII_MHZ_50_CLK	RMII Ref Clock
Power	PMIC_REGEN1	11		12	GPIO3_23_AE1 [8]	GPIO3
Reset	RESET_TO_TQMA57#	13		14	GPIO3_23_AE1 [9]	GPIO3
Reset	RSTOUT_FROM_TQMA57#	15		16	NMIN_DSP	INTC
Reset	PORZ_FROM_TQMA57#	17		18	CPU_WAKEUP0_TO_TQMA57	RTC
Power	DGND	19		20	DGND	Power
Group	Signal	Pin		Pin	Signal	Group
Power	VCC3V3	1	X46	2	QSPI_SCK	QSPI
MMC4	MMC4_DAT2	3		4	QSPI_SS0#	QSPI
MMC4	MMC4_DAT3	5		6	QSPI_SS1#	QSPI
MMC4	MMC4_CMD	7		8	QSPI_RTCLK	QSPI
MMC4	MMC4_CLK	9		10	QSPI_DATA0	QSPI
MMC4	MMC4_DAT0	11		12	QSPI_DATA1	QSPI
MMC4	MMC4_DAT1	13		14	QSPI_DATA2	QSPI
MMC4	MMC4_CD#	15		16	QSPI_DATA3	QSPI
MMC4	MMC4_WP	17		18	DGND	Power
Power	DGND	19		20	DGND	Power

8: Can be used as USB_OTG_VBUS detection.
9: Can be used as USB_OTG_ID detection.

3.2.16 100 mil headers (continued)

Table 50: Pinout header X49, X48

Group	Signal	Pin		Pin	Signal	Group
Power	VCC5V	1	X49	2	VCC3V3	Power
Power	VCC5V	3		4	VCC3V3	Power
Power	DGND	5		6	DGND	Power
Power	DGND	7		8	DGND	Power
Power	VUSB_VBUS2	9		10	VBAT_3V	Power
Power	DGND	11		12	VCC12V	Power
Power	USB2_SATA_VBUS	13		14	VCC1V7_E-FUSE	Power
Power	DGND	15		16	DGND	Power
Power	USB2_MPCIE_VBUS	17		18	NC	–
Power	DGND	19		20	NC	–
Group	Signal	Pin		Pin	Signal	Group
–	NC	1	X48	2	NC	–
–	NC	3		4	NC	–
–	NC	5		6	DGND	Power
Power	DGND	7		8	NC	–
I2C5	I2C5_SCL	9		10	NC	–
I2C5	I2C5_SDA	11		12	DGND	Power
Power	DGND	13		14	UART8_RTS#	UART8
UART4	UART4_RXD	15		16	UART8_RXD	UART8
UART4	UART4_TXD	17		18	UART8_TXD	UART8
Power	DGND	19		20	DGND	Power

3.2.16 100 mil headers (continued)

Table 51: Pinout GPMC bus, header X51, X50

Group	Signal	Pin		Pin	Signal	Group
Power	DGND	1	X51	2	DGND	Power
GPMC	GPMC_A[1]	3		4	GPMC_AD[0]	GPMC
GPMC	GPMC_A[2]	5		6	GPMC_AD[1]	GPMC
GPMC	GPMC_A[3]	7		8	GPMC_AD[2]	GPMC
GPMC	GPMC_A[4]	9		10	GPMC_AD[3]	GPMC
GPMC	GPMC_A[5]	11		12	GPMC_AD[4]	GPMC
GPMC	GPMC_A[6]	13		14	GPMC_AD[5]	GPMC
GPMC	GPMC_A[7]	15		16	GPMC_AD[6]	GPMC
GPMC	GPMC_A[8]	17		18	GPMC_AD[7]	GPMC
GPMC	GPMC_A[9]	19		20	GPMC_AD[8]	GPMC
Group	Signal	Pin		Pin	Signal	Group
GPMC	GPMC_A[10]	1	X50	2	GPMC_AD[9]	GPMC
GPMC	GPMC_A27_AF4_VAR	3		4	GPMC_AD[10]	GPMC
GPMC	GPMC_A27_G1	5		6	GPMC_AD[11]	GPMC
QSPI	QSPI_SS1#	7		8	GPMC_AD[12]	GPMC
GPMC	GPMC_WE#	9		10	GPMC_AD[13]	GPMC
GPMC	GPMC_OE#_RE#	11		12	GPMC_AD[14]	GPMC
GPMC	GPMC_CLK	13		14	GPMC_AD[15]	GPMC
GPMC	GPMC_BE#[0]	15		16	GPMC_CS0	GPMC
GPMC	GPMC_BE#[1]	17		18	GPMC_ADV#_ALE	GPMC
Power	DGND	19		20	DGND	Power

3.2.16 100 mil headers (continued)

Table 52: Pinout header X56

Group	Signal	Pin		Pin	Signal	Group
Power	VCC12V	1	X56	2	VCC3V3	Power
Power	VCC5V	3		4	VCC3V3	Power
Power	DGND	5		6	DGND	Power
LCD	VOUT1_CLK_R	7		8	VOUT1_DE_R	LCD
LCD	VOUT1_HSYNC	9		10	VOUT1_D_R[1]	LCD
LCD	VOUT1_VSYNC	11		12	VOUT1_D_R[3]	LCD
LCD	VOUT1_D_R[0]	13		14	VOUT1_D_R[5]	LCD
LCD	VOUT1_D_R[2]	15		16	VOUT1_D_R[7]	LCD
LCD	VOUT1_D_R[4]	17		18	VOUT1_D_R[9]	LCD
LCD	VOUT1_D_R[6]	19		20	VOUT1_D_R[11]	LCD
LCD	VOUT1_D_R[8]	21		22	VOUT1_D_R[13]	LCD
LCD	VOUT1_D_R[10]	23		24	VOUT1_D_R[15]	LCD
LCD	VOUT1_D_R[12]	25		26	VOUT1_D_R[17]	LCD
LCD	VOUT1_D_R[14]	27		28	VOUT1_D_R[19]	LCD
LCD	VOUT1_D_R[16]	29		30	VOUT1_D_R[21]	LCD
LCD	VOUT1_D_R[18]	31		32	VOUT1_D_R[23]	LCD
LCD	VOUT1_D_R[20]	33		34	USB_H2_VBUS	Power
LCD	VOUT1_D_R[22]	35		36	USB_H2_N	USB2
Power	DGND	37		38	USB_H2_P	USB2
I2C4	I2C4_SCL	39		40	DGND	Power
I2C4	I2C4_SDA	41		42	NC	–
SPI1	SPI1_D1 [10]	43		44	SPI1_D0	SPI1 [10]
SPI1	SPI1_CS0	45		46	SPI1_SCLK	SPI1
–	NC	47		48	DGND	Power
LCD	LCD_PWR_EN	49		50	LCD_BLT_EN	LCD
LCD	DISPLAY_RST#	51		52	LCD_CONTRAST_PWM	LCD
Power	DGND	53		54	DGND	Power
Touch	TOUCH_Y+	55		56	TOUCH_X+	Touch
Touch	TOUCH_Y–	57		58	TOUCH_X–	Touch
Power	DGND	59		60	DGND	Power

10: SPI1_D0 and SPI1_D1 can be configured as MISO or MOSI.

3.3 Diagnostic- and user interfaces

3.3.1 Diagnostic LEDs

The MBa57xx provides 32 diagnostic and status LEDs to indicate the system condition.

Table 53: Diagnostic LEDs

Function	Reference	Colour	Signal
USB	V62	Green	USB2_H1_VBUS (lit when VBUS of USB2.0 Host1 is active)
	V63	Green	USB2_H2_VBUS (lit when VBUS of USB2.0 Host2 is active)
	V64	Green	USB2_H3_VBUS (lit when VBUS of USB2.0 Host3 is active)
	V65	Green	USB2_H4_VBUS (lit when VBUS of USB2.0 Host4 is active)
	V66	Green	USB3_H1_VBUS (lit when VBUS of USB3.0 Host1 is active)
	V67	Green	USB3_H2_VBUS (lit when VBUS of USB3.0 Host2 is active)
	V68	Green	USB3_H3_VBUS (lit when VBUS of USB3.0 Host3 is active)
	V25	Green	USB2_OTG_VBUS (lit when VBUS of USB2 OTG is active)
mPCIe	V91	Green	Mini PCIe WWAN
	V92	Green	Mini PCIe WLAN
	V93	Green	Mini PCIe WPAN
SATA	V14	Green	LED lit when SATA is active
GPIO	V70	Green	LED on port expander (I2C4:0x21) Port IO0_3 (lit when port high)
	V69	Green	LED on port expander (I2C4:0x21) Port IO0_4 (lit when port high)
Power	V22	Green	Status 24 V (lit when supply 24 V active)
	V21	Green	Status 12 V (lit when supply 12 V active)
	V23	Green	Status 5 V (lit when supply 5 V active)
	V24	Yellow	Status 3.3 V (lit when supply 3.3 V active)
	V20	Green	Status 3.3 V Mini PCIe (lit when supply 3.3 V for Mini PCIe active)
	V59	Green	Status 1.8 V (lit when supply 1.8 V active)
	V60	Green	Status 1.5 V (lit when supply 1.5 V active)
	V61	Green	Status 1.1 V (lit when supply 1.1 V active)
USB Debug	V85	Green	LED lit when USB Debug is active
Eth	X52	Yellow	Activity LED Gbit Eth 1 (lit when active)
		Green	Error LED Gbit Eth 1 (lit when link is active, flashes during data transfer)
	X53	Yellow	Activity LED Gbit Eth 2 (lit when active)
		Green	Error LED Gbit Eth 2 (lit when link is active, flashes during data transfer)
	X21A	Yellow	Activity LED 100 Mbit Eth 1 (lit when active)
		Green	Error LED 100 Mbit Eth 1 (lit when link is active, flashes during data transfer)
	X21B	Yellow	Activity LED 100 Mbit Eth 2 (lit when active)
		Green	Error LED 100 Mbit Eth 2 (lit when link is active, flashes during data transfer)
Reset	V82	Red	Reset LED (lit when TQMa57xx is in reset)
		Green	Reset LED (lit when PMIC_REGEN1 = HIGH ⇨ “Power Good” on TQMa57xx)

3.3.2 GP push buttons

Three GP push buttons S10, S11, and S12, are connected to a port expander PCA9555PW on the MBa57xx. The port expander is interrupt-capable by signal GPIO2_2_P4#.

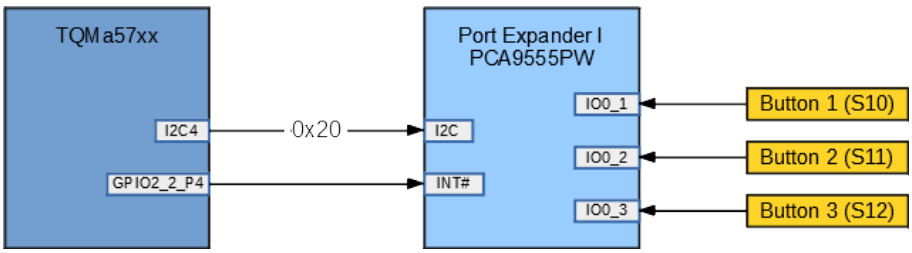

Figure 24: Block diagram GP push buttons

3.3.3 Buzzer

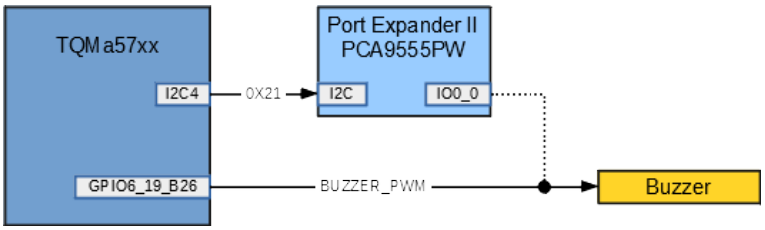

Figure 25: Block diagram buzzer

The MBa57xx provides a buzzer. The buzzer can be activated by GPIO6_19_B26 (X2-69) of the TQMa57xx, or by IO0_0 from Port Expander II, D23, see Table 11. A high level activates the buzzer.

3.3.4 Power-On and Reset push button

For further information about Power-On (S9) and Reset push button (S8), see chapter 3.1.6.

3.3.5 CAN and RS-485 termination

For further information about CAN (S3, S7) and RS-485 termination (S5), see chapter 3.2.5 and 3.2.6.

3.3.6 Boot-Mode configuration

With the MBa57xx all boot sources available for the TQMa57xx can be used:

- eMMC
- QSPI Nor Flash
- SD card

Information about the boot configurations of the AM57xx can be found in the TQMa57xx User's Manual.

- ➢ A High level at BOOT_CFG_EN# decouples DIP switches S[1:2] from the GPMC bus.
- ➢ A Low level at BOOT_CFG_EN# connects DIP switches S[1:2] to the GPMC bus. (Default)

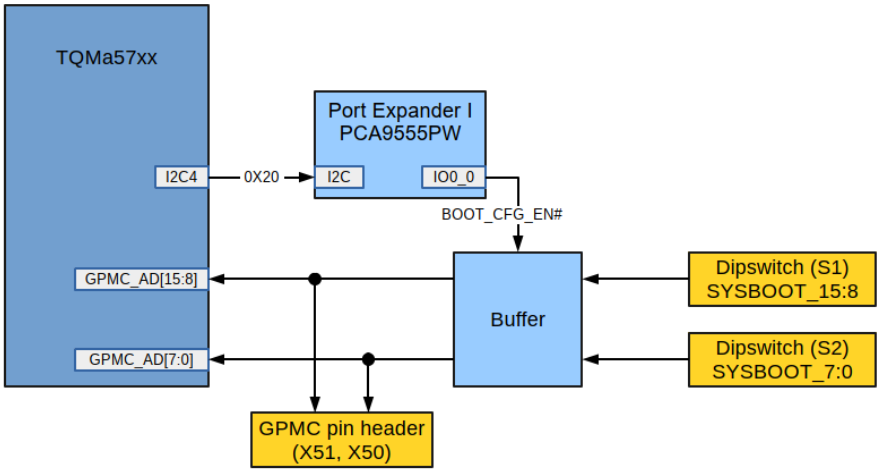

Figure 26: Block diagram Boot Mode DIP switches S1, S2

The following tables describe the DIP switch settings for the different boot sources.
Further settings, such as transfer modes and CPU clock, can be found in the User's Manual of the TQMa57xx (12).
Switch position 1 means ON, switch position 0 means OFF.

Table 54: Boot-Mode configuration, DIP switches S1, S2

DIP	Switch	GPMC	SYSBOOT	eMMC	SD card	QSPI NOR	TQMa57xx
S1	1	GPMC_AD[15]	SYSBOOT_15	0	0	0	TQMa571x
				1	1	1	TQMa572x / TQMa574x
	2	GPMC_AD[14]	SYSBOOT_14	0	0	0	–
	3	GPMC_AD[13]	SYSBOOT_13	0	0	0	–
	4	GPMC_AD[12]	SYSBOOT_12	0	0	0	–
	5	GPMC_AD[11]	SYSBOOT_11	0	0	0	–
	6	GPMC_AD[10]	SYSBOOT_10	0	0	0	–
	7	GPMC_AD[9]	SYSBOOT_9	0	0	0	–
	8	GPMC_AD[8]	SYSBOOT_8	1	1	1	–
S2	1	GPMC_AD[7]	SYSBOOT_7	0	0	0	–
	2	GPMC_AD[6]	SYSBOOT_6	0	0	0	–
	3	GPMC_AD[5]	SYSBOOT_5	1	1	1	–
	4	GPMC_AD[4]	SYSBOOT_4	0	1	1	–
	5	GPMC_AD[3]	SYSBOOT_3	0	0	0	–
	6	GPMC_AD[2]	SYSBOOT_2	0	0	1	–
	7	GPMC_AD[1]	SYSBOOT_1	0	0	1	–
	8	GPMC_AD[0]	SYSBOOT_0	0	0	0	–

3.3.7 JTAG

The JTAG interface is routed to a 20-pin header X11. 10 kΩ PUs for signals TDI, TDO, TMS, TRST#, and SRST#, and 10 kΩ PDs for signals TCK, and RTCK are assembled on the MBa57xx. The JTAG interface is designed for 3.3 V. It has no ESD protection.

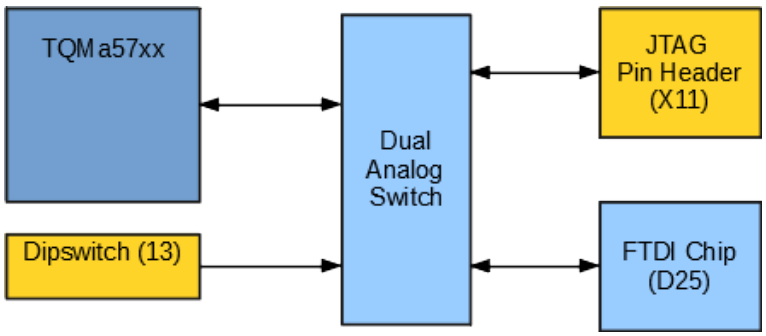

Figure 27: Block diagram JTAG

With DIP switch S13 the interface can be switched between pin header X11 and USB Micro-AB connector X10. Information on this can be found in the MBa57xx schematics.

Table 55: JTAG, DIP switch S13

DIP switch S13	Remark
ON	JTAG on USB Micro-AB connector X10 via FTDI chip
OFF	JTAG signals on header X11

The following table shows the pin assignment of the JTAG connector.

Table 56: Pinout JTAG, X11

Pin	Signal	Dir.	Remark
1	JTAG_VREF	P	100 Ω in series to 3.3 V, use only as reference
2	VCC3V3	P	0 Ω to 3.3 V, I_{max} = 10 mA
3	JTAG_TRST#	I	10 kΩ PU to 3.3 V
4	DGND	P	–
5	JTAG_TDI	I	10 kΩ PU to 3.3 V
6	DGND	P	–
7	JTAG_TMS	I	10 kΩ PU to 3.3 V
8	DGND	P	–
9	JTAG_TCK	I	22 Ω in series, 10 kΩ PD
10	DGND	P	–
11	JTAG_RTCK	P	10 kΩ PD
12	DGND	P	–
13	JTAG_TDO	O	10 kΩ PU to 3.3 V
14	DGND	P	–
15	JTAG_SRST#	I	10 kΩ PU to 3.3 V; open drain buffer at RESET_IN#
16	DGND	P	–
17	VCC3V3	P	10 kΩ to 3.3 V
18	DGND	P	–
19	DGND	P	10 kΩ to DGND
20	DGND	P	–

4. SOFTWARE

The software required for the HSIC hub can, depending on the configuration, be loaded by the TQMa57xx software, see 3.2.1.
Further software is not required for the MBa57xx.

5. MECHANICS

5.1 Dimensions

The MBa57xx has overall dimensions (length × width) of 230 × 170 mm².
The MBa57xx has a maximum height of approximately 26.4 mm.
The MBa57xx has six 3.2 mm holes for mounting in a housing and four 3.2 mm holes for mounting a heat sink.
The MBa57xx weighs approximately 295 grams without TQMa57xx.

To avoid damage due to mechanical stresses, the TQMa57xx may only be removed from the carrier board by using the extraction tool MOZIa57xx. This extraction tool can be purchased separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa57xx for the extraction tool MOZIa57xx.

5.2 Thermal management

For cooling the MBa57xx and the TQMa57xx, up to 8.4 W must be dissipated if no other devices are connected.
Further power dissipation may occur at additionally connected loads, e.g. MBa57xx pin headers, PCIe slot, etc.
The user is responsible for the dissipation of this power in his application.

Attention: Destruction or malfunction, TQMa57xx heat dissipation	
	The AM57xx belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the AM57xx must be taken into consideration when connecting the heat sink, see (10). The AM57xx is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa57xx and thus malfunction, deterioration or destruction.

5.3 Assembly

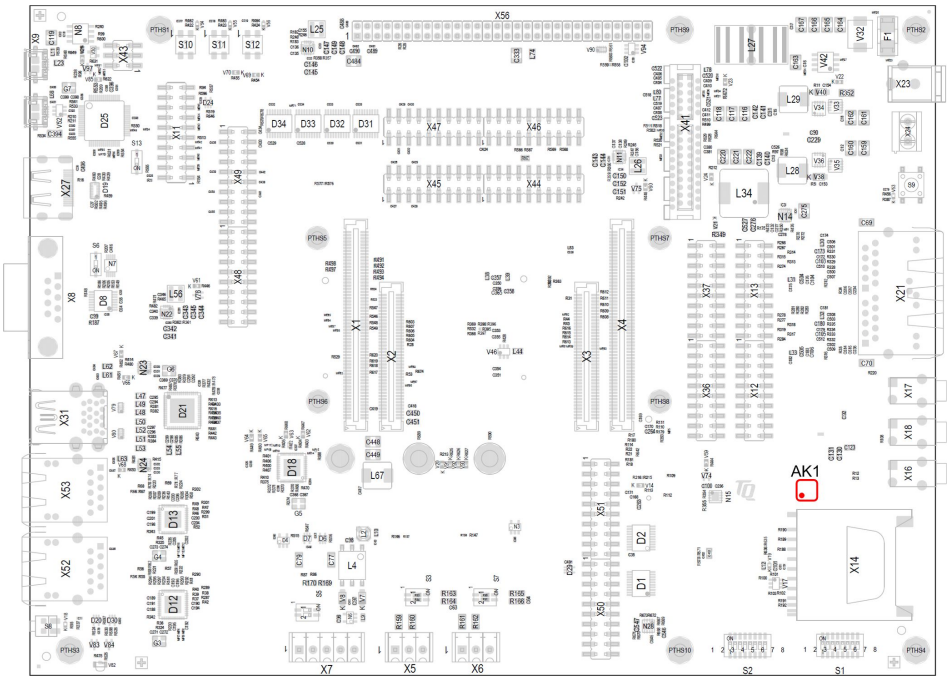

Figure 28: MBa57xx, component placement top

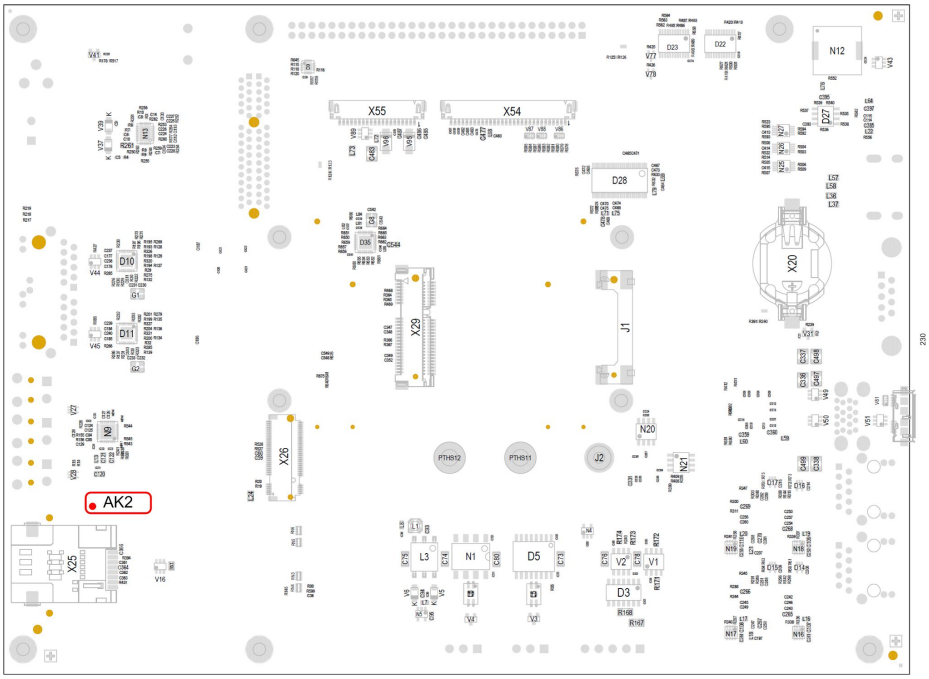

Figure 29: MBa57xx, component placement bottom

The labels on the MBa57xx show the following information:

Table 57: Labels on MBa57xx

Label	Content
AK1	Serial number
AK2	MBa57xx version and revision, tests performed

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

Because the MBa57xx is a development platform, no EMC specific tests have been carried out.

Nevertheless DIN EN 55022:2010 class A was taken into account during development:

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system.

Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.2 ESD

Most of the interfaces on the MBa57xx are protected against electrostatic discharge. [11]
Interfaces providing an ESD protection are to be taken from the MBa57xx schematics.

6.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety have not been carried out.

7. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 58: Climatic and operational conditions MBa57xx (without TQMa57xx)

Parameter	Range	Remark
Permitted environmental temperature	0 °C to +70 °C	Without Lithium battery CR2032
Permitted environmental temperature	0 °C to +60 °C	With Lithium battery CR2032
Permitted storage temperature	–10 °C to +60 °C	With Lithium battery CR2032
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

7.1 Protection against external effects

Protection class IP00 was defined for the MBa57xx. There is no protection against foreign objects, touch or humidity.

7.2 Reliability and service life

No detailed MTBF calculation has been done for the MBa57xx. The MBa57xx is designed to be insensitive to vibration and impact. High quality industrial grade connectors are assembled on the MBa57xx.

11: The JTAG and PMIC interfaces do not provide ESD protection.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The MBa57xx is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBa57xx was designed to be recyclable and easy to repair.

8.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000.
The MBa57xx must therefore always be seen in conjunction with the complete device.
The available standby and sleep modes of the components on the MBa57xx enable compliance with EuP requirements for the MBa57xx.

8.5 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa57xx, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the MBa57xx is minimised by suitable measures. The MBa57xx is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

For technical reasons a battery is necessary for the MBa57xx. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 grams per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBa57xx, it is produced in such a way, that it can be easily repaired and disassembled. The energy consumption of the MBa57xx is minimised by suitable measures. Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls). These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 59: Acronyms

Acronym	Meaning
ADR	Accord européen relatif au transport international des marchandises Dangereuses par Route
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	Camera Serial Interface
DIN	German industry standard (Deutsche Industrienorm)
DIP	Dual In-line Package
DSP	Digital Signal Processor
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multi-Media Card
EN	Europäische Norm (European Standard)
ESD	Electro-Static Discharge
EuP	Energy using Products
FFC	Flat Flex Cable
FR-4	Flame Retardant 4
GP	General Purpose
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HDMI	High Definition Multimedia Interface
HSIC	High-Speed Inter-Chip
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IEEE®	Institute of Electrical and Electronics Engineers
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signal
MII	Media-Independent Interface
MOZI	Module extractor (Modulzieher)
mPCIe	Mini PCIe
MTBF	Mean operating Time Between Failures

9.1 Acronyms and definitions (continued)

Table 59: Acronyms (continued)

Acronym	Meaning
NA	Not Applicable
NC	Not Connected
NOR	Not-Or
NP	Not Placed
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (Interface)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RJ45	Registered Jack 45
RMII	Reduced Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232, RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SAI	Serial Audio Interface
SATA	Serial ATA
SD	Secure Digital
SDHC	Secure Digital High Capacity
SIM	Subscriber Identity Module
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
UART	Universal Asynchronous Receiver and Transmitter
UHS	Ultra High-Speed (Speed Grades I, II, III)
UM	User's Manual
UN	United Nations
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WP	Write-Protection
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

9.2 References

Table 60: Further applicable documents

No.	Document	Rev. / Date	Company
(1)	AM574x Sitara™ Processors Silicon datasheet (Rev. G)	1.0 / 03/2019	TI
(2)	AM574x Sitara™ Processors Technical Reference Manual (Rev. A)	0 / 11/2018	TI
(3)	AM574x Sitara™ Processors Silicon Errata (Rev. B)	0 / 02/2019	TI
(4)	AM572x Sitara™ Processors Silicon datasheet (Rev. F)	2.0 / 03/2019	TI
(5)	AM572x Sitara™ Processors Technical Reference Manual (Rev. K)	0 / 12/2017	TI
(6)	AM572x Sitara™ Processors Silicon Errata (Rev. L)	2.0 / 03/2018	TI
(7)	AM571x Sitara™ Processors Silicon datasheet (Rev. G)	2.0 / 03/2018	TI
(8)	AM571x Sitara™ Processors Technical Reference Manual (Rev. I)	0 / 05/2019	TI
(9)	AM571x Sitara™ Processors Silicon Errata (Rev. E)	2.0 / 03/2018	TI
(10)	TPS659037 User's Guide To Power AM574x, AM572x, AM571x	0 / 03/2018	TI
(11)	USB4604 Data Sheet	1.1 / 06.03.2014	Microchip
(12)	TQMa57xx User's Manual	– current –	TQ-Systems
(13)	TQMa57xx Support-Wiki	– current –	TQ-Systems

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