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in Quality



# **User's Manual**

## **TQMa31**

**TQMa31 UM 100**

**24.01.2010**

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## Revision history

| Rev.: | Date:      | Name:   | Pos.: | Modification:    |
|-------|------------|---------|-------|------------------|
| 100   | 24.01.2010 | Petz MM |       | Document created |

# 1. About this manual

## 1.1 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.


## 1.2 Terms and conventions

| Symbol / Tag               | Meaning   |
|----------------------------|---|
|                            | This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V. |
|                            | This symbol indicates the possible use of voltages greater than 24V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage to / destruction of the component.                    |
|                            | This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.  |
| <b>! note !</b>            | This symbol represents important details or aspects for working with TQ-products.   |
| <b>Filename.ext</b>        | This specification is used to state the complete file name with its corresponding extension.  |
| Instructions /<br>Examples | Examples of an application. e.g.,<br>specifying memory partitions<br>processing a script<br>.....   |
| <b>Reference</b>           | Cross-reference to another section, figure or table.  |


Table 1: Terms and conventions

### 1.3 Handling and ESD tips

#### General handling of your TQ-products

|   |   |
|---|---|
|  | <p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is: not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system was switched off.</p> <p>Violation of this guideline may result in damage / destruction of the module and be dangerous to your health.</p> <p>Improper handling of your TQ-product would render the guarantee invalid.</p> |
|---|---|

#### Proper ESD handling

|  |  |
|--|--|
|  | <p>The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).</p> <p>Always wear antistatic clothing and use ESD-safe tools, packing materials etc. and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.</p> |
|--|--|

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## 1.8 Acronyms and definitions

The following terminology and abbreviations are used:

| Acronym          | Meaning   |
|------------------|---|
| ARM®             | Acorn Risc Machine                                      |
| ATA              | Advanced Technology Attachment                          |
| CAN              | Controller Area Network                                 |
| CF               | Compact Flash   |
| COP/JTAG         | Common On-Chip Processor/Joint Test Action Group        |
| CPU              | Central Processing Unit                                 |
| DDR              | Double Data Rate  |
| EEPROM           | Electrically Erasable Programmable Read-Only Memory     |
| EMC              | Electromagnetic Compatibility                           |
| EMI              | Electromagnetic Interference                            |
| ESD              | Electrostatic Discharge                                 |
| FPGA             | Field Programmable Gate-Array                           |
| fps              | Frames Per Second                                       |
| FR-4             | Flame Retardant-4                                       |
| FS               | Full Speed (USB: 12 Mbit/s)                             |
| GPIO             | General Purpose Input/Output                            |
| GPU              | Graphics Processing Unit                                |
| HS               | High Speed (USB: 480 Mbit/s)                            |
| I/O              | Input/Output  |
| I <sup>2</sup> C | Inter-Integrated Circuit                                |
| IF               | Interface   |
| IP00             | Ingress Protection 00                                   |
| IPU              | Image Processing Unit                                   |
| JTAG             | Joint Test Action Group                                 |
| LAN              | Local Area Network                                      |
| LCD              | Liquid Crystal Display                                  |
| LED              | Light Emitting Diode                                    |
| LS               | Low Speed (USB: 1,5 Mbit/s)                             |
| MII              | Media Independent Interface                             |
| MMC              | Multimedia Card   |
| MOZI             | Module extractor (Modulzieher)                          |
| MPEG             | Motion Pictures Experts Group                           |
| OTG              | On-The-Go   |
| PCB              | Printed Circuit Board                                   |
| PCMCIA           | Personal Computer Memory Card International Association |
| PMIC             | Power Management IC                                     |
| POR              | Power-On Reset  |
| RTC              | Real Time Clock   |
| SDIO             | Secure Digital Input Output                             |
| SDRAM            | Synchronous Dynamic Random Access Memory                |
| SMD              | Surface Mounted Device                                  |
| SMT              | Surface-Mount Technology                                |
| SPI              | Serial Peripheral Interface                             |
| SRAM             | Static RAM  |
| SSI              | Synchronous Serial Interface                            |
| UART             | Universal Asynchronous Receiver/Transmitter             |
| ULPI             | UTMI+ Low Pin Interface                                 |
| USB              | Universal Serial Bus                                    |
| USB-HS           | Universal Serial Bus - High Speed                       |
| USB-OTG          | Universal Serial Bus - On-The-Go                        |
| UTMI             | USB 2.0 Transceiver Macrocell Interface                 |
| VFP              | Vector Floating Point                                   |
| VGA              | Video Graphics Array                                    |
| WEIM             | Wireless External Interface Module                      |

Table 2: Acronyms

## 2. Brief description

The TQMa31 is a universal Minimodule based on the Freescale CPU ARM MCIMX31 (i.MX31). It offers the following key functions:

- Multimedia:
  - MPEG-4 real-time encode of up to VGA @ 30 fps
  - MPEG-4 real-time video post-processing of up to VGA @ 30 fps
  - 3D graphics and other applications acceleration with the ARM® tightly-coupled vector floating point co-processor
  - I2S compliant audio codec
- Mobile NOR flash
- Mobile DDR SDRAM
- USB 2.0 high-speed host interface
- USB full-speed On-The-Go device interface
- Software support possible for
  - Windows CE
  - Linux

All essential pins of the CPU are routed onto the module plug connectors either directly, or via the FPGA. Due to this there are no restrictions with respect to a customised design when using this module.

### 3. Technical data

#### 3.1 Overview

##### 3.1.1 Block diagram TQMa31

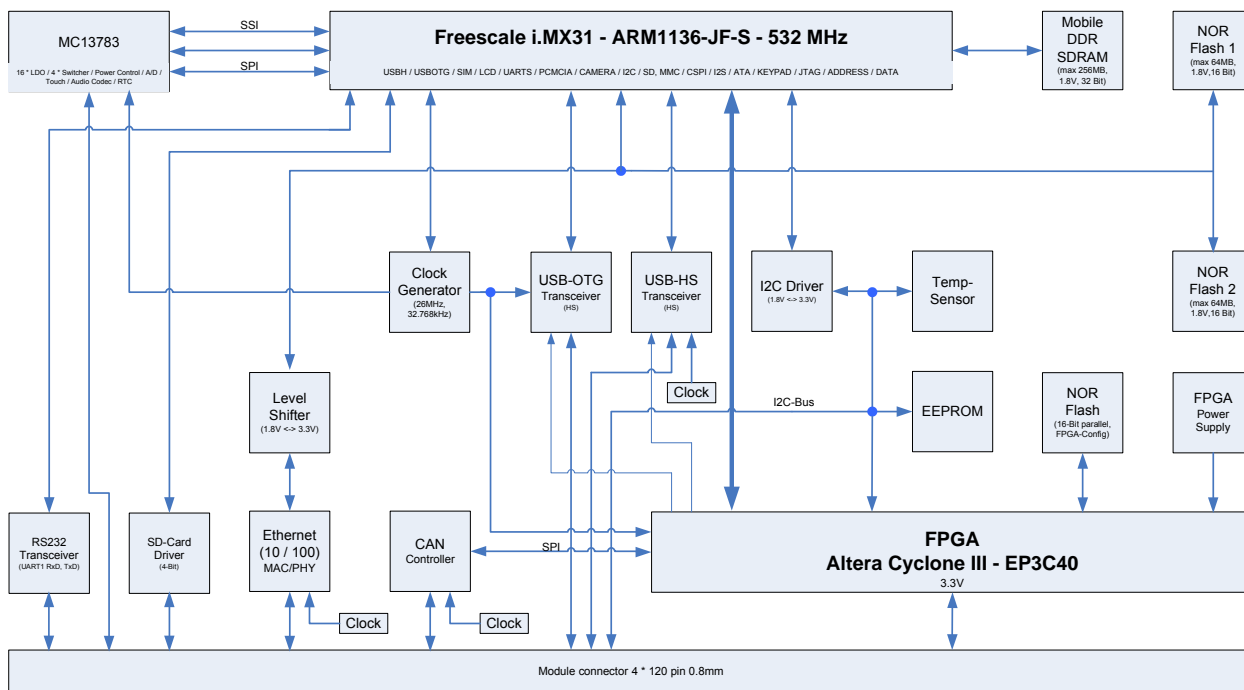


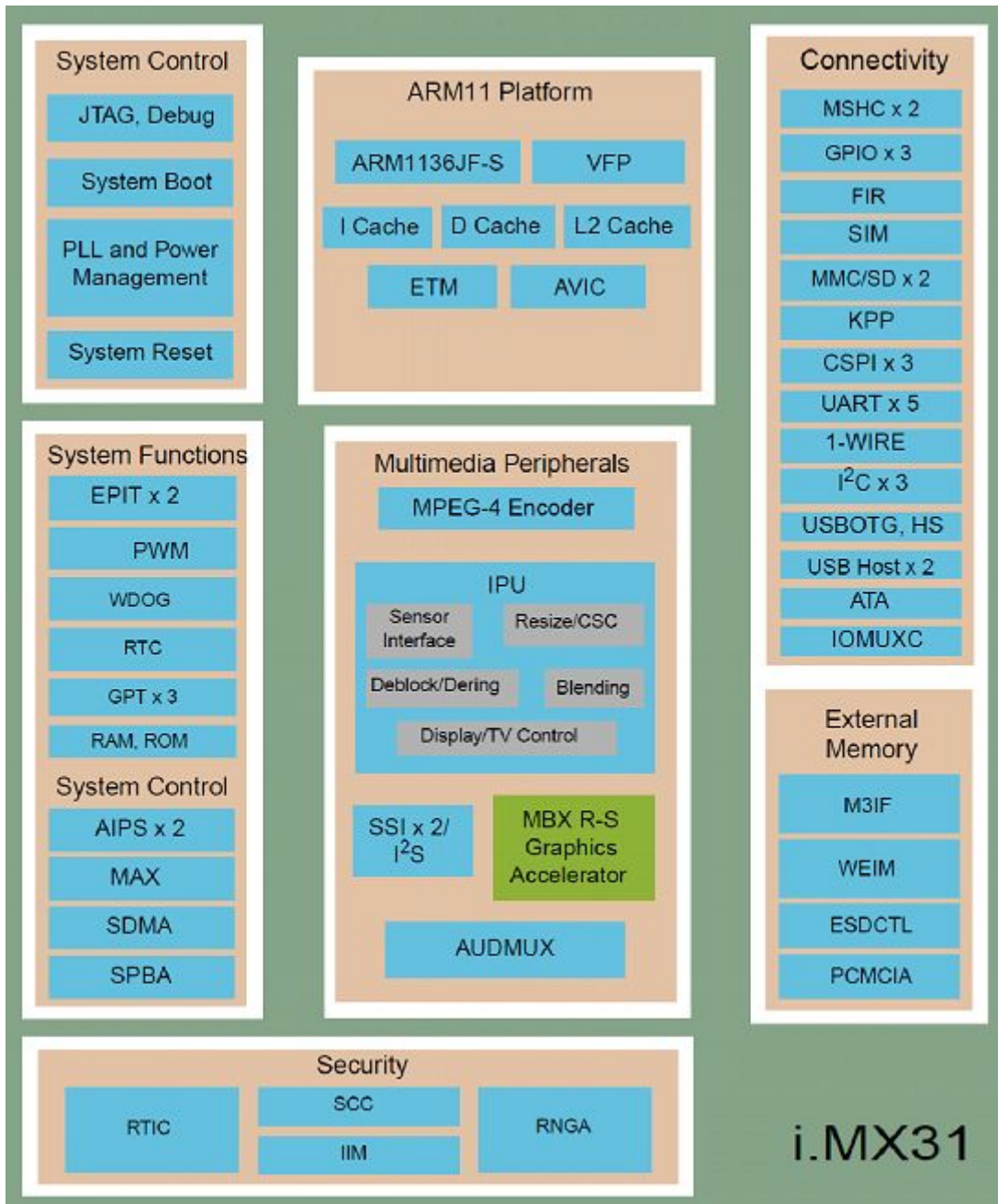
Illustration 1: Block diagram TQMa31

### 3.1.2 System components

- CPU (Freescale MCIMX31, ARM1136JF-S, 532 MHz, FPU, GPU)
- Oscillator for CPU (26 MHz)
- Power manager MC13783 (CPU power supply, audio-in/out, touch controller, analog-in, RTC)
- 32.768 kHz watch quartz for the RTC
- DDR-SDRAM (32 bit, one bank, up to 256 Mbyte)
- NOR flash (16 bit, up to 2 × 64 Mbyte)
- FPGA (Altera Cyclone III EP3C40 or EP3C120)
- FPGA configuration flash (parallel, 8 Mbyte)
- FPGA power supply (1.2 V, 1.8 V, 2.5 V)
- FPGA power supervisor (programmable via I<sup>2</sup>C bus)
- I<sup>2</sup>C repeater
- EEPROM (via I<sup>2</sup>C)
- Temperature sensor (via I<sup>2</sup>C)
- Transceiver for serial interface (RxD, TxD)
- CAN controller (SPI bus)
- 16 MHz oscillator for CAN
- USB-HS transceiver (high-speed)
- USB-OTG transceiver (high-speed)
- LAN controller (MAC/PHY – 10/100 Mbit/s)
- 25 MHz oscillator for LAN controller
- COP/JTAG interface at module plug connector (processor and FPGA)
- Board-To-Board connector system (4 × 120-pin)

### 3.2 Electronics

#### 3.2.1 CPU



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Illustration 2: Block diagram i.MX31

The Freescale i.MX31 (MCIMX31) processor, produced in 90 nm technology, is based on an ARM1136JF-S™ processor core.

**Key functionalities:**

**ARM1136 CPU:**

- I-Cache, D-Cache, L2-Cache
- Jazzelle Java Acceleration
- VFP – Vector Floating Point co-processor
- CPU speed 532 MHz

**EMI – External Memory Interface:**

- SDRAM 16/32 bit, 133 MHz; DDR-SDRAM 16/32 bit, 266 MHz
- NOR flash, SRAM

**Multimedia:**

- MPEG-4 HW encoder
- Graphic accelerator
- IPU – Image Processing Unit
- CMOS/CCD sensor interface
- Resize, colour space conversion
- Display controller

**Connectivity:**

- USB OTG full-speed, Host HS, Host FS
- PCMCIA (CF card)
- ATA (HDD) interface (limitations when used with some other interfaces)
- Audio MUX
- Key pad
- Configurable SPI × 2, SSI/I2S × 2, UART × 5, MMC.SDIO

**Package:**

- Temperature range:            –40 °C to +85 °C, MAPBGA-457, 0.5 mm grid
- Temperature range:            0 °C to +70 °C, MAPBGA-457, 0.5 mm grid

Further functionalities of the CPU shown in the block diagram can be looked up in the Reference Manual (Rev2.3, MCIMX31RM.pdf).

All essential pins of the CPU, except DDR-SDRAM interface, SD-card interface and USB interface (HS/OTG) are routed to the FPGA. The functions available at the module connector, is defined by the FPGA implementation.

| Version       | Frequency | Type                                  | Manufacturer | Remark  |
|---------------|-----------|---------------------------------------|--------------|---|
| MCIMX31CVKN5C | 532 MHz   | MAPBGA 457<br>0.5 mm grid, 14 × 14 mm | Freescale    | -40 °C to +85 °C<br>Silicon Revision 2.0<br>Device Marking M91E |
| MCIMX31VKN5C  | 532 MHz   | MAPBGA 457<br>0.5 mm grid, 14 × 14 mm | Freescale    | 0 °C to +70 °C<br>Silicon Revision 2.0<br>Device Marking M91E   |

The entries are based on the Freescale data sheet “Document Number: MCIMX31 Rev. 3.2, 08/2007”

### 3.2.1.1 CPU reset configuration

The processor has five inputs to configure the boot-mode. These inputs are read after the POR and are saved in the CCM register RCSR.

The signals have pull-up / pull-down resistors which can be assembled according to the boot-mode. The signals cannot be set by the user, due to the fact that the boot-mode depends on the module component placement.

### 3.2.1.2 CPU clock supply

The processor requires two external clock signals which are supplied via the inputs CKIL and CKIH. A 32.768 kHz signal is supplied at the input CKIL which is fed by the PMIC device. A 26 MHz oscillator is connected to the input CKIH.

All further CLK-signals required by the CPU are generated from these clock signals by three CPU-internal PLLs (MCU PLL, Serial PLL and USB PLL).

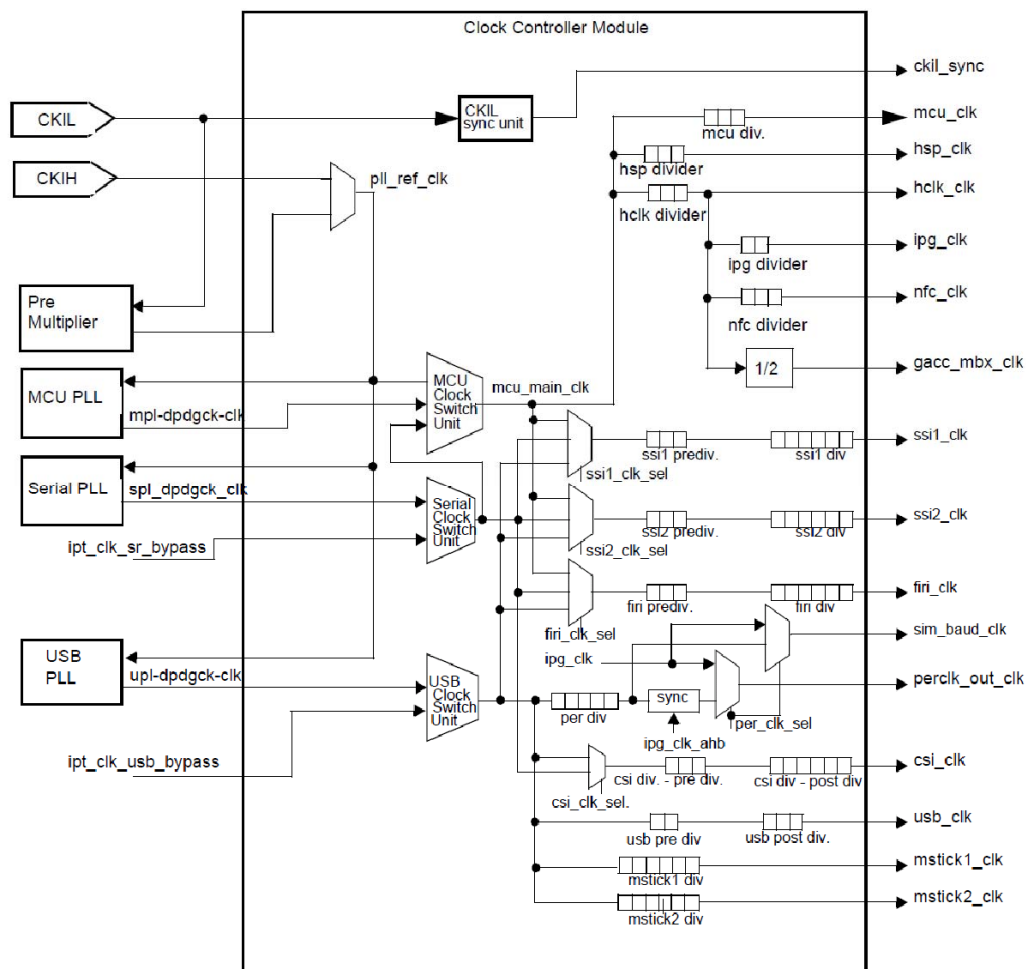


Illustration 3: Processor clock controller module

### 3.2.2 Power management IC

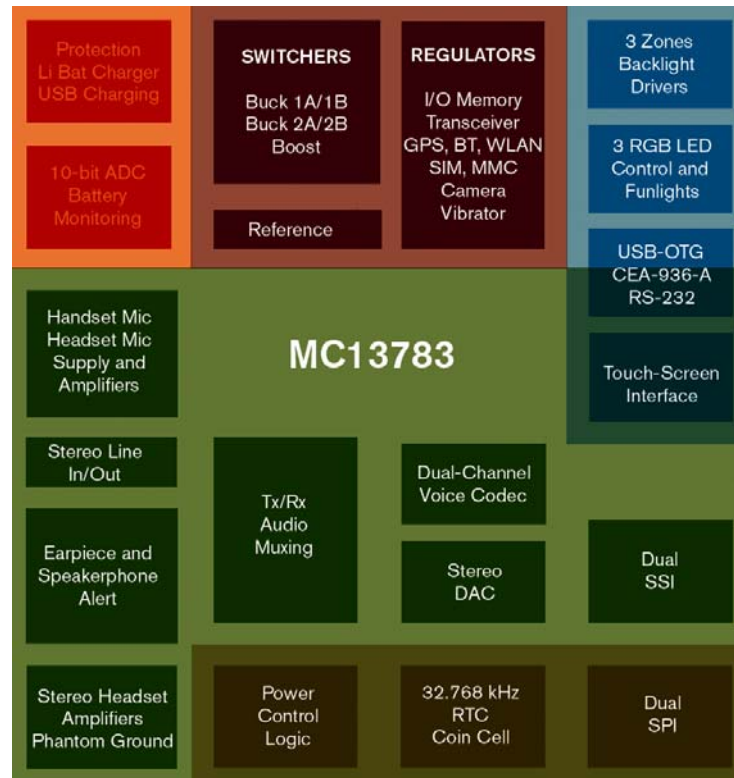


Illustration 4: Block diagram MC13783 (PMIC)

#### **Features:**

- Battery charger interface for wall charging and USB charging
- 10 bit ADC for battery monitoring and other readout functions
- Buck switchers for direct supply of the processor cores
- Boost switcher for backlight and USB on the go supply
- Regulators with internal and external pass devices
- Transmit amplifiers for two handset microphones and a headset microphone
- Amplifiers for earpiece, loudspeaker, headset and line out
- 13 bit voice CODEC with dual ADC channel and both narrow and wide band sampling
- 13 bit stereo recording from an analog input source
- 16 bit stereo DAC supporting multiple sample rates
- Dual SSI audio bus with network mode for connection to multiple devices
- Power control logic with processor interface and event detection
- Real time clock and crystal oscillator circuitry
- Dual SPI control bus with arbitration mechanism
- Multiple backlight drivers and LED control
- USB FS/LS transceiver with OTG and CEA-936-A car kit support ⇒  
(not used, instead of this a separate high speed USB-OTG transceiver is assembled on the module)
- Touch screen interface
- Temperature range  $-30\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- MAPBGA-247, 0.5 mm grid

Further functionalities of the PMIC shown in the block diagram can be looked up in the data sheet "MC13783.pdf Rev. 3.4".

This device is limited in its temperature range to  $-30\text{ }^{\circ}\text{C}$ , and therefore needs a heating source at operating temperatures below  $-30\text{ }^{\circ}\text{C}$ .

### 3.2.2.1 Clock supply

An external watch is used for the integrated real time clock. Furthermore the CLK output of the PMIC is connected to the processor.

The PMIC has a separate supply pin (VLICELL), to buffer the RTC. This pin is routed on the module plug connector.

### 3.2.3 FPGA

For customer- and application-specific extensions an FPGA type Altera Cyclone III (EP3C40 or EP3C120) is provided on the TQMa31. In the Cyclone III FPGA e.g. the following functions can be implemented (repeatedly):

- Ethernet controller
- CAN controller
- Serial interfaces (UART, SPI, I<sup>2</sup>C, ...)
- PWM controller
- Timer, counter
- Sensor-I/O
- Control of A/D or D/A converter
- Digital filter
- Data pre-processing
- Nios II embedded processor
- ...

3.2.3.1 Level adaption by FPGA

The level adaptation of the processor's low I/O levels (1.8 V) to 3.3 V is implemented on the module by the FPGA.

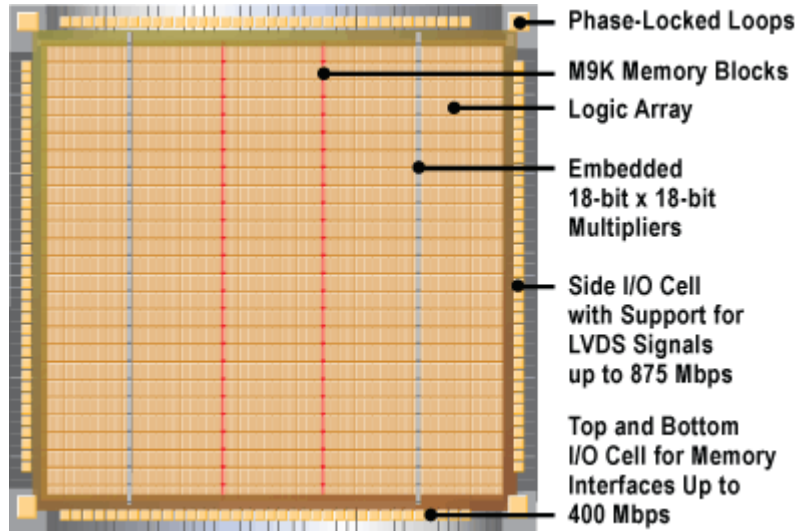


Illustration 5: Cyclone III floor plan

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| Group                 | EP3C40F780 | EP3C120F780 |
|-----------------------|------------|-------------|
| Logic Elements        | 39,600     | 119,088     |
| Memory (Kbit)         | 1,134      | 3,888       |
| Multipliers           | 126        | 288         |
| PLLs                  | 4          | 4           |
| Global Clock Networks | 20         | 20          |

Table 3: Cyclone III Equipment

3.2.3.2 Boot order of FPGA and processor

The FPGA configures itself from a parallel configuration device. The processor is held in reset, until the configuration of the FPGA is finished.

### 3.2.3.3 FPGA configuration

The configuration of the FPGA pins is to be taken from the pinout table. This is described in a separate document.

Interfaces, which are not routed via the FPGA:

- USBOTG IF: Is routed via a separate transceiver
- USB HS2 IF: Is routed via a separate transceiver
- Audio Port 5 IF: Serves for the control of the PMIC
- CSPI2 IF: Serves for the control (configuration etc.) of the PMIC
- SD1 IF: Is routed to the module connector via a special driver
- I<sup>2</sup>C: Is routed to the module connector via a special driver

The following ports are implemented with limitations:

- Serial display IF: Is routed out as a GPIO
- SPI1 IF: Module as master in FPGA configuration
- SIM IF: Is routed out as a GPIO

3.2.3.4 FPGA configuration memory

3.2.3.4.1 Setup of the configuration memory

The FPGA is configured in the "Active Parallel Mode". A parallel memory depending on the selected FPGA is used. The FPGA thereby configures itself independently after the power-up.

A 64 Mbit flash is used as a configuration memory. 10.5 Mbit are required for the configuration of the Altera FPGA (EP3C40). An EP3C120 needs 30.5 Mbit. After the configuration in the normal operation, free ranges in the flash can be used by an FPGA application.

With the choice of the configuration mode, the I/O voltage and the flash device the possibilities displayed in the following table arise for the wiring of the configuration pins of the FPGA.

| Configuration Scheme                        | Configuration Voltage Standard | MSEL3 | MSEL2 | MSEL1 | MSEL0 |
|---|--------------------------------|-------|-------|-------|-------|
| Intel Active Parallel × 16 Fast AP Fast POR | 3.3 V                          | 0     | 1     | 0     | 1     |
| Intel Active Parallel × 16 AP Standard POR  | 3.3 V                          | 0     | 1     | 1     | 1     |

Table 4: FPGA – Power-On configuration

The mode "AP Fast POR" with pull-up / pull-down resistors is set as standard. The mode "Intel Active Parallel × 16 Standard" can optionally be set by a different component placement of the resistors.

- Fast POR time is  $3\text{ ms} < T_{\text{POR}} < 9\text{ ms}$
- Standard POR time is  $50\text{ ms} < T_{\text{POR}} < 200\text{ ms}$

Note:

The time to configure the EP3C40F780I6N from a parallel flash is approximately 22 ms to 33 ms. For the configuration of the bigger derivative (EP3C120F780I8N) approximately 66 ms to 100 ms are required.

3.2.3.4.2 Programming of the configuration memory

With un-configured FPGA the programming of the configuration memory can be done via the JTAG interface (Altera – programming tool, or BST).

3.2.4 Memory-Interface

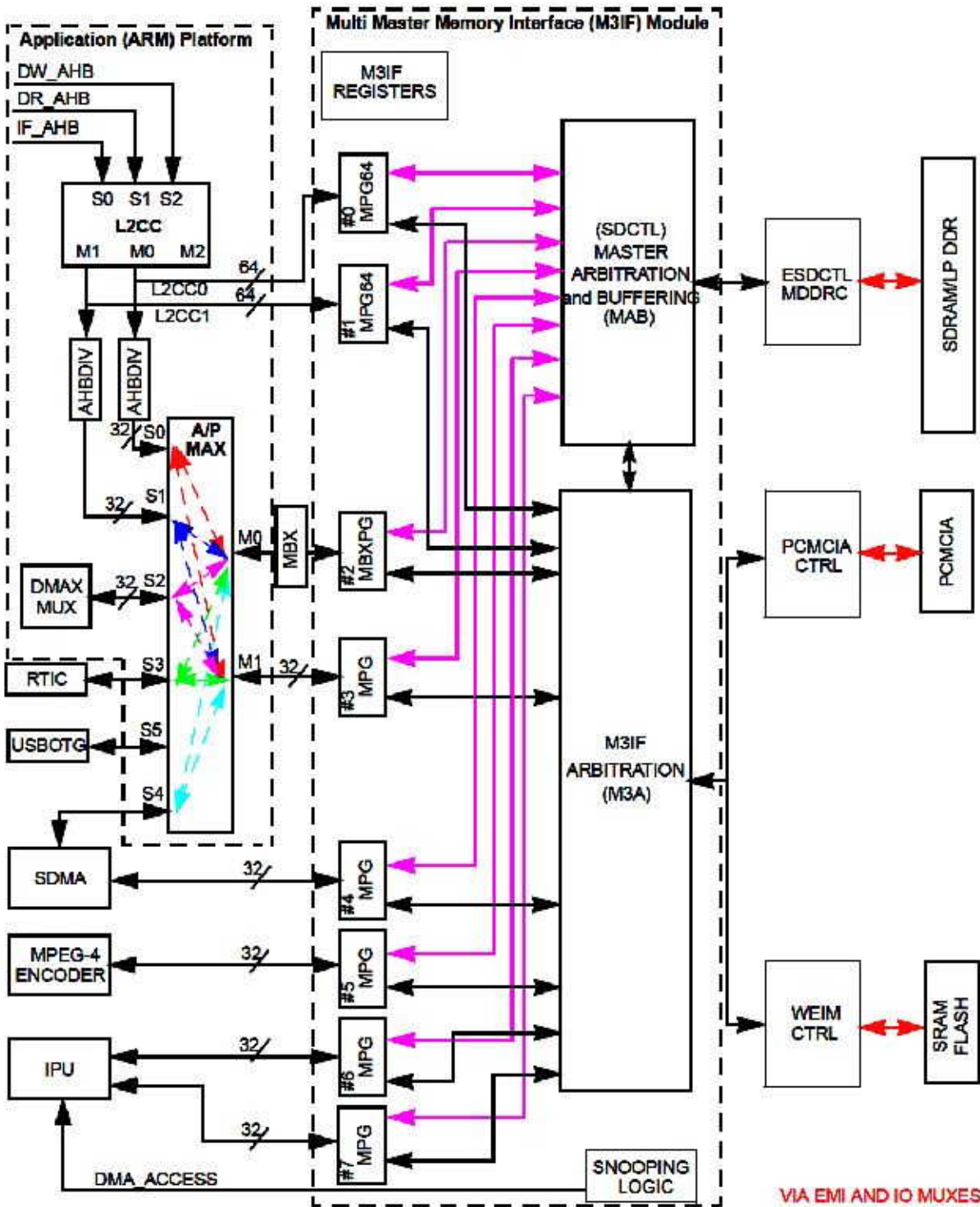


Illustration 6: Block diagram Multi Master Memory Interface (M3IF)

### 3.2.4.1 NOR FLASH

The NOR flash is connected to the external address/data bus of the controller and controlled by the processor via the WEIM (Wireless External Interface Module). For direct control, a version with a supply voltage of 1.8 volt is used. As booting is only possible in the non multiplexed mode, the NOR flash is connected with a width of 16 bit.

- 16 bit data bus
- 26 bit address lines
- Non-multiplexed
- Max. 128 Mbyte via CS0# addressable by the processor
- 1.8 V I/O voltage at the processor interface

A NOR flash memory size of 16 Mbyte up to 128 Mbyte is possible. For the maximum memory size two 512 Mbit devices are used. The chip select signals are generated by linking A25 with CS0#.

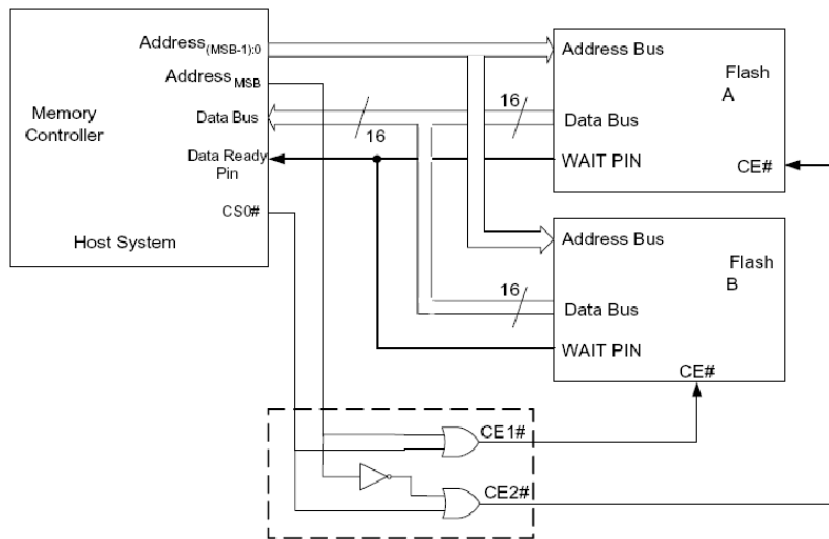


Illustration 7: NOR flash addressing

The connection with the processor is carried out in such a way, that booting from the NOR flash is possible independent of the FPGA.

**Configuration register settings for asynchronous access with 133 MHz:**

Chip Select 0 Upper Control Register (CSCR0U / 0xB800:2000 = 0x0000cc04)

| Name | Description                               | Setting                            |
|------|---|------------------------------------|
| SP   | Supervisor Protect                        | 0                                  |
| WP   | Write Protect                             | 0                                  |
| BCD  | Burst Clock Divisor                       | 0 ⇒ divide AHB by 1                |
| BCS  | Burst Clock Start                         | 0                                  |
| PSZ  | Page Size                                 | 0                                  |
| PME  | Page Mode Emulation                       | 0 ⇒ page mode emulation disable    |
| SYNC | Synchronous Burst Mode Enable             | 0 ⇒ synchronous burst mode disable |
| DOL  | Data Output Length                        | 0                                  |
| CNC  | Chip Select Negation Clock Cycles [0...3] | 3                                  |
| WSC  | Wait State Control                        | 12                                 |
| EW   | ECB/WAIT                                  | 0                                  |
| WWS  | Write Wait State                          | 0                                  |
| EDC  | Extra Dead Cycles                         | 4                                  |

Table 5: Chip Select 0 Upper Control Register CSCR0U

Chip Select 0 Lower Control Register (CSCR0L / 0xB800:2004 = 0xa0332d01)

| Name | Description                             | Setting                        |
|------|---|--------------------------------|
| OEA  | OE Assert                               | 10                             |
| OEN  | OE Negate                               | 0                              |
| EBWA | Enable Byte Write Assert                | 3                              |
| EBWN | Enable Byte Write Negate                | 3                              |
| CSA  | Chip Select Assert                      | 2                              |
| EBC  | Enable Byte Control                     | 1                              |
| DSZ  | Data Port Size                          | 5 ⇒ 16 bit on data [15:0] pins |
| CSN  | Chip Select Negate                      | 0                              |
| PSR  | Pseudo SRAM Enable (Burst Write Enable) | 0                              |
| CRE  | Control Register Enable                 | 0                              |
| WRAP | Wrap Memory Mode                        | 0                              |
| CSEN | Chip Select Enable                      | 1                              |

Table 6: Chip Select 0 Lower Control Register CSCR0L

Chip Select 0 Additional Control Register (CSCR0A / 0xB800:2008 = 0x00320b00)

| Name | Description                       | Setting |
|------|-----------------------------------|---------|
| EBRA | Enable Byte Read Assert           | 0       |
| EBRN | Enable Byte Read Negate           | 0       |
| RWA  | Read/Write Assertion              | 3       |
| RWN  | Read/Write Negation               | 2       |
| MUM  | Muxed Mode                        | 0       |
| LAH  | LBA to Address Hold               | 0       |
| LBN  | LBA Negation                      | 2       |
| LBA  | LBA Assertion                     | 3       |
| DWW  | Decrease Write Wait Stat          | 0       |
| DCT  | DTACK Check Time                  | 0       |
| WWU  | Write Wrap Unmask                 | 0       |
| AGE  | Acknowledge Glue Enable           | 0       |
| CNC2 | Chip Select Negation Clock Cycles | 0       |
| FCE  | Feedback Clock Enable             | 0       |

Table 7: Chip Select 0 Additional Control Register CSCR0A

 The timing considerations are based on the IntelP30 series data sheet (*Revision: 007; 1-May-2006; Order Number: 306666*).

### 3.2.4.2 DDR-SDRAM

The DDR-SDRAM is accessed via the enhanced SDRAM/LPDDR memory controller. A maximum of 256 Mbyte can be addressed in one bank.

- Control via chip select signal CSD0
- Memory sizes of 128 Mbyte and 256 Mbyte
- 32 bit data bus (is implemented as 2 × 16 bit)
- 1.8 V I/O and supply voltage

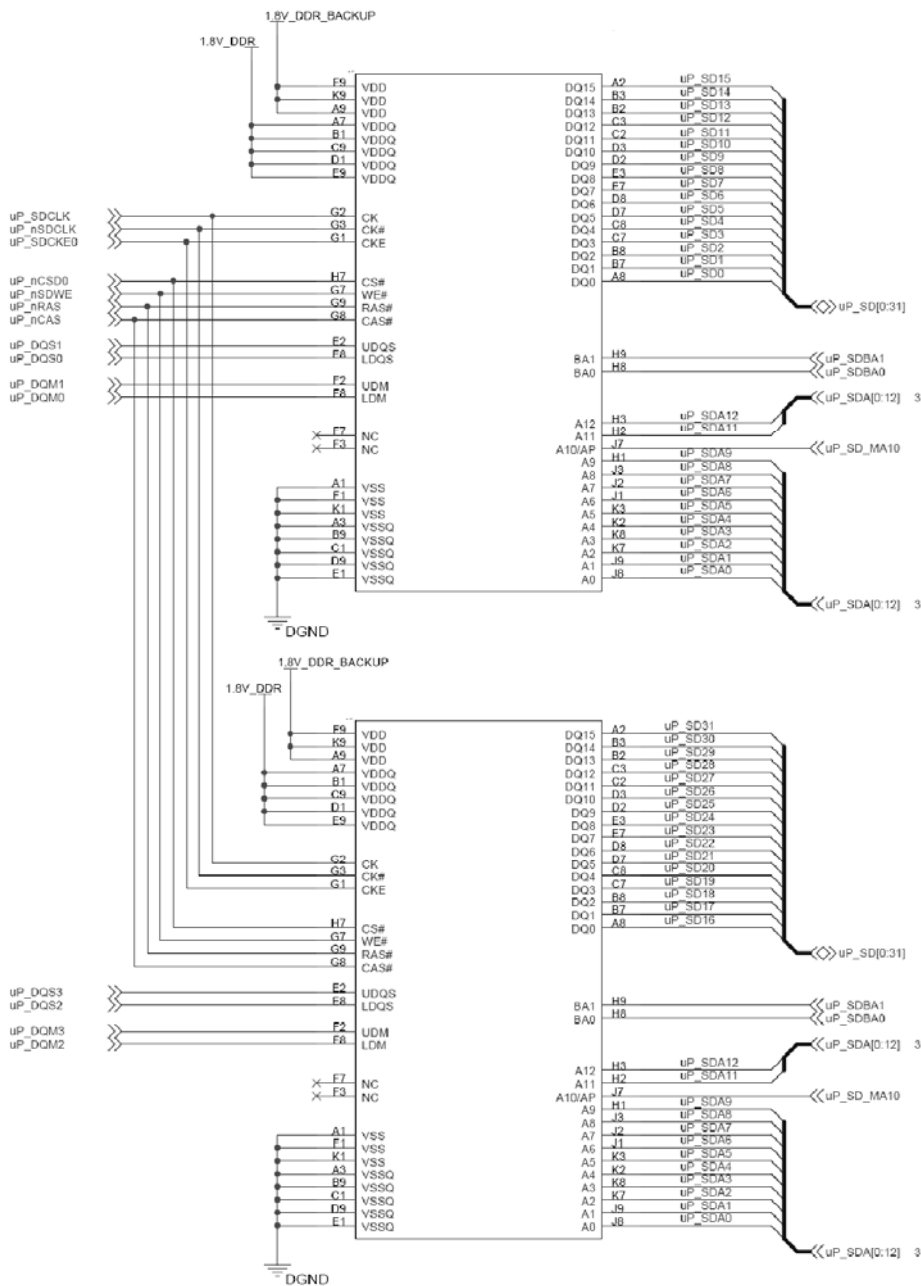


Illustration 8: LPDDR SDRAM – Interface of two 512 Mbit of devices (16 bit)

The timing considerations are based on the data sheet MT46H64M16LF/MT46H32M32LF

(Document:

pdf: 09005aef82846a0b

Source: 09005aef828c2f8f 1Gb\_DDR\_Mobile\_SDRAM\_t48m\_1\_fm - Rev. A 02/07 EN).

The standard mode register of the DDR-SDRAM is programmed with the settings:

- Burst length = 8
- CAS latency = 3

The driver's strength has to be set in the extended mode register:

- Output Driver Strength = Half strength driver

**Register settings in the CPU:**

Enhanced SDRAM control register

(ESDCTL0 / 0xb800:1000 = 0x83228080 for MT46H64M32LF / 256 Mbyte)

(ESDCTL0 / 0xb800:1000 = 0x82226080 for MT46H32M32LF / 128 Mbyte)

| Name  | Description                      | Setting for 133 MHz           |
|-------|----------------------------------|-------------------------------|
| SDE   | Enhanced SDRAM Controller Enable | 1                             |
| SMODE | SDRAM Controller Operating Mode. | 0                             |
| SP    | Supervisor Protect               | 0                             |
| ROW   | Row Address Width                | 3 (256 Mbyte) / 2 (128 Mbyte) |
| COL   | Column Address Width.            | 2                             |
| DSIZ  | SDRAM Memory Data Width          | 2                             |
| SREFR | SDRAM Refresh Rate               | 4 (256 Mbyte) / 3 (128 Mbyte) |
| PWDT  | Power Down Timer                 | 0                             |
| FP    | Full Page                        | 0                             |
| BL    | Burst Length                     | 1                             |
| PRCT  | Precharge Timer                  | 0                             |

Table 8: Enhanced SDRAM Control Register ESDCTL0

Enhanced SDRAM Configuration Register (ESDCFG0 / 0xb800:1004 = 0x006ac73c)

| Name | Description                                       | Setting for 133 MHz                  |
|------|---|--------------------------------------|
| tXP  | LPDDR exit power down to next valid command delay | 3 ⇨ 4 clock delay before new COMMAND |
| tWTR | WRITE to READ Command Delay                       | 0 ⇨ 1 clock                          |
| tRP  | Row precharge delay                               | 2 ⇨ 3 clocks                         |
| tMRD | Load mode register to active command              | 2 ⇨ 3 clocks                         |
| TWR  | WRITE to PRECHARGE Command                        | 1 ⇨ 3 clocks                         |
| TRAS | ACTIVE to PRECHARGE Command                       | 4 ⇨ 5 clocks                         |
| TRRD | ACTIVE Bank A to ACTIVE Bank B Command            | 1 ⇨ 2 clocks active to active        |
| TCAS | CAS Latency                                       | 3 ⇨ clocks SDRAM CAS latency         |
| TRCD | Row to column delay                               | 3 ⇨ 4 clocks row to column delay     |
| TRC  | Row cycle delay                                   | 12 ⇨ 13 clocks                       |

Table 9: Enhanced SDRAM Configuration Register ESDCFG0

Enhanced SDRAM Configuration Register (ESDMISC / 0xb800:1010 = 0x 80000004)

| Name        | Description                           | Value     |
|-------------|---------------------------------------|-----------|
| SDRAMRDY    | External SDRAM/LPDDR Device Status    | Read only |
| LHD         | Latency Hiding Disable                | 0         |
| MDDR_MDIS   | LPDDR Delay Line Measure Disable      | 0         |
| MDDR_DL_RST | LPDDR Delay Line Soft Reset           | 0         |
| MDDREN      | Enable Mobile/Low Power DDR SDRAM     | 1         |
| RST         | Software Initiated Local Module Reset | 0         |

Table 10: Enhanced SDRAM Configuration Register ESDMISC

### 3.2.5 LAN MAC/PHY

The LAN device LAN9218 resp. LAN9215 is connected to the external address/data bus of the controller. It is controlled by the processor via the WEIM (Wireless External Interface Module).

- Signal CS4# is used for selection
- Data bus width is 16 bit
- Corresponds with IEEE802.3/802.3u standard

The design is laid out in such a way, that both devices can be used. With the LAN9218I the upper data word (D16 ... D23) and with the LAN9215I the MII interface is not connected. All other pins of both controllers are allocated identically. The interface of the PHY is routed to the module plug connectors.

The start-up and the qualification of the module were carried out with the LAN9215I-MT. The LAN9218 was not used so far.

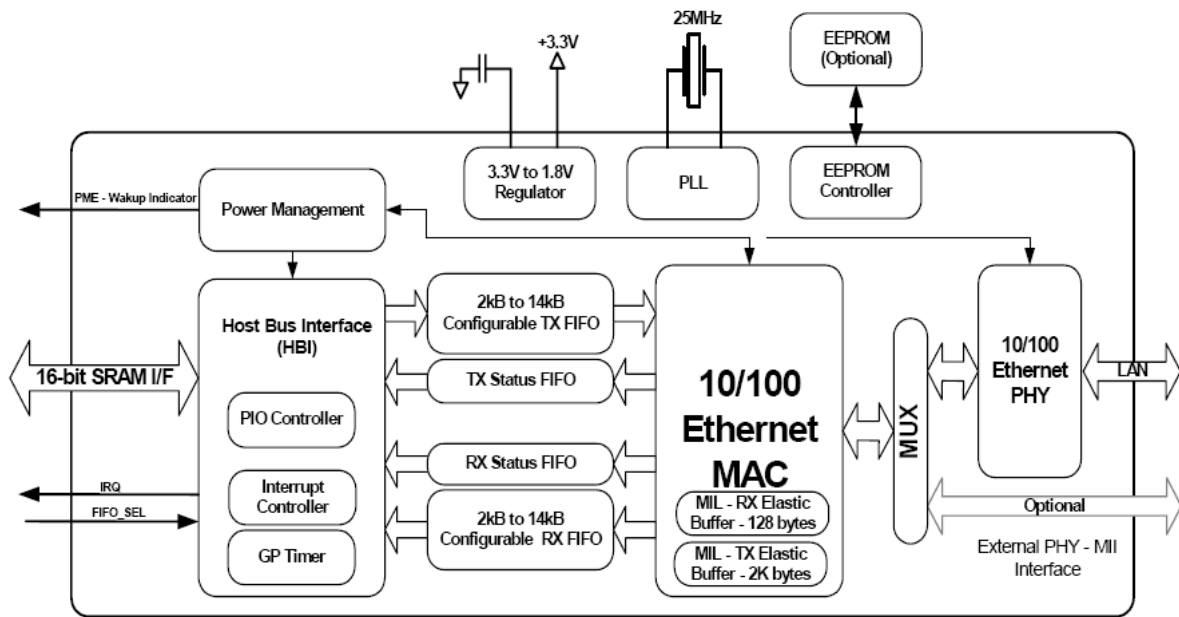


Illustration 9: Block diagram LAN9215I

The LAN controller is supplied with a 25 MHz clock.

**Configuration register settings for asynchronous access with 133 MHz:**

Chip select 4 Upper Control Register (CSCR4U / 0xB800:2040 = 00005604)

| Name | Description                               | Setting |
|------|---|---------|
| SP   | Supervisor Protect                        | 0       |
| WP   | Write Protect                             | 0       |
| BCD  | Burst Clock Divisor                       | 0       |
| BCS  | Burst Clock Start                         | 0       |
| PSZ  | Page Size                                 | 0       |
| PME  | Page Mode Emulation                       | 0       |
| SYNC | Synchronous Burst Mode Enable             | 0       |
| DOL  | Data Output Length                        | 0       |
| CNC  | Chip Select Negation Clock Cycles [0...3] | 1       |
| WSC  | Wait State Control                        | 22      |
| EW   | ECB/WAIT                                  | 0       |
| WWS  | Write Wait State                          | 0       |
| EDC  | Extra Dead Cycles                         | 4       |

Table 11: Chip select 4 Upper Control Register CSCR4U

## Chip Select 4 Lower Control Register (CSCR4L / 0xB800:2044 = 2f0005f1)

| Name | Description                             | Setting                        |
|------|---|--------------------------------|
| OEA  | OE Assert                               | 2                              |
| OEN  | OE Negate                               | 15                             |
| EBWA | Enable Byte Write Assert                | 0                              |
| EBWN | Enable Byte Write Negate                | 0                              |
| CSA  | Chip Select Assert                      | 0                              |
| EBC  | Enable Byte Control                     | 0                              |
| DSZ  | Data Port Size                          | 5 ⇔ 16-bit on Data [15:0] pins |
| CSN  | Chip Select Negate                      | 15                             |
| PSR  | Pseudo SRAM Enable (Burst Write Enable) | 0                              |
| CRE  | Control Register Enable                 | 0                              |
| WRAP | Wrap Memory Mode                        | 0                              |
| CSEN | Chip Select Enable                      | 1                              |

Table 12: Chip Select 4 Lower Control Register CSCR4L

## Chip Select 4 Additional Control Register (CSCR4A / 0xB800:2048 = 000d0000)

| Name  | Description                       | Setting |
|-------|-----------------------------------|---------|
| EBRA  | Enable Byte Read Assert           | 0       |
| EBRN  | Enable Byte Read Negate           | 0       |
| RWA   | Read/Write Assertion              | 0       |
| RWN   | Read/Write Negation               | 13      |
| MUM   | Muxed Mode                        | 0       |
| LAH   | LBA to Address Hold               | 0       |
| LBN   | LBA Negation                      | 0       |
| LBA   | LBA Assertion                     | 0       |
| DWW   | Decrease Write Wait State         | 0       |
| DCT   | DTACK Check Time                  | 0       |
| WWU   | Write Wrap Unmask                 | 0       |
| AGE   | Acknowledge Glue Enable           | 0       |
| CNC2: | Chip Select Negation Clock Cycles | 0       |
| FCE   | Feedback Clock Enable             | 0       |

Table 13: Chip Select 4 Additional Control Register CSCR4A

The timing considerations are based on the SMSC data sheets LAN9215I Rev.1.8 (06-06-07) and SMSC LAN9218I Rev.1.5 (07-18-06).

**3.2.6 EEPROM**

The serial EEPROM can record, e.g., characteristics of the module and customised parameter data. In contrast to flash, single memory cells can be erased and overwritten in the EEPROM. At delivery the EEPROM is empty. It can save, e.g., configuration data non-volatile.

- 64 Kbit
- Control via I<sup>2</sup>C bus of the CPU
- Address lines of the EEPROM on 0b000
- Common use of the I<sup>2</sup>C bus with the temperature sensor

**3.2.7 Temperature sensor**

A temperature sensor (LM75C1MM-3) is provided for indirect supervision of the CPU temperature. To get meaningful temperature values, the sensor is placed directly under the CPU on the bottom side of the module.

- Control via I<sup>2</sup>C bus of the CPU
- Address lines of the temperature sensor on 0b000
- Common use of the I<sup>2</sup>C bus with the EEPROM

The over-temperature-switch output of the LM75 is connected to the FPGA on the module.

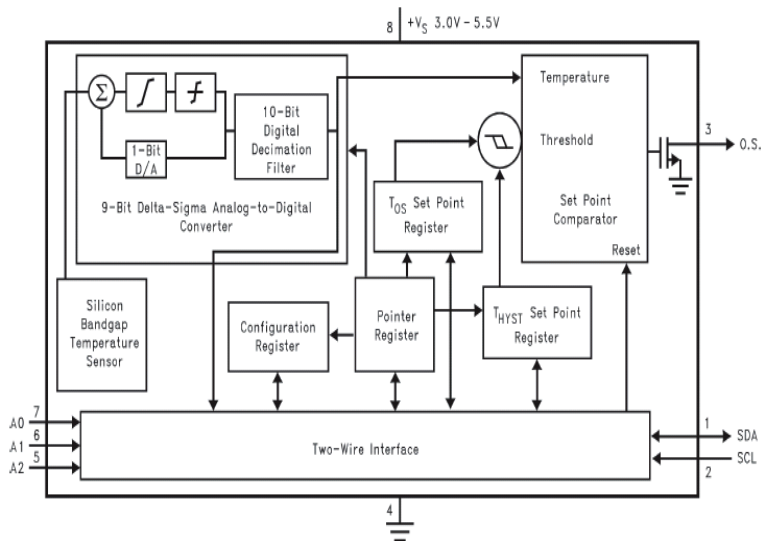


Illustration 10: Block diagram LM75

Device address:

|     |   |   |   |     |    |    |
|-----|---|---|---|-----|----|----|
| 1   | 0 | 0 | 1 | A2  | A1 | A0 |
| MSB |   |   |   | LSB |    |    |

The address consists only of the actual device address, the real access is implemented indirectly via an internal address register. The above mentioned device address doesn't lead to address conflicts with the EEPROM.

### 3.2.8 CAN controller

To extend the interfaces of the i.MX31 a CAN controller type MCP2515 is available, which is connected to the SPI bus (CSPI1). The SPI bus is level-converted by the FPGA. The selection is done via CSPI1\_SS0.

Characteristics:

- Meets CAN 2.0B
- Maximum transfer rate: 1 Mbit/s
- 2 × receive buffer, 2 × 29 bit mask, 6 × 29 bit filter
- 3 × transmit buffer
- 1 × interrupt output

The CAN controller is supplied with a 16 MHz clock.

The CAN interrupt is connected to the processor via the FPGA. The processor's capture pin is used for this.

**Note:**

Another pin can be used for changed or customised FPGA configuration.

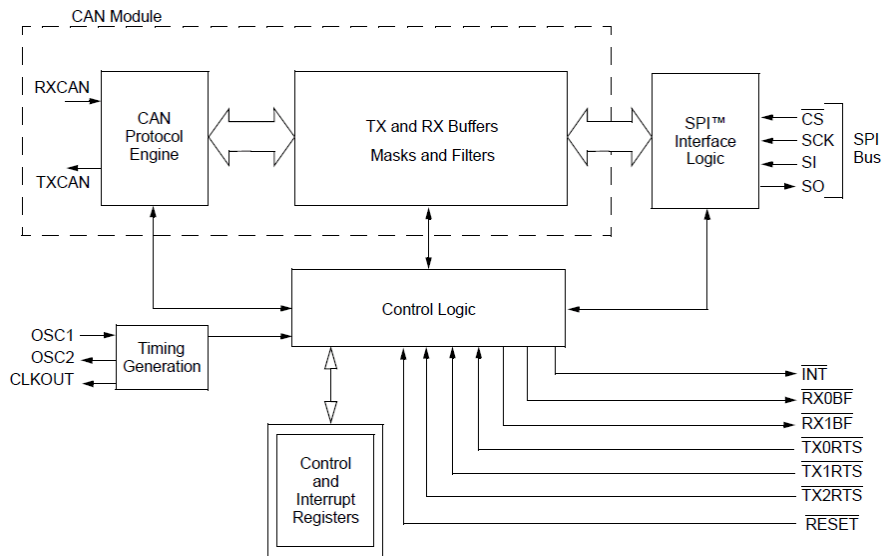


Illustration 11: Block diagram CAN controller

### 3.2.9 RS232 Transceiver

UART1 (RxD1 / A10, TxD1 / F10) of the processor is defined as the primary communication interface and for Linux and WinCE boot messages. To enable the communication during the start-up phase without external hardware, an RS232 transceiver is implemented on the module. To enable the direct communication between transceiver and processor, a device with an I/O voltage range of 1.8 V to 5 V is used.

With this interface merely the signals RxD and TxD of the UART1 are taken into consideration. The other RS232 signals are not routed via the driver. The signals of the interface to the transceiver device are additionally connected to the FPGA. Thus after the start-up phase it is possible to not equip the RS232 driver on the module. In this case the RS232 signals are level shifted by the FPGA (to 3.3 V) and routed to the module connector. A suitable transceiver has to then be provided on the base board.

Furthermore, with the chosen wiring the possibility exists to implement the full interface with all control signals on the base board.

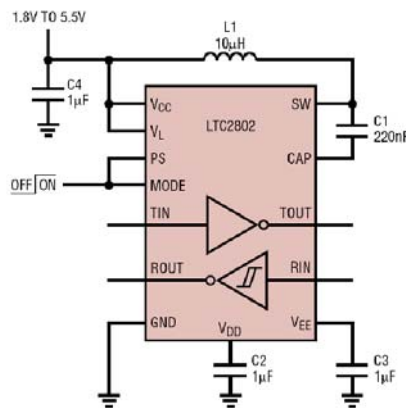


Illustration 12: RS232 transceiver

### 3.2.10 USB OTG / USB HS Transceiver

As the integrated USB OTG Transceiver of the PMIC device cannot be used, a separate device is used on the module. The selected device ISP1504 is compatible to the I/O voltage of the CPU, so that no level converters are needed. The ULP interface is directly connected to the processor. The chip select input of the USB device, which can be selected by the FPGA when required, is pulled low via a 4.7 kΩ resistor.

Characteristics of the device:

- USB2.0 compatible
- ULP interface
- Compatible to the On-The-Go supplement to the USB 2.0 specification Rev. 1.2

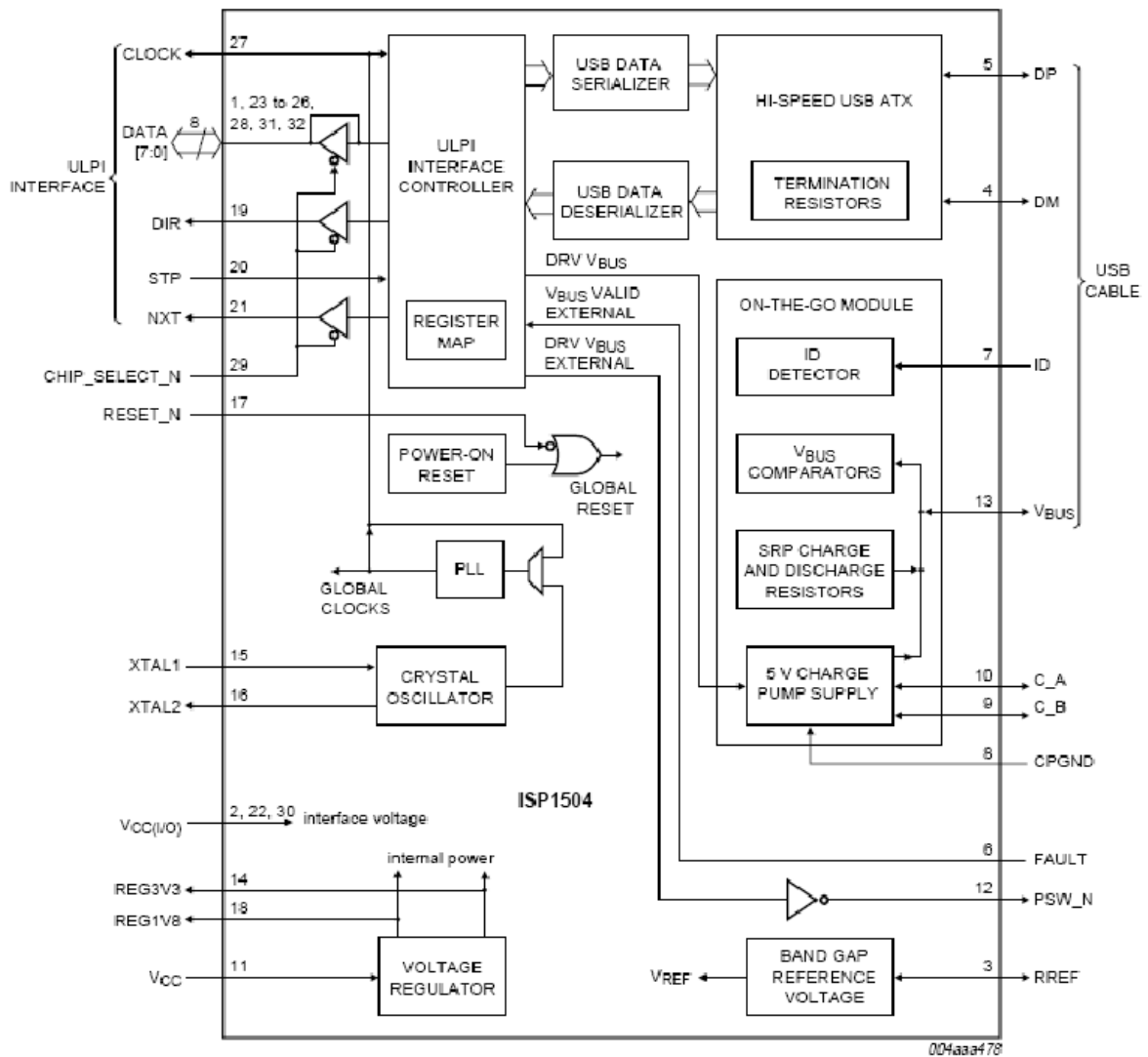


Illustration 13: Block diagram USB transceiver

3.2.11 USB Phy interface

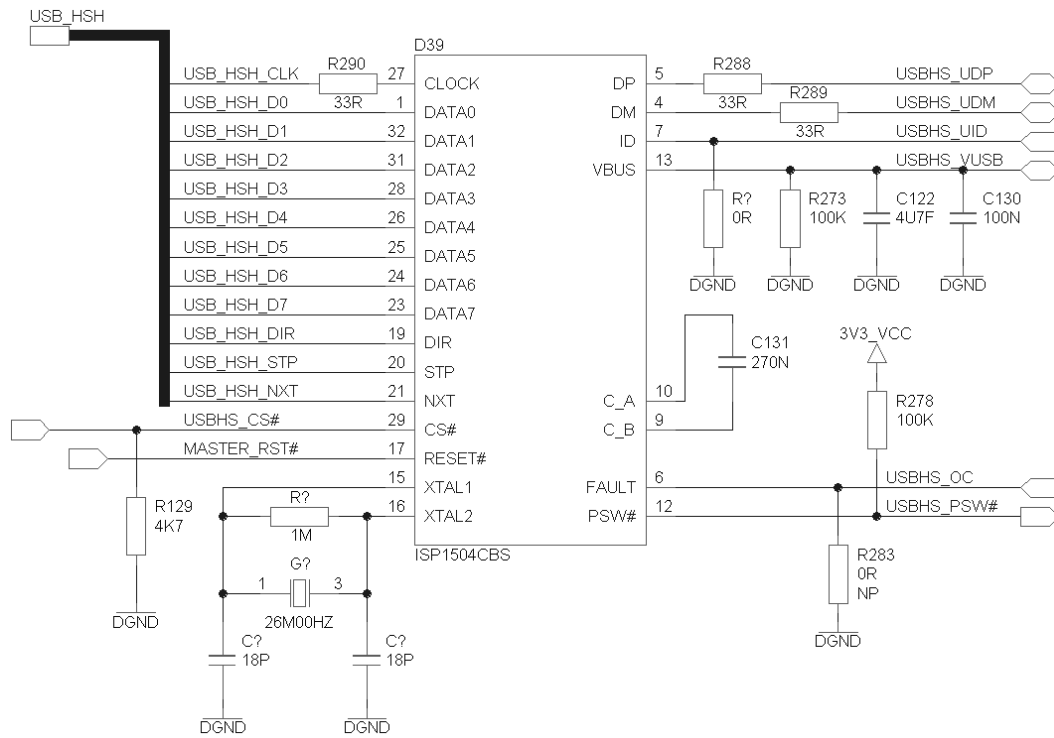


Illustration 14: USB Phy interface

The source signals of the USB transceiver are connected to the module connector.

### 3.2.12 I<sup>2</sup>C Bus

Three components are connected to the I<sup>2</sup>C bus on the module:

- EEPROM
- Temperature sensor
- Supervisor

The level adaptation of the I<sup>2</sup>C bus (I2C\_CLK / J24, I2C\_Dat / H25) of processor (1.8 V) and EEPROM (3.3 V) resp. temperature sensor (3.3 V) is implemented with a bidirectional bus driver.

The I<sup>2</sup>C bus is connected with 3.3 V level to the module plug connector.

| Device             | MSB |   |   |   |        |        |        | LSB |
|--------------------|-----|---|---|---|--------|--------|--------|-----|
| Data EEPROM        | 1   | 0 | 1 | 0 | 0 (A2) | 0 (A1) | 0 (A0) | R/W |
| Temperature sensor | 1   | 0 | 0 | 1 | 0 (A2) | 0 (A1) | 0 (A0) | R/W |
| Supervisor         | 1   | 0 | 0 | 1 | 1 (A2) | 1 (A1) | X      | R/W |

Table 14: I<sup>2</sup>C device addresses

### 3.2.13 Reset-LED

A red hardware-controlled reset-LED is used.

### 3.2.14 Power-Supply

The power supply for CPU, DDR-SDRAM and NOR flash is generated and regulated by the PMIC from the 3.3 V module supply.

### 3.2.15 Supervisor

To monitor the voltages of 2.5 V and 1.2 V generated by the power manager, as well as the 3.3 V supply, a programmable supervision device is present. The corresponding voltages are monitored for undervoltage with this device.

The I<sup>2</sup>C interface of the device is connected to the I<sup>2</sup>C bus of the processor and to the module connector.

### 3.3 Interfaces

In the following table the processor interfaces which can be realised, are listed.

| Function          | i.MX31 interface            | Destination   |
|-------------------|-----------------------------|---|
| UART1             | UART1 + Full UART IF        | Via FPGA to module connector<br>RS232 transceiver ⇔ module connector (TxD, RxD) |
| UART2             | UART2                       | Via FPGA to module connector  |
| UART3             | CSPI3                       | FPGA  |
| UART4             | -                           | Not implemented (used by USB OTG)   |
| UART5             | -                           | Not implemented (used by PCMCIA)  |
| I <sup>2</sup> C  | I2C                         | Module connector via repeater   |
| I <sup>2</sup> C2 | Full UART IF                | Optional, the full UART1 interface is implemented by default                    |
| SPI1              | CSPI1                       | Via FPGA to module connector  |
| SPI2              | CSPI2                       | PMIC (control and configuration of the PMIC)                                    |
| SPI3              | -                           | Not implemented (used by UART3)   |
| USB OTG           | USBOTG + UART1_GPS          | USB OTG transceiver   |
| USBH2             | USBH2 + Audio P3 + Audio P6 | USB HS transceiver  |
| USBH1             | -                           | Not implemented (used by SPI1)  |
| ATA               | -                           | FPGA  |
| CF card           | PCMCIA and data/address bus | Via FPGA to module connector  |
| Keypad            | Keypad                      | Via FPGA to module connector  |
| Audio P3          | -                           | Not implemented (used by USBH2)   |
| Audio P4          | Audio P4                    | PMIC  |
| Audio P5          | Audio P5                    | PMIC  |
| Audio P6          | -                           | Not implemented (used by USBH2)   |
| CSI               | IPU-CSI + ATA               | FPGA  |
| LCD               | IPU-LCD                     | Via FPGA to module connector  |
| SD1               | SD1                         | Via bidirectional driver (level converter) to module connector                  |
| SD2               | PCMCIA                      | Not implemented (used by PCMCIA – CF card)                                      |
| SIM               | SIM                         | FPGA  |

Table 15: Interfaces

As the ATA interface excludes numerous other interfaces, no ATA interface is provided for the standard module configuration.

### 3.4 Module plug connectors

The configuration of the module plug connectors is to be taken from the following pinout tables.

Table 16: Module plug connector 1

| Group              | Function      | Destination / source | Pin No. X1 |     | Destination / source | Function   | Group              |
|--------------------|---------------|----------------------|------------|-----|----------------------|------------|--------------------|
| Power              | GND           | PWR                  | 2          | 1   | PWR                  | 3.3V       | Power              |
| Ethernet (IP-FPGA) | MII_Rx_Er     | D3 / C4              | 4          | 3   | D3 / C5              | MII_CR_S   | Ethernet (IP-FPGA) |
|                    | MII_RxD2      | D3 / C22             | 6          | 5   | D3 / D21             | MII_RxD3   |                    |
|                    | MII_RxD0      | D3 / F19             | 8          | 7   | D3 / E19             | MII_RxD1   |                    |
| Power              | GND           | PWR                  | 10         | 9   | D3 / B14             | MII_Rx_CLK | Ethernet (IP-FPGA) |
| Ethernet (IP-FPGA) | MII_COL       | D3 / D5              | 12         | 11  | D3 / B15             | MII_Tx_CLK |                    |
|                    | MII_Rx_DV     | D3 / D4              | 14         | 13  | PWR                  | 3.3V       |                    |
| Power              | GND           | PWR                  | 16         | 15  | D3 / D20             | MII_MDIO   | Ethernet (IP-FPGA) |
| Ethernet (IP-FPGA) | MII_MDC       | D3 / C19             | 18         | 17  | D3 / E18             | MII_TX_ER  |                    |
|                    | MII_TxD3      | D3 / B21             | 20         | 19  | D3 / A21             | MII_TxD2   |                    |
| Power              | GND           | PWR                  | 22         | 21  | D3 / D19             | MII_TxD0   | Ethernet (IP-FPGA) |
| Ethernet (IP-FPGA) | MII_TxD1      | D3 / A22             | 24         | 23  | D3 / C3              | MII_INT    |                    |
|                    | MII_Tx_EN     | D3 / C20             | 26         | 25  | PWR                  | 3.3V       |                    |
| Power              | GND           | PWR                  | 28         | 27  | PWR                  | 3.3V       | Ethernet           |
| Reserve            | NC            |                      | 28         | 27  | D12 / 78             | ETH_TDN    |                    |
|                    | NC            |                      | 30         | 29  | D12 / 79             | ETH_TDP    |                    |
| Ethernet           | ETH_LINK_ACK# | D12 / 99             | 32         | 31  | D12 / 100            | ETH_FDPLX# | Ethernet           |
| Power              | GND           | PWR                  | 34         | 33  | D12 / 98             | ETH_SPEED# |                    |
| Ethernet           | ETH_RDN       | D12 / 82             | 36         | 35  |                      | NC         |                    |
| Power              | GND           | PWR                  | 38         | 37  | PWR                  | 3.3V       | Reserve            |
| Ethernet           | ETH_RDP       | D12 / 83             | 40         | 39  | D3 / J26             | Data_15    |                    |
| Power              | GND           | PWR                  | 42         | 41  | D3 / K22             | Data_13    | Data-Bus (FPGA)    |
| Data-Bus (FPGA)    | Data_14       | D3 / L23             | 44         | 43  | D3 / M27             | Data_11    |                    |
|                    | Data_12       | D3 / M26             | 46         | 45  | D3 / M28             | Data_9     |                    |
|                    | Data_10       | D3 / M23             | 48         | 47  | D3 / N26             | Data_7     |                    |
| Power              | GND           | PWR                  | 50         | 49  | PWR                  | 3.3V       | Data-Bus (FPGA)    |
| Data-Bus (FPGA)    | Data_8        | D3 / L22             | 52         | 51  | D3 / N25             | Data_5     |                    |
|                    | Data_6        | D3 / G24             | 54         | 53  | D3 / L25             | Data_3     |                    |
|                    | Data_4        | D3 / D26             | 56         | 55  | D3 / M24             | Data_1     |                    |
| Power              | GND           | PWR                  | 58         | 57  | D3 / K25             | Data_0     | ADDR_BUS (FPGA)    |
| ADDR_BUS (FPGA)    | ADDR_24       | D3 / F17             | 60         | 59  | D3 / E26             | ADDR_25    |                    |
|                    | ADDR_22       | D3 / F26             | 62         | 61  | PWR                  | 3.3V       |                    |
| Power              | GND           | PWR                  | 64         | 63  | D3 / F25             | ADDR_23    | ADDR_BUS (FPGA)    |
| ADDR_BUS (FPGA)    | ADDR_20       | D3 / G23             | 66         | 65  | D3 / E27             | ADDR_21    |                    |
|                    | ADDR_18       | D3 / K26             | 68         | 67  | D3 / G26             | ADDR_19    |                    |
|                    | ADDR_16       | D3 / H15             | 70         | 69  | D3 / G25             | ADDR_17    |                    |
| Power              | GND           | PWR                  | 72         | 71  | D3 / H24             | ADDR_15    | ADDR_BUS (FPGA)    |
| ADDR_BUS (FPGA)    | ADDR_14       | D3 / H22             | 74         | 73  | PWR                  | 3.3V       |                    |
|                    | ADDR_12       | D3 / H23             | 76         | 75  | D3 / J25             | ADDR_13    |                    |
|                    | ADDR_10       | D3 / J24             | 78         | 77  | D3 / L26             | ADDR_11    |                    |
| Power              | GND           | PWR                  | 80         | 79  | D3 / K27             | ADDR_9     | ADDR_BUS (FPGA)    |
| ADDR_BUS (FPGA)    | ADDR_8        | D3 / F24             | 82         | 81  | D3 / K28             | ADDR_7     |                    |
|                    | ADDR_6        | D3 / L24             | 84         | 83  | D3 / L27             | ADDR_5     |                    |
| Power              | GND           | PWR                  | 86         | 85  | PWR                  | 3.3V       | ADDR_BUS (FPGA)    |
| ADDR_BUS (FPGA)    | ADDR_4        | D3 / L28             | 88         | 87  | D3 / J23             | ADDR_3     |                    |
|                    | ADDR_2        | D3 / G18             | 90         | 89  | D3 / K21             | ADDR_1     |                    |
| Power              | GND           | PWR                  | 92         | 91  | D3 / D22             | RW#        | Bus-Ctrl (FPGA)    |
| ADDR_B (FPGA)      | ADDR_0        | D3 / H25             | 94         | 93  | D3 / A26             | LBA#       |                    |
| Bus-Ctrl (FPGA)    | ECB           | D3 / J19             | 96         | 95  | D3 / G21             | EB1#       | Bus-Ctrl (FPGA)    |
| Power              | GND           | PWR                  | 98         | 97  | PWR                  | 3.3V       |                    |
| Bus-Ctrl (FPGA)    | BCLK#         | D3 / E15             | 100        | 99  | D3 / B26             | EB0#       | Bus-Ctrl (FPGA)    |
| Bus-Ctrl (FPGA)    | WAIT#         | D3 / C21             | 102        | 101 | D3 / A4              | CS4#       |                    |
| Power              | GND           | PWR                  | 104        | 103 | D3 / A3              | CS1#       | CS# (FPGA)         |
| CS# (FPGA)         | CS5#          | D3 / L4              | 106        | 105 | D3 / L5              | GPIO1_0    |                    |
| Power              | GND           | PWR                  | 108        | 107 | D3 / F18             | GPIO3_0    | GPIO (FPGA)        |
| CS# (FPGA)         | CS3#          | D3 / M7              | 110        | 109 | PWR                  | 3.3V       |                    |
| GPIO (FPGA)        | GPIO1_6       | D3 / G17             | 112        | 111 | D3 / F22             | GPIO1_4    | GPIO (FPGA)        |
| Timer (FPGA)       | PWM           | D3 / N3              | 114        | 113 | D3 / N4              | COMPARE    |                    |
| Power              | GND           | PWR                  | 116        | 115 | D3 / M1              | CLK-OUT    | Timer (FPGA)       |
| Timer (FPGA)       | CAPTURE       | D3 / K1              | 118        | 117 |                      | NC         |                    |
| Reserve (FPGA)     | Reserve       | D3 / H17             | 120        | 119 | PWR                  | 3.3V       | Reserve            |
| Power              | GND           | PWR                  |            |     |                      |            |                    |

**Table 17: Module plug connector 2**

| Group          | Function         | Destination / source | Pin No. X2 |     | Destination / source | Function       | Group          |
|----------------|------------------|----------------------|------------|-----|----------------------|----------------|----------------|
| Power          | GND              | PWR                  | 2          | 1   | PWR                  | 3.3V           | Power          |
| PCMCIA (FPGA)  | SDBA0            | D3 / P2              | 4          | 3   | D3 / P1              | SDBA1          | PCMCIA (FPGA)  |
|                | PC_CD2#          | D3 / B25             | 6          | 5   | D3 / G20             | PC_CD1#        |                |
|                | PC_READY         | D3 / A26             | 8          | 7   | D3 / G19             | PC_WAIT#       |                |
| Power          | GND              | PWR                  | 10         | 9   | D3 / F21             | PC_PWRON       | Power          |
| PCMCIA (FPGA)  | PC_VS1           | D3 / C25             | 12         | 11  | D3 / E21             | PC_VS2         |                |
|                | PC_BVD1          | D3 / A23             | 14         | 13  | PWR                  | 3.3V           |                |
|                | PC_RST           | D3 / B23             | 16         | 15  | D3 / H19             | PC_BVD2        | PCMCIA (FPGA)  |
| Power          | GND              | PWR                  | 18         | 17  | D3 / C23             | IOIS16         |                |
| PCMCIA (FPGA)  | PC_OE            | D3 / E22             | 20         | 19  | D3 / D23             | PC_RW#         | Reserve        |
|                | NC               |                      | 22         | 21  |                      | NC             |                |
|                | NC               |                      | 24         | 23  |                      | NC             | Power          |
| Power          | GND              | PWR                  | 26         | 25  | PWR                  | 3.3V           |                |
| Key Pad (FPGA) | KEY_ROW5         | D3 / G14             | 28         | 27  | D3 / N21             | KEY_ROW4       | Key Pad (FPGA) |
|                | KEY_ROW7         | D3 / G9              | 30         | 29  | D3 / F11             | KEY_ROW6       |                |
| Reserve        | NC               |                      | 32         | 31  |                      | NC             | Reserve        |
| Power          | GND              | PWR                  | 34         | 33  |                      | NC             |                |
| Key Pad (FPGA) | KEY_COL4         | D3 / P25             | 36         | 35  |                      | NC             | Power          |
|                | KEY_COL5         | D3 / C6              | 38         | 37  | PWR                  | 3.3V           |                |
|                | KEY_COL7         | D3 / H8              | 40         | 39  | D3 / P27             | KEY_COL6       |                |
| Power          | GND              | PWR                  | 42         | 41  | D3 / D3              | Reserve (FPGA) | Reserve (FPGA) |
| Reserve (FPGA) | Reserve (FPGA)   | D3 / D2              | 44         | 43  | D3 / C2              | Reserve (FPGA) |                |
|                | Reserve (FPGA)   | D3 / M2              | 46         | 45  | D3 / D1              | Reserve (FPGA) |                |
|                | Reserve (FPGA)   | D3 / H4              | 48         | 47  | D3 / G5              | Reserve (FPGA) | Power          |
| Power          | GND              | PWR                  | 50         | 49  | PWR                  | 3.3V           |                |
| Reserve (FPGA) | Reserve (FPGA)   | D3 / J5              | 52         | 51  | D3 / H3              | Reserve (FPGA) | Reserve (FPGA) |
|                | Reserve (FPGA)   | D3 / F3              | 54         | 53  | D3 / E3              | Reserve (FPGA) |                |
| CSPI1 (FPGA)   | CSPI1_SPI_RDY    | D3 / J17             | 56         | 55  | D3 / F5              | Reserve (FPGA) | Reserve        |
| Power          | GND              | PWR                  | 58         | 57  |                      | NC             |                |
| CSPI1 (FPGA)   | CSPI1_MISO       | D3 / J16             | 60         | 59  |                      | NC             | Power          |
|                | CSPI1_SCLK       | D3 / F15             | 62         | 61  | PWR                  | 3.3V           |                |
|                | CSPI1_CS0        | D3 / G16             | 64         | 63  | D3 / E17             | CSPI1_MOSI     |                |
| Power          | GND              | PWR                  | 66         | 65  | D3 / H16             | CSPI1_CS1      | CSPI1 (FPGA)   |
| UART3 (FPGA)   | UART3_RX         | D3 / G4              | 68         | 67  | D3 / P28             | CSPI1_CS2      |                |
|                | UART3_RTS        | D3 / J6              | 70         | 69  | D3 / G3              | UART3_TX       | UART3 (FPGA)   |
| UART2 (FPGA)   | UART2_RX         | D3 / L3              | 72         | 71  | D3 / E1              | UART3_CTS      |                |
| Power          | GND              | PWR                  | 74         | 73  | PWR                  | 3.3V           | Power          |
| UART2 (FPGA)   | UART2_RTS        | D3 / H5              | 76         | 75  | D3 / J4              | UART2_TX       |                |
| UART1 (FPGA)   | UART1_RX         | D3 / J7              | 78         | 77  | D3 / H6              | UART2_CTS      | UART2 (FPGA)   |
|                | UART1_RTS        | D3 / F1              | 80         | 79  | D3 / F2              | UART1_TX       |                |
| Power          | GND              | PWR                  | 82         | 81  | D3 / K4              | UART1_CTS      | UART1 (FPGA)   |
| UART1 (FPGA)   | UART1_DTR        | D3 / K7              | 84         | 83  | D3 / K3              | UART1_DSR      |                |
|                | UART1_RI         | D3 / L6              | 86         | 85  | PWR                  | 3.3V           | Power          |
| Reserve (FPGA) | Reserve (FPGA)   | D3 / L7              | 88         | 87  | D3 / L8              | UART1_DCD      |                |
| Power          | GND              | PWR                  | 90         | 89  | D3 / M8              | Reserve (FPGA) | Reserve (FPGA) |
| USB (FPGA)     | USB_BYN          | D3 / M3              | 92         | 91  | D3 / N8              | USB_PWR        |                |
| Reserve        | NC               |                      | 94         | 93  | D3 / G1              | USB_OC         | USB (FPGA)     |
|                | NC               |                      | 96         | 95  |                      | NC             |                |
| Power          | GND              | PWR                  | 98         | 97  | PWR                  | 3.3V           | Power          |
| USB_HS         | USBHS_UID        | D39 / 7              | 100        | 99  | D39 / 5              | USBHS_UDP      |                |
|                | USBHS_VUSB       | D39 / 13             | 102        | 101 | D39 / 4              | USBHS_UDM      |                |
|                | USBHS_PSW#       | D39 / 12             | 104        | 103 | D39 / 6              | USBHS_OC       |                |
| Power          | GND              | PWR                  | 106        | 105 |                      | NC             | Reserve        |
| Reserve        | NC               |                      | 108        | 107 |                      | NC             |                |
|                | NC               |                      | 110        | 109 | PWR                  | 3.3V           |                |
|                | NC               |                      | 112        | 111 |                      | NC             |                |
| Power          | GND              | PWR                  | 114        | 113 |                      | NC             | Reserve        |
| Reserve        | NC               |                      | 116        | 115 |                      | NC             |                |
| Flash          | FLASH_Reset_3V3# | D7 / D4+<br>D6 / D4  | 118        | 117 | D7 / C6+<br>D6 / C6  | WP# / ACC      | Flash          |
| Power          | GND              | PWR                  | 120        | 119 | PWR                  | 3.3V           | Power          |

Table 18: Module plug connector 3

| Group                         | Function | Destination / source | Pin No. X3 |     | Destination / source | Function       | Group                         |
|-------------------------------|----------|----------------------|------------|-----|----------------------|----------------|-------------------------------|
| Power                         | GND      | PWR                  | 2          | 1   | PWR                  | 3.3V           | Power                         |
| IPU-LCD (FPGA)                | LD1      | D3 / D13             | 4          | 3   | D3 / C13             | LD0            | IPU-LCD (FPGA)                |
|                               | LD3      | D3 / A12             | 6          | 5   | D3 / C14             | LD2            |                               |
|                               | LD5      | D3 / E10             | 8          | 7   | D3 / B12             | LD4            |                               |
| Power                         | GND      | PWR                  | 10         | 9   | D3 / F14             | LD6            | IPU-LCD (FPGA)                |
| IPU-LCD (FPGA)                | LD8      | D3 / H12             | 12         | 11  | D3 / E14             | LD7            |                               |
| Power                         | GND      | PWR                  | 14         | 13  | PWR                  | 3.3V           | Power                         |
| IPU-LCD (FPGA)                | LD9      | D3 / J12             | 14         | 13  | D3 / B8              | LD10           | IPU-LCD (FPGA)                |
| Power                         | GND      | PWR                  | 18         | 17  | D3 / D11             | LD12           |                               |
| IPU-LCD (FPGA)                | LD14     | D3 / D10             | 20         | 19  | D3 / E7              | LD13           |                               |
| Power                         | GND      | PWR                  | 22         | 21  | D3 / F10             | LD15           | IPU-LCD (FPGA)                |
| IPU-LCD (FPGA)                | LD16     | D3 / E11             | 22         | 21  | D3 / F10             | LD15           |                               |
| Power                         | GND      | PWR                  | 24         | 23  | D3 / E8              | LD17           | IPU-LCD (FPGA)                |
| IPU-LCD (FPGA)                | SD_D_IO  | D3 / M25             | 24         | 23  | D3 / E8              | LD17           |                               |
| Power                         | GND      | PWR                  | 26         | 25  | PWR                  | 3.3V           |                               |
| IPU-LCD (FPGA)                | SD_D_CLK | D3 / J22             | 28         | 27  | D3 / M25             | SD_D_I         | IPU-LCD (FPGA)                |
| IPU-LCD (FPGA)                | PAR_RS   | D3 / G11             | 30         | 29  | D3 / G10             | SER_RS         |                               |
| IPU-LCD (FPGA)                | VSYNC3   | D3 / J10             | 32         | 31  | D3 / B3              | VSYNC0         |                               |
| Power                         | GND      | PWR                  | 34         | 33  | D3 / F8              | READ           | IPU-LCD (FPGA)                |
| IPU-LCD (FPGA)                | CONTRAST | D3 / G12             | 36         | 35  | D3 / F7              | WRITE          |                               |
| Power                         | GND      | PWR                  | 38         | 37  | PWR                  | 3.3V           | Power                         |
| IPU-LCD (FPGA)                | CLS      | D3 / A6              | 38         | 37  | D3 / H10             | REV            | IPU-LCD (FPGA)                |
| Power                         | GND      | PWR                  | 40         | 39  | D3 / H10             | REV            |                               |
| IPU-LCD (FPGA)                | HSYNC    | D3 / D8              | 44         | 43  | D3 / C9              | DRDY0          | IPU-LCD (FPGA)                |
| Power                         | GND      | PWR                  | 42         | 41  | D3 / C9              | DRDY0          |                               |
| IPU-LCD (FPGA)                | LCS1     | D3 / D6              | 46         | 45  | D3 / C8              | FPSHIFT        | IPU-LCD (FPGA)                |
| Power                         | GND      | PWR                  | 44         | 43  | D3 / C8              | FPSHIFT        |                               |
| Reserve                       | NC       |                      | 46         | 45  | D3 / A7              | LCS0           | Reserve                       |
| Power                         | GND      | PWR                  | 48         | 47  |                      | NC             |                               |
| Power                         | GND      | PWR                  | 50         | 49  | PWR                  | 3.3V           | Power                         |
| Charger (PMIC)                | NC       |                      | 52         | 51  |                      | NC             | Reserve                       |
|                               | CHRGRAW2 | D2 / A19             | 54         | 53  | D2 / D13             | CHRGLED        |                               |
|                               | CHRGRAW1 | D2 / A18             | 56         | 55  | D2 / B19             | CHRGRAW3       |                               |
| Power                         | GND      | PWR                  | 58         | 57  | D2 / C18             | CHRGCTRL       | Charger (PMIC)                |
| Charger (PMIC)                | BPFET    | D2 / B15             | 60         | 59  | D2 / B17             | CHRGISNSP      |                               |
| Power                         | GND      | PWR                  | 62         | 61  | PWR                  | 3.3V           | Power                         |
| Charger (PMIC)                | BATTISNS | D2 / A14             | 62         | 61  | D2 / C14             | CHRGISNSN      | Charger (PMIC)                |
| Power                         | GND      | PWR                  | 64         | 63  | D2 / C14             | CHRGISNSN      |                               |
| Power                         | GND      | PWR                  | 66         | 65  | D2 / A12             | BATTFET        | Reserve                       |
| Reserve                       | NC       |                      | 68         | 67  |                      | NC             |                               |
| Reserve                       | NC       |                      | 70         | 69  |                      | NC             |                               |
| Power                         | GND      | PWR                  | 72         | 71  |                      | NC             | Power                         |
| Power                         | GND      | PWR                  | 74         | 73  | PWR                  | 3.3V           |                               |
| SIM (FPGA)                    | SIMPD0   | D3 / K2              | 76         | 75  | D3 / M4              | SCLK0          | SIM (FPGA)                    |
|                               | SRX0     | D3 / L1              | 78         | 77  | D3 / L2              | SRST0          |                               |
|                               | SVEN0    | D3 / H7              | 80         | 79  | D3 / M5              | STX0           |                               |
| Power                         | GND      | PWR                  | 82         | 81  | ?                    | NC             | Reserve                       |
| CAN_IP (FPGA)                 | CAN_RX   | D3 / J3              | 84         | 83  | D3 / G2              | CAN_TX         | CAN_IP (FPGA)                 |
| Reserve                       | NC       |                      | 86         | 85  | PWR                  | 3.3V           | Power                         |
| CAN-Controller                | CAN_RX   | D8 / 2               | 88         | 87  | D8 / 1               | CAN_TX         | CAN-Controller                |
| Power                         | GND      | PWR                  | 90         | 89  | D30 / 12             | VCC_SMS47      | SMS47                         |
| SMS47                         | SMS_SCL  | D30 / 10             | 92         | 91  | D30 / 9              | SMS_SDA        |                               |
| I <sup>2</sup> C_2 (optional) | I2C2_CLK | D20 / 7              | 94         | 93  | D20 / 6              | I2C2_Data      | I <sup>2</sup> C_2 (optional) |
| I <sup>2</sup> C_1            | I2C1_CLK | D19 / 7              | 96         | 95  | D19 / 6              | I2C1_Data      | I <sup>2</sup> C_1            |
| Power                         | GND      | PWR                  | 98         | 97  | PWR                  | 3.3V           | Power                         |
| Reserve                       | NC       |                      | 100        | 99  |                      | NC             | Reserve                       |
|                               | NC       |                      | 102        | 101 | D2 / E6              | AD_TRIGGER_OUT |                               |
| TOUCHE-IF                     | TOUCHE_L | D2 / L13             | 104        | 103 | D2 / P13             | TOUCHE_R       | TOUCHE-IF                     |
| Power                         | GND      | PWR                  | 106        | 105 | D2 / P12             | TOUCHE_B       |                               |
| TOUCHE-IF                     | TOUCHE_T | D2 / M13             | 108        | 107 | D2 / M14             | AI_5           | Analog_IN (PMIC)              |
| Analog_IN (PMIC)              | AI_6     | D2 / U15             | 110        | 109 | PWR                  | 3.3V           | Power                         |
| Analog_IN (PMIC)              | AI_9     | D2 / V17             | 112        | 111 | D2 / R15             | AI_7           |                               |
| Power                         | GND      | PWR                  | 114        | 113 | D2 / P14             | AI_8           | Analog_IN (PMIC)              |
| Analog_IN (PMIC)              | AI_10    | D2 / V18             | 116        | 115 | D2 / V19             | AI_11          |                               |
| Analog_IN (PMIC)              | AI_12    | D2 / W18             | 118        | 117 | D2 / W19             | AI_13          |                               |
| Power                         | GND      | PWR                  | 120        | 119 | PWR                  | 3.3V           | Power                         |

**Table 19: Module plug connector 4**

| Group              | Function                  | Destination / source  | Pin No. X4 |     | Destination / source | Function    | Group              |
|--------------------|---------------------------|-----------------------|------------|-----|----------------------|-------------|--------------------|
| Power              | GND                       | PWR                   | 2          | 1   | PWR                  | 3.3V        | Power              |
| ARM JTAG           | TDI                       | D13 / G1              | 4          | 3   | D13 / F2             | TCK         | ARM JTAG           |
|                    | TMS                       | D13 / G2              | 6          | 5   | D13 / B2             | TDO         |                    |
|                    | DE#                       | D13 / H2              | 8          | 7   | D13 / B1             | RTCK        |                    |
| Power              | GND                       | PWR                   | 10         | 9   | D13 / H1             | TRST#       | Power              |
| Reset (FPGA)       | RESET_IN#                 | D30 / 1               | 12         | 11  | D13 / F1             | SJC_MOD     |                    |
|                    | POR#                      | D29 / 4               | 14         | 13  | PWR                  | 3.3V        | Power              |
| VBAT               | VBAT                      | D2 / C16              | 16         | 15  | D32 / 1              | JTAG_RESET# | ARM JTAG           |
| Power              | GND                       | PWR                   | 18         | 17  | D11 / 2              | RS232 TxD   | RS232 (Driver)     |
| USBOTG             | VUSB                      | D913                  | 20         | 19  | D11 / 1              | RS232 RxD   |                    |
|                    | UDP                       | D9 / 5                | 22         | 21  | D9 / 6               | OC          | USBOTG             |
|                    | UDM                       | D9 / 4                | 24         | 23  | D9 / 12              | PSW#        | USBOTG             |
| Power              | GND                       | PWR                   | 26         | 25  | PWR                  | 3.3V        | Power              |
| Reserve            | NC                        |                       | 28         | 27  | D9 / 7               | UID         | USBOTG             |
| SD card            | GPIO_1_1 (SD_CARD_Detect) | D1 / B23<br>D3 / AG18 | 30         | 29  |                      | NC          | Reserve            |
|                    | SD_CMD / CD               | D18 / C2              | 32         | 31  | D18 / D2             | SD_CLK      | SD card            |
| Power              | GND                       | PWR                   | 34         | 33  | D18 / C4             | SD_D0       |                    |
| SD card            | SD_D2                     | D18 / C3              | 36         | 35  | D18 / D4             | SD_D1       | Power              |
|                    | SD_D3                     | D18 / D3              | 38         | 37  | PWR                  | 3.3V        |                    |
| PMIC               | ON2                       | D32 / 11              | 40         | 39  | D32 / 9              | ON1         | PMIC               |
| Power              | GND                       | PWR                   | 42         | 41  | D32 / 13             | ON3         | FPGA_CTRL          |
| FPGA_CTRL          | CFG_CS#                   | D3 / E2               | 44         | 43  | D3 / F4              | CFG_D1      |                    |
|                    | CE#                       | D3 / R8               | 46         | 45  | D3 / N7              | CFG_D0      |                    |
|                    | CONF_DONE                 | D3 / P24              | 48         | 47  | D3 / M6              | STATUS#     | Power              |
| Power              | GND                       | PWR                   | 50         | 49  | PWR                  | 3.3V        | FPGA_CTRL          |
| FPGA_CTRL          | CFG_DCLK                  | D3 / P3               | 52         | 51  | D3 / P4              | CONFIG#     |                    |
|                    | FPGA_TDO                  | D3 / P6 (2V5)         | 54         | 53  | PWR                  | 2.5V        |                    |
|                    | FPGA_TCK                  | D3 / P5 (2V5)         | 56         | 55  | D3 / P7 (2V5)        | FPGA_TDI    | Power              |
|                    | GND                       | PWR                   | 58         | 57  | D3 / P8 (2V5)        | FPGA_TMS    |                    |
| FPGA_CTRL          | INIT_DONE                 | D3 / P26              | 60         | 59  | D2 / B8              | LEDMD1      | LED (PMIC)         |
| LED (PMIC)         | LEDMD2                    | D2 / F9               | 62         | 61  | PWR                  | 3.3V        | Power              |
|                    | LEDAD2                    | D2 / E8               | 64         | 63  | D2 / E9              | LEDMD3      | LED (PMIC)         |
| Power              | GND                       | PWR                   | 66         | 65  | D2 / C9              | LEDMD4      |                    |
| Tri-Col-LED (PMIC) | LEDR1                     | D2 / B10              | 68         | 67  | D2 / C8              | LEDAD1      | Tri-Col-LED (PMIC) |
|                    | LEDB1                     | D2 / F11              | 70         | 69  | D2 / C7              | LEDKP       |                    |
|                    | LEDG2                     | D2 / F10              | 72         | 71  | D2 / E11             | LEDG1       |                    |
| Power              | GND                       | PWR                   | 74         | 73  | PWR                  | 3.3V        | Power              |
| Tri-Col-LED (PMIC) | LEDG3                     | D2 / C10              | 76         | 75  | D2 / E10             | LEDR2       | Tri-Col-LED (PMIC) |
|                    | LEDB3                     | D2 / GB9              | 78         | 77  | D2 / G10             | LEDB2       |                    |
| Reserve            | NC                        |                       | 80         | 79  | D2 / E10             | LEDR3       | Reserve            |
| Power              | GND                       | PWR                   | 82         | 81  |                      | NC          |                    |
| Reserve            | NC                        |                       | 84         | 83  |                      | NC          | Power              |
|                    | NC                        |                       | 86         | 85  | PWR                  | 3.3V        |                    |
|                    | NC                        |                       | 88         | 87  |                      | NC          |                    |
| Power              | GND                       | PWR                   | 90         | 89  |                      | NC          | Reserve            |
| Reserve            | NC                        |                       | 92         | 91  |                      | NC          | Audio (PMIC)       |
| Audio (PMIC)       | CDCOUT                    | D2 / U6               | 94         | 93  | D2 / U5              | LSPL        |                    |
|                    | TX_OUT                    | D2 / V3               | 96         | 95  | D2 / U4              | TX_IN       | Power              |
| Power              | GND                       | PWR                   | 98         | 97  | PWR                  | 3.3V        | Audio (PMIC)       |
| Audio (PMIC)       | RX_OUT_L                  | D2 / P9               | 100        | 99  | D2 / U7              | RX_OUT_R    |                    |
|                    | RX_IN_L                   | D2 / U8               | 102        | 101 | D2 / R9              | RX_IN_R     |                    |
|                    | HS_OUT_R                  | D2 / U9               | 104        | 103 | D2 / P10             | HSPGS       | Power              |
|                    | GND                       | PWR                   | 106        | 105 | D2 / V7              | HSPGF       |                    |
| Audio (PMIC)       | HS_OUT_L                  | D2 / V8               | 108        | 107 | D2 / R8              | HSL_DET     | Power              |
|                    | MIC1L_IN                  | D2 / U2               | 110        | 109 | PWR                  | 3.3V        |                    |
|                    | MIC1R_IN                  | D2 / V2               | 112        | 111 | D2 / U3              | MIC2_IN     | Audio (PMIC)       |
| Power              | GND                       | PWR                   | 114        | 113 | PWR                  | GND         |                    |
| Audio (PMIC)       | SPEAK_L_N                 | D2 / V4               | 116        | 115 | D2 / V10             | SPEAK_R_N   | Power              |
|                    | SPEAK_L_P                 | D2 / V5               | 118        | 117 | D2 / V9              | SPEAK_R_P   |                    |
| Power              | GND                       | PWR                   | 120        | 119 | PWR                  | 3.3V        | Power              |

## 3.5 Cooling

### 3.5.1 Heat sink

The necessary heat sink depends of the mode of operation (e.g., clock frequency, installation height, airflow), and can therefore not be universally defined.

The following components have to be taken into consideration for heat dissipation:

- Processor: MCIMX31
- Power management: MC13783
- LAN controller: LAN9215
- FPGA: EP3C40 resp. EP3C120

## 3.6 Mechanics

### 3.6.1 General information

- High pin count SMD plug connectors with 0.8 mm pitch
- The combination with different counterparts allows customisation of the stack height to the height of the parts mounted on the base board
- Double-sided SMD assembly

### 3.6.2 Dimensions

- Board dimensions 75 mm × 60 mm (see Illustration 15)
- Stack height see Illustration 16 and Table 20

3.6.2.1 Board dimensions

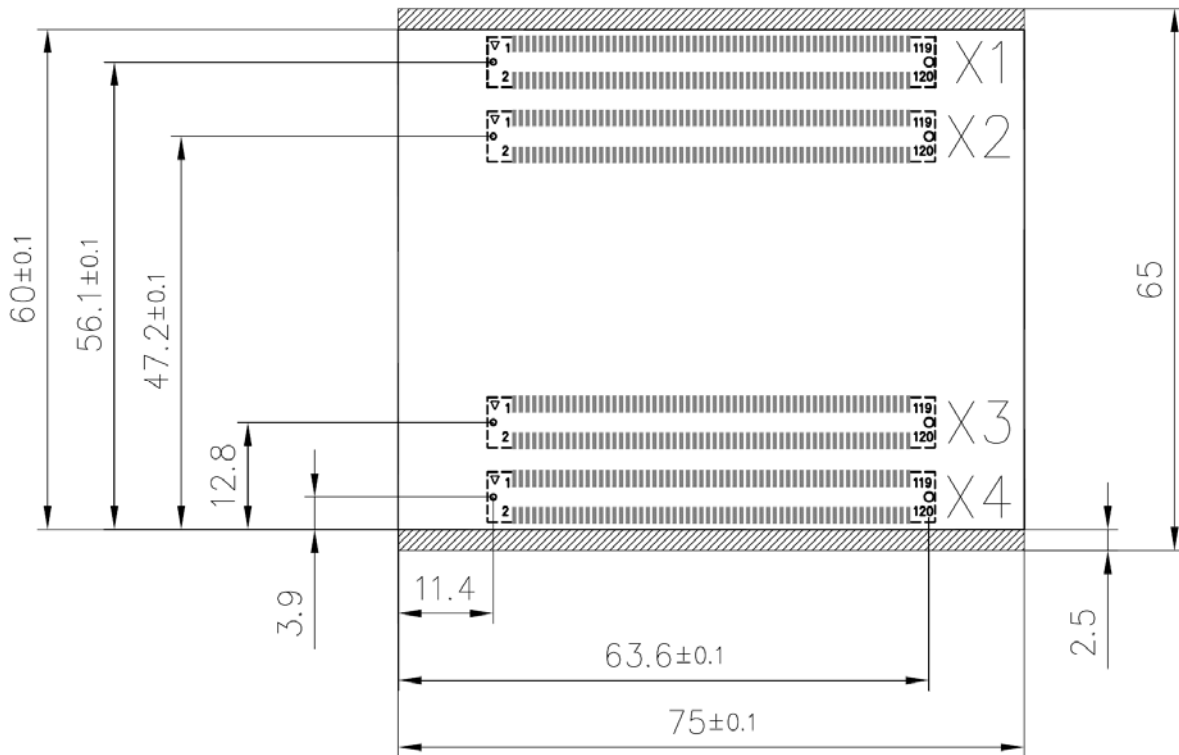


Illustration 15: View from top side through printed circuit board

**Note:**

2.5 mm should be kept free on the base board, along the longitudinal edges on both sides of the module for the extraction tool MOZI52xx.

3.6.2.2 Stack height

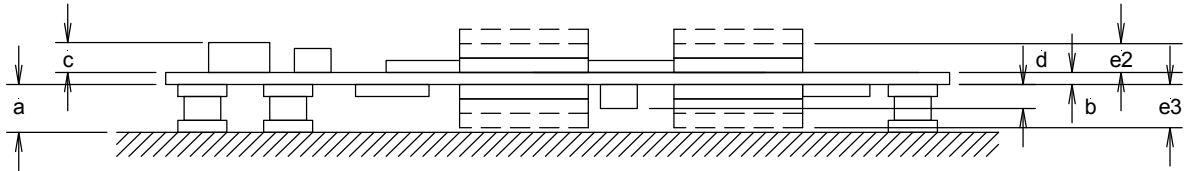


Illustration 16: Stack heights (not to scale)

| Dim. | Value [mm] | Remark   |
|------|------------|--|
| a    | 5.0 ±0.2   | Combination module connector with receptacle;<br>6, 7 and 8 mm are possible with different plug connectors on base board |
| b    | 1.48       | Printed circuit board  |
| c    | 3.4 ±0.4   | Coil L1 (highest stack height top side)  |
| d    | 1.8 ±0.2   | Ceramic capacitor type 1206 (highest stack height bottom side)   |

Table 20: Component heights

| Stack height without heat sink max.<br>a + b + c | Free stack height under module min.<br>a – d | Stack height without heat sink in the area of SDRAMs max.<br>a + b + e (... e4) | Free stack height under module in the area of SDRAMs min.<br>a – e (... e4) |
|--|--|---|---|
| 9.88 mm  | 2.8 mm                                       | 8.6 mm  | 3.3 mm  |

Table 21: Stack heights

3.6.3 Notes of treatment

To avoid damages caused by mechanical stress, the TQMa31 may only be extracted from the base board using the special extraction tool MOZI52xx. This extraction tool is delivered with the Starterkit STKa31. It can, however, also be obtained separately.

### 3.7 Boot Loader

The boot loader "EBoot" is the basic software delivered with the TQMa31. For more information see separate specification.

### 3.8 Safety requirements and protective regulations

#### 3.8.1 EMC

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- With metal casings, a good (at least according to RF) connection to the printed circuit board or to the potential of the housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding
- Filtering of all signals which can be connected externally (also "slow" and DC can radiate RF indirectly)

#### 3.8.2 ESD

In order to avoid interspersions on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the base board, no special preventive measures were planned on the module. According to the data sheets, the used devices already have some protection; however, this is generally not sufficient to fulfil the legal requirements without any further measures.

Following measures are recommended:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, e.g. Zener diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

### 3.9 Reliability and service life

The subassembly is designed for a service life of 10 years. It was also designed to be insensitive to vibration and impact.

### 3.10 Climatic and operational conditions

- Protection class IP00
- Storage temperature -40 ... +85 °C

The possible temperature range strongly depends on the installation situation, (heat dissipation by conduction and convection). Hence, no fixed value can be given for the whole assembly. Reliable operation is generally achieved when the following conditions are met:

Standard temperature range:

- Chip temperature of CPU 0 ... 70 °C
- Package temperature of PMIC 0 ... 70 °C
- Package temperature of all other ICs 0 ... 70 °C

Extended temperature range:

- Chip temperature of CPU -40 ... 85 °C
- Package temperature of PMIC -30 ... 85 °C
- Package temperature of all other ICs -40 ... 85 °C

Detailed information to the thermal characteristics of the CPU is found in (3). Information about example configurations with active and passive cooling can be obtained from TQC support.

### 3.11 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94  
(source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96  
(source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98  
(source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01  
(source of information: BGBl I 2001, 3379)

## 4. Appendix

### 4.1 References

| No. | Description   | Version / Date       | Author | Company   |
|-----|---|----------------------|--------|-----------|
| 1   | Cyclone III Device Handbook   | V1.4 / Oct. 2007     |        | Altera    |
| 2   | MCIMX31 and MCIMX31L Datasheet (MCIMX31_5)  | Rev. 4.2 / Nov. 2008 |        | Freescale |
| 3   | MCIMX31 and MCIMX31L Reference Manual (MCIMX31RM)   | Rev. 2.4 / Dec. 2008 |        | Freescale |
| 4   | MCIMX31 and MCIMX31L Chip Errata (MCIMX31CE)  | Rev. 5.5 / Nov. 2008 |        | Freescale |
| 5   | MC13783 Technical Data MC13783/D  | Rev. 3.4 / 3.2007    |        | Freescale |
| 6   | MC13783 User's Guide MC13783UG  | Rev. 3.5 / 2.2007    |        | Freescale |
| 7   | Intel StrataFlash® Embedded Memory (P30) Family Datasheet (309045)                          | Rev. 007 / May. 2006 |        | Intel     |
| 8   | Intel StrataFlash® Embedded Memory (P33) Family Datasheet (314749-002US)                    | Aug. 2006            |        | Intel     |
| 9   | Mobile DDR SDRAM Datasheet MT46H64M16LF<br>PDF:09005aef82846a0b<br>Source: 09005aef828c2f8f | Rev. A02/07 EN       |        | Micron    |
| 10  | Mobile DDR SDRAM Datasheet MT46H32M16LF<br>PDF:09005aef81a16e9d<br>Source: 09005aef81a6c5f3 | Rev. L05/07 EN       |        | Micron    |

Table 22: References