For Technology
in Quality

User Manual
TQM885D

TQM885D.UM.100
2007/10/22

	Date:	Name:	Description:	User Manual	
Created:	2007/10/22	PETZ MM / fpe	Project:	TQM885D	
Checked:		Robert Nerbl	Document–No.:	TQM885D.UM.100	
Company:			Release status:	Released	
			Client:	TQC	Page 1 of 38
File:	TQM885D.UM.100.DOC				Revision: 100

Table of contents

Table directory

Illustration directory

1. About this manual

1.1 Update index

Table 1: Update history

Rev.	Date	Pos.	Name	Modification
100	14.09.2007	1	PETZ MM / fpe	Creation

1.2 Scope

This document contains comprehensive information for OEM manufacturers who integrate systems and/or develop customer-specific system components using the module TQM885D.

In this manual the TQM885D is described based on two standard variations, representative for all further variations.

Several specific features are covered by additional module variations.

To get an overview of all possible variations, please contact your responsible sales TQ-Components GmbH representative.

1.3 Variations

The present document describes the technical details of different microcontroller modules of the TQM88xD series. The name MPC885D is mostly used synonymously for all applicable microcontrollers of the MPC88x series (see >> ***Table 2***). In most cases TQM885D also refers to all variations listed below.

Table 2: Product key

Product key	CPU
TQM880D.....-xx...	MPC880D and Variants (xx)
TQM885D.....-xx...	MPC885D and Variants (xx)

The variation key is explained in a separate document see >> ***[4]***.

1.4 Conventions and terminology

1.4.1 Conventions

In this document the following fonts are used to display special parts of the text.

Table 3: Conventions

Convention	Description
[PATH:/filename.ext]	Rectangular brackets and italic boldface are used to designate a directory, a file name and its extension.
`Address / command`	Different fonts and accentuations are used to indicate character strings referring to the application, such as • Memory addresses • Software code
>> ***Reference***	Two arrows and italic boldface are used to designate a cross-reference to another section, figure or table.

1.4.2 Acronyms and definitions

The following acronyms and abbreviations are used in this document.

Table 4: Abbreviations

Abbreviation	Description
AES	Advanced Encryption Standard
ATM	Asynchronous Transfer Mode
BDM	Background Debug Mode
CAN	Controller Area Network
CLES	Core Little Endian Swap
CMOS	Complementary Metal Oxide Semiconductor
CPM	Communications Processor Module
CPU	Central Processing Unit
DES/3DES	Data Encryption Standard/Triple Data Encryption Standard
EEPROM	Electrically Erasable Programmable Read-Only Memory (Byte-wise re-writable)
EGB	Elektrostatisch Gefährdete Bauelemente (Electrostatic sensitive components)
EMV	ElektroMagnetische Verträglichkeit (Electromagnetic compatibility)
ENMON	ENable MONitor
ESD	ElectroStatic Discharge
FBGA	Fine pitch Ball Grid Array
Flash	Electrically Erasable Programmable Read-Only Memory (Block Erase)
GPCM	General-Purpose Chip-select Machine
HDLC	High-level Data Link Control
HMAC	Hash Message Authentication Code
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit

Abbreviation	Description
JTAG	Joint Test Action Group
LQFP	Low profile Quad Flat Package
MD5	Message-Digest Algorithm 5
OEM	Original Equipment Manufacturer
OSCM	Oscillator Module
PBGA	Plastic Ball Grid Array
PCB	Polychlorierte Biphenyle (Polychlorinated biphenyls)
PCMCIA	Personal Computer Memory Card International Association
PCMCIA	People Can't Memorize Computer Industry Acronyms
PCN	Product Change Note
QFP	Quad Flat Package
RISC	Reduced Instruction Set Computing
RTC	Real Time Clock
SCC	Serial Communications Controller
SDRAM	Synchronous Dynamic Random Access Memory
SHA	Secure Hash Algorithm
SMC	Serial Management Controller
SMD	Surface Mounted Device
TSSOP	Thin Shrink Small Outline Package
TTL	Transistor-Transistor-Logic
UART	Universal Asynchronous Receiver/Transmitter
UPM	User-Programmable Machine
USB	Universal Serial Bus

1.5 Continuing documents

The following documents contain information which is linked to this user manual.

Table 5: Continuing documents

Document	Revision	Published
Starterkit Hardware manual STK8xxL	latest version	TQ-Components
Schaltplan STK8xxL	latest version	TQ-Components
Bestückungsplan STK8xxL	latest version	TQ-Components
Spezifikation TQ-Monitor MON8xx	latest version	TQ-Components
Fast Ethernet-Adapter FETHD_USB_8xx_ADAP Schaltplan	latest version	TQ-Components
Fast Ethernet-Adapter FETHD_USB_8xx_ADAP Bestückungsplan	latest version	TQ-Components
If necessary current Application Notes	latest version	TQ-Components
MPC885D RM Family Reference Manual: Technical Data	latest version	Freescale Semiconductor
MPC885D Errata	latest version	Freescale Semiconductor
Application Notes	latest version	Freescale Semiconductor

An adaptor (FETHD_USB_8xx_Adap) was developed for the TM88xD modules which extends the STK8xxL by two Fast Ethernet interfaces and a host/device port USB1.1, so that the TQM88xD modules can be used with the consisting Starterkit (STK8xxL.400 or newer). Plug connectors (jacks) are placed on the upper side on this subassembly module for the TQM88xD module (compatible to modules TQM8xx). On the STK8xxL.400 the plug connectors with which the adaptor can be put in the module slot are on the underside.

The subassembly FETHD_USB_8xx_Adap is described in a separate document.

1.6 Document updating

This user manual refers to revision 100 of the module TQM885D. All following revisions are discussed in later product change notifications (PCN). These become with the publication an integral component of this document.

1.7 Disclaimer

TQ-Components GmbH does not guarantee the up-to-dateness, correctness, completeness or quality of the information provided in this manual as well as its further use. Claims lodged against TQ-Components GmbH, related to damages of material or intellectual nature, arising out of the use or non-use of information contained in this manual, or out of the use of incorrect or incomplete information, will not be accepted as long as there is no evidence of intentional or negligent fault on the part of TQ-Components GmbH.

TQ-Components GmbH explicitly reserves the right to change or supplement the contents of this manual or parts thereof, without prior announcement.

1.8 Registered trademark

TQ-Components GmbH has strived to observe the copyright of the graphics and texts used in all publications, and to use self-created, or those, which are license-free.

All brand names and trademarks contained in this publication are protected by copyright, unless specifically stated otherwise, of the corresponding owner or holder of the same. The mere mentioning cannot be used to conclude that brand names and registered trademarks are not copy protected by third parties.

1.9 Copyright

1.10 Imprint

TQ-Components GmbH

Schulstraße 29a
82234 Weßling

Tel: +49 (0)8153 9308-333
Fax: +49 (0)8153 9308-134

E-Mail: info@tqc.de
Web: http://www.tq-components.com/

1.11 File archiving

This document is archived on the server under the project TQM885D in the subdirectory DOK under the name TQM885D.UM.100.doc in the present revision state.

2. Safety

2.1 Safety tips and icons

The following safety warnings in connection with the suitable icons and colours can be used in this document. Before using this product please also read >> ***Safety regulations***.

Caution: Electric shock!  **Text of warning.**	This icon indicates the possible use of voltages higher than 24V. Please, take notice of the appropriate legal regulations. The non-observance of the regulations can lead to serious damages of your health as well as to the damage / destruction of the component.
Attention: Damage or malfunction!  **Text of warning.**	Possible source of danger. By disregarding the prescribed approach your health can possibly be damaged, and/or the used material can be damaged / broken.
Attention: ESD Electrostatic discharge!  **Text of warning.**	Contact with EGB (electrostatic sensitive components) sensitive subassemblies and/or components. These components can already be damaged or broken with discharge voltages of approx. 50V. The human body perceives this discharge often only from a voltage of approx. 3,000V.
Note… **Text of note**	Important details or aspects for your work are highlighted.

2.2 Safety regulations

Much effort was made to ensure that the module TQM885D is a safe product.

However, certain risks cannot be excluded for persons and materials due to improper use. These risks are described below.

To avoid danger to the life or the health of persons, or damage to property, please make sure that your module TQM885D is used only used by certified personnel who have taken note of the information and of safety regulations in this document and all related rules and regulations.

2.2.1 Electric shock

Caution: Electric shock!

No danger to life can be caused by the module TQM885D. However, it cannot be excluded, that due to system integration a higher voltage than 24V occurs. In this case there is a possible danger to the life of persons who do not keep to the compulsory safety rules.

A general rule is, not to touch the system or the module TQM885D during operation. This is important especially in cases of switching on, changing jumper settings, or connecting other devices without making sure beforehand that the power supply of the system was switched off!

The TQM885D and/or system may only be used and serviced by certified personnel who have taken note of the information and of safety regulations in this document and all related rules and regulations.

2.2.2 Information to the temperature range

Attention: Damage or malfunction!

A risk of the damage to property or the malfunction can originate from the given specifications of the components if the necessary ambient temperature is not kept.

Please make sure that the following temperature ranges for the system design and the operation of all used components are kept:

- 0 … +70°C (Standard)
- -40 … +85°C (extended)

The TQM885D and/or system may only be operated by certified personnel who have taken note of the information and of safety regulations in this document.

2.2.3 Information concerning ESD handling

Attention: ESD Electrostatic discharge

The electronic components of your module TQM885D are naturally sensitive to electrostatic discharge (ESD).

Please always wear antistatic clothes and use ESD-safe tools, packing materials etc. and operate your TQM885D in an ESD-safe environment. Especially if you switch on modules, change jumper settings, or connect other devices!

3. Hardware TQM885D

3.1 TQM885D system architecture / block diagram

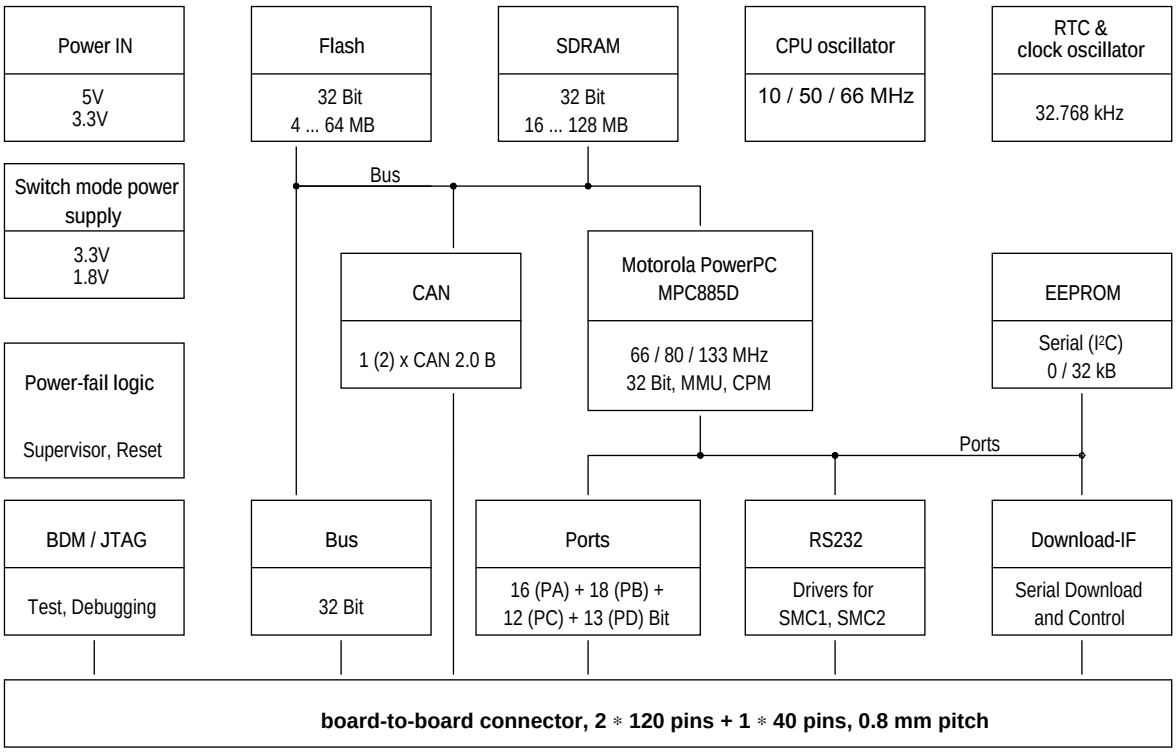

Illustration 1: Block diagram TQM885D

3.2 System components

- CPUs MPC880, MPC885D
- Oscillator for CPU
- RTC
- Oscillator for RTC
- Power-fail logic
- DC/DC converter
- SDRAM, Flash
- 1 * full CAN 2.0 B active
- 2 * RS232 serial drivers for SMC1 and SMC2
- BDM interface
- Board-to-board connector system, 280 pins, 0.8 mm pitch

3.2.1 CPU MPC885D / MPC880D

The MPC885D has a different port pin assignment compared to those of the processors used on the TQM8xxM modules. In addition, some functions are distributed differently to the ports A, B, C, and D compared to the ports of older CPUs. Furthermore the CPU has a port E, which the previously used CPUs do not have.

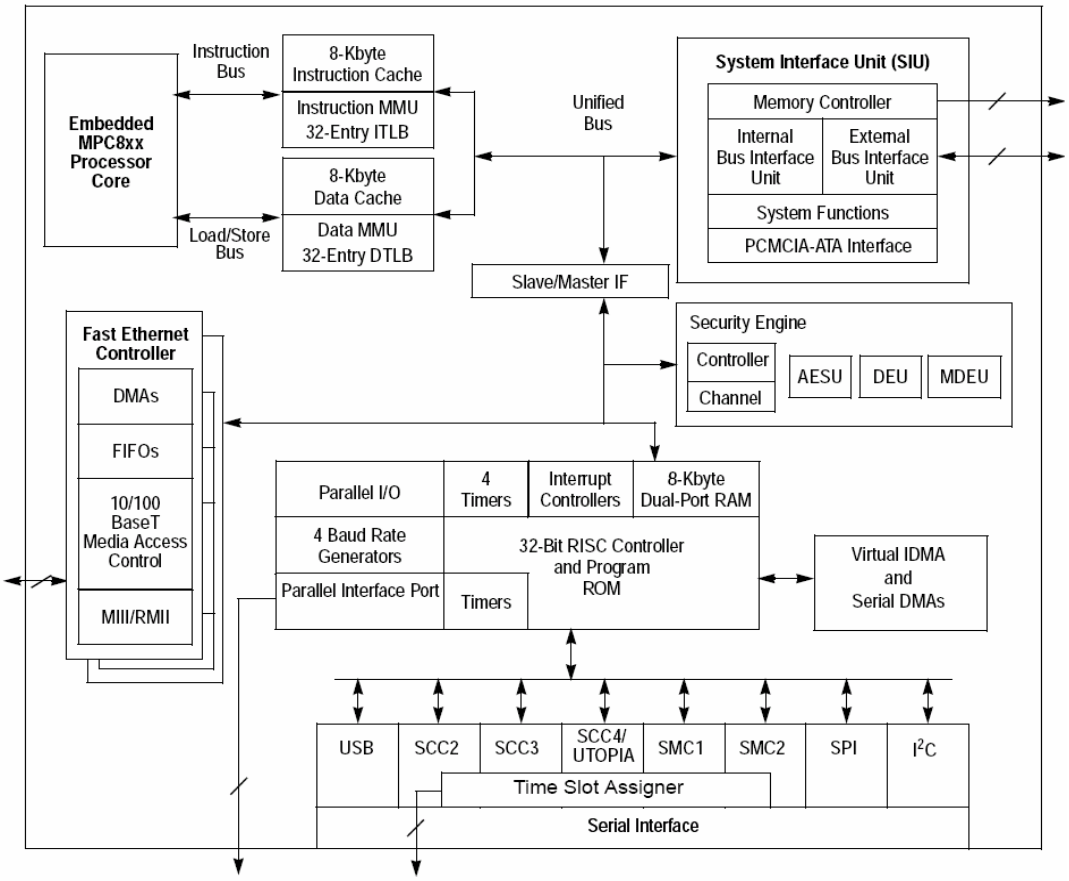

Illustration 2: Block diagram MPC885D

Table 6: CPU

Component	Package	Model	Ext. temp.	Manufacturer	Alternative manufacturer
MPC885D	PBGA 357	PowerQUICC I Processor	yes	Freescale	–
MPC880D	PBGA 357	PowerQUICC I Processor	yes	Freescale	–

3.2.1.1 MPC885D / MPC880D features

- Efficient architecture which contains an 8xx-core with separate RISC and CPM
- CPU clock frequencies 66 MHz, 80 MHz and 133 MHz
- 8 KB instruction cache and 8 KB data cache
- Powerful memory controller and system functions
- Integrated on-chip security engine, which supports AES, DES/3DES, SHA/MD5/HMAC
- Support for PCMCIA (e.g.: to connect 802.11 a/b/g WLAN modules)
- Support for two Fast Ethernet (10/100 Mbps), UART, HDLC, ATM and other, depending on MPC885D derivative
- USB 1.1 host/device (USB 2.0 full/low speed compatible)
- Up to three SCCs and up to two SMCs
- Many other features: timer, baud rate generators, etc.
- 357-pin PBGA package
- 0.18 µ process technology
- 1.8V core, 3.3V input / with a power consumption of less than 1 W

3.2.2 Supervisor

To monitor the reset trigger level for VCC3V3 a 3.3V supervisor is used which guarantees a reset down to approx. 0V. The precise supervision of both supply voltages is achieved by using a reference voltage and a comparator. The LM4050 is used as the reference and the LMC7221 as the comparator.

3.2.2.1 Tolerances and reset trigger levels for VCC5V

Tolerance of supply (see >> ***Illustration 3*** pos. D):
VCC5V = 5V – 8.66% / +10% = 4.561V … 5.5V

Tolerance of the supervisor circuit:
VReset = 4.501V … 4.561V (extended temperature range, LM4050 / LMC7221)

Permitted operation range for CAN controller and 5V logic (see >> ***Illustration 3***, pos. E):
VCC5V = 5V ± 10% = 4.5V … 5.5V

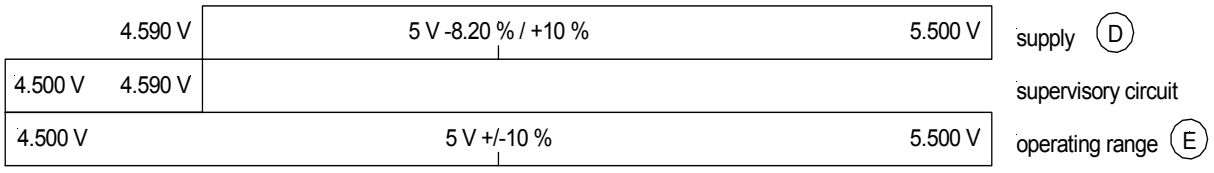

Illustration 3: Tolerances of the 5V supply

3.2.2.2 Tolerances and reset trigger levels for VCC3.3V

Tolerance for external supply (see >> ***Illustration 4***, pos. A):
VCC3V3 = 3.3V – 3.811% / +5% = 3.174V … 3.465V

Tolerance for internal supply / switching regulator (see >> ***Illustration 4***, pos. B):
VCC3V3 = 3.185V … 3.392V (extended temperature range)

Permitted operation range for CPU and 3.3V logic (see >> ***Illustration 4***, pos. C):
VCC3V3 = 3.3V ± 5% = 3.135V … 3.465V

Tolerance of the supervisor circuit (extended temperature range, LM4050 / LMC7221):
VReset = 3.136V … 3.174V

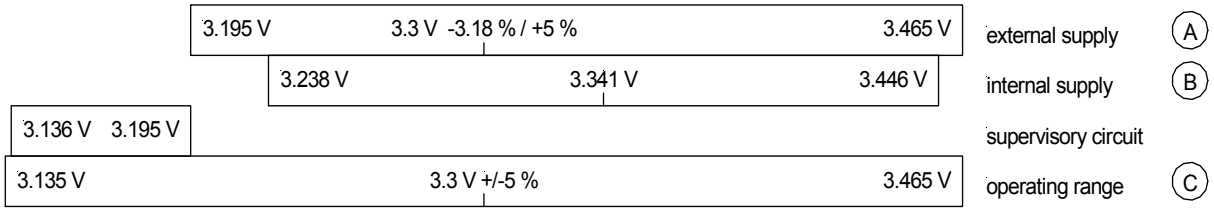

Illustration 4: Tolerances of the 3.3V supply

3.2.2.3 Tolerances and reset trigger level for VDDL (1.8V)

Tolerance for internal supply / switching regulator (see >> ***Illustration 5***, pos. F):
VDDL = 1.752V … 1.853V (extended temperature range)

Permitted operation range of CPU (see >> ***Illustration 5***, pos. G):
VDDL = 1.7V … 1.9V

Tolerance of the supervisor circuit (extended temperature range, LM4050 / LMC7221):
VReset = 1.704V … 1.731V

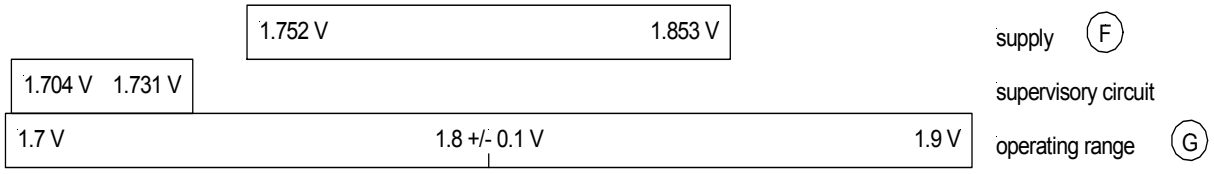

Illustration 5: Tolerances of the 1.8V supply

3.2.3 External reset input

The signal RESIN# is decoupled in such a way, that it can be controlled by a push-pull output without any retroactive effects to the reset circuit. This is accomplished by use of a Schottky diode at the MR (Manual Reset) input of the supervisor.

3.2.4 ENMON# switch

- The signal ENMON# (ENable MONitor) serves to activate the TQ-Monitor software. This additionally needed input signal is created by multiplexing PA15.
- After ending HRESET# the ENMON# circuit remains active for approx. 10 ms; in this time the status of ENMON# can be read.

After that the circuit returns to its normal operation, PA15 is switched through, the ENMON# circuit is transparent.

3.2.5 Reset configuration

In normal use the system reads the reset configuration from the bus (RSTCONF# = 0). If required the default configuration (RSTCONF# = 1 → bits 0 … 15 to 0), can be used by applying a logic “1” to RSTCONF#.

Table 7: Reset configuration

Bits	Name	Description	66 MHz	80 / 133 MHz
0	EARB	External arbitration If this bit is set, external arbitration is assumed. If it is cleared, an internal arbitration is executed.	0	0
1	IIP	Initial interrupt prefix Defines the initial setting of MSR [IP] which defines the position of the interrupt table in the memory. If IIP is deleted (default), the initial setting of MSR [IP] is logic 1; if it is set, the initial setting of MSR [IP] is logic 0.	1	1
2	BBE	Boot Burst Enable 0 The boot device does not support burst. 1 The boot device supports burst.	0	0
3	BDIS	Boot disable If BDIS is set, memory bank 0 is invalid; i.e. BR0 [V] is cleared. 0 After a reset the memory controller is activated, all addresses are customised. 1 After a reset the memory controller is cleared, but not activated.	0	0
4–5	BPS	Boot Port Size Defines the port size of the boot device as listed in the table: 00 32-bit port size 01 8-bit port size 10 16-bit port size 11 Reserved	00	00
6	–	Reserved	0	0
7–8	ISB	Initial internal space base select Defines the initial setting of IMMR bits 0 – 15 and determines the base address of the internal memory. 00 0x00000000 01 0x00F00000 10 0xFF000000 11 0xFFF00000	11	11

Bits	Name	Description	66 MHz	80 / 133 MHz
9–10	DBGC	Debug pin configuration See >> ***7.1*** for details.	11	11
11–12	DPPC	Debug port pins configuration See >> ***7.1*** for details. Configuration for BDM debugging (JTAG/BDM# = 1 or floating) Configuration for JTAG test (JTAG/BDM# = 0)	01 / 00*	01 / 00*
13–14	EBDF	External bus division factor Defines the frequency division factor between GCLK1/GCLK2 and GCLK1_50/GCLK2_50. CLKOUT is similar to GCLK2_50. GCLK2_50 and GCLK1_50 are used as an interface to the external system by the system interface and the memory controller. 00 Full speed bus 01 Half speed bus 10 Reserved 11 Reserved	01	01
15	CLES	Core Little Endian Swap Defines core access operation after a reset. 0 Big Endian 1 Little Endian	0	0

* Depending on JTAG/BDM# signal

3.2.6 Clock

3.2.6.1 CPU clock

The clock for the CPU is generated with an oscillator at the OSCM input and then multiplied. The necessary settings are performed via the "reset configuration word“ and in the software.

The central clock signal of the module is CLKOUT (= external bus clock). The whole timing of the MPC885D is synchronous to this signal. It is used to control the SDRAM and is led onto the connector. To avoid retroactive effects from the used base board to the module (SDRAMs), the signal is buffered on the module with a zero delay buffer. The driver's full power of the buffer of 50 pF can be used by the external hardware.

Table 8: Oscillator for the CPU

Component	Package	Model	Ext. temp.	Manufacturer	Alternative manufacturer
SXO3-05032-S-E-50-W-10.000MHz	SMD 5 ∗ 3.2 mm	10MHz / ±50 ppm	yes	Petermann	–

3.2.6.2 CAN clock

The oscillator integrated in the CAN controller generates a clock of 16 MHz by using an external quartz. Take note of this when initialising the CAN controller. The CAN controller generates the baud rates for the CAN bus from its clock.

Table 9: Quartz crystal for CAN controller

Component	Package	Model	Ext. Temp.	Manufacturer	Alternative manufacturer
Q16.0JXS321210/20T1LF	SMD 3.2 ∗ 2.5 mm	16 MHz / ±50 ppm	yes	Jauch	FOX

3.2.6.3 RTC clock

The oscillator integrated in the RTC generates the RTC clock of 32.768 kHz by using an external quartz. This clock is used to drive the external RTC.

Table 10: Quartz crystal for RTC (4.8 ∗ 1.9 mm)

Component	Package	Model	Ext. Temp.	Manufacturer	Alternative manufacturer
M4819 32,768 kHz ±30 ppm, -40 … +85 °C / 6pF	SMD 4.8 ∗ 1.9 mm	32.768 kHz ±30 ppm / 6pF	yes	Petermann	FOX; Jauch

3.2.7 RTC (Real Time Clock)

As there is no CPU-internal RTC, this was assembled externally:

- RTC DS1337U, control via I^2C bus of CPU
- Clock frequency I^2C 400 kHz, not to impair speed of the I^2C bus
- Battery buffering possible
- Alarm INT# (possible for two different times), is not hard-wired on the module, but is led to the connector for free use on the base board (X3-4)

Table 11: RTC

Component	Package	Model	Ext. Temp.	Manufacturer	Alternative manufacturer
DS1337U	UMAX 8	RTC	yes	Maxim	–

3.2.8 EEPROM (Non-volatile read/write memory)

The serial EEPROM can store, e.g., module-specific data as well as customised parameters. In contrast to Flash, single memory cells can be deleted and overwritten in the EEPROM. In the delivery condition the EEPROM is blank. It can save, e.g., configuration data permanently.

- 0 or 4 … 32 kiByte
- Control via I^2C bus of CPU (I2CSCL / I2CSDA)
- Address lines of EEPROMs on 0b000
- Shares the I^2C bus with RTC

Table 12: EEPROM devices

Component	Package	Model	Ext. Temp.	Manufacturer	Alternative manufacturer
M24C32-WDW6TP	TSSOP8	EEPROM 4kiByte	yes	STM	–
M24C64-WDW6TP	TSSOP8	EEPROM 8kiByte	yes	STM	–
AT24C64-10TU-2.7	TSSOP8	EEPROM 8kiByte	yes	Atmel	–
AT24C128-10TU-2.7	TSSOP8	EEPROM 16kiByte	yes	Atmel	–
AT24C256B-10TU-1.8	TSSOP8	EEPROM 32kiByte	yes	Atmel	–
24LC256I / STG	TSSOP8	EEPROM 32kiByte	yes	Microchip	–
M24256-BWDW6P	TSSOP8	EEPROM 32kiByte	yes	STM	–

3.2.9 CAN controller

Features of the CAN controller:

- Full CAN 2.0 B compatible interface, accomplished with an AS82527 (Intel) or CC770E (Bosch Microelectronics)
- Automatic message filtering
- Control via UPMC
- Access mode 8-bit non-multiplexed
- Used signals:
  CS_CAN#/CS3#
  GPL_AB2# (R/W# CAN)
  GPL_A5# (Buffer enable bus transceiver for CAN)
  A22, A23 (Address decoding)
  HRESET# (RESET# CAN)
  IRQ_CAN#/IRQ7# (Interrupt for CAN)
- No CAN transceiver (In– and outputs with TTL level)
- 5V supply

Table 13: CAN controller

Component	Package	Model	Ext. Temp.	Manufacturer	Alternative manufacturer
CC770E	LQFP44	CAN controller (16 MHz)	yes	Bosch	–
QE82527	QFP44	CAN controller (16 MHz)	yes	Intel	–

3.2.10 Bus driver

- No buffered address lines on the module: SDRAM and FLASH are operated without additional delay.
- Unbuffered address bus led to the connector: Peripheral can be connected externally just by adding a driver. The necessary load capacity for a driver's input is still available.
- Unbuffered data bus led to the connector: Direct connection of up to approx. 20 pF is possible; external buffers are necessary for a higher load.
  HINT: To avoid conflicts with the reset configuration, no buffers with "bus hold" function are allowed.

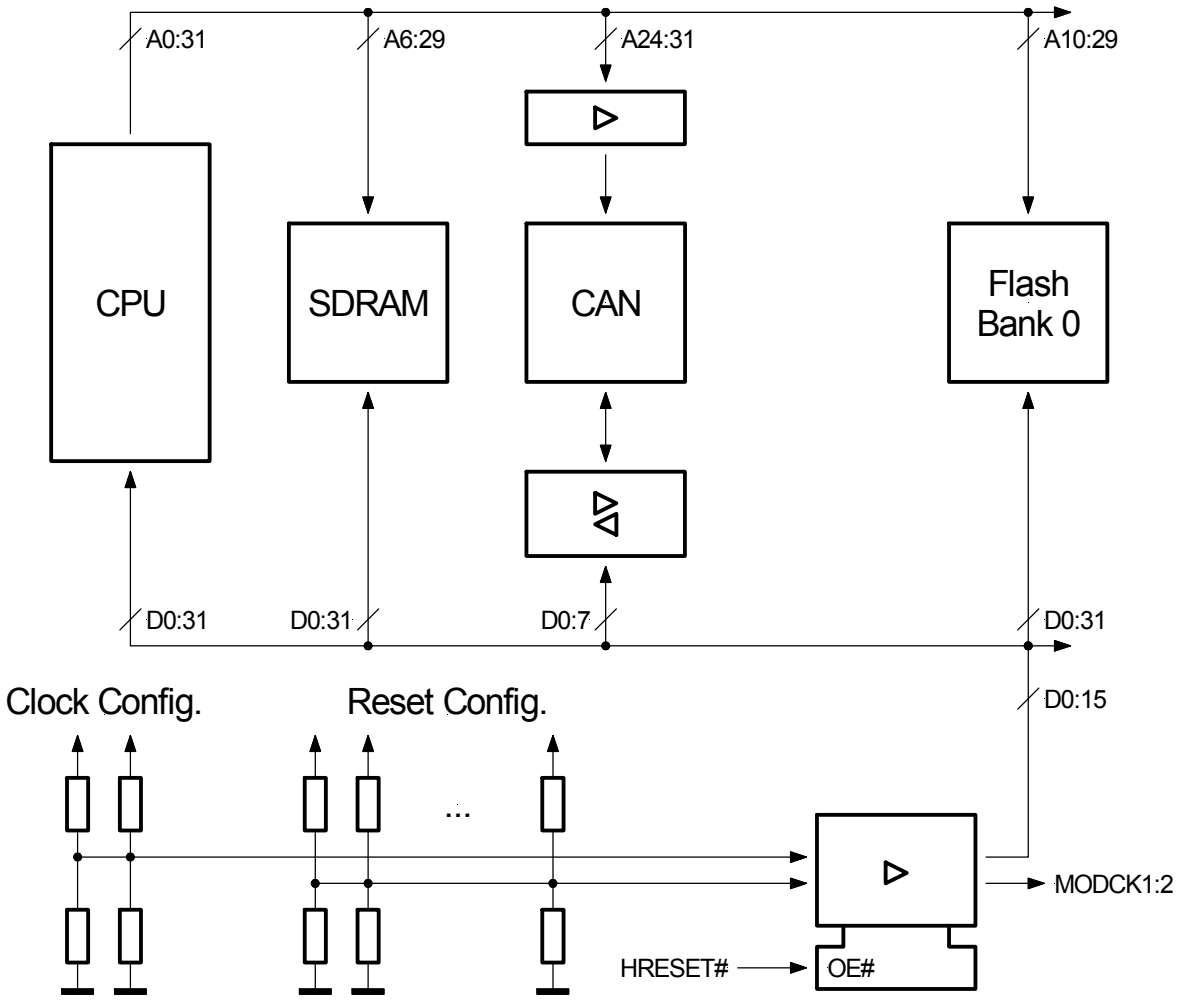

Illustration 6: Bus structure

3.2.11 Non-volatile memory (Flash)

There is one Flash bank on the module. Devices in BGA package with 16-bit bus width are used for it. The Flash devices are accessed directly by the CPU. No drivers are used.

- 4 to 64 MiByte
- One bank with 32-bit width
- Access times between 100 and 120 ns
- Used signals:
  CS_FLASH0#/CS0# (bootable) and CS_FLASH1#/CS1# if req.,
  OE#/GPL_AB1#, WE0#/BS_B0#, WE2#/BS_B2#
- Addressing via GPCM, the recommended timing is shown in the following tables

Table 14: Flash timing for 100 ns devices

Access type	Bus clock [MHz]	CSNT	ACS	SCY	TRLX	EHTR
Boot read	66	1	11b	15	1	0
Normal read / write			00b	3		1

Table 15: Flash timing for 120 ns devices

Access type	Bus clock [MHz]	CSNT	ACS	SCY	TRLX	EHTR
Boot read	66	1	11b	15	1	0
Normal read / write			00b	4		1

The status signal RY/BY# of the Flash is not used, i.e. the execution of write- and erase-cycles must be monitored by polling the Flash status bits (DQ7#, Toggle bits etc.).

Each of the two 16-bit wide Flashes of the 32-bit wide bank has only one write enable signal. The components can therefore only be written to (programmed) with 16 or 32-bit width.

Table 16: Flash devices

Component	Package	Model	Ext. Temp.	Manufacturer	Alternative manufacturer
S29AL016M90FFI020	FBGA64	MirrorBit Flash	yes	Spansion	–
S29GL016A10FFIR20	FBGA64	MirrorBit Flash	yes	Spansion	–
S29GL032A11FFIR20	FBGA64	MirrorBit Flash	yes	Spansion	–
S29GL064A11FFIR20	FBGA64	MirrorBit Flash	yes	Spansion	–
S29GL128N11FFI020	FBGA64	MirrorBit Flash	yes	Spansion	–
S29GL256N11FFI020	FBGA64	MirrorBit Flash	yes	Spansion	–

3.2.12 Dynamic read/write-memory (SDRAM)

Devices in a TSSOP54 package in 16-bit organisation are used as SDRAM.

- 16 – 128 MiByte
- One memory bank with 32-bit width
- Clock max. 66 MHz (66 and 132 MHz modules)
- Used signals:
  CS_SDRAM0# / CS2#
  GPL_AB0# (A10 SDRAM)
  OE#/GPL_AB1# (WE# SDRAM)
  GPL_AB2# (RAS# SDRAM)
  GPL_AB3# (CAS# SDRAM)
  BS_A0# (DQMU SDRAM, bits 0 … 7)
  BS_A1# (DQML SDRAM, bits 8 … 15)
  BS_A2# (DQMU SDRAM, bits 16 … 23)
  BS_A3# (DQML SDRAM, bits 24 … 31)
  CLKOUT
  CKE (only provided with pull-up)
- Addressing and refresh via UPMA
- CAS Latency 2

Depending on module variation and memory size 2 SDRAM devices with 64, 128, 256 or 512 MiBit are used. The variation-depending selection of address lines is realised with optional equipped 0Ω resistors.

The following access schemes are recommended:

Table 17: Access timing with CL = 2

CLKOUT	Single Read	Burst Read	Single Write	Burst Write	SDRAM type
66 MHz	4 + 1	4 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1+ 1	PC133

The configuration of the address signals of the SDRAM models is implemented as described in the following tables:

Table 18: Address multiplexing for SDRAMs

	Hardwired			multiplexed CPU-internal											
64 MiBit															
SDRAM	BA1	BA0	NC	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	8	9	7	10	11	12	13	14	15	16	17	18	19	20	21
non-mux	8	9	7	18	AP	20	21	22	23	24	25	26	27	28	29
128 MiBit															
SDRAM	BA1	BA0	NC	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	8	7	7	9	10	11	12	13	14	15	16	17	18	19	20
non-mux	8	7	7	18	AP	20	21	22	23	24	25	26	27	28	29
256 MiBit															
SDRAM	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	8	6	7	9	10	11	12	13	14	15	16	17	18	19	20
non-mux	8	6	7	18	AP	20	21	22	23	24	25	26	27	28	29
512 MiBit															
SDRAM	BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
mux	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
non-mux	5	6	7	18	AP	20	21	22	23	24	25	26	27	28	29

Table 19: SDRAM devices

Device	Package	Model	Ext. Temp.	Manufacturer	Alternative manufacturer
MT48LC4M16A2P-75	TSOP2 54	SDRAM 64MiBit	no	Micron	–
MT48LC4M16A2P-75L	TSOP2 54	SDRAM 64MiBit	no	Micron	–
MT48LC4M16A2P-8E	TSOP2 54	SDRAM 64MiBit	no	Micron	–
MT48LC4M16A2P-75IT	TSOP2 54	SDRAM 64MiBit	yes	Micron	–
MT48LC8M16A2P-75	TSOP2 54	SDRAM 128MiBit	no	Micron	–
MT48LC8M16A2P-75IT	TSOP2 54	SDRAM 128MiBit	yes	Micron	–
MT48LC16M16A2P-75	TSOP2 54	SDRAM 256MiBit	no	Micron	–
MT48LC16M16A2P-75L	TSOP2 54	SDRAM 256MiBit	no	Micron	–
MT48LC16M16A2P-75IT	TSOP2 54	SDRAM 256MiBit	yes	Micron	–
MT48LC32M16A2P-75	TSOP2 54	SDRAM 512MiBit	no	Micron	–
MT48LC32M16A2P-75IT	TSOP2 54	SDRAM 512MiBit	yes	Micron	–

3.2.13 Supply

The following voltages are used on the module:

Table 20: Supply voltages on the module

Voltage	Use
5V	CAN controller
3.3V	CPU, Flash, SDRAM, RTC, I^2C EEPROM, other logic
1.8V	CPU (Core)

3.2.13.1 Supply possibilities

The supply encloses the following function blocks:

- Step-down switching regulator from 3.3V to core voltage (1.8V)
- Power sequencing for 3.3V (I/O-Voltage)

Illustration 7 shows the structure of supply.

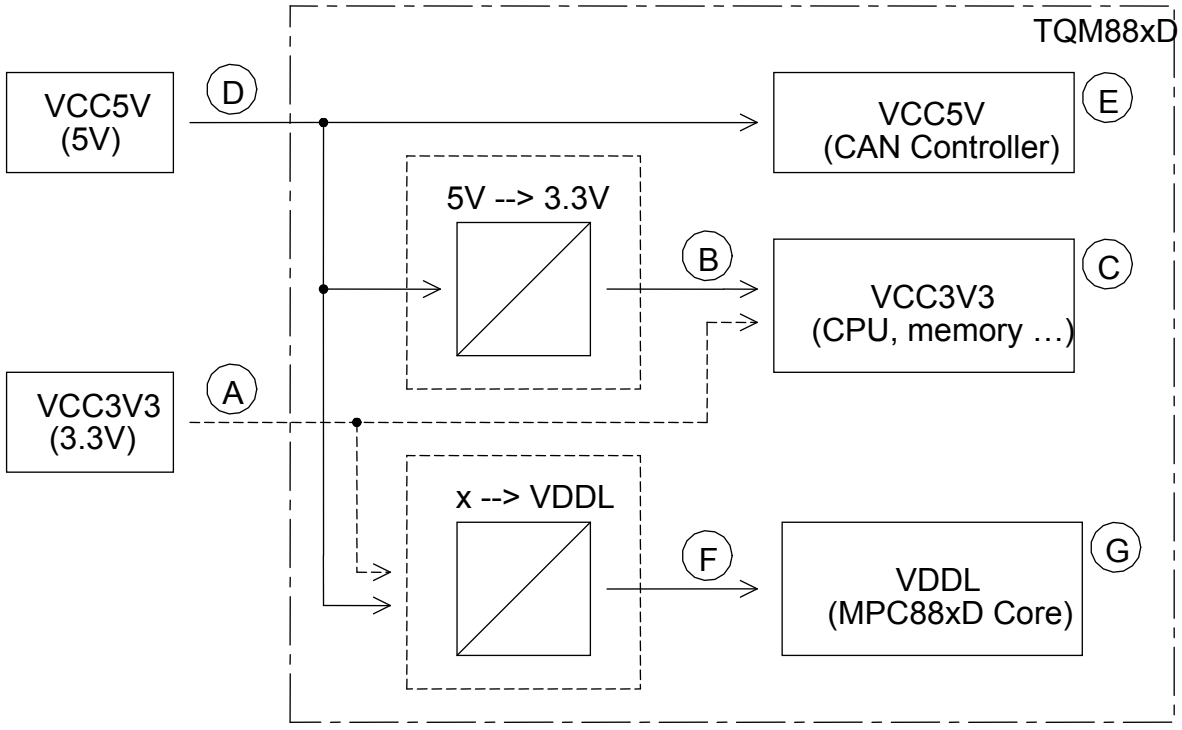

Illustration 7: Structure of supply

Depending on the module variation the following possibilities to supply the module exist:

- Supply 3.3V (without CAN controller)
- Supply 5V (with CAN controller)
- Supply 3.3V and 5V (with CAN controller)

The following maximum ratings apply for the supply voltages:

Table 21: Requirements for 5V external

Voltage VCC5VF	4.666V … 5.500V	Defined by the voltage range of devices and supervisor threshold
Ripple max.	50 mV	peak to peak
Current consumption	850 mA	typical

Table 22: Requirements for 3.3V external

Voltages VCC3V3IN and VCC3V3ID	3.219V … 3.465V	Defined by the voltage range of devices and supervisor threshold
Ripple max.	30 mV	peak to peak
Current consumption	1 A	typical

3.2.13.2 RTC supply

Table 23: Requirements for the RTC supply

Voltage VBAT	1.8V … 5.5V	Defined by the voltage range of RTC
Ripple max.	1 %	peak to peak
Current consumption	2 µA	VCC3V3IF = 0V, oscillator running

3.2.13.3 5V supply

- externally fed, requirements see >> ***Table 21***
- No additional load (e.g., for the supply of external devices) allowed

3.2.13.4 3.3V supply

- Main supply of the module
- No additional load (e.g., for the supply of external devices) allowed

3.3 Interfaces to other systems and devices

3.3.1 Download interface

- RxD und TxD
- Reset via the RS232 interface (RESIN#)
- additional input line of RS232 (ENMON#, status can be checked via a port pin)

The download interface is an extension of the serial interface for control purposes. It consists of five signals which exist merely on the connectors to the base board. On the Starterkit STK8xxL they are combined with the connector for SMC1.

Table 24: Download interface

Pin*	Signal name	Type	Function
6	ENMON#	I	Switch-over monitor / normal boot process
3	SMTXD1	O	TxD of debugging interface (SMC1, RS232 level)
5	GND	–	Ground
1	RESIN#	I	Reset input (master-reset of reset device)
2	SMRXD1	I	RxD of debugging interface (SMC1, RS232 level)

* On Starterkit STK8xxL

The switch-over signal ENMON# is implemented on the module by using port line PA15 and a (discretely designed) CMOS switch. This switch opens while the reset phase is active, so that a high-resistance coupling of the port line with ENMON# becomes active. After the reset phase the CMOS switch interconnects the port line with a delay of approx. 10 ms low-resistive outward. The CPU thereby has enough time to interpret the level during the reset phase.

3.3.2 RS232 transceiver

- Two internal UARTs
- Max. 115200 Baud
- Drivers with RS232 compatible levels
- All signals also available without driver
- Default assembly is 2 ∗ driver RxD / TxD

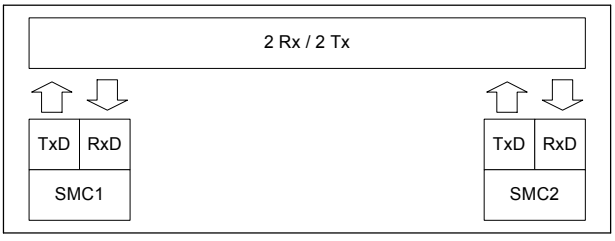

Illustration 8: Driver's structure of the RS232 interfaces

3.3.3 I²C bus

On the module two components are connected to the I²C bus:

- EEPROM
- RTC

Table 25: I²C bus addresses

Device	MSB				A2	A1	A0	LSB
Data EEPROM	1	0	1	0	0	0	0	R/W!
Real Time Clock	1	1	0	1	0	0	0	R/W!

The I²C bus is led out to the module connector.

3.3.4 BDM interface

All lines of the BDM interface (Debugging interface) are made available externally. Like the download interface the BDM interface is also led exclusively on the connectors to the base board. It is made up of the following signals:

Table 26: BDM interface

Pin*	Signal name	Type	Function
1	FRZ# (VFSL0)**	O	Freeze (CPU history buffer status)
2	SRESET#	I/O	Soft reset
3	DGND	–	Ground
4	DSCK/TCK	I	Clock
5	DGND	–	Ground
6	FRZ# (VFLS1)**	O	Freeze (CPU history buffer status)
7	HRESET#	I/O	Hard reset
8	DSDI/TDI	I	Data input
9	VCC3V3	–	Supply
10	DSDO/TDO	O	Data output

* On Starterkit STK8xxL

** Alternative configuration in brackets

3.4 Climate and operational conditions

Relative humidity (operation / storage): 10 … 90% (not condensing)

The possible temperature range strongly depends on the installation situation (loss of heat by heat conduction and convection); hence, no defined value of the whole subassembly can be given. In general a reliable operation is possible when the following conditions are fulfilled:

Version standard temperature range:	
Ambient temperature of CPU (min)	0 °C
Chip temperature of CPU (max.)	+70 °C
Package temperature of the remaining ICs	0 … +70 °C
Version extended temperature range:	
Ambient temperature of CPU (min)	-40 °C
Chip temperature of CPU (max.)	+85 °C
Package temperature of the remaining ICs	-40 … +85 °C

Protection level: IP00 (No protection against objects and humidity)

3.5 Reliability and service life

The subassembly is designed for a service life of 10 years. It was also designed to be insensitive to vibration and impact.

3.6 Environment protection

By environmentally friendly processes, production equipment and products we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way that it can be easily repaired and disassembled on account of modular construction.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Because at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.

We aspire to avoid the use of PCB containing capacitors and transformers (polychlorinated biphenyls) where possible.

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94 (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96 (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98 (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01 (source of information: BGBl I 2001, 3379)

4. Software

4.1 Monitor software

On the TQM885D modules the monitor program MON8xx is the basic software which is installed by default. After connecting a serial interface and applying power to the Starterkit STK8xxL it enables the communication with the module. The MON8xx provides basic functions for the initial operation of the TQM8xxL. These are made up of the ranges:

- Monitor functions:
  Memory and register monitor for addressing memory and the registers of the MPC8xx, extension possibilities for addressing of further– also external – memory mapped I/Os. Simple I/O functions are available like memory edit, dump, register modify, as well as the possibility to load S-Record files to RAM or Flash.
- Automatic start of applications:
  After a reset the monitor or an application / an operating system can be started alternatively. When the MON885D is started it polls the port pin which is routed to the debug interface (signal ENMON#), and forks alternatively to the monitor, or starts an application or an operating system.

The specification of the MON8xx is described in a separate document.

5. Installation

5.1 Safety requirements and protective regulations

5.1.1 EMV requirements

The module was developed carefully according to the requirements of electromagnetic compatibility (EMV). Depending on the target system, measures for filtering can still be necessary to guarantee to meet the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- With metal casings a good (at least according to RF) connection to the printed circuit board or to the potential of the housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding
- Filtering of all signals which can be connected externally (also "slow" and DC can radiate RF indirectly)

5.1.2 ESD requirements

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the base board, no special preventive measures were planned on the module. According to the data sheets, the used devices already have some protection; however, this is generally not sufficient to fulfil the legal requirements without any further measures.

Following measures are recommended:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Z-diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

5.1.3 Operational safety and personal protection

On account of the present voltages (≤ 5V DC) a separate verification can be omitted.

5.2 Mechanics specification TQM885D

5.2.1 General information

- Double row, high pole SMD plug connectors with 0.8 mm pitch, 2 ∗ 120 pin and 1 ∗ 40 pin
- The combination with different mating plugs allows different stacking heights in order to adapt to the parts mounted on the base board (main board)
- Double-sided SMD mounting
- 10-layered multilayer in micro via technology

5.2.2 Module connectors

Possibilities for board-to-board connection with 120 pin and 40 pin connectors with 0.8 mm pitch:

Table 27: Module connectors

Board distance	Module connector				Base board connector		
	Qty.	Pins	Supplier	Order-no.	Pins	Supplier	Order-no.
5 mm	1	40	tyco	177983-1	40	tyco	177984-1
6 mm					40	tyco	179029-1
7 mm					40	tyco	179030-1
8 mm					40	tyco	179031-1
5 mm	2	120	tyco	177983-5	120	tyco	177984-5
6 mm					120	tyco	179029-5
7 mm					120	tyco	179030-5
8 mm					120	tyco	179031-5

As an alternative connectors from company Berg are available.

5.2.3 Dimensions

- Board dimensions: 54 mm ∗ 44 mm
- Height: a + b + c = 10.6 mm
- Free space under the module: a – d = 2.6 mm

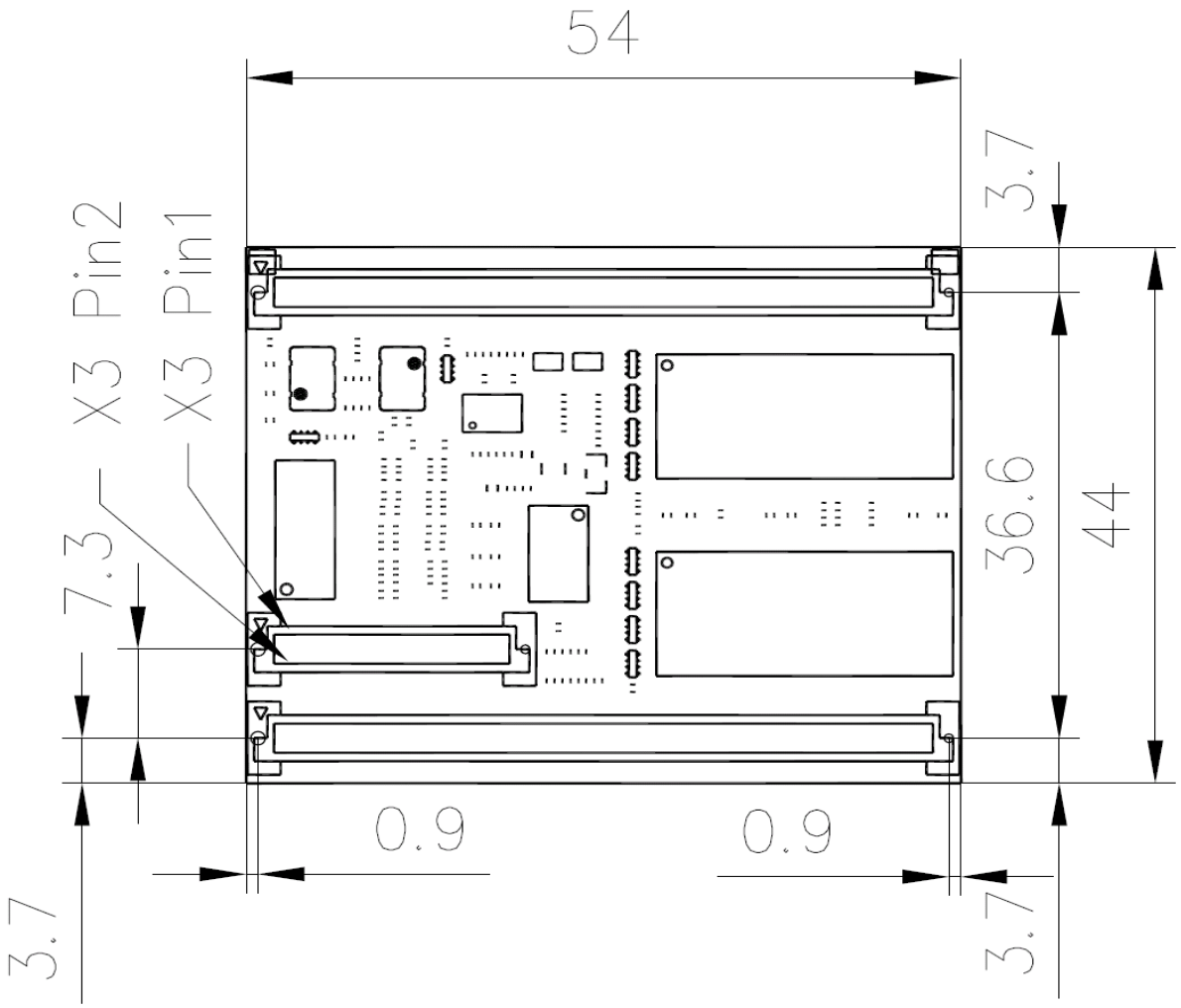

Illustration 9: Top view through pc-board (TQM885D)

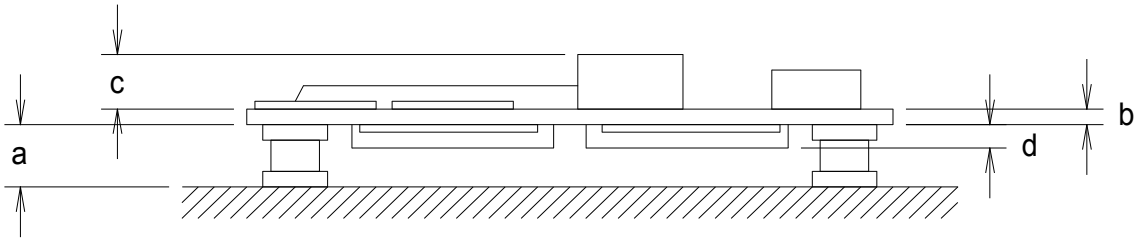

Illustration 10: Heights (not to scale of TQM885D)

Table 28: Height measures

Dimension	Value [mm]	Remark
A	5.0 ± 0.2	Combination module connector with mating plug; 6, 7 and 8 mm are also possible with different connectors on base board
B	1.5 ± 0.15	PC-board
C	3.5 ± 0.5	Storage coil (highest part on top side)
D	2.35 max.	(Highest part on underside)

5.2.4 Tips of treatment

To remove the module safely from base boards the extraction tool MOZI8xxL delivered with the Starterkit is recommended.

6. Configuration

6.1 Module connector

6.1.1 Pin configuration X1

Table 29: Pin configuration X1

Pin-no. Module connector	Processor ball	Port	Port pin function 1	Port pin function 2	Port pin function 3	Port pin function 4	Port pin function 5
X1-1	no CPU	GND					
X1-2	N4	IRQ0#					
X1-3	P3	IRQ1#					
X1-4	B10	IRQ2#	RSV#				
X1-5	n.c.						
X1-6	n.c.						
X1-7	n.c.						
X1-8	n.c.						
X1-9	P4	IRQ7#					
X1-10	A2	WAIT_A#		SOC_Split			
X1-11	B7	ALE_A					
X1-12	B1	IP_A0		UTPB_Split[0]			
X1-13	C1	IP_A1		UTPB_Split[1]			
X1-14	F4	IP_A2		UTPB_Split[2]	IOIS16_A#		
X1-15	E3	IP_A3		UTPB_Split[3]			
X1-16	D2	IP_A4		UTPB_Split[4]			
X1-17	D1	IP_A5		UTPB_Split[5]			
X1-18	E2	IP_A6		UTPB_Split[6]			
X1-19	D3	IP_A7		UTPB_Split[7]			
X1-20	C6	OP1					
X1-21	B6	OP0		UtpClk_Split			
X1-22	D6	OP2	MODCK1	STS#			
X1-23	A6	OP3	MODCK2	DSDO			
X1-24	C3	WAIT_B					

Pin-no. Module connector	Processor ball	Port	Port pin function 1	Port pin function 2	Port pin function 3	Port pin function 4	Port pin function 5
X1-25	D8	ALE_B	DSCK	AT1			
X1-26	B8	IP_B7	PTR#	AT3			
X1-27	A8	IP_B6	DSDI	AT0			
X1-28	A10	IP_B5	LWP1	VF1			
X1-29	B9	IP_B4	LWP0	VF0			
X1-30	C9	IP_B3	IWP2	VF2			
X1-31	C8	IP_B2	IOIS16_B#	AT2			
X1-32	D9	IP_B1	IWP1	VFLS1			
X1-33	A9	IP_B0	IWP0	VFLS0			
X1-34	no CPU	RESIN#					
X1-35	B3	PORESET#					
X1-36	C4	TEXP					
X1-37	B4	HRESET#					
X1-38	D4	RSTCONF#					
X1-39	A5	EXTCLK					
X1-40	G4	CLKOUT					
X1-41	no CPU	ENMON#					
X1-42	A3	SRESET#					
X1-43	no CPU	JTAG / BDM#					
X1-44	no CPU	HRESETF#					
X1-45	no CPU	CKE					
X1-46	n.c.						
X1-47	n.c.						
X1-48	no CPU	TX0_CAN1					
X1-49	no CPU	RX0_CAN1					
X1-50	no CPU	SMRXD2					
X1-51	no CPU	SMTXD2					
X1-52	no CPU	SMRXD1					
X1-53	no CPU	SMTXD1					
X1-54	B15	CE1_A#					
X1-55	C15	CE2_A#					
X1-56	D17	BS_A0#					
X1-57	C18	BS_A1#					
X1-58	C19	BS_A2#					
X1-59	F16	BS_A3#					
X1-60	B13	GPL_A4#	UPWAITA				
X1-61	A14	GPL_B4#	UPWAITB				
X1-62	C13	GPL_A5#					
X1-63	A13	BDIP#	GPL_B5#				
X1-64	B16	CS7#	CE2_B#				
X1-65	D15	CS6#	CE1_B#				
X1-66	A16	CS5#					
X1-67	C16	CS4#					
X1-68	D14	CS3#					

Pin-no. Module connector	Processor ball	Port	Port pin function 1	Port pin function 2	Port pin function 3	Port pin function 4	Port pin function 5
X1-69	A15	CS2#					
X1-70	C14	CS1#					
X1-71	B14	CS0#					
X1-72	B17	GPL_A0#	GPL_B0#				
X1-73	A18	GPL_A1#	GPL_B1#	OE#			
X1-74	D16	GPL_A2#	GPL_B2#	CS2#			
X1-75	A17	GPL_A3#	GPL_B3#	CS3#			
X1-76	B18	WE0#	BS_B0#	IORD#			
X1-77	E16	WE1#	BS_B1#	IOWR#			
X1-78	C17	WE2#	BS_B2#	PCOE#			
X1-79	B19	WE3#	BS_B3#	PCWE#			
X1-80	D18	A31					
X1-81	F18	A30					
X1-82	G18	A29					
X1-83	E18	A28					
X1-84	H19	A27					
X1-85	D19	A26					
X1-86	F19	A25					
X1-87	H16	A24					
X1-88	G17	A23					
X1-89	F17	A22					
X1-90	G19	A21					
X1-91	H17	A20					
X1-92	H18	A19					
X1-93	E19	A18					
X1-94	J16	A17					
X1-95	J18	A16					
X1-96	J17	A15					
X1-97	J19	A14					
X1-98	K16	A13					
X1-99	K17	A12					
X1-100	K18	A11					
X1-101	K19	A10					
X1-102	L18	A9					
X1-103	L17	A8					
X1-104	L19	A7					
X1-105	L16	A6					
X1-106	M18	A5					
X1-107	M17	A4					
X1-108	M19	A3					
X1-109	N19	A2					
X1-110	N18	A1					
X1-111	M16	A0					
X1-112	no CPU	VCC3V3					

Pin-no. Module connector	Processor ball	Port	Port pin function 1	Port pin function 2	Port pin function 3	Port pin function 4	Port pin function 5
X1-113	no CPU	VCC3V3					
X1-114	no CPU	VCC3V3					
X1-115	no CPU	GND					
X1-116	no CPU	VCC5V					
X1-117	no CPU	GND					
X1-118	no CPU	VCC5V					
X1-119	no CPU	GND					
X1-120	no CPU	VCC5V					

6.1.2 Pin configuration X2

Table 30: Pin configuration X2

Pin-No. Module connector	Processor ball	Port	Port-Pin function 1	Port-Pin function 2	Port-Pin function 3	Port-Pin function 4	Port-Pin function 5
X2-1	no CPU	VBAT					
X2-2	no CPU	GND					
X2-3	T9	PD3		CLK7	SOC	TIN4	
X2-4	W4	PD4		CLK4	UTPB7		
X2-5	V6	PD5		CLK8	UTPB6	L1TCLKB	
X2-6	W5	PD6		RTS4#	UTPB5		
X2-7	W3	PD7		RTS3#	UTPB4		
X2-8	R3	PD8	MII-MDC	RXD4	RMII-MDC		
X2-9	U2	PD9		TXD4	UTPCLK		
X2-10	T2	PD10		TXD3	TXENB#		
X2-11	R2	PD11		RXD3	RXENB#		
X2-12	U5	PD12		UTPB3	L1RSYNCB		
X2-13	U6	PD13		UTPB2	L1TSYNCB		
X2-14	U7	PD14		UTPB1	L1RSYNCA		
X2-15	U8	PD15		UTPB0	L1TSYNCA		
X2-16	W10	PC4	CD3#		L1RSYNCA		
X2-17	T10	PC5	CTS3#	SDACK2	L1TSYNCA		
X2-18	U11	PC6	CD4#	USBTXN	L1RSYNCB		
X2-19	V12	PC7	CTS4#	USBTXP	L1TSYNCB		
X2-20	W14	PC8	CD2#	TGATE2#			
X2-21	T14	PC9	CTS2#				
X2-22	U15	PC10	USBRXN	TGATE1#			
X2-23	V16	PC11	USBRXP				
X2-24	T18	PC12		MII1-TXD2		TOUT1#	
X2-25	V10	PC13		MII1-TXD3		SDACK1#	
X2-26	R18	PC14	DREQ1#	L1ST2			RTS2#
X2-27	R19	PC15	DREQ0#	L1ST1	TxClav	RxClav	RTS3#
X2-28	U3	PA0		MII1-RXD1	RMII1-RXD1	TOUT4#	
X2-29	U1	PA1		MII1-RXD0	RMII1-RXD0	BRGO4	
X2-30	T4	PA2	TXD4	MII1-RXDV	RMII1-		

Pin-No. Module connector	Processor ball	Port	Port-Pin function 1	Port-Pin function 2	Port-Pin function 3	Port-Pin function 4	Port-Pin function 5
					CRS_DV		
X2-31	W2	PA3		MII1-RXER	RMII1-RXER	BRGO3	
X2-32	U4	PA4	CTS4#	MII1-TXD1	RMII1-TXD1		
X2-33	W13	PA5	CLK3	L1TCLKA	BRGO2	TIN2	
X2-34	U13	PA6	CLK2			TOUT1#	
X2-35	V14	PA7	CLK1	L1RCLKA	BRGO1	TIN1	
X2-36	W15	PA8	TXD3	L1RXDA			
X2-37	T15	PA9	RXD3	L1TXDA			
X2-38	W17	PA10	CLK7	MII1-TXER		TIN4	
X2-39	W9	PA11	RXD4	MII1-TXD0	RMII1-TXD0		
X2-40	P16	PA12	TXD2				
X2-41	W11	PA13	RXD2				
X2-42	P17	PA14	USBOE#				
X2-43	N16	PA15	USBRXD				
X2-44	T16	TDI	DSDI				
X2-45	T17	TDO	DSDO				
X2-46	U17	TCK	DSCK				
X2-47	V18	TMS					
X2-48	U18	PB14		RXADDR2	TXADDR2		
X2-49	U10	PB15		BRGO3	TxClav	RxClav	
X2-50	V11	PB16	RTS4#	RXADDR0	TXADDR0	L1RQa#	PHREQ0
X2-51	W12	PB17	BRGO2	RXADDR1	TXADDR1	L1ST3	PHREQ1
X2-52	T12	PB18	RTS2#	RXADDR4	TXADDR4	L1ST2	
X2-53	V13	PB19	RTS4#	MII1-RXD3			
X2-54	T13	PB20	SMRXD2	TXADDR0	RXADDR0	L1CLKOA	PHSEL0
X2-55	U14	PB21	SMTXD2	TXADDR1	RXADDR1	BRGO1	PHSEL1
X2-56	V15	PB22	SMSYN2#	TXADDR4	RXADDR4	SDACK2#	
X2-57	W16	PB23	SMSYN1#	TXADDR2	RXADDR2	SDACK1#	
X2-58	U16	PB24	SMRXD1	TXADDR3	RXADDR3		
X2-59	V17	PB25	SMTXD1	RXADDR3	TXADDR3		
X2-60	R17	PB26	I2CSCL	BRGO2			
X2-61	U19	PB27	I2CSDA	BRGO1			
X2-62	V19	PB28	SPIMISO	BRGO4			
X2-63	T19	PB29	SPIMOSI				
X2-64	P18	PB30	SPICLK				
X2-65	V3	PB31	SPISEL#	MII1-TXCLK	RMII1-REFCLK		
X2-66	A7	BADDR30	REG#				
X2-67	B5	BADDR29					
X2-68	C5	BADDR28					
X2-69	D7	AS#					
X2-70	A11	IRQ3#	CR#				
X2-71	D10	IRQ6#	FRZ				
X2-72	C7	IRQ4#	KR#	RETRY#	SPKROUT		
X2-73	D13	RD	WR#				

Pin-No. Module connector	Processor ball	Port	Port-Pin function 1	Port-Pin function 2	Port-Pin function 3	Port-Pin function 4	Port-Pin function 5
X2-74	C11	BG#					
X2-75	B11	BB#					
X2-76	D11	BR#					
X2-77	C12	TA#					
X2-78	G16	TSIZ0	REG#				
X2-79	E17	TSIZ1					
X2-80	B12	TEA#					
X2-81	D12	BI#					
X2-82	C10	BURST#					
X2-83	A12	TS#					
X2-84	U12		MII1_COL				
X2-85	T5		MII1_TX_EN				
X2-86	P19		MII_MDIO				
X2-87	T11		MII1_CRS				
X2-88	P2	D0					
X2-89	M1	D1					
X2-90	L1	D2					
X2-91	K2	D3					
X2-92	N1	D4					
X2-93	K4	D5					
X2-94	H3	D6					
X2-95	F2	D7					
X2-96	P1	D8					
X2-97	L4	D9					
X2-98	L3	D10					
X2-99	L2	D11					
X2-100	N3	D12					
X2-101	N2	D13					
X2-102	K3	D14					
X2-103	K1	D15					
X2-104	J2	D16					
X2-105	M4	D17					
X2-106	J1	D18					
X2-107	J3	D19					
X2-108	H2	D20					
X2-109	H1	D21					
X2-110	J4	D22					
X2-111	M3	D23					
X2-112	G2	D24					
X2-113	G1	D25					
X2-114	G3	D26					
X2-115	M2	D27					
X2-116	H4	D28					
X2-117	F1	D29					

Pin-No. Module connector	Processor ball	Port	Port-Pin function 1	Port-Pin function 2	Port-Pin function 3	Port-Pin function 4	Port-Pin function 5
X2-118	E1	D30					
X2-119	F3	D31					
X2-120	no CPU	GND					

6.1.3 Pin configuration X3

Table 31: Pin configuration X3

Pin-No. Module connector	Processor ball	Port	Port-Pin function 1	Port-Pin function 2	Port-Pin function 3	Port-Pin function 4	Port-Pin function 5
X3-1	Non CPU	GND					
X3-2	Non CPU	GND					
X3-3	T1	PE26	MII2-RXDV		RMII2-CRS_DV	L1CLKOB	
X3-4	Non CPU	RTC-Alarm					
X3-5	R1	PE18	MII2-TXD3	SMTXD1		L1TSYNCA	
X3-6	V1	PE22	MII2-RXD1	SDACK1#	RMII2-RXD1	TOUT2#	
X3-7	T3	PE25	MII2-RXD3	RXD4		L1ST2	
X3-8	V2	PE23	MII2-RXCLK	SMSYN2#	TXD4	L1ST1	
X3-9	R4	PE20	MII2-TXER	SMTXD2		L1RSYNCA	CTS3#
X3-10	V4	PE27	MII2-RXER	RTS3#	RMII2-RXER	L1RQB	
X3-11	Non CPU	GND					
X3-12	Non CPU	GND					
X3-13	V5	PE28	MII2-COL			TOUT3#	
X3-14	W6	PE15	MII2-TXD1	TGATE1#	RMII2-TXD1		
X3-15	T6	PE19	MII2-TXEN		RMII2-TXEN	L1TXDB	
X3-16	V7	PE14	MII2-TXD0	RXD3	RMII2-TXD0		
X3-17	W7	PE30	MII1-RXD2		L1RXDB		
X3-18	V8	PE24	MII2-RXD2	SMRXD1		BRGO1	
X3-19	T7	PE16	MII2-TXCLK	TXD3	RMII2-REFCLK	L1RCLKB	CLK6
X3-20	W8	PE17	MII2-TXD2	SMSYSN1#	CLK5	BRGO3	TIN3
X3-21	Non CPU	GND					
X3-22	Non CPU	GND					
X3-23	T8	PE29	MII2-CRS				
X3-24	U9	PE31	MII1-RXCLK	CLK8	L1TCLKB		
X3-25	Reserve						
X3-26	V9	PE21	MII2-RXD0	SMRXD2	RMII2-RXD0	TOUT1#	RTS3#
X3-27	Reserve						
X3-28	Reserve						
X3-29	Reserve						
X3-30	Reserve						
X3-31	Non CPU	GND					
X3-32	Non CPU	GND					
X3-33	Reserve						
X3-34	Reserve						
X3-35	Reserve						

Pin-No. Module connector	Processor ball	Port	Port-Pin function 1	Port-Pin function 2	Port-Pin function 3	Port-Pin function 4	Port-Pin function 5
X3-36	Reserve						
X3-37	Reserve						
X3-38	Reserve						
X3-39	Reserve						
X3-40	Reserve						

7. Attachment

7.1 Literature

[1] MPC885DRM Rev. 1 MPC885D/MPC880 User Manual Freescale

[2] MPC885DEC Rev. 3 MPC885D/MPC880 Hardware Specifications Freescale

[3] MPC885DRMAD Rev. 0 Errata to the MPC885D Freescale

[4] TQM885D.Varianten.0101B Variation key TQS