

For Technology  
in Quality



# **User's Manual**

## **TQM8360L**

**TQM8360L UM 104**

**29.10.2010**

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## Revision history

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# 1. About this manual

## 1.1 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.


## 1.2 Terms and conventions

| Symbol / Tag               | Meaning   |
|----------------------------|---|
|                            | This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed with the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V. |
|                            | This symbol indicates the possible use of voltages greater than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.                        |
|                            | This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.  |
| <b>! note !</b>            | This symbol represents important details or aspects for working with TQ-products.   |
| <b>Filename.ext</b>        | This specification is used to state the complete file name with its corresponding extension.  |
| Instructions /<br>Examples | Examples of an application. e.g., <ul style="list-style-type: none"> <li>• specifying memory partitions</li> <li>• processing a script</li> <li>• .....</li> </ul>  |
| <b>Reference</b>           | Cross-reference to another section, figure or table.  |


Table 1: Terms and conventions

### 1.3 Handling and ESD tips

#### General handling of your TQ-products

|   |  |
|---|--|
|  | <p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is: not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the system's power supply is switched off.</p> <p>Violation of this guideline may result in damage / destruction of the module and be dangerous to your health.</p> <p>Improper handling of your TQ-product renders the guarantee invalid.</p> |
|---|--|

#### Proper ESD handling

|  |  |
|--|--|
|  | <p>The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).</p> <p>Always wear antistatic clothing and use ESD-safe tools, packing materials etc. and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.</p> |
|--|--|

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## 1.5 Imprint

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## 1.8 Acronyms and definitions

The following terminology and abbreviations are used:

| Acronym          | Meaning   |
|------------------|---|
| BGA              | Ball Grid Array                                     |
| BMS              | Boot Memory Space                                   |
| CIB              | Configuration Information Block                     |
| COP              | Common on-chip processor                            |
| CPU              | Central Processing Unit                             |
| CE               | Communication Engine (= QUICC Engine)               |
| DDR              | Double Data Rate                                    |
| DUART            | Dual Universal Asynchronous Receiver/Transmitter    |
| ECC              | Error Correction Code                               |
| EEPROM           | Electrically Erasable Programmable Read-Only Memory |
| EMC              | Electromagnetic Compatibility                       |
| ESD              | Electrostatic Discharge                             |
| FR-4             | Flame Retardant-4                                   |
| GMII             | Gigabit Media Independent Interface                 |
| I <sup>2</sup> C | Inter-Integrated Circuit                            |
| IP00             | Ingress Protection 00                               |
| JTAG             | Joint Test Action Group                             |
| LED              | Light Emitting Diode                                |
| LSB              | Least Significant Bit                               |
| MII              | Media Independent Interface                         |
| MOZI             | Module extractor (Modulzieher)                      |
| MSB              | Most Significant Bit                                |
| PCI              | Peripheral Component Interconnect                   |
| PLL              | Phase-Locked Loop                                   |
| QUICC            | Quad Integrated Communications Controller           |
| RAM              | Random Access Memory                                |
| RGMII            | Reduced Gigabit Media Independent Interface         |
| RMII             | Reduced Media Independent Interface                 |
| ROM              | Read Only Memory                                    |
| RTC              | Real Time Clock                                     |
| SDRAM            | Synchronous Dynamic Random Access Memory            |
| SMD              | Surface Mounted Device                              |
| TBGA             | Tape Ball Grid Array                                |
| TSEC             | Three-speed Ethernet controller                     |
| TSOP             | Thin Small-Outline Package                          |
| UART             | Universal Asynchronous Receiver/Transmitter         |
| UPM              | User Programmable Machine                           |

Table 2: Acronyms

## 2. Brief description

The TQM8360L is a universal Minimodule with Freescale's PowerPC CPU MPC8360E. It complements the PowerPC product family in the range of middle to high computing performance and is in addition to the TQM8349L the second module of a new family which is based on the MPC83xx CPUs.

From its calculation power the used PowerQUICC II Pro (MPC83xx) is situated between PowerQUICC II (MPC82xx, TQM82xx modules) and PowerQUICC III (MPC85xx, TQM85xx modules).

In comparison to the TQM8349L it offers the following additional features:

- Communication processor module with QUICC-engine
- Up to eight Ethernet interfaces with 10/100 Mbit/s or up to two 10/100/1000 Mbit/s possible
- DDR2 instead of DDR-SDRAM

On account of extensive compatibility of the pinouts and the mechanics to the TQM85xx family the same development environment (Starterkit STK85xx) can be used for the following modules:

- TQM8540, TQM8560, TQM8541, TQM8555
- TQM8347E, TQM8349E
- TQM8358E, TQM8360E (the module described here)
- Future derivatives in the range of PowerQUICC III and beyond it

All pins of the microprocessor are led through to the module plug connectors. There are therefore no restrictions for customers using a module with respect to an integrated customised design.

### 3. Technical data

#### 3.1 Overview

##### 3.1.1 Block diagram

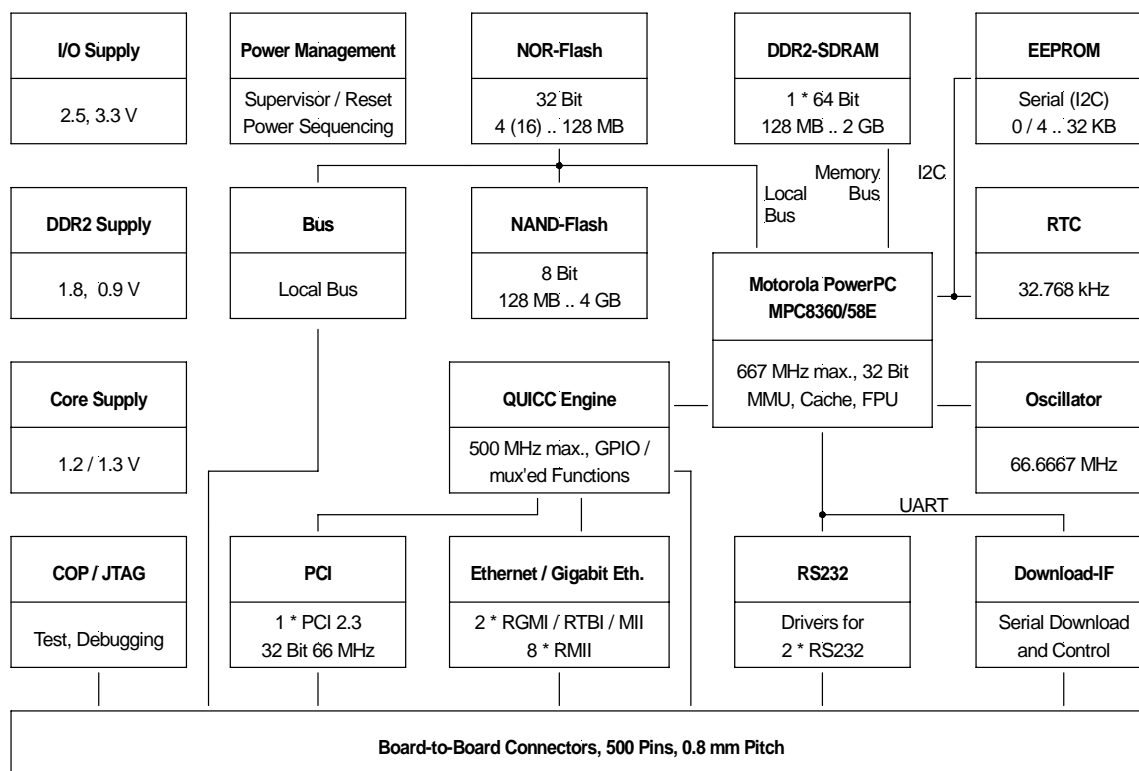


Illustration 1: Block diagram

##### 3.1.2 System components

- CPU MPC8360E, MPC8358E (TBGA)
- Oscillator for CPU
- Power fail logic
- DC/DC converter
- DDR2-SDRAM
- NOR flash, NAND flash
- EEPROM
- RTC
- Driver for two serial interfaces
- COP/JTAG interface
- Board-to-board connector system

## 3.2 Electronics

### 3.2.1 CPU

The module can be equipped with the MPC8360E as well as with the MPC8358E. The MPC8358E differs from the MPC8360E in that it only supports one PCI bus with a width of 32 bit. The pin compatibility of the CPUs is given; the MPC8358E forms a subset of the MPC8360E.

Provided that nothing else is mentioned, the name MPC8360E also stands for the MPC8358E.

The MPC8360E offers numerous interfaces. Special attention is to be dedicated to the following interfaces on account of the high data rates.

#### 3.2.1.1 Three-Speed Ethernet Controller (TSEC)

All relevant pins of the TSECs are led through to the module plug connectors, so that all interface modes supported by the CPU can be used according to own discretion. For RF-technical reasons PHY and transformer have to be placed on the base board.

- GMII-/MII mode:  
Maximum frequency to be transmitted 125 MHz (Tx clock and Rx clock)
- RGMII mode:
  - Maximum frequency to be transmitted 125 MHz (Tx clock and Rx clock)
  - Lower number of signals than with GMII / MII
  - Timing narrower than with GMII / MII, because both clock edges are used

### 3.2.2 Reset logic

The reset logic contains the following functions:

- Monitoring of the voltages used on the module as follows:  
3.3 V, 2.5 V, 1.8 V, VDD (1.2 V)
- VREF (DDR2-SDRAM) not monitored, monitoring optionally possible
- External reset input
- Reset state indicated by LED (HRESET# low  $\Rightarrow$  LED lights up)

#### 3.2.2.1 Tolerance and reset trigger level for 3.3 V

Tolerance range of the fed supply voltage:

$$V_{CC3V3ID} = 3.067 \text{ V} \dots 3.600 \text{ V} = 3.3 \text{ V} -7.1 \% / +9.1 \%$$

Permitted voltage range for CPU and 3.3 V logic:

$$V_{CC3V3} = 3.0 \text{ V} \dots 3.6 \text{ V}$$

Tolerance of the voltage supervision, voltage drop in VCC3V3 taken into consideration:

$$V_{Reset} = 3.003 \text{ V} \dots 3.067 \text{ V}$$

Excess voltage monitoring is optionally possible.

### 3.2.2.2 Optional supervision VREF

The reference voltage VREF for DDR2 can be monitored optionally. The integrated monitoring device must be configured suitably.

### 3.2.2.3 Reset-LED

- LED is controlled via this SRESET#-Signal, SRESET# low ⇒ LED lights up.
- SRESET# is set to the same state as, and controlled by PORESET# and HRESET# within the CPU → LED also lights up, when PORESET# and / or HRESET# low; details see [1].
- The luminous duration of the LED is extended by approx. 100 ms to ensure the visibility with very short reset pulses, e.g., with an internal reset.

### 3.2.2.4 JTAG reset TRST#

- TRST# must be pulled low by PORESET# when PORESET# is set low, but still be able to be triggered separately (COP/JTAG debugging).
- The used circuit is shown in the following illustration.

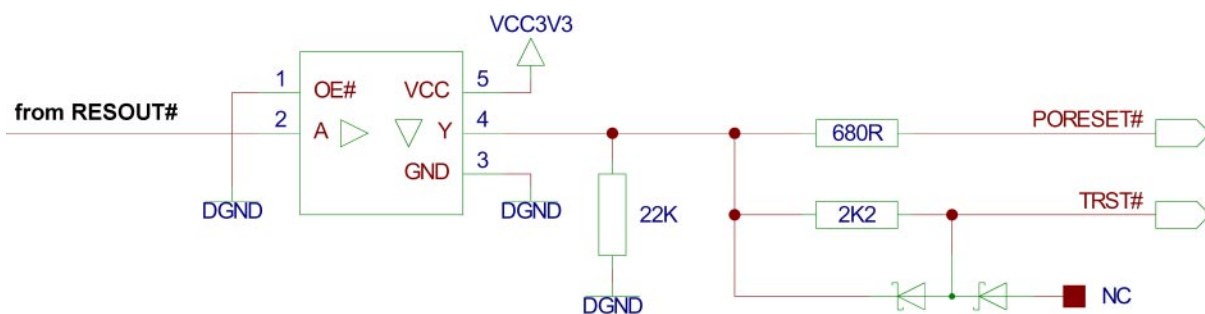


Illustration 2: Wiring of TRST# on the TQM8360L

3.2.3 Reset configuration

3.2.3.1 Choice of the configuration source

- Encoded configuration information must be applied externally to the module pins (SEL\_RESET\_SOURCE and SEL\_CLKIN\_DIV)
- PLD takes over and decodes the data
- PLD supplies configuration signals CFG\_RESET\_SOURCE[0:2] and CFG\_CLKIN\_DIV to the CPU as a function of HRESET#

| Module signal    | CPU signal at reset   | Configuration  |
|------------------|-----------------------|--|
| SEL_CLKIN_DIV    | CFG_CLKIN_DIV         |  |
| 0                | 0                     | CLKIN : PCI_SYNC_OUT = 1 : 1 (TQ default)                                  |
| 1                | 1                     | CLKIN : PCI_SYNC_OUT = 2 : 1   |
| SEL_RESET_SOURCE | CFG_RESET_SOURCE[0:2] |  |
| 0                | 0b000                 | Local bus  |
| 1                | 0b010                 | I <sup>2</sup> C-EEPROM, high speed (TQ default)                           |
| Z                | 0b001                 | I <sup>2</sup> C-EEPROM, low speed<br>(not recommended, use 0b010 instead) |

Table 3: Configuration signals

3.2.3.2 Power-on reset configuration from I<sup>2</sup>C-EEPROM

- Simply alterable by the CPU itself, e.g., for the adaptation of the TSEC modes
- Special I<sup>2</sup>C bus reset sequence prevents problems with stuck I<sup>2</sup>C bus by transmitting a special I<sup>2</sup>C bus reset sequence

3.2.3.3 Power-on reset configuration from flash

- Alternative to reset configuration from I<sup>2</sup>C-EEPROM
- Updates are more difficult (only complete sectors of the flash can be deleted, reset configuration is stored in the same sector as the MON83xx or other boot loader)  
→ to use this feature please contact the TQC support
- Possible use, e.g. for a default configuration (factory setting), if configuration data in the I<sup>2</sup>C-EEPROM is invalid

### 3.2.3.4 Reset configuration in detail

By updating the configuration EEPROM all settings can be customised according to the requirements of the respective application. The following table shows the configurable settings of the CPU. The possible values are described in [1].

| Reset conf. name | Register bit(s) meaning                | Factory default* | SW writable |
|------------------|--|------------------|-------------|
| LBIUCM           | Local bus memory controller clock mode | 0                | -           |
| DDRCM            | DDR SDRAM memory controller clock mode | 0                | -           |
| SPMF[0:3]        | System PLL multiplication factor       | 0b0100           | -           |
| COREPLL[0:6]     | Core PLL configuration                 | 0b0000100        | -           |
| CEVCOD[0:1]      | QUICC engine PLL VCO division          | 0b10             | -           |
| CEPDF            | QUICC engine PLL division factor       | 0                | -           |
| CEPMF[0:4]       | QUICC engine PLL multiplication factor | 0b00110          | -           |
| PCIHOST          | PCI host mode                          | 1                | -           |
| PCIARB           | PCI internal arbiter mode              | 1                | +           |
| PCICKDRV         | PCI clock output drive                 | 0                | +           |
| COREDIS          | Core disable mode                      | 0                | -           |
| BMS              | Boot memory space                      | 0                | +           |
| BOOTSEQ[0:1]     | Boot sequencer configuration           | 0b00             | -           |
| SWEN             | Software watchdog enable               | 1                | ***         |
| ROMLOC[0:2]      | Boot ROM interface location            | 0b111            | -           |
| SDDRIOE          | Secondary DDR I/O enable               | 0                |             |
| TLE              | True Little Endian                     | 0                | -           |
| LALE             | Local bus LALE signal timing           | 0                | -           |
| LDP              | LDP / CKSTP pin mux state              | 0                | +           |

\* with configuration EEPROM as programmed by TQ

\*\* writeable once after reset

+ = yes, - = no

Table 4: Configuration data CPU

### 3.2.3.5 Settings via boot sequencer

The boot sequencer offers an additional possibility to configure the CPU without any support by the software. The boot sequencer is not linked with the reset configuration (details see [1]).

- Identical with the mechanism which reads the reset configuration word from the I<sup>2</sup>C-EEPROM. Starts, however, only after the reset has ended.
- Can partly replace / anticipate the configuration of the CPU by the software
- Application cases:
  - Multi processor environments
  - Preconfiguration to boot other systems (e.g., PCI, DDR2...)
  - Eliminating incompatibilities with reset values (e.g., bus driver control LBCTL)

#### Notes:

- Incorrect data can lead to an unbootable system!
- The boot software (e.g., U-Boot) in combination with the Starterkit / Starterkit + adaptor should not be dependent of the boot sequencer

### 3.2.4 PLD

The PLD fulfils the following tasks:

- Choice of the configuration source (see 3.2.3.1)
- I<sup>2</sup>C bus reset (see 3.2.3.2)

3.2.5 Clock

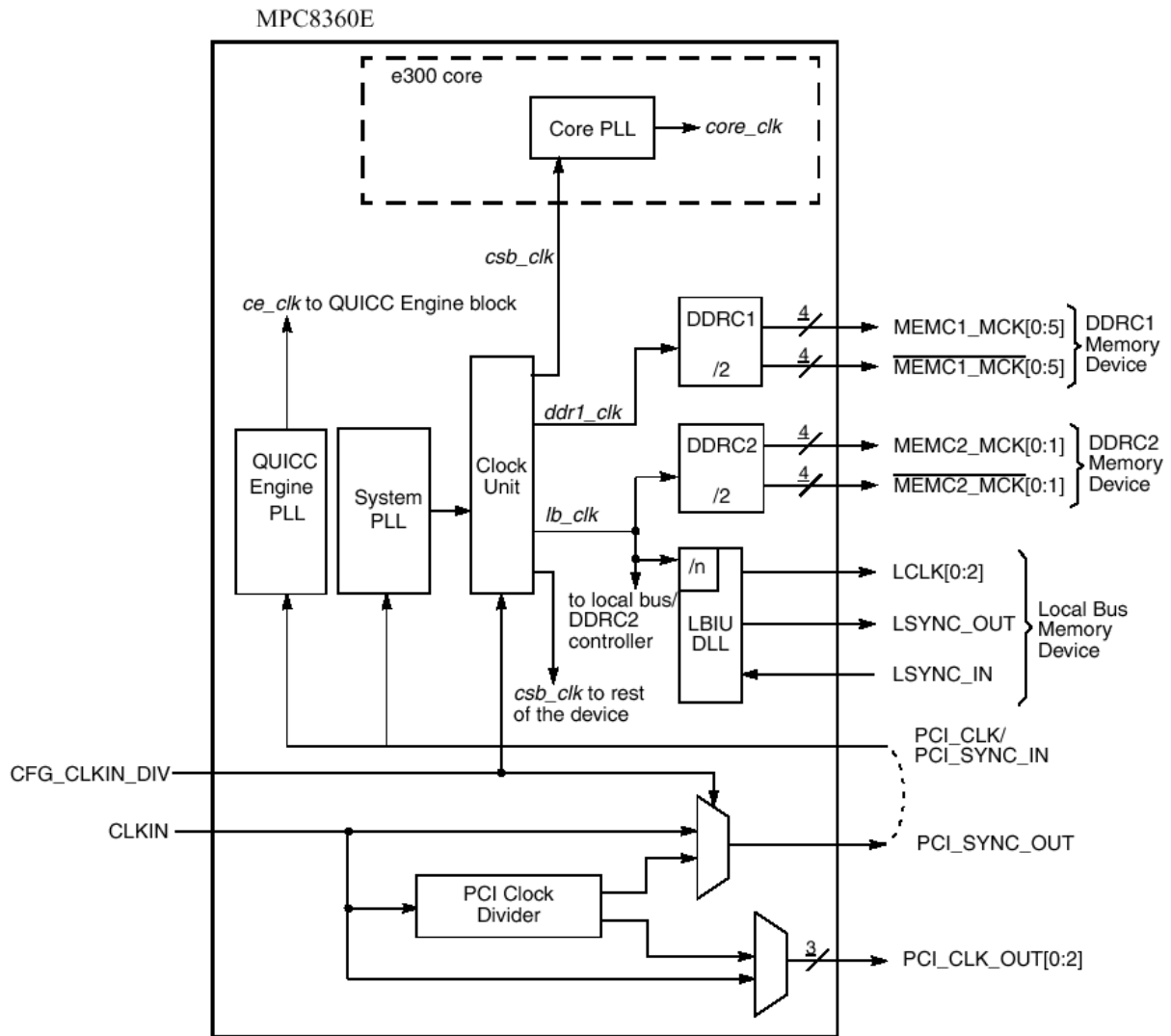


Illustration 3: Internal clock structure MPC8360E

Important notes:

1. Freescale offers the flash based reset and clock configuration tool already known from the MPC8349E, which also supports the MPC8360E in the current revision 1.
2. On account of a hardware problem of the CPU Rev. 2.0 (erratum "General 9") the CPU cannot operate simultaneously with
  - maximum core clock frequency
  - maximum QUICC engine clock frequency
  - minimum operating voltage and
  - maximum chip temperature

The limitation of at least one of these parameters is sufficient to guarantee correct functioning. Suitable combinations of clock frequencies are specified in the errata sheet therefore [3]. Independent of this, the core supply voltage VDD must be set dependent on the clock frequency.

3. The clocks generated on the module have no serial termination.  
The serial termination has to be provided on the target hardware.

3.2.5.1 System clock

- When the CPU is the host PCI, CLKIN is the clock input. In this case a feedback of PCI\_SYNC\_OUT → PCI\_CLK / PCI\_SYNC\_OUT is necessary (to be implemented on the base board).
- Frequency leads 1 : 1 or divided 2 : 1 to all PCI clocks (see 3.2.5.2)
- On the module clocked with 66.6667 MHz, the internal clock is switchable for agent mode or external feed (signal CLKOE)
- External supplied frequency: max. 66 MHz
- Slew rate of CLKIN is specified with very close tolerances ⇒ for an external feed it is recommended to mount a driver NC7SV126 with a serial resistor of 33 Ω very close to the module.

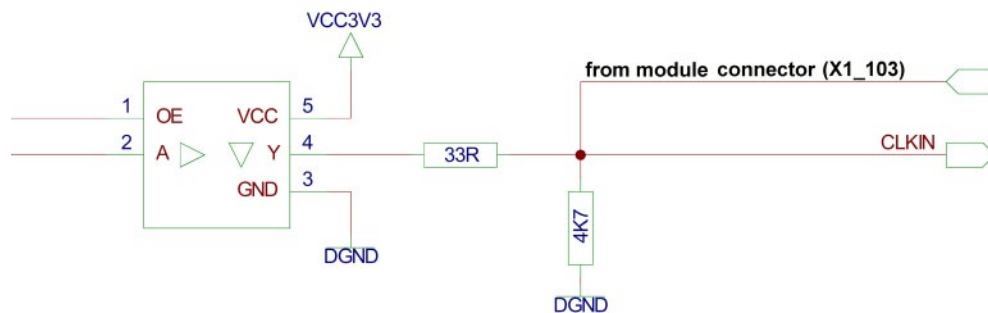


Illustration 4: Wiring of CLKIN on the TQM8360L

Additional information:

D19, pin 1 (OE) ist active, when CLKOE is high and PCI\_MODE# is low.

D19, pin 2 (A) is fed by a 66.667 MHz crystal oscillator.

3.2.5.2 PCI clocks

- Complex CLKIN / CFG\_CLKIN\_DIV / PCI\_SYNC\_OUT / PCI\_CLK\_OUT[0:2] is an integrated clock driver with PLL to balance the signal run times of the PCI clocks
- The reference is always PCI\_CLK / PCI\_SYNC\_IN

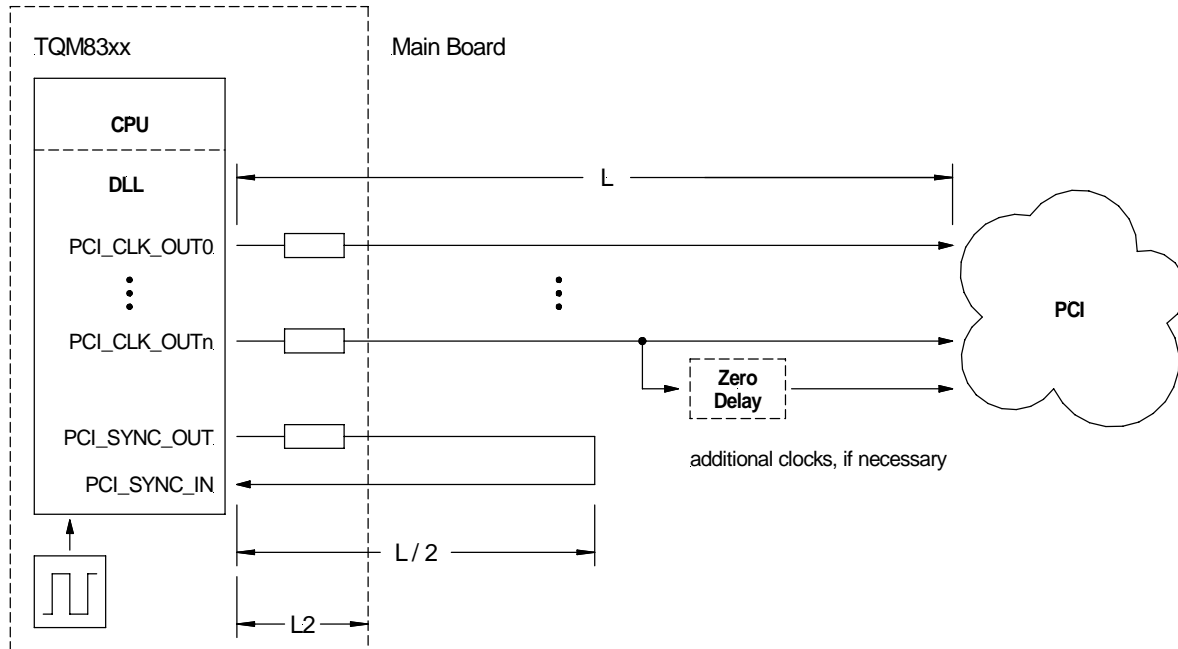


Illustration 5: Clock driver

Important notes:

The clocks generated on the module have no serial termination. The serial termination has to be provided on the target hardware

All clock outputs PCI\_CLK\_OUT [0:2] are made externally available. If more subscribers than existing clock outputs have to be supplied, an additional zero delay buffer has to be provided on the base board.

If PCI is not used, the length of the return wiring (not the return itself!) is irrelevant.

For the operation as a PCI agent the clock generator can be switched off (according to PCI spec at constant low level). Then the PCI clock is fed from external to PCI\_SYNC\_IN. In this case the base board is exclusively responsible for the clock distribution. In this mode the outputs PCI\_CLK\_OUT [0:2] are not usable.

### 3.2.5.3 Coherent system bus clock

- Is generated by multiplication from PCI\_CLK / PCI\_SYNC\_IN (Multiplication factor defined by reset configuration)
- Available as a CPU-internal signal only
- Used for the DDR(2)-SDRAM, local bus and CPU-internal
- Frequency range of 133 MHz ... 333 MHz [2]

### 3.2.5.4 Processor core clock

- Is generated by multiplication from CSB\_CLK (Multiplication factor defined by reset configuration)
- Available as a CPU-internal signal only
- Used for e300 core
- Frequency range of 266 MHz ... 667 MHz [2], 667 MHz with raised core voltage (1.3 V)

### 3.2.5.5 QUICC engine clock

- Is generated by multiplication from PCI\_CLK / PCI\_SYNC\_IN (Multiplication factor defined by reset configuration)
- Available as a CPU-internal signal only
- Used for QUICC engine
- Frequency range of 200 MHz ... 500 MHz [2], 500 MHz with raised core voltage (1.3 V)

### 3.2.5.6 Memory bus clock

- Is generated from CSB\_CLK (Factor 1 or 2, defined by reset configuration bit DDRCM)
- Used for DDR-SDRAM (= frequency MCKx = half the data rate)
- Frequency range of 100 MHz ... 166 MHz [2]

### 3.2.5.7 Local bus clock

- Is generated from CSB\_CLK (factor 1 or 2 defined by reset configuration bit LBIUCM)
- Used for local bus
- Configurable at run time via LCRR [CLKDIV] (division by 2 / 4 / 8)
- Frequency range of 16.67 MHz ... 133 MHz [2]

3.2.5.8 Real time clock

- Independent clock input for time base, as a multiplexed function on QUICC engine pin, see Table 5
- No possibility available for buffering for the purpose of a real time clock (real time clock see 3.2.10)
- Enables as the reference clock the measurement of the own clock frequency, or in connection with the CIB of the monitor it enables the monitor's control
- Is fed with 16.6667 MHz regardless of all other CPU clocks
- Decoupling reference clock through a serial resistor of 470 Ω
  - sufficient low resistant signals (MPC8360E or external signals) can overwrite the signal of the internal clock generator

| Pin  |     | Pin functions      |                |               |                    |                |               |                    |                |               |                    |                |               |
|------|-----|--------------------|----------------|---------------|--------------------|----------------|---------------|--------------------|----------------|---------------|--------------------|----------------|---------------|
|      |     | CPPARCx[SELn] = 00 |                |               | CPPARCx[SELn] = 01 |                |               | CPPARCx[SELn] = 10 |                |               | CPPARCx[SELn] = 11 |                |               |
|      |     | Function           | CPDIRxC [DIRn] | Default input | Function           | CPDIRxC [DIRn] | Default input | Function           | CPDIRxC [DIRn] | Default input | Function           | CPDIRxC [DIRn] | Default input |
| PC26 | IN  | GPI_PC26           | 10             |               | RTC_CLK<br>PIT_CLK | 10             | GND           |                    |                |               |                    |                |               |
|      | OUT | GPO_PC26           | 01             |               |                    |                |               | SI:STRB3           | 01             |               |                    |                |               |

Table 5: Multiplexing PC26

3.2.6 Flash / non-volatile memory

- 3.3V flashes of the P33 series of Intel, 16 bit wide
- Connected to the local bus, via a latch due to multiplexed addresses and data addresses
- 1 bank with a bus width of 32 bit
- 16 Mbyte to 128 Mbyte
- Access time 120 ns
- Chip-Select LCS0#

Because the boot process is performed from the flash, boot chip select LCS0# has to be used.

As the status signal WAIT of the flashes is not used by the CPU, i.e. the execution of the write cycles and the delete cycles must be monitored by polling.

### 3.2.7 NAND flash

- NAND flash 1 × 8 bit wide, TSOP48
- Connected to the local bus via buffer, see Illustration 6
- Address decoding for multi-chip-NANDs (max. 2 × 4 chip selects), decoding via LAD[21:22]
- 1 bank with a bus width of 8 bit
- 256 Mbyte to 1 Gbyte
- Access time  $t_{RC} / t_{WC} = 50 \text{ ns}$
- Chip select LCS3#
- Control via UPM sequences
- ECC calculation by software
- Flash status signals R/B#[0:3] connected to a common signal, supplied with a pull-up and connected to a module pin

Possible use of the R/B signals by the software:

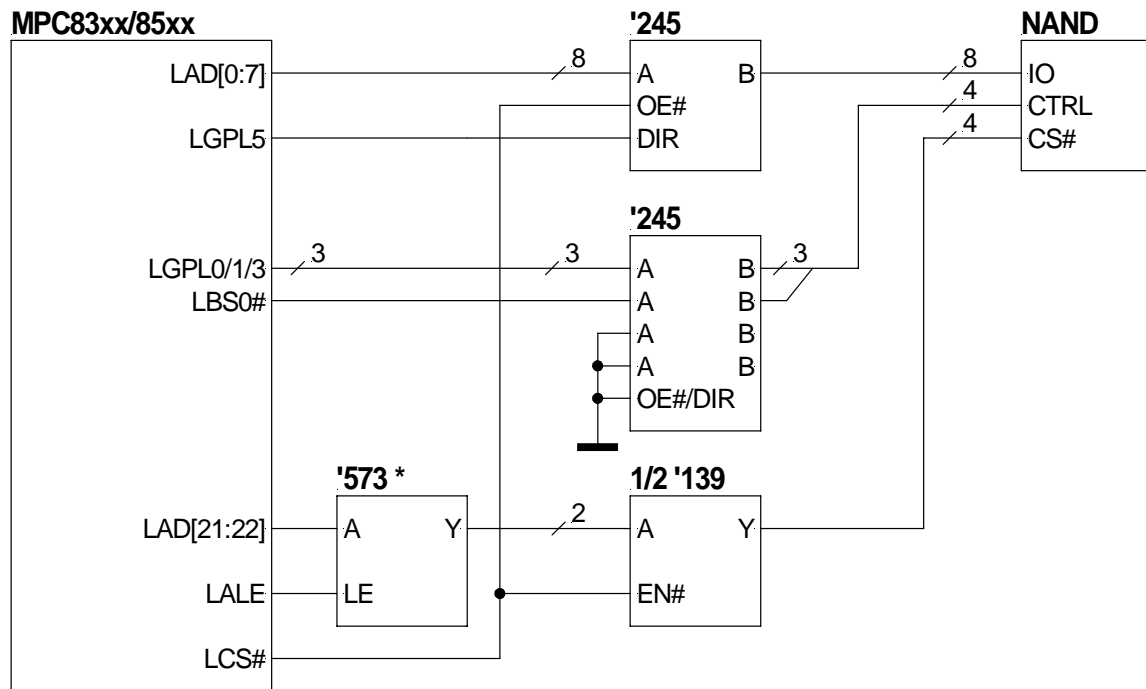
Possibility 1:

R/B# is not used, and instead of this the maximum time  $t_R = 20 \mu\text{s}$  is waited for the reading cycle.

Possibility 2:

R/B# is made readable for the CPU by the user at own risk (via general purpose I/O or similar). The software must be configured in such a way that it uses a suitable method to read out the status pin.

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\* already existing

Illustration 6: Driver's structure for NAND flashes

### 3.2.8 DDR2-SDRAM

- DDR2-SDRAMs, 16 bit data width
- Synchronous dynamic RAM, double data rate
- 256 Mbyte ... 512 Mbyte, 1 Gbyte in planning
- 133 MHz clock (DDR2-266)
- Strobes single ended
- One memory bank with 64 bit width or 2 memory banks with 32 bit width, configurable via reset configuration
- CAS Latency 3
- BGA package

### 3.2.9 EEPROM

All I<sup>2</sup>C bus devices on the module are connected to the I<sup>2</sup>C controller of the CPU. The used addresses are shown in the following table.

| Device               | MSB |   |   |   |        |        |        | LSB |
|----------------------|-----|---|---|---|--------|--------|--------|-----|
| Data EEPROM          | 1   | 0 | 1 | 0 | 1 (A2) | 1 (A1) | 1 (A0) | R/W |
| Configuration EEPROM | 1   | 0 | 1 | 0 | 0 (A2) | 0 (A1) | 0 (A0) | R/W |
| Real time clock      | 1   | 1 | 0 | 1 | 0      | 0      | 0      | R/W |
| Temperature sensor   | 1   | 0 | 0 | 1 | 0 (A2) | 0 (A1) | 0 (A0) | R/W |
| Power manager        | 1   | 0 | 0 | 0 | 1      | 0 (A1) | 0 (A0) | R/W |

Table 6: IIC1 device addresses

#### 3.2.9.1 Data EEPROM

The serial EEPROM can store, e.g., characteristics of the module and customer specific parameter data. In the EEPROM single memory cells can be deleted and be overwritten in contrast to flash. At delivery the EEPROM is erased. It can, e.g., save application parameters non-volatile.

- 0 / 4 Kbyte ... 32 Kbyte
- Possible I<sup>2</sup>C clock frequency 400 kHz
- Is freely available, can be used as a boot sequencer if desired
- Control via I<sup>2</sup>C controller IIC1, device address see Table 6

#### 3.2.9.2 Configuration EEPROM

At delivery the configuration EEPROM contains a standard reset configuration (see 3.2.3.4).

- 4 Kbyte
- Possible I<sup>2</sup>C clock frequency 400 kHz
- For reset configuration and as a boot sequencer if desired
- Update by the CPU is possible
- Control via I<sup>2</sup>C controller IIC1, device address see Table 6

### 3.2.10 RTC

Because there is no CPU-internal bufferable RTC, the RTC was realised externally.

- RTC DS1337U, control via I<sup>2</sup>C bus of the CPU
- Possible I<sup>2</sup>C clock frequency 400 kHz
- Battery buffering possible (battery on base board)
- Alarm outputs INTA# and SQW/INTB# (open drain) connected to common pin
- Control via I<sup>2</sup>C controller IIC1, device address see Table 6
- Quartz tolerance 30 ppm

### 3.2.11 Temperature supervision

- Is placed near the CPU for indirect monitoring of the CPU-temperature
- Sensor LM75
- Possible I<sup>2</sup>C clock frequency 400 kHz
- Switch output of the LM75 led out
- Control via I<sup>2</sup>C controller IIC1, device address see Table 6

### 3.2.12 General purpose I/O

- 213 GPIOs, split on  
PA (32 bit), PB (28 bit), PC (31 bit), PD (28 bit), PE (32 bit), PF (30 bit), PG (32 bit)
- Partly multiplexed at the CPU with other signals of the QUICC engine, e.g., PCI, (Gigabit) Ethernet etc.
- High-resistance after power-on-reset
- Open drain capable
- Partly interruptible

Note:

With the CodeWarrior QUICC engine utility Freescale offers a software solution which should support the user to choose suitable pin multiplexing, amongst other things.

## 3.3 Supply

The following voltages exist on the module:

| Voltage       | Usage   |
|---------------|---|
| 3.3 V         | CPU (Local bus, PCI, if applicable Ethernet via GMII, TBI, MII, RMII ...)<br>Flash, RTC, I <sup>2</sup> C-EEPROM, other logic |
| 2.5 V         | CPU (If applicable Ethernet via RGMII, RTBI)  |
| 1.8 V         | CPU (DDR2), DDR2-SDRAM  |
| 1.2 V / 1.3 V | CPU (Core)  |
| 0.9 V         | DDR2-SDRAM reference voltage  |

Table 7: Supply voltages

### 3.3.1 Supply possibilities

The supply contains the following function blocks:

- Regulator from 3.3 V to 2.5 V (LVDD[0:2] = I/O voltages for certain CE pins, e.g., Ethernet)
- Step-down switching regulator from 3.3 V to 1.8 V (= voltage for DDR2-SDRAMs)
- Step-down switching regulator from 3.3 V to core voltage (1.2 V or 1.3 V)
- Power-Sequencing for 3.3 V (I/O voltage)

The module is supplied exclusively with 3.3 V.

The supply structure is shown in the following illustration.

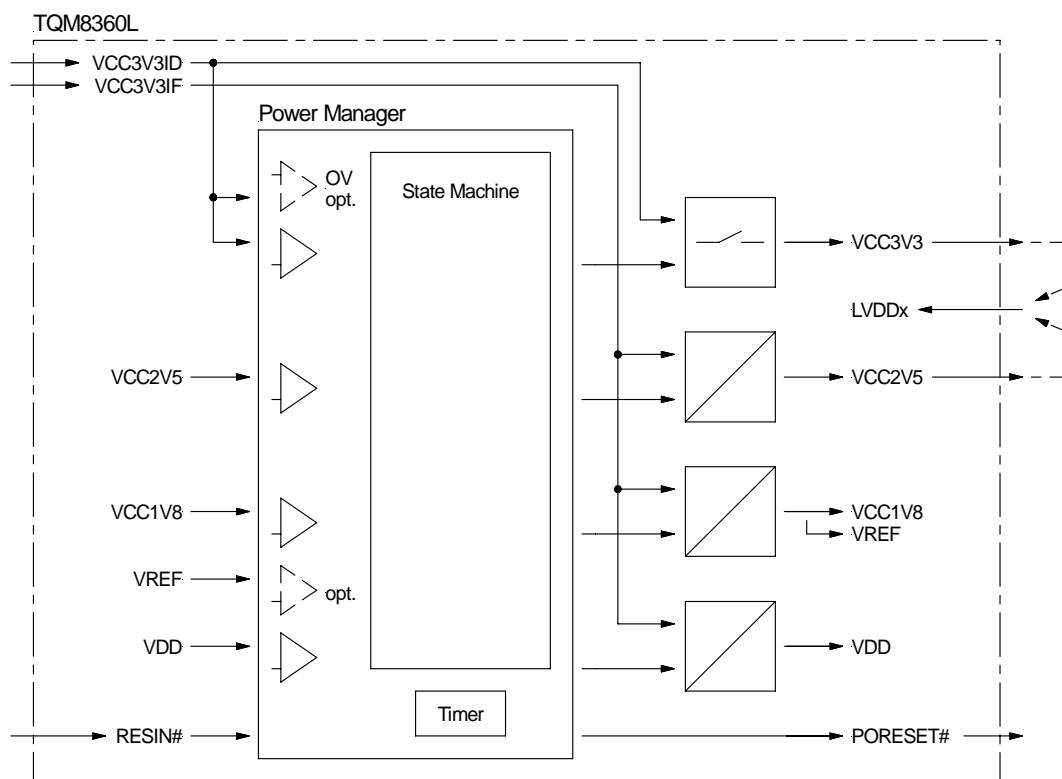


Illustration 7: Supply structure

For the supply voltages to be fed, the following maximum ratings apply:

|                                |                          |  |
|--------------------------------|--------------------------|--|
| Voltages VCC3V3IF and VCC3V3ID | 3.067 V ... 3.600 V      | Determined by voltage range of components and supervisor threshold (see 3.2.2.1)                         |
| Ripple max.                    | 30 mV                    | peak to peak   |
| Current consumption            | 5.8 A max.<br>3.8 A typ. | TQM8360L @ 667/333/500 MHz (Core/DDR/CE, worst case)<br>TQM8360L @ 533/266/400 MHz (Core/DDR/CE, U-Boot) |

Table 8: Requirements for 3.3 V external

3.3.2 Power Sequencing

- The power sequencing is realised by an integrated power management device, see Illustration 7. A high flexibility is thereby ensured.
- As recommended in the specification of the MPC8360E, the core voltage VDD is booted up first (thereby, PORESET# = low), before the other voltages are switched on. In this way undefined start-up conditions of the CPU should be avoided. [2]
- In spite of this measure these undefined start-up conditions may occur. If necessary this should be taken into consideration in the design of the base board. Especially endangered are non-volatile memories, e.g., the chip select for a battery-buffered RAM.

3.3.3 RTC supply VBAT

- Supply of the RTC
- Current consumption only, if VBAT > VCC3V3 (connection to VCC3V3 via Schottky diode is present on module)

|                     |                 |   |
|---------------------|-----------------|---|
| Voltage VBAT        | 1.8 V ... 5.5 V | Determined by voltage range of RTC (see 3.2.10) |
| Ripple max.         | 1 %             | Peak to peak                                    |
| Timekeeping current | 2 µA            | VCC3V3IF = VCC3V3ID = 0 V, oscillator running   |

Table 9: Requirements for the RTC supply

3.3.4 3.3 V supply

- Main supply of the module, 3.3 V
- Led through for application specific supply of LVDD[0:2], cf. Illustration 7
- In addition, no current drain (e.g., for the supply of external devices) allowed

3.3.5 2.5 V supply

- 2.5 V exclusively for the application-centric supply of 2.5 V peripheral in LVDD[0:2], cf. Illustration 7
- In addition, no current drain (e.g., for the supply of external devices) allowed

3.3.6 Supply Ethernet-I/O

- 2.5 V or 3.3 V, depending on the use of the interfaces supplied from it
- Determined by connection on base board of VCC3V3 to LVDDx respectively VCC2V5 to LVDDx, see Illustration 7

3.3.7 Reference voltage VREF

- Reference voltage 0.9 V for DDR2-SDRAMs
- Monitoring optionally possible by configuration update of the power management device

### 3.4 Interfaces to other systems and devices

#### 3.4.1 Serial interfaces

- Two internal UARTs: UART0, UART1
- Max. 115200 baud (limited by driver / level converter)
- Driver with RS232 compatible levels
- All signals also available without driver
- Default assembly is a driver with 2 × RxD / TxD

#### 3.4.2 COP/JTAG interface

All lines of the Freescale COP/JTAG interface (debugging interface) are made available externally. Like the TQS-debugging interface, the COP/JTAG interface is also exclusively led through to the connectors to the base board.

The COP/JTAG interface incorporates the following signals (signal direction seen from the module respective the STK85xx):

| Pin* | Signal name                    | Type | Function  |
|------|--------------------------------|------|---|
| 1    | TDO                            | O    | Test Data Output  |
| 3    | TDI                            | I    | Test Data Input   |
| 9    | TMS                            | I    | Test Mode Select  |
| 7    | TCK                            | I    | Test Clock  |
| 4    | TRST#                          | I    | Test Reset  |
| 5    | NC                             | –    | –   |
| 12   | NC                             | –    | –   |
| 11   | SRESET#                        | O    | Soft Reset  |
| 13   | HRESET#                        | I/O  | Hard Reset  |
| 15   | MCP_OUT#<br>(not CKSTP_OUT# !) | O    | Machine Check Interrupt Out<br>(Check Stop Out on STK85xx with TQM85xx) |
| 16   | DGND                           | –    | (Digital) ground  |
| 6    | VDD_SENSE                      | O    | 3.3 V Sensing   |

\* on Starterkit STK85xx

Table 10: COP/JTAG interface

### 3.4.3 External bus / other interfaces

The interfaces described here are led through to the plug connectors leading to the base board:

- 2 × 160 pins +
- 1 × 120 pins +
- 1 × 60 pins

#### 3.4.3.1 Treatment of unused pins

The module was designed in such a way, that only one a minimum number of signals are necessary for the operation. Hence, many signals do not need external wiring if their function is not required.

- Outputs (type = O): No wiring necessary
- Inputs and I/Os with pull-up / pull-down (type = I, I/O, pull-up or pull-down is described): No wiring necessary
- The I/Os which can be configured as an output (GPIO1[x], GPIO2[x]):  
In general it is sufficient to configure unused pins as an output during initialization
- Continuing notes are found in [1]

#### 3.4.3.2 How to use the QUICC Engine for Ethernet PHY connection

The following measures are recommended for connecting the Fast-/Gigabit-Ethernet-Phys to the pins of the QUICC Engine:

- Serial termination of fast signals at the beginning of the line or at the module (especially all clocks, but not at slow signals like MDIO, MDC)
- Adequate separation of clock signals to data lines
- Compliance with the layout requirements regarding line impedance and length difference

#### 3.4.3.3 Hints for external use of the LocalBus

If the LocalBus is used on the target hardware the following measures are recommended:

- Serial termination of fast signals, especially all clocks
- Adequate separation of clock signals to data lines
- Check, whether the configuration of the LocalBus suits the common use on the module and on the target hardware
- Use of address latches for external components, if necessary (see 3.2.7)

3.4.3.4 Pin-out according to function groups

| Signal                        | CPU pin | Type    | Description   | Module pin |
|-------------------------------|---------|---------|---|------------|
| <b>PCI</b>                    |         |         |   |            |
| PCI_INTA# / IRQ_OUT# / CE_PF5 | A20     | I/O     | PCI interrupt out / Interrupt output / QUICC engine parallel I/O, ↑ 8k2 | X1-37      |
| PCI_RESET_OUT# / CE_PF6       | E19     | I/O     | PCI reset output / QUICC engine parallel I/O                            | X1-38      |
| PCI_AD31 / CE_PG31            | D20     | I/O, TS | PCI address/data 31 / QUICC engine parallel I/O 31, ↑ 8k2               | X2-39      |
| PCI_AD30 / CE_PG30            | D21     | I/O, TS | PCI address/data 30 / QUICC engine parallel I/O 30, ↑ 8k2               | X2-40      |
| PCI_AD29 / CE_PG29            | A24     | I/O, TS | PCI address/data 29 / QUICC engine parallel I/O 29, ↑ 8k2               | X2-43      |
| PCI_AD28 / CE_PG28            | B23     | I/O, TS | PCI address/data 28 / QUICC engine parallel I/O 28, ↑ 8k2               | X2-42      |
| PCI_AD27 / CE_PG27            | C23     | I/O, TS | PCI address/data 27 / QUICC engine parallel I/O 27, ↑ 8k2               | X2-45      |
| PCI_AD26 / CE_PG26            | E23     | I/O, TS | PCI address/data 26 / QUICC engine parallel I/O 26, ↑ 8k2               | X2-44      |
| PCI_AD25 / CE_PG25            | A26     | I/O, TS | PCI address/data 25 / QUICC engine parallel I/O 25, ↑ 8k2               | X2-47      |
| PCI_AD24 / CE_PG24            | B21     | I/O, TS | PCI address/data 24 / QUICC engine parallel I/O 24, ↑ 8k2               | X2-46      |
| PCI_AD23 / CE_PG23            | C24     | I/O, TS | PCI address/data 23 / QUICC engine parallel I/O 23, ↑ 8k2               | X2-49      |
| PCI_AD22 / CE_PG22            | C25     | I/O, TS | PCI address/data 22 / QUICC engine parallel I/O 22, ↑ 8k2               | X2-50      |
| PCI_AD21 / CE_PG21            | D25     | I/O, TS | PCI address/data 21 / QUICC engine parallel I/O 21, ↑ 8k2               | X2-51      |
| PCI_AD20 / CE_PG20            | B25     | I/O, TS | PCI address/data 20 / QUICC engine parallel I/O 20, ↑ 8k2               | X2-52      |
| PCI_AD19 / CE_PG19            | E24     | I/O, TS | PCI address/data 19 / QUICC engine parallel I/O 19, ↑ 8k2               | X2-55      |
| PCI_AD18 / CE_PG18            | F24     | I/O, TS | PCI address/data 18 / QUICC engine parallel I/O 18, ↑ 8k2               | X2-54      |
| PCI_AD17 / CE_PG17            | A27     | I/O, TS | PCI address/data 17 / QUICC engine parallel I/O 17, ↑ 8k2               | X2-57      |
| PCI_AD16 / CE_PG16            | A28     | I/O, TS | PCI address/data 16 / QUICC engine parallel I/O 16, ↑ 8k2               | X2-56      |
| PCI_AD15 / CE_PG15            | F27     | I/O, TS | PCI address/data 15 / QUICC engine parallel I/O 15, ↑ 8k2               | X2-59      |
| PCI_AD14 / CE_PG14            | A30     | I/O, TS | PCI address/data 14 / QUICC engine parallel I/O 14, ↑ 8k2               | X2-58      |
| PCI_AD13 / CE_PG13            | C30     | I/O, TS | PCI address/data 13 / QUICC engine parallel I/O 13, ↑ 8k2               | X2-61      |
| PCI_AD12 / CE_PG12            | D30     | I/O, TS | PCI address / data12 / QUICC engine parallel I/O 12, ↑ 8k2              | X2-62      |
| PCI_AD11 / CE_PG11            | E29     | I/O, TS | PCI address/data 11 / QUICC engine parallel I/O 11, ↑ 8k2               | X2-63      |
| PCI_AD10 / CE_PG10            | B31     | I/O, TS | PCI address/data 10 / QUICC engine parallel I/O 10, ↑ 8k2               | X2-64      |
| PCI_AD9 / CE_PG9              | C31     | I/O, TS | PCI address/data 9 / QUICC engine parallel I/O 9, ↑ 8k2                 | X2-67      |
| PCI_AD8 / CE_PG8              | D31     | I/O, TS | PCI address/data 8 / QUICC engine parallel I/O 8, ↑ 8k2                 | X2-66      |
| PCI_AD7 / CE_PG7              | D32     | I/O, TS | PCI address/data 7 / QUICC engine parallel I/O 7, ↑ 8k2                 | X2-69      |

| Signal                                 | CPU pin | Type    | Description   | Module pin |
|--|---------|---------|---|------------|
| <b>PCI</b>                             |         |         |   |            |
| PCI_AD6 /<br>CE_PG6                    | A32     | I/O, TS | PCI address/data 6 /<br>QUICC engine parallel I/O 6, ↑ 8k2                                      | X2-68      |
| PCI_AD5 /<br>CE_PG5                    | C33     | I/O, TS | PCI address/data 5 /<br>QUICC engine parallel I/O 5, ↑ 8k2                                      | X2-71      |
| PCI_AD4 /<br>CE_PG4                    | B33     | I/O, TS | PCI address/data 4 /<br>QUICC engine parallel I/O 4, ↑ 8k2                                      | X2-70      |
| PCI_AD3 /<br>CE_PG3                    | F30     | I/O, TS | PCI address/data 3 /<br>QUICC engine parallel I/O 3, ↑ 8k2                                      | X2-73      |
| PCI_AD2 /<br>CE_PG2                    | E31     | I/O, TS | PCI address/data 2 /<br>QUICC engine parallel I/O 2, ↑ 8k2                                      | X2-74      |
| PCI_AD1 /<br>CE_PG1                    | A34     | I/O, TS | PCI address/data 1 /<br>QUICC engine parallel I/O 1, ↑ 8k2                                      | X2-75      |
| PCI_AD0 /<br>CE_PG0                    | D33     | I/O, TS | PCI address/data 0 /<br>QUICC engine parallel I/O 0, ↑ 8k2                                      | X2-76      |
| PCI_C_BE3# /<br>CE_PF10                | E22     | I/O, TS | PCI command byte enable 3 /<br>QUICC engine parallel I/O 10, ↑ 8k2                              | X2-97      |
| PCI_C_BE2# /<br>CE_PF9                 | B26     | I/O, TS | PCI command byte enable 2 /<br>QUICC engine parallel I/O 9, ↑ 8k2                               | X2-98      |
| PCI_C_BE1# /<br>CE_PF8                 | E28     | I/O, TS | PCI command byte enable 1 /<br>QUICC engine parallel I/O 8, ↑ 8k2                               | X2-99      |
| PCI_C_BE0# /<br>CE_PF7                 | F28     | I/O, TS | PCI command byte enable 0 /<br>QUICC engine parallel I/O 7, ↑ 8k2                               | X2-100     |
| PCI_PAR / CE_PF11                      | D28     | I/O, TS | PCI parity / QUICC engine parallel I/O 11, ↑ 8k2  | X2-78      |
| PCI_FRAME# / CE_PF12                   | D26     | I/O, TS | PCI frame / QUICC engine parallel I/O 12, ↑ 8k2   | X2-80      |
| PCI_TRDY# /<br>CE_PF13                 | C27     | I/O, TS | PCI target ready /<br>QUICC engine parallel I/O 13, ↑ 8k2                                       | X2-81      |
| PCI_IRDY# /<br>CE_PF14                 | C28     | I/O, TS | PCI initiator ready /<br>QUICC engine parallel I/O 14, ↑ 8k2                                    | X2-82      |
| PCI_STOP# /<br>CE_PF15                 | B28     | I/O, TS | PCI stop /<br>QUICC engine parallel I/O 15, ↑ 8k2   | X2-83      |
| PCI_DEVSEL# /<br>CE_PF16               | E26     | I/O, TS | PCI device select /<br>QUICC engine parallel I/O 16, ↑ 8k2                                      | X2-86      |
| PCI_IDSEL /<br>CE_PF17                 | F22     | I/O     | PCI initial device select /<br>QUICC engine parallel I/O 17, ↓ 8k2                              | X2-85      |
| PCI_SERR# /<br>CE_PF18                 | B29     | I/O, TS | PCI system error /<br>QUICC engine parallel I/O 18, ↑ 8k2                                       | X2-91      |
| PCI_PERR# /<br>CE_PF19                 | A29     | I/O, TS | PCI parity error /<br>QUICC engine parallel I/O 19, ↑ 8k2                                       | X2-90      |
| PCI_REQ0# /<br>CE_PF20                 | F19     | I/O     | PCI request 0 /<br>QUICC engine parallel I/O 20, ↑ 8k2  | X2-112     |
| PCI_REQ1# /<br>CPCI_HS_ES /<br>CE_PF21 | A21     | I/O     | PCI request 1 /<br>Compact PCI hot swap ejector switch /<br>QUICC engine parallel I/O 21, ↑ 8k2 | X2-111     |
| PCI_REQ2# /<br>CE_PF22                 | C21     | I/O     | PCI request 2 /<br>QUICC engine parallel I/O 22, ↑ 8k2  | X2-110     |
| PCI_GNT0# /<br>CE_PF23                 | E20     | I/O     | PCI grant 0 /<br>QUICC engine parallel I/O 23, ↑ 8k2  | X2-107     |
| PCI_GNT1# / CPCI_HS_LED /<br>CE_PF24   | B20     | I/O     | PCI grant 1 / Compact PCI hot swap LED /<br>QUICC engine parallel I/O 24                        | X2-104     |
| PCI_GNT2# / CPCI_HS_ENUM# /<br>CE_PF25 | C20     | I/O     | PCI grant 2 / Compact PCI hot swap enumerator /<br>QUICC engine parallel I/O 25, ↑ 8k2          | X2-105     |
| PCI_MODE#                              | D36     | I       | PCI mode select, ↓ 8k2  | X2-109     |
| M66EN /<br>CE_PF4                      | B37     | I/O     | PCI 66-MHz timing on/off /<br>QUICC engine parallel I/O 4, ↑ 8k2                                | X1-36      |

| Signal                  | CPU pin | Type    | Description  | Module pin |
|-------------------------|---------|---------|--|------------|
| <b>Local Bus</b>        |         |         |  |            |
| LAD0                    | N32     | I/O, TS | LBC address/data 0 (MSB)                                   | X3-74      |
| LAD1                    | N33     | I/O, TS | LBC address/data 1   | X3-67      |
| LAD2                    | N35     | I/O, TS | LBC address/data 2   | X3-72      |
| LAD3                    | N36     | I/O, TS | LBC address/data 3   | X3-65      |
| LAD4                    | P37     | I/O, TS | LBC address/data 4   | X3-70      |
| LAD5                    | P32     | I/O, TS | LBC address/data 5   | X3-63      |
| LAD6                    | P34     | I/O, TS | LBC address/data 6   | X3-68      |
| LAD7                    | R36     | I/O, TS | LBC address/data 7   | X3-61      |
| LAD8                    | R35     | I/O, TS | LBC address/data 8   | X3-66      |
| LAD9                    | R34     | I/O, TS | LBC address/data 9   | X3-59      |
| LAD10                   | R33     | I/O, TS | LBC address/data 10  | X3-64      |
| LAD11                   | T37     | I/O, TS | LBC address/data 11  | X3-57      |
| LAD12                   | T35     | I/O, TS | LBC address/data 12  | X3-60      |
| LAD13                   | T34     | I/O, TS | LBC address/data 13  | X3-55      |
| LAD14                   | T33     | I/O, TS | LBC address/data 14  | X3-58      |
| LAD15                   | U37     | I/O, TS | LBC address/data 15  | X3-51      |
| LAD16                   | T32     | I/O, TS | LBC address/data 16  | X3-56      |
| LAD17                   | U36     | I/O, TS | LBC address/data 17  | X3-49      |
| LAD18                   | U34     | I/O, TS | LBC address/data 18  | X3-54      |
| LAD19                   | V36     | I/O, TS | LBC address/data 19  | X3-47      |
| LAD20                   | V35     | I/O, TS | LBC address/data 20  | X3-52      |
| LAD21                   | W37     | I/O, TS | LBC address/data 21  | X3-45      |
| LAD22                   | W35     | I/O, TS | LBC address/data 22  | X3-50      |
| LAD23                   | V33     | I/O, TS | LBC address/data 23  | X3-43      |
| LAD24                   | V32     | I/O, TS | LBC address/data 24  | X3-48      |
| LAD25                   | W34     | I/O, TS | LBC address/data 25  | X3-41      |
| LAD26                   | Y36     | I/O, TS | LBC address/data 26  | X3-44      |
| LAD27                   | W32     | I/O, TS | LBC address/data 27  | X3-39      |
| LAD28                   | AA37    | I/O, TS | LBC address/data 28  | X3-42      |
| LAD29                   | Y33     | I/O, TS | LBC address/data 29  | X3-35      |
| LAD30                   | AA35    | I/O, TS | LBC address/data 30  | X3-40      |
| LAD31                   | AA34    | I/O, TS | LBC address/data 31 (LSB)                                  | X3-33      |
| LDP0 / CKSTOP_OUT#      | AB37    | I/O, TS | LBC data parity 0 / Checkstop out, ↑ 4k7                   | X3-8       |
| LDP1 / CKSTOP_IN#       | AB36    | I/O, TS | LBC data parity 1 / Checkstop in, ↑ 4k7                    | X3-7       |
| LDP2 / LCS6#            | AB35    | I/O, TS | LBC data parity 2 / LBC chip select 6, ↑ 4k7               | X3-6       |
| LDP3 / LCS7#            | AA33    | I/O, TS | LBC data parity 3 / LBC chip select 7, ↑ 4k7               | X3-3       |
| LA27                    | AC37    | O       | LBC port address 27  | X3-38      |
| LA28                    | AA32    | O       | LBC port address 28  | X3-31      |
| LA29                    | AC36    | O       | LBC port address 29  | X3-36      |
| LA30                    | AC34    | O       | LBC port address 30  | X3-29      |
| LA31                    | AD36    | O       | LBC port address 31  | X3-34      |
| LCS0# / CS_FLASH0#      | AD33    | O       | LBC chip select 0 (boot chip select) used for flash bank 0 | X3-28      |
| LCS1#                   | AG37    | O       | LBC chip select 1  | X3-27      |
| LCS2#                   | AF34    | O       | LBC chip select 2  | X3-26      |
| LCS3# / CS_NAND#        | AE33    | O       | LBC chip select 3 used for NAND flashes                    | X3-25      |
| LCS4#                   | AD32    | O       | LBC chip select 4  | X3-24      |
| LCS5#                   | AH37    | O       | LBC chip select 5  | X3-23      |
| LWE0# / LSDDQM0 / LBS0# | AG35    | O       | LBC write enable 0 / Byte lane data mask 0 / Byte select 0 | X3-20      |
| LWE1# / LSDDQM1 / LBS1# | AG34    | O       | LBC write enable 1 / Byte lane data mask 1 / Byte select 1 | X3-17      |

| Signal   | CPU pin | Type | Description   | Module pin |
|--|---------|------|---|------------|
| <b>Local Bus</b>                               |         |      |   |            |
| LWE2# /<br>LSDDQM2 /<br>LBS2#                  | AH36    | O    | LBC write enable 2 /<br>Byte lane data mask 2 /<br>Byte select 2  | X3-18      |
| LWE3# /<br>LSDDQM3 /<br>LBS3#                  | AE32    | O    | LBC write enable 3 /<br>Byte lane data mask 3 /<br>Byte select 3  | X3-15      |
| LBCTL  | AD35    | O    | LBC data buffer control   | X3-4       |
| LALE   | M37     | O    | LBC address latch enable  | X3-32      |
| LGPL0 /<br>LSDA10 /<br>cfg_reset_source0       | AB32    | I/O  | LBC UPM general purpose line 0 /<br>SDRAM address bit 10 /<br>Configuration reset source 0  | X3-16      |
| LGPL1 /<br>LSDWE# /<br>cfg_reset_source1       | AE37    | I/O  | LBC UPM general purpose line 1 /<br>SDRAM write enable /<br>Configuration reset source 1  | X3-13      |
| LGPL2 /<br>LSDRAS# /<br>LOE#                   | AC33    | O    | LBC UPM general purpose line 2 /<br>SDRAM RAS /<br>LBC output enable  | X3-12      |
| LGPL3 /<br>LSDCAS# /<br>cfg_reset_source2      | AD34    | I/O  | LBC UPM general purpose line 3 /<br>SDRAM CAS /<br>Configuration reset source 2   | X3-11      |
| LGPL4 /<br>LGTA# /<br>LUPWAIT /<br>LPBSE       | AE35    | I/O  | LBC UPM general purpose line 4 /<br>GPCM terminate access /<br>UPM wait /<br>LBC parity byte select, ↑ 4k7  | X3-10      |
| LGPL5 /<br>cfg_clkin_div                       | AF36    | I/O  | LBC UPM general purpose line 5 /<br>Configuration clock in div  | X3-9       |
| LCKE   | G36     | O    | LBC clock enable  | X3-1       |
| LCLK0  | J33     | O    | LBC clocks 0  | X3-78      |
| LSYNC_OUT                                      | F34     | O    | LBC DLL synchronization output, feedback to<br>LSYNC_IN for flight time adjustment via DLL  | X3-73      |
| LSYNC_IN                                       | G35     | I    | LBC DLL synchronization input, ↑ 4k7, feedback<br>from LSYNC_IN for flight time adjustment via DLL  | X3-71      |
| <b>Programmable Interrupt Controller</b>       |         |      |   |            |
| MCP_OUT#                                       | E34     | O    | Machine check interrupt output, ↑ 4k7   | X1-144     |
| IRQ0# /<br>MCP_IN#                             | C37     | I    | External interrupt 0 /<br>Machine check interrupt input, ↑ 10k  | X1-106     |
| IRQ1# /<br>M1SRCID4 /<br>M2SRCID4 /<br>LSRCID4 | F35     | I/O  | External interrupt 1 /<br>DDR memory debug source port ID4 /<br>Secondary DDR memory debug source port ID4 /<br>LBC debug source port ID 4, ↑ 10k | X1-99      |
| IRQ2# /<br>M1DVAL /<br>M2DVAL /<br>LDVAL       | F36     | I/O  | External interrupt 2 /<br>DDR memory debug data valid /<br>Secondary DDR memory debug data valid /<br>LBC debug data valid, ↑ 10k                 | X1-104     |
| IRQ3# /<br>CORE_SRESET#                        | H34     | I    | External interrupt 3 /<br>Core soft reset, ↑ 10k  | X1-97      |
| IRQ4#  | G33     | I    | External interrupt 4, ↑ 10k   | X1-102     |
| IRQ5#  | G32     | I    | External interrupt 5, ↑ 10k   | X1-95      |
| IRQ6# /<br>LCS6# /<br>CKSTOP_OUT#              | E35     | I/O  | External interrupt 6 /<br>LBC chip select 6 /<br>Checkstop output, ↑ 10k  | X1-100     |
| IRQ7# /<br>LCS7# /<br>CKSTOP_IN#               | H36     | I/O  | External interrupt 7 /<br>LBC chip select 7 /<br>Checkstop input, ↑ 10k   | X1-93      |

| Signal  | CPU pin | Type | Description   | Module pin |
|---|---------|------|---|------------|
| <b>I<sup>2</sup>C Interface</b>                     |         |      |   |            |
| IIC1_SDA  | E32     | I/O  | I <sup>2</sup> C serial data, ↑ 22k   | X1-117     |
| IIC1_SCL  | B34     | I/O  | I <sup>2</sup> C serial clock, ↑ 22k  | X1-115     |
| IIC2_SDA  | C34     | I/O  | I <sup>2</sup> C serial data, ↑ 22k   | X1-79      |
| IIC2_SCL  | A35     | I/O  | I <sup>2</sup> C serial clock, ↑ 22k  | X1-80      |
| <b>DUART</b>  |         |      |   |            |
| UART1_SOUT /<br>M1SRCID0 /<br>M2SRCID0 /<br>LSRCID0 | E32     | O    | UART1 serial data out /<br>DDR memory debug source port ID0 /<br>Secondary DDR memory debug source port ID0 /<br>LBC debug source port ID 0       | X1-156     |
| UART1_SIN /<br>M1SRCID1 /<br>M2SRCID1 /<br>LSRCID1  | B34     | I/O  | UART1 serial data in /<br>DDR memory debug source port ID1 /<br>Secondary DDR memory debug source port ID1 /<br>LBC debug source port ID 1, ↑ 10k | X1-159     |
| UART1_CTS# /<br>M1SRCID2 /<br>M2SRCID2 /<br>LSRCID2 | C34     | I/O  | UART1 clear to send /<br>DDR memory debug source port ID2 /<br>Secondary DDR memory debug source port ID2 /<br>LBC debug source port ID 2, ↑ 10k  | X1-153     |
| UART1_RTS# /<br>M1SRCID3 /<br>M2SRCID3 /<br>LSRCID3 | A35     | O    | UART1 ready to send /<br>DDR memory debug source port ID3 /<br>Secondary DDR memory debug source port ID3 /<br>LBC debug source port ID 3         | X1-157     |
| <b>QUICC engine Block</b>                           |         |      |   |            |
| CE_PA0  | F8      | I/O  | QUICC engine parallel port A 0 (MSB)  | X8-1       |
| CE_PA1  | AH1     | I/O  | QUICC engine parallel port A 1  | X8-2       |
| CE_PA2  | AG5     | I/O  | QUICC engine parallel port A 2  | X8-3       |
| CE_PA3  | F6      | I/O  | QUICC engine parallel port A 3  | X8-4       |
| CE_PA4  | D4      | I/O  | QUICC engine parallel port A 4  | X8-6       |
| CE_PA5  | C3      | I/O  | QUICC engine parallel port A 5  | X8-7       |
| CE_PA6  | E5      | I/O  | QUICC engine parallel port A 6  | X8-8       |
| CE_PA7  | A3      | I/O  | QUICC engine parallel port A 7  | X8-9       |
| CE_PA8  | AG3     | I/O  | QUICC engine parallel port A 8  | X8-10      |
| CE_PA9  | F7      | I/O  | QUICC engine parallel port A 9  | X8-11      |
| CE_PA10   | B3      | I/O  | QUICC engine parallel port A 10   | X8-54      |
| CE_PA11   | E6      | I/O  | QUICC engine parallel port A 11   | X8-55      |
| CE_PA12   | B4      | I/O  | QUICC engine parallel port A 12   | X8-56      |
| CE_PA13   | AG1     | I/O  | QUICC engine parallel port A 13   | X8-51      |
| CE_PA14   | AF6     | I/O  | QUICC engine parallel port A 14   | X8-52      |
| CE_PA15   | B2      | I/O  | QUICC engine parallel port A 15   | X3-156     |
| CE_PA16   | AF4     | I/O  | QUICC engine parallel port A 16   | X8-57      |
| CE_PA17   | B16     | I/O  | QUICC engine parallel port A 17   | X3-155     |
| CE_PA18   | A16     | I/O  | QUICC engine parallel port A 18   | X3-154     |
| CE_PA19   | E17     | I/O  | QUICC engine parallel port A 19   | X3-153     |
| CE_PA20   | A17     | I/O  | QUICC engine parallel port A 20   | X3-152     |
| CE_PA21   | B17     | I/O  | QUICC engine parallel port A 21   | X3-151     |
| CE_PA22   | AF3     | I/O  | QUICC engine parallel port A 22   | X8-13      |
| CE_PA23   | C18     | I/O  | QUICC engine parallel port A 23   | X3-150     |
| CE_PA24   | D18     | I/O  | QUICC engine parallel port A 24   | X3-149     |
| CE_PA25   | E18     | I/O  | QUICC engine parallel port A 25   | X3-148     |
| CE_PA26   | A18     | I/O  | QUICC engine parallel port A 26   | X3-147     |
| CE_PA27   | AF2     | I/O  | QUICC engine parallel port A 27   | X8-14      |
| CE_PA28   | AE6     | I/O  | QUICC engine parallel port A 28   | X8-15      |
| CE_PA29   | B19     | I/O  | QUICC engine parallel port A 29   | X8-58      |
| CE_PA30   | AE5     | I/O  | QUICC engine parallel port A 30   | X8-16      |
| CE_PA31   | F16     | I/O  | QUICC engine parallel port A 31 (LSB)   | X8-59      |

| Signal                    | CPU pin | Type | Description                          | Module pin |
|---------------------------|---------|------|--------------------------------------|------------|
| <b>QUICC engine Block</b> |         |      |                                      |            |
| CE_PB0                    | AE2     | I/O  | QUICC engine parallel port B 0 (MSB) | X1-21      |
| CE_PB1                    | AE1     | I/O  | QUICC engine parallel port B 1       | X1-22      |
| CE_PB2                    | AD5     | I/O  | QUICC engine parallel port B 2       | X1-23      |
| CE_PB3                    | AD3     | I/O  | QUICC engine parallel port B 3       | X1-24      |
| CE_PB4                    | AD2     | I/O  | QUICC engine parallel port B 4       | X1-25      |
| CE_PB5                    | AC6     | I/O  | QUICC engine parallel port B 5       | X1-26      |
| CE_PB6                    | AC5     | I/O  | QUICC engine parallel port B 6       | X1-27      |
| CE_PB7                    | AC4     | I/O  | QUICC engine parallel port B 7       | X1-28      |
| CE_PB8                    | AC2     | I/O  | QUICC engine parallel port B 8       | X1-31      |
| CE_PB9                    | AC1     | I/O  | QUICC engine parallel port B 9       | X1-32      |
| CE_PB10                   | AB5     | I/O  | QUICC engine parallel port B 10      | X1-33      |
| CE_PB11                   | AB4     | I/O  | QUICC engine parallel port B 11      | X1-34      |
| CE_PB12                   | AB3     | I/O  | QUICC engine parallel port B 12      | X1-35      |
| CE_PB13                   | AB1     | I/O  | QUICC engine parallel port B 13      | X1-41      |
| CE_PB14                   | AA6     | I/O  | QUICC engine parallel port B 14      | X1-42      |
| CE_PB15                   | AA4     | I/O  | QUICC engine parallel port B 15      | X1-43      |
| CE_PB16                   | AA2     | I/O  | QUICC engine parallel port B 16      | X1-47      |
| CE_PB17                   | Y6      | I/O  | QUICC engine parallel port B 17      | X1-48      |
| CE_PB18                   | Y4      | I/O  | QUICC engine parallel port B 18      | X1-49      |
| CE_PB19                   | Y3      | I/O  | QUICC engine parallel port B 19      | X1-50      |
| CE_PB20                   | Y2      | I/O  | QUICC engine parallel port B 20      | X1-53      |
| CE_PB21                   | Y1      | I/O  | QUICC engine parallel port B 21      | X1-54      |
| CE_PB22                   | W6      | I/O  | QUICC engine parallel port B 22      | X1-55      |
| CE_PB23                   | W5      | I/O  | QUICC engine parallel port B 23      | X1-56      |
| CE_PB24                   | W2      | I/O  | QUICC engine parallel port B 24      | X1-57      |
| CE_PB25                   | V5      | I/O  | QUICC engine parallel port B 25      | X1-58      |
| CE_PB26                   | V3      | I/O  | QUICC engine parallel port B 26      | X1-59      |
| CE_PB27                   | V2      | I/O  | QUICC engine parallel port B 27(LSB) | X1-60      |
| CE_PC0                    | V1      | I/O  | QUICC engine parallel port C 0 (MSB) | X2-23      |
| CE_PC1                    | U6      | I/O  | QUICC engine parallel port C 1       | X2-25      |
| CE_PC2                    | C16     | I/O  | QUICC engine parallel port C 2       | X3-143     |
| CE_PC3                    | A15     | I/O  | QUICC engine parallel port C 3       | X3-144     |
| CE_PC4                    | U4      | I/O  | QUICC engine parallel port C 4       | X2-26      |
| CE_PC5                    | U3      | I/O  | QUICC engine parallel port C 5       | X2-27      |
| CE_PC6                    | T6      | I/O  | QUICC engine parallel port C 6       | X2-28      |
| CE_PC7                    | C19     | I/O  | QUICC engine parallel port C 7       | X8-60      |
| CE_PC8                    | A4      | I/O  | QUICC engine parallel port C 8       | X3-145     |
| CE_PC9                    | C5      | I/O  | QUICC engine parallel port C 9       | X3-146     |
| CE_PC10                   | T5      | I/O  | QUICC engine parallel port C 10      | X2-30      |
| CE_PC11                   | T4      | I/O  | QUICC engine parallel port C 11      | X2-31      |
| CE_PC12                   | T2      | I/O  | QUICC engine parallel port C 12      | X2-32      |
| CE_PC13                   | T1      | I/O  | QUICC engine parallel port C 13      | X2-33      |
| CE_PC14                   | R5      | I/O  | QUICC engine parallel port C 14      | X2-34      |
| CE_PC15                   | R3      | I/O  | QUICC engine parallel port C 15      | X2-35      |
| CE_PC16                   | R1      | I/O  | QUICC engine parallel port C 16      | X2-37      |
| CE_PC17                   | C11     | I/O  | QUICC engine parallel port C 17      | X2-38      |
| CE_PC18                   | D12     | I/O  | QUICC engine parallel port C 18      | X2-79      |
| CE_PC19                   | F13     | I/O  | QUICC engine parallel port C 19      | X2-87      |
| CE_PC20                   | B10     | I/O  | QUICC engine parallel port C 20      | X2-88      |
| CE_PC21                   | C10     | I/O  | QUICC engine parallel port C 21      | X2-92      |
| CE_PC22                   | E12     | I/O  | QUICC engine parallel port C 22      | X2-93      |
| CE_PC23                   | A9      | I/O  | QUICC engine parallel port C 23      | X2-94      |

| Signal                    | CPU pin | Type | Description   | Module pin |
|---------------------------|---------|------|---|------------|
| <b>QUICC engine Block</b> |         |      |   |            |
| CE_PC24                   | B8      | I/O  | QUICC engine parallel port C 24   | X2-95      |
| CE_PC25                   | D10     | I/O  | QUICC engine parallel port C 25   | X2-102     |
| CE_PC26 /<br>RTC_CLK      | A14     | I/O  | QUICC engine parallel port C 26 /<br>RTC input for time base, multiplexed | X1-110     |
| CE_PC27                   | E15     | I/O  | QUICC engine parallel port C 27   | X2-103     |
| CE_PC28                   | B14     | I/O  | QUICC engine parallel port C 28   | X1-152     |
| CE_PC29                   | D15     | I/O  | QUICC engine parallel port C 29   | X1-154     |
| CE_PC30                   | AH2     | I/O  | QUICC engine parallel port C 30(LSB)                                      | X2-106     |
| CE_PD0                    | E11     | I/O  | QUICC engine parallel port D 0 (MSB)                                      | X1-63      |
| CE_PD1                    | D9      | I/O  | QUICC engine parallel port D 1  | X1-64      |
| CE_PD2                    | C8      | I/O  | QUICC engine parallel port D 2  | X1-65      |
| CE_PD3                    | F11     | I/O  | QUICC engine parallel port D 3  | X1-66      |
| CE_PD4                    | A7      | I/O  | QUICC engine parallel port D 4  | X1-67      |
| CE_PD5                    | E9      | I/O  | QUICC engine parallel port D 5  | X1-68      |
| CE_PD6                    | C7      | I/O  | QUICC engine parallel port D 6  | X1-69      |
| CE_PD7                    | A6      | I/O  | QUICC engine parallel port D 7  | X1-70      |
| CE_PD8                    | F10     | I/O  | QUICC engine parallel port D 8  | X1-73      |
| CE_PD9                    | B6      | I/O  | QUICC engine parallel port D 9  | X2-1       |
| CE_PD10                   | D7      | I/O  | QUICC engine parallel port D 10   | X2-2       |
| CE_PD11                   | E8      | I/O  | QUICC engine parallel port D 11   | X2-3       |
| CE_PD12                   | B5      | I/O  | QUICC engine parallel port D 12   | X2-4       |
| CE_PD13                   | A5      | I/O  | QUICC engine parallel port D 13   | X2-6       |
| CE_PD14                   | C2      | I/O  | QUICC engine parallel port D 14   | X2-7       |
| CE_PD15                   | E4      | I/O  | QUICC engine parallel port D 15   | X2-8       |
| CE_PD16                   | F5      | I/O  | QUICC engine parallel port D 16   | X2-9       |
| CE_PD17                   | B1      | I/O  | QUICC engine parallel port D 17   | X2-10      |
| CE_PD18                   | D2      | I/O  | QUICC engine parallel port D 18   | X2-11      |
| CE_PD19                   | G5      | I/O  | QUICC engine parallel port D 19   | X2-13      |
| CE_PD20                   | D1      | I/O  | QUICC engine parallel port D 20   | X2-14      |
| CE_PD21                   | E2      | I/O  | QUICC engine parallel port D 21   | X2-15      |
| CE_PD22                   | H6      | I/O  | QUICC engine parallel port D 22   | X2-16      |
| CE_PD23                   | F3      | I/O  | QUICC engine parallel port D 23   | X2-18      |
| CE_PD24                   | E1      | I/O  | QUICC engine parallel port D 24   | X2-19      |
| CE_PD25                   | F2      | I/O  | QUICC engine parallel port D 25   | X2-20      |
| CE_PD26                   | G3      | I/O  | QUICC engine parallel port D 26   | X2-21      |
| CE_PD27                   | H4      | I/O  | QUICC engine parallel port D 27(LSB)                                      | X2-22      |
| CE_PE0                    | K3      | I/O  | QUICC engine parallel port E 0 (MSB)                                      | X8-18      |
| CE_PE1                    | J2      | I/O  | QUICC engine parallel port E 1  | X8-19      |
| CE_PE2                    | F1      | I/O  | QUICC engine parallel port E 2  | X8-20      |
| CE_PE3                    | G2      | I/O  | QUICC engine parallel port E 3  | X8-21      |
| CE_PE4                    | J5      | I/O  | QUICC engine parallel port E 4  | X8-22      |
| CE_PE5                    | H3      | I/O  | QUICC engine parallel port E 5  | X8-23      |
| CE_PE6                    | G1      | I/O  | QUICC engine parallel port E 6  | X8-25      |
| CE_PE7                    | H2      | I/O  | QUICC engine parallel port E 7  | X8-26      |
| CE_PE8                    | K6      | I/O  | QUICC engine parallel port E 8  | X8-27      |
| CE_PE9                    | J3      | I/O  | QUICC engine parallel port E 9  | X8-28      |
| CE_PE10                   | K5      | I/O  | QUICC engine parallel port E 10   | X8-30      |
| CE_PE11                   | K4      | I/O  | QUICC engine parallel port E 11   | X8-31      |
| CE_PE12                   | L6      | I/O  | QUICC engine parallel port E 12   | X8-32      |
| CE_PE13                   | P6      | I/O  | QUICC engine parallel port E 13   | X8-33      |
| CE_PE14                   | P4      | I/O  | QUICC engine parallel port E 14   | X8-34      |
| CE_PE15                   | P3      | I/O  | QUICC engine parallel port E 15   | X8-35      |

| Signal                       | CPU pin | Type | Description  | Module pin |
|------------------------------|---------|------|--|------------|
| <b>QUICC engine Block</b>    |         |      |  |            |
| CE_PE16                      | P1      | I/O  | QUICC engine parallel port E 16  | X8-37      |
| CE_PE17                      | N4      | I/O  | QUICC engine parallel port E 17  | X8-38      |
| CE_PE18                      | N5      | I/O  | QUICC engine parallel port E 18  | X8-39      |
| CE_PE19                      | N2      | I/O  | QUICC engine parallel port E 19  | X8-40      |
| CE_PE20                      | N1      | I/O  | QUICC engine parallel port E 20  | X8-42      |
| CE_PE21                      | M2      | I/O  | QUICC engine parallel port E 21  | X8-43      |
| CE_PE22                      | M3      | I/O  | QUICC engine parallel port E 22  | X8-44      |
| CE_PE23                      | M5      | I/O  | QUICC engine parallel port E 23  | X8-45      |
| CE_PE24                      | M6      | I/O  | QUICC engine parallel port E 24  | X8-46      |
| CE_PE25                      | L1      | I/O  | QUICC engine parallel port E 25  | X8-47      |
| CE_PE26                      | L2      | I/O  | QUICC engine parallel port E 26  | X8-49      |
| CE_PE27                      | L4      | I/O  | QUICC engine parallel port E 27  | X8-50      |
| CE_PE28 / SPIMOSI            | E14     | I/O  | QUICC engine parallel port E 28  | X1-140     |
| CE_PE29 / SPIMISO            | C13     | I/O  | QUICC engine parallel port E 29  | X1-141     |
| CE_PE30 / SPICLK             | C14     | I/O  | QUICC engine parallel port E 30  | X1-142     |
| CE_PE31 / SPISEL#            | B13     | I/O  | QUICC engine parallel port E 31(LSB)   | X1-139     |
| CE_PF0 /<br>UART2_SOUT#      | F14     | I/O  | QUICC engine parallel port F 0 /<br>UART2 serial data out  | X1-155     |
| CE_PF1 /<br>UART2_CTS#       | D13     | I/O  | QUICC engine parallel port F 1 /<br>UART2 clear to send  | X1-151     |
| CE_PF2 /<br>UART2_RTS#       | A12     | I/O  | QUICC engine parallel port F 2 /<br>UART2 ready to send  | X1-160     |
| CE_PF3 /<br>UART2_SIN#       | A11     | I/O  | QUICC engine parallel port F 3 /<br>UART2 serial data in   | X1-158     |
| <b>Clocks</b>                |         |      |  |            |
| PCI_CLK_OUT0 /<br>CE_PF26    | B22     | I/O  | PCI clock out 0 /<br>QUICC engine parallel port F 26   | X1-111     |
| PCI_CLK_OUT1 /<br>CE_PF27    | D22     | I/O  | PCI clock out 1 /<br>QUICC engine parallel port F 27   | X1-109     |
| PCI_CLK_OUT2 /<br>CE_PF28    | A23     | I/O  | PCI clock out 2 /<br>QUICC engine parallel port F 28   | X1-44      |
| CLKIN                        | E37     | I/O  | Clock input, connected to the clock generator  | X1-103     |
| PCI_SYNC_IN /<br>PCI_CLOCK   | M36     | I    | PCI clock sync input /<br>PCI clock, feedback from PCI_SYNC_OUT for flight<br>time adjustment                  | X1-112     |
| PCI_SYNC_OUT<br>/<br>CE_PF29 | D37     | I/O  | PCI clock sync output /<br>QUICC Engine parallel I/O<br>feedback to PCI_SYNC_OUT for flight time adjustment    | X1-114     |
| <b>Debug Test</b>            |         |      |  |            |
| TCK                          | K33     | I    | Test clock, $\uparrow$ 10k   | X1-124     |
| TDI                          | K34     | I    | Test data in   | X1-125     |
| TDO                          | H37     | O    | Test data out  | X1-128     |
| TMS                          | J36     | I    | Test mode select   | X1-126     |
| TRST#                        | L32     | I    | Test reset   | X1-127     |
| TEST_SEL /<br>TEST_SEL#      | AU34    | I    | Test mode (MPC8360) /<br>Test mode# (MPC8358)<br>Don't connect!  | X1-76      |
| <b>Reset</b>                 |         |      |  |            |
| PORESET#                     | L37     | O    | Power-on reset, connected to Voltage Supervisor<br>Output with $\rightarrow$ 680 $\Omega$ (see Illustration 2) | X1-122     |
| HRESET#                      | L36     | I/O  | Hard reset, $\uparrow$ 10k   | X1-119     |
| SRESET#                      | M33     | I/O  | Soft reset, $\uparrow$ 1k5   | X1-123     |

| Signal                 | CPU pin  | Type  | Description  | Module pin   |
|------------------------|--|-------|--|--|
| <b>Miscellaneous</b>   |  |       |  |  |
| QUIESCE#               | B36  | O     | QUIESCENT state  | X1-120   |
| SPARE1                 | B11  | I/O   | Spare 1  | X1-98  |
| SPARE2                 | AH32   | I/O   | Spare 2, must be left unconnected  | X1-91  |
| SPARE4                 | AU18   | I/O   | Spare 4, ↓ 0 Ω   | X1-96  |
| SPARE5                 | AP1  | I/O   | Spare 5, must be left unconnected  | X1-89  |
| <b>Non-CPU signals</b> |  |       |  |  |
| CLKOE                  | 1  | I     | Internal 66.666 MHz enable, ↑ 4k7  | X1-137   |
| RESIN#                 | 1  | I     | Reset Input (of voltage supervisor), ↑ 4k7   | X1-135   |
| SEL_RESET_SOURCE       | 1  | I     | Select reset source, Tri-state input, see 3.2.3.1  | X2-120   |
| SEL_CLKIN_DIV          | 1  | I     | Select CLK divider, Tri-state input, see 3.2.3.1   | X2-119   |
| TEMP_OS#               | 1  | O, OC | Temperature sensor excess temperature shutdown output, ↑ 10k   | X1-131   |
| RTC_INT#               | 1  | O, OC | Real time clock interrupt outputs INTA# and SQW / INTB# connected together, ↑ 10k via Schottky diode to VCC3V3 | X1-129   |
| SIN1                   | 1  | I     | UART1 serial in data, RS232 level  | X1-148   |
| SOUT1                  | 1  | O     | UART1 serial out data, RS232 level   | X1-150   |
| SIN2                   | 1  | I     | UART2 serial in data, RS232 level  | X1-147   |
| SOUT2                  | 1  | O     | UART2 serial out data, RS232 level   | X1-149   |
| R /B#                  | 1  |       | ↑ 10k  | X1-74  |
| Not connected          | X1-18, X1-81, X1-82, X1-83, X1-84, X1-85, X1-86, X1-88, X1-90, X1-92, X1-105, X1-118, X1-132, X1-133<br>X2-113, X2-114, X2-115, X2-116, X2-117, X2-118<br>X3-2, X3-19, X3-22, X3-77, X3-79, X3-80, X3-81, X3-83, X3-84, X3-85, X3-86, X3-88, X3-89, X3-90, X3-91,<br>X3-92, X3-93, X3-95, X3-96, X3-97, X3-98, X3-100, X3-101, X3-102, X3-103, X3-104, X3-105, X3-107, X3-108,<br>X3-109, X3-110, X3-112, X3-113, X3-114, X3-115, X3-116, X3-117, X3-119, X3-120, X3-121, X3-122, X3-124,<br>X3-125, X3-126, X3-127, X3-128, X3-129, X3-131, X3-132, X3-133, X3-134, X3-136, X3-137, X3-138, X3-139,<br>X3-140, X3-157, X3-158, X3-159, X3-160 |       |  |  |
| <b>Power Supply</b>    |  |       |  |  |
| VBAT                   | 1  | V     | Battery Voltage, connected directly to RTC supply pin and OR'ed with VCC3V3 via Schottky Diode                 | X1-17  |
| VCC3V3IF               | 7  | V     | 3.3 V supply, filtered DC/DC converter input voltage   | X1-10, X1-11, X1-12, X1-13, X1-14, X1-15, X1-16      |
| VCC3V3ID               | 9  | V     | 3.3 V supply, filtered directly used for 3.3 V logic   | X1-1, X1-2, X1-3, X1-4, X1-5, X1-6, X1-7, X1-8, X1-9 |
| VCC3V3                 | 1  | V     | Internal 3.3 V supply after power sequencing switch, use only for LVDD[0:2] supply !                           | X1-134   |
| VCC2V5                 | 1  | V     | Internal 2.5 V supply, use only for LVDD[0:2] supply !   | X1-138   |
| LVDD0                  | 1  | V     | TSEC0 I/O supply voltage, connect to either VCC3V3 or VCC2V5, depending on Physical Interface Mode             | X1-75  |
| LVDD1                  | 1  | V     | TSEC1 I/O supply voltage, connect to either VCC3V3 or VCC2V5, depending on Physical Interface Mode             | X1-136   |
| LVDD2                  | 1  | V     | TSEC2 I/O supply voltage, connect to either VCC3V3 or VCC2V5, depending on Physical Interface Mode             | X1-143   |
| DGND                   | X1-19, X1-20, X1-29, X1-30, X1-39, X1-40, X1-45, X1-46, X1-51, X1-52, X1-61, X1-62, X1-71, X1-72, X1-77,<br>X1-78, X1-87, X1-94, X1-101, X1-107, X1-108, X1-113, X1-116, X1-121, X1-130, X1-145, X1-146<br>X2-5, X2-12, X2-17, X2-24, X2-29, X2-36, X2-41, X2-48, X2-53, X2-60, X2-65, X2-72, X2-77, X2-84, X2-89,<br>X2-96, X2-101, X2-108<br>X3-5, X3-14, X3-21, X3-30, X3-37, X3-46, X3-53, X3-62, X3-69, X3-75, X3-76, X3-82, X3-87, X3-94, X3-99,<br>X3-106, X3-111, X3-118, X3-123, X3-130, X3-135, X3-141, X3-142<br>X8-5, X8-12, X8-17, X8-24, X8-29, X8-36, X8-41, X8-48, X8-53   |       |  |  |

### 3.5 Cooling

#### 3.5.1 Power dissipation

Maximum power consumption of the module (667/333/500 MHz Core/DDR/QE): 17.93 W

#### 3.5.2 Heat sink

The necessary heat sink depends on the mode of operation (e.g., clock frequency, installation height, airflow), and can therefore not be defined universally.

### 3.6 Mechanics

#### 3.6.1 General information

- High pin count SMD plug connectors with 0.8 mm pitch
- The combination with different counterparts allow, customisation of the stack height to the height of the parts mounted on the base board
- Double-sided SMD assembly

#### 3.6.2 Dimensions

- Board dimensions 77 mm x 75 mm (see Illustration 8)
- Stack height see the following table

| Stack height without heat sink<br>max. a + b + c | Free stack height under module<br>min. a – d | Stack height without heat sink in the area of the SDRAM |
|--|--|---|
| 10.9 mm  | 2.1 mm                                       | 8.6 mm  |

Table 11: Stack heights

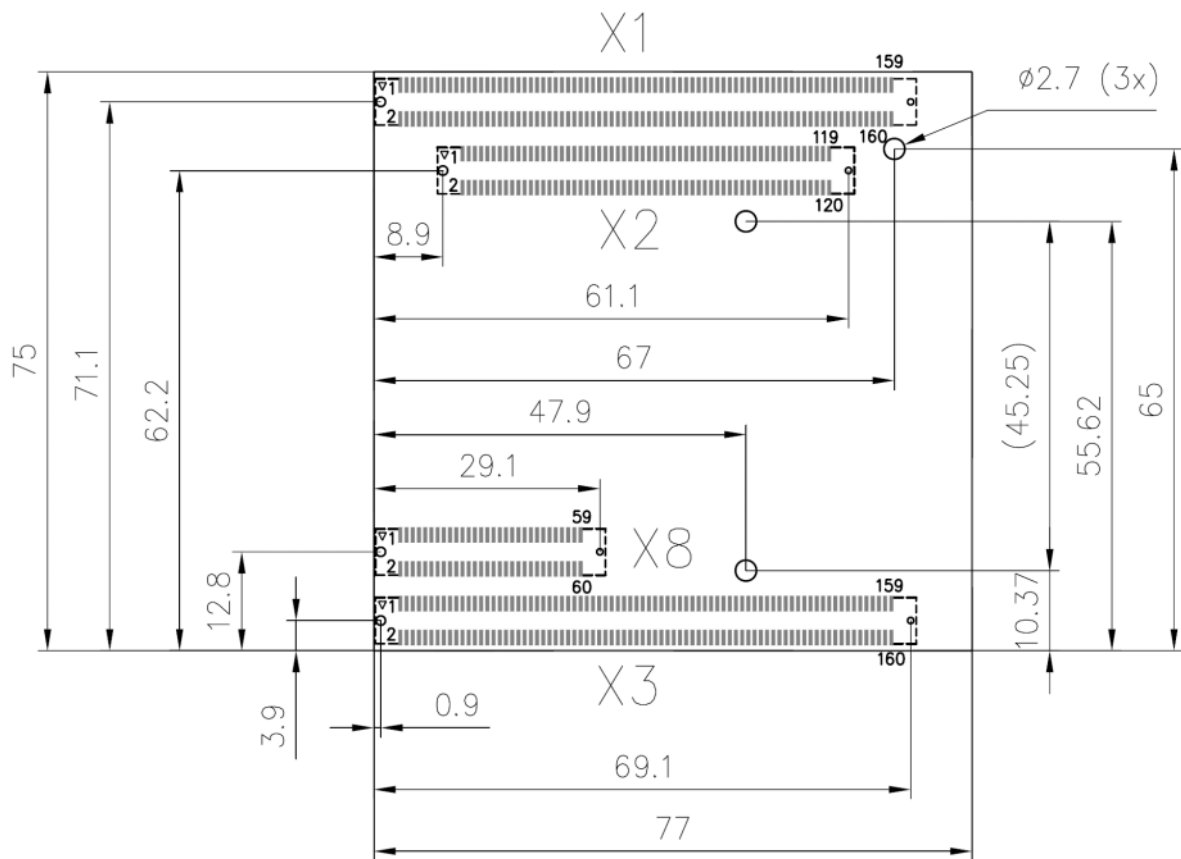



Illustration 8: Top view through the printed circuit board

|   |   |
|---|---|
|  | <p>To avoid damages caused by mechanical stress, it is recommended to extract the TQM8360L from the target hardware only by using the special extraction tool MOZI85xx.</p> |
| <p><b>! note !</b></p>  | <p>2.5 mm should be kept free on the target hardware along the longitudinal edges on both sides of the module for the extraction tool MOZI85xx.</p>                         |

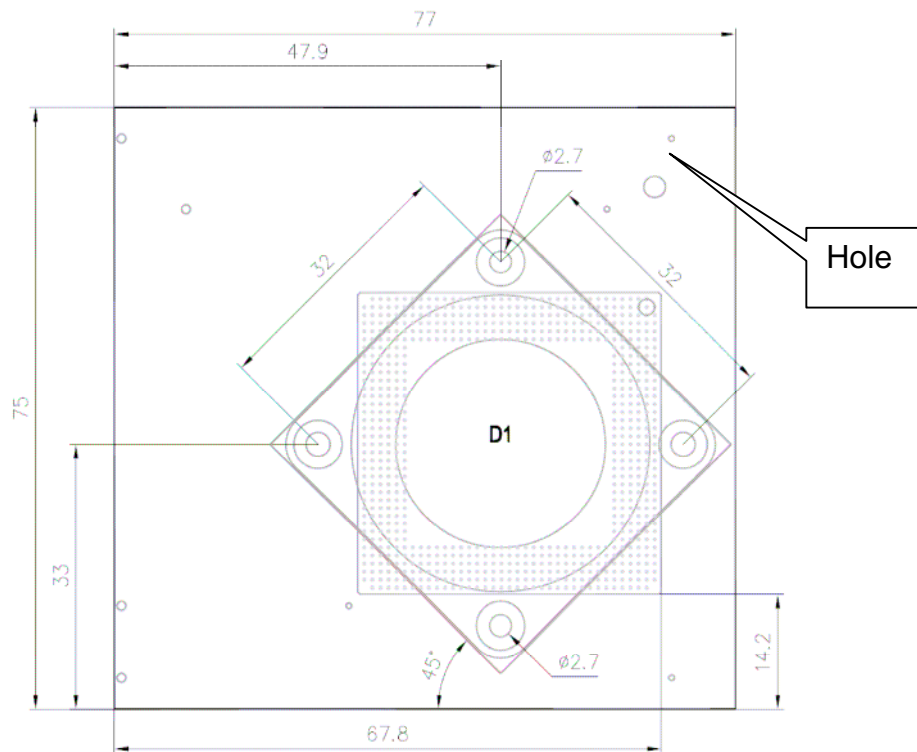


Illustration 9: Position of the CPU and mounting holes for cooling

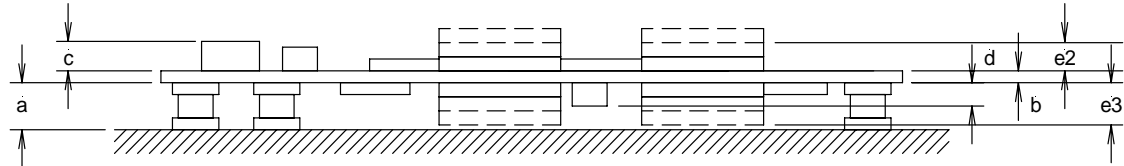


Illustration 10: Stack heights

| Dim. | Value [mm] | Remark  |
|------|------------|---|
| a    | 5.0 ±0.2   | Combination connector with mating plug (with other connectors on the target hardware heights of 6, 7 or 8 mm are also possible) |
| b    | 2.05 ±0.1  | Printed circuit board   |
| c    | 3.4 ±0.4   | Coil L1 (maximum height at the upper side)  |
| d    | 2.5 ±0.2   | Ceramic capacitors type 1210 (maximum height at the lower side)   |

Table 12: Height dimensions

### 3.6.3 Notes of treatment

To avoid damages caused by mechanical stress, the TQM8360L may only be extracted from the base board by using the extraction tool MOZI85xx. This extraction tool is delivered with the Starterkit STK85xx. It can, however, also be obtained separately.

### 3.7 Boot loader

The boot loader "U-Boot" is the basic software delivered with the TQM8360L. For more information see separate specification.

### 3.8 Safety requirements and protective regulations

#### 3.8.1 EMC

The module was developed carefully according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- With metal casings, a good (at least according to RF) connection to the printed circuit board or to the potential of the housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding
- Filtering of all signals which can be connected externally (also "slow" signals and DC can radiate RF indirectly)

#### 3.8.2 ESD

In order to avoid interspersions on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the base board, no special preventive measures were planned on the module. According to the data sheets, the used devices already have some protection; however, this is generally not sufficient to fulfil the legal requirements without any further measures.

Following measures are recommended:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Z-diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

### 3.9 Climate conditions and operational conditions

Protection class IP00

Relative air humidity (operation / storing): 10 % to 90 % (not condensing)

The possible temperature range strongly depends on the installation situation, (heat dissipation by conduction and convection). Hence, no fixed value can be given for the whole assembly. Reliable operation is generally given when the following conditions are met:

Model standard temperature range:

Die-temperature of the CPU 0 °C ... +105 °C

Package temperature of the remaining ICs 0 °C ... +70 °C

Model extended temperature range:

Die-temperature of the CPU -40 °C ... +105 °C

Package temperature of the remaining ICs -40 °C ... +85 °C

Detailed information to the thermal characteristics of the CPU is found in [2]. Information about example configurations with active and passive cooling can be obtained from TQC support.

### 3.10 Reliability and service life

The module is designed for a service life of 10 years.

It was also designed to be insensitive to vibration and impact.

### 3.11 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that there is presently still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (**polychlorinated biphenyls**).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94  
(source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96  
(source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98  
(source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01  
(source of information: BGBl I 2001, 3379)

This information is to be considered as remarks. There are no considerations for tests or certifications concerning this matter.

## 4. Appendix

### 4.1 References

- [1] MPC8360E PowerQUICC II Pro  
Integrated Communications Processor Family Reference Manual  
MPC8360ERM Rev. 2, Freescale Semiconductor Inc. 5/2007
- [2] MPC8360E/58E PowerQUICC™ II Pro Processor Revision 2.0 Silicon  
Hardware Specifications  
Advance Information / Freescale Confidential Proprietary  
MPC8360EEC Rev. 0, Freescale Semiconductor Inc. 09/2006
- [3] Chip Errata for the MPC8360E  
MPC8360ECE Rev. 1, Freescale Semiconductor Inc. 12/2006

### 4.2 Recommended reading

- [4] High Speed Digital Design  
A Handbook of Black Magic  
Howard Johnson, Martin Graham, Prentice Hall 1993
- [5] High Speed Signal Propagation  
Advanced Black Magic  
Howard Johnson, Martin Graham, Prentice Hall 2003