

For Technology
in Quality



User's Manual

TQM5329

TQM5329 UM 200

05.11.2010

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Revision history

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1. About this manual

1.1 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.


1.2 Terms and conventions

Symbol / Tag	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed with the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages greater than 24V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
! note !	This symbol represents important details or aspects for working with TQ-products.
Filename.ext	This specification is used to state the complete file name with its corresponding extension.
Instructions / Examples	Examples of an application. e.g., <ul style="list-style-type: none"> • specifying memory partitions • processing a script •
Reference	Cross-reference to another section, figure or table.


Table 1: Terms and conventions

1.3 Handling and ESD tips

General handling of your TQ-products

	<p>The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations.</p> <p>A general rule is: not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system was switched off.</p> <p>Violation of this guideline may result in damage / destruction of the module and be dangerous to your health.</p> <p>Improper handling of your TQ-product would render the guarantee invalid.</p>
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Proper ESD handling

	<p>The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD).</p> <p>Always wear antistatic clothing and use ESD-safe tools, packing materials etc. and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.</p>
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1.8 Acronyms and definitions

The following terminology and abbreviations are used:

Acronym	Meaning
BDM	Background Debug Mode
BGA	Ball Grid Array
CAN	Controller Area Network
CCR	Clock/Control Register
CPU	Central Processing Unit
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FEC	Fast Ethernet Controller
FIT	Failure In Time
FR-4	Flame Retardant-4
GPIO	General Purpose Input/Output
HMI	Human-Machine Interface
I ² C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
MOZI	Module extractor (Modulzieher)
MSB	Most Significant Bit
MTBF	Mean operating Time Between Failures
OTG	On-The-Go
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
QSPI	Queued Serial Peripheral Interface
RAM	Random Access Memory
RCON	Reset Configuration Register
RF	Radio Frequency
RFU	Reserved for Future Use
ROM	Read Only Memory
RTC	Real Time Clock
RoHS	Restriction of Hazardous Substances
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSI	Synchronous Serial Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WD	Watchdog

Table 2: Acronyms

2. Brief description

The TQM5329 is a TQC module with TQ-standard dimensions of 54 mm × 44 mm. It is equipped with the Freescale CPU MCF5329. The available pin-compatible CPU MCF5328 has no CAN controller. The ColdFire CPU MCF5329 distinguishes itself from other CPUs by its low power dissipation and attractive price with extensive functionality. This product is especially suited for small display solutions for visualisation and HMI.

The CPU MCF5329 contains functional units such as Ethernet, CAN controller, SPI, UART, timer, memory controller and LCD controller. These functional units are complemented by an address/data bus called FlexBus. Not all available functional units can be used independently of each other. The I/Os of the individual functional units are switched to the CPU pins by CPU-internal multiplexers.

The CPU is complemented with SDR SDRAM and flash memory. Further peripheral units on the module are the ISL12028, which contains the supervisor, watchdog, RTC and EEPROM. Another peripheral unit, the MAX3353, contains the charge pump, which is necessary for the USB On-The-Go mode, as well as pull-up / pull-down resistors for the USB signals.

The supply voltage for the TQM5329 is 3.3 V. The core voltage for the CPU is provided by a switching regulator on the module.

All CPU pins, which can be used on the target hardware, are led to the module plug connectors. The control signals of the SDR SDRAM controller are not available at the module plug connectors, as they are only needed locally. Due to signal integrity and EMC no additional SDR SDRAM should be connected on the target hardware.

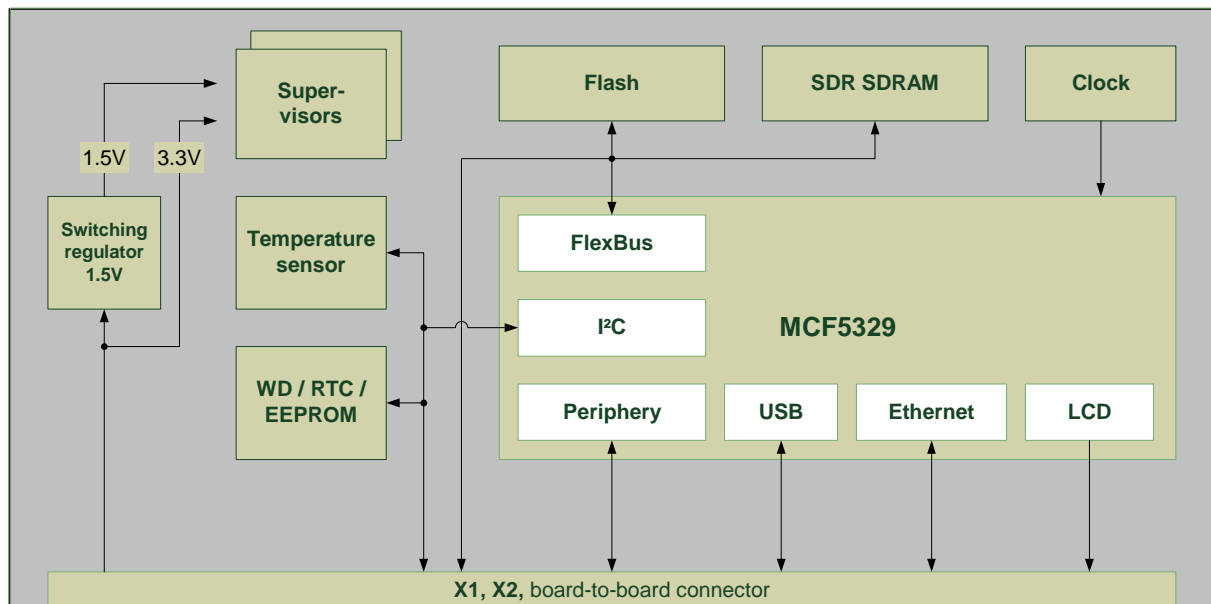


Illustration 1: Simple block diagram of the TQM5329

3. Technical data

3.1 Overview

3.1.1 Block diagram

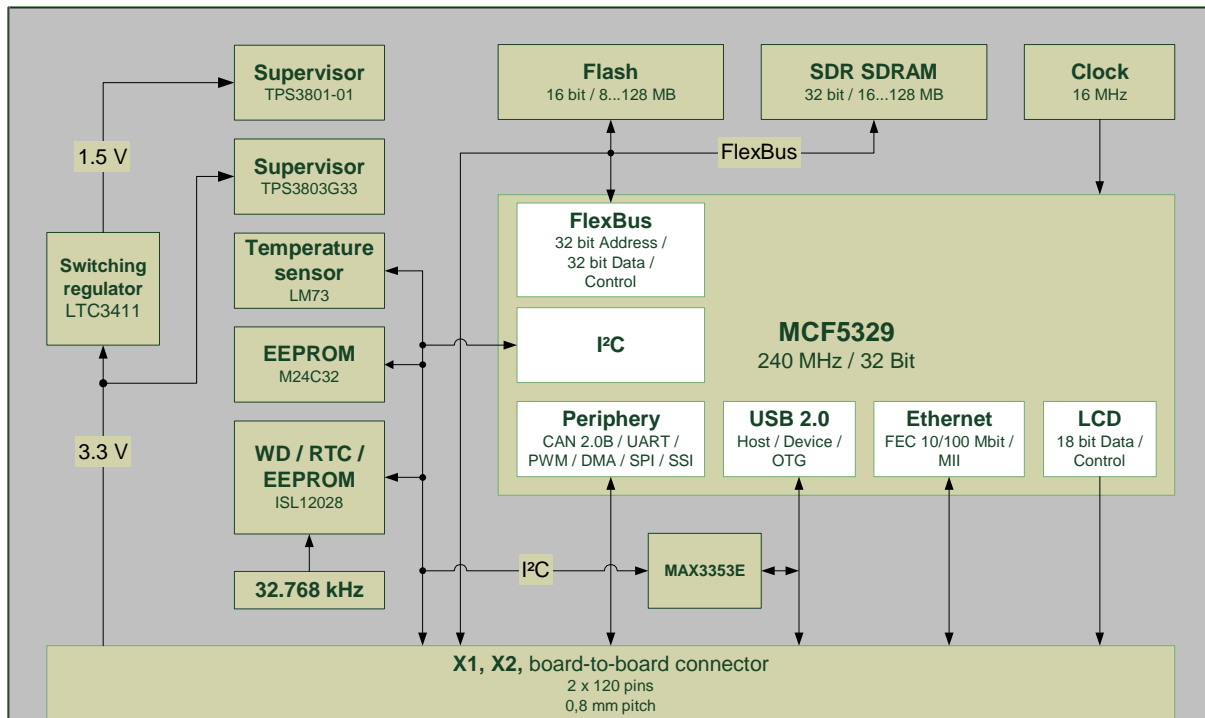


Illustration 2: Block diagram of the TQM5329

3.1.2 System components

Module comes with

- Freescale CPU MCF5329 or MCF5328
- SDR SDRAM 16 Mbyte, 32 Mbyte (default), 64 Mbyte or 128 Mbyte
- Flash ROM 8 Mbyte, 16 Mbyte (default), 32 Mbyte, 64 Mbyte or 128 Mbyte
- USB OTG charge pump
- Watchdog / RTC / EEPROM
- Temperature sensor
- Power supply 1.5 V
- Voltage supervision 1.5 V and 3.3 V

4. Electronics specification

4.1 CPU

Attention: Malfunction!	
	Please pay attention to the current errata of the individual Freescale CPU.

4.2 Pin multiplexing

The pin multiplexing enables, depending on the configuration, pins to be allocated for different purposes.

Attention: Destruction or malfunction!	
	Many of the CPU pins permit the use of up to four different configurations. Concerning the wiring of these pins please consult the MCF5329 Reference Manual before integration / start-up of your target hardware / Starterkit.

4.3 Reset system

The following illustration shows the generation and the utilisation of the reset signals of the TQM5329.

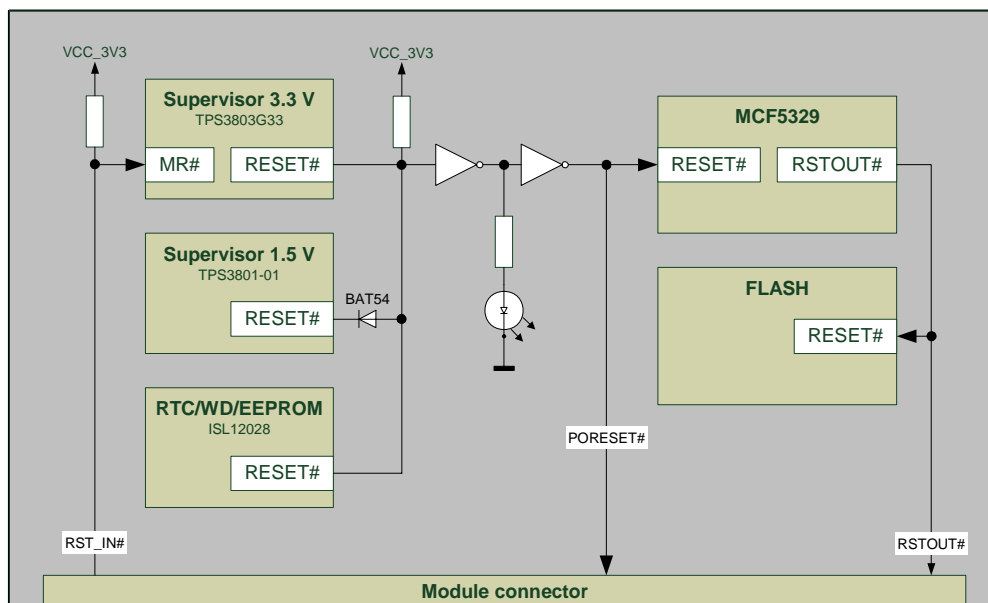


Illustration 3: Diagram reset system

The reset inputs of the MCF5329 and the flash remain low and therefore in reset until all supervisors and the watchdog supply a high level. RSTOUT# is a CPU signal and is available at the module plug connector. The correct use of this signal is described in the Freescale data sheet. This information should be adhered to.

During power up (before the set operating voltage thresholds are reached or with their undercut) the voltage supervision circuits of the power supply trigger the Power-On reset. This signal is also available at the module plug connector and should be loaded with no more than 20 mA.

PORESET# is also set if the watchdog is not served and, therefore, triggers. By means of supervision of PORESET# the state of the CPU can be monitored.

The signal RST_IN# from the module plug connector allows an external reset of the module. To trigger a valid reset, RST_IN# must be low for at least 100 ns.

Attention: Malfunction!



It is to be taken into consideration that the I/O pins can supply any value during the reset phase. Thereby the data of non-volatile memory is endangered if, e.g., the chip select of a battery-buffered RAM is selected unintentionally. To avoid undesirable effects, these circumstances have to be taken into consideration during the design of a customised target hardware.

4.4 Power-On configuration

The data pins of the Power-On configuration are actively driven by an 8-fold bus driver SN74LVC245A. Its inputs are connected by means of pull-up / pull-down configuration according to the entries in Table 3. The inputs of the driver are designed with two resistors with a common pad, to enable changes of the configuration by an alternative assembly.

During Power-On reset the configuration data is read and written in CPU registers.

The relevant CPU registers are RCON (Reset Configuration Register) and CCR (Chip Configuration Register), which are read-only registers, during normal operation.

If an 8 Mbyte flash is used, RCON[9:8] can be configured to "10", to make the signal CS5# available on the module plug connector.

The following principle diagram displays the implementation of the bus driver to generate the Power-On configuration of the MCF5329.

4.4.1 **Default configuration of the MCF5329**

Default configuration	Override pins in reset	Function		Pin(s) affected	
RCON[1] = 1	D1	PLL mode: 0 = 180/60 MHz operation 1 = 240/80 MHz operation		None	
RCON[2] = 0	D2	Oscillator mode: 0 = Crystal oscillator mode 1 = Oscillator bypass mode		None	
RCON[4:3] = 01	D[4:3]	Boot device: 00 = External with 32 bit port 01 = External with 16 bit port 10 = External with 8 bit port 11 = External with 32 bit port		None	
RCON[5] = 0	D5	Output pad drive strength: 0 = Low drive strength 1 = High drive strength		All output pins	
RCON[6] = 0	D6	Limp mode: 0 = PLL mode 1 = Limp mode		None	
RCON[9:8] = 00	D[9:8]	Chip select configuration:		A[23:22] / FB_CS[5:4]	
		00: A[23:22] = A[23:22]			16 Mbyte / 32 Mbyte / 64 Mbyte
		01: Reserved			/
		10: A23 = FB_CS5 and A22 = A22			8 Mbyte
		11: A[23:22] = FB_CS[5:4]			/

Table 3: Default Power-On configuration

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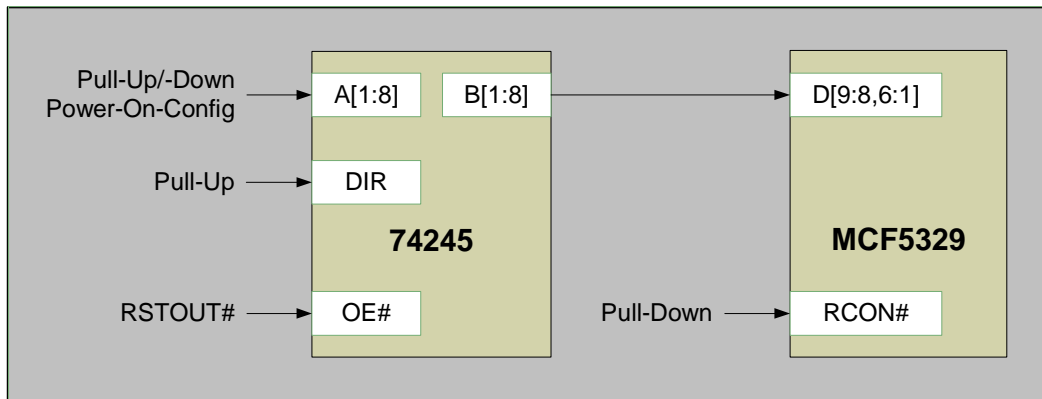


Illustration 4: Detailed diagram Power-On configuration

Attention: Destruction or malfunction!	
	An altered Power-On configuration can lead to an unusable module!

4.5 Clock concept

As displayed in the following illustration, the clock sources required by the MCF5329 are provided on the module. The basic CPU clock is 16 MHz. The clock frequency of the core (up to 240 MHz) is generated by a PLL.

The RTC of the ISL12028 is operated with a quartz crystal (32.768 kHz). The USB clock is derived from the system clock. The SDRAM clock SDR SDCLK is generated by the RAM controller. The powered FBCLK is provided for external function units at the FlexBus.

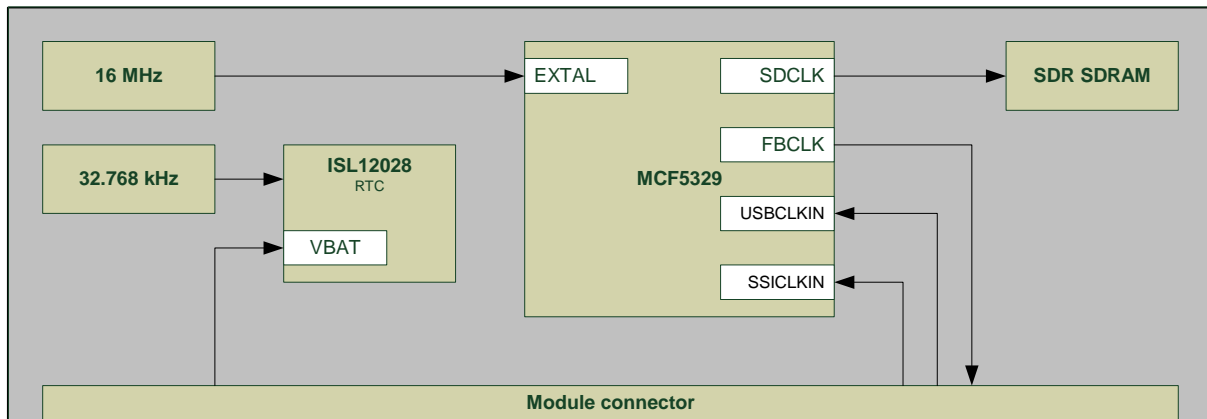


Illustration 5: Clock concept

4.6 FlexBus

The SDR SDRAM is 32 bit wide and the flash is 16 bit wide connected to the MCF5329 via the FlexBus. To be able to connect external peripheral devices, the corresponding address and data lines are available at the module plug connector.

If external peripheral devices are connected the maximum allowed fan out and the reflecting behaviour of the lines have to be taken into consideration. If bus drivers have to be used, they have to be provided on the target hardware.

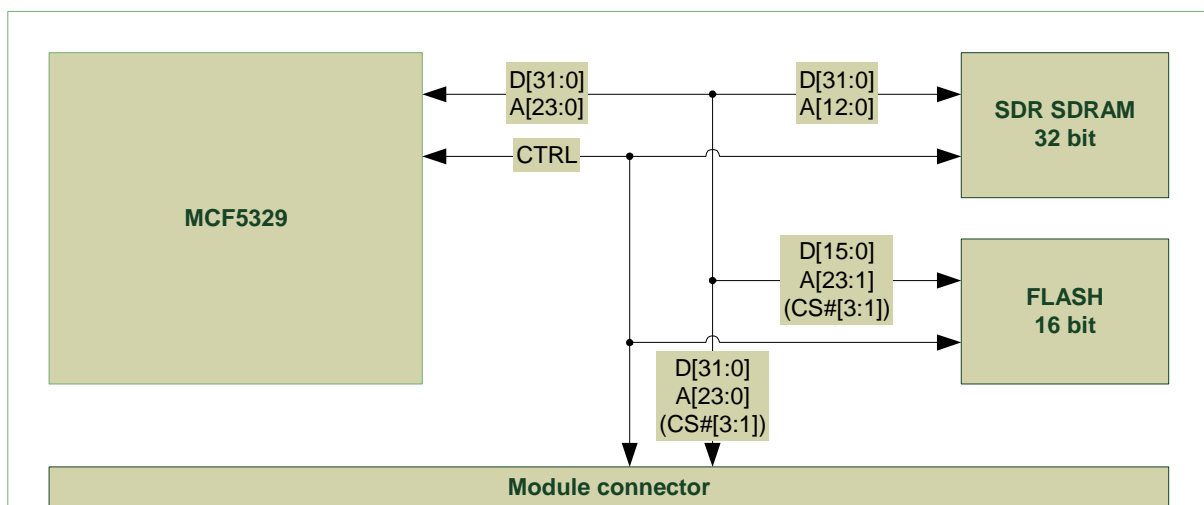


Illustration 6: Connection of data / addresses to the FlexBus

4.6.1 FlexBus DRAM interface

The DRAM interface of the MCF5329 is configurable. It is not independent of the FlexBus and, therefore, must always be taken into consideration. The following configuration was selected:

Type of memory	Width	SDRAMSEL	FlexBus data	FlexBus address
SDR SDRAM	32 bit	1	D[31:0]	A[12:0]

Table 4: Operation mode of the DRAM interface

4.7 SDR SDRAM

4.7.1 Supported memory

As an alternative the following devices can be assembled on the TQM5329:

Manu- facturer	64 Mbit (16 bit bus)	128 Mbit (16 bit bus)	256 Mbit (16 bit bus)	512 Mbit (16 bit bus)
ISSI	IS42S16400D-7TL	IS42S16800D-7TL	IS42S16160B-7TL	IS42S16320B-7TL
Samsung	K4S641632K-UC75	K4S281632I-UC75	K4S561632H-UC75	K4S511632D-UC75
Micron	MT48LC4M16A2P-75	MT48LC8M16A2P-75	MT48LC16M16A2P-75	MT48LC32M16A2P-75
Hynix	HY57V641620ET	HY57V281620ET(P)	HY57V561620CT	-

Table 5: Memory devices SDR SDRAM

The 128 Mbit IS42S16800D-7TL of ISSI is the default device. To provide a memory width of 32 bits, two memory devices are assembled on the TQM5329. A memory size of 32 Mbyte is achieved in this way.

4.7.2 Connection to the MCF5329

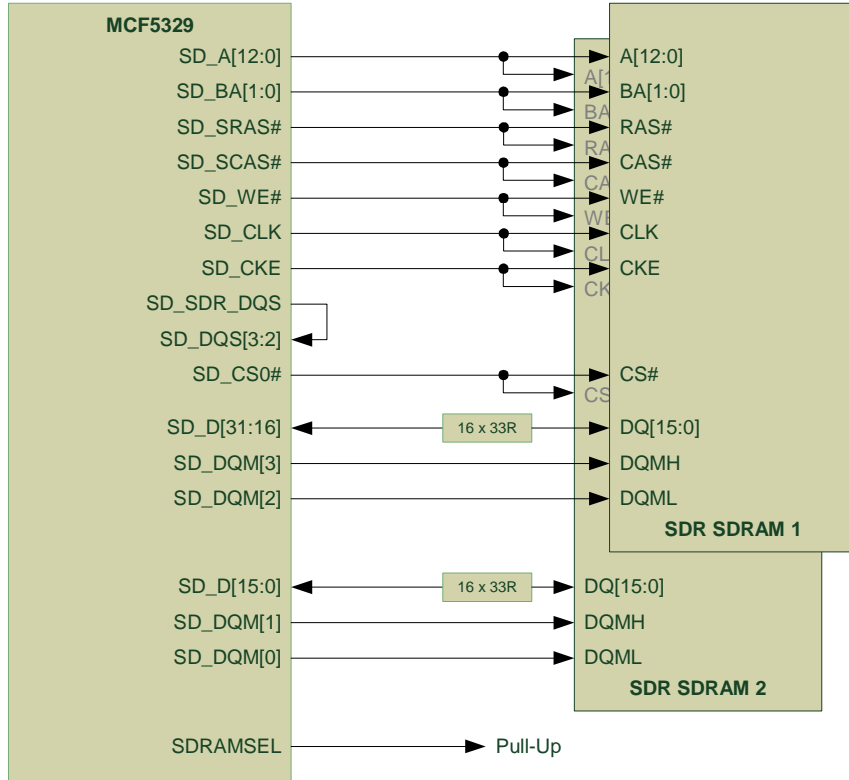


Illustration 7: Connection SDR SDRAM

4.8 Flash

4.8.1 Supported memory

Different sizes of flash are available. The flash devices are NOR flash.

Manu- facturer	64 Mbit (16 bit bus)	128 Mbit (16 bit bus)	256 Mbit (16 bit bus)	512 Mbit (16 bit bus)	1 Gbit (16 bit bus)
Numonyx	PC28F064M29EWL	PC28F128M29EWL	PC28F256M29EWL	PC28F512M29EWL	PC28F00AM29EWL

Table 6: Flash memory devices

Numonyx 128 Mbit PC28F128M29EWL is assembled by default, to achieve a memory size of 16 Mbyte.

In order to achieve a memory width of 32 bit, two memory modules are assembled on the TQM5329.

4.8.2 Connection to the MCF5329

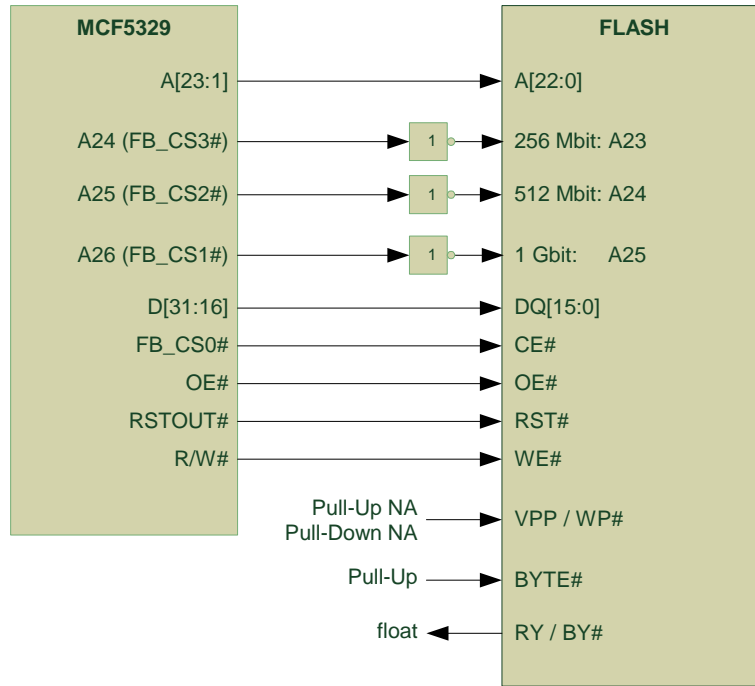


Illustration 8: Connection flash

4.8.3 Address map flash

Illustration 9 shows the creation of the additional address signals A[26:24] of the CPU, if the module is equipped with 32 Mbyte, 64 Mbyte or 128 Mbyte of flash memory.

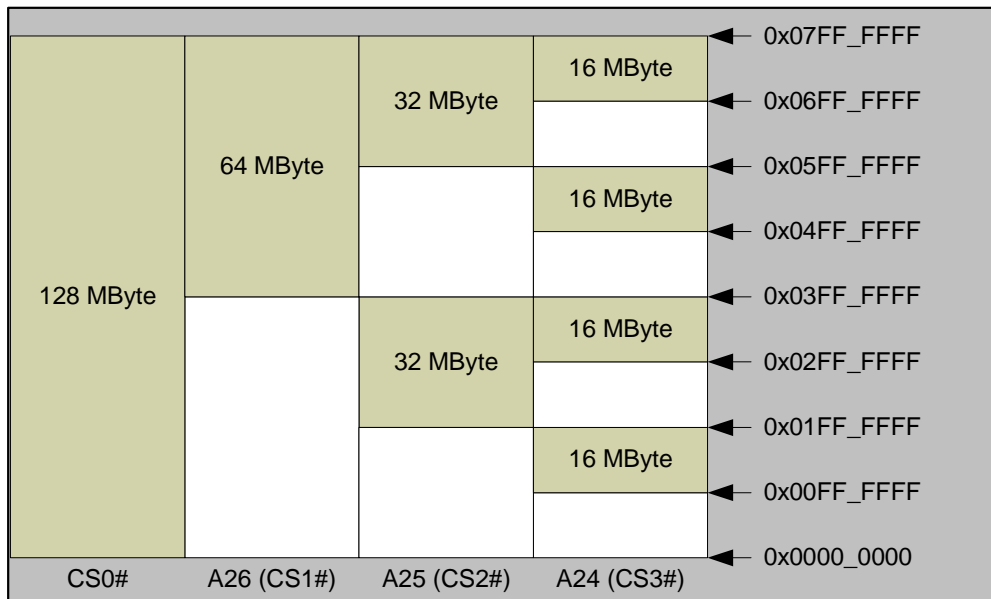


Illustration 9: Address map of the flash

4.8.4 Usable chip selects

The following table shows the chip select signals usable at the module plug connectors as a function of the size of the available flash memory.

Size of flash [Mbit]	Size of flash [Mbyte]	FB_CS4	FB_CS5	FB_CS3	FB_CS2	FB_CS1	FB_CS0
64	8	A22	free ¹	free	free	free	CS flash
128	16	A22	A23	free	free	free	
256	32	A22	A23	A24	free	free	
512	64	A22	A23	A24	A25	free	
1024	128	A22	A23	A24	A25	A26	

Table 7: Usable chip selects

4.8.5 Flash CS definitions

Table 8 shows the address masks for the respective chip select signals.

Chip select	Mask type	Address mask	Remark
CS0	BA BAM	0x0000 0x07FF	128 Mbyte from 0
CS1	BA BAM	0x0400 0x03FF	64 Mbyte from 64 Mbyte
CS2	BA BAM	0x0200 0x05FF	32 Mbyte from 32 Mbyte, 96 Mbyte
CS3	BA BAM	0x0100 0x06FF	16 Mbyte from 16 Mbyte, 48 Mbyte, 80 Mbyte, 112 Mbyte

Table 8: CS definitions flash

4.9 RTC, watchdog

The RTC and the watchdog are implemented by the ISL12028 of Intersil.

VBAT voltage range	1.8 V to 5.5 V
Max. current consumption	1.2 μ A
Time deviation (with 20 ppm crystal)	\pm 10 min / year

Table 9: Technical parameters battery for RTC ISL12028

¹ Free according to assembly option of the Power-On configuration

A necessary capacity of at least 10.51 mAh per year results from these parameters. Furthermore, the voltage may not drop below 1.8 V. The backup battery is not a part of the TQM5329 and must be implemented on the target hardware.

To be able to signal a malfunction in case of clock generation failure of the CPU of the superior assembly, the watchdog function is implemented externally. The CPU internal watchdog cannot be used, as it is out of order if no clock is available.

The I²C address of the EEPROM is 0b1010111, the address of the clock / control unit is 0b1101111 (address map I²C bus see Table 11).

4.10 EEPROM

Besides the 512 byte EEPROM contained in the ISL12028 (RTC, WD), an additional EEPROM type M24C32-WDW6TP of 4 Kbyte size is implemented on the TQM5329. It is connected via the local I²C bus. On the target hardware further EEPROMs can be connected via I²C.

The I²C address of the EEPROM is set to 0b1010000 (address map I²C bus see Table 11). Pull-up resistors are provided as an assembly option at the inputs E[0:2] of the EEPROM, which represent the three LSBs of the I²C address. The I²C address of the EEPROM can thereby be configured afterwards.

4.11 Temperature sensor

A temperature sensor LM73CIMK-0/NOPB is used, which can be read via I²C.

The I²C address of the sensor is set to 0b1001000 (address map I²C bus see Table 11). A pull-up and a pull-down resistor are provided as an assembly option at the input ADDR of the sensor, which influences the last two LSBs of the I²C address. The I²C address of the sensor can thereby be configured afterwards.

The temperature sensor is placed on the component side of the module and is in the area of the CPU (see Illustration 12: D9).

4.12 USB

4.12.1 USB host

Table 16 on page 31 shows the pinout of the module plug connector X2 with the signals of the USB host interface. The signals D+ and D- are directly connected via series resistors between MCF5329 and X2 (see Illustration 10). Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

4.12.2 USB OTG

On the target hardware additional filtering and EMC protection circuitry has to be provided for the USB signals. Tips and hints can be found in the USB standard and in the data sheet of the MCF5329 from Freescale.

A MAX3353EEUE+ (USB On-The-Go charge pump with switchable pull-up / pull-down resistors) is assembled on the TQM5329. It enables the USB OTG operation modes.

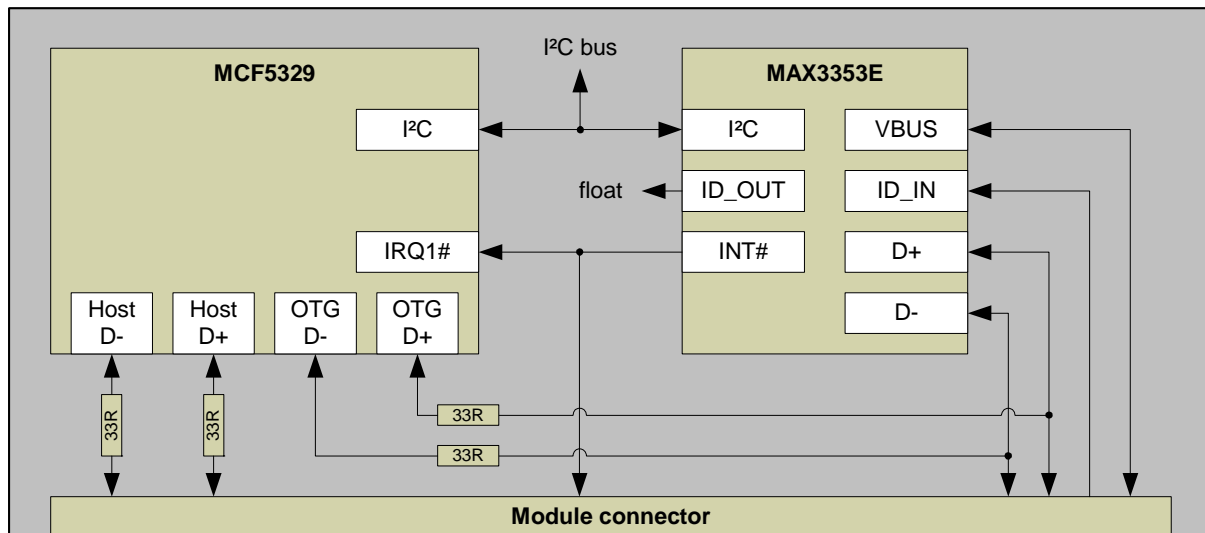


Illustration 10: Connection of USB OTG charge pump

The signals VBUS, ID_IN, D+, D- are standard USB signals (see USB standard).

The I²C address of the MAX3353EEUE+ is 0b0101100 (address map I²C bus see Table 11). A pull-up resistor is provided as an assembly option at the input ADD of the MAX3353EEUE+, which represents the LSB of the I²C address. The I²C address of the MAX3353EEUE+ can thereby be configured afterwards. If not assembled (default) the input is interpreted as (0).

4.13 LCD controller

Table 15 on page 28 shows the pinout of the module plug connector X1 with the signals of the LCD controller. The signals are directly connected between the MCF5329 and X1. Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

4.14 Fast Ethernet controller

Table 15 on page 28 shows the pinout of the module plug connector X1 with the signals of the FEC. The signals are directly connected between the MCF5329 and X1. Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

4.15 UARTs

Table 15 on page 28 shows the pinout of the module plug connector X1 with the signals of the UART. The signals are directly connected between the MCF5329 and X1. Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

4.16 Serial interfaces

Table 10 shows the configuration possibilities of the serial interfaces provided by the MCF5329. To complete the table UART0 is also listed. The highlighted entries show the chosen configuration. With it the assignment to the corresponding signals of the CPU pins are fixed. In Table 10, the interfaces, which can be used simultaneously, are also shown.

	Signal	BGA ball	UART2	I ² C	FlexCAN	SSI
UART0	U0CTS#	R15				
	U0RTS#	T15				
	U0RXD	R14				
	U0TXD	T14				
UART1	U1CTS#	D11				SSI_BCLK
	U1RTS#	E10				SSI_FS
	U1RXD	E12				SSI_RXD
	U1TXD	E11				SSI_TXD
I ² C	I2C_SCL	F3	1_U2TXD	1_I2C	1_CANTX	
	I2C_SDA	F2	1_U2RXD		1_CANRX	
QSPI	QSPI_CS2	T12	1_U2RTS#			
	QSPI_CLK	R12		2_I2C_SCL		
	QSPI_DIN	N12	1_U2CTS#			
	QSPI_DOUT	P12		2_I2C_SDA		
SSI	SSI_BCLK	F4	2_U2CTS#			2_SSI
	SSI_FS	G3	2_U2RTS#			
	SSI_RXD	G2	2_U2RXD		2_CANRX	
	SSI_TXD	G1	2_U2TXD		2_CANTX	
FEC	FEC_MDC	C1		3_I2C_SCL		
	FEC_MDIO	C2		3_I2C_SCL		
DT	DT2IN	E1	3_U2TXD			
	DT3IN	F1	3_U2RXD			
LCD	LCD_D17	C9			3_CANTX	
	LCD_D16	D9			3_CANRX	

Table 10: Signals serial interface

4.17 I²C

Table 15 on page 28 shows the pinout of the module plug connector X1 with the signals of the I²C bus. The signals are directly connected between the MCF5329 and X1. Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

The following table shows the I²C address map. If a device offers an address setting, corresponding pull-up or pull-down resistors are provided at the address inputs.

Device	Address range of the device	Chosen address
USB-OTG MAX3353	0x2C...0x2D	0x2C / 0b0101100
EEPROM M24C32	0x50...0x57 ²	0x50 / 0b1010000
Temperature sensor LM73	0x48...0x4A	0x48 / 0b1001000
ISL12028 (EEPROM)	0x57	0x57 / 0b1010111
ISL12028 (CCR)	0x6F	0x6F / 0b1101111

Table 11: I²C address map

4.18 FlexCAN

Table 15 on page 28 shows the pinout of the module plug connector X1 with the signals of the FlexCAN. The signals are directly connected between the MCF5329 and X1. Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

FlexCAN is only available with CPU type MCF5329.

4.19 QSPI, SSI, PWM, DMA

Table 15 and Table 16 on pages 28 and 31 show the pinout of the module plug connectors X1 and X2 with the signals of the corresponding function units. The signals are directly connected between the MCF5329 and X1 or X2. Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

4.20 External interrupt ports

Table 16 on page 31 shows the pinout of the interrupt signals at the module plug connector X2. The signals are directly connected between the MCF5329 and X2. Pull-up or pull-down resistors are marked as a footnote in the column „Dir“. All pull-up resistors at the interrupt port are provided by the CPU.

On the TQM5329 IRQ1# is used as the USB OTG interrupt.

² Attention: 0x57 is already used by the EEPROM ISL12028.

4.21 BDM, JTAG

Table 16 on page 31 shows the pinout of the BDM/JTAG signals at the module plug connector X2. The signals are directly connected between MCF5329 and X2. Pull-up or pull-down resistors, which could be necessary, are marked as a footnote in the column "Dir". The value of the resistor is described in section 4.26 on page 26.

4.22 GPIO

As a second configuration or multiple configurations in combination with other function units the CPU MCF5329 offers GPIO ports for a large number of pins. For the configuration please refer to the Freescale reference manual.

4.23 Diagnosis LED

A red LED is implemented. It serves to indicate the state of the signal PORESET#.

PORESET#	LED
H	OFF
L	ON

Table 12: Truth-table diagnosis LED

4.24 Supply

The TQM5329 is supplied with 3.3 V via the module plug connectors of the target hardware. The maximum tolerance of the supply voltage is $\pm 5\%$. The power consumption distribution (worst case values) of the components can be estimated as follows:

Device	3.3 V	1.5 V
MCF5329 (@240 MHz; memory clock 80 MHz)	48 mA	133 mA
MCF5329 SDRAM-IF	34 mA	-
SDR SDRAM	221 mA	-
Flash (programming)	90 mA	-
RTC/WD/EEPROM	4 mA	-
USB OTG charge pump	25 mA	-
Total:	422 mA	133 mA

Table 13: Current consumption TQM5329

No driver currents for external signals (FlexBus, FEC,) and no USB supply currents were taken into account for the estimation.

4.25 Module plug connectors

The TQM5329 is connected by a total of 240 pins on two module plug connectors to the target hardware. The board is held with a considerable holding force by the plug connectors. It is advisable to use an extraction tool like the available MOZI8xx).

Module				Target hardware connector		Board-to-board distance
No. of pins	Qty	Supplier	Order No.	Supplier	Order No.	
120	2	tyco	5177985-5	tyco	5177984-5	5 mm
				tyco	5179029-5	6 mm
				tyco	5179030-5	7 mm
				tyco	5179031-5	8 mm

Table 14: Module plug connector and mating connectors

4.26 Pins assignment of module plug connectors

The multiple configuration of the CPU pins by different CPU internal function units has to be taken note of.

Whether a pull-up or pull-down resistor is already implemented on the TQM5329 is noted in column „Dir“. The abbreviation “CPU” in column „Dir“ indicates that the corresponding resistor is provided by the MCF5329. The resistance value for the I²C signals is 4.7 kΩ and 10 kΩ in all other cases.

4.26.1 Module plug connector X1

Pin No. module connector	Port name module	CPU pin function 1	CPU pin function 2	CPU pin function 3	CPU pin function 4	PBGA pin	Dir
X1-1	RFU	-	-	-	-	-	-
X1-2	RFU	-	-	-	-	-	-
X1-3	RFU	-	-	-	-	-	-
X1-4	FEC_MDIO	FEC_MDIO	PFECCI2C2	I2C_SDA	-	C2	I/OPU
X1-5	GND	-	-	-	-	-	P
X1-6	FEC_MDC	FEC_MDC	PFECCI2C3	I2C_SCL	-	C1	I/OPU-CPU
X1-7	FEC_TXD3	FEC_TXD3	PFECL7	ULPI_DATA3	-	D3	I/OPU
X1-8	FEC_TXD2	FEC_TXD2	PFECL6	ULPI_DATA2	-	D2	I/OPU
X1-9	FEC_TXD1	FEC_TXD1	PFECL5	ULPI_DATA1	-	D1	I/OPU
X1-10	FEC_TXD0	FEC_TXD0	PFECH5	ULPI_DATA0	-	E4	I/OPU
X1-11	FEC_TXEN	FEC_TXEN	PFECH6	-	-	B2	O
X1-12	GND	-	-	-	-	-	P
X1-13	FEC_TXER	FEC_TXER	PFECL4	-	-	B1	O
X1-14	FEC_TXCLK	FEC_TXCLK	PFECH7	-	-	A2	I _{PU}
X1-15	GND	-	-	-	-	-	P
X1-16	FEC_CRS	FEC_CRS	PFECH0	ULPI_DIR	-	B8	I _{PU}
X1-17	GND	-	-	-	-	-	P
X1-18	FEC_COL	FEC_COL	PFECH4	ULPI_CLK	-	A8	I/OPU
X1-19	FEC_RXD3	FEC_RXD3	PFECL3	ULPI_DATA7	-	E7	I/OPU
X1-20	FEC_RXD2	FEC_RXD2	PFECL2	ULPI_DATA6	-	A6	I/OPU
X1-21	FEC_RXD1	FEC_RXD1	PFECL1	ULPI_DATA5	-	B6	I/OPU

Pin No. module connector	Port name module	CPU pin function 1	CPU pin function 2	CPU pin function 3	CPU pin function 4	PBGA pin	Dir
X1-22	FEC_RXD0	FEC_RXD0	PFECH1	ULPI_DATA4	-	C6	I/OPU
X1-23	FEC_RXDV	FEC_RXDV	PFECH2	ULPI_STP	-	D8	IPU
X1-24	GND	-	-	-	-	-	P
X1-25	FEC_RXER	FEC_RXER	PFECL0	-	-	D4	IPU
X1-26	FEC_RXCLK	FEC_RXCLK	PFECH3	ULPI_NXT	-	C8	IPU
X1-27	GND	-	-	-	-	-	P
X1-28	U0CTS#	U0CTS#	PUARTL3	-	-	R15	IPU
X1-29	GND	-	-	-	-	-	P
X1-30	U0RTS#	U0RTS#	PUARTL2	-	-	T15	O
X1-31	RFU	-	-	-	-	-	-
X1-32	U1CTS#	U1CTS#	PUARTL7	SSI_BCLK	-	D11	I/OPU
X1-33	U0RXD	U0RXD	PUARTL0	-	-	R14	IPU
X1-34	U1RTS#	U1RTS#	PUARTL6	SSI_FS	-	E10	I/OPU
X1-35	U0TXD	U0TXD	PUARTL1	-	-	T14	O
X1-36	GND	-	-	-	-	-	P
X1-37	U1RXD	U1RXD	PUARTL4	SSI_RXD	-	E12	IPU
X1-38	SCL	I2C_SCL	PFECI2C1	CANTX	U2TXD	F3	I/OPU
X1-39	U1TXD	U1TXD	PUARTL5	SSI_TXD	-	E11	O
X1-40	SDA	I2C_SDA	PFECI2C0	CANRX	U2RXD	F2	I/OPU
X1-41	GND	-	-	-	-	-	P
X1-42	SSI_FS	SSI_FS	PSSI2	U2RTS#	PWM5	G3	I/OPU
X1-43	SSI_MCLK	SSI_MCLK	PSSI4	-	-	G4	I/OPU
X1-44	SSI_RXD	SSI_RXD	PSSI1	U2RXD	CANRX	G2	IPU
X1-45	SSI_TXD	SSI_TXD	PSSI0	U2TXD	CANTX	G1	O
X1-46	SSI_BCLK	SSI_BCLK	PSSI3	U2CTS#	PWM7	F4	I/OPU
X1-47	SPI_SOUT	QSPI_DOUT	PQSPI0	I2C_SDA	-	P12	I/OPU-CPU
X1-48	GND	-	-	-	-	-	P
X1-49	SPI_SIN	QSPI_DIN	PQSPI1	U2CTS#	-	N12	IPU
X1-50	SPI_SCK	QSPI_CLK	PQSPI2	I2C_SCL	-	R12	I/OPU-CPU
X1-51	SPI_CS1	QSPI_CS1	PQSPI4	PWM7	USBOTG_PU_EN	T13	I/O
X1-52	SPI_CS2	QSPI_CS2	PQSPI5	U2RTS#	-	T12	O
X1-53	GND	-	-	-	-	-	P
X1-54	SPI_CS0	QSPI_CS0	PQSPI3	PWM5	-	P11	O
X1-55	TIN3	DT3IN	PTIMER3	DT3OUT	U2RXD	F1	I/OPU
X1-56	TIN2	DT2IN	PTIMER2	DT2OUT	U2TXD	E1	I/OPU
X1-57	TIN1	DT1IN	PTIMER1	DT1OUT	DACK1#	E2	I/OPU
X1-58	TIN0	DT0IN	PTIMER0	DT0OUT	DREQ0#	E3	I/OPU
X1-59	LCD_PS	LCD_PS	PLCDCTLL2	-	-	A11	O
X1-60	GND	-	-	-	-	-	P
X1-61	LCD_REV	LCD_REV	PLCDCTLL1	-	-	B11	O
X1-62	LCD_LSCLK	LCD_LSCLK	PLCDCTLL3	-	-	A10	O
X1-63	LCD_SPL_SPR	LCD_SPL_SPR	PLCDCTLL0	-	-	C11	O
X1-64	LCD_CONTRAST	LCD_CONTRAST	PLCDCTLL6	-	-	D10	O
X1-65	GND	-	-	-	-	-	P
X1-66	LCD_CLS	LCD_CLS	PLCDCTLL7	-	-	A9	O
X1-67	LCD_FLM/LCD_VSYNC	LCD_FLM/LCD_VSYNC	PLCDCTLL5	-	-	C10	O
X1-68	LCD_ACD/LCD_OE	LCD_ACD/LCD_OE	PLCDCTLH0	-	-	B9	O
X1-69	LCD_LP/LCD_HSYNC	LCD_LP/LCD_HSYNC	PLCDCTLL4	-	-	B10	O
X1-70	LCD_D16	LCD_D16	PLCDDH0	CANRX	-	D9	I/OPU

Pin No. module connector	Port name module	CPU pin function 1	CPU pin function 2	CPU pin function 3	CPU pin function 4	PBGA pin	Dir
X1-71	LCD_D17	LCD_D17	PLCDDH1	CANTX		C9	O
X1-72	GND	-	-	-	-	-	P
X1-73	LCD_D15	LCD_D15	PLCDDM7	-		A7	O
X1-74	LCD_D14	LCD_D14	PLCDDM6	-		B7	O
X1-75	LCD_D13	LCD_D13	PLCDDM5	-		C7	O
X1-76	LCD_D12	LCD_D12	PLCDDM4	-		D7	O
X1-77	GND	-	-	-	-	-	P
X1-78	LCD_D10	LCD_D10	PLCDDM2	-		E6	O
X1-79	LCD_D11	LCD_D11	PLCDDM3	-		D6	O
X1-80	LCD_D8	LCD_D8	PLCDDM0	-		B5	O
X1-81	LCD_D9	LCD_D9	PLCDDM1	-		A5	O
X1-82	LCD_D6	LCD_D6	PLCDDL6	-		D5	O
X1-83	LCD_D7	LCD_D7	PLCDDL7	-		C5	O
X1-84	GND	-	-	-	-	-	P
X1-85	LCD_D5	LCD_D5	PLCDDL5	-		A4	O
X1-86	LCD_D4	LCD_D4	PLCDDL4	-		A3	O
X1-87	LCD_D3	LCD_D3	PLCDDL3	-		B4	O
X1-88	LCD_D2	LCD_D2	PLCDDL2	-		C4	O
X1-89	GND	-	-	-	-	-	P
X1-90	LCD_D0	LCD_D0	PLCDDL0	-		C3	O
X1-91	LCD_D1	LCD_D1	PLCDDL1	-		B3	O
X1-92	A22	A22	-	FB_CS4#	-	D13	O
X1-93	A23	A23	-	FB_CS5#	-	C13	O
X1-94	A20	A20	-	-	-	A14	O
X1-95	A21	A21	-	-	-	E13	O
X1-96	GND	-	-	-	-	-	P
X1-97	A19	A19	-	-	-	B14	O
X1-98	A18	A18	-	-	-	C14	O
X1-99	A17	A17	-	-	-	A15	O
X1-100	A16	A16	-	-	-	B15	O
X1-101	GND	-	-	-	-	-	P
X1-102	A14	A14	-	SD_BA0	-	B16	O
X1-103	A15	A15	-	SD_BA1	-	D14	O
X1-104	A12	A12	-	SD_A12	-	C16	O
X1-105	A13	A13	-	SD_A13	-	C15	O
X1-106	A10	A10	-	-	-	D16	O
X1-107	A11	A11	-	SD_A11	-	D15	O
X1-108	GND	-	-	-	-	-	P
X1-109	A9	A9	-	SD_A9	-	E14	O
X1-110	A8	A8	-	SD_A8	-	E15	O
X1-111	A7	A7	-	SD_A7	-	E16	O
X1-112	A6	A6	-	SD_A6	-	F13	O
X1-113	GND	-	-	-	-	-	P
X1-114	A4	A4	-	SD_A4	-	F15	O
X1-115	A5	A5	-	SD_A5	-	F14	O
X1-116	A2	A2	-	SD_A2	-	G16	O
X1-117	A3	A3	-	SD_A3	-	F16	O
X1-118	A0	A0	-	SD_A0	-	G14	O
X1-119	A1	A1	-	SD_A1	-	G15	O
X1-120	GND	-	-	-	-	-	P

Table 15: Pin assignment module plug connector X1

4.26.2 Module plug connector X2

Pin No. module connector	Port name module	CPU pin function 1	CPU pin function 2	CPU pin function 3	CPU pin function 4	PBGA pin	Dir
X2-1	VCC3V3	-	-	-	-	-	P
X2-2	VCC3V3	-	-	-	-	-	P
X2-3	VCC3V3	-	-	-	-	-	P
X2-4	VCC3V3	-	-	-	-	-	P
X2-5	VCC3V3	-	-	-	-	-	P
X2-6	VCC3V3	-	-	-	-	-	P
X2-7	VCC3V3	-	-	-	-	-	P
X2-8	VBAT	-	-	-	-	-	P
X2-9	GND	-	-	-	-	-	P
X2-10	GND	-	-	-	-	-	P
X2-11	GND	-	-	-	-	-	P
X2-12	GND	-	-	-	-	-	P
X2-13	GND	-	-	-	-	-	P
X2-14	GND	-	-	-	-	-	P
X2-15	GND	-	-	-	-	-	P
X2-16	GND	-	-	-	-	-	P
X2-17	GND	-	-	-	-	-	P
X2-18	IRQ6#	IRQ6#	PIRQ6	USBHOST_VBUS_EN	-	J14	I/OPU-CPU
X2-19	IRQ7#	IRQ7#	PIRQ7	-	-	J13	IPU-CPU
X2-20	IRQ4#	IRQ4#	PIRQ4	SSI_MCLK	-	J16	I/OPU-CPU
X2-21	IRQ5#	IRQ5#	PIRQ5	USBHOST_VBUS_OC	-	J15	IPU-CPU
X2-22	IRQ2#	IRQ2#	PIRQ2	USB_CLKIN	-	K15	IPU-CPU
X2-23	IRQ3#	IRQ3#	PIRQ3	-	-	K14	IPU-CPU
X2-24	GND	-	-	-	-	-	P
X2-25	IRQ1#	IRQ1#	PIRQ1	DREQ1#	SSI_CLKIN	K16	IPU-CPU
X2-26	RFU	-	-	-	-	-	-
X2-27	RFU	-	-	-	-	-	-
X2-28	DDATA2	DDATA2	-	-	-	P9	O
X2-29	GND	-	-	-	-	-	P
X2-30	DDATA0	DDATA0	-	-	-	P10	O
X2-31	DDATA3	DDATA3	-	-	-	N9	O
X2-32	PST2	PST2	-	-	-	T10	O
X2-33	DDATA1	DDATA1	-	-	-	N10	O
X2-34	PST0	PST0	-	-	-	T11	O
X2-35	PST3	PST3	-	-	-	R10	O
X2-36	GND	-	-	-	-	-	P
X2-37	PST1	PST1	-	-	-	R11	O
X2-38	JTAG_EN	JTAG_EN	-	-	-	M13	IPD-CPU
X2-39	DSCLK	DSCLK	-	TRST#	-	P15	IPU

Pin No. module connector	Port name module	CPU pin function 1	CPU pin function 2	CPU pin function 3	CPU pin function 4	PBGA pin	Dir
X2-40	DSI	DSI	-	TDI	-	N14	I _{PU}
X2-41	GND	-	-	-	-	-	P
X2-42	DSO	DSO	-	TDO	-	N11	O
X2-43	RSTIN#		-	-	-	-	I _{PU}
X2-44	BKPT#	BKPT#	-	TMS	-	R16	I _{PU}
X2-45	RSTOUT#	RSTOUT#	-	-	-	P14	O
X2-46	PSTCLK	PSTCLK	-	TCLK	-	T9	I/O _{PU}
X2-47	PORESET#	-	-	-	-	N15	O
X2-48	GND	-	-	-	-	-	P
X2-49	USBOTG_VBUS	-	-	-	-	-	P
X2-50	USBOTG_D-	USBOTG_M	-	-	-	L15	I/O
X2-51	USBOTG_ID	-	-	-	-	-	I
X2-52	USBOTG_D+	USBOTG_P	-	-	-	L16	I/O
X2-53	GND	-	-	-	-	-	P
X2-54	GND	-	-	-	-	-	P
X2-55	RFU	-	-	-	-	-	-
X2-56	USB_D-	USBHOST_M	-	-	-	M15	I/O
X2-57	PWM7	PWM7	PPWM7	-	-	H13	I/O _{PU}
X2-58	USB_D+	USBHOST_P	-	-	-	M16	I/O
X2-59	PWM5	PWM5	PPWM5	-	-	H14	O
X2-60	GND	-	-	-	-	-	P
X2-61	PWM3	PWM3	PPWM3	DT3OUT	DT3IN	H15	I/O _{PU}
X2-62	CLKOUT	FB_CLK	-	-	-	T2	O
X2-63	PWM1	PWM1	PPWM1	DT2OUT	DT2IN	H16	I/O _{PU}
X2-64	RFU	-	-	-	-	-	-
X2-65	GND	-	-	-	-	-	P
X2-66	CS4#	FB_CS4#	PCS4	-	-	A13	O
X2-67	CS5#	FB_CS5#	PCS5	-	-	B13	O
X2-68	CS2#	FB_CS2#	PCS2	-	-	B12	O
X2-69	CS3#	FB_CS3#	PCS3	-	-	A12	O
X2-70	CS0#	FB_CS0#	-	-	-	D12	O
X2-71	CS1#	FB_CS1#	PCS1	-	-	C12	O
X2-72	GND	-	-	-	-	-	P
X2-73	TA#	TA#	PBUSCTL2	-	-	G13	I _{PU}
X2-74	R/W#	R/W#	PBUSCTL1	-	-	N8	O
X2-75	TS#	TS#	PBUSCTL0	DACK0#	-	H4	O
X2-76	OE#	OE#	PBUSCTL3	-	-	R9	O
X2-77	GND	-	-	-	-	-	P
X2-78	BE#/BWE2#	BE#/BWE2#	PBE2	SD_DQM2#	-	P6	O
X2-79	BE#/BWE3#	BE#/BWE3#	PBE3	SD_DQM3#	-	L4	O
X2-80	BE#/BWE0#	BE#/BWE0#	PBE0	SD_DQM0#	-	N6	O

Pin No. module connector	Port name module	CPU pin function 1	CPU pin function 2	CPU pin function 3	CPU pin function 4	PBGA pin	Dir
X2-81	BE#/BWE1#	BE#/BWE1#	PBE1	SD_DQM1#	-	L3	O
X2-82	D30	D30	-	SD_D30	-	M2	I/O _{PU}
X2-83	D31	D31	-	SD_D31	-	M1	I/O _{PU}
X2-84	GND	-	-	-	-	-	P
X2-85	D29	D29	-	SD_D29	-	M3	I/O _{PU}
X2-86	D28	D28	-	SD_D28	-	M4	I/O _{PU}
X2-87	D27	D27	-	SD_D27	-	N1	I/O _{PU}
X2-88	D26	D26	-	SD_D26	-	N2	I/O _{PU}
X2-89	GND	-	-	-	-	-	P
X2-90	D24	D24	-	SD_D24	-	N4	I/O _{PU}
X2-91	D25	D25	-	SD_D25	-	N3	I/O _{PU}
X2-92	D22	D22	-	SD_D22	-	P4	I/O _{PU}
X2-93	D23	D23	-	SD_D23	-	T3	I/O _{PU}
X2-94	D20	D20	-	SD_D20	-	T4	I/O _{PU}
X2-95	D21	D21	-	SD_D21	-	R4	I/O _{PU}
X2-96	GND	-	-	-	-	-	P
X2-97	D19	D19	-	SD_D19	-	N5	I/O _{PU}
X2-98	D18	D18	-	SD_D18	-	P5	I/O _{PU}
X2-99	D17	D17	-	SD_D17	-	R5	I/O _{PU}
X2-100	D16	D16	-	SD_D16	-	T5	I/O _{PU}
X2-101	GND	-	-	-	-	-	P
X2-102	D14	D14	-	FB_D30	-	J2	I/O _{PU}
X2-103	D15	D15	-	FB_D31	-	J3	I/O _{PU}
X2-104	D12	D12	-	FB_D28	-	K4	I/O _{PU}
X2-105	D13	D13	-	FB_D29	-	J1	I/O _{PU}
X2-106	D10	D10	-	FB_D26	-	K2	I/O _{PU}
X2-107	D11	D11	-	FB_D27	-	K3	I/O _{PU}
X2-108	GND	-	-	-	-	-	P
X2-109	D9	D9	-	FB_D25	-	K1	I/O _{PU}
X2-110	D8	D8	-	FB_D24	-	L2	I/O _{PU}
X2-111	D7	D7	-	FB_D23	-	R6	I/O _{PU}
X2-112	D6	D6	-	FB_D22	-	N7	I/O _{PU}
X2-113	GND	-	-	-	-	-	P
X2-114	D4	D4	-	FB_D20	-	R7	I/O _{PU}
X2-115	D5	D5	-	FB_D21	-	P7	I/O _{PU}
X2-116	D2	D2	-	FB_D18	-	P8	I/O _{PU}
X2-117	D3	D3	-	FB_D19	-	T7	I/O _{PU}
X2-118	D0	D0	-	FB_D16	-	T8	I/O _{PU}
X2-119	D1	D1	-	FB_D17	-	R8	I/O _{PU}
X2-120	GND	-	-	-	-	-	P

Table 16: Pin assignment module plug connector X2

5. Mechanics specification

- Dimensions (W x D x H): 54 mm x 44 mm x 7.5 mm
- Mounting holes: none
- Board-to-board distance: 5 mm
- Maximum stack height: 9 mm
- Weight: 15 g ±1 g

5.1 Mounting

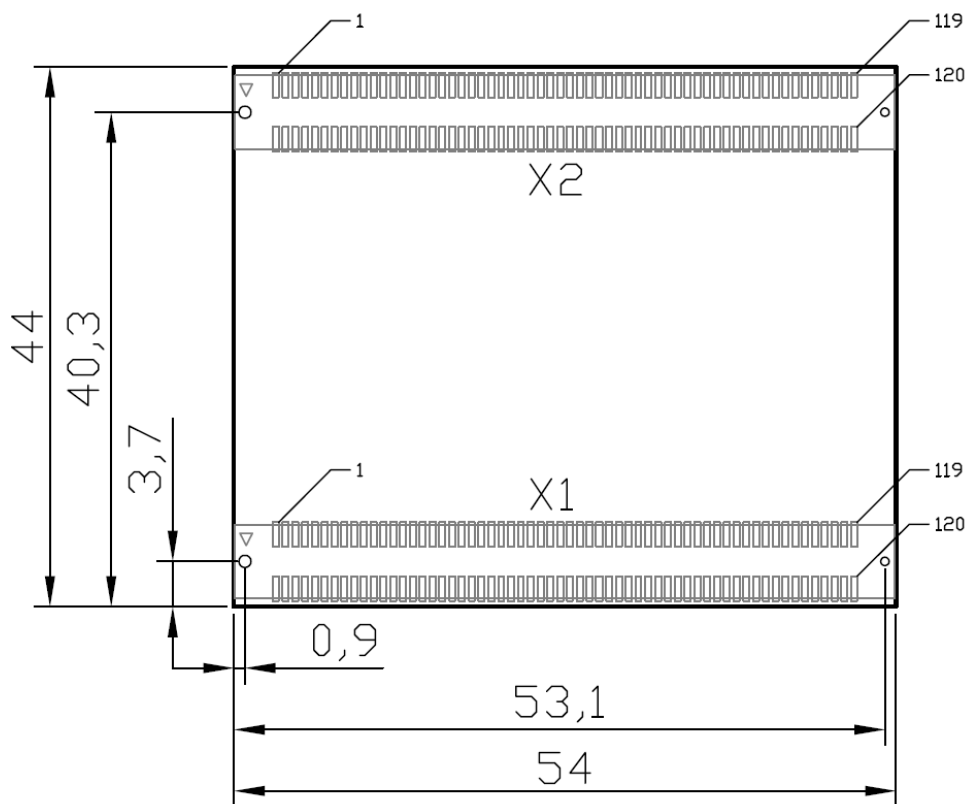


Illustration 11: TQM5329 dimensions

View from top through the board.

Attention: Destruction or malfunction!



To avoid damages due to mechanical stress, the module may only be extracted from the target hardware by use of the extraction tool MOZI8xx.

Therefore an area of 2.5 mm width has to be kept free on the target hardware along the longitudinal edges on both sides of the module for the extraction tool MOZI8xx.

5.2 Top View TQM5329

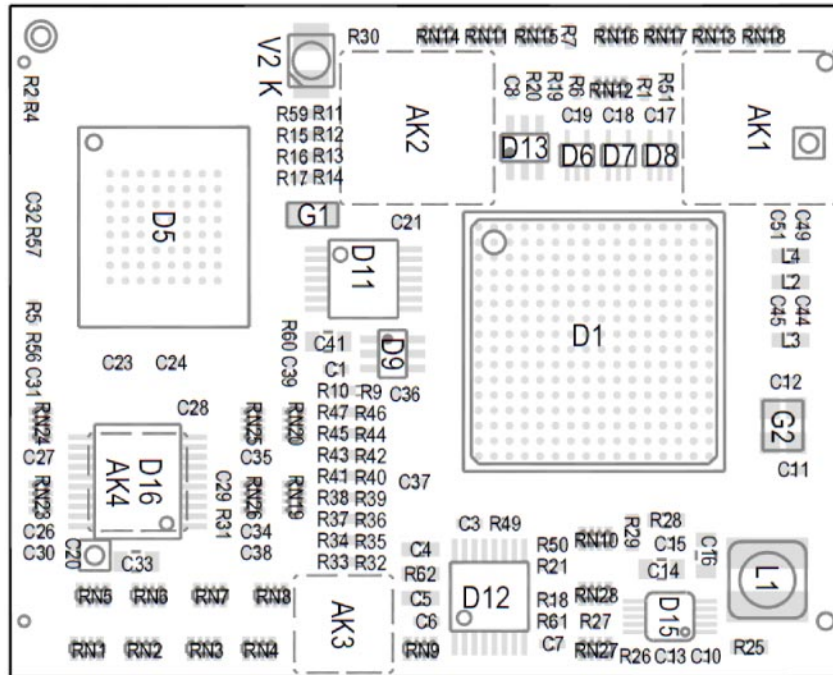


Illustration 12: TQM5329 top view

5.3 Bottom View TQM5329

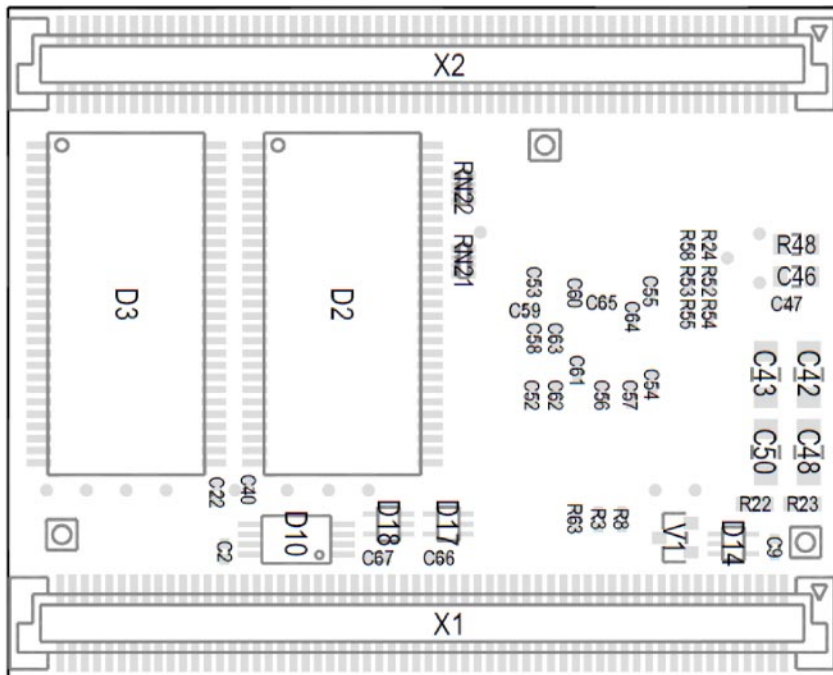


Illustration 13: TQM5329 bottom view

6. Appendix

6.1 Safety requirements and protective regulations

6.1.1 EMC

The module was developed carefully according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- With metal casings, a good (at least according to RF) connection to the printed circuit board or to the potential of the housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding
- Filtering of all signals, which can be connected externally (also "slow" signals and DC can radiate RF indirectly)

6.1.2 ESD

In order to avoid interspersions on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the base board, no special preventive measures were planned on the module. According to the data sheets, the used devices already have some protection; however, this is generally not sufficient to fulfil the legal requirements without any further measures.

Following measures are recommended:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Z-diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

6.1.3 Operational safety and personal security

Due to the occurring voltages (≤ 5 V DC) tests with respect to the operational and personal safety haven't been carried out.

6.2 Climate conditions and operational conditions

Protection class	IP00
Relative air humidity (operation / storing):	10 % to 90 % (not condensing)

The possible temperature range strongly depends on the installation situation, (heat dissipation by conduction and convection). Hence, no fixed value can be given for the whole assembly. Reliable operation is generally given when the following conditions are met:

- Model standard temperature range: 0 °C to +70 °C
- Model extended temperature range: -40 °C to +85 °C

6.3 Reliability and product life

No detailed MTBF calculation has been done for the TQM5329. According to experience the MTBF will be in the range of $MTBF = 1 / FIT = 1 / (800 * 10^{-9} / h) = 1,250,000 \text{ h}$ (40 °C).

Middle grade connectors, which guarantee at least 100 mating cycles, were used for the module.

6.4 RoHS conformity

The module is manufactured RoHS compliant.

- All used components and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

6.5 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that there is presently still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (**polychlorinated biphenyls**).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
(source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
(source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
(source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
(source of information: BGBl I 2001, 3379)

This information is to be considered as remarks. There are no considerations for tests or certifications concerning this matter.

6.6 Requirements for the superior system

6.6.1 Protection against external influences

As an installation module the module is not protected against dust, external influences and direct contact (IP00). Appropriate protection has to be guaranteed by the surrounding system.

6.6.2 Thermal management

For the cooling of the TQM5329 a maximum of approximately 1.85 W has to be dissipated. The power dissipation originates primarily from the CPU and the SDR SDRAM. The customer is responsible for the power dissipation in his application. In most cases a passive cooling should be sufficient.

In a warm environment (more than approximately 40 °C) it can be necessary to mount the TQM5329 "upright" (vertical module plug connectors), to enable a sufficient airflow on both sides of the module for passive cooling.

Attention: Destruction or malfunction!



The CPU belongs to a performance category, which needs to be cooled in certain applications. It is the customer's responsibility to define a suitable heat sink according to the specific operation situation (e.g., by clock frequency, stack height and airflow).

6.6.3 Stability requirements

The TQM5329 is held by the holding force of the pins (a total of 240) in the module socket. If high requirements concerning vibration and shock firmness are essential in the final application a plastic module holder, which holds the module in place, has to be used. TQ-Components offers a standard solution.

No further requirements are given, because no heavy and big components are used.

7. Software specification

The TQM5329 is supplied with a preinstalled boot loader. Information is to be taken from the separate software specification of the TQM5329.