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User Manual

STK85xx

STK85xx.UM.106

27.06.2006

	Datum:	Name:	Description:	User Manual	
Created:	16.06.2006	J.Trepte	Project:	STK85xx	
Checked:	27.06.2006	ROE	Document-No.:	STK85xx.UM.106	
Firma:			Release status:	checked	
			Client:	TQC	Page 1 of 39
File:	C:\N_TQ-C Docs\Documentations\STK85xx\STK85xx.UM.106.doc				Sample revision: 001

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1 About this Manual

This manual contains the technical information about the STK85xx specifications.

1.1 Terms and Conventions

Symbol/Tag	Description
	This symbol represents the handling of electrostatic - sensitive modules and/or components. These components are often damaged/ destroyed with the transmission of a voltage higher than about 50V. Human body usually notices electrostatic discharges only above approximately 3,000V.
	This symbol indicates the possible use of voltages greater than 24V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage/destruction of the component.
	This symbol indicates the possible source of danger. Acting against the procedure described can lead to possible damage to your health and/or cause damage/destruction of the material used.
	This symbol represents important details or aspects for working with TQ products.
Filename.ext	This specification is used to state the complete file name with its corresponding extension.
`Instructions / Examples`	Examples of application. e.g. • Specifying memory partitions • Processing a script • .....
Reference	Cross-reference to another section, figure or table.

1.2 Acronyms and Definitions

The following terminology and abbreviations are used:

Acronym	Full Form
BST	Boundary Scan Test
CAN	Controller Area Network
CIB	Configuration Info Block
COP	Common On-chip Processor
CPU	Central Processing Unit
CPCI	Compact Peripheral Component Interface
DDR	Double Data Rate
EEPROM	Electrically Erasable Programmable Read-Only Memory (Byte-wise re-writable)
ESD	Electrostatic Discharge
EMV	Electro Magnetic Compatibility
FKT	Functions Test
HIP	Hardware Interoperability Platform
ICT	In-Circuit Test
JTAG	Joint Test Action Group
MCU	Memory Control Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCI	Peripheral Component Interconnect
PLD	Programmable Logic Device
POST	Power-On Self Test
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SMD	Surface Mounted Device
SCC	Serial Communication Control
TSEC	Triple Speed Ethernet Controller
UART	Universal Asynchronous Receiver/Transmitter

Acronym	Full Form
USB	Universal Serial Bus

1.3 Tips on Safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.4 Handling / ESD Tips

General handling of your TQ products

The handling and use of your TQ product may be done exclusively by qualified personnel.

Ensure that while using your TQ product, particularly while plugging in/out of modules, changing jumper settings, or connecting other external devices, the power supply is not connected to your TQ product. Violation of this guideline can result in damage/destruction of the module and cause danger to your health.

Improper handling of your TQ product would render the guarantee invalid.

Proper ESD handling

The ESD components must be used in workplaces, which are suitable for their handling in order to avoid damage or destruction.

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1.9 Revision History:

Rev.	Date	Name	Pos.	Modification
103	25.10.05	JTR		Compilation from STK85xx.KO.006
	03.11.05	JTR		Completion
	09.11.05	JTR		Accept the results of the internal testing
104	14.11.05	JTR	4.1.1	PS/2-support for TQM8555/41
			4.1.2, 4.1.3	Headings TQM8347L and TQM8541 added
			4.2.1.1, 4.2.1.2	Disambiguation Configuration matrix
			4.2.5.1	Implementation Status / Control-Register added
105	21.11.05	ROE	4.1.1	Correction: Number of FEC's with TQM8540
106	27.06.06	ROE	4.4.7.3	Added: Supply from a regulated power supply 24V DC

2 General

The Starter kit STK85xx Rev.105 is a universal development board for PowerQUICC-III- and PowerQUICC-II-Pro-based Mini Module like TQM8560, TQM8349L and its derivatives.

It directly provides all important functions and interfaces of the Mini Module to the user. In addition, extra functions e.g. RTC buffering and PC-Card-Controller are implemented.

There are several installation possibilities:

- Development Board in the Software-Development
- Development Board in the Hardware-Development for implementation and for testing the application specific additional functions.
- Demonstration-Board for presentations and trade fairs.
- Standard product for directly installation at the client side.
- Internal installation during product qualification and during testing a small batch of the existing and future Mini Modules.

3 System Architecture

3.1 Block Circuit Diagram

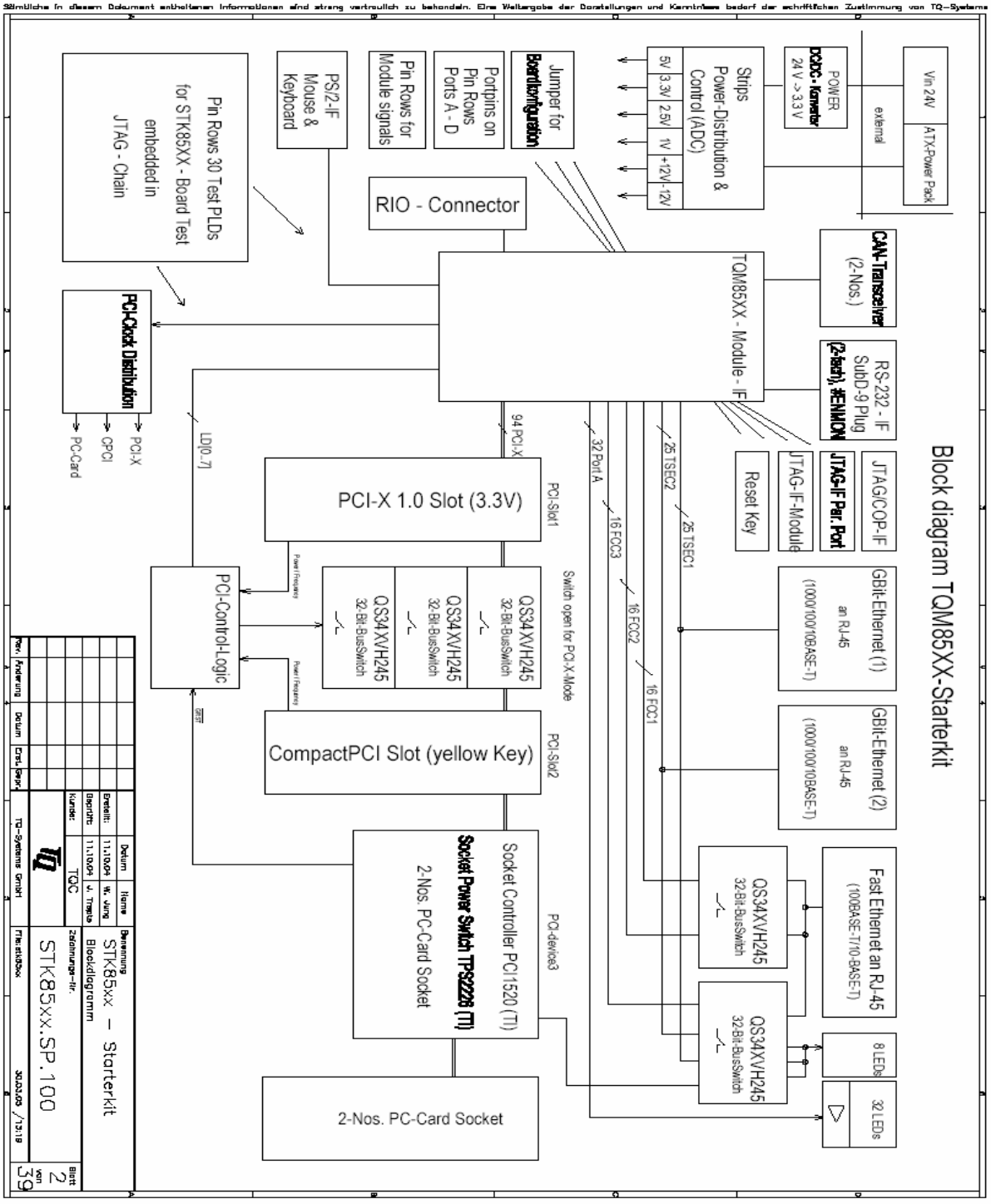

Illustration 1: Block circuit diagram

3.2 Brief Description

- 2 * GBit Ethernet
- 1 * Fast Ethernet
- 1 * Parallel Rapid I/O
- 2 * RS232 Interface (RXD, TXD)
- 1 * PCI-X
- 1 * Compact PCI
- 2 * PC-Card-Interface
- 2 * CAN
- 2 * PS/2-Interface (Keyboard + Mouse)
- Module-Connector for TQM85xx or TQM83xx
- JTAG-/Debug-Interface
- Reset-Button
- Circuit/ Jumper for Monitor-Enable-Signal
- General-Purpose-LEDs
- Buffer battery for RTC on the TQ-Module
- Power supply from the DC-power supply, ATX-power supply or regulated 24V power supply.

4 Electronic-Specification

4.1 Module

4.1.1 Functions depending on the installed Module type

There are limitations to the usage of the functions available on the module or provided by the STK85xx.

Function	TQM8560	TQM8540	TQM8555	TQM8541	TQM8349L	TQM8347L
GBit Ethernet TSEC1	+	+	+	+	+	+
GBit Ethernet TSEC2	+	+	+ (a)	+ (a)	+ (a)	+ (a)
Fast Ethernet on FCC1	+	+	+	+	– 1	– 1
Fast Ethernet on FCC2	+	– 1	+	+	– 1	– 1
Fast Ethernet on FCC3 / FEC	+	– 1	– 1	– 1	– 1	– 1
Parallel Rapid I/O	+	+	– 1	– 1	– 1	– 1
RS232 #1	+	+	(b)	(b)	+	+
RS232 #2	+	+	+	+	+	+
PCI1 as PCI-X	+	+	– 1	– 1	– 1	– 1
PCI1 64 Bit	+	+	+	+	+	+
PCI1 32 Bit	+	+	+	+	+	+
PCI2	– 1, 2	– 1, 2	– 2	– 2	– 2	– 2
Compact PCI	+	+	+	+	+	+
PC-Card	+	+	+	+	+	+
USB High Speed	– 1, 2	– 1, 2	– 1, 2	– 1, 2	– 2	– 2
USB Full Speed	– 1, 2	– 1, 2	– 2	– 2	– 2	– 2
CAN	+	+	+	+	– 1	– 1
PS/2	+	+	+	+	+	+
JTAG / Debug	+	+	+	+	+	+
Reset	+	+	+	+	+	+
General Purpose LEDs on Port A	+	+	(c)	(c)	– 1	– 1
General Purpose LEDs on TSEC1	– 1	– 1	– 1	– 1	+	+
General Purpose LEDs on TSEC2	+	+	+	+	+	+
General Purpose LEDs on PCI	+	+	+	+	+	+
Backup Battery	+	+	+	+	+	+
Supply from AC Adapter	+	+	+	+	+	+
Supply from ATX Power Supply	+	+	+	+	+	+

+ supported
– 1 not supported by CPU / module
– 2 not supported by STK85xx
(a) common I/O voltage with TSEC1
(b) only via RS232-transceiver on module
(c) only 24 bits present

Further deviating signals can be guided in the area of Test- / Extension strips (refer 4.3), by differential assignment of the Module Connector. An overview of the differential assignment is shown in Illustration 2.

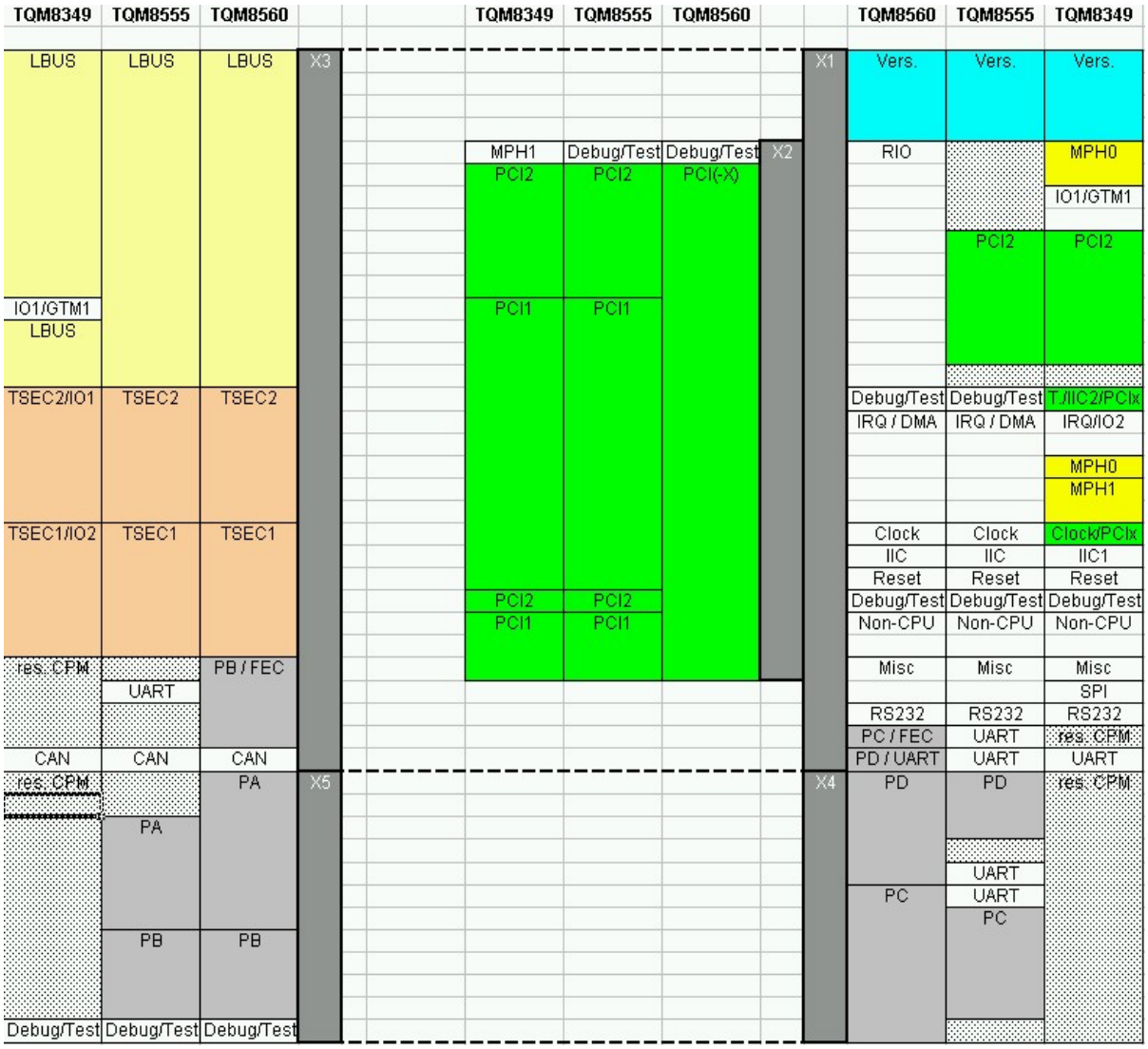

Illustration 2: Overview Module Pin outs

4.1.2 Precautions for operation with TQM8349L/47L

STK85xx in Rev. 100 was not developed for operation with a TQM8349L/47L. But operation with it is possible due to the Pin-compatibility of the Module.

- Functional limitations refer 4.1.1
- Additional circuits and configuration possibilities: refer below
- References to PCI-Bus-Clocking refer 4.2.5

LVDD2	Separate TSEC2 I/O voltage
X38.6 – X87.3	2.5 V **Caution:** No power sequencing guaranteed
X38.6 – X1.138	2.5 V via "green wire", power sequencing ok
X38.6 – X23.1	3.3 V **Caution:** No power sequencing guaranteed
X38.6 – X1.134	3.3 V via "green wire", power sequencing ok

Note: As LVDD2 will be supplied by the PHY via the CPU's I/O protection diodes, leaving LVDD2 open will also work under laboratory conditions.

Configuration Signals:

Module Signal	CPU Signal at Reset	Configuration
SEL_CLKIN_DIV = STK85xx TRIG_IN = X14 Pin 7	**CFG_CLKIN_ DIV**	
0	0	CLKIN : PCI_SYNC_OUT = 1 : 1
1	1	CLKIN : PCI_SYNC_OUT = 2 : 1

Module Signal	CPU Signal at Reset	Configuration
SEL_RESET_SOURCE = STK85xx TRIG_OUT = X14 Pin 8	CFG_RESET_ SOURCE [0:2]	
0	0b000	Local Bus
1	0b010	I2C-EEPROM, High Speed
Z *	0b001	I2C-EEPROM, Low Speed (not recommended, use 0b010 instead)

* Z = open (not connected)

4.1.3 Precautions for operation with TQM8555/41

STK85xx in Rev. 100 was not developed for operation with a TQM8555/41. But operation with it is possible due to the Pin-compatibility of the Module.

- Functional limitations refer 4.1.1
- NO special precautions are required

4.1.4 Local Bus

- Connected components: PCI-Bus-Control-PLD (D21), A/D-Converter, Control-PLD (D39)
- Further PLD as Bus drive (D37)

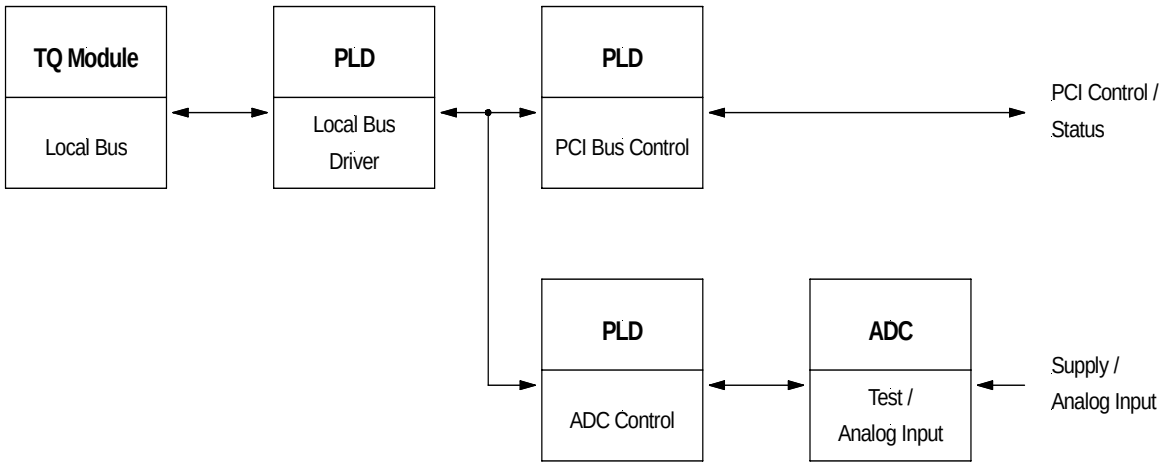

Illustration 3: Structure Local Bus

4.2 External interfaces

External interfaces are interfaces that are meant for specification driven operations for example; they can be used for installation in a casing. It has an ESD fuse and if required an EMV circuit.

4.2.1 GBit Ethernet

4.2.1.1 TSEC1

- Available on the socket X17, on the right side from the connector,
  For individual Signal assignment, refer to the GBit Ethernet (1) schematic
- Controller TSEC1 in CPU on the TQ Module
- PHY Marvell 88E1111 (D13), PHY Address 2
- Transducer integrated in the RJ 45 socket HALO HFJ12-1G01E (X17)
- Interrupt by IRQ8# is possible
- Reset configuration for PHY can be derived from the configuration matrix (Assembly options)

Usable Interface-Mode:

MII Mode	MDI Mode	Properties
GMII	1000Base-T	125 MHz data rate, 8 bit data width
MII	100/10Base-T	25 MHz max. data rate, 4 bit data width

Configuration matrix:

Configuration Bits	Value	Meaning
PHYADDR[4:0]	0b00010	PHY address 2
ENA_PAUSE	0	Disable Pause
ANEG[3:0]	0b1001	Auto Neg., advertise only 1000Base-T full duplex, forced slave
ENA_XC	0	MDI Crossover disabled
DIS_125	0	125 MHz clock enabled
HWCFG_MODE[3:0]	0b1111	GMII to copper
DIS_FC	1	Disable fiber / copper auto-selection
DIS_SLEEP	1	Disable energy detect

Configuration Bits	Value	Meaning
SEL_TWSI	0	Select MDC/MDIO interface
INT_POL	1	INTn signal is active low
75/50_OHM	0	50 Ω termination for fiber (don't care)

LEDs:

Reference	Signal	Description
V63	LED_LINK10	Low = 10 Link Up High = 10 Link Down
V65	LED_LINK100	Low = 100 Link Up High = 100 Link Down
V66	LED_LINK1000	Low = 1000 Link Up High = 1000 Link Down
V67	LED_DUPLEX	Low = Full Duplex High = Half Duplex Blink = Collision
V68	LED_RX	Low = Link Up High = Link Down Blink = Receiving
V69	LED_TX	Low = Transmitting High = Not Transmitting

Note: LED drivers are configurable and may be used for other purposes

Jumper:

X4	TSEC1 Interrupt
open	PHY interrupt disabled
1 – 2	PHY interrupt connected to IRQ8#

4.2.1.2 TSEC2

- Available on the socket X17, on the right side from the connector,
  For individual Signal assignment, refer to the GBit Ethernet (2) schematic.
- Controller TSEC2 in CPU on the TQ-Module
- PHY Marvell 88E1111 (D28), PHY-Address 1
- Transducer integrated in RJ-45-Socket HALO HFJ12-1G01E (X17)
- Interrupt by IRQ8# is possible
- Reset-configuration for PHY can be derived from the configuration matrix (Assembly options)

Usable Interface-Mode:

MII Mode	MDI Mode	Properties
GMII	1000Base-T	125 MHz data rate, 8 bit data width
MII	100/10Base-T	25 MHz max. data rate, 4 bit data width

Configuration matrix:

Configuration bits	Value	Meaning
PHYADDR[4:0]	0b00001	PHY address 1
ENA_PAUSE	0	Disable Pause
ANEG[3:0]	0b1001	Auto Neg., advertise only

Configuration bits	Value	Meaning
		1000Base-T full duplex, forced slave
ENA_XC	0	MDI Crossover disabled
DIS_125	0	125 MHz clock enabled
HWCFG_MODE[3:0]	0b1111	GMII to copper
DIS_FC	1	Disable fiber / copper auto-selection
DIS_SLEEP	1	Disable energy detect
SEL_TWSI	0	Select MDC/MDIO interface
INT_POL	1	INTn signal is active low
75/50_OHM	0	50 Ω termination for fiber (don't care)

LEDs:

Reference	Signal	Description
V34	LED_LINK10	Low = 10 Link Up High = 10 Link Down
V41	LED_LINK100	Low = 100 Link Up High = 100 Link Down
V49	LED_LINK1000	Low = 1000 Link Up High = 1000 Link Down
V75	LED_DUPLEX	Low = Full Duplex High = Half Duplex Blink = Collision
V79	LED_RX	Low = Link Up High = Link Down Blink = Receiving
V80	LED_TX	Low = Transmitting High = Not Transmitting

Note: LED drivers are configurable and may be used for other purposes

Jumper:

X1	TSEC2 Interrupt
Open	PHY interrupt disabled
1 – 2	PHY interrupt connected to IRQ8#

4.2.2 Fast Ethernet

- Available on the socket X43, for individual Signal assignment refer to the Fast-Ethernet schematic.
- Controller FCC1/2/3 (TQM8560), FEC (TQM8540) or FCC1/2 (TQM8555/41) in CPU on the TQ-Module.
- PHY Intel LXT971A, PHY-Address 3
- Isolation module HALO TG110-5050N2
- Interrupt via IRQ8# is possible.

Configuration:

Configuration signal	Value	Meaning
SD/TP#	0	Twisted pair
TXSLEW[1:0]	0b00	TX slew rate 3.0 ns

Configuration signal	Value	Meaning
ADDR[4:0]	0b0001 1	PHY address 3
PAUSE	1	Advertise pause capabilities
SLEEP	0	Disable sleep mode
PWRDWN	0	Disable power-down mode
LED/CFG[1:3]	0b111	Auto-negotiation, 10/100 MBit, full / half duplex

Jumper:

X53	Fast Ethernet Interrupt
open	PHY interrupt disabled
1 – 2	PHY interrupt connected to IRQ8#

X2	Fast Ethernet Management data interface
open	Management data interface disabled
1 – 2	Management data interface enabled

X47 / X50	Fast Ethernet MII multiplexing
open	FCC1, FCC2, FCC3/FEC disabled
a – b (X47.2- X50.2)	FCC1 selected (TQM8560 only)
a – c (X50.2 – 1)	FCC2 selected (TQM8560 only)
a – d (X50.2 – 3)	FCC3 (TQM8560) / FEC (TQM8540) selected *

* Note: Setting a – d gives a contention with UART0 on TQM8555/41

4.2.3 Parallel Rapid I/O

- HIP-Slot (Rapid I/O combined with PCI)
  Rapid I/O Data on X3, Rapid I/O supply on X60 / X78, PCI-X on X103.
  For individual Signal assignment refer to the RIO (Rapid I/O) schematic.
- Controller RIO in CPU on TQ-Module
- External clock up to 500 MHz is possible
- Jumper STK85xx-RIO enables direct connection of two STK85xx via X3

Reference: Use of Parallel Rapid I/O is not recommended by Freescale. Please contact your sales representative in case you intend to use Parallel Rapid I/O

Transmit-Clock-Mode:

Cfg_rio_clk [0:1]*	Properties
01	Rapid I/O receive clock is the source of the transmit clock
10	Rapid I/O transmit clock inputs (RIO_TX_CLK_IN and RIO_TX_CLK_IN#) are the source of the transmit clock
11	CCB clock is the source of the transmit clock (default)

* Determined by TQM8560/40 reset configuration

Configuration / Jumpers:

X63	External Rapid I/O Clock	
	Config Signal	Description
1 – 2	M8	External clock multiplied by M
3 – 4	M7	
5 – 6	M6	
7 – 8	M5	
9 – 10	M4	
11 – 12	M3	
13 – 14	M2	
15 – 16	M1	
17 – 18	M0	
19 – 20	N1	External clock divided by 2^N
21 – 22	N0	
open	OE	External clock disabled
23 – 24		External clock enabled

4.2.4 RS232

Reference: UART1 of TQM8349L/47L corresponds to the UART0 of TQM8560/40 and TQM8555/41.

Jumper (both interfaces):

X12	Shutdown RS232-Transceiver (SHDN#)
open	Transceiver shutdown
1 – 2	Transceiver active

X104	Shutdown RS232-Enable (EN#)
open	Transceiver disabled
1 – 2	Transceiver enabled

4.2.4.1 SCC1 / UART0

- Available on the upper socket X18, for Individual signal assignment as well as suggested Null modem cable, refer to the RS232 & Reset-Taster schematic.
- Controller SCC1 (TQM8560) or DUART (TQM8540, TQM8555/41) in CPU on the TQ-Module.
- Transceiver on TQ-Module or optionally MAX3222 on STK85xx (for Module without Transceiver)
- Signals RXD, TXD provided with Transceiver.
- RTS and DTR as static Signals for the Monitor-Functions (Reset, Enable Monitor-Software)

Pinouts:

Pin	Signal TQM8560	Signal TQM8540	Type	Description
6	ENMON#	ENMON#	I	Temporary input for MON85xx / MON83xx software, RS232-level tolerant 0 = Interactive Mode (responds to RS232 commands) 1 = Initial Mode (initialize CPU and start application)
3	TXD1	UART_SOUT0*	O	Transmit data (RS232 level)
5	GND	GND	-	Ground
1	RESIN#	RESIN#	I	Reset input, connected to Reset input of supervisor circuit, RS232-level tolerant 0 = Reset 1 = No reset

Pin	Signal TQM8560	Signal TQM8540	Type	Description
6	ENMON#	ENMON#	I	Temporary input for MON85xx / MON83xx software, RS232-level tolerant 0 = Interactive Mode (responds to RS232 commands) 1 = Initial Mode (initialize CPU and start application)
2	RXD1	UART_SIN0**	I	Receive data (RS232 level)

* UART_SOUT1 with TQM8349L/47L
** UART_SIN1 with TQM8349L/47L

4.2.4.2 SCC2 / UART1

- Available on the socket X18 below, for individual Signal assignment refer to the RS232 & Reset-Taster schematic.
- Controller SCC2 (TQM8560) or DUART (TQM8540, TQM8555/41) in CPU on the TQ-Module.
- Transceiver on TQ-Module or optionally MAX3222 on STK85xx (for Module without the Transceiver)
- Signal RXD, TXD provided with the Transceiver.

Jumper:

X61	RXD2# / UART_SIN1# Usage
open	Not connected on STK85xx (transceiver on module may still be active)
1 – 2*	Connected to X18 via transceiver on STK85xx
2 – 3*	Connected to PS/2 controller.

* Note: With board Rev. 1xx, label "X61.2" written in copper of top layer is wrong, should be "X61.1". However, pin 1 marking (square pad, bottom layer) is correct.

4.2.5 PCI / PCI-X

- Controller PCI in CPU on TQM8560/40, PCI1 on TQM8349L/47L and TQM8555/41
- 3.3-V-Signal, 5-V-intolerant
- Clocking in Rev. 1xx designed for TQM85xx, PCI_CLK_OUT0 and PCI_CLK_OUT[2:7] not used, refer Illustration 4 and Illustration 5.

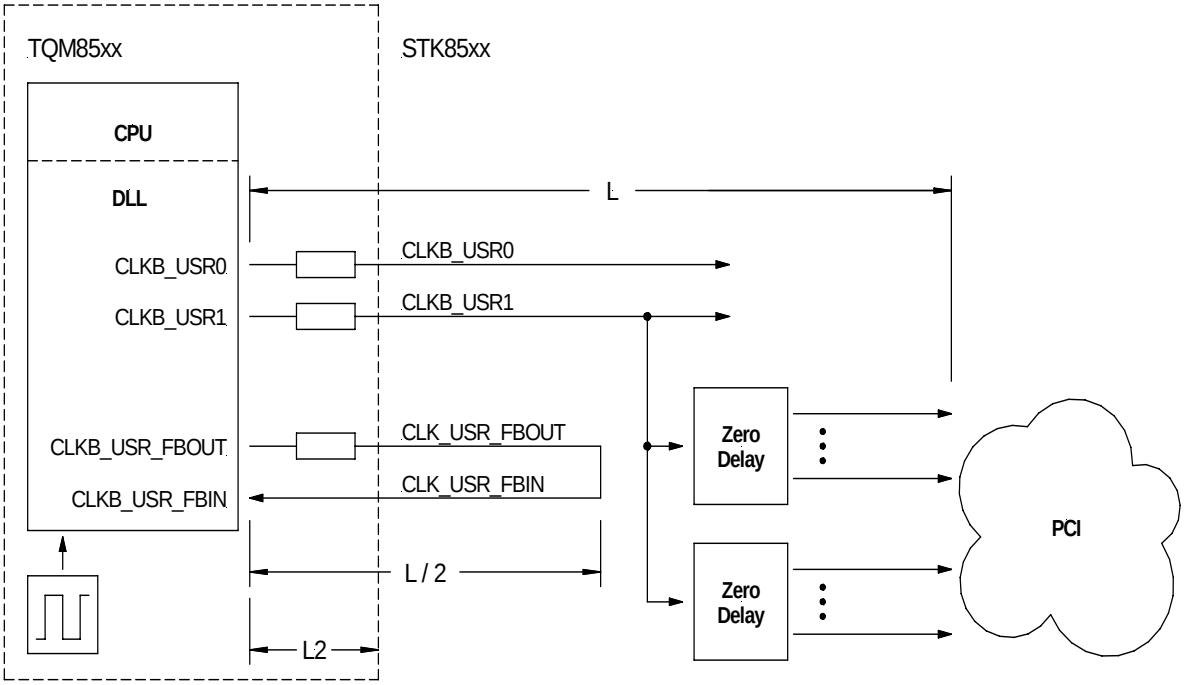

Illustration 4: Structure PCI-Clocks with TQM85xx

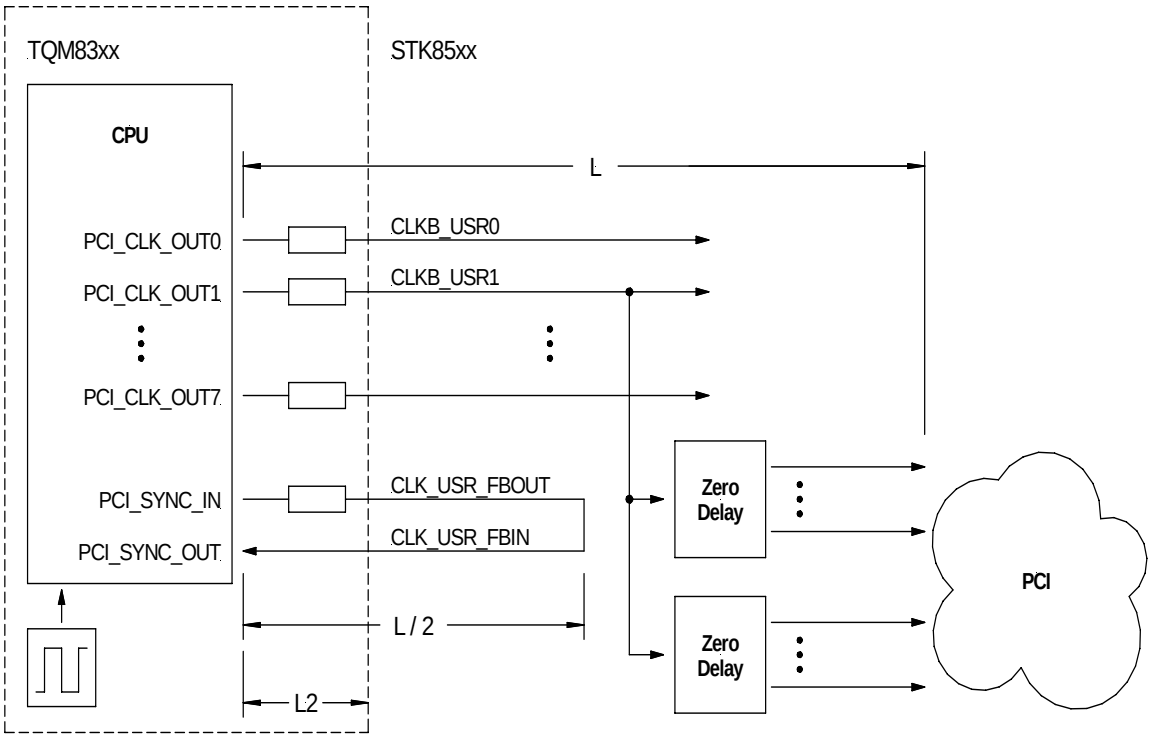

Illustration 5: Structure PCI-Clocks with TQM83xx

Connections of REQ/GNT-Signals:

REQ / GNT	Function
0	-
1	PCI/PCI-X Slot
2	Compact PCI Slot

REQ / GNT	Function
3	PC-Card-Controller
4	-

PCI connections (compatible with Freescale ADS except for IRQ6 instead of IRQ4)

Device / Slot		Interrupt connections				Function
IDSEL	Device #	Pin INTA	Pin INTB	Pin INTC	Pin INTD	
AD19	8					
AD20	9					
AD21	10					
AD22	11					
AD23	12					
AD24	13					
AD25	14					
AD26	15					
AD27	16					CPU (Agent Mode)
AD28	17	IRQ2	IRQ3	IRQ6	IRQ5	PCI/PCI-X Slot
AD29	18	IRQ3	IRQ6	IRQ5	IRQ2	Compact PCI Slot
AD30	19	IRQ6	IRQ5	-	-	PC-Card-Controller
AD31	20					

Jumper:

X52	M66EN
Open	M66EN determined by cards in PCI-X and Compact PCI slot
1 – 2	M66EN forced low manually (force 33 MHz Mode)

4.2.5.1 PCI Bus Control

- Status- / Control-Register realized in PLD D21
- Control via Local Bus.
- Provides PCI-Status signals (Card-Detect- and Capability-Signals)
- Controls the FET-Switch for the PCI-X-Mode.
- Sets the PC-Card-Controller to the Reset mode, as soon as at least a 66-MHz-card is inserted (refer also Jumper X109 under 4.2.5.4)

Status / Control Register

Bit	Type	Description
0:1	R	PCI-X Capability 0b00 = PCIXCAP open, PCI-X 133 MHz 0b01 = reserved 0b10 = PCIXCAP pull-down, PCI-X 66 MHz 0b11 = PCIXCAP connected to ground, not PCI-X capable
2:3	R	Compact PCI Capability 0b00 = reserved 0b01 = reserved 0b10 = CPCICAP pull-down, PCI-X 66 MHz

Bit	Type	Description
		0b11 = CPCICAP connected to ground, not PCI-X capable
4	R	PCI-X Present 1 0 = PRSNT1# connected to ground, card present 1 = PRSNT1# open, no card present
5	R	PCI-X Present 2 0 = PRSNT2# connected to ground, card present 1 = PRSNT2# open, no card present
6	R	Compact PCI Present 0 = CPCI_PRESENT# connected to ground, card present 1 = CPCI_PRESENT# open, no card present
7	R	1
8	R	1
9	R	1
10	R	0
11	R	0
12	R	PCI 66 MHz Enable 0 = at least one detected card not 66 MHz capable or no card detected (on-board PC-Card controller is not 66 MHz capable) 1 = all detected cards 66 MHz capable
13	R/W	PCI-X Enable 0 = Compact PCI Slot and PC-Card-Controller disconnected, PCI-X possible (reset state, entered on HRESET#) 1 = Compact PCI Slot and PC-Card-Controller connected to PCI
14	R	0
15	R	0

Jumper:

X49	PCI-X Enable
Open	Compact PCI Slot and PC-Card-Controller connected to PCI
1 – 2	Compact PCI Slot and PC-Card-Controller disconnected, PCI-X possible

4.2.5.2 PCI-X-Slot

- HIP-Slot (Rapid I/O combined with PCI) Rapid I/O data on X3, Rapid I/O supply on X60 / X78, PCI-X on X103 for individual Signal assignment refer to the PCI-X 1.0 Slot 3.3V Slot1 schematic.
- Clock frequency max. 133 MHz (only this slot); all other PCI-Devices can be detached by the FET-switch (controlled by the PCI-Bus-Control-PLD or Jumper)
- 3.3-V-Signal, 5-V-intolerant.

4.2.5.3 Compact-PCI-Slot

- 64-Bit Compact PCI, available on socket X46. For individual Signal assignment refer to the Compact PCI Slot 2 schematic.
- Clock frequency max. 66 MHz
- 3.3-V-Signal, 5-V-intolerant.

4.2.5.4 PC-Card-Interface

- Two PC-Card-Slots.
- Available on X44. For individual Signal assignment refer to the PC – Card Slot A & B schematic.
- Controller PCI1520 on STK85xx
- Connection via a 32-Bit PCI 33 MHz

Reference: As the Controller can work only till a max. of 33 MHz clock frequency, it is set to Reset Mode, as soon as a card of at least 66-MHz is inserted.

LED:

Reference	Signal	Description
V61	MFUNC4 (active high)	PC-Card Socket Activity configurable, may be used for other purposes

Jumper:

X109	PC-Card Controller Reset
Open	PC-Card Controller Reset controlled by PCI-Bus Control PLD
1 – 2	PC-Card Controller Reset forced manually

4.2.6 CAN

- Two Full CAN 2.0b compatible interfaces.
- Available on the socket X25, for individual Signal assignment refer to the JTAG / COP & CAN schematic.
- Controller 2 * AS82527 on TQ-Module.
- Transceiver TJA1050 Philips.

Reference: Current drain via X25 is the user's responsibility; no measures are provided against short circuit or overload. The maximum permissible power is 100 mA.

Jumper:

X26	Ground on Interface
Open	X25 Pin 6 open
1 – 2	X25 Pin 6 connected to DGND

X27	5 V on Interface
Open	X25 Pin 9 open
1 – 2	X25 Pin 9 connected to VCC5V

X28	Termination CAN1
Open	No termination
1 – 2	Termination 120 Ω

X29	Termination CAN2
Open	No termination
1 – 2	Termination 120 Ω

4.2.7 PS/2-Interfaces

- Two PS/2-Interfaces (Keyboard and mouse)
- Available on the socket X32, above / green mouse, below / blue keyboard.
  For individual Signal assignment refer to the Keyboard / Mouse schematic.
- Controller PIC16F627 on STK85xx, Connected to the TQM-Module via RS232
- Refer the special document PS2RS232.SZ.008 for description of the interface converter.

Jumper:

X66	RS232 interface selector
open	No interface selected
1 – 2, 9 – 10	SCC2 (TQM8560) UART1 (TQM8540, TQM8555/41) UART2 (TQM8349L)
3 – 4, 11 – 12	SCC3 primary (TQM8560) UART0 (TQM8555/41)
5 – 6, 13 – 14	SCC3 secondary (TQM8560, TQM8555)
7 – 8, 15 – 16	SCC4 (TQM8560, TQM8555)

4.3 Test- / Extension strips

All relevant signals of the module connector are guided to the strip in a 2.54mm grid. The assignment of this strip is to be derived from the Supply Voltage Strips (Power Distribution) schematic.

X13 Port A
X8 Port B
X20 Port C
X22 Port D
X51 I2C Modules
X72 I2C PC Card Controller Configurations EEPROM (Option)
X14 MSRCID / Trigger / MDVAL
X21 Test / MDC / Reserved
X23 MECC
X70 DMA
X68 Local Bus Addresses / Data
X69 Local Bus Control signal
X35 TSEC1
X5 TSEC2
X39 Clocks
X38 Resets
X33 Interrupts

4.4 Internal Interfaces

Internal interfaces are interfaces that are not available to the outside when operated according to regulations. They are used exclusively for lab operations, so that one can assume the appropriate ESD precautions of the external test structure. Thus, ESD-fuse and EMV-circuit are not required.

4.4.1 JTAG- / Debug-Interface

- Available on the socket X11
- Signal assignment compatible to [1], For Details refer to the JTAG via PPORT schematic.

4.4.2 JTAG- / Debug-Interface via Parallel-Port

- Simple JTAG- / Debug-Interface for connection to the PC Parallel-Port, compatible to MPCBDM by VAS GmbH, refer http://www.vas-gmbh.de/software/mpcbdm/
- BDM-Interface is guided on a 16-pole strip, PC-Interface is provided as SubD-25 strip. (Pin-Assignment for 25-pole 1:1-cable with connector socket)
- Connection to the PC with a flat cable, 26-pole pole connector and 25-pole Sub-D-connector in Crimp-technology, as shown in the JTAG via PPORT schematic.

Jumper:

X37	JTAG / Debug Parallel TCK
Open	TCK not connected
1 – 2	TCK from parallel port connected to CPU

X59	JTAG / Debug Parallel TDI
Open	TDI not connected
1 – 2	TDI from parallel port connected to CPU

X7	JTAG / Debug Parallel TMS
Open	TMS not connected
1 – 2	TMS from parallel port connected to CPU

4.4.3 Reset

- Reset-Key S1 effects the Signal RESIN#
- Additional connection possibilities for external Reset-Key, Reset- and Power-LED to X75 for Signal assignment refer power supply diagram
- Self-Reset with TQM85xx (all Revisions) are possible, configurable

Jumper:

X6	TQM8560.1xx/2xx Self-Reset Compatibility
Open	TQM8560/40 Rev. 1xx and 2xx: No Self-Reset possible TQM8560/40 newer revisions, TQM8555/41: Self-Reset circuitry is on the module, always use this setting
1 – 2	TQM8560/40 Rev. 1xx and 2xx: Self-Reset possible (compatible to newer versions and TQM8555/41) TQM8560/40 newer revisions, TQM8555/41: Don't use this setting

X57	Permanent Reset
Open	Normal operation
1 – 2	RESIN# tied low

X58	Self-Reset Disable
Open	Normal operation, Self-Reset possible depending on module type and X6 setting
1 – 2	Pull-up 2k2 on RESIN#, no self-reset possible

4.4.4 General-Purpose-LEDs

- 32 LEDs to Port A
- 8 LEDs optionally to PCI_AD[47:40], TSEC2_TX[0:7] or TSEC1_TXD[0:7]

LED's:

Reference	Signal	Description
V4	PA0	Port Signal (active high)
V5	PA1	Port Signal (active high)
V6	PA2	Port Signal (active high)
V7	PA3	Port Signal (active high)
V9	PA4	Port Signal (active high)
V10	PA5	Port Signal (active high)
V11	PA6	Port Signal (active high)
V17	PA7	Port Signal (active high)
V25	PA8	Port Signal (active high)
V24	PA9	Port Signal (active high)
V23	PA10	Port Signal (active high)
V22	PA11	Port Signal (active high)
V21	PA12	Port Signal (active high)
V20	PA13	Port Signal (active high)
V19	PA14	Port Signal (active high)
V18	PA15	Port Signal (active high)
V128	PA16	Port Signal (active high)
V127	PA17	Port Signal (active high)
V126	PA18	Port Signal (active high)
V125	PA19	Port Signal (active high)
V124	PA20	Port Signal (active high)
V123	PA21	Port Signal (active high)
V122	PA22	Port Signal (active high)
V121	PA23	Port Signal (active high)
V136	PA24	Port Signal (active high)
V135	PA25	Port Signal (active high)
V134	PA26	Port Signal (active high)
V133	PA27	Port Signal (active high)
V132	PA28	Port Signal (active high)
V131	PA29	Port Signal (active high)
V130	PA30	Port Signal (active high)
V129	PA31	Port Signal (active high)

Reference	Signal	Description
V26	PCI_AD47 / TSEC2_TXD0	General Purpose Output as configured by X30 / X67 (active high)
V27	PCI_AD46 / TSEC2_TXD1	General Purpose Output as configured by X30 / X67 (active high)
V28	PCI_AD45 / TSEC2_TXD2	General Purpose Output as configured by X30 / X67 (active high)
V29	PCI_AD44 / TSEC2_TXD3	General Purpose Output as configured by X30 / X67 (active high)
V30	PCI_AD43 / TSEC2_TXD4 / TSEC1_TXD4	General Purpose Output as configured by X30 / X67 (active high)
V31	PCI_AD42 / TSEC2_TXD5 /	General Purpose Output as configured by X30 / X67 (active high)

Reference	Signal	Description
	TSEC1_TXD5	
V32	PCI_AD41 / TSEC2_TXD6 / TSEC1_TXD6	General Purpose Output as configured by X30 / X67 (active high)
V33	PCI_AD40 / TSEC2_TXD7 / TSEC1_TXD7	General Purpose Output as configured by X30 / X67 (active high)

Jumper:

X30	General Purpose LEDs PCI / TSEC
open	LEDs driven by TSEC1 / TSEC2
1 – 2	LEDs driven by PCI_AD

X67	General Purpose LEDs TSEC1 / 2
open	LEDs driven by TSEC2
1 – 2	LEDs driven by TSEC1 (TQM8349L only)

4.4.5 Fan Connection

- Available on the socket X80, for individual Signal assignment refer to the Fan schematic.
- 5 V (12 V possible as an assembly option)
- Input speed can be applied to the Interrupt IRQ7

Jumper:

X79	Fan Speed Signal
Open	Fan Speed Interrupt disabled
1 – 2	Fan Speed Interrupt connected to IRQ7#

4.4.6 Buffer battery for RTC

- Connected to the VBAT of the Module
- Lithium battery Type CR2032, 3 V, 235 mAh (G4)
- Socketed, convertible
- Alternative connection possibilities for Buffer voltage to X86. For pin assignment refer 4.4.7
- Protection against excess current by series resistance.
- Reverse current lock by a Diode in the Series with R939 (subsequently added)

4.4.7 Power Supply

- All important power supply is available through the screw clamp or strips.
- Feeding in and removing only for testing and is the responsibility of the user.
- The power supply can be differentiated between the supply and user (for testing e.g. current metering, user responsibility, refer Illustration 6).

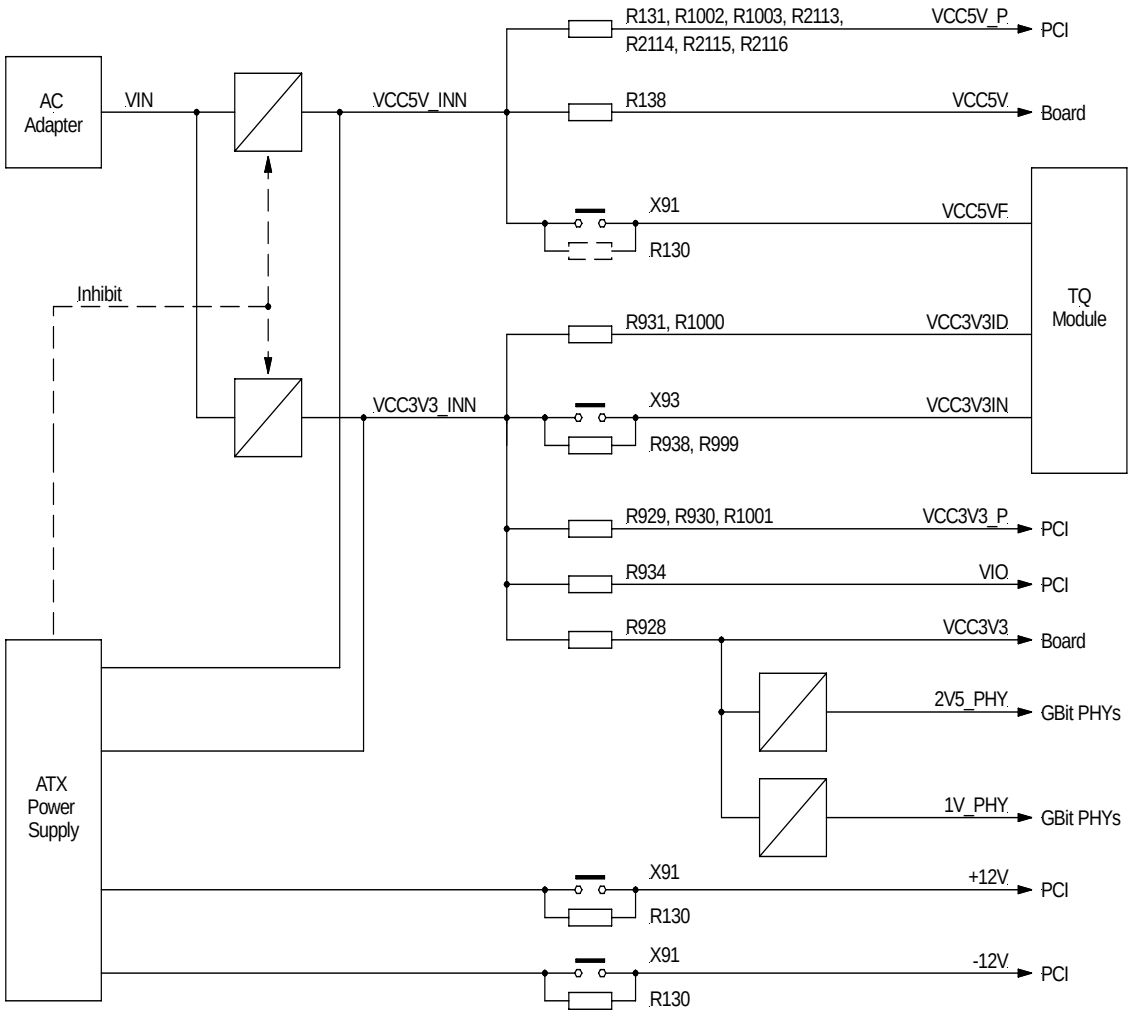

Illustration 6: Supply structure

Voltage and connection possibilities:

Voltage	Reference / Pin	Description
VIN	X82.1	Input voltage from AC adapter
+12V	X83.1	+12 V from ATX power supply
-12V	X83.3	-12 V from ATX power supply
VCC5_INN	X85.1, X85.2	5 V supply from internal 5 V power supply or ATX power supply
VCC5VF	X92.1	5 V supply to or from TQ module
VCC5V	X21.2, X8.3	5 V supply to STK85xx board
VCC5V_P	X78.1b – 4b, X78.1c – 4c	5 V supply to PCI
VCC3V3_INN	X81.1, X81.2	3.3 V supply from internal 3.3 V power supply or ATX power supply
VCC3V3IN		3.3 V supply to TQ module (used by voltage regulators)
VCC3V3ID		3.3 V supply to TQ module (used directly)
VCC3V3	X35.6, X45.1	3.3 V supply to STK85xx board

Voltage	Reference / Pin	Description
VCC3V3_P	X60.1a – 4a, X60.1b – 4b	3.3 V supply to PCI
VIO	X46.c10	3.3 V supply to PCI I/O voltage
2V5_PHY	X87.3	2.5 V supply for GBit PHYs
1V_PHY	X87.1	1 V supply for GBit PHYs
VBAT	X86.1	
DGND	X81.3, X82.2, X83.2, X85.3, X86.2, X87.2, X92.2	Digital Ground

4.4.7.1 Supply from the DC power supply

- Power Supply Cincon Electronics TR70A18-01A03, 18 V 3.9 A
- Connection to the low voltage socket X24, internal conductor is positive.
- Generating 3.3 and 5 V on STK85xx through the regulator; is automatically deactivated while connecting it to an ATX-power supply adaptor.
- Available power is sufficient for the module (TQM8560/40, TQM8349L/47L), STK85xx and PC-Cards, however without PCI- / Compact-PCI-Plug-in Card.

Jumper:

X41	3.3 V Enable
open	Internal 3.3 V supply disabled
1 – 2	Internal 3.3 V supply enabled

X62	5 V Enable
open	Internal 5 V supply disabled
1 – 2	Internal 5 V supply enabled

4.4.7.2 Supply from the ATX-power supply

Reference: To ensure a sufficiently good compensation during load variation, an additional input capacity of 6 * 4700 µF a VCC3V3_INN must be provided.

- ATX-power supply Bicker BEA-530 or similar 300 W, with Remote Sensing for 3.3 V
- Connection to the X65
- Available power is sufficient for the Module (TQM8560/40, TQM8349L/47L), STK85xx, PC-Cards and PCI- / Compact-PCI-Plug IN cards
- Basic load 1 A at 5 V is automatically connected during operation with ATX-power supply (R117, R125). WARNING: Basic Load will be hot!!!!

4.4.7.3 Supply from a regulated power supply 24V DC

- +24VDC +-20% on X82.1, DGND on X82.2
- This is the recommended power supply for STK85xx

Attention: there is a plus-mark close to X82. This plus mark is for PCB-adjustment only; it does not mark the polarity of the supply voltage!

4.4.8 Power Supply 5 V

- Active only when the power supply is received from the board power supply (VCC5V_INN), deactivated when power supply is received from the ATX- power supply.

- Available on the screw clamp X85.1, X85.2, refer 4.4.7
- Synchronous regulator LTC1628 with external MOSFETs
- Ceramic input and output condensers

4.4.9 Power Supply 3.3 V

- Active only when the power supply is received from the board power supply (VCC3V3_INN), deactivated when the power supply is received from the ATX- power supply.
- Available on the screw clamp X81.1, X81.2, refer 4.4.7
- Synchronous regulator LTC1628 with external MOSFETs
- Ceramic input and output condensers

4.4.10 Power Supply 2.5 V

- Available on the screw clamp X87.3 (2V5_PHY), refer 4.4.7
- Synchronous regulator TPS40003 with external MOSFETs
- Ceramic input and output condensers

4.4.11 Power Supply 1 V

- Available on the screw clamp X87.1 (1V_PHY), refer 4.4.7
- Synchronous regulator TPS40003 with external MOSFETs
- Ceramic input and output condensers

4.5 Test-Functions

4.5.1 A/D-Converter

- Control via a PLD
  - via JTAG
  - via Local Bus (the required PLD-Program has not yet been created)
- A/D-Converter National ADC12048
- 8 channels, resolution 13 Bit or 12 Bit + Signs
- Utilized for measuring the power supply and reference voltage on the Module and STK85xx, optional free usage for general metering is possible (Change in the assembly 0 Ω / voltage divider, connection to X19)

Voltages metered for testing purposes:

Channel	Signal	Description
0	1V_PHY	1 V supply for GBit PHYs
1	2V5_PHY	2.5 V supply for GBit PHYs
2	VBAT	RTC Backup-Voltage not connected (R1006 removed to prevent G4 from being discharging when power off)
3	VCC3V3IN	3.3 V supply for TQ module
4	VCC5VF	5 V supply to or from TQ module, divided by 2: 1
5	VDD_TEST	CPU core voltage on TQ module
6	VREF	DDR SDRAM reference voltage on TQ module
7	VIN	Input voltage from AC adapter, divided by 5.4: 1

4.5.2 Test PLDs

- Almost each Signal for JTAG-Test should be guided to an un-programmed PLD
- PLD Lattice LC4032V-75TN48C
  Reference: The internal Pull-Ups are activated in an un-programmed state!
- In order to solve the signal quality problems by unfavorable Routing and / or high load, each individual Pin of the Test PLDs can be separated by a 0-Ω-resistance.
- Further, in the case of problems, 0-Ω- resistance can be replaced by a higher value e.g. 47k with the help of the internal Pull-Up.
- For the current status, refer to the Test PLDs schematics and parts list.

4.5.3 Scan-chain, JTAG- and Programmer adaptor

- All the JTAG capable components form a single scan chain for the entire STK85xx, refer below
- The PLD on the TQ-Module can be contacted by testing pins and X55
- The PLDs can be used in the normal mode besides the pure JTAG-function and should be programmed accordingly. PLDs can also be contacted separately.

Scan-chain 1 (Top most component is the last in the JTAG-chain)

Device	Description
D60	Test-PLD
D45	- " -
D64	- " -
D61	- " -
D65	- " -

Device	Description
D66	- " -
D69	- " -
D67	- " -
D68	- " -
D35	- " -
D63	- " -
D58	- " -
D51	- " -
D50	- " -
D62	Test-PLD
D71	- " -
D52	- " -
D40	- " -
D57	- " -
D48	- " -
D59	- " -
D42	- " -
D49	- " -
D70	- " -
D41	- " -
D44	- " -
D43	- " -
D37	Bus Driver PLD
D39	ADC Control PLD
D38	Clock Divider
D21	PCI Bus Control
D28	GBit Ethernet PHY 88E1111 TSEC2
D13	GBit Ethernet PHY 88E1111 TSEC1
D5	Fast Ethernet PHY LXT971A

Scan-chain 2 (Top most component is the last in the JTAG-chain)

Device	Description
TN1, TN2, TN3, TN4	PLD on TQ module
D2 (X1)	CPU on TQ module

Programmer connector PLDs (suitable for the Lattice-Programmer adapter):

Connector	Device	Description
X45	D21	PCI Bus Control PLD
X90	D37	Bus Driver PLD
X55	TN1, TN2, TN3, TN4	PLD on TQ module

Further JTAG-adaptors (assignment; refer power supply diagram):

Connector	Device	Description
X36	D5	Fast Ethernet PHY LXT971A
X31	D13	Gbit Ethernet PHY 88E1111 TSEC1
X71	D28	Gbit Ethernet PHY 88E1111 TSEC2

Other programmer adaptors

Connector	Device	Description
X40	D11	PS/2-Controller PIC16F627, mates with Microchip programming tools (e. g. ICD2)

4.5.4 Testing pins

- Signals that are used only for the module tests are not guided to the module connector, but to the testing point on the lower side of the module.
- All test points can be directly contacted by the test pins soldered in the STK85xx- circuit board (diameter 1.37 mm, length unloaded / fitted with springs 15.5 / 12 mm)
- If the signals are not available on other connectors, the signals are provided on X74.

X74:

Pin	Test Pin	Signal	Description
1	TN6	WP#/ACC	Flash on TQ module, WP#/ACC pins (connected together)
2	TN8	CFG_ERR	PLD on TQ module, configuration error CFG_ERR
3	TN10	CFG_RDY	PLD on TQ module, configuration ready CFG_RDY
4	TN7	LATCH_OE#	Address Latch on TQ module, output enable OE#
8		DGND	

4.5.5 CPU-Type

- The processor type can be changed within the CPU through the circuit of the TESTSEL-Signals
- The change is not a documented feature; there is no functional guarantee.

Jumper:

X88	CPU Type
Open	Original CPU type as determined by TQ module
1 – 2	TQM8560/40: TESTSEL = low, force to 8540 TQM8555/41: TESTSEL0 = low, force to 8541 TQM8349L/47L: TEST_SEL = low, force to 8349E
2 – 3	TQM8560/40: TESTSEL = high, force to 8560 TQM8555/41: TESTSEL0 = high, force to 8555 TQM8349L/47L: TEST_SEL = high, force to 8347E

4.6 Jumpers Description

The following table shows the available Jumper. The possible settings are described in the associated chapters.

Reference	Description	Default setting	
X4	TSEC1 Interrupt	Open	Disabled
X1	TSEC2 Interrupt	Open	Disabled
X53	Fast Ethernet Interrupt	Open	Disabled
X2	Fast Ethernet Management data interface	1 – 2	Enabled
X47 / X50	Fast Ethernet MII multiplexing	a – d (X50.2 – 3)	FCC3 (TQM8560) / FEC (TQM8540) selected
X63	External Rapid I/O clock	All open	Disabled
X12	Shutdown RS232-Transceiver (SHDN#)	Open	Disabled
X104	Shutdown RS232-Enable (EN#)	Open	Disabled
X61	RXD2# / UART_SIN1# usage	Open	Not connected
X52	M66EN	Open	Determined by cards
X49	PCI-X Enable	Open	All slots active
X109	PC-Card Controller Reset	Open	Controlled by PLD
X26	Ground on Interface	Open	Open
X27	5 V on Interface	Open	Open
X28	Termination CAN1	Open	No termination
X29	Termination CAN2	Open	No termination
X66	RS232 interface selector	Open	No interface selected
X37	JTAG / Debug Parallel TCK	Open	Disabled
X59	JTAG / Debug Parallel TDI	Open	Disabled
X7	JTAG / Debug Parallel TMS	Open	Disabled
X6	TQM8560.1xx/2xx Self-Reset Compatibility	Open	Newer rev. / TQM8555/41
X57	Permanent Reset	Open	Normal operation
X58	Self-Reset Disable	Open	Self-Reset enabled
X30	General Purpose LEDs PCI / TSEC	1 – 2	PCI_AD
X67	General Purpose LEDs TSEC1 / 2	Open	TSEC2
X79	Fan Speed Signal	Open	Disabled
X41	3.3 V Enable	1 – 2	Enabled
X62	5 V Enable	1 – 2	Enabled
X88	CPU Type	Open	Default

5 Mechanical- Specification

5.1 Dimensions

STK85xx is mechanically compatible with the ATX-Form factor of PC-Motherboards. The outer dimensions of STK85xx are 305 mm * 244 mm. The following Illustration shows the important dimensions.

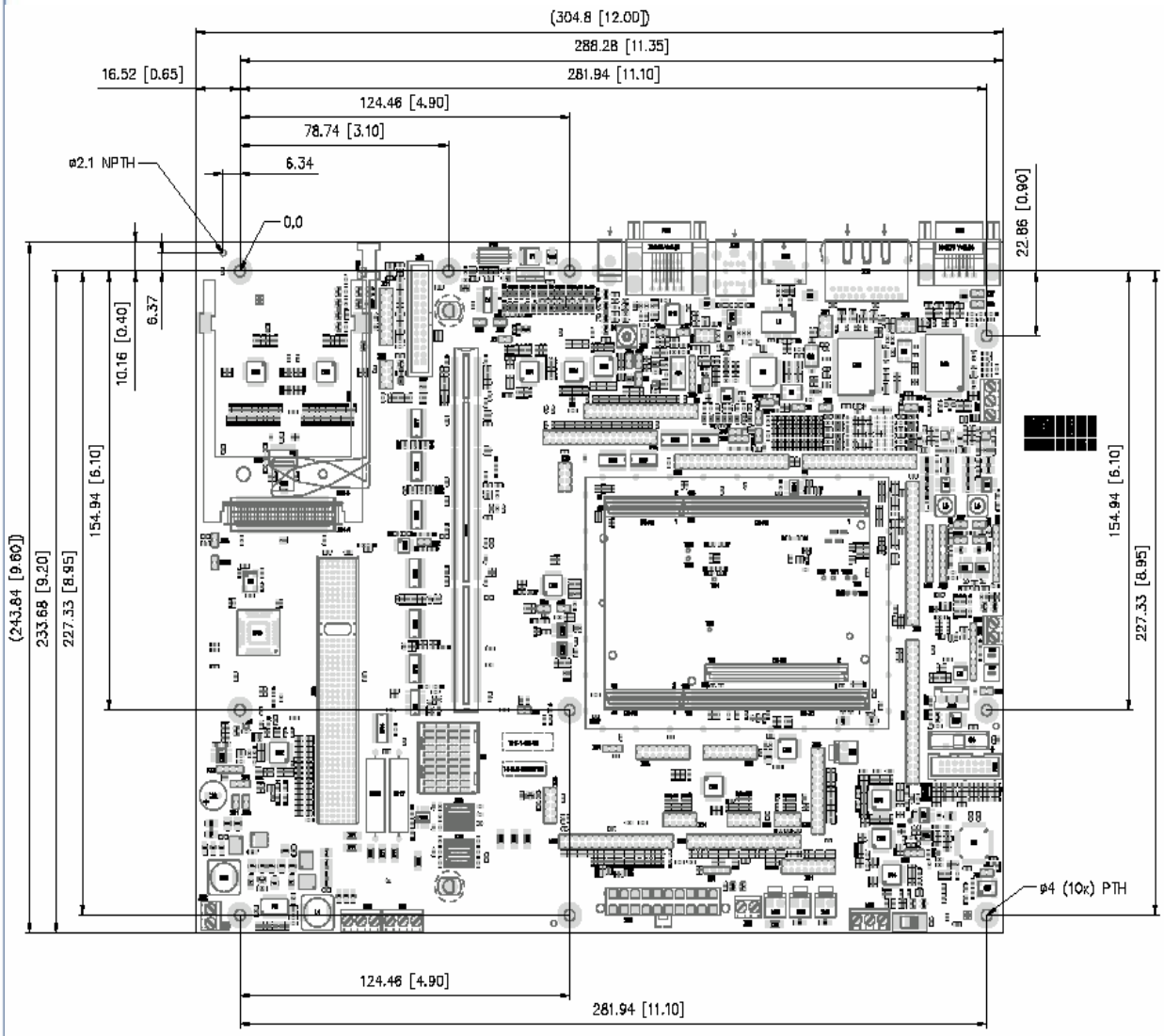

Illustration 7: Dimensioned Drawing STK85xx

6 Safety requirements and protection provisions

6.1 Climatic and installation conditions

Ambient Temperature : 0 ... 50 °C

Storage Temperature : -25 ... + 70 °C

Protection Class : IP00 (no special protection against foreign bodies and moisture)

6.2 Reliability and durability

The components are designed for a typical durability period of 5 years.

6.3 Environment protection

We contribute to environment protection by environment friendly processes, operating tools and products.

To reuse the used product, it is manufactured in such a manner that it can be easily repaired.

7 Enclosures

7.1 Further documents

[1] MPC8560 Integrated Processor Hardware Specifications
MPC8560EC Rev. 3.2, Freescale Semiconductor Inc. 06/2005

[2] MPC8555E Integrated Communications Processor Reference Manual
MPC8555ERM Rev. 1, Freescale Semiconductor Inc. 08/2004