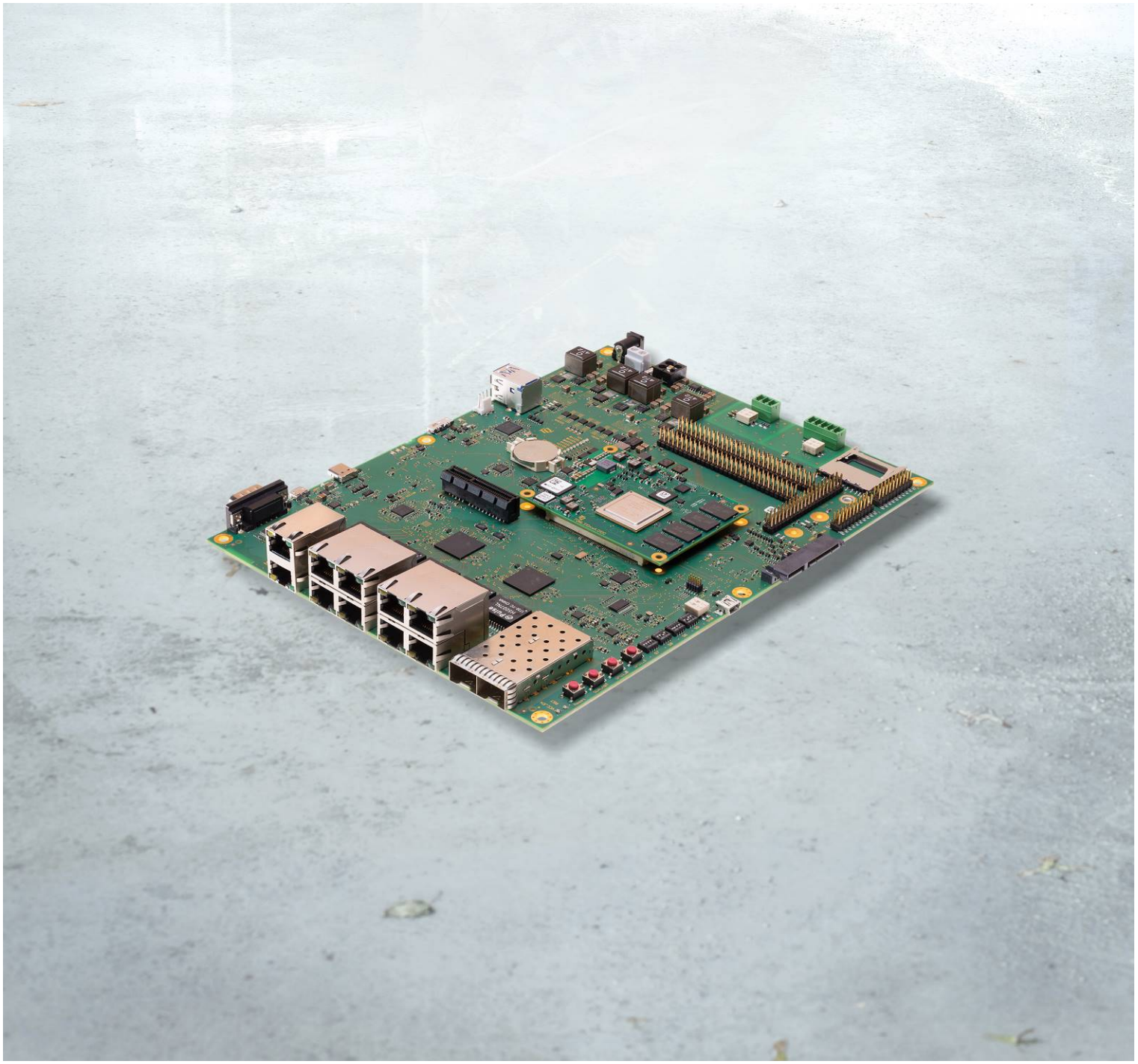
MBLS10xxA
User's Manual

MBLS10xxA UM 0100
11.07.2020



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	11.07.2020	Petz		First edition

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBLS10xxA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLS10xxA circuit diagram
- TQMLS10xxA User's Manual
- LS10xxA Data Sheets
- LS10xxA Reference Manuals
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMLS10xxA

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBLS10xxA as of revision 0200.

The MBLS10xxA is designed as a carrier board for the TQMLS10xxA. Core of the system is the TQMLS10xxA with an NXP CPU LS1043A, LS1046A or LS1088A. The TQMLS10xxA connects all peripheral components.

In addition to the standard communication interfaces such as USB, Ethernet, RS-232, RS-485 etc., all other available signals of the TQMLS10xxA are routed on 100 mil standard pin headers on the MBLS10xxA.

Currently five Layerscape CPUs are supported:

- LS1023A (Dual Cortex®-A53)
- LS1043A (Quad Cortex®-A53)
- LS1026A (Dual Cortex®-A72)
- LS1046A (Quad Cortex®-A72)
- LS1088A (Octal Cortex®-A53)

Other CPU derivatives can be supported on request.

CPU features and interface can be evaluated, software development for a TQMLS10xxA-based project can start immediately.

3. TECHNICAL DATA

3.1 MBLS10xxA block diagram

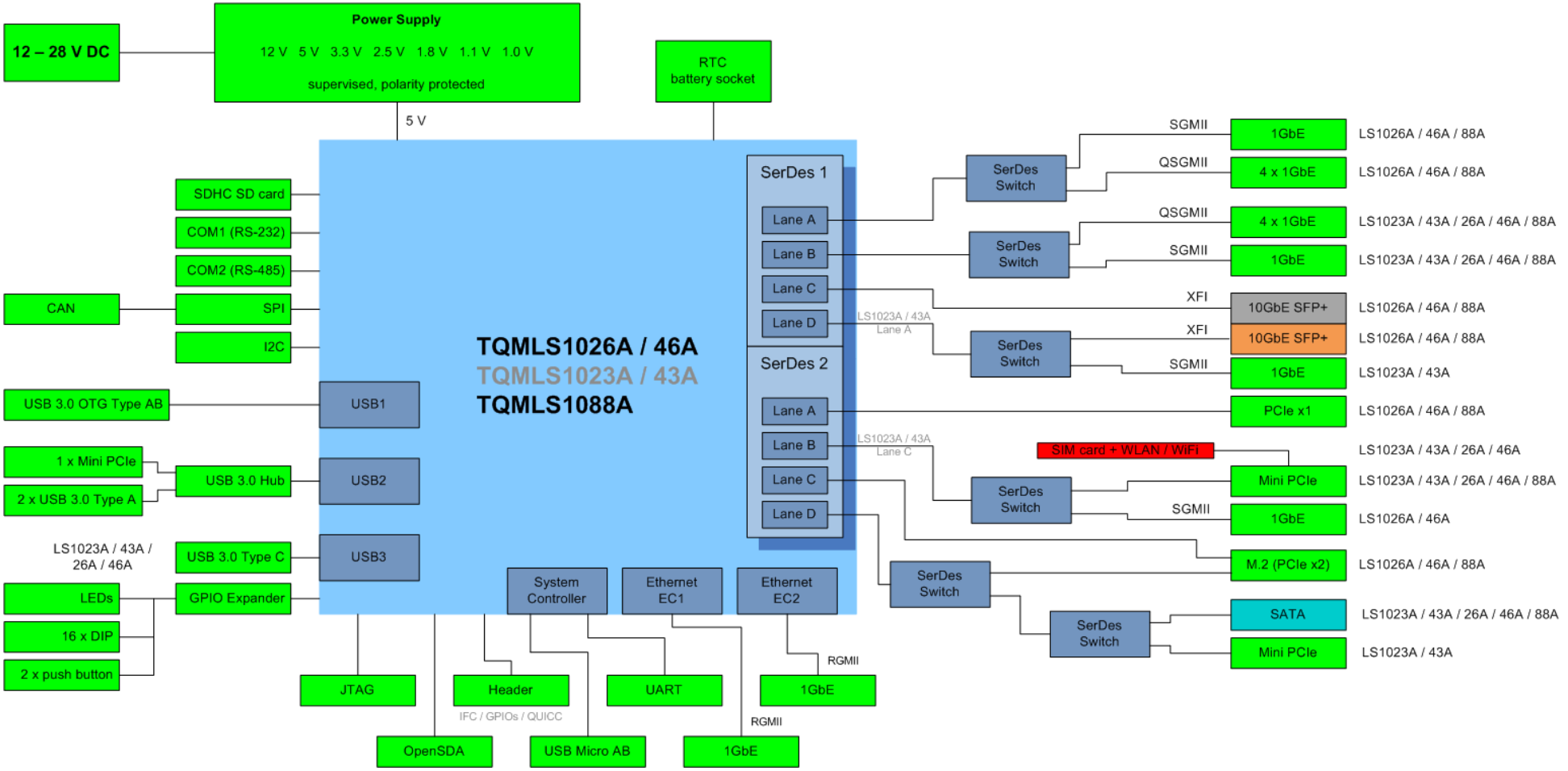

Figure 1: Block diagram MBLS10xxA

3.2 MBLS10xxA data interfaces

The following interfaces/functions and user interfaces are available on the MBLS10xxA:

Table 2: Overview data interfaces

Interface	Qty.	Connector	Type	Remark
USB 2.0 Hi-Speed Host	1	X19	100 mil header	–
USB 2.0 Hi-Speed Host	1	X6	Mini PCIe slot	–
USB 3.0 SS Host	2	X15	USB, Type A	Stacked
USB 3.0 SS OTG	1	X35	USB, Micro B	–
USB 3.0 SS	1	X16	USB, Type C	CPU derivative dependent
Ethernet, 10 Gbit	2	X41, X42	SFP	1 × 2-fold, CPU derivative dependent
Ethernet, 1000 Base-T	2	X12	RJ45	1 × 2-fold, RGMII, with integrated magnetics
Ethernet, 1000 Base-T	8	X39, X40	RJ45	2 × 4-fold, QSGMII/SGMII, with integrated magnetics, CPU derivative dependent
CAN	1	X24	Phoenix, 3-pin	Via SPI/CPLD, Galvanically separated
RS-485	1	X23	Phoenix, 5-pin	Galvanically separated
RS-232	1	X29	D-Sub9	Debug UART
OpenSDA	1	X33	Mini USB Type B	
M.2 PCIe	1	X5	M.2 M key (PCIe ×2)	
SD card	1	X10	Push-Pull	–
SATA	1	X9	Slimline SATA connector	–
PCIe	1	X13	PCIe (×1)	CPU derivative dependent
	2	X6, X7	Mini PCIe	
	1	X8	SIM Card holder	
Headers	3	X19 X17, X18	100 mil headers 1 × 40-pin 2 × 60-pin	Power-Out (12 V, 5 V, 3.3 V), 1 × IFC, 5 × GPIO from CPLD, 1 × ECSPI (4 × Chip Select), 2 × UART, (1 × with handshake), 3 × I^2C, 1 × SDHC (SYNC In-/Output), 1 × FTM (8 channels), 4 × IRQ, 1 × SDA_UART (TX / RX), 17 × signals from TQMLS10xxA, 6 × EVT#, 4 × PHY_GPIO (Ethernet-Controller), 1 × USB
Power In	1	X14	DC jack (2.5 mm / 5.5 mm)	V_{IN} = 24 V DC ±5 %
	1	X36	2-pin screw terminal block	
Coin cell	1	X22	CR2032 holder	Backup battery for RTC on TQMLS10xxA

3.3 MBLS10xxA diagnostic and user interfaces

The MBLS10xxA provides the following diagnostic and user interfaces:

Table 3: Overview diagnostic and user interfaces

Interface	Qty.	Component	Remark
Status LEDs	6	Green LED	1 × USB1_VBUS 1 × USB2_VBUS 1 × USB3_VBUS 1 × USB_H1_VBUS 1 × USB_H2_VBUS 1 × USB_H3_VBUS
	3	Green LED	Mini PCIe WWAN, WLAN, WPAN
	1	Green LED	GPIO LED at port expander
	9	Green LED	Power LEDs (24 V, 12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.1 V, 1.0 V)
	1	Green LED	M.2 interface
	1	Green / red LED	VCC_EN / BUTTON_RST# (Reset LED)
	12	Green / yellow LED	Ethernet LEDs (Activity / Speed)
	1	Green LED	OpenSDA
Power / Reset button	2	Push button	MB_RST# / RESIN# SDA_RST_IN# / JTAG_TRST#
Navigation button	2	Push button	GPIO push button at port expander
Boot-Mode configuration	4	DIP switch	2 × Boot-Source configuration 1 × Boot-Device configuration (eMMC/SD) 1 × MCU_BOOTLDR (system controller)
Lane / Clock / PHY configuration	12	DIP switch	6 × Lane configuration 1 × Demuxing configuration 3 × Clock configuration (1 × SerDes / 2 × QSGMII) 2 × PHY configuration (QSGMII / SGMII)
CAN / RS-485 termination	2	DIP switch	–
JTAG	2	20-pin, 100 mil header	CPU / system controller

4. ELECTRONICS

4.1 System components

4.1.1 TQMLS10xxA

The TQMLS10xxA is the central system component. It provides DDR4 SDRAM, eMMC, NOR flash and an EEPROM. All TQMLS10xxA internal voltages are derived from the 5 V supply voltage. Further information can be found in the TQMLS10xxA User's Manual.

The available signals are routed to the MBLS10xxA to four connectors. On the MBLS10xxA the standard interfaces like USB, Ethernet, RS-232, or RS-485 provided by the TQMLS10xxA are routed to industry standard connectors. All other signals und buses provided by the TQMLS10xxA are routed to 100 mil headers.

Furthermore the MBLS10xxA provides all power supplies and configurations required for the operation of the TQMLS10xxA.

The MBLS10xxA supports TQMLS10xxA modules with an LS1023A, LS1043A, LS1026A, LS1046A, or LS1088A CPU.

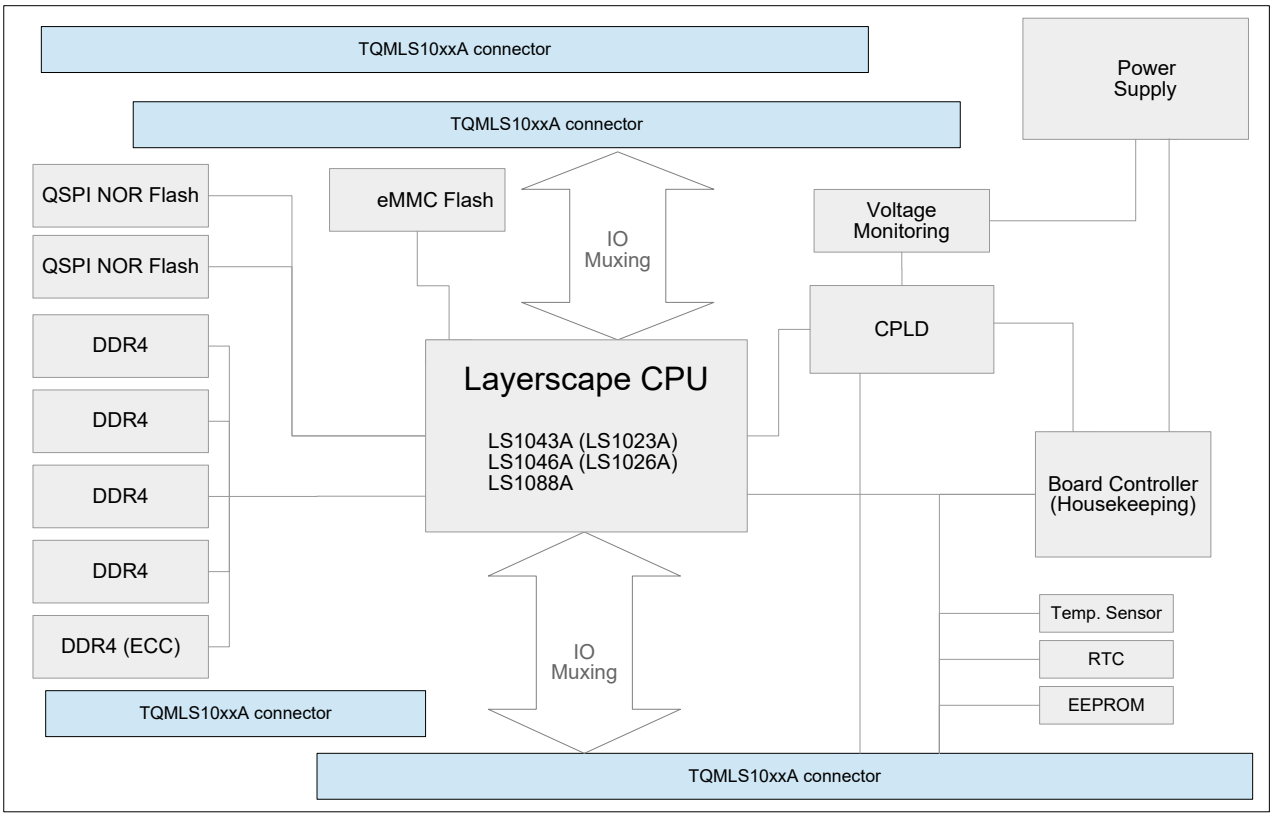

Figure 2: Block diagram TQMLS10xxA

4.1.1.1 TQMLS10xxA pinout

All available TQMLS10xxA signals are routed to four connectors on the MBLS10xxA.

Note: Available interfaces	
	Depending on the TQMLS10xxA derivative not all interfaces are available. Refer to the TQMLS10xxA User's Manual and the TQMLS10xxA pinout table for available interfaces.

4.1.1.1 TQMLS10xxA pinout (continued)

Table 4: Pinout TQMLS10xxA connector X1

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	–	5 V	Power	VIN	1	2	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	3	4	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	5	6	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	7	8	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	9	10	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	11	12	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	13	14	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	15	16	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	17	18	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	19	20	VIN	Power	5 V	–	–
–	–	5 V	Power	VIN	21	22	VIN	Power	5 V	–	–
–	–	0 V	Ground	DGND	23	24	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	25	26	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	27	28	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	29	30	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	31	32	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	33	34	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	35	36	DGND	Ground	0 V	–	–
–	–	3.0 V	Power	VBAT	37	38	VCC1V8	Power	1.8 V	–	–
–	–	1.8 V	Power	VCC1V8	39	40	VCC3V3	Power	3.3 V	–	–
–	–	1.8 V	Power	VCC1V8	41	42	VCC3V3	Power	3.3 V	–	–
–	–	1.8 V	Power	VCC1V8	43	44	VCC1V2_MOD	Power	1.2 V	–	–
–	–	1.2 V	Power	VCC1V2_MOD	45	46	NC	NC	–	–	–
–	–	1.2 V	Power	VCC1V2_MOD	47	48	NC	NC	–	–	–
–	–	2.5 V	Power	VCC2V5	49	50	LVDDIN	Power	1.8 / 2.5 / 3.3 V	–	–
–	–	2.5 V	Power	VCC2V5	51	52	LVDDIN	Power	1.8 / 2.5 / 3.3 V	–	–
–	–	1.8 / 2.5 / 3.3 V	Power	VCCGPIIN	53	54	LVDDIN	Power	1.8 / 2.5 / 3.3 V	–	–
–	–	1.8 / 2.5 / 3.3 V	Power	VCCGPIIN	55	56	DVDD	Power	1.8 / 2.5 / 3.3 V	–	–
–	–	1.2 / 1.8 / 2.5 V	Power	TVDD	57	58	DVDD	Power	1.8 / 2.5 / 3.3 V	–	–
–	–	1.2 / 1.8 / 2.5 V	Power	TVDD	59	60	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	61	62	USR_GPIO_6	SYSTEM	1.8 / 2.5 / 3.3 V (1)	I	–
–	I	1.8 / 2.5 / 3.3 V (1)	SYSTEM	USR_GPIO_7	63	64	DGND	Ground	0 V	–	–
–	–	3.3 V	Factory Test	I2C_BRD_SDA	65	66	BCTL_UARTx_TX	Factory Test	–	O	–
–	–	3.3 V	Factory Test	I2C_BRD_SCL	67	68	BCTL_UARTx_RX	Factory Test	–	I	–
–	–	0 V	Ground	DGND	69	70	DGND	Ground	0 V	–	–
B8	I/O	1.8 V (2)	IFC	IFC_AD00	71	72	USR_GPIO_1	SYSTEM	1.8 / 2.5 / 3.3 V (1)	I	–
A8	I/O	1.8 V (2)	IFC	IFC_AD01	73	74	USR_GPIO_2	SYSTEM	1.8 / 2.5 / 3.3 V (1)	I	–
B9	I/O	1.8 V (2)	IFC	IFC_AD02	75	76	USR_GPIO_3	SYSTEM	1.8 / 2.5 / 3.3 V (1)	I	–
A9	I/O	1.8 V (2)	IFC	IFC_AD03	77	78	USR_GPIO_4	SYSTEM	1.8 / 2.5 / 3.3 V (1)	I	–
A10	I/O	1.8 V (2)	IFC	IFC_AD04	79	80	USR_GPIO_5	SYSTEM	1.8 / 2.5 / 3.3 V (1)	I	–
B11	I/O	1.8 V (2)	IFC	IFC_AD05	81	82	DGND	Ground	0 V	–	–
A11	I/O	1.8 V (2)	IFC	IFC_AD06	83	84	IFC_PERR#	IFC	1.8 V (2)	I/O	E17
B12	I/O	1.8 V (2)	IFC	IFC_AD07	85	86	IFC_PAR0	IFC	1.8 V (2)	I/O	B18
–	–	0 V	Ground	DGND	87	88	IFC_PAR1	IFC	1.8 V (2)	I/O	D17
A12	I/O	1.8 V (2)	IFC	IFC_AD08	89	90	IFC_NDDQS	IFC	1.8 V (2)	I/O	B17
A13	I/O	1.8 V (2)	IFC	IFC_AD09	91	92	DGND	Ground	0 V	–	–
B14	I/O	1.8 V (2)	IFC	IFC_AD10	93	94	IFC_AVD	IFC	1.8 V (2)	O	A18
A14	I/O	1.8 V (2)	IFC	IFC_AD11	95	96	IFC_BCTL	IFC	1.8 V (2)	O	E15
B15	I/O	1.8 V (2)	IFC	IFC_AD12	97	98	IFC_CLE	IFC	1.8 V (2)	I/O	C19
A15	I/O	1.8 V (2)	IFC	IFC_AD13	99	100	DGND	Ground	0 V	–	–
A16	I/O	1.8 V (2)	IFC	IFC_AD14	101	102	IFC_CLK0	IFC	1.8 V (2)	O	A20
A17	I/O	1.8 V (2)	IFC	IFC_AD15	103	104	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	105	106	IFC_CLK1	IFC	1.8 V (2)	O	B20
C16	I	1.8 V (2)	IFC	IFC_RB0#	107	108	DGND	Ground	0 V	–	–
D16	I	1.8 V (2)	IFC	IFC_RB1#	109	110	IFC_CS0#	IFC	1.8 V (2)	O	C17
E14	O	1.8 V (2)	IFC	IFC_TE	111	112	IFC_CS1#	IFC	1.8 V (2)	I/O	A19
C15	O	1.8 V (2)	IFC	IFC_WE0#	113	114	IFC_CS2#	IFC	1.8 V (2)	I/O	D20
D19	O	1.8 V (2)	IFC	IFC_WP0#	115	116	IFC_CS3#	IFC	1.8 V (2)	I/O	C20
E16	O	1.8 V (2)	IFC	IFC_NDDDR_CLK	117	118	IFC_OE#	IFC	1.8 V (2)	I/O	C18
–	–	0 V	Ground	DGND	119	120	DGND	Ground	0 V	–	–

1: VCCGPIIN (X1-53, 55)
2: OVDD

4.1.1.1 TQMLS10xxA pinout (continued)

Table 5: Pinout TQMLS10xxA connector X2

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	–	0 V	Ground	DGND	1	2	DGND	Ground	0 V	–	–
F11	I	1.8 V (3)	IRQ	IRQ0	3	4	IRQ2	IRQ	1.8 V (3)	I	H7
F15	I	1.8 V (3)	IRQ	IRQ1	5	6	IRQ11	IRQ	1.8 / 2.5 V (4)	I/O	W3
–	–	0 V	Ground	DGND	7	8	DGND	Ground	0 V	–	–
M5	I/O	1.8 / 3.3 V (5)	IRQ	FTM3_CH4	9	10	FTM3_CH0	IRQ	1.8 / 3.3 V (5)	I/O	J4
N5	I/O	1.8 / 3.3 V (5)	IRQ	FTM3_CH5	11	12	FTM3_CH1	IRQ	1.8 / 3.3 V (5)	I/O	J5
P4	I/O	1.8 / 3.3 V (5)	IRQ	FTM3_CH6	13	14	FTM3_CH2	IRQ	1.8 / 3.3 V (5)	I/O	K5
J3	I/O	1.8 / 3.3 V (5)	IRQ	FTM3_CH7	15	16	FTM3_CH3	IRQ	1.8 / 3.3 V (5)	I/O	L5
F5	I	–	USB	USB1_ID	17	18	DGND	Ground	0 V	–	–
E7	I	–	USB	USB1_VBUS	19	20	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	21	22	USB1_TX_P	USB	–	O	F1
–	–	0 V	Ground	DGND	23	24	USB1_TX_M	USB	–	O	F2
F6	I/O	–	USB	USB1_D_P	25	26	DGND	Ground	0 V	–	–
E6	I/O	–	USB	USB1_D_M	27	28	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	29	30	USB1_RX_P	USB	–	I	E3
–	–	0 V	Ground	DGND	31	32	USB1_RX_M	USB	–	I	E4
G6	I/O	1.8 / 3.3 V (5)	USB	USB_PWRFAULT	33	34	DGND	Ground	0 V	–	–
H6	I/O	1.8 / 3.3 V (5)	USB	USB_DRVBUS	35	36	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	37	38	USB2_TX_P	USB	–	O	D1
–	–	0 V	Ground	DGND	39	40	USB2_TX_M	USB	–	O	D2
D5	I/O	–	USB	USB2_ID	41	42	DGND	Ground	0 V	–	–
C7	I/O	–	USB	USB2_VBUS	43	44	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	45	46	USB2_RX_P	USB	–	I	C3
–	–	0 V	Ground	DGND	47	48	USB2_RX_M	USB	–	I	C4
D6	I/O	–	USB	USB2_D_P	49	50	DGND	Ground	0 V	–	–
C6	I/O	–	USB	USB2_D_M	51	52	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	53	54	USB3_TX_P	USB	–	O	B1
–	–	0 V	Ground	DGND	55	56	USB3_TX_M	USB	–	O	B2
B6	I/O	–	USB	USB3_D_P	57	58	DGND	Ground	0 V	–	–
A6	I/O	–	USB	USB3_D_M	59	60	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	61	62	USB3_RX_P	USB	–	I	A3
–	–	0 V	Ground	DGND	63	64	USB3_RX_M	USB	–	I	A4
M4	I/O	1.8 / 3.3 V (5)	USB	USB2_PWRFAULT	65	66	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	67	68	DGND	Ground	0 V	–	–
P3	I/O	1.8 / 3.3 V (6)	SDHC	SDHC_CLK_MOD	69	70	USB2_DRVVBUS	USB	1.8 / 3.3 V (5)	I/O	L4
–	–	0 V	Ground	DGND	71	72	USB3_VBUS	USB	–	I	A7
U3	I/O	1.8 V (3)	SDHC	SDHC_CLK_SYNC_IN	73	74	USB3_ID	USB	–	I	B5
–	–	0 V	Ground	DGND	75	76	DGND	Ground	0 V	–	–
V3	I/O	1.8 V (3)	SDHC	SDHC_CLK_SYNC_OUT	77	78	SPI_SCK	SPI	1.8 V (3)	O	U2
–	–	0 V	Ground	DGND	79	80	DGND	Ground	0 V	–	–
P1	I/O	1.8 / 3.3 V (6)	SDHC	SDHC_DAT0_MOD	81	82	SPI_PCS0	SPI	1.8 V (3)	I/O	U1
R2	I/O	1.8 / 3.3 V (6)	SDHC	SDHC_DAT1_MOD	83	84	SPI_PCS1	SPI	1.8 V (3)	I/O	R3
R1	I/O	1.8 / 3.3 V (6)	SDHC	SDHC_DAT2_MOD	85	86	SPI_PCS2	SPI	1.8 V (3)	I/O	T3
T1	I/O	1.8 / 3.3 V (6)	SDHC	SDHC_DAT3_MOD	87	88	SPI_PCS3	SPI	1.8 V (3)	I/O	V1
–	–	0 V	Ground	DGND	89	90	DGND	Ground	0 V	–	–
P2	I/O	1.8 / 3.3 V (6)	SDHC	SDHC_CMD_MOD	91	92	SPI_SIN	SPI	1.8 V (3)	I/O	U3
K3	I/O	1.8 / 3.3 V (5)	SDHC	SDHC_CD#	93	94	SPI_SOUT	SPI	1.8 V (3)	I/O	V3
L3	I/O	1.8 / 3.3 V (5)	SDHC	SDHC_WP	95	96	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	97	98	IIC1_SCL_MOD	I2C	3.3 V	O	N1
J1	I/O	1.8 / 3.3 V (5)	UART	UART1_CTS#	99	100	IIC1_SDA_MOD	I2C	3.3 V	I/O	M1
J2	I/O	1.8 / 3.3 V (5)	UART	UART1_RTS	101	102	IIC4_SCL	I2C	1.8 / 3.3 V (5)	I/O	M3
H2	I	1.8 / 3.3 V (5)	UART	UART1_SIN	103	104	IIC4_SDA	I2C	1.8 / 3.3 V (5)	I/O	N3
H1	O	1.8 / 3.3 V (5)	UART	UART1_SOUT (7)	105	106	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	107	108	EVT9#	SYSTEM	1.8 V (3)	I/O	G7
K1	I/O	1.8 / 3.3 V (5)	UART	UART2_SIN	109	110	CPU_ASLEEP	SYSTEM	1.8 V (3)	I/O	E9
L2	I/O	1.8 / 3.3 V (5)	UART	UART2_SOUT (7)	111	112	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	113	114	CLK_OUT	SYSTEM	1.8 V (3)	O	G16
–	O	3.3 V	SYSTEM	TEMP_CRIT_MOD#	115	116	DGND	Ground	0 V	–	–
–	I	3.3 V	SYSTEM	RESIN#	117	118	CPU_RTC	SYSTEM	1.8 V (3)	I/O	F17
–	O	3.3 V	SYSTEM	RESET_OUT#	119	120	CLKOE	Factory Test	3.3 V	I	–

3: OVDD
4: LVDDIN (X1-50, 52, 54)
5. DVDD
6: EVDD
7: 4.7 kΩ Pull-Up on carrier board is recommended.

4.1.1.1 TQMLS10xxA pinout (continued)

Table 6: Pinout TQMLS10xxA connector X3

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	–	0 V	Ground	DGND	1	2	DGND	Ground	0 V	–	–
AG2	I/O	1.8 / 2.5 V (8)	EC1	EMI1_MDC	3	4	EMI1_MDIO	EC1	1.8 / 2.5 V (8)	I/O	AF2
–	–	0 V	Ground	DGND	5	6	DGND	Ground	0 V	–	–
AC3	I/O	1.8 / 2.5 V (8)	EC1	EC1_GTX_CLK125	7	8	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	9	10	EC1_GTX_CLK	EC1	1.8 / 2.5 V (8)	I/O	W4
W1	I/O	1.8 / 2.5 V (8)	EC1	EC1_RX_CLK	11	12	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	13	14	EC1_TX_EN	EC1	1.8 / 2.5 V (8)	I/O	AB4
AB1	I/O	1.8 / 2.5 V (8)	EC1	EC1_RX_DV	15	16	EC1_TXD0	EC1	1.8 / 2.5 V (8)	I/O	AB3
AA2	I/O	1.8 / 2.5 V (8)	EC1	EC1_RXD0	17	18	EC1_TXD1	EC1	1.8 / 2.5 V (8)	I/O	AA3
AA1	I/O	1.8 / 2.5 V (8)	EC1	EC1_RXD1	19	20	EC1_TXD2	EC1	1.8 / 2.5 V (8)	I/O	Y4
Y1	I/O	1.8 / 2.5 V (8)	EC1	EC1_RXD2	21	22	EC1_TXD3	EC1	1.8 / 2.5 V (8)	I/O	Y3
W2	I/O	1.8 / 2.5 V (8)	EC1	EC1_RXD3	23	24	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	25	26	SWDIO	Factory Test	3.3 V	I/O	–
–	I	1.8 / 3.3 V (9)	SYSTEM	SDHC_EXT_SEL	27	28	SWCLK	Factory Test	3.3 V	I/O	–
–	O	3.3 V	SYSTEM	RTC_INT_OUT	29	30	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	31	32	JTAG_TDI	JTAG	3.3 V	I	–
E10	I/O	1.8 V (10)	EVENT	EVT0#	33	34	JTAG_TDO	JTAG	3.3 V	O	–
E13	I/O	1.8 V (10)	EVENT	EVT1#	35	36	JTAG_TMS	JTAG	3.3 V	I	–
E8	I/O	1.8 V (10)	EVENT	EVT2#	37	38	JTAG_TRST#	JTAG	3.3 V	I	–
E12	I/O	1.8 V (10)	EVENT	EVT3#	39	40	JTAG_TCK	JTAG	3.3 V	I	–
E11	I/O	1.8 V (10)	EVENT	EVT4#	41	42	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	43	44	CKSTP_OUT#	SYSTEM	1.8 V (10)	O	G15
–	I	3.3 V	SYSTEM	BOOT_SRC1	45	46	PROG_SFP	SYSTEM	1.8 V (11)	I	–
–	I	3.3 V	SYSTEM	BOOT_SRC0	47	48	TA_BB_TMP_DETECT#	SYSTEM	0.9 / 1.0 V (12)	I	H12
–	I/O	3.3 V	SYSTEM	GPIO_EXP_01	49	50	TA_TMP_DETECT#	SYSTEM	1.8 V (10)	I	H20
F8	I	1.8 V (10)	SYSTEM	HRESET#	51	52	TBSCAN_EN#	SYSTEM	1.8 V (10)	I	F19
F9	O	1.8 V (10)	SYSTEM	PORESET#	53	54	NC	NC	–	–	–
–	O	3.3 V	SYSTEM	RESET_REQ_OUT#	55	56	POWER_GOOD	SYSTEM	3.3 V	O	–
–	I	3.3 V	SYSTEM	POWER_FAIL	57	58	SLEEP	SYSTEM	3.3 V	I	–
–	–	0 V	Ground	DGND	59	60	DGND	Ground	0 V	–	–

8: LVDDIN (X1-50, 52, 54)
9: EVDD
10: OVDD
11: TA_PROG_SFP
12: TA_BB_VDD

4.1.1.1 TQMLS10xxA pinout (continued)

Table 7: Pinout TQMLS10xxA connector X4

CPU ball	Dir.	Level	Group	Signal	Pin		Signal	Group	Level	Dir.	CPU ball
–	–	0 V	Ground	DGND	1	2	DGND	Ground	0 V	–	–
AH4	I/O	1.2 / 1.8 / 2.5 V (13)	EC2	EMI2_MDC	3	4	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	5	6	EMI2_MDIO	EC2	1.2 / 1.8 / 2.5 V (13)	I/O	AH3
AG4	I/O	1.8 / 2.5 V (14)	EC2	EC2_GTX_CLK125	7	8	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	9	10	DGND	Ground	0 V	–	–
AC1	I/O	1.8 / 2.5 V (14)	EC2	EC2_RX_CLK	11	12	EC2_GTX_CLK	EC2	1.8 / 2.5 V (14)	I/O	AC4
–	–	0 V	Ground	DGND	13	14	DGND	Ground	0 V	–	–
AF1	I/O	1.8 / 2.5 V (14)	EC2	EC2_RX_DV	15	16	EC2_TX_EN	EC2	1.8 / 2.5 V (14)	I/O	AG3
AE2	I/O	1.8 / 2.5 V (14)	EC2	EC2_RXD0	17	18	EC2_TXD0	EC2	1.8 / 2.5 V (14)	I/O	AF3
AE1	I/O	1.8 / 2.5 V (14)	EC2	EC2_RXD1	19	20	EC2_TXD1	EC2	1.8 / 2.5 V (14)	I/O	AE4
AD1	I/O	1.8 / 2.5 V (14)	EC2	EC2_RXD2	21	22	EC2_TXD2	EC2	1.8 / 2.5 V (14)	I/O	AE3
AC2	I/O	1.8 / 2.5 V (14)	EC2	EC2_RXD3	23	24	EC2_TXD3	EC2	1.8 / 2.5 V (14)	I/O	AD3
–	–	0 V	Ground	DGND	25	26	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	27	28	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	29	30	SD1_TX0_N	SERDES	1.35 V (15)	O	AE6
–	–	0 V	Ground	DGND	31	32	SD1_TX0_P	SERDES	1.35 V (15)	O	AD6
AH6	I	0.9 / 1.0 V (16)	SERDES	SD1_RX0_N	33	34	DGND	Ground	0 V	–	–
AG6	I	0.9 / 1.0 V (16)	SERDES	SD1_RX0_P	35	36	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	37	38	SD1_TX1_N	SERDES	1.35 V (15)	O	AE8
–	–	0 V	Ground	DGND	39	40	SD1_TX1_P	SERDES	1.35 V (15)	O	AD8
AH8	I	0.9 / 1.0 V (16)	SERDES	SD1_RX1_N	41	42	DGND	Ground	0 V	–	–
AG8	I	0.9 / 1.0 V (16)	SERDES	SD1_RX1_P	43	44	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	45	46	SD1_TX2_N	SERDES	1.35 V (15)	O	AE10
–	–	0 V	Ground	DGND	47	48	SD1_TX2_P	SERDES	1.35 V (15)	O	AD10
AH10	I	0.9 / 1.0 V (16)	SERDES	SD1_RX2_N	49	50	DGND	Ground	0 V	–	–
AG10	I	0.9 / 1.0 V (16)	SERDES	SD1_RX2_P	51	52	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	53	54	SD1_TX3_N	SERDES	1.35 V (15)	O	AE11
–	–	0 V	Ground	DGND	55	56	SD1_TX3_P	SERDES	1.35 V (15)	O	AD11
AH11	I	0.9 / 1.0 V (16)	SERDES	SD1_RX3_N	57	58	DGND	Ground	0 V	–	–
AG11	I	0.9 / 1.0 V (16)	SERDES	SD1_RX3_P	59	60	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	61	62	SD2_TX0_N	SERDES	1.35 V (15)	O	AE15
–	–	0 V	Ground	DGND	63	64	SD2_TX0_P	SERDES	1.35 V (15)	O	AD15
AH15	I	0.9 / 1.0 V (16)	SERDES	SD2_RX0_N	65	66	DGND	Ground	0 V	–	–
AG15	I	0.9 / 1.0 V (16)	SERDES	SD2_RX0_P	67	68	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	69	70	SD2_TX1_N	SERDES	1.35 V (15)	O	AE16
–	–	0 V	Ground	DGND	71	72	SD2_TX1_P	SERDES	1.35 V (15)	O	AD16
AH16	I	0.9 / 1.0 V (16)	SERDES	SD2_RX1_N	73	74	DGND	Ground	0 V	–	–
AG16	I	0.9 / 1.0 V (16)	SERDES	SD2_RX1_P	75	76	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	77	78	SD2_TX2_N	SERDES	1.35 V (15)	O	AE18
–	–	0 V	Ground	DGND	79	80	SD2_TX2_P	SERDES	1.35 V (15)	O	AD18
AH18	I	0.9 / 1.0 V (16)	SERDES	SD2_RX2_N	81	82	DGND	Ground	0 V	–	–
AG18	I	0.9 / 1.0 V (16)	SERDES	SD2_RX2_P	83	84	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	85	86	SD2_TX3_N	SERDES	1.35 V (15)	O	AE19
–	–	0 V	Ground	DGND	87	88	SD2_TX3_P	SERDES	1.35 V (15)	O	AD19
AH19	I	0.9 / 1.0 V (16)	SERDES	SD2_RX3_N	89	90	DGND	Ground	0 V	–	–
AG19	I	0.9 / 1.0 V (16)	SERDES	SD2_RX3_P	91	92	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	93	94	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	95	96	SD1_REF_CLK1_N	SERDES	0.9 / 1.0 V (16)	I	AH13
–	–	0 V	Ground	DGND	97	98	SD1_REF_CLK1_P	SERDES	0.9 / 1.0 V (16)	I	AG13
AE13	I	0.9 / 1.0 V (16)	SERDES	SD2_REF_CLK1_N	99	100	DGND	Ground	0 V	–	–
AD13	I	0.9 / 1.0 V (16)	SERDES	SD2_REF_CLK1_P	101	102	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	103	104	SD1_REF_CLK2_N	SERDES	0.9 / 1.0 V (16)	I	AB8
–	–	0 V	Ground	DGND	105	106	SD1_REF_CLK2_P	SERDES	0.9 / 1.0 V (16)	I	AA8
AB19	I	0.9 / 1.0 V (16)	SERDES	SD2_REF_CLK2_N	107	108	DGND	Ground	0 V	–	–
AB18	I	0.9 / 1.0 V (16)	SERDES	SD2_REF_CLK2_P	109	110	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	111	112	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	113	114	DGND	Ground	0 V	–	–
M2	I	1.8 / 3.3 V (17)	UART	UART4_SIN	115	116	UART4_SOUT (18)	UART	1.8 / 3.3 V (17)	O	L1
–	–	0 V	Ground	DGND	117	118	DGND	Ground	0 V	–	–
–	–	0 V	Ground	DGND	119	120	DGND	Ground	0 V	–	–

13: TVDD (X1-57, 59)
14: LVDDIN (X1-50, 52, 54)
15: XVDD
16: SVDD
17. DVDD
18: 4.7 kΩ Pull-Up on carrier board is recommended.

4.1.1.2 MBLS10xxA connectors

The TQMLS10xxA is connected to the MBLS10xxA with 420 pins on four connectors.
The following table shows details of the connectors assembled on the MBLS10xxA:

Table 8: Connectors assembled on MBLS10xxA

Manufacturer	Pin count / part number	Qty.	Remark
TE connectivity	120-pin / 5177986-5	3	0.2 µm gold plating
	60-pin / 5177986-2	1	0.2 µm gold plating

The TQMLS10xxA is held in the mating connectors on the MBLS10xxA by 420 pins with a retention force of approximately 42 N.
To avoid damaging the connectors of the MBLS10xxA or the TQMLS10xxA while removing the TQMLS10xxA, the use of the extraction tool MOZI52XX is strongly recommended.

4.1.1.3 Boot configuration

With the MBLS10xxA all boot media intended for the TQMLS10xxA can be used.

- eMMC (on TQMLS10xxA)
- QSPI-Nor-Flash (on TQMLS10xxA)
- SD card (on MBLS10xxA)

After reading the SDHC_EXT_SEL and BOOT_SRC[1:0] boot configuration, the module-internal CPLD switches the RCW and the boot medium.
Information about the boot configurations of the LS10xxA can be found in the TQMLS10xxA User's Manual.

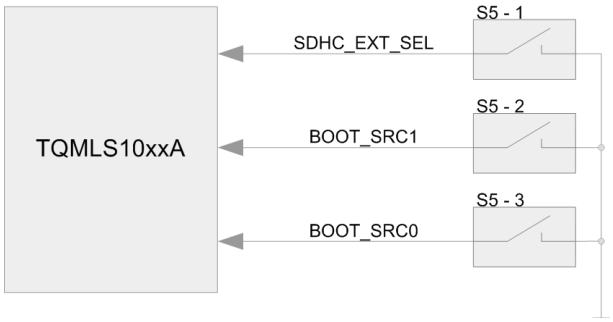

Figure 3: Block diagram Boot Modes, DIP switch S5

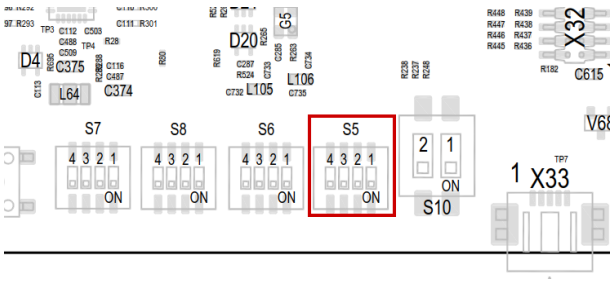

Figure 4: Position of DIP switch S5

The following table describes the DIP switch settings for the possible boot media and RCW configurations.
Further settings like transmission modes and CPU clock are described in the TQMLS10xxA User's Manual.
Switch position 1 (ON) means a low signal, switch position 0 (OFF) means a high signal.

Table 9: Boot Mode configuration, DIP switch S5

Boot Mode	S5-1 (SDHC_EXT_SEL)	S5-2 (BOOT_SRC1)	S5-3 (BOOT_SRC0)
SD card, on MBLS10xxA	OFF	X	X
eMMC, on TQMLS10xxA	ON	X	X
RCW	X	OFF	OFF
RCW	X	OFF	ON
RCW	X	ON	OFF
RCW	X	ON	ON

4.1.2 Clock generation

The following clock generators are used on the MBLS10xxA:

- A 24 MHz crystal for the USB hub (internal PLLs generate the clock for the internal USB PHY).
- Depending on the 3-pad assembly, the Ethernet controller is fed via a 125 MHz crystal oscillator, or from a 25 MHz crystal oscillator via the RGMII PHY. (The PHY has an internal PLL that multiplies to 125 MHz).
  By default, the circuitry with the 25 MHz crystal oscillator is used, the resistors for 125 MHz are not populated.
- A 25 MHz crystal on a clock generator (internal via PLL to 125 MHz) for the SerDes PLLs.
- A 156.25 MHz crystal oscillator for the 10 Gbit interface. The corresponding PLL (SerDes 1 PLL2) can be switched. (DIP switch S8-4 or port expander (SD1_REF_CLK2_SEL)).
- A 25 MHz crystal on a clock generator (internal via PLL to 100 MHz) for all PCIe interfaces.

The following Figure shows the clocks required by MBLS10xxA and TQMLS10xxA, and how they are generated.

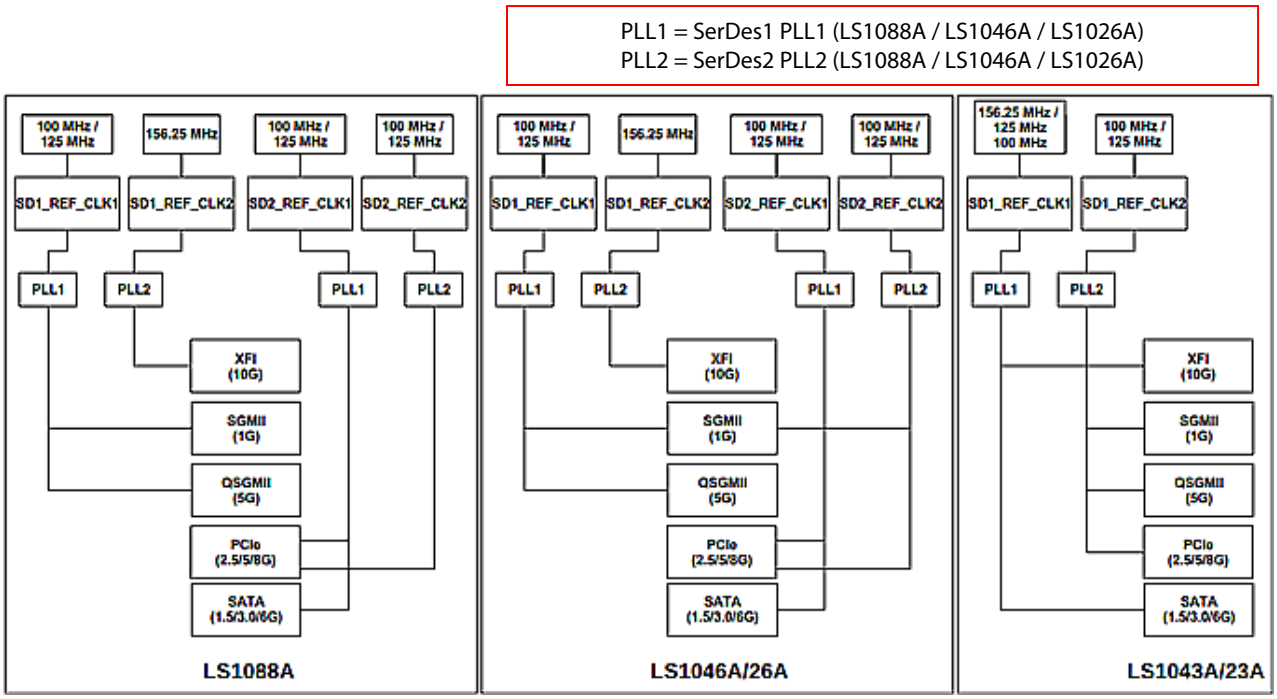

Figure 5: Block diagram clock architecture on TQMLS10xxA

Note: Spread spectrum	
	Spectrum Spreading is only permitted for PCIe. Once this function is activated on the clock generator, the lanes that use other protocols but are supplied by the same PLL cannot be used.

4.1.2 Clock generation (continued)

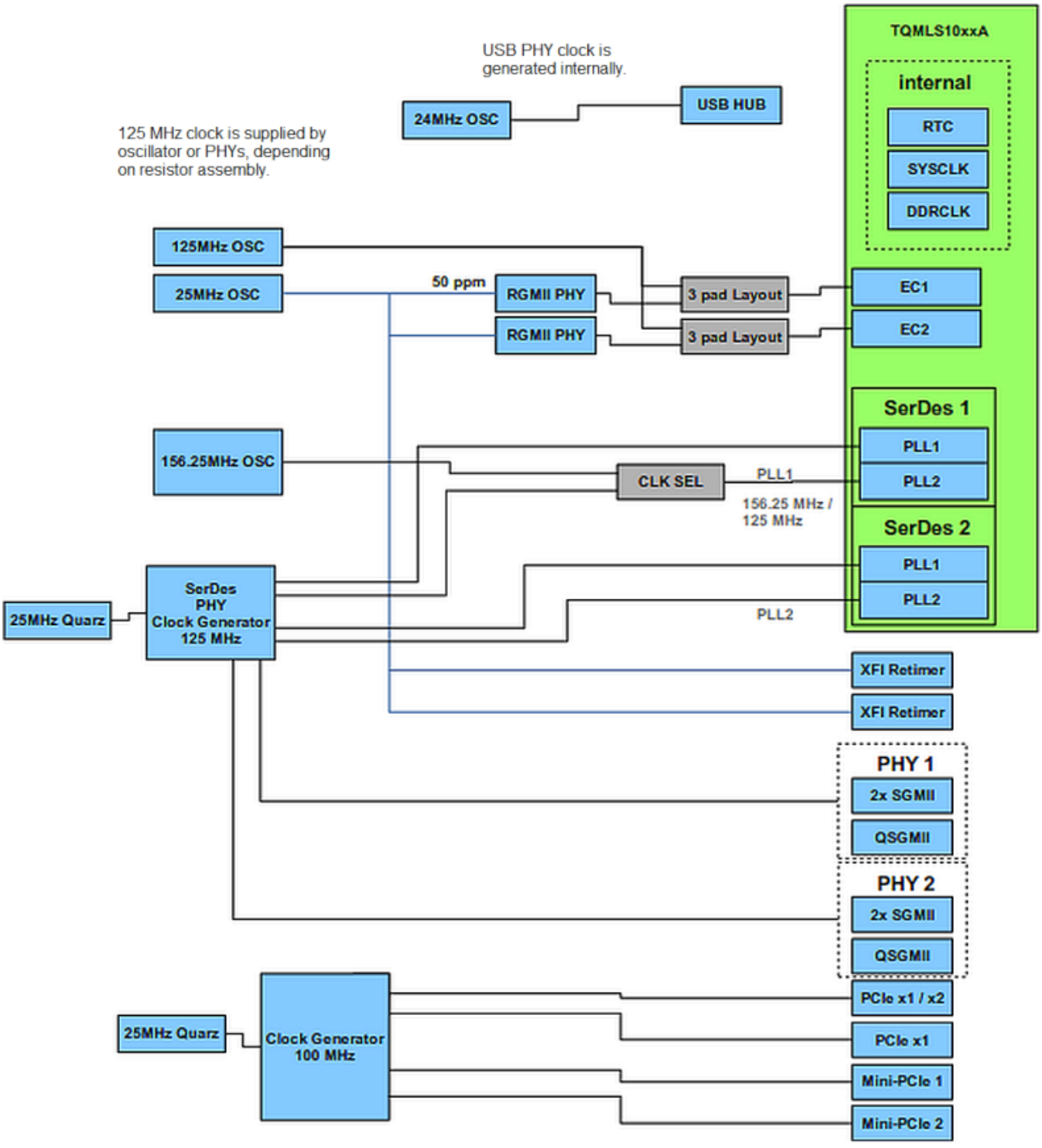

Figure 6: Block diagram clock generation on MBLS10xxA

4.1.3 SerDes clock multiplexing

High-speed multiplexers are used to support the widest possible range of SerDes interfaces of the TQMLS10xxA CPU derivatives. Optionally, the SerDes 1 Lane D (SD1_0) can be connected via T-pads, since the 10Gbit interface is used here.

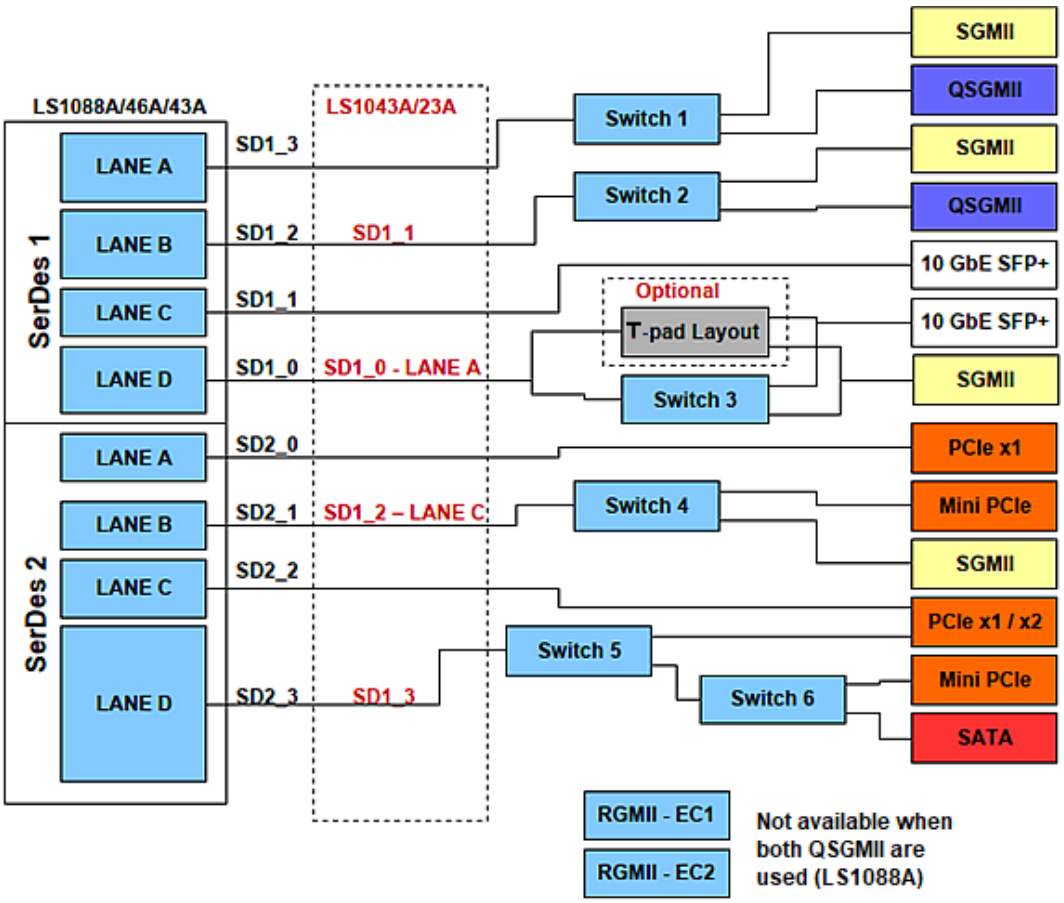

Figure 7: Block diagram SerDes clock assignment on MBLS10xxA

Table 10: SerDes multiplexing – available interfaces

Interface	LS1043A/23A		LS1046A/26A		LS1088A	
RGMII	2 MAC3 MAC4	2 MAC3 MAC4	2 MAC3 MAC4	2 MAC3 MAC4	2 MAC4 MAC5	–
SGMII	2 MAC2 MAC9	–	2 MAC5 MAC6	1 MAC2	2 MAC3 MAC7	–
QSGMII	–	1 MAC1 MAC2 MAC5 MAC6	–	1 MAC1 MAC5 MAC6 MAC10	–	2 MAC3 MAC4 MAC5 MAC6 MAC7 MAC8 MAC9 MAC10
XFI	–	1 MAC9	2 MAC9 MAC10	1 MAC9	2 MAC1 MAC2	2 MAC1 MAC2
SRDS_PRTCL_S1	0x3358	0x1455	0x1133	0x1040	0x1133	0x1144
SRDS_PRTCL_S2	–	–	0x5577	0x5A59	0x5577	0x5559

4.1.4 I²C devices

IIC4 of the TQMLS10xxA is used on the MBLS10xxA, all other IIC interfaces of the TQMLS10xxA are assigned to other functions. On the MBLS10xxA, the IIC4 interface is routed to a 4-fold I²C multiplexer, which provides four interfaces I2C0 to I2C3. The I2C0 provided by the multiplexer addresses the Mini PCIe and PCIe interfaces, a USB hub and the IO expanders, while I2C1 of the multiplexer addresses the Retimer and SFP+ interfaces as well as the clock generators.

The following block diagram shows the I²C bus structure.

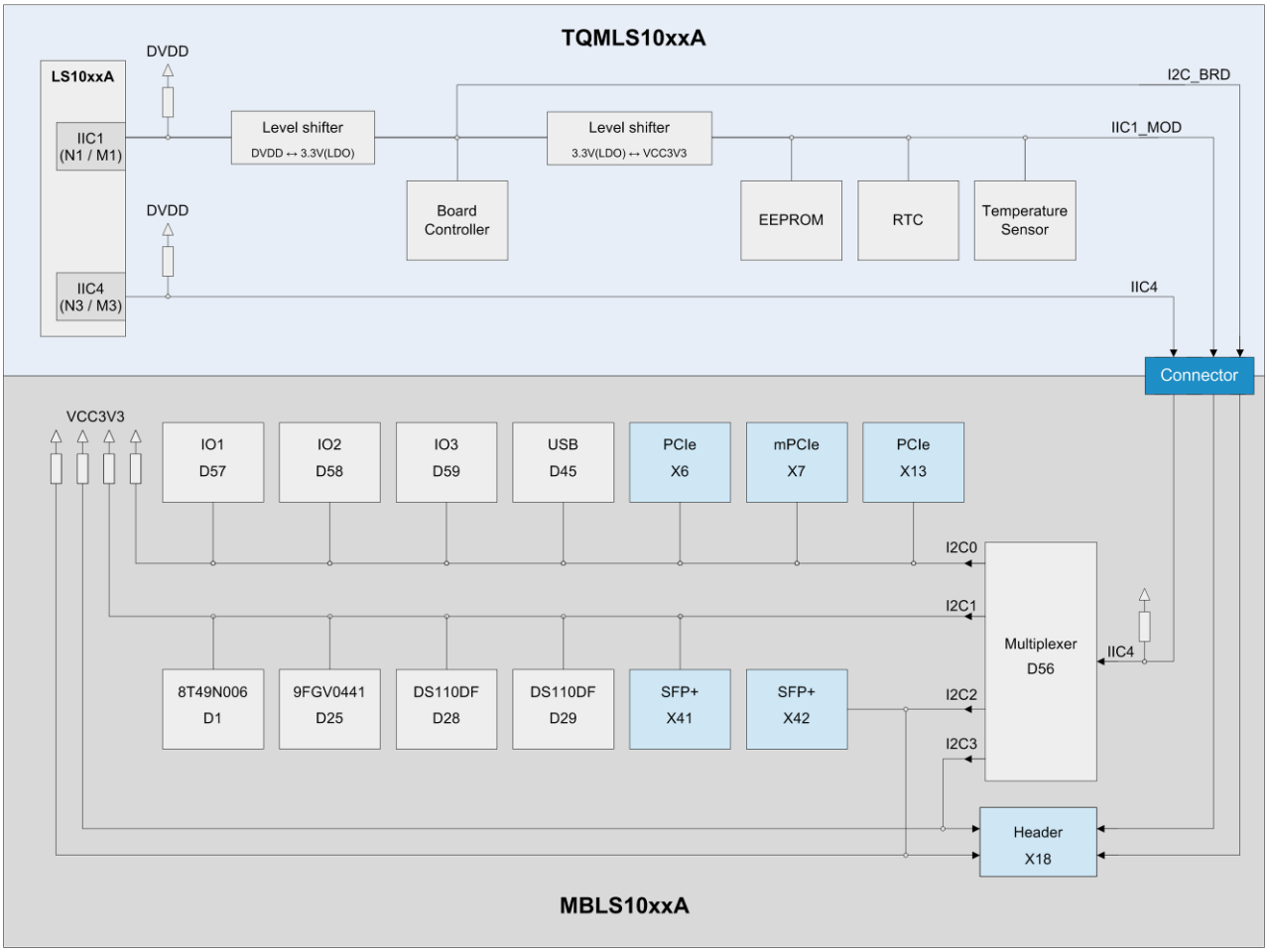

Figure 8: Block diagram I²C bus

4.1.4 I2C devices (continued)

On the TQMLS10xxA further I²C devices are connected, therefore the already assigned I²C addresses were taken into account. The following table shows the I²C address mapping on TQMLS10xxA and MBLS10xxA.

Table 11: I²C devices, address mapping on TQMLS10xxA and MBLS10xxA

Location	I²C bus	Device	Function	7-bit address	Remark
MBLS10xxA	IIC4	PCA9544ABS	Multiplexer	0x70 / 111 0000b	D56
		TUSB8041I	USB 3.0 Hub	0x44 / 100 0100b	D45, I2C0
		PCA9555PW	IIO1	0x22 / 010 0010b	D57, I2C0
		PCA9555PW	IIO2	0x20 / 010 0000b	D58, I2C0
		PCA9555PW	IIO3	0x21 / 010 0001b	D59, I2C0
		Socket	mPCIe	(Device dependent)	X6, I2C0
		Socket	mPCIe	(Device dependent)	X7, I2C0
		Slot	PCIe	(Device dependent)	X13, I2C0
		9FGV0441	Clock Generator	0x34 / 011 0100b	D25, 100 MHz, I2C1
		8T49N006A	Clock Generator	0x6E / 110 1110b	D1, 125 MHz, I2C1
		DS110DF111	Retimer 1	0x19 / 001 1001b	D28, I2C1
		SFP+ 1	10 GbE	(Device dependent)	X41, I2C1
		DS110DF111	Retimer 2	0x18 / 001 1000b	D29, I2C1
		SFP+ 2	10 GbE	(Device dependent)	X42, I2C2
TQMLS10xxA	IIC1	STM32	System Controller	0x11 / 001 0001b	Should not be altered
		SE97B	Temperature sensor	0x18 / 001 1000b	–
			EEPROM	0x50 / 101 0000b	R/W access in Normal Mode
			EEPROM	0x30 / 011 0000b	R/W access in Protected Mode
		24LC256T	EEPROM	0x57 / 101 0111b	–
		PCF85063A	RTC	0x51 / 101 0001b	–

4.1.5 GPIO port expander

Three port expanders PCA9555 with 16 ports each are provided on the MBLS10xxA to control components like LEDs, GPIOs, status GPIOs and navigation buttons on the MBLS10xxA. The port expanders are controlled via I2C0, which is controlled by IIC4.

The I²C addresses of the port expanders can be changed by reassembling resistors. When the address is altered, care must be taken to avoid address conflicts with existing I²C devices. The assembly options are documented in the MBLS10xxA schematics.

After power-up, all ports are set as input and the connected component is thus deactivated.

The following table shows the signals controlled by the port expanders.

Table 12: Function of Port Expanders

Device	Port	Signal	Dir.	Default	Remark	
D57, I²C address 0x22 / 010 0010b	IO0_0	EC1_PHY_PWDN#/INT#	I/O	High	Ethernet1-PHY-PWDN / INT	
	IO0_1	EC2_PHY_PWDN#/INT#	I/O	High	Ethernet2-PHY-PWDN / INT	
	IO0_2	USB_C_PWRON	O	Low	USB Type-C power on / off	
	IO0_3	USB_EN_OC_3V3#	I	High	USB Type-C FAULT# (overcurrent)	
	IO0_4	USB_H_GRST#	O	High	USB hub reset	
	IO0_5	GPIO_BUTTON0	I	High	Input for navigation button S3	
	IO0_6	GPIO_BUTTON1	I	High	Input for navigation button S4	
	IO0_7	SDA_PWR_EN	O	Low	OpenSDA Power Enable	
	IO1_0	QSGMII_PHY1_INT#	I	High	QSGMII interrupt	
	IO1_1	QSGMII_PHY2_INT#	I	High	QSGMII interrupt	
	IO1_2	SPI_CLKO_SOF	I	–	Clock output / start of frame (SPI / CAN)	
	IO1_3	SPI_INT#	I	High	SPI interrupt (CAN)	
	IO1_4	CAN_SEL	O	High	CAN select (CPLD / SPI)	
	IO1_5	LED	O	High	LED Green On / Off	
	IO1_6	PCIE_RST_3V3#	O	High	Reset for PCIe	
	IO1_7	PCIE_WAKE_3V3#	O	High	Wake-Up for PCIe	
D58, I²C address 0x20 / 010 0000b	IO0_0	SD1_0_LANE_A_MUX	I/O	High	ON: SGMII PHY1	OFF: QSGMII PHY1
	IO0_1	SD1_1_LANE_B_MUX	I/O	High	ON: SGMII PHY2	OFF: QSGMII PHY2
	IO0_2	SD1_3_LANE_D_MUX	I/O	High	ON: SGMII PHY2	OFF: XFI2
	IO0_3	SD2_1_LANE_B_MUX	I/O	High	ON: mPCIe slot 2	OFF: SGMII PHY1
	IO0_4	SD2_3_LANE_D_MUX1	I/O	High	ON: mPCIe slot 2	OFF: Mux for mPCIe / SATA
	IO0_5	SD2_3_LANE_D_MUX2	I/O	High	ON: SATA	OFF: mPCIe Slot 1
	IO0_6	SD_MUX_SHDN	I/O	High	ON: Demuxing off	OFF: Demuxing on
	IO0_7	SD1_REF_CLK2_SEL	I/O	High	ON: 156.25 MHz	OFF: 125 MHz
	IO1_0	MPCIE1_DISABLE#	O	Low	mPCIe1 Disable	
	IO1_1	MPCIE1_WAKE#	O	High	mPCIe1 wake	
	IO1_2	MPCIE2_DISABLE#	O	Low	mPCIe2 Disable	
	IO1_3	MPCIE2_WAKE#	O	High	mPCIe2 wake	
	IO1_4	PRSNT2#	O	High	PCIe Hot Plug Detect	
	IO1_5	PCIE_PWR_EN	O	High	Switch supply for PCIe on/off	
	IO1_6	DCDC_PWR_EN	O	High	Switch supply for all switching regulators on/off (except 5 V / 3.3 V)	
	IO1_7	DCDC_PGOOD_1V8	I	High	Feedback from 1.8 V switching regulator	
D59, I²C address 0x21 / 010 0001b	IO0_0	XFI1_TX_FAULT	I	High	SFP+ signal	
	IO0_1	XFI1_TX_DIS	O	High	SFP+ signal	
	IO0_2	XFI1_MODDEF_DET	I	High	SFP+ signal	
	IO0_3	XFI1_RX_LOSS	I	High	SFP+ signal	
	IO0_4	RETIMER1_LOSS#	I	High	Retimer-Loss-Signal	
	IO0_5	XFI1_ENSMB#	O	Low	Retimer Enable SM-Bus	
	IO0_6	QSGMII1_CLK_SEL0	I/O	High	ON = 156.25 MHz	OFF = 125 MHz
	IO0_7	QSGMII_PHY1_CONFIG3	I/O	High	ON = QSGMII	OFF = SGMII
	IO1_0	XFI2_TX_FAULT	I	High	SFP+ signal	
	IO1_1	XFI2_TX_DIS	O	High	SFP+ signal	
	IO1_2	XFI2_MODDEF_DET	I	High	SFP+ signal	
	IO1_3	XFI2_RX_LOSS	I	High	SFP+ signal	
	IO1_4	RETIMER2_LOSS#	I	High	Retimer-Loss-Signal	
	IO1_5	XFI2_ENSMB#	O	Low	Retimer Enable SM-Bus	
	IO1_6	QSGMII2_CLK_SEL0	I/O	High	ON = 156.25 MHz	OFF = 125 MHz
	IO1_7	QSGMII_PHY2_CONFIG3	I/O	High	ON = QSGMII	OFF = SGMII

4.1.6 Power management and Reset

The MBLS10xxA provides different ways for a complete or partial reset of the TQMLS10xxA.
The following table shows the signals used.

Table 13: Reset signals

Signal	Source	Dir.	Default	Remark
RESIN#	TQMLS10xxA	I	High	Global reset from external for the TQMLS10xxA
RESET_OUT#	TQMLS10xxA	O	High	Global reset from module for MBLS10xxA
MB_RST#	Reset-Chain	O	High	Reset for QSGMII and PCIe
JTAG_RST#	JTAG	O	High	Reset by debugger
PHY_RST_2V5#	Reset-Chain	O	High	Reset via JTAG® chain for PHYs
TRST_2V5#	JTAG	O	High	JTAG® reset for PHYs
POWER_GOOD	TQMLS10xxA	I	High	Power-Good-State from TQMLS10xxA
DCDC_PWR_EN	Reset-Chain (Port-Expander)	O	High	Switches VCC_DCDC_EN
VCC_EN	Reset-Chain	O	High	Switches VCC5V_SOURCE and VCC3V3_SOURCE to POWER_GOOD
PCIE_PWR_EN	Reset-Chain (Port-Expander)	O	High	Switches VCC_PCIE_EN
VCC_DCDC_EN	Reset-Chain / Enable -Chain	O	High	Switches the switching regulators
VCC_PCIE_EN	Reset-Chain / Enable -Chain	O	High	Switches the PCIe switching regulators

4.1.7 Power supply

The MBLS10xxA has to be supplied with 18 V to 28 V at X14 or X36. The typical supply voltage is 24 V.

On the MBLS10xxA, 1.0 V, 1.1 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V and 12 V are generated from this. These voltages are used to supply the components on the MBLS10xxA.

In addition, 3.3 V, 5 V and 12 V are available at the three headers (X17, X18 and X19) on the MBLS10xxA. The three connectors share the available total power of the individual voltage levels.

The Mini PCIe connectors are supplied with 1.5 V and 3.3 V. The 1.5 V are generated from 3.3 V and are only present on the Mini PCIe connector. The PCIe connector is supplied with 3.3 V and 12 V, the M.2 connector with 3.3 V, the SFP+ connectors with 3.3 V, the SATA connector with 3.3 V, 5 V and 12 V.

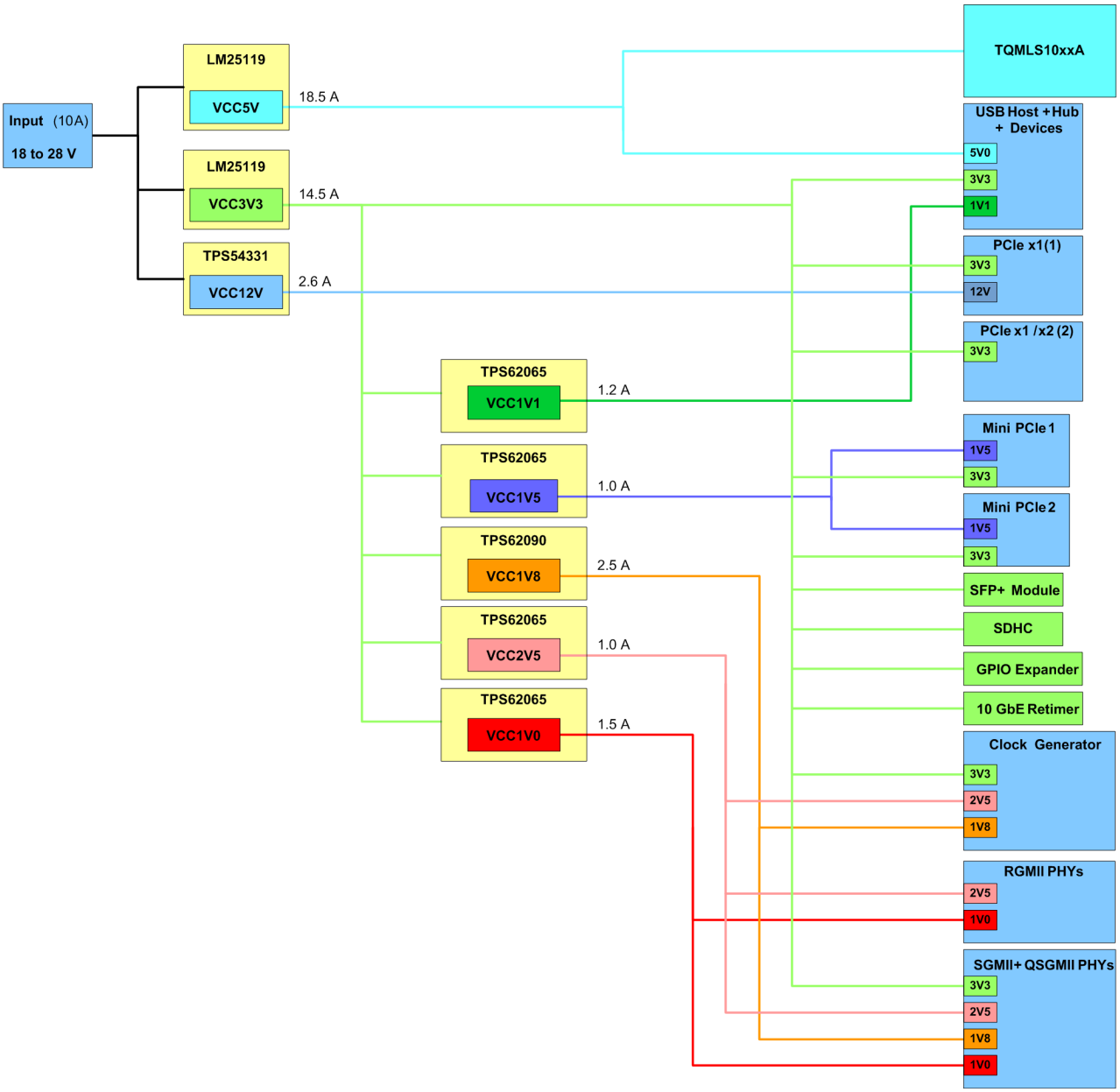

Figure 9: Block diagram power supply

4.1.7 Power supply (continued)

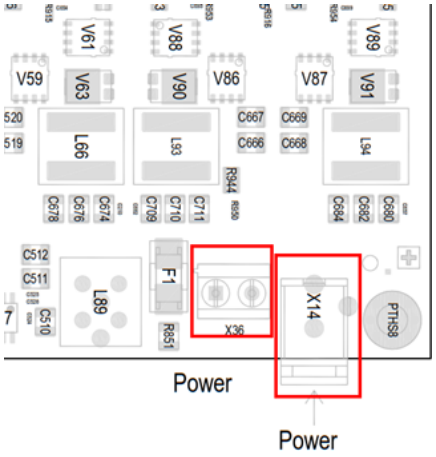

Figure 10: Connectors X14 / X36

Attention: Malfunction caused by cross supply	
	To avoid cross-supply and resulting errors in the power up/down sequence of the TQMLS10xxA, the reset configuration to switch the switching regulators on or off must be taken into account. A circuit proposal can be taken from the MBLS10xxA schematics.

Voltages DVDD and EVDD can be set to 1.8 V or 3.3 V with DIP switch S10.

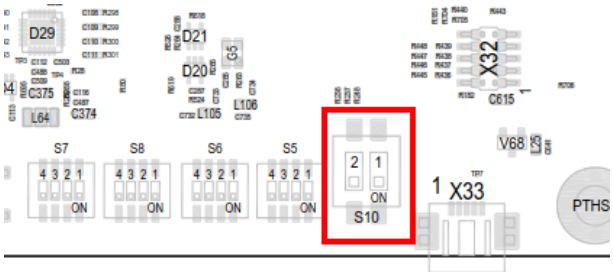

Figure 11: Position of DIP switch S10

Table 14: DVDD / EVDD voltage selection, DIP switch S10

DIP switch S10	ON	OFF
S10-1 (1~2)	DVDD = 3.3 V	DVDD = 1.8 V
S10-2 (3~4)	EVDD = 3.3 V	EVDD = 1.8 V

4.1.7.1 Protective circuitry

The protection circuit (see Figure 12) features the following characteristics:

- Overcurrent protection by fuse 10 A, Fast Blow
- Overvoltage protection
- PI filter
- Reverse polarity protection
- Capacitors for voltage smoothing

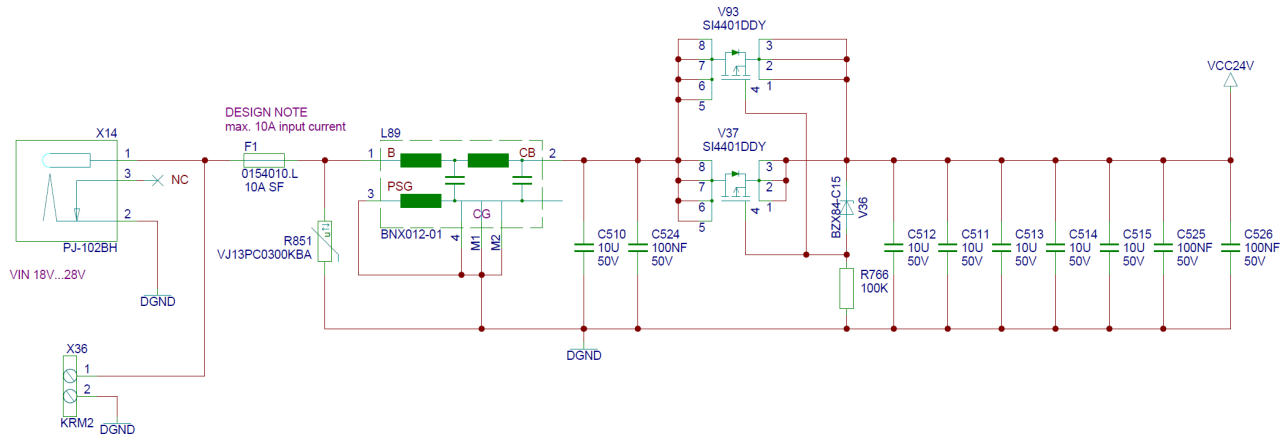

Figure 12: MBLS10xxA protective circuit

The carrier board including module consumes approx. 140 W under full load when all supply voltages are loaded with maximum current, e.g. by external loads on the pin headers. The power supply for the carrier board must be dimensioned accordingly. In most applications, however, the power consumption will be significantly lower. The sole operation of the carrier board including the module consumes approx. 8.5 watts when the processor is fully loaded.

4.1.7.2 Voltage monitoring

The supply voltages on the MBLS10xxA are monitored by comparators and a reference voltage. If the voltage falls below a defined threshold, this is signalled by a LED. If the VCC5V_SOURCE falls below a defined threshold, a global reset is triggered (BUTTON_RST#) and this is indicated simultaneously by a LED. The status of the respective voltage is indicated by a status LED.

Table 15: Voltage supervision

Voltage	Permitted voltage range [V]	DC/DC [V]	Threshold [V]	Set threshold [V]
12.0 V	11.4 ~ 12.6	11.64 ~ 12.36	11.6	11.41 ~ 11.87
5.0 V	4.45 ~ 5.25	4.90 ~ 5.10	4.8	4.73 ~ 4.82
3.3 V	3.14 ~ 3.47	3.20 ~ 3.40	3.15	3.13 ~ 3.20
2.5 V	2.38 ~ 2.63	2.45 ~ 2.55	2.40	2.38 ~ 2.43
1.8 V	1.70 ~ 1.90	1.764 ~ 1.836	1.74	1.71 ~1.74
1.5 V	1.425 ~ 1.575	1.470 ~ 1.530	1.45	1.43 ~ 1.46
1.1 V	1.045 ~ 1.155	1.078 ~ 1.122	1.06	1.04 ~ 1.08
1.0 V	0.95 ~ 1.05	0.98 ~ 1.02	0.96	0.94 ~ 0.98

4.1.8 Battery

In case of power failure or power down a lithium battery type CR2032 on the MBLS10xxA supplies the RTC on the TQMLS10xxA via pin VBAT (X1-37), which can be supplied with 2.1 V to 3.7 V, typical 3.0 V.

4.2 Communication interfaces

4.2.1 Ethernet 1000 Base-T (RGMII)

Both Ethernet MACs of the TQMLS10xxA are connected to the MBLS10xxA via a TI PHY DP83867 each. Depending on the RCW the Ethernet MACs can be used or not. Further information can be taken from the Ls10xxA data sheet. Both RGMII interfaces have own interrupt signals and a global reset.

The PHY DP83867 provides boot straps to start with configurable default values. All boot straps can be customized on the MBLS10xxA by assembly options. Further information can be found in the MBLS10xxA schematics.

The achievable data throughput is influenced by the system load and the software platform used.

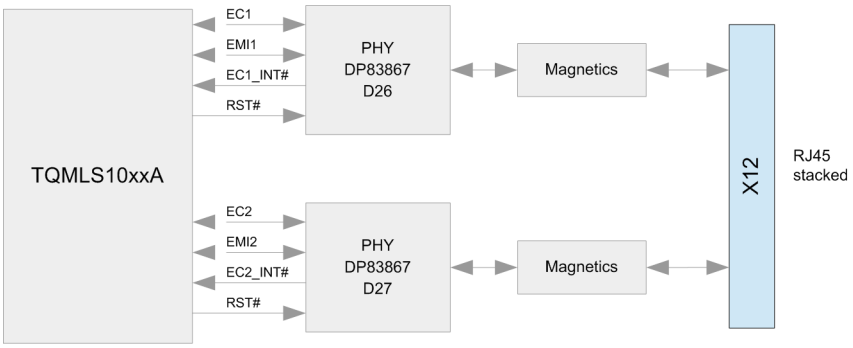

Figure 13: Block diagram Ethernet 1000 Base-T

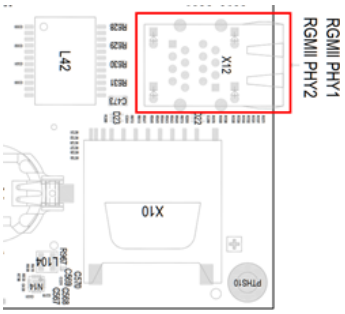

Figure 14: Position Ethernet 1 & 2, X12

Table 16: Pinout RJ-45 Ethernet connector, X12

Pin	Pin name	Signal
1	1A	EC1_A_P
2	2A	EC1_A_M
3	3A	EC1_B_P
6	6A	EC1_B_M
4	4A	EC1_C_P
5	5A	EC1_C_M
7	7A	EC1_D_P
8	8A	EC1_D_M
1	1B	EC2_A_P
2	2B	EC2_A_M
3	3B	EC2_B_P
6	6B	EC2_B_M
4	4B	EC2_C_P
5	5B	EC2_C_M
7	7B	EC2_D_P
8	8B	EC2_D_M

4.2.2 SGMII / QSGMII

Depending on the CPU derivative and the RCW, different configurations are available on the SerDes interface. Refer to the CPU data sheet for more information.

Two Marvell PHYs 88E1340S are available, which can be configured for SGMII or QSGMII. Both PHYs have their own interrupt signals and a global reset.

The PHY 88E1340S provides boot straps to start with configurable default values. All boot straps can be customized on the MBLS10xxA by using assembly options. Further information is available in the MBLS10xxA schematics.

The achievable data throughput is influenced by the system load and the software platform used.

The following tables show the pinout of the quad Ethernet jacks.

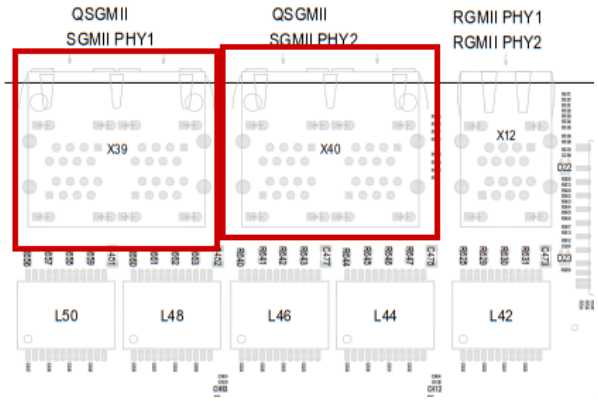

Figure 15: Position SGMII / QSGMII Ethernet 1 & 2, RJ45, X39, X40

4.2.2 SGMII / QSGMII (continued)

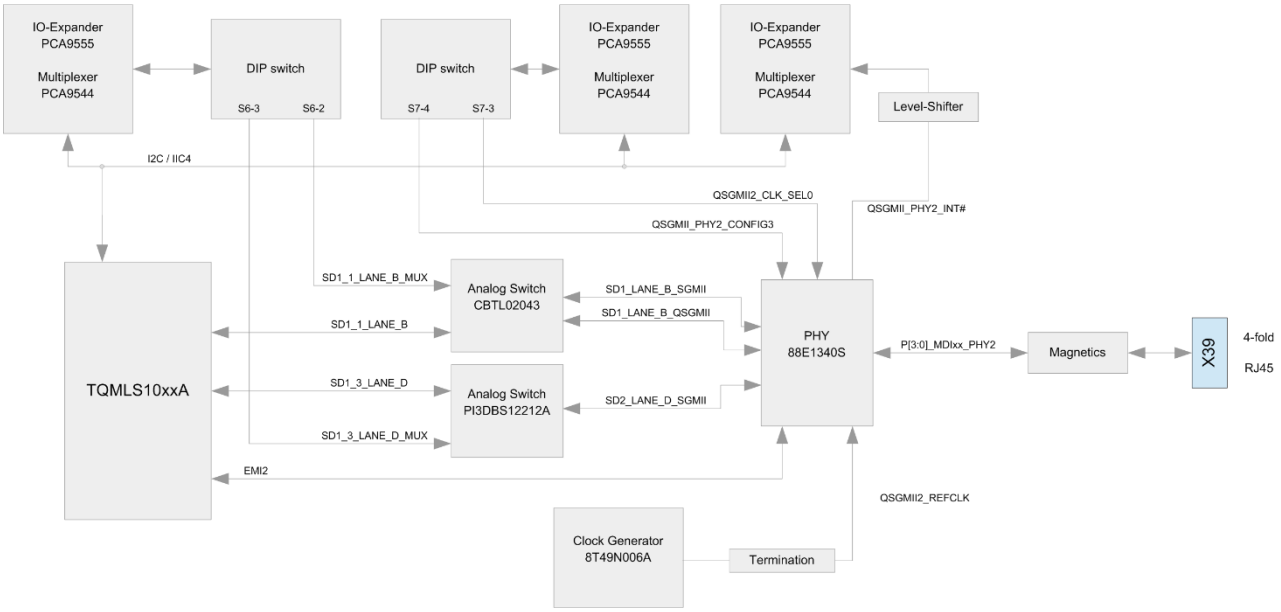

Figure 16: Block diagram QSGMII PHY 1

Table 17: Pinout RJ-45 Ethernet connector, X39

Pin	Pin name	Signal	Connector
1	1AA	P0_MDIP0_PHY2	X39 bottom left
2	2AA	P0_MDIN0_PHY2	
3	3AA	P0_MDIP1_PHY2	
6	6AA	P0_MDIN1_PHY2	
4	4AA	P0_MDIP2_PHY2	
5	5AA	P0_MDIN2_PHY2	
7	7AA	P0_MDIP3_PHY2	
8	8AA	P0_MDIN3_PHY2	
1	1BA	P1_MDIP0_PHY2	X39 top left
2	2BA	P1_MDIN0_PHY2	
3	3BA	P1_MDIP1_PHY2	
6	6BA	P1_MDIN1_PHY2	
4	4BA	P1_MDIP2_PHY2	
5	5BA	P1_MDIN2_PHY2	
7	7BA	P1_MDIP3_PHY2	
8	8BA	P1_MDIN3_PHY2	
1	1AB	P2_MDIP0_PHY2	X39 bottom right
2	2AB	P2_MDIN0_PHY2	
3	3AB	P2_MDIP1_PHY2	
6	6AB	P2_MDIN1_PHY2	
4	4AB	P2_MDIP2_PHY2	
5	5AB	P2_MDIN2_PHY2	
7	7AB	P2_MDIP3_PHY2	
8	8AB	P2_MDIN3_PHY2	
1	1BB	P3_MDIP0_PHY2	X39 top right
2	2BB	P3_MDIN0_PHY2	
3	3BB	P3_MDIP1_PHY2	
6	6BB	P3_MDIN1_PHY2	
4	4BB	P3_MDIP2_PHY2	
5	5BB	P3_MDIN2_PHY2	
7	7BB	P3_MDIP3_PHY2	
8	8BB	P3_MDIN3_PHY2	

4.2.2 SGMII / QSGMII (continued)

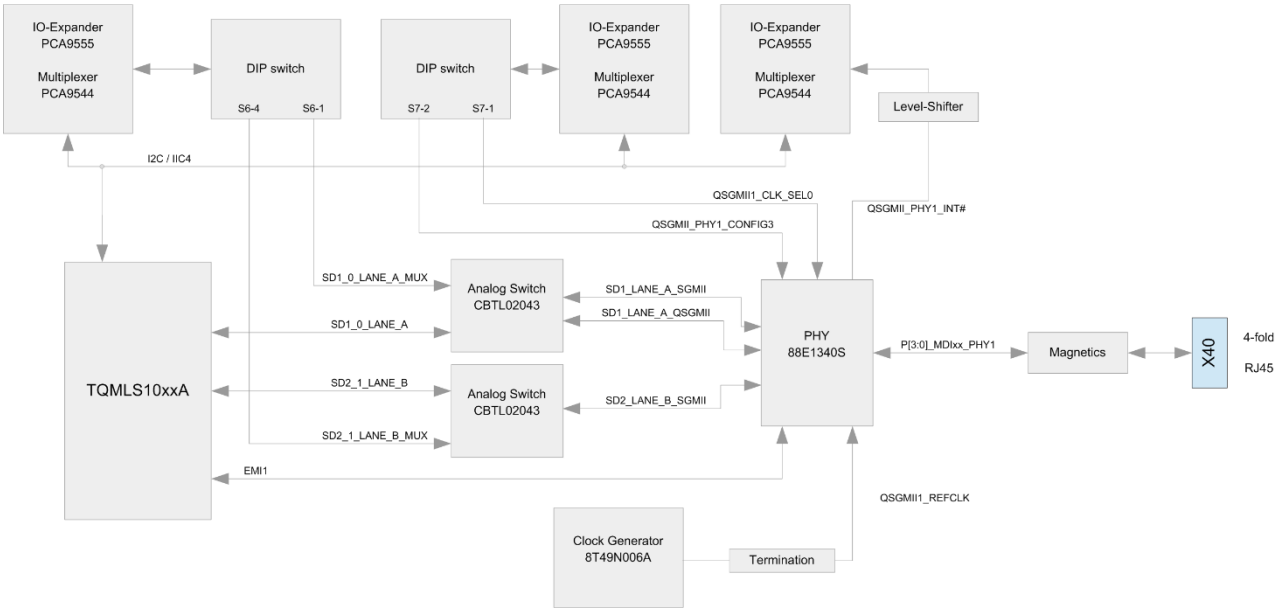

Figure 17: Block diagram QSGMII PHY 2

Table 18: Pinout RJ-45 Ethernet connector, X40

Pin	Pin name	Signal	Connector
1	1AA	P0_MDIP0_PHY1	X40 bottom left
2	2AA	P0_MDIN0_PHY1	
3	3AA	P0_MDIP1_PHY1	
6	6AA	P0_MDIN1_PHY1	
4	4AA	P0_MDIP2_PHY1	
5	5AA	P0_MDIN2_PHY1	
7	7AA	P0_MDIP3_PHY1	
8	8AA	P0_MDIN3_PHY1	
1	1BA	P1_MDIP0_PHY1	X40 top left
2	2BA	P1_MDIN0_PHY1	
3	3BA	P1_MDIP1_PHY1	
6	6BA	P1_MDIN1_PHY1	
4	4BA	P1_MDIP2_PHY1	
5	5BA	P1_MDIN2_PHY1	
7	7BA	P1_MDIP3_PHY1	
8	8BA	P1_MDIN3_PHY1	
1	1AB	P2_MDIP0_PHY1	X40 bottom right
2	2AB	P2_MDIN0_PHY1	
3	3AB	P2_MDIP1_PHY1	
6	6AB	P2_MDIN1_PHY1	
4	4AB	P2_MDIP2_PHY1	
5	5AB	P2_MDIN2_PHY1	
7	7AB	P2_MDIP3_PHY1	
8	8AB	P2_MDIN3_PHY1	
1	1BB	P3_MDIP0_PHY1	X40 top right
2	2BB	P3_MDIN0_PHY1	
3	3BB	P3_MDIP1_PHY1	
6	6BB	P3_MDIN1_PHY1	
4	4BB	P3_MDIP2_PHY1	
5	5BB	P3_MDIN2_PHY1	
7	7BB	P3_MDIP3_PHY1	
8	8BB	P3_MDIN3_PHY1	

4.2.3 10 GbE (XFI / SFP+)

Depending on the CPU derivative and the RCW, two 10GbE interfaces (SFP+) are available to the user. For further information please refer to the CPU data sheet. Both DS110DF111 Retimers have their own interrupt signals and a global reset. The SFP+ signals are connected to an IO expander to evaluate the SFP+ interface. The Retimer provides boot straps to start with configurable default values. All boot straps can be customized on the MBLS10xxA by assembly options or via I²C. Further information is available in the MBLS10xxA schematics. The achievable data throughput is influenced by the system load and the software platform used. The following tables show the pinout of the SFP+ connectors.

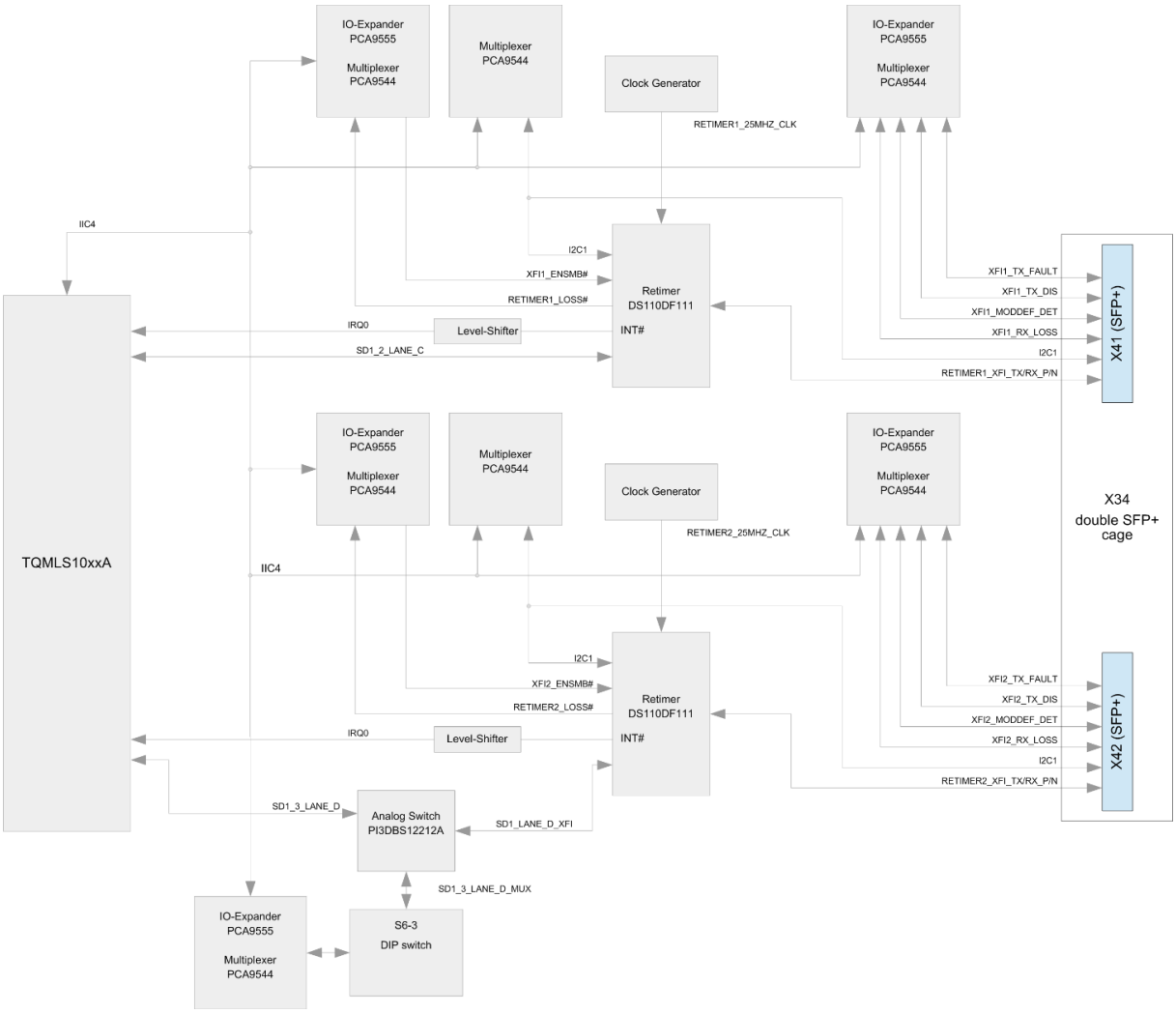

Figure 18: Block diagram 10 GbE

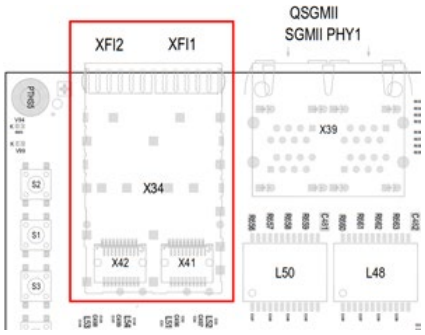

Figure 19: Position XFI1+XFI2, X41+X42

4.2.3 10 GbE (XFI / SFP+) (continued)

Table 19: Pinout XFI1, X41 and XFI2, X42

Pin	Pin name	Signal X41	Signal X42	Dir.	Remark
1	TGND	DGND	DGND	P	–
2	TX_FAULT	XFI1_TX_FAULT	XFI2_TX_FAULT	I	10 kΩ Pull-Up to VCC3V3
3	TX_DIS	XFI1_TX_DIS	XFI2_TX_DIS	O	10 kΩ Pull-Up to VCC3V3
4	I2C_SDA	I2C1_SDA	I2C1_SDA	I/O	–
5	I2C_SCL	I2C1_SCl	I2C1_SCl	O	–
6	MODDEF_DET	XFI1_MODDEF_DET	XFI2_MODDEF_DET	I	10 kΩ Pull-Up to VCC3V3
7	RS0	–	–	I	10 kΩ Pull-Up to VCC3V3
8	RXLOSS	XFI1_RX_LOSS	XFI2_RX_LOSS	I	10 kΩ Pull-Up to VCC3V3
9	RS1	–	–	I	10 kΩ Pull-Up to VCC3V3
10	RGND	DGND	DGND	P	–
11	RGND	DGND	DGND	P	–
12	RX_DAT–	RETIMER1_XFI_RX_N (XFI1_BYPASS_RX_N)	RETIMER2_XFI_RX_N (XFI2_BYPASS_RX_N)	I	Placement option for Bypass (Retimer)
13	RX_DAT+	RETIMER1_XFI_RX_P (XFI1_BYPASS_RX_P)	RETIMER2_XFI_RX_P (XFI2_BYPASS_RX_P)	I	Placement option for Bypass (Retimer)
14	RGND	DGND	DGND	P	–
15	VDDR	VCC3V3	VCC3V3	P	–
16	VDDT	VCC3V3	VCC3V3	P	–
17	TGND	DGND	DGND	P	–
18	TX_DAT+	RETIMER1_XFI_TX_P (XFI1_BYPASS_TX_P)	RETIMER2_XFI_TX_P (XFI2_BYPASS_TX_P)	O	Placement option for Bypass (Retimer)
19	TX_DAT–	RETIMER1_XFI_TX_N (XFI1_BYPASS_TX_N)	RETIMER2_XFI_TX_N (XFI2_BYPASS_TX_N)	O	Placement option for Bypass (Retimer)
20	TGND	DGND	DGND	P	–

4.2.4 USB 3.0 Hub

The TQMLS10xxA provides a USB3.0 interface via a USB3.0 controller with integrated PHY. A USB hub TUSB8041I is connected to this USB3.0 interface on the MBLS10xxA, which provides four USB 3.0 / 2.0 host interfaces. The USB connectors are supplied with 5 V via power distribution switches. The current is monitored and can be switched off in case of an overload and/or overheating.

USB Host 1 and 2 are connected to a Dual USB 3.0 Type A socket (X15). USB host 3 (USB2.0) can be used at pin header X19 and USB host 4 (USB2.0) at Mini PCIe connector X6.

The USB hub used is programmed via bootstrapping or I²C. Further information can be found in the TUSB8041I data sheet and the MBLS10xxA schematics.

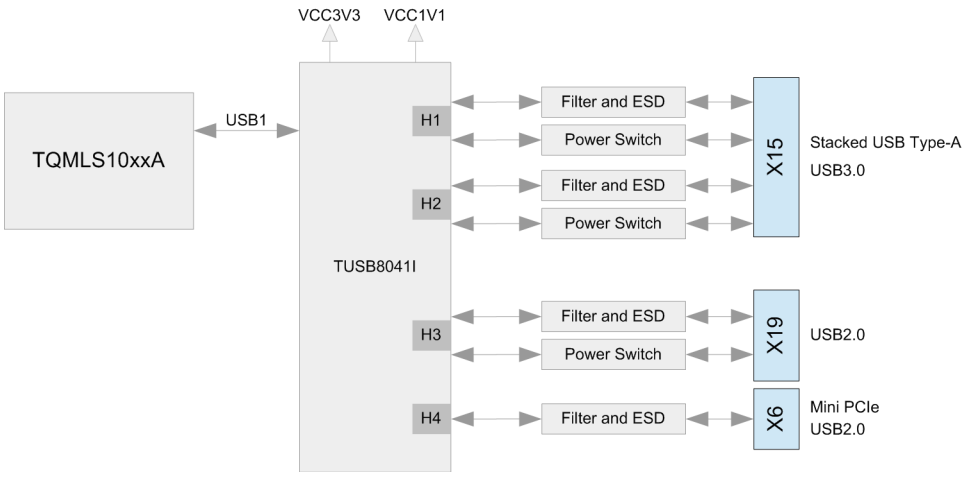

Figure 20: Block diagram USB Hosts

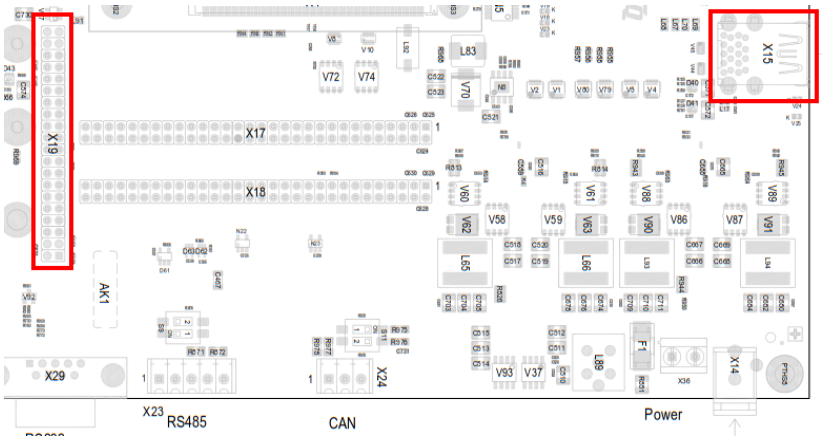

Figure 21: Position USB Host, X15, X19

Figure 22: Position USB Host, X6

4.2.4 USB 3.0 Hub (continued)

The USB host port of the TQMLS10xxA provides a theoretical data rate of 5 Gbit/s. This is divided among the connected ports. Depending on the software and hardware used, the effective read and write rates of the ports may vary.
The following table shows the pinout of stacked USB connector X15.

Table 20: Pinout USB Host1&2, Stacked Type-A, X15

Pin	Pin name	Signal	Remark	Position
1	VBUS_2	USB_H2_VBUS	100 µF + EMI filter	Bottom
2	D–_2	USB2_H2_D_N	Common Mode Choke in series	
3	D+_2	USB2_H2_D_P	Common Mode Choke in series	
4	GND_2	DGND	–	
5	SSRX–_2	USB3_H2_RX_D_N	Common Mode Choke in series	
6	SSRX+_2	USB3_H2_RX_D_P	Common Mode Choke in series	
7	GND-DRAIN_2	DGND	–	
8	SSTX–_2	USB3_H2_TX_D_N	Common Mode Choke + 100 nF in series	
9	SSTX+_2	USB3_H2_TX_D_P	Common Mode Choke + 100 nF in series	
10	VBUS_1	USB_H1_VBUS	100 µF + EMI filter	Top
11	D–_1	USB2_H1_D_N	Common Mode Choke in series	
12	D+_1	USB2_H1_D_P	Common Mode Choke in series	
13	GND_1	DGND	–	
14	SSRX–_1	USB3_H1_RX_D_N	Common Mode Choke in series	
15	SSRX+_1	USB3_H1_RX_D_P	Common Mode Choke in series	
16	GND-DRAIN_1	DGND	–	
17	SSTX–_1	USB3_H1_TX_D_N	Common Mode Choke + 100 nF in series	
18	SSTX+_1	USB3_H1_TX_D_P	Common Mode Choke + 100 nF in series	
M1 ~ M4	Shield	DGND	–	

Table 21: Pinout USB Host4, 40-pin header, X19

Pin	Pin name	Signal	Remark
30	DGND	DGND	–
36	VBUS	USB_H3_VBUS	100 µF + EMI filter
38	D–	USB2_H3_D_N	Common Mode Choke in series
39	DGND	DGND	–
40	D+	USB2_H3_D_P	Common Mode Choke in series

Table 22: Pinout USB Host3, mPCIe connector, X6

Pin	Pin name	Signal	Remark
36	D–	USB2_H4_D_N	Common Mode Choke in series
38	D+	USB2_H4_D_P	Common Mode Choke in series

Table 23: USB Host power supply

Parameter	Min	Typical	Max	Remark
Voltage	4.75 V	5 V	5.25 V	Ensured at max. 900 mA (per VBUS)
Current	–	500 mA	900 mA	–

4.2.5 USB 3.0 OTG and Type-C (DFP)

Depending on the CPU derivative, one or two additional USB3.0-OTG interfaces of the TQMLS10xxA are available on the MBLS10xxA. USB2 is available on all module variants at a 10-pin Micro-B connector. USB3 is only available with the CPU derivatives LS1023A/43A/26A/46A on a USB Type C connector.

Both OTG interfaces are operated in the standard BSP exclusively in host mode. An OTG or device function is not implemented in software.

The ports USB2 and USB3 of the TQMLS10xxA provide a theoretical data rate of 5000 Mbit/s. Depending on the software and hardware used, the effective read and write rates of the ports may vary.

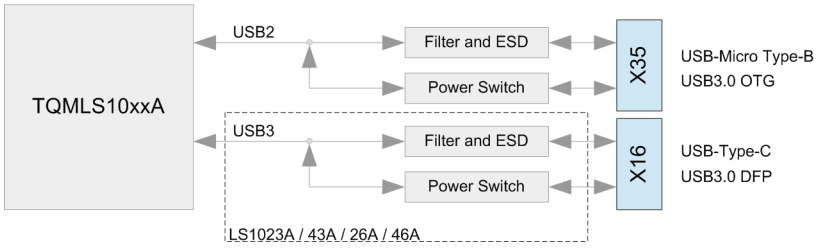

Figure 23: Block diagram USB OTG

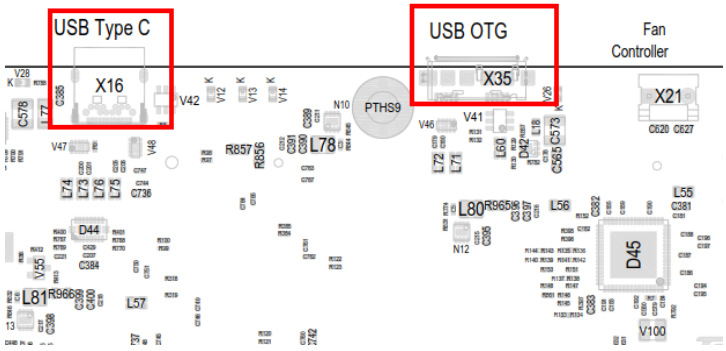

Figure 24: Position USB OTG, X16, X35

4.2.5 USB 3.0 OTG and Type-C (DFP) (continued)

The USB1 port of the TQMLS10xxA provides a theoretical data rate of 5 Gbit/s.
Depending on the software and hardware used, the effective read and write rates of the ports may vary.
The following table shows the pinout of USB OTG connector X35.

Table 24: Pinout USB2 OTG (USB Micro B), X35

Pin	Pin name	Signal	Remark
1	VBUS	USB_H1_VBUS	100 µF + EMI filter
2	D–	USB2_D_M	Common Mode Choke in series
3	D+	USB2_D_P	Common Mode Choke in series
4	ID	USB2_ID	–
5	GND	DGND	–
6	SSTX–	USB2_TX_M	Common Mode Choke + 100 nF in series
7	SSTX+	USB2_TX_P	Common Mode Choke + 100 nF in series
8	GND_DRAIN	DGND	–
9	SSRX–	USB2_RX_M	Common Mode Choke + 100 nF in series
10	SSRX+	USB2_RX_P	Common Mode Choke + 100 nF in series
M1 ~ M6	Shield	DGND	–

Table 25: Pinout USB3 DFP (Type-C), X16

Pin	Pin name	Signal	Remark
A1	GND	DGND	–
B12	GND	DGND	–
A2	SSTX1+	USB3_C0_TX3_L_P	Common Mode Choke in series
B11	SSRX1+	USB3_C1_RX3_L_P	Common Mode Choke in series
A3	SSTX1–	USB3_C0_TX3_L_N	Common Mode Choke in series
B10	SSRX1–	USB3_C1_RX3_L_N	Common Mode Choke in series
A4	VBUS	USB3_VBUS	2 × 100 µF + EMI Filter
B9	VBUS	USB3_VBUS	
A5	CC1	–	USB Power Delivery Communication
B8	SBU2	–	Floating (Optional 1 MΩ to DGND) – Secondary Bus
A6	D+	USB2_C_DP	Common Mode Choke in series
B7	D–	USB2_C_DN	Common Mode Choke in series
A7	D–	USB2_C_DN	Common Mode Choke in series
B6	D+	USB2_C_DP	Common Mode Choke in series
A8	SBU1	–	Floating (Optional 1 MΩ to DGND) – Secondary Bus
B5	CC2	–	USB Power Delivery Communication
A9	VBUS	USB3_VBUS	2 × 100 µF + EMI Filter
B4	VBUS	USB3_VBUS	
A10	SSRX2–	USB3_B1_RX3_L_N	Common Mode Choke in series
B3	SSTX2–	USB3_B0_TX3_L_N	Common Mode Choke in series
A11	SSRX2+	USB3_B1_RX3_L_P	Common Mode Choke in series
B2	SSTX2+	USB3_B0_TX3_L_P	Common Mode Choke in series
A12	GND	DGND	–
B1	GND	DGND	–
M1 ~ M4	Shield	DGND	–

4.2.6 PCIe, Mini PCIe and M.2

The PCIe interfaces are supplied with the required clock by a clock generator 9FGB0441.
On the MBLS10xxA a Mini PCIe slot, a PCIe slot, an M.2 M key slot and a Mini PCIe slot with SIM card holder are available. SIM cards, which require a 5 V supply, are not supported.
Depending on the RCW, the following interfaces are available on these CPU derivatives:

- The PCIe interface can only be used with the LS1026A, 46A and 88A, the Mini PCIe interface with SIM card holder can be used with any CPU derivative.
- The M.2 M key interface can be used with the LS1026A, 46A and 88A, depending on the multiplexing.
- The Mini PCIe interface without SIM card holder can only be used with the LS1023A and 43A, depending on the multiplexing.

The maximum load for the provided voltages is the current specified in Table 30.

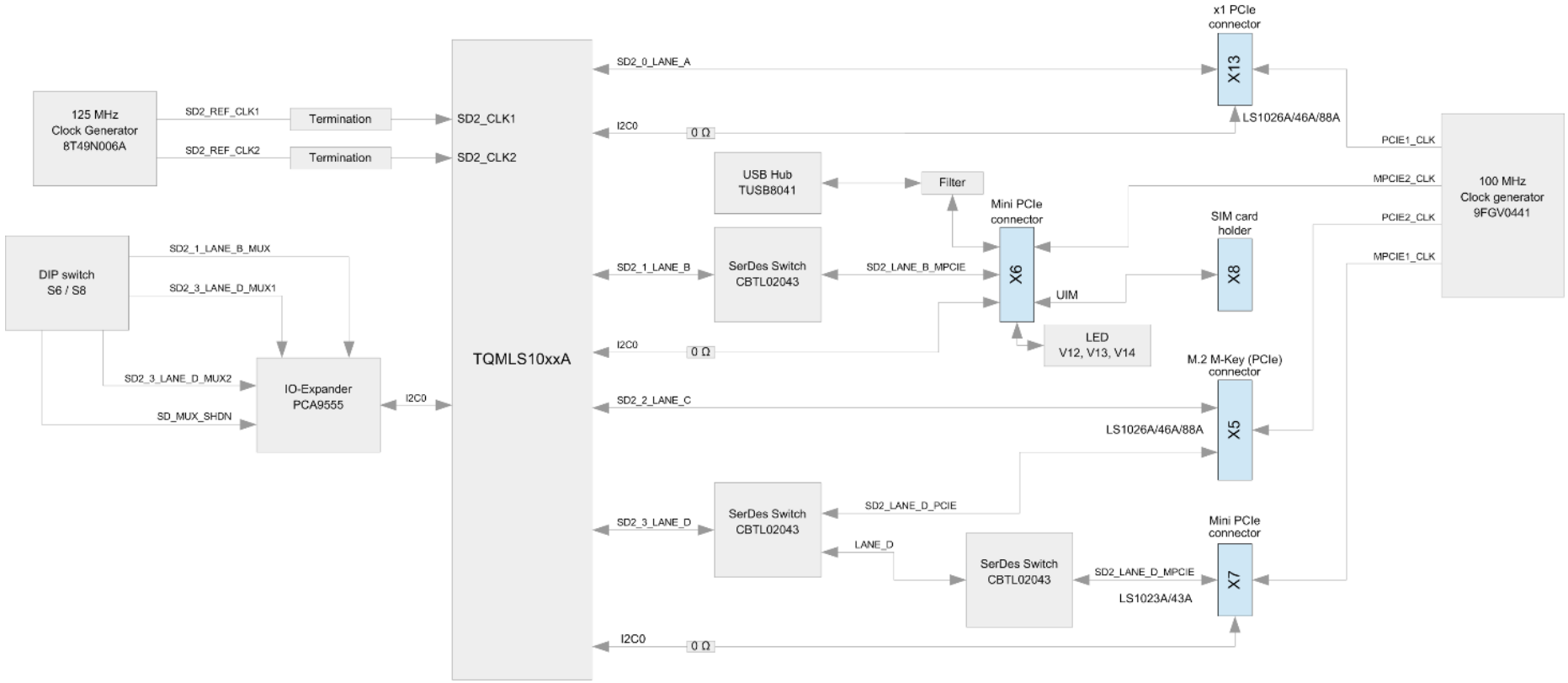

Figure 25: Block diagram PCIe, Mini PCIe, Mini PCIe + SIM card and M.2

4.2.6 PCIe, Mini PCIe and M.2 (continued)

Figure 26: Position PCIe, X13

Figure 27: Position Mini PCIe X7, Mini PCIe + SIM card, X6 + X8

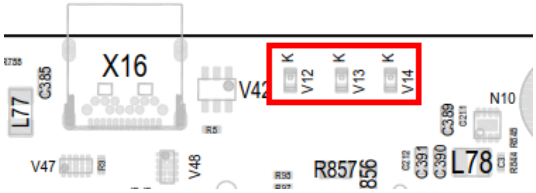

Figure 28: Position Mini PCIe Status-LEDs, V12, V13, V14

4.2.6 PCIe, Mini PCIe and M.2 (continued)

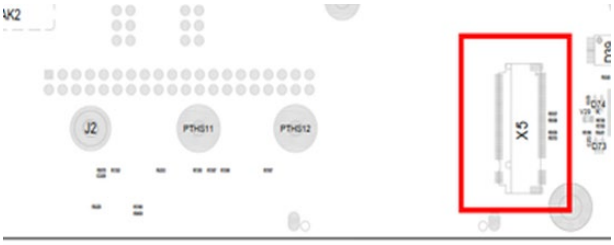

Figure 29: Position M.2 M key, X5

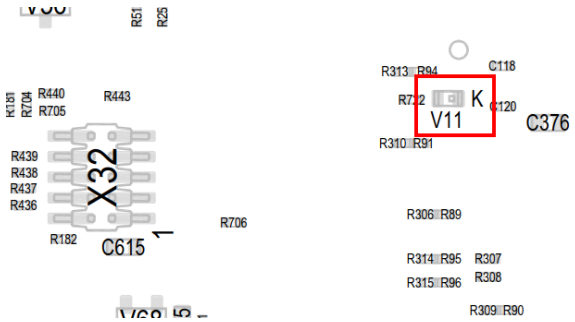

Figure 30: Position M.2 M key status LED, V11

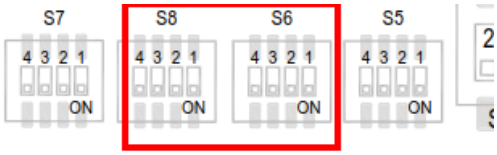

Figure 31: Position DIP switch, S6, S8

4.2.6 PCIe, Mini PCIe and M.2 (continued)

The pinout of the PCIe, Mini PCIe and M.2 interfaces can be found in the following tables.

Table 26: Pinout PCIe, X13

Remark	Signal	Pin		Signal	Remark
Connected to DGND	PRSNT1#	A1	B1	VCC12V	–
–	VCC12V	A2	B2	VCC12V	–
–	VCC12V	A3	B3	RSVD	NC
–	DGND	A4	B4	DGND	–
0 Ω in series, NP	TCK_3V3	A5	B5	I2C0_SCL	–
0 Ω in series, NP	QSGMII_PHY2_TDO	A6	B6	I2C0_SDA	I^2C address see Table 11
0 Ω in series, NP	PCIE_TDO	A7	B7	DGND	–
0 Ω in series, NP	TMS_3V3	A8	B8	VCC3V3_PCIE1	–
–	VCC3V3_PCIE1	A9	B9	JTAG_TRST#	0 Ω in series, NP
–	VCC3V3_PCIE1	A10	B10	VCC3V3_PCIE1	–
Global Reset	MB_RST#	A11	B11	NC	–
Key notch					
–	DGND	A12	B12	RSVD	NC
Signal from Clock Generator	PCIE1_CLK_P	A13	B13	DGND	–
Signal from Clock Generator	PCIE1_CLK_N	A14	B14	SD2_TX0_P	100 nF in series
	DGND	A15	B15	SD2_TX0_N	100 nF in series
0 Ω in series	SD2_RX0_P	A16	B16	DGND	–
0 Ω in series	SD2_RX0_N	A17	B17	PRSNT2#	4.7 kΩ PU to VCC3V3_PCIE1
–	DGND	A18	B18	DGND	–
NC	RSVD	A19	B19	PETP[1]	NC
–	DGND	A20	B20	PETN[1]	NC
NC	PERP[1]	A21	B21	DGND	–
NC	PERN[1]	A22	B22	DGND	–
–	DGND	A23	B23	PETP[2]	NC
–	DGND	A24	B24	PETN[2]	NC
NC	PERP[2]	A25	B25	DGND	–
NC	PERN[2]	A26	B26	DGND	–
–	DGND	A27	B27	PETP[3]	NC
–	DGND	A28	B28	PETN[3]	NC
NC	PERP[3]	A29	B29	DGND	–
NC	PERN[3]	A30	B30	RSVD	NC
–	DGND	A31	B31	PRSNT2#	4.7 kΩ PU to VCC3V3_PCIE1
NC	RSVD	A32	B32	DGND	–

4.2.6 PCIe, Mini PCIe and M.2 (continued)

Table 27: Pinout Mini PCIe, X7

Remark	Signal	Pin		Signal	Remark
–	PCIE_WAKE#	1	2	VCC3V3_MPCIE1	–
–	NC	3	4	DGND	–
–	NC	5	6	VCC1V5_MPCIE1	–
–	NC	7	8	NC	–
–	DGND	9	10	NC	–
Signal from Clock Generator	MPCIE1_CLK_N	11	12	NC	–
Signal from Clock Generator	MPCIE1_CLK_P	13	14	NC	–
–	DGND	15	16	NC	–
Key notch					
–	NC	17	18	DGND	–
–	NC	19	20	MPCI1E_DISABLE#	10 kΩ PU or PD (default: PD)
–	DGND	21	22	MB_RST#	Global Reset
–	SD2_MPCIE_RX3_N	23	24	VCC3V3_MPCIE1	–
–	SD2_MPCIE_RX3_P	25	26	DGND	–
–	DGND	27	28	VCC1V5_MPCIE1	–
–	DGND	29	30	I2C0_SCL	–
100 nF in series	SD2_MPCIE_TX3_N	31	32	I2C0_SDA	I^2C address, see Table 11
100 nF in series	SD2_MPCIE_TX3_P	33	34	DGND	–
–	DGND	35	36	NC	–
–	DGND	37	38	NC	–
–	VCC3V3_MPCIE1	39	40	DGND	–
–	VCC3V3_MPCIE1	41	42	NC	–
–	DGND	43	44	NC	–
–	NC	45	46	NC	–
–	NC	47	48	VCC1V5_MPCIE1	–
–	NC	49	50	DGND	–
–	NC	51	52	VCC3V3_MPCIE1	–

4.2.6 PCIe, Mini PCIe and M.2 (continued)

Table 28: Pinout Mini PCIe, X6

Remark	Signal	Pin		Signal	Remark
–	MPCIE2_WAKE#	1	2	VCC3V3_MPCIE2	–
–	NC	3	4	DGND	–
–	NC	5	6	VCC1V5_MPCIE2	–
–	NC	7	8	UIM_PWR	SIM card signal, see Table 29
–	DGND	9	10	UIM_DATA	SIM card signal, see Table 29
Signal from Clock Generator	MPCIE2_CLK_N	11	12	UIM_CLK	SIM card signal, see Table 29
Signal from Clock Generator	MPCIE2_CLK_P	13	14	UIM_RST	SIM card signal, see Table 29
–	DGND	15	16	UIM_VPP	SIM card signal, see Table 29
Key notch					
–	NC	17	18	DGND	–
–	NC	19	20	MPCIE2_DISABLE#	Global Reset
–	DGND	21	22	MB_RST#	–
–	SD2_MPCIE_RX1_N	23	24	VCC3V3_MPCIE2	–
–	SD2_MPCIE_RX1_P	25	26	DGND	–
–	DGND	27	28	VCC1V5_MPCIE2	–
–	DGND	29	30	I2C0_SCL	–
100 nF in series	SD2_MPCIE_TX1_N	31	32	I2C0_SDA	I^2C address, see Table 11
100 nF in series	SD2_MPCIE_TX1_P	33	34	DGND	–
–	DGND	35	36	USB2_H4_D_N	Common mode choke in series
–	DGND	37	38	USB2_H4_D_P	Common mode choke in series
–	VCC3V3_MPCIE2	39	40	DGND	–
–	VCC3V3_MPCIE2	41	42	LED_WWAN#	Green LED
–	DGND	43	44	LED_WLAN#	Green LED
–	NC	45	46	LED_WPAN	Green LED
–	NC	47	48	VCC1V5_MPCIE2	–
–	NC	49	50	DGND	–
–	NC	51	52	VCC3V3_MPCIE2	–

Table 29: Pinout SIM Card connector, X8

Pin	Signal
C1	UIM_PWR
C2	UIM_RST
C3	UIM_CLK
C4	(NA)
C5	DGND
C6	UIM_VPP
C7	UIM_DATA
SW1	NC
SW2	NC

4.2.6 PCIe, Mini PCIe and M.2 (continued)

The voltages provided for the Mini PCIe card must not exceed the currents specified in the following table.

Table 30: Maximum permitted currents Mini PCIe

Voltage rail	Nominal voltage	I_{max}
VCC12V	12 V	2.1 A
VCC3V3_MPCIEx	3.3 V	1.1 A
VCC1V5_MPCIEx	1.5 V	0.5 A

Table 31: Pinout M.2 M key, X5

Remark	Signal	Pin		Signal	Remark
10 kΩ PU or 0 Ω PD (default: PU)	M2_CONFIG3	1			
–	DGND	3	2	VCC3V3_PCIE2	–
–	NC	5	4	VCC3V3_PCIE2	–
–	NC	7	6	NC	–
–	DGND	9	8	NC	–
–	NC	11	10	LED	LED, data transfer
–	NC	13	12	VCC3V3_PCIE2	–
–	DGND	15	14	VCC3V3_PCIE2	–
–	NC	17	16	VCC3V3_PCIE2	–
–	NC	19	18	VCC3V3_PCIE2	–
10 kΩ PU or 0 Ω PD (default: PU)	M2_CONFIG0	21	20	NC	–
–	NC	23	22	NC	–
–	NC	25	24	NC	–
–	DGND	27	26	NC	–
0 Ω in series	SD2_PCIE_RX3_N	29	28	NC	–
0 Ω in series	SD2_PCIE_RX3_P	31	30	NC	–
–	DGND	33	32	NC	–
100 nF in series	SD2_PCIE_TX3_N	35	34	NC	–
100 nF in series	SD2_PCIE_TX3_P	37	36	NC	–
–	DGND	39	38	DEVSLP	10 kΩ PU or 0 Ω PD (default: NP)
0 Ω in series	SD2_RX2_N	41	40	NC	–
0 Ω in series	SD2_RX2_P	43	42	NC	–
–	DGND	45	44	NC	–
100 nF in series	SD2_TX2_N	47	46	NC	–
100 nF in series	SD2_TX2_P	49	48	NC	–
–	DGND	51	50	PCIE_RST_3V3#	10 kΩ PU or 0 Ω PD (default: PU)
Signal from Clock Generator	PCIE2_CLK_N	53	52	NC	–
Signal from Clock Generator	PCIE2_CLK_P	55	54	PCIE_WAKE_3V3#	10 kΩ PU or 0 Ω PD (default: PU)
–	DGND	57	56	NC	–
			58	NC	–
M key notch					
–	NC	67			
10 kΩ PU or 0 Ω PD (default: PU)	M2_CONFIG1	69	68	SUSCLK	10 kΩ PU or 0 Ω PD (default: NP)
–	DGND	71	70	VCC3V3_PCIE2	–
–	DGND	73	72	VCC3V3_PCIE2	–
10 kΩ PU or 0 Ω PD (default: PU)	M2_CONFIG2	75	74	VCC3V3_PCIE2	–

4.2.7 SATA

On the MBLS10xxA a SATA connector is available as 7+15p (7 signals + 15 power).

The SATA interface pinout can be taken from the following table. Depending on the RCW the SATA interface is available on the CPU derivatives. The voltages provided may be loaded with the maximum currents specified in Table 33.

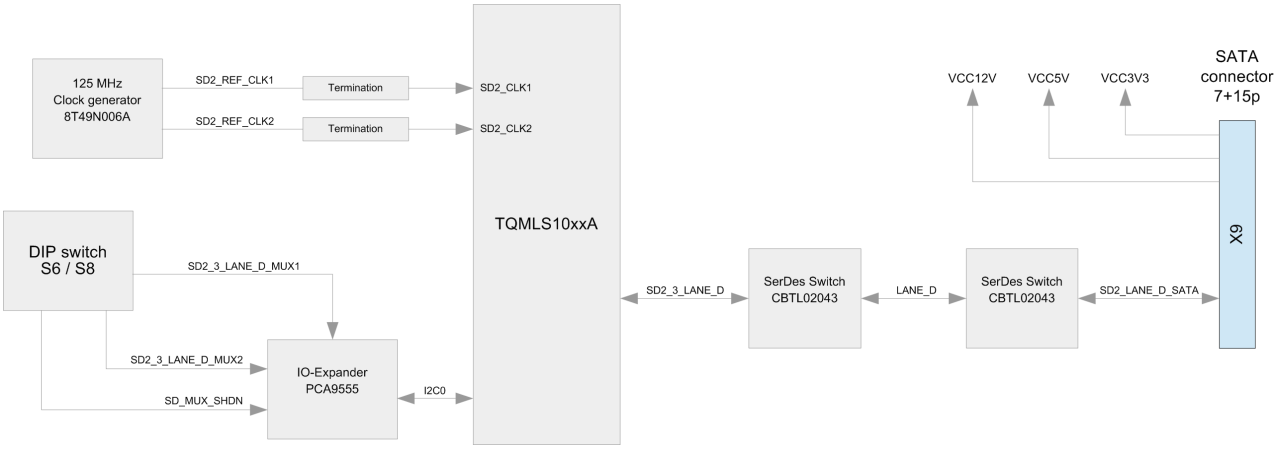

Figure 32: Block diagram SATA

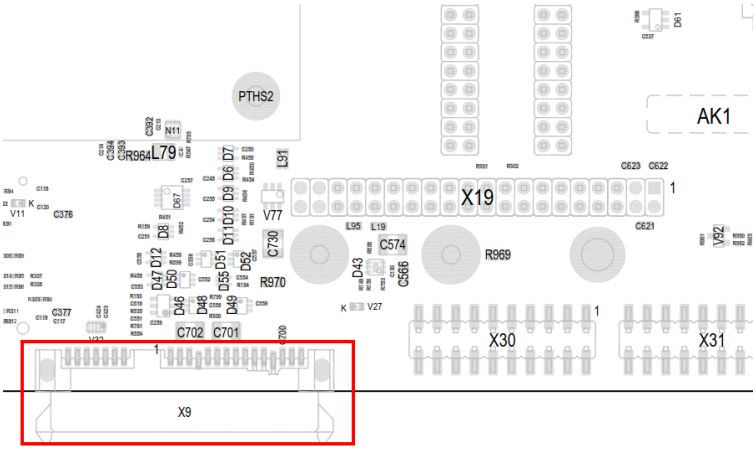

Figure 33: Position SATA, X9

Figure 34: Position DIP switch, S6, S8

4.2.7 SATA (continued)

Table 32: Pinout SATA, X9

Pin	Signal	Remark
S1	GND	Power
S2	TX+	10 nF in series
S3	TX–	10 nF in series
S4	GND	Power
S5	RX–	10 nF in series
S6	RX+	10 nF in series
S7	GND	Power
P1	3V3	VCC3V3 @ 3 W max.
P2	3V3	VCC3V3 @ 3 W max.
P3	3V3	VCC3V3 @ 3 W max.
P4	GND	Power
P5	GND	Power
P6	GND	Power
P7	5V	VCC5V @ 3 W max.
P8	5V	VCC5V @ 3 W max.
P9	5V	VCC5V @ 3 W max.
P10	GND	Power
P11	RES	–
P12	GND	Power
P13	12V	VCC12V @ 5 W max.
P14	12V	VCC12V @ 5 W max.
P15	12V	VCC12V @ 5 W max.
M1	Shield (DGND)	Shield connected to DGND
M2	Shield (DGND)	Shield connected to DGND

Table 33: Maximum permitted currents SATA

Voltage rail	Nominal voltage	I_{max}	P_{max}
VCC12V	12 V	0.4 A	5 W
VCC5V	5 V	0.6 A	3 W
VCC3V3	3.3 V	0.9 A	3 W

4.2.8 CAN

The LS10xxA has no CAN interface, therefore a CAN interface is generated using the CPLD and the SPI interface. Via a multiplexer, either the SPI interface or the IOs of the CPLD can be used and are available at the 3-pin connector X24. The interface is galvanically separated.

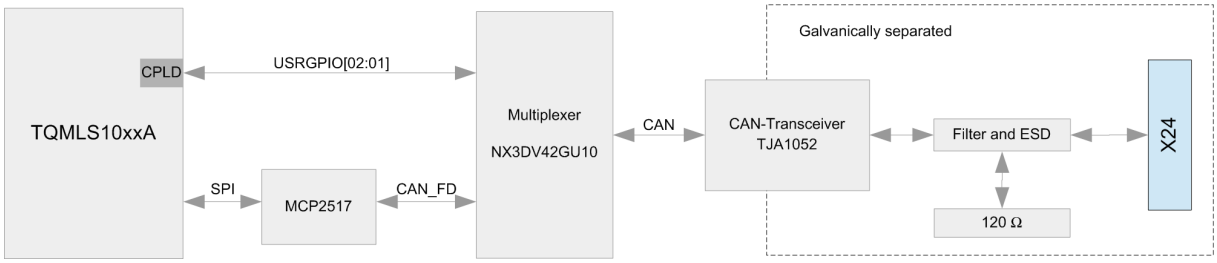

Figure 35: Block diagram CAN

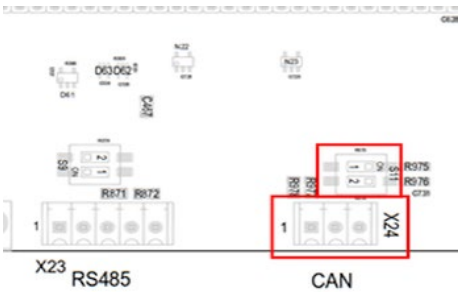

Figure 36: Position CAN, X24, DIP switch, S11

The following table shows the pinout of the CAN connector.

Table 34: Pinout CAN, X24

Pin	Signal	Direction	Remark
1	CAN_H	I/O	Galvanically separated
2	CAN_L	I/O	
3	GND_CAN	P	

The CAN signals can be terminated with 60 Ω using the DIP switches S11-1 & S11-2

Table 35: CAN termination, DIP switch S11

DIP switch	Signal	ON	OFF
S11-1 (1~2)	CANH	CANH terminated with 60 Ω	CANH not terminated
S11-2 (3~4)	CANL	CANL terminated with 60 Ω	CANL not terminated

All other combinations of S11 (e.g., S11-1 ON & S11-2 OFF) are not permitted.

4.2.9 RS-485

The UART1 interface of the TQMLS10xxA is connected to an RS-485 transceiver (SP491), which provides the signals at the 5-pin connector X23. The RS-485 interface is electrically separated.

The interface is configured for full-duplex operation by default, but can be changed to half-duplex by assembly options. In this case the receiver is controlled by UART7.CTS#. The placement options are shown in the MBLS10xxA schematics.

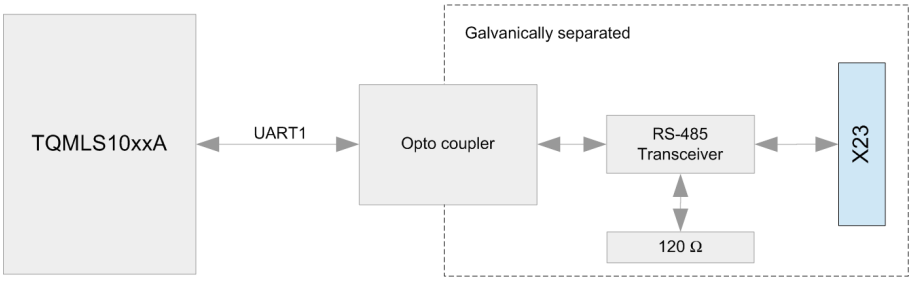

Figure 37: Block diagram RS-485

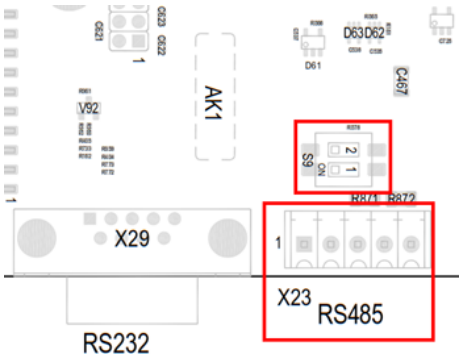

Figure 38: Position RS-485, X23, DIP switch, S9

The following table shows the pin assignment of the RS-485 connector.

Table 36: Pinout RS-485, X23

Pin	Pin name	Signal	Direction	Remark
1	A	RS-485_A	I	Galvanically separated
2	B	RS-485_B	I	
3	Y	RS-485_Y	O	
4	Z	RS-485_Z	O	
5	DGND	DGND_RS-485	P	

The RS-485 signals can be terminated with DIP switches S9-1 and S9-2 with 120 Ω.

Table 37: RS-485 termination, DIP switch S9

DIP switch	ON	OFF
S9-1 (1~2)	Receive path terminated with 120 Ω	Receive path terminated with 120 Ω
S9-2 (3~4)	Receive path terminated with 120 Ω	Receive path terminated with 120 Ω

4.2.10 RS-232

On the MBLS10xxA a RS-232 debug interface is available. By default UART2 of the TQMLS10xxA is used, optionally UART1 as placement option. No software configuration is required.

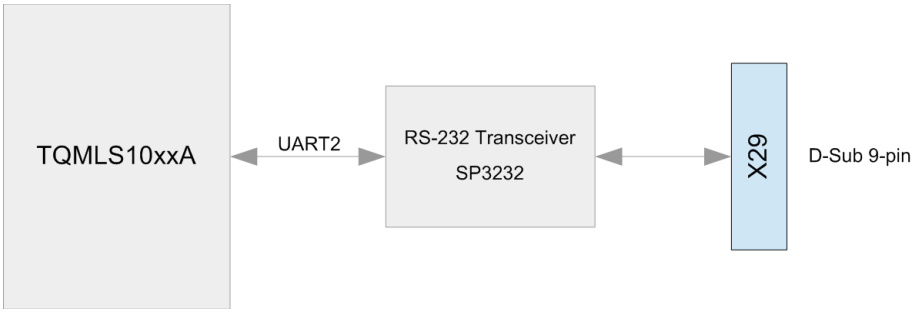

Figure 39: Block diagram RS-232

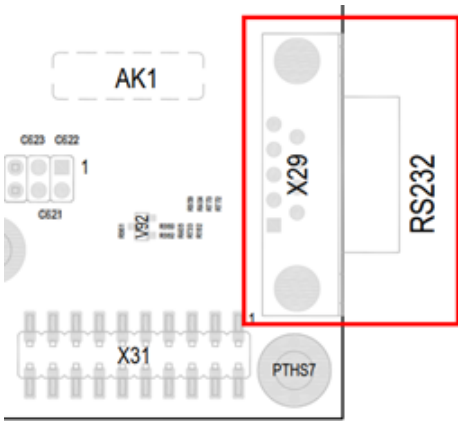

Figure 40: Position RS-232, X29

The following table shows the pin assignment of the RS-232 connector.

Table 38: Pinout RS-232, X29

Pin	Signal
1	NC
2	RS-232_RXD
3	RS-232_TXD
4	NC
5	DGND
6	NC
7	RS-232_RTS#
8	RS-232_CTS#
9	NC
M1, M2	DGND

4.2.11 SD card

The SD card connector is connected to the SDHC controller of the TQMLS10xxA via a multiplexer. A four bit wide data interface is used. To set the multiplexer correctly, DIP switch (S5-1) must be set accordingly.

The SDHC controller in the TQMLS10xxA basically supports the USH-I mode, but on the MBLS10xxA it is not used. At most the High-Speed mode is available. From SD card can be booted, see chapter 4.1.1.3. All data lines are provided with ESD protection.

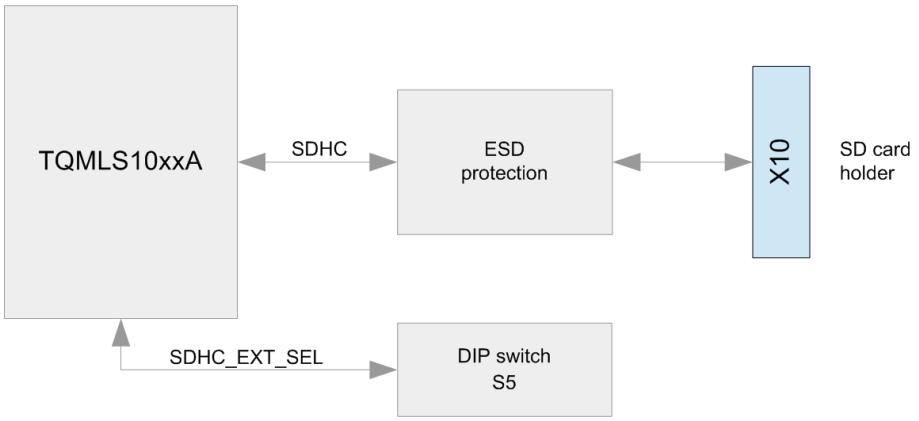

Figure 41: Block diagram SD card

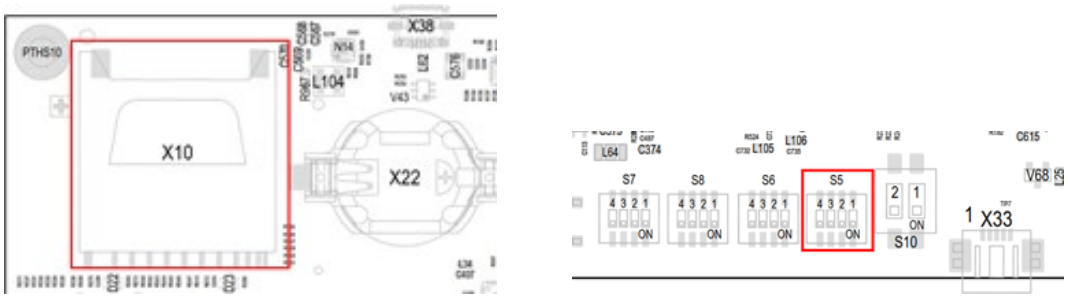

Figure 42: Position SD card socket, X10, DIP switch, S5

4.2.11 SD card (continued)

Table 39: Pinout SD card socket, X10

Pin	Signal	Remark
1	SDHC_DAT3_MOD	22 Ω in series, 10 kΩ PU to 3.3 V + ESD protection
2	SDHC_CMD_MOD	22 Ω in series, 10 kΩ PU to 3.3 V + ESD protection
3	DGND	–
4	VCC3V3	–
5	SDHC_CLK_MOD	22 Ω in series, 10 kΩ PU to 3.3 V + ESD protection
6	DGND	–
7	SDHC_DAT0_MOD	22 Ω in series, 10 kΩ PU to 3.3 V + ESD protection
8	SDHC_DAT1_MOD	22 Ω in series, 10 kΩ PU to 3.3 V + ESD protection
9	SDHC_DAT2_MOD	22 Ω in series, 10 kΩ PU to 3.3 V + ESD protection
CDS	SDHC_CD#	10 kΩ PU to 3.3 V + ESD protection
COM	DGND	–
WP	SDHC_WP	10 kΩ PU to 3.3 V + ESD protection
M1, M2	SHIELD	Connected to DGND

Table 40: Boot Source Selection, DIP switch S5-1

DIP switch	Signal	ON	OFF
S5-1 (1~2)	SHDC_EXT_SEL	eMMC	SDHC

Note: SD card supply voltage	
	SD cards always start with 3.3 V I/O voltage after power-up. For the modes with 1.8 V I/O voltage they are switched by software. When rebooting or resetting the MBLS10xxA, the SD card remains at the last used I/O voltage because it does not have a separate reset signal. The SDHC controller, on the other hand, returns to 3.3 V I/O voltage. Therefore, the supplied BSP is limited to the 3.3 V modes.

4.2.12 Headers

The MBLS10xxA features three pin headers. All unused signals are made available on these pin headers.
In addition to the signals, 3.3 V, 5 V and 12 V are available on each pin header. Each of the three voltage rails can be loaded with 1 A each, i.e. 1 A in total on all three pin headers.

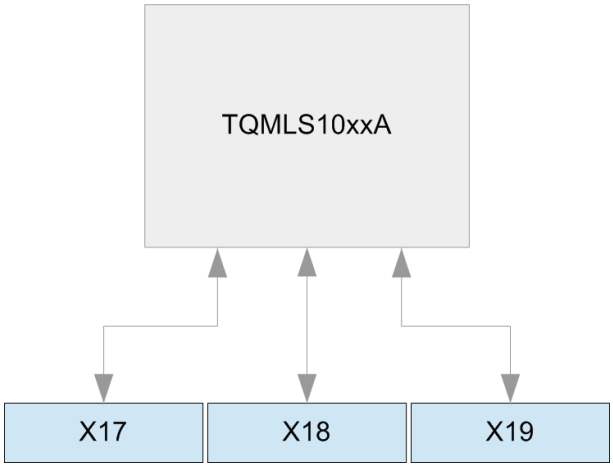

Figure 43: Block diagram headers

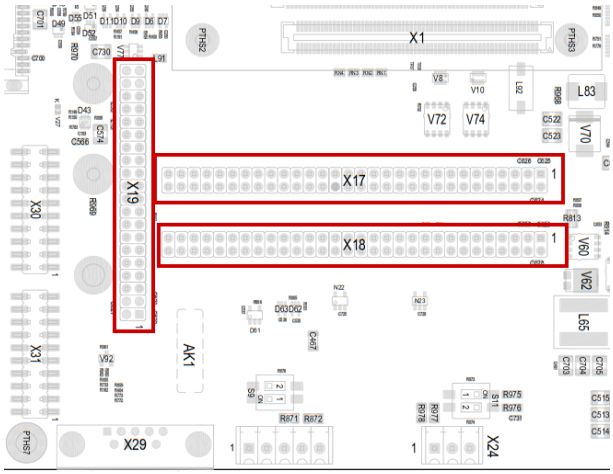

Figure 44: Position headers, X17, X18, X19

4.2.12 Headers (continued)

Table 41: Pinout Header 1, X17

Group	Signal	Pin		Signal	Group
Power	VCC5V	1	2	VCC3V3	Power
Power	VCC12V	3	4	DGND	Power
Power	DGND	5	6	DGND	Power
IFC	IFC_AD00_CFG_GPINPUT0	7	8	IFC_AD08_CFG_RCW_SRC0	IFC
IFC	IFC_AD01_CFG_GPINPUT1	9	10	IFC_AD09_CFG_RCW_SRC1	IFC
IFC	IFC_AD02_CFG_GPINPUT2	11	12	IFC_AD10_CFG_RCW_SRC2	IFC
IFC	IFC_AD03_CFG_GPINPUT3	13	14	IFC_AD11_CFG_RCW_SRC3	IFC
IFC	IFC_AD04_CFG_GPINPUT4	15	16	IFC_AD12_CFG_RCW_SRC4	IFC
IFC	IFC_AD05_CFG_GPINPUT5	17	18	IFC_AD13_CFG_RCW_SRC5	IFC
IFC	IFC_AD06_CFG_GPINPUT6	19	20	IFC_AD14_CFG_RCW_SRC6	IFC
IFC	IFC_AD07_CFG_GPINPUT7	21	22	IFC_AD15_CFG_RCW_SRC7	IFC
Power	DGND	23	24	DGND	Power
IFC	IFC_AVD	25	26	IFC_CS0#	IFC
IFC	IFC_BCTL	27	28	IFC_CS1#	IFC
IFC	IFC_CLE_CFG_RCW_SRC8	29	30	IFC_CS2#	IFC
Power	DGND	31	32	IFC_CS3#	IFC
IFC	IFC_CLK0	33	34	DGND	Power
IFC	IFC_CLK1	35	36	DGND	Power
Power	DGND	37	38	IFC_NDDR_CLK	IFC
IFC	IFC_PAR0	39	40	DGND	Power
IFC	IFC_PAR1	41	42	IFC_NDDQS	IFC
IFC	IFC_PERR#	43	44	IFC_OE#_CFG_ENG_USE1	IFC
IFC	IFC_RB0#	45	46	IFC_WE0#	IFC
IFC	IFC_RB1#	47	48	IFC_WP0#_CFG_ENG_USE2	IFC
IFC	IFC_TE_CFG_IFC_TE	49	50	DGND	Power
Power	DGND	51	52	DGND	Power
IO	USRGPI01	53	54	DGND	Power
IO	USRGPI02	55	56	USRGPI04	IO
IO	USRGPI03	57	58	USRGPI05	IO
Power	DGND	59	60	DGND	Power

4.2.12 Headers (continued)

Table 42: Pinout Header 2, X18

Group	Signal	Pin		Signal	Group
Power	VCC5V	1	2	VCC3V3	Power
Power	VCC12V	3	4	DGND	Power
Power	DGND	5	6	DGND	Power
I2C	I2C_BRD_SCL	7	8	I2C2_SDA	I2C
I2C	I2C_BRD_SDA	9	10	I2C2_SCL	I2C
I2C	IIC1_SCL_MOD	11	12	I2C3_SDA	I2C
I2C	IIC1_SDA_MOD	13	14	I2C3_SCL	I2C
Power	DGND	15	16	DGND	Power
SD_MOD	SDHC_CLK_SYNC_IN	17	18	DGND	Power
SD_MOD	SDHC_CLK_SYNC_OUT	19	20	DGND	Power
Power	DGND	21	22	SPI_SOUT	SPI
UART_CPU	UART2_SIN	23	24	SPI_SIN	SPI
UART_CPU	UART2_SOUT	25	26	DGND	Power
Power	DGND	27	28	SPI_SCK	SPI
UART_CPU	UART1_SIN	29	30	DGND	Power
UART_CPU	UART1_RTS#	31	32	SPI_PCS0	SPI
UART_CPU	UART1_CTS#	33	34	SPI_PCS1	SPI
UART_CPU	UART1_SOUT	35	36	SPI_PCS2	SPI
Power	DGND	37	38	SPI_PCS3	SPI
FTM	FTM3_CH0	39	40	DGND	Power
FTM	FTM3_CH1	41	42	EVT0#	EVT
FTM	FTM3_CH2	43	44	EVT1#	EVT
FTM	FTM3_CH3	45	46	EVT2#	EVT
Power	DGND	47	48	EVT3#	EVT
FTM	FTM3_CH4	49	50	EVT4#	EVT
FTM	FTM3_CH5	51	52	EVT9#	EVT
FTM	FTM3_CH6	53	54	DGND	Power
FTM	FTM3_CH7	55	56	IRQ0	IRQ
Power	DGND	57	58	IRQ1	IRQ
IRQ	IRQ11	59	60	IRQ2	IRQ

4.2.12 Headers (continued)

Table 43: Pinout Header 3, X19

Group	Signal	Pin		Signal	Group
Power	VCC5V	1	2	VCC3V3	Power
Power	VCC12V	3	4	DGND	Power
Power	DGND	5	6	SDA_UART_RX	SDA
SDA	SDA_UART_TX	7	8	GPIO_EXP_01	TQMLS10xxA
Power	DGND	9	10	DGND	Power
TQMLS10xxA	RTC_INT_OUT#	11	12	RESIN#	Reset
TQMLS10xxA	TEMP_CRIT_MOD#	13	14	RESET_OUT#	Reset
TQMLS10xxA	CPU_ASLEEP	15	16	CPU_RTC	TQMLS10xxA
TQMLS10xxA	CKSTP_OUT#	17	18	CLKOE	TQMLS10xxA
TQMLS10xxA	PROG_SFP	19	20	DGND	Power
Reset	RESET_REQ_OUT#	21	22	HRESET#	Reset
Reset	POWER_FAIL#	23	24	PORESET#	Reset
TQMLS10xxA	TBSCAN_EN#	25	26	TA_BB_TMP_DETECT#	TQMLS10xxA
TQMLS10xxA	SLEEP	27	28	TA_TMP_DETECT#	TQMLS10xxA
Power	DGND	29	30	DGND	Power
PHY	EC1_PHY_GPIO0	31	32	EC2_PHY_GPIO0	PHY
PHY	EC1_PHY_GPIO1	33	34	EC2_PHY_GPIO1	PHY
Power	DGND	35	36	USB_H3_VBUS	USB
Power	DGND	37	38	USB2_H3_D_N	USB
Power	DGND	39	40	USB2_H3_D_P	USB

4.3 Diagnostic and user interfaces

4.3.1 Status LEDs

The MBLS10xxA offers 43 diagnosis and status LEDs to signal the system status.
The following table shows the meaning of the LEDs.

Table 44: Status LEDs

Interface	Ref.	Colour	Signal
USB	V24	Green	VBUS USB Host 1 (lit, when VBUS of USB Host 1 is active)
	V25	Green	VBUS USB Host 2 (lit, when VBUS of USB Host 2 is active)
	V26	Green	VBUS USB2 (lit, when VBUS of USB2 is active)
	V27	Green	VBUS USB Host 3 (lit, when VBUS of USB Host 3 is active)
	V28	Green	VBUS USB3 (lit, when VBUS of USB3 is active)
	V76	Green	VBUS USB1 (lit, when VBUS of USB1 is active)
Mini PCIe	V12	Green	Mini PCIe WWAN
	V13	Green	Mini PCIe WLAN
	V14	Green	Mini PCIe WPAN
M.2 M key	V11	Green	M.2 status (lit during data transfer)
GPIO	V78	Green	LED on Port Expander Port IO1_5 (lit when port low)
Power	V15	Green	Status 12 V (lit, when supply 12 V is active)
	V16	Green	Status 5.0_SOURCE V (lit, when supply 5 V is active)
	V17	Green	Status 1.1 V (lit, when supply 1.1 V is active)
	V18	Green	Status 1.8 V (lit, when supply 1.8 V is active)
	V19	Green	Status 1.0 V (lit, when supply 1.0 V is active)
	V20	Green	Status 3.3_SOURCE V (lit, when supply 3.3 V is active)
	V21	Green	Status 2.5 V (lit, when supply 2.5 V is active)
	V22	Green	Status 1.5 V (lit, when supply 1.5 V is active)
	V23	Green	Status 24 V (lit, when supply 24 V is active)
OpenSDA	V29	Green	OpenSDA status (lit when OpenSDA is used)
Ethernet	X12A	Yellow	Activity LED Ethernet 1 (lit on error) lit on error
	X12A	Green	Error LED Ethernet 1 (lit when link is active, flashes during data transfer)
	X12B	Yellow	Activity LED Ethernet 2 (lit on error)
	X12B	Green	Error LED Ethernet 2 (lit when link is active, flashes during data transfer)
	X40AA	Yellow	Activity LED QSGMII 1 (lit on error)
	X40AA	Green	Error LED QSGMII 1 (lit when link is active, flashes during data transfer)
	X40AB	Yellow	Activity LED QSGMII 1 (lit on error)
	X40AB	Green	Error LED QSGMII 1 (lit when link is active, flashes during data transfer)
	X40BA	Yellow	Activity LED QSGMII 1 (lit on error)
	X40BA	Green	Error LED QSGMII 1 (lit when link is active, flashes during data transfer)
	X40BB	Yellow	Activity LED QSGMII 1 (lit on error)
	X40BB	Green	Error LED QSGMII 1 (lit when link is active, flashes during data transfer)
	X39AA	Yellow	Activity LED QSGMII 2 (lit on error)
	X39AA	Green	Error LED QSGMII 2 (lit when link is active, flashes during data transfer)
	X39AB	Yellow	Activity LED QSGMII 2 (lit on error)
	X39AB	Green	Error LED QSGMII 2 (lit when link is active, flashes during data transfer)
	X39BA	Yellow	Activity LED QSGMII 2 (lit on error)
	X39BA	Green	Error LED QSGMII 2 (lit when link is active, flashes during data transfer)
	X39BB	Yellow	Activity LED QSGMII 2 (lit on error)
	X39BB	Green	Error LED QSGMII 2 (lit when link is active, flashes during data transfer)
Reset	V99	Red	Reset LED (lit when reset button S2 is pressed)
	V94	Green	VCC_EN (lit, when POWER_GOOD is present)

4.3.2 Navigation buttons

For development purposes two push buttons are connected to a port expander on the MBLS10xxA.
By using the signal IRQ2 this expander is interrupt capable.
The signal lines between button and port expander are provided with 10 kΩ pull-up resistors to 3.3 V.

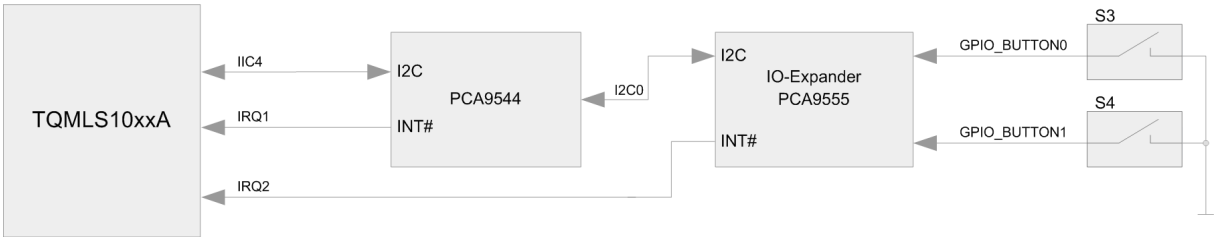

Figure 45: Block diagram navigation buttons

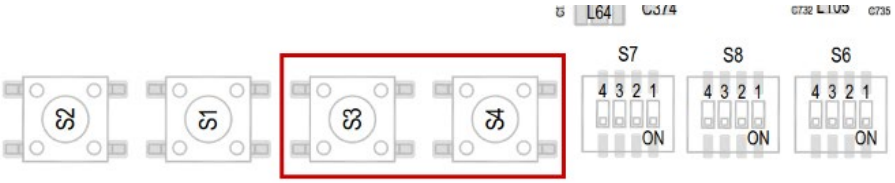

Figure 46: Position Navigation buttons, S3, S4

4.3.3 Power and Reset button

A reset button (S2) is provided on the MBLS10xxA.

4.3.4 JTAG®

The JTAG® port of the LS10xxA is routed to a standard ARM® 20-pin JTAG® connector (X30) on the MBLS10xxA.
The pull-ups for the signals TDI, TMS, TRST# and SRST# are populated on the MBLS10xxA. All signals have 3.3 V level.
The JTAG® interface is not ESD protected.
The JTAG® chain can be extended by an assembly option, since the JTAG® chain between TQMLS10xxA and JTAG® connector X30 is closed by default. (See following Figure, blue dotted line). Refer to the MBLS10xxA schematic for more information.

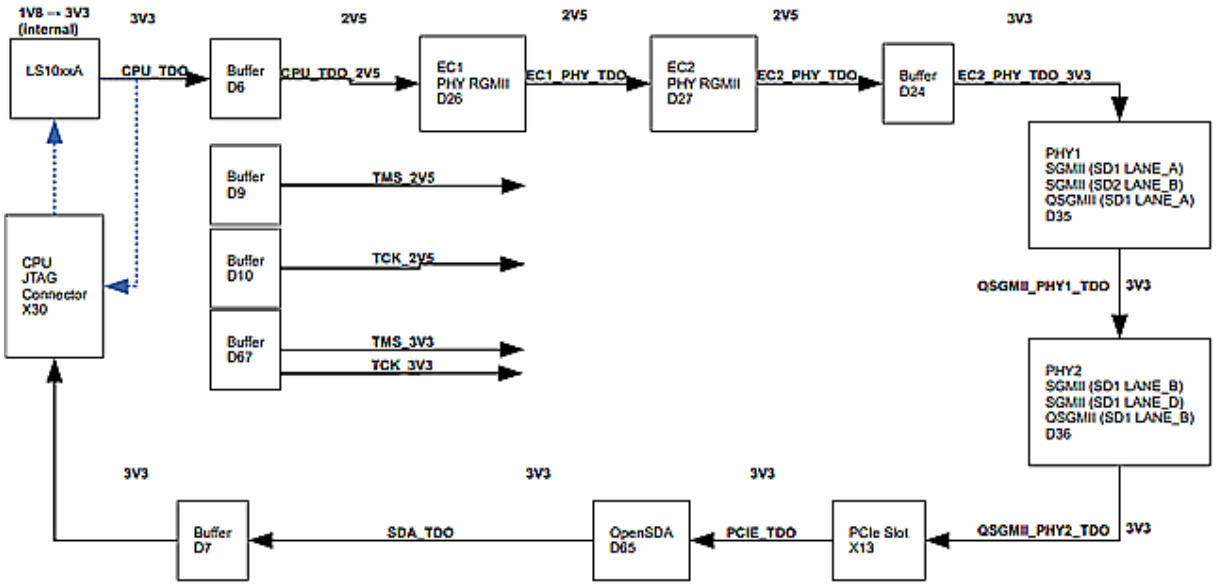

Figure 47: Block diagram JTAG® chain

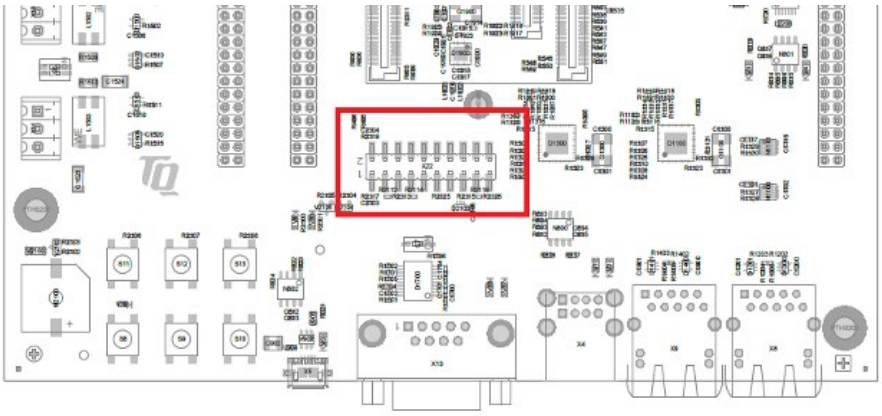

Figure 48: Position of JTAG® connector X30

4.3.4 JTAG® (continued)

The following table shows the JTAG® connector pinout.

Table 45: Pinout JTAG® header, X30

Pin	Signal	Remark
1	JTAG_VREF	100 Ω in series to 3.3 V, use only as reference
2	3.3 V	0 Ω to 3.3 V, I_{max} = 10 mA
3	JTAG_TRST#	10 kΩ PU to 3.3 V
4	DGND	–
5	JTAG_TDI	–
6	DGND	–
7	JTAG_TMS	–
8	GND_DETECT	10 kΩ PU to 3.3 V – OpenSDA interface
9	JTAG_TCK	Optional 10 kΩ PU to 3.3 V
10	DGND	–
11	NC	10 kΩ to DGND
12	DGND	–
13	JTAG_TDO	–
14	DGND	–
15	JTAG_SRST#	10 kΩ PU to 3.3 V, Open-Drain-Buffer at RESET_IN#
16	DGND	–
17	3.3 V	10 kΩ to 3.3 V
18	DGND	–
19	DGND	10 kΩ to DGND
20	DGND	–

4.3.5 OpenSDA

The OpenSDA interface serves as a plug and play programming interface for the TQMLS10xxA and is provided via a Kinetis µC (MK22FX512AVLH12). It can be used to program and debug the CPU via USB.

The Kinetis µC is connected to the CPU via JTAG. Furthermore, communication with the µC is possible via a UART on connector X19 (pin assignment see Table 43).

To prevent the OpenSDA and a debugger connected to JTAG® from accessing the JTAG® interface of the CPU simultaneously, the GND_DETECT signal is used to detect a connected debugger. In this case the OpenSDA is deactivated. A USB Mini-B connector (X33) as interface to a PC is available.

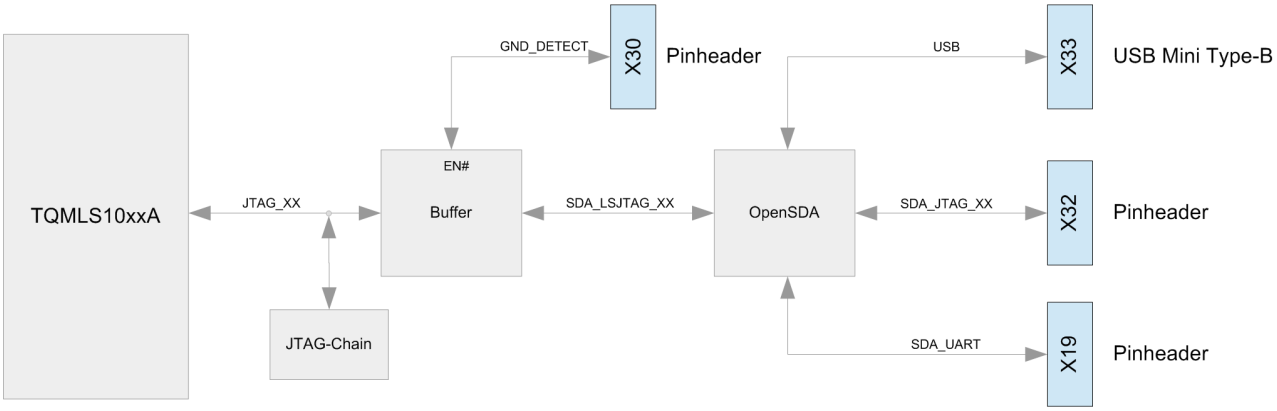

Figure 49: Block diagram OpenSDA / JTAG®

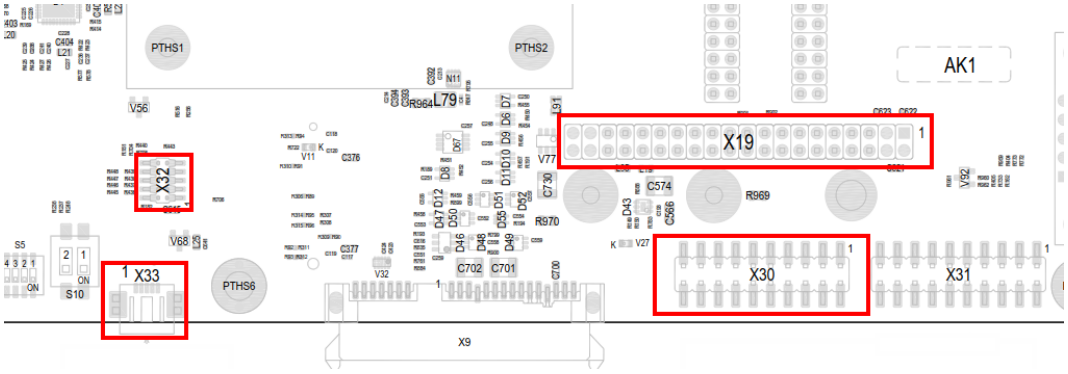

Figure 50: Position of OpenSDA / JTAG® interface

4.3.5 OpenSDA (continued)

The following table shows the pin assignment of the JTAG® connector X32 for the Kinetis µC.

Table 46: Pinout OpenSDA, 100 mil header, X32

Pin	Signal	Remark
1	VCC3V3_SDA	–
2	SDA_JTAG_TMS	10 kΩ PU to V_SDA_3V3 ⇨ OpenSDA Interface
3	DGND	–
4	SDA_JTAG_TCLK	–
5	DGND	–
6	SDA_JTAG_TDO	–
7	NC	–
8	SDA_JTAG_TDI	–
9	DGND	–
10	SDA_RST#	–

Table 47: Pinout OpenSDA, USB Mini-B, X33

Pin	Signal	Remark
1	V_SDA_VBUS	–
2	USB0_DM	33 Ω in series
3	USB0_DP	33 Ω in series
4	NC	–
5	DGND	–
M1	Shield	–
M2	NC	–

5. SOFTWARE

No software is required for the MBLS10xxA.
Suitable software is only required on the TQMLS10xxA and is not a part of this User's Manual.
More information can be found in the TQ-Support Wiki for the TQMLS10xxA.

6. MECHANICS

6.1 MBLS10xxA dimensions

The MBLS10xxA has overall dimensions (length × width) of 250 × 190 mm².
The MBLS10xxA has a maximum height of approximately 34.7 mm.
The MBLS10xxA has six 4.3 mm mounting holes for the housing, and four 2.7 mm mounting holes for a heat sink.
The MBLS10xxA weighs approximately 430 grams without TQMLS10xxA.

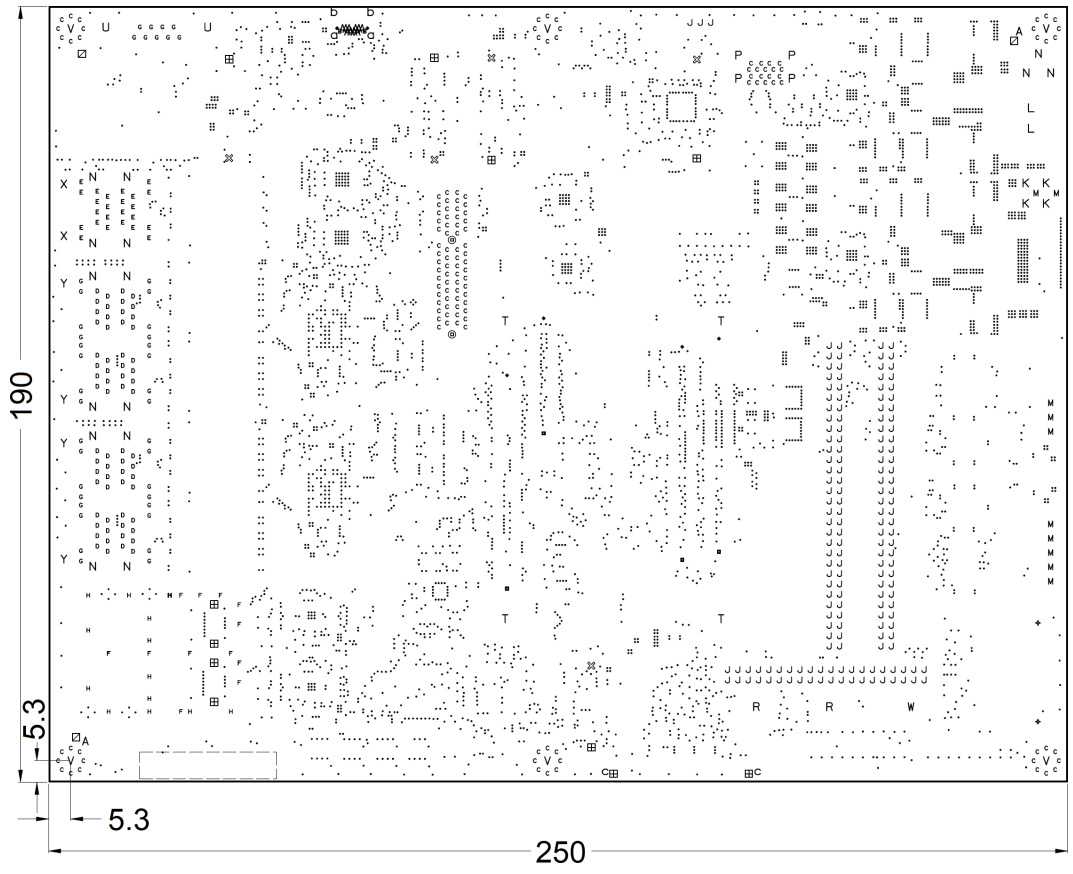

Figure 51: MBLS10xxA dimensions

6.2 Notes of treatment

The MBLS10xxA is held in the mating connectors with a retention force of approximately 42 N.
To avoid damaging the MBLS10xxA connectors as well as the carrier board connectors while removing the MBLS10xxA the use of the extraction tool MOZI52XX is strongly recommended.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBLS10xxA for the extraction tool MOZI52XX.

6.3 Embedding in the overall system

The MBLS10xxA serves as a design base for customer products, as well as a platform to support during development.

6.4 Housing

The form factor and the mounting holes of the MBLS10xxA are designed for installation in a standard EURO housing.

6.5 Thermal management

MBLS10xxA plus TQMLS10xxA have a maximum peak power consumption of approx. 8.5 watts.
Further power loss occurs mainly at externally connected devices.

Attention: TQMLS10xxA heat dissipation	
	The LS10xxA CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMLS10xxA must be taken into consideration when connecting the heat sink. The TQMLS10xxA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMLS10xxA or the MBLS10xxA and thus malfunction, deterioration or destruction.

6.6 Assembly

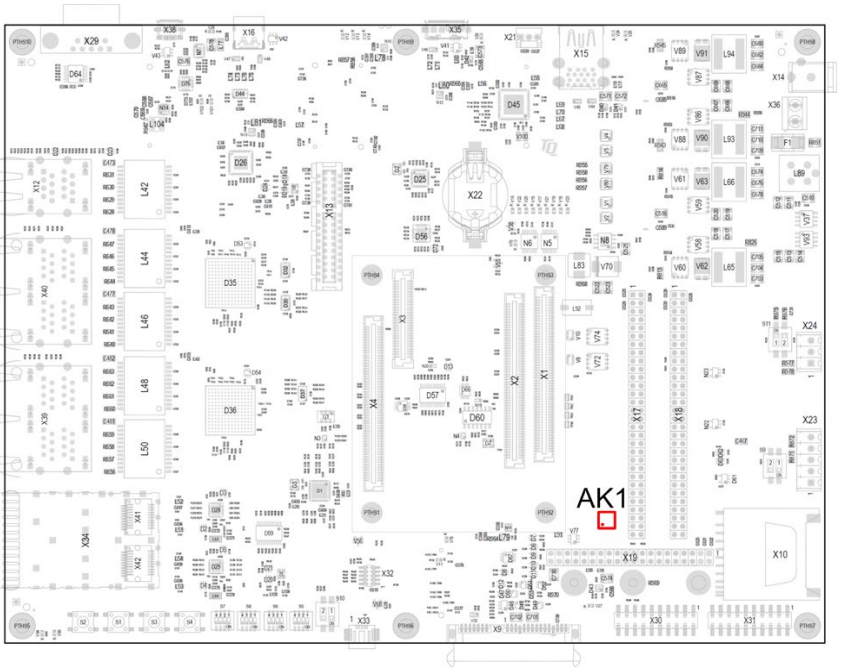

Figure 52: MBLS10xxA component placement top

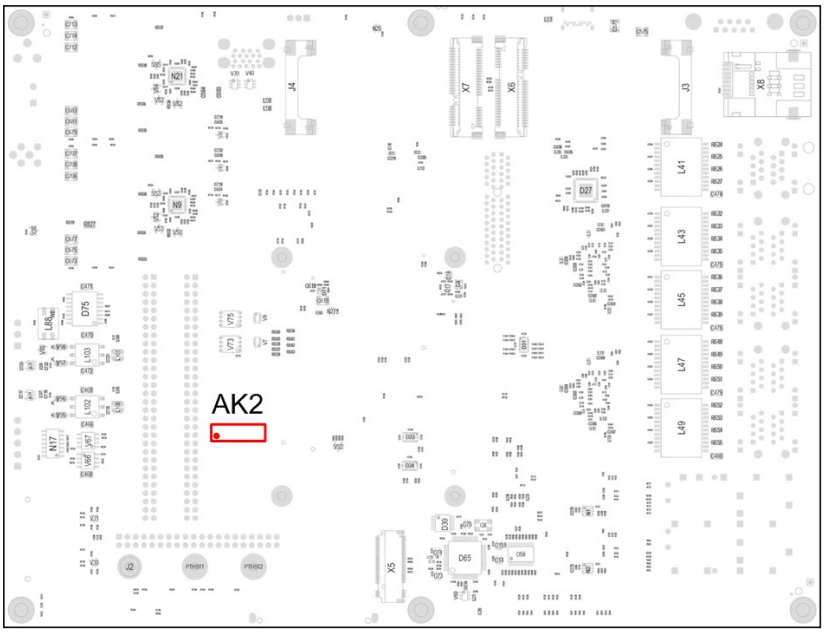

Figure 53: MBLS10xxA component placement bottom

The labels on the MBLS10xxA revision 0200 show the following information:

Table 48: Labels on MBLS10xxA

Label	Text
AK1	Serial number
AK2	MBLS10xxA version and revision + tests performed

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

Since the MBLS10xxA is a development platform, no EMC tests have been performed.
During the development of the MBLS10xxA the standard DIN EN 55022 A1:2007 was taken into account.

7.2 ESD

ESD protection is provided on most interfaces of the MBLS10xxA.
The MBLS10xxA circuit diagram shows which interfaces provide ESD protection.

7.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

8. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 49: Climatic and operational conditions MBLS10xxA

Parameter	Range	Remark
Ambient temperature	0 °C to +60 °C	With Lithium battery
Ambient temperature	0 °C to +70 °C	Without Lithium battery
Storage temperature	–10 °C to +60 °C	With Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMLS10xxA heat dissipation	
	The LS10xxA CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMLS10xxA must be taken into consideration when connecting the heat sink. The TQMLS10xxA is not the highest component. Inadequate cooling connections can lead to overheating of the TQMLS10xxA and thus malfunction, deterioration or destruction.

8.1 Protection against external effects

Protection class IP00 was defined for the MBLS10xxA. There is no protection against foreign objects, touch or humidity.

8.2 Reliability and service life

No detailed MTBF calculation has been done for the MBLS10xxA.
The MBLS10xxA is designed to be insensitive to vibration and impact.

9. ENVIRONMENT PROTECTION

9.1 RoHS

The MBLS10xxA is manufactured RoHS compliant. All components and assemblies are RoHS compliant. The soldering processes are RoHS compliant.

9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBLS10xxA was designed to be recyclable and easy to repair.

9.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

9.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBLS10xxA must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBLS10xxA enable compliance with EuP requirements for the MBLS10xxA.

9.5 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBLS10xxA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The MBLS10xxA is delivered in reusable packaging.

9.6 Batteries

9.6.1 General notes

Due to technical reasons a battery is necessary for the MBLS10xxA. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

9.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the MBLS10xxA, it is produced in such a way, that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls). These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

10. APPENDIX

10.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 50: Acronyms

Acronym	Meaning
AC	Alternating Current
AHCI	Advanced Host Controller Interface
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR4	Double Data Rate 4
DIP	Dual In-line Package
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GPU	Graphics Processing Unit
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Controller
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean operating Time Between Failures
NA	Not Available
NC	Not Connected
NOR	Not-Or
NP	Not Placed
O	Output
OC	Open Collector
OpenSDA	Serial and Debug Adapter (NXP)
OTG	On-The-Go

10.1 Acronyms and definitions (continued)

Table 50: Acronyms (continued)

Acronym	Meaning
P	Power
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PTC	Positive Temperature Coefficient
PU	Pull-Up
PWM	Pulse-Width Modulation
QSGMII	Quad Serial Gigabit Media-Independent Interface
R/W	Read/Write
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SSD	Solid-State Disk
SVHC	Substances of Very High Concern
TSN	Time Sensitive Networking
UART	Universal Asynchronous Receiver/Transmitter
UHS-I	Ultra High-Speed (Speed Grades I, II, III)
UM	User's Manual
UN	United Nations
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network
XSPI	Expanded Serial Peripheral Interface

10.2 References

Table 51: Further applicable documents

No.	Name	Rev., Date	Company
(1)	Reference Manuals: LS1043A LS1046A LS1088A	Rev. 3, 02/2017 Rev. 1, 10/2017 Rev. 0, 02/2018	NXP NXP NXP
(2)	Data Sheets: LS1043A LS1046A LS1088A	Rev. 3, 03/2018 Rev. 1, 03/2018 Rev. 0, 01/2018	NXP NXP NXP
(3)	TQMLS10xxA User's Manual	– current –	TQ-Systems
(4)	TQMLS10xxA Support Wiki	– current –	TQ-Systems

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