MBLS102xA
User's Manual

MBLS102xA UM 0100
24.08.2016

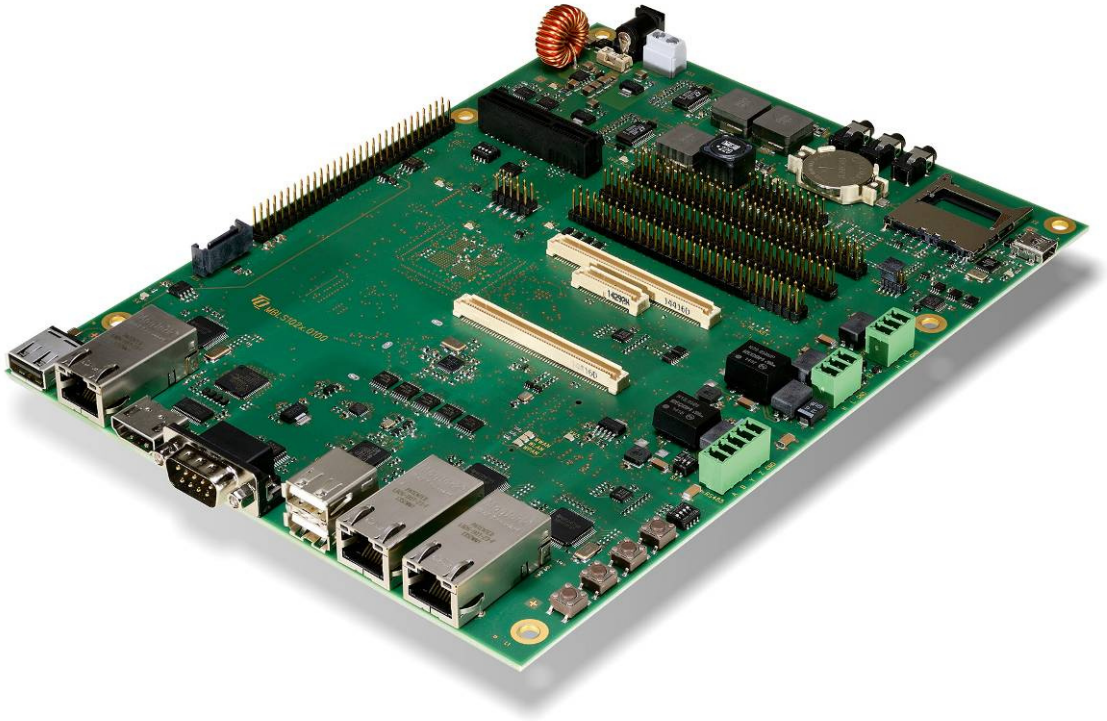

TABLE OF CONTENTS

1. ABOUT THIS MANUAL 1
1.1 Copyright and licence expenses 1
1.2 Registered trademarks 1
1.3 Disclaimer 1
1.4 Imprint 1
1.5 Tips on safety 1
1.6 Symbols and typographic conventions 2
1.7 Handling and ESD tips 2
1.8 Naming of signals 3
1.9 Further applicable documents / presumed knowledge 3
2. BRIEF DESCRIPTION 4
3. TECHNICAL DATA 4
3.1 System architecture and functionality 4
3.1.1 Block diagram 4
3.1.2 Functionality 4
4. ELECTRONICS 5
4.1 System components 6
4.1.1 Power supply 6
4.1.2 Power sequencing 6
4.1.3 Voltage monitoring 6
4.1.4 CPLD 7
4.2 Communication interfaces 8
4.2.1 USB 8
4.2.2 Ethernet 1000BASE-T 8
4.2.3 CAN 8
4.2.4 RS-485 8
4.2.5 RS-232 8
4.2.6 2D-ACE (display interface) 9
4.2.6.1 24 bit RGB 9
4.2.6.2 HDMI 9
4.2.6.3 LVDS 9
4.2.7 I^2C 9
4.2.8 PWM 10
4.2.9 SerDes 10
4.2.10 Audio 10
4.2.11 SD card 10
4.2.12 SATA 10
4.2.13 PCIe 10
4.2.14 Mini-PCIe 10
4.2.15 SPI 11
4.2.16 WLAN / WiFi 11
4.2.17 JTAG 11
4.2.18 OpenSDA 11
4.2.19 Headers X1 to X4 12
4.3 Demultiplexing on MBLS102xA 17
4.4 Reset generation 18
4.5 Diagnose- and user interfaces 18
4.5.1 LEDs 18
4.5.2 Push buttons 19
4.5.3 DIP switches 19
4.5.4 GPIO 20
4.5.5 Boot-Mode configuration 20
4.6 TQMLS102xA connectors 21
4.7 Pinout of connectors to TQMLS102xA 22

TABLE OF CONTENTS (continued)

5.	SOFTWARE-SPECIFICATION	25
6.	MECHANICS	25
6.1	Dimensions	25
6.2	Housing	26
6.3	Thermal management	26
6.4	Assembly top	26
6.5	Assembly bottom	27
7.	SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS	28
7.1	EMC	28
7.2	ESD	28
7.3	Operational safety and personal security	28
8.	CLIMATIC AND OPERATIONAL CONDITIONS	28
8.1	Protection against external effects	28
8.2	Reliability and service life	28
9.	ENVIRONMENT PROTECTION	29
9.1	RoHS	29
9.2	WEEE	29
9.3	REACH	29
9.4	EuP	29
9.5	Packaging	29
9.6	Batteries	29
9.6.1	General notes	29
9.6.2	Lithium batteries	29
9.7	Other entries	29
10.	APPENDIX	30
10.1	Acronyms and definitions	30
10.2	References	32

TABLE DIRECTORY

Table 1: Terms and Conventions 2
Table 2 Supply voltages undervoltage detection 6
Table 3 USB Ports 8
Table 4: I^2C devices, address mapping 9
Table 5: Configuration of SerDes lanes 10
Table 6: Headers, component 12
Table 7: Pinout header 1, X17 13
Table 8: Pinout header 2, X16 14
Table 9: Pinout header 3, X18 15
Table 10: Pinout header 4, X39 16
Table 11: Functions of DIP switch S9 17
Table 12: LEDs 18
Table 13: Push buttons 19
Table 14: Termination RS-485 19
Table 15: Termination CAN 19
Table 16: Boot-source and GPIO 19
Table 17: GPIO assignment 20
Table 18: Boot-source 20
Table 19: Suitable carrier board mating connectors 21
Table 20: Pinout connector X36 (X1 on TQMLS102xA) 22
Table 21: Pinout connector X7 (X2 on TQMLS102xA) 23
Table 22: Pinout connector X22 (X3 on TQMLS102xA) 24
Table 23: Climatic and operational conditions MBLS102xA 28
Table 24: Acronyms 30
Table 25: Further applicable documents 32

ILLUSTRATION DIRECTORY

Illustration 1: Block diagram MBLS102xA, simple 4
Illustration 2: Block diagram MBLS102xA, detailed 5
Illustration 3: Block diagram CPLD functional description 7
Illustration 4: UART1 Or'ed 11
Illustration 5: Position of headers X1 to X4 12
Illustration 6: Demultiplexing on MBLS102xA 17
Illustration 7: Reset structure 18
Illustration 8: MBLS102xA dimensions 25
Illustration 9: Component placement top 26
Illustration 10: Component placement bottom 27

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBLS102xA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- Circuit diagram of MBLS102xA
- CPU Data Sheet LS102xA
- User's Manual of TQMLS102xA
- Documentation of boot loader U-Boot (http://www.denx.de/wiki/U-Boot/Documentation)
- Documentation of PTXdist (http://www.ptxdist.de)

2. BRIEF DESCRIPTION

The MBLS102xA is designed as a carrier board for the TQMLS102xA.

All of the TQMLS102xA interfaces are available on the MBLS102xA. The user can evaluate the characteristics of the LS102xA CPU and therefore the software development for a TQMLS102xA project can start immediately.

The MBLS102xA supports all LS102xA-based TQ-Modules with the NXP CPUs LS1020xA, LS1021xA, and LS1022xA.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 Block diagram

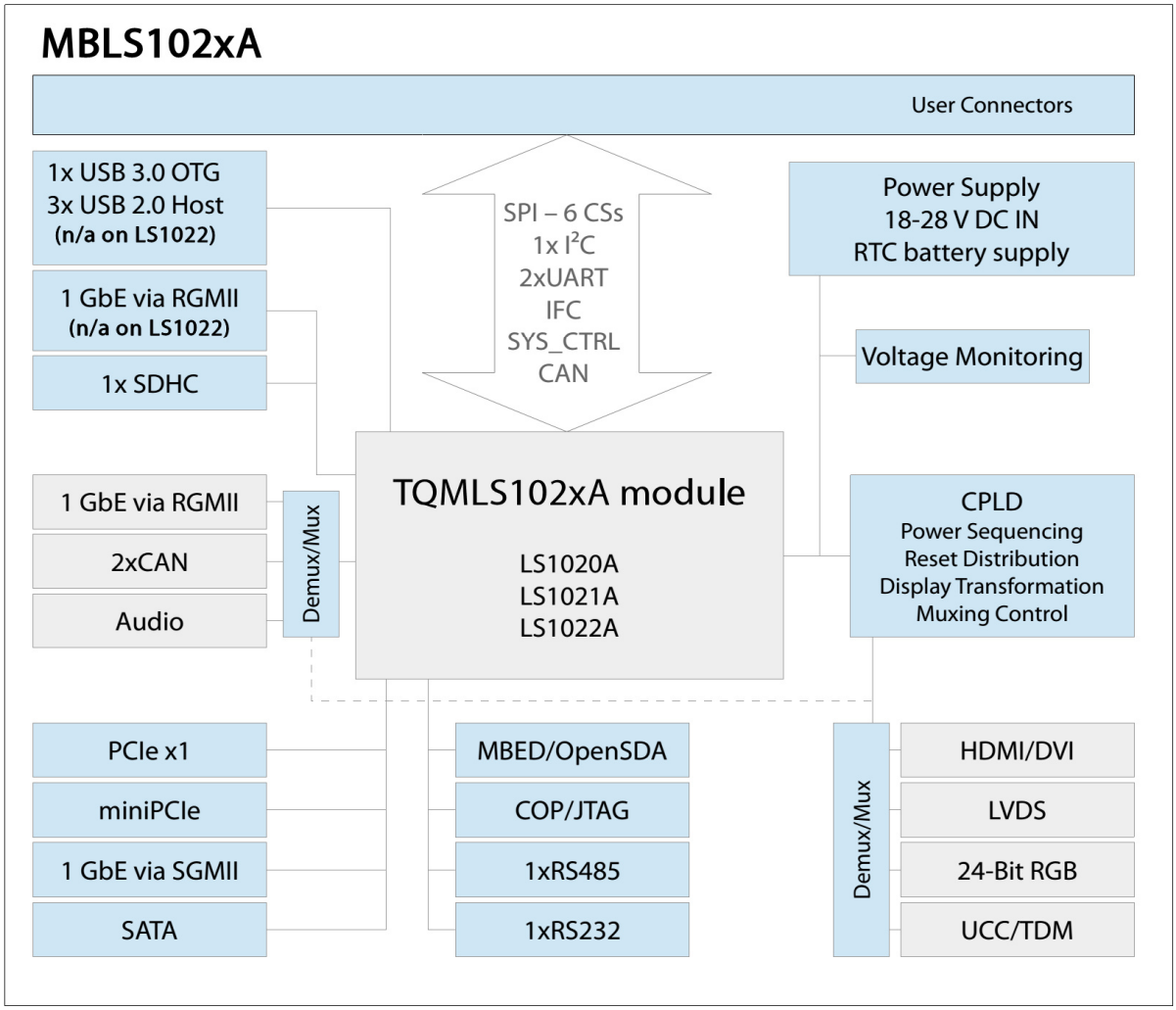


Illustration 1: Block diagram MBLS102xA, simple

3.1.2 Functionality

Core of the system is the CPU module based on an NXP LS102xA CPU, plugged in the MBLS102xA.

The MBLS102xA contains all peripheral components and provides, in addition to the standard communication interfaces like USB, Ethernet, RS-232, RS-485, LVDS etc. All other available signals of the MBLS102xA are routed to 2.54 mm standard headers.

4. ELECTRONICS

The TQ-Module TQMLS102xA with the LS102xA CPU is the central system component. It provides DDR3L-SDRAM, eMMC, NOR flash and EEPROM memory. All voltages required by the TQMLS102xA are derived from the supply voltage of 3.3 V.

The available signals are routed to two connectors on the MBLS102xA. More detailed information is to be taken from the accompanying User's Manual of the TQMLS102xA.

The boot behaviour of the TQMLS102xA can be customised. The required boot-mode configuration can be set with DIP switches, see section 4.5.5.

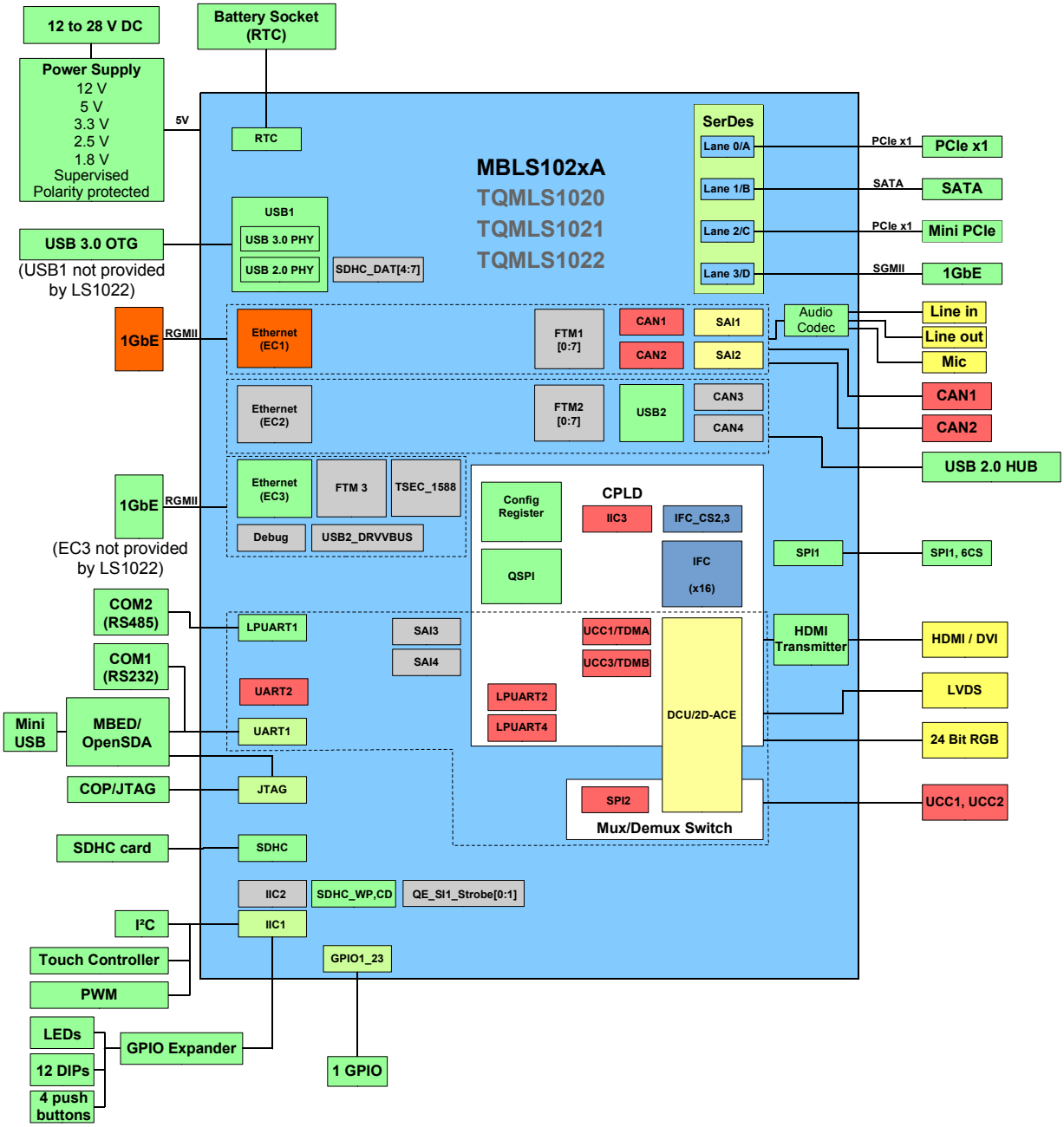


Illustration 2: Block diagram MBLS102xA, detailed

4.1 System components

4.1.1 Power supply

The MBLS102xA has to be supplied with 18 V to 28 V at X33 or X34.

4.1.2 Power sequencing

1 After applying the supply voltage to the MBLS102xA at first the VCC5V regulator is activated.
The 3.3 V supply for the CPLD is generated with an LDO from the VCC5V_SOURCE supply and hence initiates the Power-Up of the CPLD. In this state weak pull-downs (10 kΩ to 100 kΩ) are active at all I/O pins of the CPLD.

2 As soon as the CPLD is configured, the module reset (RESIN#) is activated, the multiplexing (MUX_SEL[a:b]) is defined and L1VDD is selected.

3 Then all voltage regulators are activated. Because the VCC5V_SOURCE regulator already works, the VCC5V net of the remaining components is switched on with MOSFETs.

4 Afterwards the PMIC is activated (POWER_EN).

5 Finally, the system is dismissed from reset.

4.1.3 Voltage monitoring

The following voltages are monitored for undervoltage.

Table 2 Supply voltages undervoltage detection

Voltage Name	Nominal Voltage [V]	Permitted[1] [V]	DC/DC Nominal[2] [V]	Actual threshold [V]
VCC5V_SOURCE	5.0	4.45 – 5.25	4.9 – 5.1	4.733 – 4.824
VCC3V3	3.3	3.135 – 3.465	3.20 – 3.40	3.139 – 3.190
VCC3V3_PCIE	3.3	3.135 – 3.465	3.20 – 3.40	3.139 – 3.190
VCC2V5	2.5	2.375 – 2.625	2.45 – 2.55	2.386 – 2.425
VCC1V8	1.8	1.70 – 1.90	1.764 – 1.836	1.712 – 1.740
VCC1V5	1.5	1.425 – 1.575	1.470 – 1.530	1.436 – 1.460
VCC1V2	1.2	1.14 – 1.26	1.176 – 1.224	1.143 – 1.165
VCC1V1	1.1	1.045 – 1.155	1.078 – 1.122	1.060 – 1.081

If VCC5V_SOURCE or VCC3V3 drop below the respective specified voltage (actual threshold), PWRGD_2 signals this to the CPLD and a power-cycle is carried out.

If VCC2V5, VCC1V8, VCC1V2, or VCC1V1 drop below the respective specified voltage (actual threshold), PWRGD_1 signals this to the CPLD, the system is held in reset, until the voltages are again within the specified range.

If VCC3V3_PCIE or VCC1V5 drop below the respective specified voltage (actual threshold), PWRGD_PCIE signals this to the CPLD, the MBLS102xA is held in reset, until the voltages are again within the specified range.

1: According to specification of respective device.
2: Voltage range at the output of the regulator including resistor tolerances.

4.1.4 CPLD

Das CPLD (D41) on the MBLS102xA has the following functions:

- Power sequencing (see 4.1.2)
- Reset distribution (see 4.4)
- Demultiplexing (see 4.3)
- LCD interface transformation (see 4.2.6)

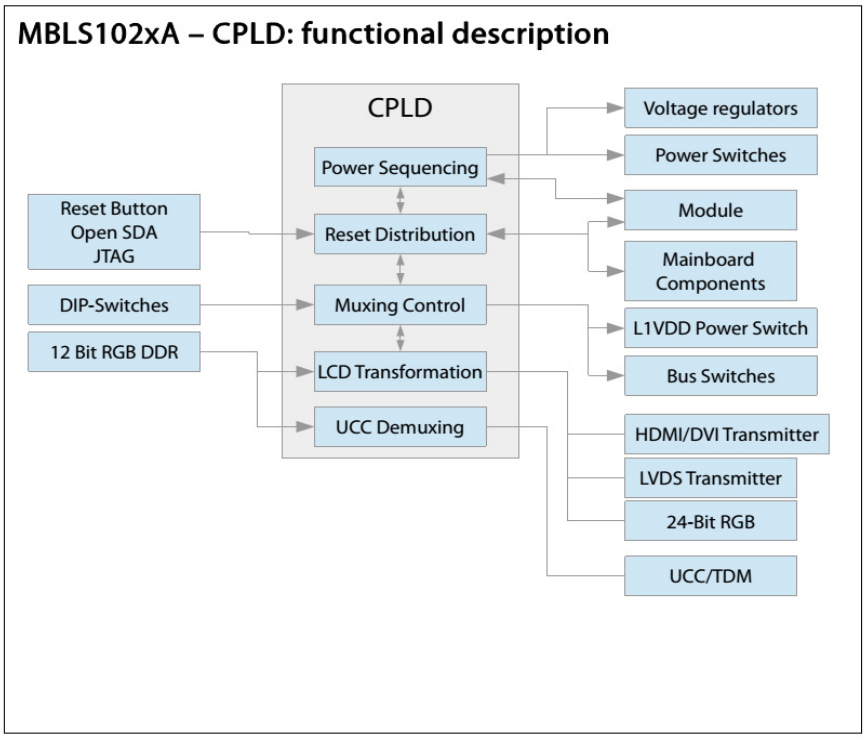


Illustration 3: Block diagram CPLD functional description

The CPLD firmware can be updated via JTAG connector X38 using a Lattice programmer.

4.2 Communication interfaces

4.2.1 USB

Both USB modules of the LS1021A are available. USB1 is routed to X40 (Micro USB 3.0) as a USB 3.0- and OTG interface.

A PHY, as well as a hub is connected to USB2. The MBLS102xA offers therefore up to seven USB 2.0 hosts ports.

The 5 V supply for the USB ports is implemented by power distribution switches. The power distribution switches used provide current monitoring and can switch-off the bus voltage at overload and/or overheating.

USB2 host 1 and 2 are routed to a dual USB type-A receptacle (X3).

The USB2 host 3 is routed to a single type-A receptacle (X4).

USB2 host 4 is available at header X17 and USB2 host 6 is available at header X16 on the Starterkit.

USB2 host 5 is available at the LVDS-CMD connector X32.

USB2 host 7 is routed to the Mini PCIe connector X24.

Table 3 USB Ports

USB Port	Type	Connector
USB1	USB 3.0 SS OTG	X40, micro B USB 3.0
USB2_H1	USB 2.0 High-Speed Host	X3, type-A, Dual (1)
USB2_H2	USB 2.0 High-Speed Host	X3, type-A, Dual (2)
USB2_H3	USB 2.0 High-Speed Host	X4, type-A
USB2_H4	USB 2.0 High-Speed Host	X17, RM 2.54
USB2_H5	USB 2.0 High-Speed Host	X32, LVDS CMD connector
USB2_H6	USB 2.0 High-Speed Host	X16, RM 2.54
USB2_H7	USB 2.0 High-Speed Host	X24, Mini-PCIe

4.2.2 Ethernet 1000BASE-T

Up to three Gigabit-Ethernet interfaces are available: Two via RGMII, one via SGMII.

All interfaces are implemented using the TI PHY DP83867IS.

4.2.3 CAN

Both CAN interfaces of the TQMLS102xA (CAN1, CAN2) are available at the 3-pin Phoenix connectors X27 and X28.
Both interfaces are galvanically separated (1 kV functional isolation).

4.2.4 RS-485

The LPUART1 interface of the TQMLS102xA is routed to a RS-485 transceiver (D6, SP491), which provides the RS-485 signals at the 5-pin Phoenix connector X1. The RS-485 interface is galvanically separated (1 kV functional isolation).

4.2.5 RS-232

The UART1 interface of the TQMLS102xA is routed to a RS-232 transceiver (D7, SP3222E), which provides the RS-232 signals at the 9-pin D-Sub connector X5. The interface is used to output debug information.

UART1 is also used by the OpenSDA interface.

4.2.6 2D-ACE (display interface)

The 2D-ACE display interface of the LS1021A can output 24 bit RGB signals on 12 data lines via DDR. Since many displays or transmitters do not support these 12 bit DDR signals, the CPLD (D41) converts the signals from 12 bit DDR to 24 bit SDR. Thus a 24 bit RGB compliant display interface is available. This interface is output threefold by the CPLD, to allow the operation of different displays.

4.2.6.1 24 bit RGB

The 24 bit RGB interface, control signals for backlight, turning on, contrast (PWM), a 4 Wire air interface, as well as a reset signal are available at header X17. TQ-Systems GmbH can provide suitable displays. Please ask your local sales representative.

4.2.6.2 HDMI

The HDMI interface is routed to a HDMI receptacle where a monitor can be connected. The HDMI transmitter SiI9022ACNU (D15) receives the 24 bit RGB signals from the CPLD. The transmitter is protected against ESD by a HDMI port protector (N12).

Attention: I²C1 address conflict	
	Currently the HDMI interface does not work with most displays. The EDID of most monitors is at address 0x50, which is already taken by the EEPROM on the TQMLS102xA.

4.2.6.3 LVDS

The signals of the LVDS-Transmitter SN75LVDS83BDGGR (D12) are routed to the 30-pin FFC plug connector X10, where an LVDS display can be connected. TQ-Systems GmbH can provide suitable displays. Please ask your local sales representative.

4.2.7 I²C

Only the IIC1 bus is used.

Table 4: I²C devices, address mapping

Function	Device	Address	Remark
Audio	N10, TLV320AIC3204RHBT	001 1000	
HDMI	D15, SiI9022A		CI2CA = High
	TPI Programming	0111 0110	
	CPI Programming	1100 0100	
	SiI9020 compatible registers	0111 0110	
	SiI9020 compatible registers	0111 1010	
	Monitors	(various)	Most of the monitors available: 0x50
GPIO Expander 1	D35, PCA9554BS	0010 0000	A0: 10 kΩ ↓, A1: 10 kΩ ↓, A2: 10 kΩ ↓
GPIO Expander 2	D39, PCA9554BS	0010 0001	A0: 10 kΩ ↑, A1: 10 kΩ ↓, A2: 10 kΩ ↓
GPIO Expander 3	D63, PCA9554BS	0010 0010	A0: 10 kΩ ↓, A1: 10 kΩ ↑, A2: 10 kΩ ↓
PWM LED Dimmer	D42, PCA9530D	0110 0000	A0: tied to DGND
Touch-Controller	D34, ST STMPE811	1000 0010	A0: 10 kΩ ↓
Mini PCIe Socket	–	–	
PCIe Socket	–	–	Optional
Starterkit header	–	–	
Clock-Generator	–	110 1000	SMBUS, optional
RTC	PCF85063	101 0001	On TQMLS102xA
Temperature sensor	SA56004EDP	100 1100	On TQMLS102xA
EEPROM	M24C64	101 0000 101 1000	On TQMLS102xA
PMC	MKL05Z8	001 0001	On TQMLS102xA
PMIC	34VR500	000 0100	On TQMLS102xA
Supervisor	ADM1069	100 1111	On TQMLS102xA

4.2.8 PWM

PWM signals are generated with a 2 bit I²C LED dimmer (D42).
Contrast and brightness of a display can be controlled by PWM0 and PWM1.

4.2.9 SerDes

Only the configuration SRDS_PRTCL_S1[128:135] = 70 is supported. The SerDes lanes are configured as follows:

Table 5: Configuration of SerDes lanes

Type	Name	Function
Lane A	SD1_RX0_P	PCIe1 (×1)
	SD1_RX0_N	
	SD1_TX0_P	
	SD1_TX0_N	
Lane B	SD1_RX1_P	SATA1
	SD1_RX1_N	
	SD1_TX1_P	
	SD1_TX1_N	
Lane C	SD1_RX2_P	PCIe2 (×1)
	SD1_RX2_N	
	SD1_TX2_P	
	SD1_TX2_N	
Lane D	SD1_RX3_P	SGMII
	SD1_RX3_N	
	SD1_TX3_P	
	SD1_TX3_N	

4.2.10 Audio

The audio-codec TLV320AIC is available for audio input and output. The codec is routed to the SAI1 interface of the LS102xA.
The MBLS102xA provides a stereo line-in, a stereo line-out and a microphone input.
It is possible to select line out or headphone by assembly option.

4.2.11 SD card

The SDHC interface is routed to the SD/MMC card connector (X2) on the MBLS102xA.
All signals and voltages at the connector are protected against ESD.
S3-1 has to be set to “ON” to boot the TQMLS102xA from SD card.

4.2.12 SATA

The SATA interface of the LS102xA is routed via SerDes lane B (SATA1) to a 7-pin SATA connector (X29).
Connected SATA devices require a separate power supply. The data lines are protected against ESD.

4.2.13 PCIe

SerDes lane A of the TQMLS102xA is routed to a PCIe ×4 connector. IIC1, Reset and JTAG are also routed to the connector.

4.2.14 Mini-PCIe

A Mini PCIe interface is provided on the MBLS102xA. It offers all signals (PCIe lane, I²C, USB) and permits the usage of various Mini PCIe devices. A SIM card holder is provided to connect a UMTS/GSM modem.

4.2.15 SPI

The SPI interface is available at X18 if the Reset Configuration Word (RCW) of the TQMLS102xA is set accordingly.

4.2.16 WLAN / WiFi

WLAN can be used with a suitable Mini PCIe card in connector X24.

4.2.17 JTAG

The JTAG interface of the TQMLS102xA is routed to a 20-pin header (X37, ARM® 20-pin interface).
All signal lines use O1VDD (1.8 V) of the TQMLS102xA as a reference.
Programming and debugging via JTAG is possible using a Lauterbach TRACE32 debugger (e.g. LA-7707 plus LA-7843X).
The JTAG interface is not protected against ESD.

4.2.18 OpenSDA

The OpenSDA interface is provided by the Kinetis µC (D13, MK20DX128VFM5) as a programming interface for the TQMLS102xA. Through the OpenSDA interface, the CPU (or the TQMLS102xA) can be programmed or debugged using the USB interface of the Kinetis µC. The µC is connected to the CPU via JTAG and UART1.
The OpenSDA interface shares the UART1 interface with the RS-232 transceiver and the JTAG interface with a debugger connected at the JTAG connector X37. Accordingly the console can only be accessed alternatively via UART1 by the RS-232 transceiver or the OpenSDA interface at the Mini-USB connector X43.

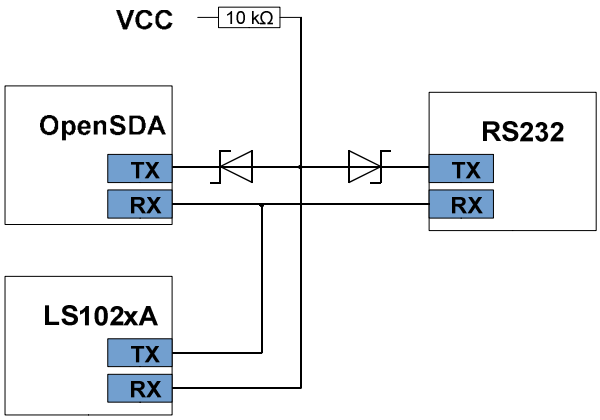


Illustration 4: UART1 Or'ed

The GND_DETECT# signal at X37 pin 8 detects a debugger connected at X37 to avoid simultaneous access of the JTAG interface by the CPU and the Kinetis µC. In this case the JTAG interface of the Kinetis µC is deactivated.
Different Debug-/Programming applications can be used. More information can be found on https://developer.mbed.org/.
Only console was tested.

4.2.19 Headers X1 to X4

All unused as well as other signals are routed to the headers X1 to X4 on the MBLS102xA, to permit a comprehensive evaluation of all features of the MBLS102xA. All headers are 60-pin with 2.54 mm pitch.

The headers are positioned in such a way, to easily plug in adaptor boards which additional electronics and connectors.

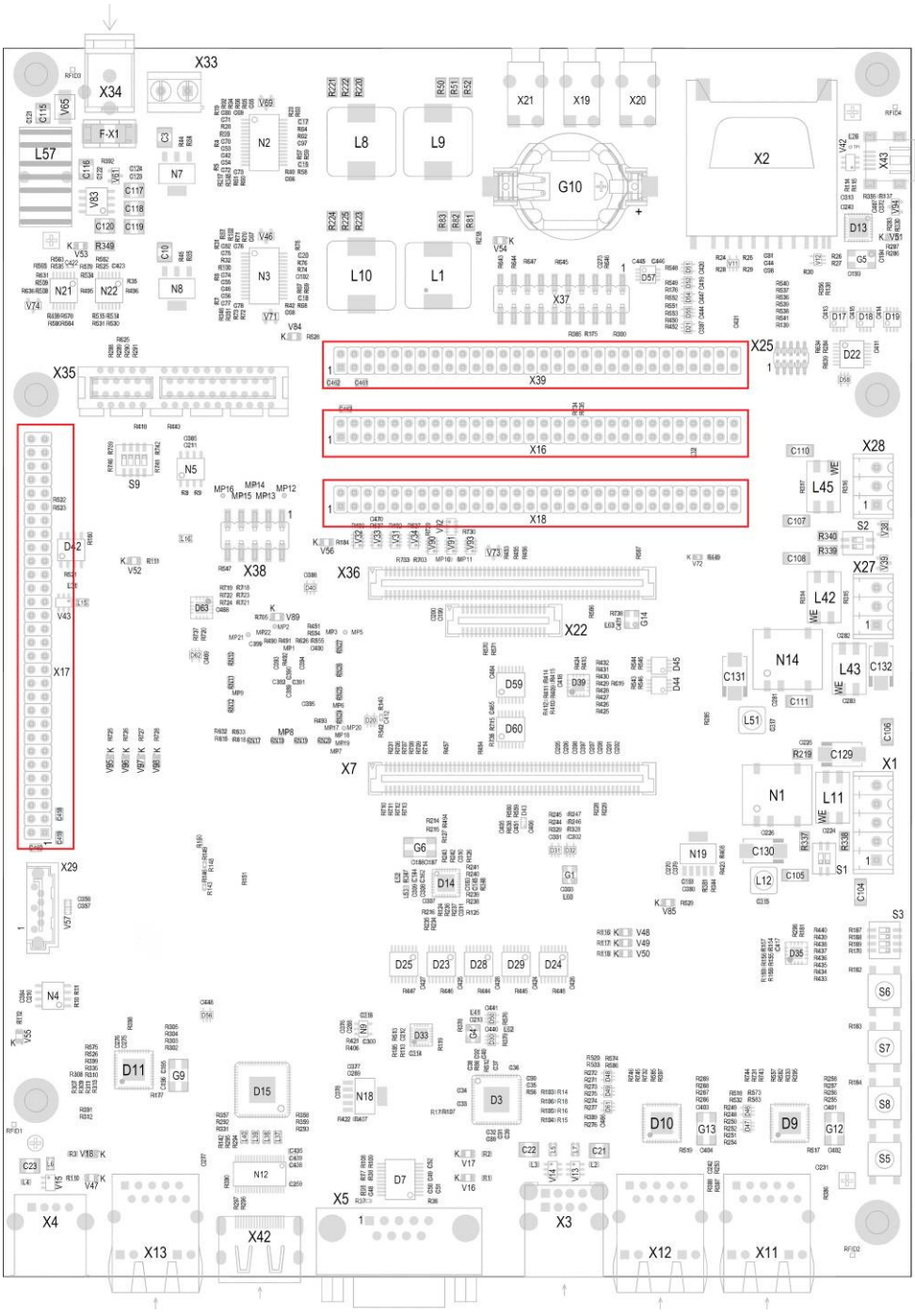


Illustration 5: Position of headers X1 to X4

Table 6: Headers, component

Manufacturer / Number	Description	Package
Fischer Elektronik / SL 22 124 60 G	Header, 2.54 mm pitch, 2 × 30 pins	THT60

Table 7: Pinout header 1, X17

Pin	Name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	111 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
2	VCC3V3	VCC3V3	P	11 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
3	VCC5V	VCC5V	P	11 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
4	VCC3V3	VCC3V3	P	11 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
5	DGND	DGND	P	
6	DGND	DGND	P	
7	LCD_RGB_CLK_OUT	LCD_RGB_CLK_OUT	O	
8	LCD_RGB_DE	LCD_RGB_DE	O	
9	LCD_RGB_HSYNC	LCD_RGB_HSYNC	O	
10	–	LCD_RGB_D11	O	
11	–	LCD_RGB_VSYNC	O	
12	LCD_RGB_D13	LCD_RGB_D13	O	
13	LCD_RGB_D17	LCD_RGB_D17	O	
14	LCD_RGB_D15	LCD_RGB_D15	O	
15	LCD_RGB_D12	LCD_RGB_D12	O	
16	LCD_RGB_D6	LCD_RGB_D6	O	
17	LCD_RGB_D14	LCD_RGB_D14	O	
18	LCD_RGB_D8	LCD_RGB_D8	O	
19	LCD_RGB_D5	LCD_RGB_D5	O	
20	LCD_RGB_D10	LCD_RGB_D10	O	
21	LCD_RGB_D7	LCD_RGB_D7	O	
22	LCD_RGB_D0	LCD_RGB_D0	O	
23	LCD_RGB_D9	LCD_RGB_D9	O	
24	LCD_RGB_D2	LCD_RGB_D2	O	
25	LCD_RGB_D16	LCD_RGB_D16	O	
26	LCD_RGB_D4	LCD_RGB_D4	O	
27	LCD_RGB_D1	LCD_RGB_D1	O	
28	LCD_RGB_D23	LCD_RGB_D23	O	
29	LCD_RGB_D3	LCD_RGB_D3	O	
30	LCD_RGB_D20	LCD_RGB_D20	O	
31	LCD_RGB_D22	LCD_RGB_D22	O	
32	LCD_RGB_D19	LCD_RGB_D19	O	
33	LCD_RGB_D21	LCD_RGB_D21	O	
34	USB	USB_H4_VBUS	P	100 µF to DGND + EMI filter
35	24 Bit RGB	LCD_RGB_D18	O	
36	USB	USB_H4_D_N	I/O	Common mode choke in series
37	DGND	DGND	P	
38	USB	USB_H4_D_P	I/O	Common mode choke in series
39	I2C1	IIC1_SCL	O	
40	DGND	DGND	P	
41	I2C1	IIC1_SDA	I/O	
42	NC	NC	O	
43	NC	NC	O	
44	NC	NC	I	
45	NC	NC	O	
46	NC	NC	O	
47	–	EXT_TOUCH_INT#	–	
48	DGND	DGND	P	
49	LCD	LCD_PWR_EN	O	10 kΩ ↑ to 3.3 V is assembled on MBLS102xA
50	LCD	LCD_BLT_EN	O	10 kΩ ↑ to 3.3 V is assembled on MBLS102xA, 10 kΩ ↓ is optional
51	LCD	STKT_RST#	O	
52	LCD	PWM0	O	
53	DGND	DGND	P	
54	DGND	DGND	P	
55	–	TOUCH_Y+	–	
56	–	TOUCH_X+	–	
57	–	TOUCH_Y–	–	
58	–	TOUCH_X–	–	
59	DGND	DGND	P	
60	DGND	DGND	P	

Table 8: Pinout header 2, X16

Pin	Name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	111 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
2	VCC3V3_PCIE	VCC3V3_PCIE	P	11 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
3	VCC5V	VCC5V	P	11 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
4	DGND	DGND	P	
5	DGND	DGND	P	
6	TA_BB_RTC	TA_BB_RTC	I	
7	RTC_INT#	RTC_INT#	I	
8	TA_BB_TMP_DETECT#	TA_BB_TMP_DETECT#	I	
9	RTC_CLK_OUT	RTC_CLK_OUT	O	
10	TA_PROG_SFP	TA_PROG_SFP	I	
11	POWER_STBY	POWER_STBY	I	
12	TA_TMP_DETECT#	TA_TMP_DETECT#	I	
13	TEMP_CRIT_OUT#	TEMP_CRIT_OUT#	P	
14	DGND	DGND	P	
15	TEMP_ALERT#	TEMP_ALERT#	P	
16	DGND	DGND	P	
17	DGND	DGND	I	
18	NC	NC		
19	NC	NC		
20	SWD_DIO (TQMLS102xA Rev. 01xx)	SWD_DIO (TQMLS102xA Rev. 01xx)	I	
	EVT1# (TQMLS102xA Rev. 02xx)	EVT1# (TQMLS102xA Rev. 02xx)	I	
21	CLK_OE	CLK_OE	O	
22	SWD_CLK (TQMLS102xA Rev. 01xx)	SWD_CLK (TQMLS102xA Rev. 01xx)	I	
	EVT0# (TQMLS102xA Rev. 02xx)	EVT0# (TQMLS102xA Rev. 02xx)	I	
23	DGND	DGND	P	
24	DGND	DGND	P	
25	TEST_SEL#	TEST_SEL#	I	
26	CAN1_TX	CAN1_TX	O	
27	NC	NC		
28	CAN1_RX	CAN1_RX	I	
29	ASLEEP	ASLEEP	O	
30	CAN1_TX	CAN1_TX	O	
31	EEPROM_WC#	EEPROM_WC#	I	
32	CAN2_RX	CAN2_RX	I	
33	DGND	DGND	P	
34	DGND	DGND	P	
35	NC	NC		
36	NC (TQMLS102xA Rev. 01xx)	NC (TQMLS102xA Rev. 01xx)		
	IIC2_SDA (TQMLS102xA Rev. 02xx)	IIC2_SDA (TQMLS102xA Rev. 02xx)		R734 is not assembled, see MBLS102xA schematics, page 12
37	NC	NC		
38	NC (TQMLS102xA Rev. 01xx)	NC (TQMLS102xA Rev. 01xx)		
	IIC2_SCL (TQMLS102xA Rev. 02xx)	IIC2_SCL (TQMLS102xA Rev. 02xx)		R735 is not assembled, see MBLS102xA schematics, page 12
39	DGND	DGND	P	
40	DGND	DGND	P	
41	UART1_RX_1	UART1_RX_1	I	
42	UART1_TX	UART1_TX	O	
43	DGND	DGND	P	
44	DGND	DGND	P	
45	LPUART1_SIN	LPUART1_SIN	I	
46	LPUART1_SOUT	LPUART1_SOUT	O	
47	LPUART1_RTS#	LPUART1_RTS#	I	
48	LPUART1_CTS#	LPUART1_CTS#	O	
49	NC	NC		
50	DGND	DGND	P	
51	DGND	DGND	P	
52	SDHC_DAT4	SDHC_DAT4	I/O	
53	USB_H6_VBUS	USB_H6_VBUS	P	
54	SDHC_DAT5	SDHC_DAT5	I/O	
55	USB2_H6_D_N	USB2_H6_D_N	I/O	
56	USB1_DRVVBUS	USB1_DRVVBUS	I	
57	USB2_H6_D_P	USB2_H6_D_P	I/O	
58	USB1_PWRFAULT	USB1_PWRFAULT	O	
59	DGND	DGND	P	
60	DGND	DGND	P	

Table 9: Pinout header 3, X18

Pin	Name	Signal	Dir.	Remark
1	IFC_AD00	IFC_AD00	P	
2	IFC_AVD	IFC_AVD	P	
3	IFC_AD01	IFC_AD01	P	
4	IFC_BTCL	IFC_BTCL	P	
5	IFC_AD02	IFC_AD02	P	
6	IFC_TE/CFG_IFC_TE	IFC_TE/CFG_IFC_TE	O	
7	IFC_AD03	IFC_AD03	I	Pin not configured in BSP
8	DGND	DGND	I	
9	DGND	DGND	P	
10	IFC_CS0#	IFC_CS0#	P	
11	IFC_AD04	IFC_AD04	I	
12	IFC_OE#	IFC_OE#	I	
13	IFC_AD05	IFC_AD05	I	
14	IFC_RB0#	IFC_RB0#	I	
15	IFC_AD06	IFC_AD06		
16	IFC_WE0#	IFC_WE0#	I	
17	IFC_AD07	IFC_AD07	I	
18	IFC_WP0#	IFC_WP0#	P	
19	DGND	DGND	I	
20	IFC_CLE	IFC_CLE	I	
21	IFC_AD14	IFC_AD14	I	
22	IFC_CLK1	IFC_CLK1	I	
23	IFC_AD15	IFC_AD15	I	
24	DGND	DGND	I	
25	IFC_NDDDR_CLK	IFC_NDDDR_CLK	I	
26	IFC_CLK0	IFC_CLK0	I	
27	DGND	DGND	P	
28	IFC_NDDQS	IFC_NDDQS	P	
29	SPI1_PCS2/IFC_AD9	SPI1_PCS2/IFC_AD9	I	
30	DGND	DGND	I	
31	SPI1_PCS3/IFC_AD10	SPI1_PCS3/IFC_AD10	I	
32	NC	NC	I	
33	SPI1_PCS4/IFC_AD10	SPI1_PCS4/IFC_AD10	I	
34	SPI1_PCS5/IFC_AD12	SPI1_PCS5/IFC_AD12	I	
35	SPI1_SCK/IFC_CS2#	SPI1_SCK/IFC_CS2#	I	
36	SPI1_SIN/IFC_RB1#	SPI1_SIN/IFC_RB1#	I	
37	SPI1_PCS0/IFC_CS1#	SPI1_PCS0/IFC_CS1#	I	
38	SPI1_SOUT/IFC_AD13	SPI1_SOUT/IFC_AD13	I	
39	DGND	DGND	I	
40	SPI1_PCS1/IFC_AD8	SPI1_PCS1/IFC_AD8	I	
41	DGND	DGND	I	
42	DGND	DGND	I	
43	QSPI_A_CS0	QSPI_A_CS0	I	
44	QSPI_A_IO0	QSPI_A_IO0	I	
45	QSPI_A_CS1	QSPI_A_CS1	P	
46	QSPI_A_IO1	QSPI_A_IO1	P	
47	QSPI_A_DQS	QSPI_A_DQS	I	
48	QSPI_A_IO2	QSPI_A_IO2	–	
49	QSPI_B_IO0	QSPI_B_IO0	O	
50	QSPI_A_IO3	QSPI_A_IO3	O	
51	QSPI_B_IO1	QSPI_B_IO1	O	
52	QSPI_B_CS0	QSPI_B_CS0	O	
53	QSPI_B_IO2	QSPI_B_IO2	I	
54	QSPI_B_CS1	QSPI_B_CS1	P	
55	QSPI_B_IO3	QSPI_B_IO3	P	
56	QSPI_B_DQS	QSPI_B_DQS	O	
57	DGND	DGND	P	
58	DGND	DGND	P	
59	QSPI_B_CK	QSPI_B_CK	P	
60	QSPI_A_CK	QSPI_A_CK	P	

Table 10: Pinout header 4, X39

Pin	Name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	111 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
2	VCC3V3_PCIE	VCC3V3_PCIE	P	11 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
3	VCC5V	VCC5V	P	11 µF to DGND (I_{max} = 1 A minus the current drawn from the headers)
4	DGND	DGND	P	
5	DGND	DGND	P	
6	PWM_1	PWM_1	O	
7	TDMA_RXD	TDMA_RXD	I	Pin not configured in BSP
8	DGND	DGND	I	
9	TDMA_RSYNC	TDMA_RSYNC	P	
10	GPIO_ADC_I2C1_1	GPIO_ADC_I2C1_1	P	
11	TDMA_TXD	TDMA_TXD	I	
12	GPIO_ADC_I2C1_2	GPIO_ADC_I2C1_2	I	
13	TDMA_TSYNC	TDMA_TSYNC	I	
14	GPIO_ADC_I2C1_3	GPIO_ADC_I2C1_3	I	
15	TDMA_RQ	TDMA_RQ		
16	GPIO_ADC_I2C1_4	GPIO_ADC_I2C1_4	I	
17	DGND	DGND	I	
18	DGND	DGND	P	
19	CLK9	CLK9	I	
20	EVT0 (TQMLS102xA Rev. 01xx)#	EVT0# (TQMLS102xA Rev. 01xx)	I	
	SWD_CLK (TQMLS102xA Rev. 02xx)	SWD_CLK (TQMLS102xA Rev. 02xx)	I	
21	CLK10	CLK10	I	
22	EVT1# (TQMLS102xA Rev. 01xx)	EVT1# (TQMLS102xA Rev. 01xx)	I	
	SWD_DIO (TQMLS102xA Rev. 02xx)	SWD_DIO (TQMLS102xA Rev. 02xx)	I	
23	DGND	DGND	I	
24	EVT2#	EVT2#	I	
25	TDMB_RXD	TDMB_RXD	I	
26	EVT3#	EVT3#	I	
27	TDMB_RSYNC	TDMB_RSYNC	P	
28	EVT4#	EVT4#	P	
29	TDMB_TXD	TDMB_TXD	I	
30	EVT9#_GPIO2_24	EVT9#_GPIO2_24	I	
31	TDMB_TSYNC	TDMB_TSYNC	I	
32	GPIO1_14	GPIO1_14	I	
33	TDMB_RQ	TDMB_RQ	I	
34	DGND	DGND	I	
35	DGND	DGND	I	
36	GPIO_1	GPIO_1	I	
37	CLK11	CLK11	I	
38	IRQ0	IRQ0	I	
39	CLK12	CLK12	I	
40	IRQ1	IRQ1	I	
41	DGND	DGND	I	
42	IRQ2	IRQ2	I	
43	EXT_AUDIO_MCLK2	EXT_AUDIO_MCLK2	I	
44	DGND	DGND	I	
45	DGND	DGND	P	
46	SGMII_PHY_GPIO1	SGMII_PHY_GPIO1	P	
47	SAI2_RX_DATA	SAI2_RX_DATA	I	
48	SGMII_PHY_GPIO2	SGMII_PHY_GPIO2	–	
49	SAI2_RX_BCLK	SAI2_RX_BCLK	O	
50	DGND	DGND	O	
51	SAI2_RX_SYNC	SAI2_RX_SYNC	O	
52	EC1_PHY_GPIO1	EC1_PHY_GPIO1	O	
53	NC	NC	I	
54	EC1_PHY_GPIO2	EC1_PHY_GPIO2	P	
55	NC	NC	P	
56	EC3_PHY_GPIO1	EC3_PHY_GPIO1	O	
57	NC	NC	P	
58	EC3_PHY_GPIO2	EC3_PHY_GPIO2	P	
59	DGND	DGND	P	
60	DGND	DGND	P	

4.3 Demultiplexing on MBLS102xA

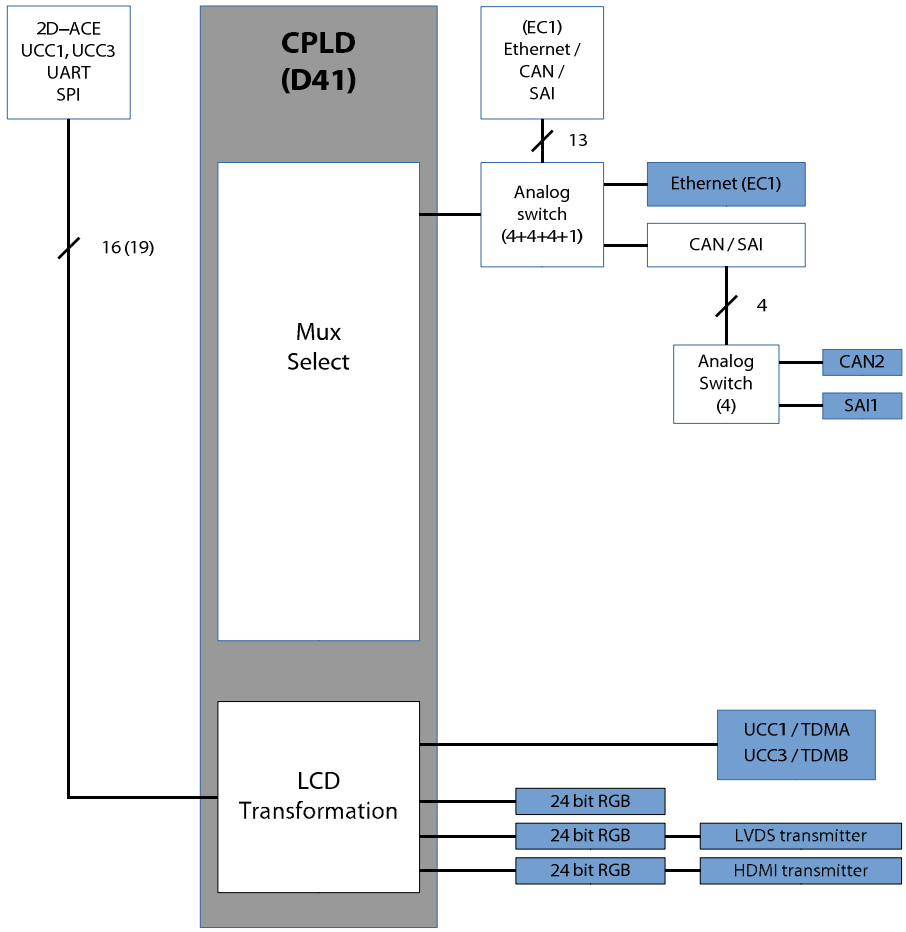


Illustration 6: Demultiplexing on MBLS102xA

The CPLD sets the multiplexing according to DIP switch S9 (4 bit). Function #1 is selected, when the bit string is invalid.

Table 11: Functions of DIP switch S9

No.	Function	00 = EC1 01 = CAN1/CAN2 10 = SAI1/SAI2 11 = Reserved	00 = HDMI 01 = LVDS 10 = UCC 11 = LVDS_RGBINV	VHDL MuxSel[3:0]	DIP switch MUX_SEL_x				DIP switch S9			
					3	2	1	0	4	3	2	1
1	EC1_HDMI	00	00	0000	0	0	0	0	ON	ON	ON	ON
2	EC1_LVDS	00	01	0001	0	0	0	1	ON	ON	ON	OFF
3	EC1_UCC	00	10	0010	0	0	1	0	ON	ON	OFF	ON
4	EC1_LVDS_RGBINV	00	11	0011	0	0	1	1	ON	ON	OFF	OFF
5	CAN_HDMI	01	00	0100	0	1	0	0	ON	OFF	ON	ON
6	CAN_LVDS	01	01	0101	0	1	0	1	ON	OFF	ON	OFF
7	CAN_UCC	01	10	0110	0	1	1	0	ON	OFF	OFF	ON
8	CAN_LVDS_RGBINV	01	11	0111	0	1	1	1	ON	OFF	OFF	OFF
9	SAI_HDMI	10	00	1000	1	0	0	0	OFF	ON	ON	ON
10	SAI_LVDS	10	01	1001	1	0	0	1	OFF	ON	ON	OFF
11	SAI_UCC	10	10	1010	1	0	1	0	OFF	ON	OFF	ON
12	SAI_LVDS_RGBINV	10	11	1011	1	0	1	1	OFF	ON	OFF	OFF
13 – 16	Reserved	11	XX	Other	1	1	x	x	OFF	OFF	X	X

4.4 Reset generation

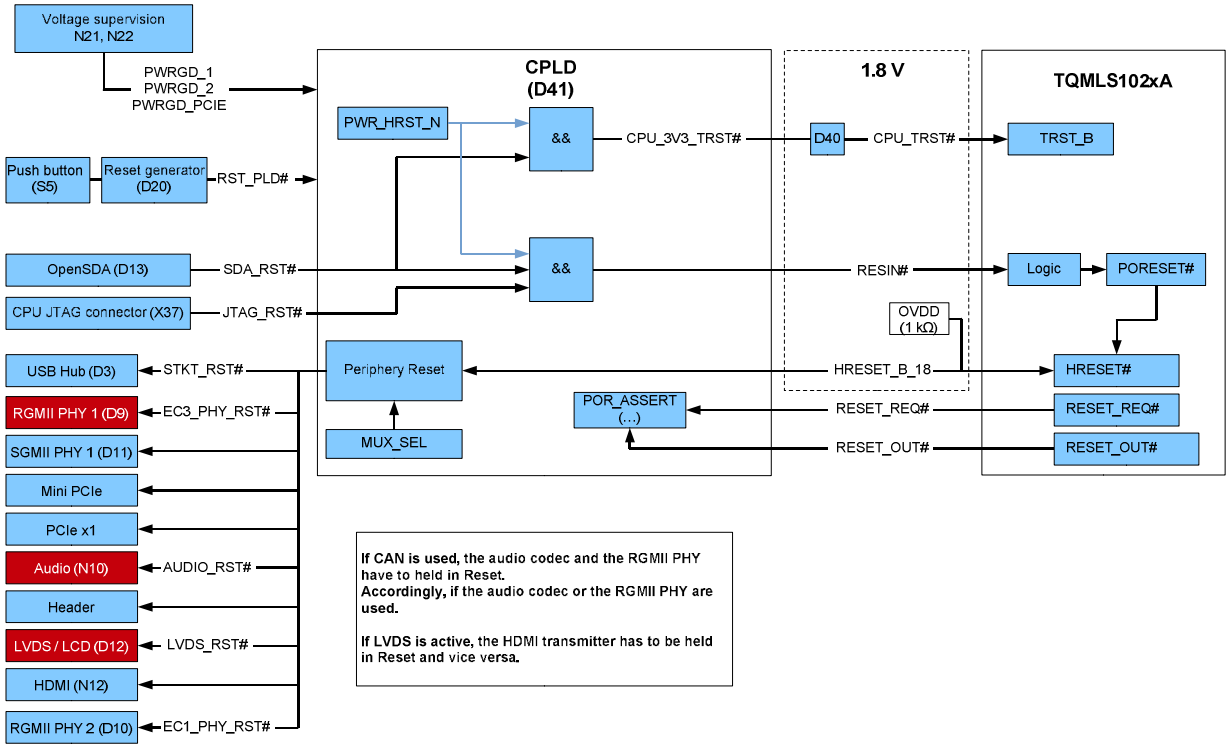


Illustration 7: Reset structure

4.5 Diagnose- and user interfaces

4.5.1 LEDs

The MBLS102xA provides 20 green status LEDs.

Table 12: LEDs

LED Reference	Colour	Function
V16	green	USB_H1_VBUS
V17	green	USB_H2_VBUS
V18	green	USB_H3_VBUS
V47	green	USB1_VBUS
V48	green	LED_WWAN#
V49	green	LED_WLAN#
V50	green	LED_WPAN#
V51	green	OpenSDA Status
V52	green	USB_H5_VBUS
V53	green	VCC24V
V54	green	VCC12V
V55	green	VCC5V
V56	green	VCC3V3
V84	green	VCC3V3_PCIE
V85	green	VCC2V5
V89	green	CPLD Status: Blinking = working
V95	green	User GPIO Led
V96	green	User GPIO Led
V97	green	User GPIO Led
V98	green	User GPIO Led

4.5.2 Push buttons

The MBLS102xA provides four push buttons.
S5 is the reset button, the other three serve as general push buttons.

Table 13: Push buttons

Push button	Function
S5	Reset
S6	GPIO
S7	GPIO
S8	GPIO

4.5.3 DIP switches

Table 14: Termination RS-485

DIP switch	Position	Signal	Remark
S1-1	ON	–	120 Ω Termination Rx
	OFF		No termination Rx
S1-2	ON	–	120 Ω Termination Tx
	OFF		No termination Tx

Table 15: Termination CAN

DIP switch	Position	Signal	Remark
S2-1	ON	–	120 Ω Termination CAN1
	OFF		No termination CAN1
S2-2	ON	–	120 Ω Termination CAN2
	OFF		No termination CAN2

Table 16: Boot-source and GPIO

DIP switch	Position	Signal	Remark
S3-1	ON	BOOT_CFG0	Boot interface: SDHC controller
	OFF		Boot source: QSPI NOR flash on TQMLS102xA
S3-2	ON	EMMC_SEL	Boot source: SD card
	OFF		Boot source: eMMC on TQMLS102xA
S3-3	–	GPIO_DIP2	GPIO
S3-4	–	GPIO_DIP3	GPIO

4.5.4 GPIO

The following table lists the freely available GPIOs.

Table 17: GPIO assignment

I/O Expander (Reference)	Signal	Port	Level
I/O Expander 1 (D35)	GPIO_BUTTON0	IO0	3.3 V
	GPIO_BUTTON1	IO1	3.3 V
	GPIO_BUTTON2	IO2	3.3 V
	GPIO_DIP1	IO3	3.3 V
	GPIO_DIP2	IO4	3.3 V
	GPIO_DIP3	IO5	3.3 V
	EXT_TOUCH_INT#	IO6	3.3 V
	GPIO_1	IO7	3.3 V
I/O Expander 2 (D39)	PCIE_PWR_EN	IO0	3.3 V
	MPCIE_DISABLE#	IO1	3.3 V
	MPCIE_WAKE#	IO2	3.3 V
	LCD_BLT_EN	IO3	3.3 V
	LCD_PWR_EN	IO4	3.3 V
	EC1_PHY_PWDN#/INT#_3V3	IO5	3.3 V
	EC3_PHY_PWDN#/INT#_3V3	IO6	3.3 V
	SGMII_PHY_PWDN#/INT#_3V3	IO7	3.3 V
I/O Expander 3 (D63)	MUX_SEL_0	IO0	3.3 V
	MUX_SEL_1	IO1	3.3 V
	MUX_SEL_2	IO2	3.3 V
	MUX_SEL_3	IO3	3.3 V
	LED V95	IO4	3.3 V
	LED V96	IO5	3.3 V
	LED V97	IO6	3.3 V
	LED V98	IO7	3.3 V
Touch Controller (D34)	GPIO_ADC_I2C1_1	GPIO0	3.3 V
	GPIO_ADC_I2C1_2	GPIO1	3.3 V
	GPIO_ADC_I2C1_3	GPIO2	3.3 V
	GPIO_ADC_I2C1_4	GPIO3	3.3 V
TQMLS102xA	EVT9#_GPIO2_24	–	1.8 V

4.5.5 Boot-Mode configuration

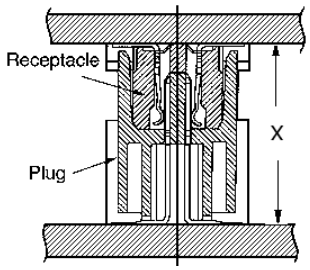
Table 18: Boot-source

DIP switch	Position	Signal	Remark
S3-1	ON	BOOT_CFG0	Boot interface: SDHC controller
	OFF		Boot source: QSPI NOR flash on TQMLS102xA
S3-2	ON	EMMC_SEL	Boot source: SD card
	OFF		Boot source: eMMC on TQMLS102xA

4.6 TQMLS102xA connectors

The connector used on the MBLS102xA is shown in Table 19.
If a different board-to-board distance is required, higher connectors are available. Suitable types are to be taken from Table 19.

Table 19: Suitable carrier board mating connectors

Manufacturer	Pin count / Part number	Remark	Stack height (X)	
TE connectivity	40-pin: 5177986-1 120-pin: 5177986-5	Used on MBLS102xA	5 mm	
TE connectivity	40-pin: 1-5177986-1 120-pin: 1-5177986-5	–	6 mm	
TE connectivity	40-pin: 2-5177986-1 120-pin: 2-5177986-5	–	7 mm	
TE connectivity	40-pin: 3-5177986-1 120-pin: 3-5177986-5	–	8 mm	

The pins assignment listed in Table 5 to Table 7 refer to the corresponding standard BSP of TQ-Systems GmbH.
Information regarding I/Os in Table 5 to Table 7 refers to the CPU pins.

Attention: Pin multiplexing	
	Depending on the selected MBLS102xA, not all interfaces are available. Available interfaces are to be taken from the User's Manual and the pinout table of the MBLS102xA.

4.7 Pinout of connectors to TQMLS102xA

The available signals are routed via three connectors onto the MBLS102xA.
The pins assignment listed in Table 20, Table 21 and Table 22 refer to the corresponding standard BSP of TQ-Systems GmbH.

Table 20: Pinout connector X36 (X1 on TQMLS102xA)

I/O	Description	Group	Signal	Pin		Signal	Group	Description	I/O
IN		Power	VCC3V3IF	1	2	VCC3V3IF	Power		IN
IN		Power	VCC3V3IF	3	4	VCC3V3IF	Power		IN
IN		Power	VCC3V3IF	5	6	VCC3V3IF	Power		IN
IN		Power	VCC3V3IF	7	8	VCC3V3IF	Power		IN
IN		Power	L1VDD_IN	9	10	VBAT	Power		IN
OUT		Power	L1VDD_OUT	11	12	DGND			
OUT		Power	LVDD_OUT	13	14	USB1_D_P	USB		BI
IN		Power	LVDD_IN	15	16	USB1_D_M	USB		BI
			DGND	17	18	DGND			
OUT		Power	O1VDD	19	20	USB1_RX_P	USB		IN
			DGND	21	22	USB1_RX_M	USB		IN
IN		SYSTEM	RESIN#	23	24	DGND			
IN		SYSTEM	POWER_STBY	25	26	USB1_TX_P	USB		OUT
IN		SYSTEM	POWER_EN	27	28	USB1_TX_M	USB		OUT
			DGND	29	30	DGND			
OUT	For internal tests	TEST	SYSCLK_EXT	31	32	CLK_OE	TEST	For internal tests	IN
			DGND	33	34	IIC1_SDA	I2C	4.7 kΩ ↑ to 3.3 V[3]	BI
OUT	For internal tests	TEST	DDRCLK_EXT	35	36	IIC1_SCL	I2C	4.7 kΩ ↑ to 3.3 V[3]	OUT
			DGND	37	38	DGND			
IN	2D_ACE_VSYNC	UART	UART3_SIN	39	40	IIC2_SDA	I2C	SDHC_WP	BI
OUT	2D_ACE_HSYNC	UART	UART3_SOUT	41	42	IIC2_SCL	I2C	SDHC_CD#	OUT
OUT		UART	UART1_SOUT	43	44	DGND			
IN	10 kΩ ↑ to 3.3 V	UART	UART1_SIN	45	46	GPIO4_19	GPIO	2D_ACE_D10	BI
			DGND	47	48	DGND			
IN	2D_ACE_D11	GPIO	GPIO4_20	49	50	GPIO4_12	GPIO	2D_ACE_D03	BI
			DGND	51	52	GPIO4_11	GPIO	2D_ACE_D02	BI
OUT	2D_ACE_D04	GPIO	GPIO4_13	53	54	GPIO4_10	GPIO	2D_ACE_D01	BI
IN	1 kΩ ↑ to O1VDD[4]	TEST	TEST_SEL#	55	56	GPIO4_09	GPIO	2D_ACE_D00	BI
IN		USB	USB1_ID	57	58	HRESET#	SYSTEM	1 kΩ ↑ to O1VDD[4]	IN
IN		USB	USB1_VBUS	59	60	RESET_REQ_OUT#	SYSTEM	2.2 kΩ ↑ to 3.3 V[4]	OUT
			DGND	61	62	RESET_OUT#	SYSTEM		OUT
IN	GPIO_INT1#, 10 kΩ ↑ to 3.3 V[5]	IRQ	IRQ4	63	64	DGND			
IN	GPIO_INT2#, 10 kΩ ↑ to 3.3 V[5]	IRQ	IRQ5	65	66	TEMP_CRIT_OUT#	SYSTEM	10 kΩ ↑ to 3.3 V[4]	OUT
			DGND	67	68	TEMP_ALERT#	SYSTEM	Open Drain	OUT
OUT		RTC	RTC_CLK_OUT	69	70	BOOT_CFG0	SYSTEM	10 kΩ ↓[4]	IN
OUT	2.2 kΩ ↑ to 3.3 V / VBAT[4]	RTC	RTC_INT_OUT#	71	72	DGND			
BI	10 kΩ ↑ to O1VDD[4]	SYSTEM	EVT1# (TQMLS102xA Rev. 01xx)	73	74	EVT0# (TQMLS102xA Rev. 01xx)	SYSTEM	10 kΩ ↑ to O1VDD[4]	BI
BI		PMC SWD	SWD_DIO (TQMLS102xA Rev. 02xx)			SWD_CLK (TQMLS102xA Rev. 02xx)	PMC SWD		IN
BI	10 kΩ ↑ to O1VDD[4]	SYSTEM	EVT2#	75	76	JTAG_TMS	JTAG	10 kΩ ↑ to OVDD[4]	IN
BI	10 kΩ ↑ to O1VDD[4]	SYSTEM	EVT3#	77	78	JTAG_TCK	JTAG	10 kΩ ↑ to OVDD[4]	IN
BI	10 kΩ ↑ to O1VDD[4]	SYSTEM	EVT4#	79	80	JTAG_TDO	JTAG		OUT
BI	10 kΩ ↑ to O1VDD[4]	SYSTEM	EVT9#	81	82	JTAG_TDI	JTAG	10 kΩ ↑ to OVDD[4]	IN
OUT	4.7 kΩ ↑ to O1VDD[4]	SYSTEM	ASLEEP	83	84	JTAG_TRST#	JTAG	10 kΩ ↑ to OVDD[4]	IN
IN	4.7 kΩ ↑ to O1VDD[4]	IRQ	IRQ0	85	86	PMC_PWR_STATUS	SYSTEM		OUT
IN	4.7 kΩ ↑ to OVDD[4]	IRQ	IRQ1	87	88	EEPROM_WC#	SYSTEM	10 kΩ ↓[4]	IN
			DGND	89	90	GPIO1_14 / RTC	SYSTEM		BI
BI		IFC	QSPI_B_IO0	91	92	DGND			
BI		IFC	QSPI_B_IO1	93	94	QSPI_B_CS0	IFC		OUT
BI		IFC	QSPI_B_IO2	95	96	QSPI_B_CS1	IFC		OUT
BI		IFC	QSPI_B_IO3	97	98	QSPI_B_DQS	IFC	4.7 kΩ ↑ to 3.3 V	BI
OUT		IFC	QSPI_B_CK	99	100	DGND			
			DGND	101	102	SPI1_CS0#	IFC		OUT
BI		IFC	QSPI_A_IO0	103	104	SPI1_SCK	IFC		OUT
BI		IFC	QSPI_A_IO1	105	106	SPI1_CS5 / RCW_SRC4	IFC	RCW config during POR	BI
BI	10 kΩ ↑ to 3.3 V[4]	IFC	QSPI_A_IO2	107	108	SPI1_SIN	IFC		IN
BI	10 kΩ ↑ to 3.3 V[4]	IFC	QSPI_A_IO3	109	110	SPI1_SOUT / RCW_SRC5	IFC	RCW config during POR	BI
OUT		IFC	QSPI_A_CK	111	112	SPI1_CS1 / RCW_SRC0	IFC	RCW config during POR	BI
			DGND	113	114	SPI1_CS2 / RCW_SRC1	IFC	RCW config during POR	BI
OUT	4.7 kΩ ↓ or ↑[4]	IFC	QSPI_A_CS0	115	116	SPI1_CS3 / RCW_SRC2	IFC	RCW config during POR	BI
OUT	4.7 kΩ ↓ or ↑[4]	IFC	QSPI_A_CS1	117	118	SPI1_CS4 / RCW_SRC3	IFC	RCW config during POR	BI
BI	4.7 kΩ ↑ to 3.3 V	IFC	QSPI_A_DQS	119	120	DGND			

3: 2.2 kΩ ↑ to 3.3 V on TQMLS102xA.
4: On TQMLS102xA.
5: 4.7 kΩ ↑ to 3.3 V on TQMLS102xA.

Table 21: Pinout connector X7 (X2 on TQMLS102xA)

I/O	Description / Function	Group	Signal	Pin		Pin	Signal	Group	Description / Function	I/O
			DGND	1		2	SDHC_DAT4	SDHC		BI
OUT		SDHC	SDHC_CLK	3		4	SDHC_DAT5	SDHC		BI
			DGND	5		6	SDHC_DAT6	SDHC	USB1_DRVVBUS	BI
BI		SDHC	SDHC_DAT0	7		8	SDHC_DAT7	SDHC	USB1_PWRFAULT	BI
BI		SDHC	SDHC_DAT1	9		10	SDHC_CMD	SDHC		BI
BI		SDHC	SDHC_DAT2	11		12	DGND			
BI		SDHC	SDHC_DAT3	13		14	GPIO4_22	GPIO		BI
			DGND	15		16	DGND			
BI	2D_ACE_DE	GPIO	GPIO4_21	17		18	GPIO4_18	GPIO	2D_ACE_D09	BI
			DGND	19		20	GPIO4_14	GPIO	2D_ACE_D05	BI
BI	2D_ACE_D07	GPIO	GPIO4_16	21		22	GPIO4_15	GPIO	2D_ACE_D06	BI
BI	2D_ACE_D08	GPIO	GPIO4_17	23		24	UART2_SIN	UART	LPUART1_SIN	IN
IN	LPUART1_CTS#	UART	UART4_SIN	25		26	UART2_SOUT	UART	LPUART1_SOUT	OUT
OUT	LPUART1_RTS#	UART	UART4_SOUT	27		28	DGND			
IN	TOUCH_GPIO_INT#, 4.7 kΩ ↑ to LVDD[6]	IRQ	IRQ3	29		30	USB2_D0	USB		BI
			DGND	31		32	USB2_D1	USB		BI
IN		USB	USB2_CLK	33		34	USB2_D2	USB		BI
BI		USB	USB2_D4	35		36	USB2_D3	USB		BI
BI		USB	USB2_D5	37		38	USB2_NXT	USB		IN
BI		USB	USB2_D6	39		40	USB2_DIR	USB		IN
BI		USB	USB2_D7	41		42	DGND			
OUT	1 kΩ ↓[6]	USB	USB2_STP	43		44	EC3_RXD0	EC3		IN
IN	10 kΩ ↓	USB	USB2_PWRFAULT	45		46	EC3_RXD1	EC3		IN
			DGND	47		48	EC3_RXD2	EC3		IN
OUT		EC3	EC3_GTX_CLK	49		50	EC3_RXD3	EC3		IN
OUT		EC3	EC3_TXD0	51		52	EC3_RX_DV	EC3		IN
OUT		EC3	EC3_TXD1	53		54	EC3_RX_CLK	EC3		IN
OUT		EC3	EC3_TXD2	55		56	DGND			
OUT		EC3	EC3_TXD3	57		58	MDIO	MDIO	1 kΩ ↑ to L1VDD_IN	BI
OUT	1 kΩ ↓[6]	EC3	EC3_TX_EN	59		60	MDC	MDIO	1 kΩ ↑ to L1VDD_IN	OUT
			DGND	61		62	DGND			
IN		EC3	EC3_GTX_CLK125	63		64	EC1_RX_CLK	EC1		IN
			DGND	65		66	EC1_RX_DV	EC1		IN
OUT		EC1	EC1_TXD0	67		68	EC1_RXD0	EC1		IN
OUT		EC1	EC1_TXD1	69		70	EC1_RXD1	EC1		IN
OUT		EC1	EC1_TXD2	71		72	EC1_RXD2	EC1		IN
OUT		EC1	EC1_TXD3	73		74	EC1_RXD3	EC1		IN
OUT	1 kΩ ↓[6]	EC1	EC1_TX_EN	75		76	DGND			
IN		EC1	EC1_GTX_CLK125	77		78	EC1_GTX_CLK	EC1		IN
			DGND	79		80	IRQ2	IRQ	4.7 kΩ ↑ to L1VDD[6]	IN
OUT	LANE_A_TX_P	SERDES	SD_TX0_P	81		82	DGND			
			DGND	83		84	SD_REF_CLK1_P	SERDES		IN
OUT	LANE_A_TX_N	SERDES	SD_TX0_N	85		86	DGND			
			DGND	87		88	SD_REF_CLK1_N	SERDES		IN
OUT	SATA_TX_P	SERDES	SD_TX1_P	89		90	DGND			
			DGND	91		92	SD_RX0_P	SERDES	LANE_A_RX_P	IN
OUT	SATA_TX_N	SERDES	SD_TX1_N	93		94	DGND			
			DGND	95		96	SD_RX0_N	SERDES	LANE_A_RX_N	IN
OUT	LANE_C_TX_P	SERDES	SD_TX2_P	97		98	DGND			
			DGND	99		100	SD_RX1_P	SERDES	SATA_RX_P	IN
OUT	LANE_C_TX_N	SERDES	SD_TX2_N	101		102	DGND			
			DGND	103		104	SD_RX1_N	SERDES	SATA_RX_N	IN
OUT	LANE_D_TX_P	SERDES	SD_TX3_P	105		106	DGND			
			DGND	107		108	SD_RX2_P	SERDES	LANE_C_RX_P	IN
OUT	LANE_D_TX_N	SERDES	SD_TX3_N	109		110	DGND			
			DGND	111		112	SD_RX2_N	SERDES	LANE_C_RX_N	IN
IN		SERDES	SD_REF_CLK2_P	113		114	DGND			
			DGND	115		116	SD_RX3_P	SERDES	LANE_D_RX_P	IN
IN		SERDES	SD_REF_CLK2_N	117		118	DGND			
			DGND	119		120	SD_RX3_N	SERDES	LANE_D_RX_N	IN

6: On TQMLS102xA.

Table 22: Pinout connector X22 (X3 on TQMLS102xA)

I/O	Description	Group	Signal	Pin		Pin	Signal	Group	Description	I/O
			DGND	1		2	DGND			
IN		PMC SWD	SWD_CLK (TQMLS102xA Rev. 01xx)	3		4	TA_BB_TMP_DETECT#	TRUST	1 kΩ ↓[7]	IN
BI	10 kΩ ↑ to O1VDD[7]	SYSTEM	EVT0# (TQMLS102xA Rev. 02xx)							
BI		PMC SWD	SWD_DIO (TQMLS102xA Rev. 01xx)	5		6	TA_PROG_SFP	FUSE PRG	330 Ω ↓[7]	IN
BI	10 kΩ ↑ to O1VDD[7]	SYSTEM	EVT1# (TQMLS102xA Rev. 02xx)							
IN	330 Ω ↓[7]	FUSE PRG	PROG_MTR	7		8	TA_TMP_DETECT#	TRUST	1 kΩ ↓[7]	IN
IN	10 kΩ ↓[7]	TRUST	TA_BB_RTC	9		10	DGND			
			DGND	11		12	IFC_AD00	IFC		BI
BI		IFC	IFC_AD01	13		14	IFC_AD02	IFC		BI
BI		IFC	IFC_AD03	15		16	IFC_AD04	IFC		BI
BI		IFC	IFC_AD05	17		18	IFC_AD06	IFC		BI
BI		IFC	IFC_AD07	19		20	IFC_WE0#	IFC		OUT
			DGND	21		22	IFC_BTCL	IFC		OUT
OUT		IFC	IFC_NDDDR_CLK	23		24	DGND			
BI	RCW cfg during POR	IFC	IFC_AD14 / RCW_SRC6	25		26	IFC_TE / RCW_IFC_TE	IFC	RCW cfg during POR	OUT
BI	RCW cfg during POR	IFC	IFC_AD15 / RCW_SRC7	27		28	IFC_AVD	IFC		OUT
–		–	NC	29		30	IFC_NDDQS	IFC		BI
OUT	4.7 kΩ ↑ to 3.3 V	IFC	IFC_CS0#	31		32	DGND			
IN	4.7 kΩ ↑ to 3.3 V	IFC	IFC_RB0#	33		34	IFC_OE#	IFC		OUT
			DGND	35		36	IFC_CLE / RCW_SRC8	IFC	RCW cfg during POR	OUT
OUT		IFC	IFC_CLK0	37		38	DGND			
OUT		IFC	IFC_WP0#	39		40	IFC_CLK1	IFC		OUT

7: On TQMLS102xA.

5. SOFTWARE-SPECIFICATION

No software is required for the MBLS102xA.
Suitable software is only required on the TQMLS102xA and is not a part of this specification.
More information can be found in the Support Wiki for the TQMLS102xA.

6. MECHANICS

6.1 Dimensions

The overall dimensions (length × width) of the MBLS102xA are 230 × 170 mm².
The maximum height of the MBLS102xA is approximately 19.5 mm.
The MBLS102xA has six mounting holes with a diameter of 4.3 mm.
The MBLS102xA weighs approximately 310 g without TQMLS102xA.

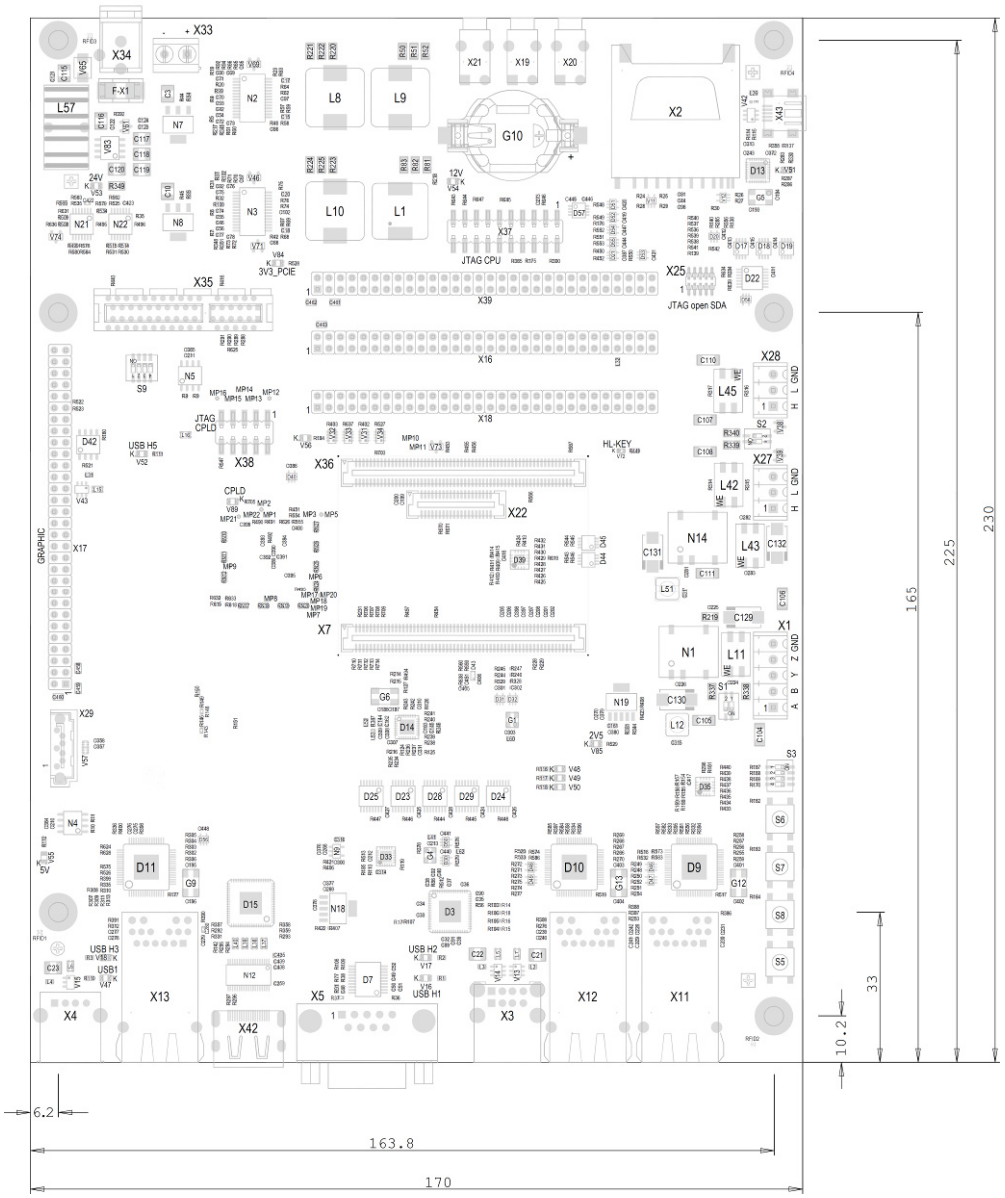


Illustration 8: MBLS102xA dimensions

6.2 Housing

The form factor and the mounting holes are designed for installation in the COMSys housing.

6.3 Thermal management

No special precautions were taken concerning the thermal management of the TQMLS102xA.
Cooling the TQMLS102xA may be necessary depending on the software or the TQMLS102xA used.
More information is to be taken from the User's Manual of the TQMLS102xA.

6.4 Assembly top

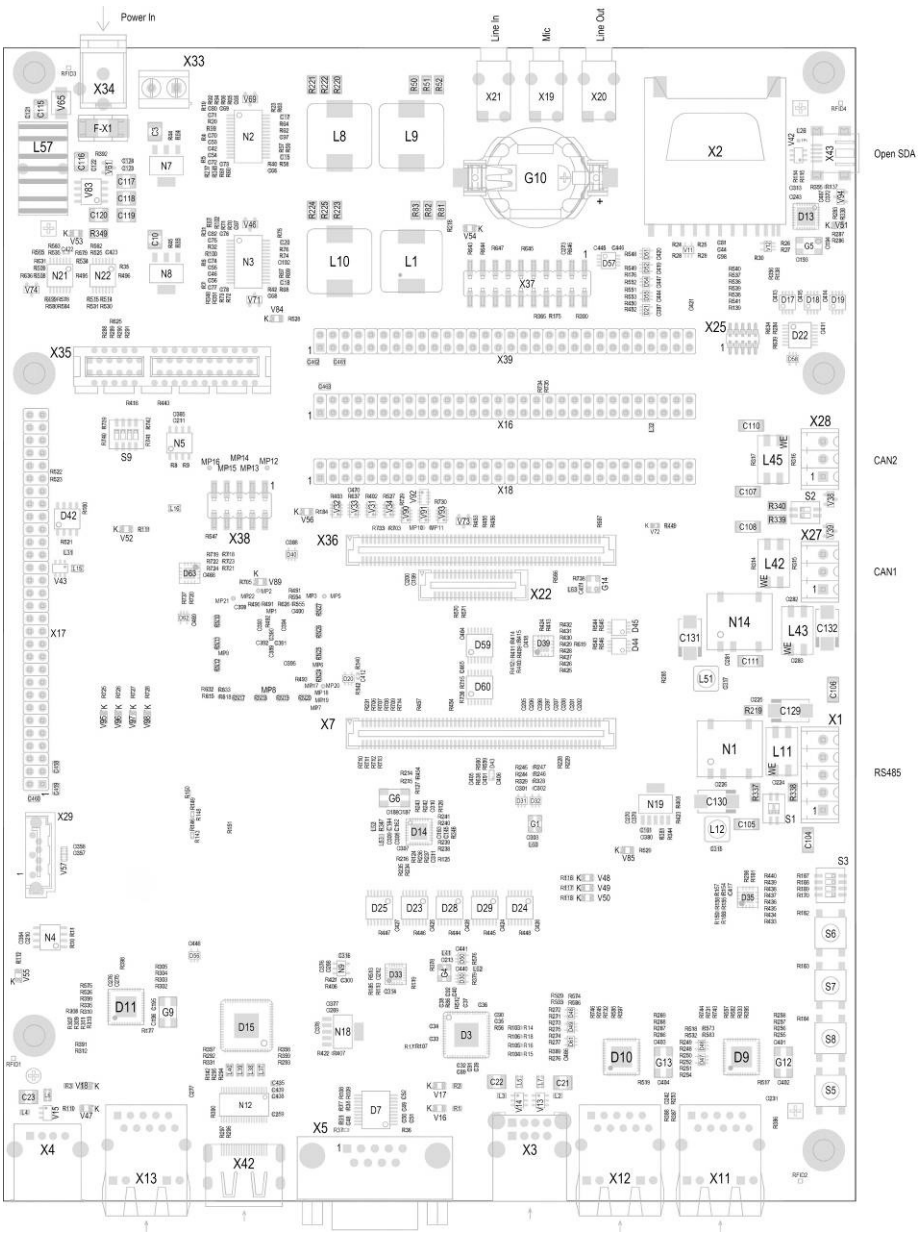


Illustration 9: Component placement top

6.5 Assembly bottom

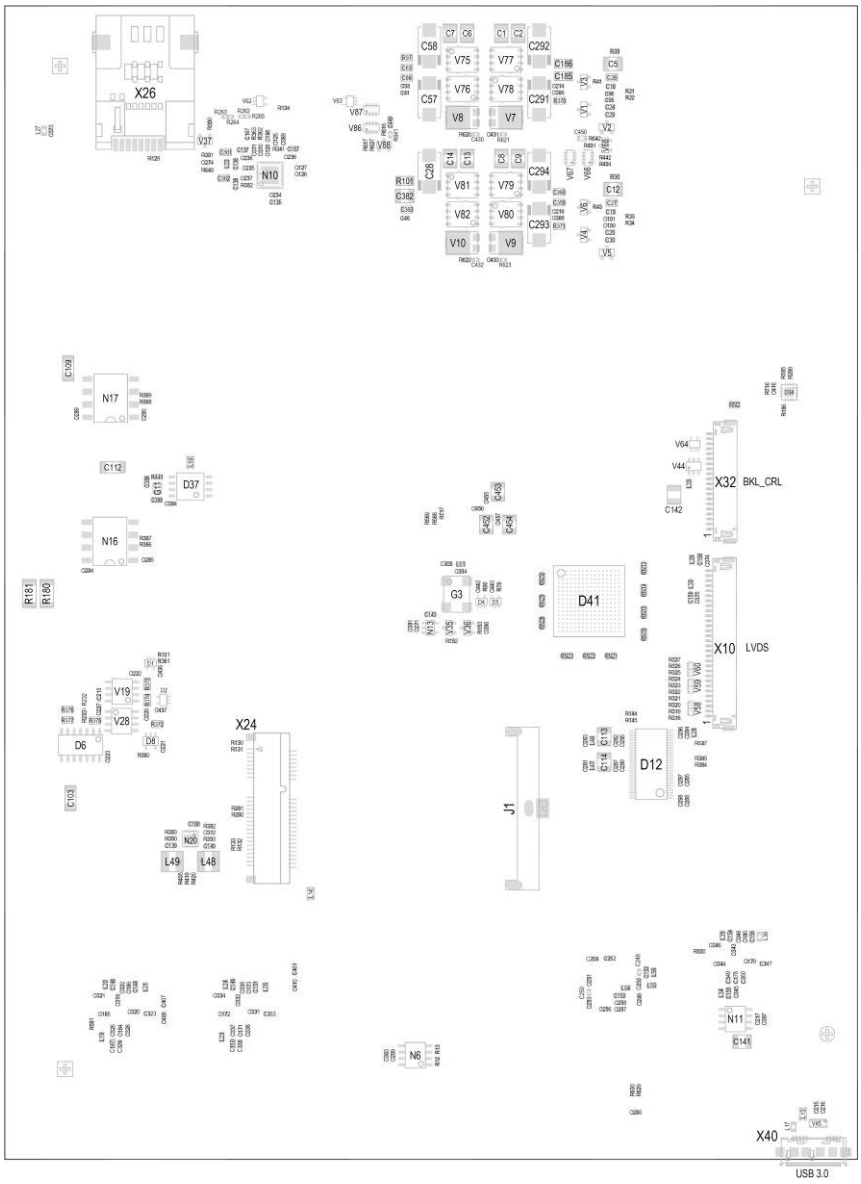


Illustration 10: Component placement bottom

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

Because the MBLS102xA is a development platform, no EMC specific tests have been carried out.
During the development of the MBLS102xA the following standard was taken into account:

- EMC-Interference radiation:
  Measurement of the electrically radiated emission according to EN50082-1.

7.2 ESD

Most of the interfaces on the MBLS102xA are protected against electrostatic discharge. [8]
The interfaces protected against ESD are to be taken from the circuit diagram.

7.3 Operational safety and personal security

Due to the occurring voltages (≤30 V DC), tests with respect to the operational and personal safety haven't been carried out.

8. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 23: Climatic and operational conditions MBLS102xA

Parameter	Range	Remark
Permitted environmental temperature	0 °C to +50 °C	
Permitted storage temperature	–20 °C to +60 °C	With Lithium battery
Permitted storage temperature	–20 °C to +100 °C	Without Lithium battery
Relative air humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: Cooling	
	The CPU belongs to a performance category in which a cooling system may be essential in certain applications. It is the responsibility of the customer to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software).

8.1 Protection against external effects

Protection class IP00 was defined for the MBLS102xA. There is no protection against foreign objects, touch or humidity.

8.2 Reliability and service life

No detailed MTBF calculation has been done for the MBLS102xA. The MBLS102xA is designed to be insensitive to vibration and impact. Connectors, which guarantee at least 100 mating cycles, are assembled on the MBLS102xA.
The device is designed for a typical product life of 10 years.
Excluded is the lithium cell, which must be renewed after about 5 years.

8: The JTAG interface is not protected against ESD.

9. ENVIRONMENT PROTECTION

9.1 RoHS

The MBLS102xA is manufactured RoHS compliant.

- All components and assemblies used are RoHS compliant
- RoHS compliant soldering processes are used

9.2 WEEE

The company placing the product on the market is responsible for the observance of the WEEE regulation (TQ-Systems GmbH).
To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

9.3 REACH

The EU-chemical regulation 1907/2006 (REACH regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as TQ-Systems GmbH is informed by suppliers accordingly. Regarding REACH an examination exceeding RoHS verification was not carried out.

9.4 EuP

The guideline 2005/32/EC, also Energy using Products (EuP), is not applicable for the following reasons:

- The guideline is only applicable for products with an annual production quantity of >200,000.
- The external power supply is a purchased part.

9.5 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the MBLS102xA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.
The energy consumption of this subassembly is minimised by suitable measures. The MBLS102xA is delivered in reusable packaging.

9.6 Batteries

9.6.1 General notes

Due to technical reasons a battery is necessary for this product. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used.
If this is unavoidable for technical reasons, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

9.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2 grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.
- During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
The energy consumption of this subassembly is minimised by suitable measures.
Printed pc-boards are delivered in reusable packaging.
Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, 1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

10. APPENDIX

10.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 24: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
BIOS	Basic Input/Output System
CAN	Controller Area Network
CEC	Consumer Electronics Control
CPI	CEC Programming Interface (Silicon Image)
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
DC	Direct Current
DDR3L	Double Data Rate 3 Low voltage
DIP	Dual In-line Package
EDID	Extended Display Identification Data
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
ESD	Electrostatic Discharge
EuP	Energy using Products
FFC	Flat Flex Cable
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GSM	Global System for Mobile Communications (Groupe Spécial Mobile)
HDMI	High Definition Multimedia Interface
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IFC	Integrated Flash-Controller
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LDO	Low Drop-Out
LED	Light Emitting Diode
LVDS	Low Voltage Differential Signaling
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTBF	Mean operating Time Between Failures
NC	Not Connected
O	Output
OpenSDA	Serial and Debug Adapter (NXP)
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (layer of the OSI model)
PMC	Power Management Controller
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PWM	Pulse-Width Modulation
QSPI	Quad Serial Peripheral Interface

Table 24: Acronyms (continued)

Acronym	Meaning
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232	Recommended Standard (serial interface)
RS-485	Recommended Standard (serial interface)
RTC	Real-Time Clock
SAI	Serial Audio Interface
SATA	Serial ATA
SD	Secure Digital
SD/MMC	Secure Digital Multimedia Card
SDHC	Secure Digital High Capacity
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SMBUS	System Management Bus
SPI	Serial Peripheral Interface
SS	Super Speed
SVHC	Substances of Very High Concern
SWD	Serial Wire Debug
TDM	Time-Division Multiplexing
THT	Through-Hole Technology
TPI	Transmitter Programming Interface (Silicon Image)
UART	Universal Asynchronous Receiver/Transmitter
UCC	Unified Communications Controller
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
VHDL	VHSIC Hardware Description Language
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network

10.2 References

Table 25: Further applicable documents

No.	Name	Rev. / Date	Company
(1)	QorIQ LS1021A Reference Manual	Rev. D, 09 / 2014	NXP
(2)	PMIC 34VR500	Rev. 3.0, 1 / 2015	NXP
(3)	TQMLS102xA User's Manual	– current –	TQ-Systems
(4)	Support-Wiki for the TQMLS102xA	– current –	TQ-Systems
(5)			

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Technology in Quality