TQMT104x
User's Manual

TQMT104x UM 0110
11.04.2023

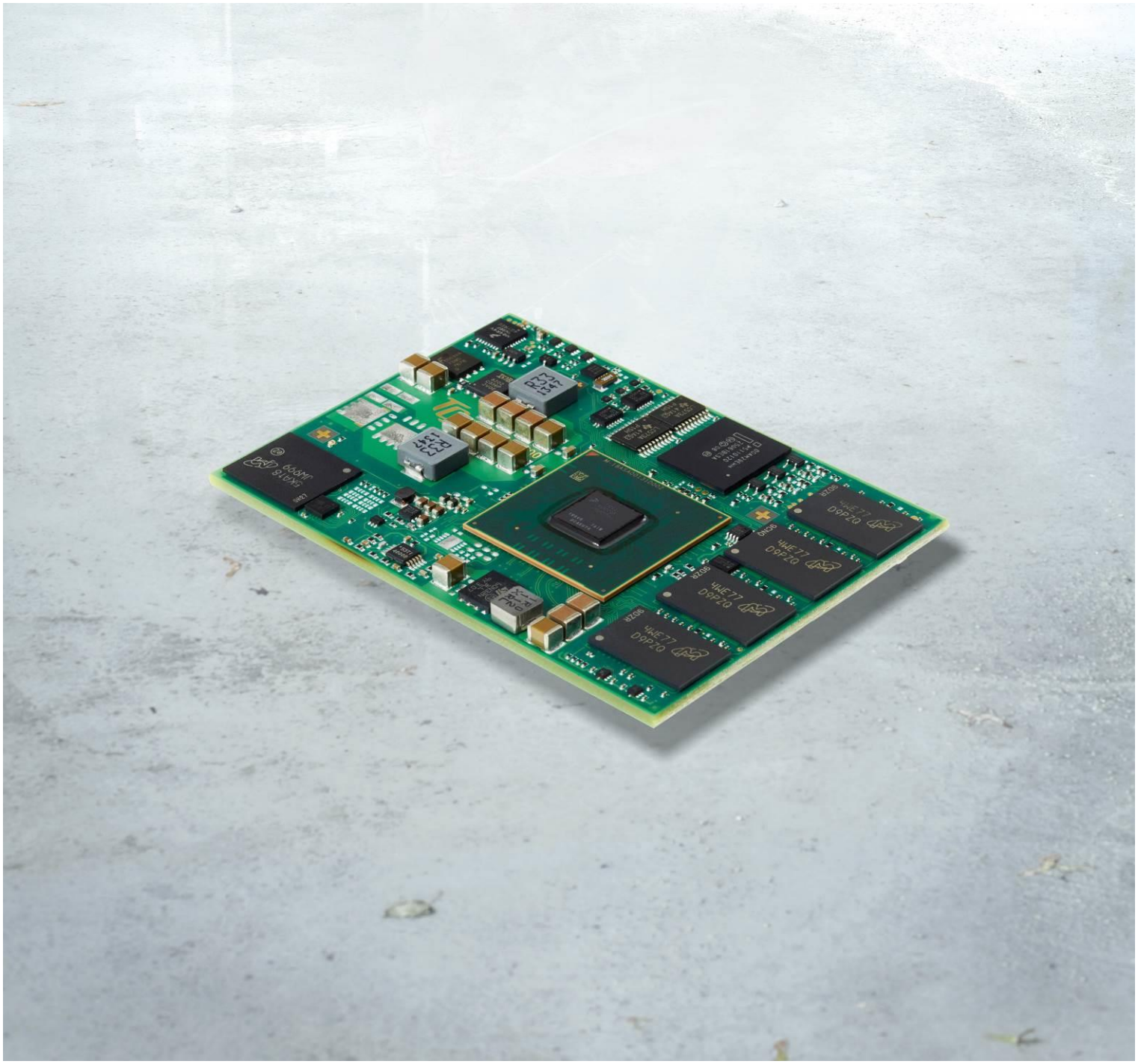

TABLE OF CONTENTS

TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	18.07.2016	Petz		First edition
0101	07.03.2018	Petz	1.3 1.9 3.2.3 Illustration 1, 3.3.7.1, 3.3.7.2 Table 10, Table 14 Illustration 4, 7.3	Updated Some CPU Reference Manuals added Information regarding X3 added Reworked Added Updated
0102	19.04.2018	Petz	All Table 2	"VCC3V3SBYF" replaced with "VCC3V3SBY" Column headers corrected, X1-30: "VCC3V3" replaced with "VCC3V3F"
0103	25.04.2018	Petz	Table 2	CPU ball assignment corrected
0104	25.10.2018	Petz	All Table 15, Table 16 6, 7 7.7	Links updated "Package temperature" replaced with "Case temperature" Chapters restructured Removed (duplicate of 7.4)
0105	13.09.2019	Petz	1.9 3.3.2 3.3.4 Table 10 3.3.8.1, 3.3.8.4 3.4.1, 3.4.2 5.4	Link to Yocto added, Link to ELDK removed Reworked Added Device information added, SE97B I²C addresses added Reworked and updated Added Removed
0106	04.10.2019	Petz	All Table 2 3.3.8, 3.3.8.1, 3.3.8.2 3.4.2	Formatting, lower case signal names corrected to upper case. Footnotes 3, 4, 8 regarding DVDD / RCW dependency added Footnote 2 added Completely reworked Note on page 17 extended
0107	21.11.2019	Petz	3.2 3.3.4, Table 7, Table 8	Chapters 3.2.1 to 3.2.3 merged Clarified
0108	11.10.2021	Kreuzer	Table 10	I²CAddress of SA56004 corrected
0109	29.10.2021	Kreuzer	3.3.2 Table 7 Table 8	HRESET# corrected to RESET_OUT# HRESET_REQ# corrected to RESET_REQ# HRESET_REQ# corrected to RESET_REQ#
0110	11.04.2023	Trepte	Table 2	Pinout X1, pins 21 and 22: Remark "5 V" removed

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMT104x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C/D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2#/OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- STKT104X circuit diagram
- STKT104X User's Manual
- QorIQ T1040 Reference Manual (also supports T1040, T1042, T1020, T1022)
- U-Boot documentation www.denx.de/wiki/U-Boot/Documentation
- Yocto Documentation www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMT104x

2. BRIEF DESCRIPTION

The TQMT104x extends the product range of Power Architecture™ based TQ modules utilizing the next generation of processors with four Cores (Quad Core). Single, Dual and Octal Core variants are also supported by the design (available on request).

The TQMT104x offers the following advantages:

- Easy migration to a higher performance level for Power Architecture™ based designs.
- More system performance for an attractive price, in comparison to the present Power Architecture™-based modules.
- The most attractive combination of size, price, long-term availability, as well as extended temperature range.

Suitable for the TQMT104x, TQ-Systems GmbH provides a Starterkit, which supports the essential CPU interfaces.
The Starterkit serves for the following purposes:

- Start-up of TQMT104x modules
- Reference platform for own carrier board development
- Test and evaluation platform
- Development platform for low-level software (BSP)
- Easy and simple development platform

3. ELECTRONICS

3.1 Overview

3.1.1 TQMT104x Block diagram

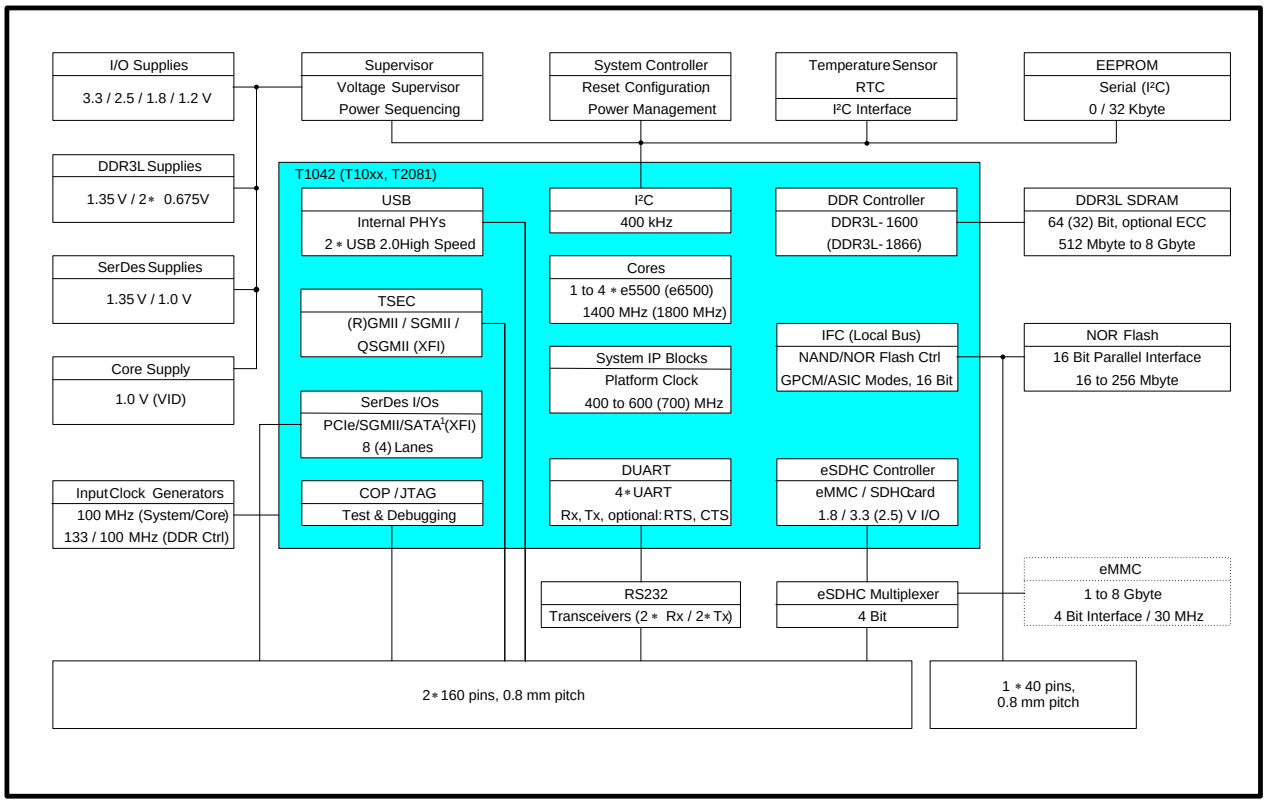


Illustration 1: TQMT104x Block diagram [1]

3.1.2 TQMT104x system components

- QorIQ processor T1042 or pin compatible, see 3.3.1
- Oscillators for CPU clocks
- Reset-Generator / Supervisor and Power Management
- System controller for Reset-Configuration and Power Management incl. glue logic
- Voltage regulator for voltages required on the TQMT104x
- DDR3L SDRAM
- NOR flash
- 2 × serial I²C EEPROM (data + configuration)
- RTC
- Temperature sensors
- 2 × RS-232 driver
- Board-to-Board connector system

1: The T2081 does not provide a SATA interface, see Table 5.

3.2 Pinout connectors X1 to X3

Table 2: Pinout X1

Remark	CPU ball	I/O	Signal	Pin		Signal	I/O	CPU ball	Remark
5 V		P/I	VIN	1	2	VIN	P/I		5 V
5 V		P/I	VIN	3	4	VIN	P/I		5 V
5 V		P/I	VIN	5	6	VIN	P/I		5 V
5 V		P/I	VIN	7	8	VIN	P/I		5 V
5 V		P/I	VIN	9	10	VIN	P/I		5 V
5 V		P/I	VIN	11	12	VIN	P/I		5 V
5 V		P/I	VIN	13	14	VIN	P/I		5 V
5 V		P/I	VIN	15	16	VBAT	P/I		
		P/O	VDD	17	18	VDDC	P/O		
		P/O	VDD	19	20	VDDC	P/O		
		P/I	USB_SVDD_IN	21	22	USB_SVDD_IN	P/I		
		P/O	VCC1V8	23	24	VCC1V8	P/O		
		P/O	VCC1V8	25	26	USB_OVDD_IN	P/I		
		P/O	VCC1V8S	27	28	USB_HVDD_IN	P/I		
		P/O	VCC1V8S	29	30	VCC3V3F	P/O		
		P/O	VCC1V8S	31	32	EVDD	P/I		
		P/O	VCC1V8S	33	34	CVDD	P/I		
		P/O	VCC3V3S	35	36	DVDD [2]	P/I		
		P/I	LVDD	37	38	LVDD	P/I		
		P/I	L1VDD	39	40	L1VDD	P/I		
		P/O	VCC2V5S	41	42	VCC2V5	P/O		
		P/O	VCC2V5S	43	44	VCC2V5	P/O		
		P / I/O	TVDD	45	46	CLK09	I	P4	
		P	DGND	47	48	CLK10	I	P3	
	F8	I	USBCLK	49	50	CLK11	I	N4	
	F1	I/O	USB1_UDP	51	52	CLK12	I	M4	
	F2	I/O	USB1_UDM	53	54	TDMB_RQ	O	R4	
	F4	I	USB1_UID	55	56	TDMB_TSYNC	I	R3	
	F5	I	USB1_PWRFAULT	57	58	TDMB_RSYNC	I	T3	
	E4	I	USB1_VBUSCLMP	59	60	TDMB_RXD	I	U4	
	F6	O	USB1_DRVVBUS	61	62	TDMB_TXD	O	T4	
		P	DGND	63	64	TDMA_RQ	O	R2	
	H1	I/O	USB2_UDP	65	66	TDMA_TSYNC	I	R1	
	H2	I/O	USB2_UDM	67	68	TDMA_RSYNC	I	U1	
	H4	I	USB2_UID	69	70	DGND	P		
	H5	I	USB2_PWRFAULT	71	72	TDMA_RXD	I	U2	
	J4	I	USB2_VBUSCLMP	73	74	TDMA_TXD	O	T1	
	J5	O	USB2_DRVVBUS	75	76	SWD_DIO	I/O		
	A4	I/O	IFC_AD0	77	78	SWD_CLK	I		
	A5	I/O	IFC_AD2	79	80	IFC_AD1	I/O	B5	

2: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (3), Table 4-11, DVDD_VSEL.

3.2 Pinout connectors X1 to X3 (continued)

Table 2: Pinout X1 (continued)

Remark	CPU ball	I/O	Signal	Pin		Signal	I/O	CPU ball	Remark
	A6	I/O	IFC_AD4	81	82	IFC_AD3	I/O	B6	
	B8	I/O	IFC_AD6	83	84	IFC_AD5	I/O	A7	
		P	DGND	85	86	IFC_AD7	I/O	A8	
	C6	O	IFC_A17	87	88	IFC_A16	O	C5	
	C7	O	IFC_A19	89	90	IFC_A18	O	D7	
	C8	O	IFC_A21	91	92	IFC_A20	O	D8	
	D9	O	IFC_A22	93	94	DGND	P		
	D10	O	IFC_A24	95	96	IFC_A23	O	C9	
	E11	O	IFC_A26	97	98	IFC_A25	O	C10	
	D11	O	IFC_A28	99	100	IFC_A27	O	C11	
	D12	O	IFC_A30	101	102	IFC_A29	O	C12	
		P	DGND	103	104	IFC_A31	O	E12	
	D17	O	IFC_AVD	105	106	IFC_CS1#	O	E15	
	B14	O	IFC_TE	107	108	IFC_CS2#	O	D16	
	D13	O	IFC_WE0#	109	110	IFC_CS3#	O	C16	
	D15	O	IFC_OE#	111	112	DGND	P		
	A14	O	IFC_BCTL	113	114	IFC_CLE	O	F16	
	G8	I	TEST_SEL#	115	116	TCK	I	E18	
4.7 kΩ PU to VCC1V8	B2	O	ASLEEP	117	118	TMS	I	B18	
		O	STAT1	119	120	TDO	O	C18	
		O	STAT0/PGOOD	121	122	TDI	I	A18	
4.7 kΩ PU to VCC3V3	P5	I	DMA1_DREQ0#	123	124	TRST#	I	D19	
	U5	O	DMA1_DACK0#	125	126	IRQ00#	I	F7	4.7 kΩ PU to VCC1V8
	R5	O	DMA1_DDONE0#	127	128	IRQ01#	I	D3	4.7 kΩ PU to VCC1V8
4.7 kΩ PU to VCC3V3	V5	I	DMA2_DREQ0#	129	130	IRQ02#	I	E9	4.7 kΩ PU to VCC1V8
	AA5	O	DMA2_DACK0#	131	132	IRQ03#	I	D1	4.7 kΩ PU to VCC1V8
	Y5	O	DMA2_DDONE0#	133	134	IRQ04#	I	D4	4.7 kΩ PU to VCC1V8
		P	DGND	135	136	CLK_OUT	O	E6	22 Ω in-line
4.7 kΩ PU to VCC1V8	D5	I	IRQ05#	137	138	DGND	P		
4.7 kΩ PU to L1VDD	AB4	I	IRQ06#	139	140	SYSCLK	O		4.7 kΩ PD
4.7 kΩ PU to L1VDD	AD5	I	IRQ07#	141	142	DDRCLK	O		4.7 kΩ PD
4.7 kΩ PU to L1VDD	AB1	I	IRQ08#	143	144	DGND	P		
4.7 kΩ PU to L1VDD	AC5	I	IRQ09#	145	146	RTC	I	B17	
4.7 kΩ PU to CVDD	L4	I	IRQ10#	147	148	VDD_LP	I	P6	
4.7 kΩ PU to DVDD [3]	U3	I	IRQ11#	149	150	NC	--		Not connected
4.7 kΩ PU to VCC1V8	A3	O	IRQ_OUT#/EVT9#	151	152	DGND	P		
4.7 kΩ PU to VCC1V8	E8	O	HRESET#	153	154	SDHC_EXT_SEL#	I		10 kΩ PU to EVDD
330 Ω PD	F12	O	PROG_SFP	155	156	RCW_SRC_SEL	I		10 kΩ PU to VCC3V3SBY
	F13	O	PORESET#	157	158	RESET_REQ_OUT#	I/O		2.2 kΩ PU to VCC3V3
12 kΩ PU to VCC3V3		I	RESIN#	159	160	RESET_OUT#	O		1 kΩ PU to VCC3V3

3: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (3), Table 4-11, DVDD_VSEL.

3.2 Pinout connectors X1 to X3 (continued)

Table 3: Pinout X2

Remark	CPU ball	I/O	Signal	Pin		Signal	I/O	CPU ball	Remark
	P1	I	SPI_MISO	1	2	SDHC_DAT0_MOD	I/O		
	P2	O	SPI_MOSI	3	4	SDHC_DAT1_MOD	I/O		
	N1	O	SPI_CLK	5	6	DGND	P		
	M1	O	SPI_CS0#/SDHC_DAT4	7	8	SDHC_DAT2_MOD	I/O		
	M2	O	SPI_CS1#/SDHC_DAT5	9	10	SDHC_DAT3_MOD	I/O		
	M3	O	SPI_CS2#/SDHC_DAT6	11	12	SDHC_CMD_MOD	I/O		
	N3	O	SPI_CS3#/SDHC_DAT7	13	14	DGND	P		
	L5	I	SDHC_CD#	15	16	SDHC_CLK_MOD	I/O		
	M5	I	SDHC_WP	17	18	EMI1_MDC	O	AH3	
	AB6	I	TSEC_1588_TRIG_IN1	19	20	EMI1_MDIO	I/O	AH4	10 kΩ PU to L1VDD
	AE6	O	TSEC_1588_PULSE_OUT1	21	22	TSEC_1588_CLK_IN	I	AC8	
	AF5	O	TSEC_1588_ALARM_OUT1	23	24	TSEC_1588_CLK_OUT	O	AD7	
		P	DGND	25	26	TSEC_1588_TRIG_IN2	I	AE5	
	AF2	I	EC1_RXD0	27	28	TSEC_1588_PULSE_OUT2	O	AD8	
	AF1	I	EC1_RXD1	29	30	TSEC_1588_ALARM_OUT2	O	AC7	
	AE1	I	EC1_RXD2	31	32	EC2_RXD0	I	AH8	
	AD2	I	EC1_RXD3	33	34	EC2_RXD1	I	AG7	
	AC2	I/O	EC1_RX_ER	35	36	EC2_RXD2	I	AH7	
	AG2	I	EC1_RX_CTL	37	38	DGND	P		
	AD1	I	EC1_RX_CLK	39	40	EC2_RXD3	I	AH6	
		P	DGND	41	42	EC2_RX_CTL	I	AG8	
	AE3	O	EC1_TXD0	43	44	EC2_RX_CLK	I	AH5	
	AE4	O	EC1_TXD1	45	46	EC2_TXD0	O	AE7	
	AD3	O	EC1_TXD2	47	48	EC2_TXD1	O	AF7	
	AC3	O	EC1_TXD3	49	50	EC2_TXD2	O	AF6	
	AC4	I/O	EC1_TX_ER	51	52	EC2_TXD3	O	AG5	
	AF4	O	EC1_TX_CTL	53	54	DGND	P		
		P	DGND	55	56	EC2_TX_CTL	O	AF8	
	AC1	I/O	EC1_COL	57	58	EC2_GTX_CLK	O	AE8	
	AF3	O	EC1_GTX_CLK	59	60	EC2_GTX_CLK125	I	AC6	
	AG3	I	EC1_GTX_CLK125	61	62	DGND	P		
		P	DGND	63	64	SD1_TX0_P	O	AD10	
		P	DGND	65	66	SD1_TX0_N	O	AE10	
	AH10	I	SD1_RX0_P	67	68	DGND	P		
	AG10	I	SD1_RX0_N	69	70	DGND	P		
		P	DGND	71	72	SD1_TX1_P	O	AD11	
		P	DGND	73	74	SD1_TX1_N	O	AE11	
	AH11	I	SD1_RX1_P	75	76	DGND	P		
	AG11	I	SD1_RX1_N	77	78	DGND	P		
		P	DGND	79	80	SD1_TX2_P	O	AD13	

3.2 Pinout connectors X1 to X3 (continued)

Table 3: Pinout X2 (continued)

Remark	CPU ball	I/O	Signal	Pin		Signal	I/O	CPU ball	Remark
		P	DGND	81	82	SD1_TX2_N	O	AE13	
	AH13	I	SD1_RX2_P	83	84	DGND	P		
	AG13	I	SD1_RX2_N	85	86	DGND	P		
		P	DGND	87	88	SD1_TX3_P	O	AD14	
		P	DGND	89	90	SD1_TX3_N	O	AE14	
	AH14	I	SD1_RX3_P	91	92	DGND	P		
	AG14	I	SD1_RX3_N	93	94	DGND	P		
		P	DGND	95	96	SD1_TX4_P	O	AD16	
		P	DGND	97	98	SD1_TX4_N	O	AE16	
	AH16	I	SD1_RX4_P	99	100	DGND	P		
	AG16	I	SD1_RX4_N	101	102	DGND	P		
		P	DGND	103	104	SD1_TX5_P	O	AD17	
		P	DGND	105	106	SD1_TX5_N	O	AE17	
	AH17	I	SD1_RX5_P	107	108	DGND	P		
	AG17	I	SD1_RX5_N	109	110	DGND	P		
		P	DGND	111	112	SD1_TX6_P	O	AD19	
		P	DGND	113	114	SD1_TX6_N	O	AE19	
	AH19	I	SD1_RX6_P	115	116	DGND	P		
	AG19	I	SD1_RX6_N	117	118	DGND	P		
		P	DGND	119	120	SD1_TX7_P	O	AD20	
		P	DGND	121	122	SD1_TX7_N	O	AE20	
	AH20	I	SD1_RX7_P	123	124	DGND	P		
	AG20	I	SD1_RX7_N	125	126	DGND	P		
		P	DGND	127	128	SD1_REF_CLK1_P	I	AB14	
		P	DGND	129	130	SD1_REF_CLK1_N	I	AA14	
	AB18	I	SD1_REF_CLK2_P	131	132	DGND	P		
	AA18	I	SD1_REF_CLK2_N	133	134	DGND	P		
		P	DGND	135	136	IIC1_SCL_SPV	I/O		10 kΩ PU to VCC3V3SBY
4.7 kΩ PU to DVDD [4]	V2	I/O	IIC3_SCL	137	138	IIC1_SDA_SPV	I/O		10 kΩ PU to VCC3V3SBY
4.7 kΩ PU to DVDD [4]	W3	I/O	IIC3_SDA	139	140	IIC2_SCL	I/O	V3	4.7 kΩ PU to DVDD [4]
4.7 kΩ PU to DVDD [4]	AA3	I/O	IIC4_SCL	141	142	IIC2_SDA	I/O	Y3	4.7 kΩ PU to DVDD [4]
4.7 kΩ PU to DVDD [4]	AB3	I/O	IIC4_SDA	143	144	RES/EMI2_MDC	O		
		P	DGND	145	146	RES/EMI2_MDIO	I/O		
4.7 kΩ PU to VCC3V3		I	CLKOE	147	148	UART1_SIN#	I	AA1	
	W4	I	UART2_SIN#	149	150	UART1_SOUT#	O	AA2	
	AA4	O	UART2_SOUT#	151	152	DGND	P		
	Y1	O	UART3_SOUT#/UART1_RTS#	153	154	SOUT1	O		
4.7 kΩ PU to DVDD [4]	Y2	I	UART3_SIN#/UART1_CTS#	155	156	SOUT2	O		
	V4	O	UART4_SOUT#/UART2_RTS#	157	158	SIN1	I		
4.7 kΩ PU to DVDD [4]	Y4	I	UART4_SIN#/UART2_CTS#	159	160	SIN2	I		

4: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (3), Table 4-11, DVDD_VSEL.

3.2 Pinout connectors X1 to X3 (continued)

Table 4: Pinout X3

Remark	CPU ball	I/O	Signal	Pin		Signal	I/O	CPU ball	Remark
1 kΩ PU to VCC1V8	F9	I	SCAN_MODE#	1	2	EVT4#	I/O	C3	
4.7 kΩ PU to VCC1V8	F18	O	CKSTP_OUT#	3	4	EVT3#	I/O	C2	
4.7 kΩ PU to VCC1V8	F19	I	TMP_DETECT#	5	6	EVT2#	I/O	C1	4.7 kΩ PU to VCC1V8
	R6	I	RES/LP_TMP_DETECT#	7	8	EVT1#	I/O	C4	
		O	RTC_CLKOUT	9	10	EVT0#	I/O	D6	
2.2 kΩ PU to VCC3V3SBY		I/O	RTC_INT_OUT#	11	12	DGND	P		
10 kΩ PU to VCC3V3		I/O	TEMP_CRIT_MOD#	13	14	IFC_AD15	I/O	A13	
	C14	I/O	IFC_PAR1	15	16	IFC_AD14	I/O	A12	
	C15	I/O	IFC_PAR0	17	18	IFC_AD13	I/O	B12	
		P	DGND	19	20	IFC_AD12	I/O	A11	
4.7 kΩ PU to VCC1V8	E14	I	IFC_PERR#	21	22	IFC_AD11	I/O	B11	
	F17	O	IFC_WP0#	23	24	IFC_AD10	I/O	A10	
1 kΩ PU to VCC1V8	A15	I	IFC_RB1#	25	26	IFC_AD9	I/O	A9	
1 kΩ PU to VCC1V8	B15	I	IFC_RB0#	27	28	IFC_AD8	I/O	B9	
	A16	I/O	IFC_NDDQS	29	30	DGND	P		
	D14	O	IFC_NDDDR_CLK	31	32	IFC_CS7#	O	C19	4.7 kΩ PU to VCC1V8
		P	DGND	33	34	IFC_CS6#	O	D18	4.7 kΩ PU to VCC1V8
22 Ω in-line	A19	O	IFC_CLK1	35	36	IFC_CS5#	O	C17	4.7 kΩ PU to VCC1V8
22 Ω in-line	A17	O	IFC_CLK0	37	38	IFC_CS4#	O	E17	4.7 kΩ PU to VCC1V8
		P	DGND	39	40	IFC_CS0#/CS_NOR#	O	C13	4.7 kΩ PU to VCC1V8

Connector X3 is assembled by default, but can be omitted, if necessary. Contact TQ-Support for details.

3.3 Function blocks

3.3.1 CPU

The TQMT104x is developed as a platform for the CPUs T1042/22, T1040/20, T1024/14 and T2081.
Provided that nothing else is mentioned, the name T1042 stands for all supported derivatives, with and without Encryption.

Table 5: CPUs derivatives

CPU derivative	T1020	T1022	T1014 / T1024	T1040	T1042	T2081
QorIQ™ Platform	T1	T1	T1	T1	T1	T2
Cores	2 × e5500	2 × e5500	1 or 2 × e5500	4 × e5500	4 × e5500	4 × e6500 (dual-threaded)
Core Clock / MHz	1200 to 1500	1200 to 1500	Max. 1400	1200 to 1500	1200 to1500	1500 to 1800
I-Cache Size / Kbyte	32	32	32	32	32	32
D-Cache Size / Kbyte	32	32	32	32	32	32
L2 Cache Size / Kbyte	256	256	256	256	256	2048, shared
L3 Cache Size	256 Kbyte CoreNet	256 Kbyte CoreNet	256 Kbyte CoreNet	256 Kbyte CoreNet	256 Kbyte CoreNet	512 Kbyte CoreNet
Core data bus width	64 bit	64 bit	64 bit	64 bit	64 bit	64 bit
DDR 3/4 Support	32/64 bit DDR3L/4	32/64 bit DDR3L/4	32/64 bit DDR3L/4	32/64 bit DDR3L/4	32/64 bit DDR3L/4	64 bit DDR3/3L
Gbit Ethernet ports	4 × 1 Gbit + 8-Port switch	5 × 1 Gbit	1 × 10 Gbit, 3 × 1 Gbit	4 × 1 Gbit + 8-Port switch	5 × 1 Gbit	2 × 1/10 Gbit + 5 × 1 Gbit
SerDes lanes	8 (5 GHz)	8 (5 GHz)	4 (10 GHz)	8 (5 GHz)	8 (5 GHz)	8 (10 GHz)
PCIe controller	4 × Gen-2	4 × Gen-2	3 × Gen-2	4 × Gen-2	4 × Gen-2	1 × Gen-3 + 3 × Gen-2
TDM	On QUICC Engine	On QUICC Engine	On QUICC Engine	On QUICC Engine	On QUICC Engine	No
IEEE 1588	Yes, v2	Yes, v2	No	Yes, v2	Yes, v2	Yes, v2
SDHC / MMC	Yes	Yes	Yes	Yes	Yes	Yes
USB H/D/O	2 × 2.0 w/PHY	2 × 2.0 w/PHY	2 × 2.0 w/PHY	2 × 2.0 w/PHY	2 × 2.0 w/PHY	2 × 2.0 w/PHY
Local Bus	16 bit IFC	16 bit IFC	16 bit IFC	16 bit IFC	16 bit IFC	IFC
Security Engine	v5.x	v5.x	v5.x	v5.x	v5.x	v5.x
Secure boot	Yes	Yes	Yes	Yes	Yes	Yes
FPU	DP	DP	DP	DP	DP	DP
I^2C	4 ×	4 ×	4 ×	4 ×	4 ×	4 ×
SPI	Yes	Yes	Yes	Yes	Yes	Yes
UART	2 × DUART	2 × DUART	2 × DUART	2 × DUART	2 × DUART	2 × DUART
GPIO	Yes	Yes	Yes	Yes	Yes	Yes
Standard-Temp T_J Industrial-Temp T_J	0 °C to +105 °C –40 °C to +105 °C	0 °C to +105 °C –40 °C to +105 °C	0 °C to +105 °C –40 °C to +105 °C	0 °C to +105 °C –40 °C to +105 °C	0 °C to +105 °C –40 °C to +105 °C	0 °C to +105 °C –40 °C to +105 °C
MIPS	3.0 DMIPS/MHz	3.0 DMIPS/MHz	3.0 DMIPS/MHz	3.0 DMIPS/MHz	3.0 DMIPS/MHz	6.0 DMIPS/MHz
Power Consumption	Typ. 5 W	Typ. 4.5 W	Typ. 4 W	Typ. 6 W	Typ. 5.5 W	Max. 25 W
Power Management	Yes, Deep Sleep	Yes, Deep Sleep	Yes, Deep Sleep	Yes, Deep Sleep	Yes, Deep Sleep	Yes
SATA	2 ×	2 ×	2 ×	2 ×	2 ×	No
LCD interface (DIU)	Yes	Yes	Yes	Yes	Yes	No
Technology	28 nm	28 nm	28 nm	28 nm	28 nm	28 nm
Other	QUICC Engine	QUICC Engine	QUICC Engine	QUICC Engine	QUICC Engine	AltiVec SIMD
Package	780-pin FCBGA 23 × 23 mm^2 0.8 mm pitch	780-pin FCBGA 23 × 23 mm^2 0.8 mm pitch	780-pin FCBGA 23 × 23 mm^2 0.8 mm pitch	780-pin FCBGA 23 × 23 mm^2 0.8 mm pitch	780-pin FCBGA 23 × 23 mm^2 0.8 mm pitch	780-pin FCBGA 23 × 23 mm^2 0.8 mm pitch

3.3.1.1 CPU derivatives

All CPUs listed are pin compatible.
The TQMT104x also supports the following CPU derivatives: T1020, T1022, T1024/14, T1040, and T2081 [5].

3.3.1.2 CPU configuration

The CPU is configured to a small extent by pins and for the greater part by software.

3.3.1.3 CPU power management

3.3.1.3.1 CPU power management modes

Table 6: Power management modes

Mode	Name	Characteristics
PH10	Doze	Instruction execution (per Thread) stopped; peripheral completely active, Wake-Up by interrupt, Cache Snooping active
PH15	Nap	Instruction execution (per Core) stopped, internal clocks switched off, no Cache Snooping ⇨ Cache Coherency not guaranteed
LPM10	Full On	At least one Core not in PH10 mode (Full On State)
LPM20	Sleep	Internal clocks switched off, periphery partly active for Wakeup
LPM35	Deep Sleep	Like “Sleep”, but various supplies are shut down
–	"RAM Only"	A further possible condition of the TQMT104x (not the CPU): Only RAM content is preserved, CPU completely switched off

3.3.1.3.2 Deep Sleep

Deep Sleep is an especially efficient energy saving mode (LPM35), a variation of the LPM20, in which parts of the Core supply are switched off. LPM35 is supported by the T1042/22, T40/20, T1024/14 CPUs, it is not supported by the T2081 CPU.
The transition to Deep Sleep is a complex multistage process, which is partly controlled by the software and partly by a software-configurable CPU-internal State Machine.

3.3.2 Reset logic, Reset LED, voltage supervision

The reset logic contains the following functions:

- Monitoring of voltages used on the TQMT104x
- External Reset input
- PGOOD output (e.g., for Power-Up of external PHYs)

A Reset condition is indicated by a LED. When RESET_OUT# is low, the LED lights up. The RESET_REQ_OUT# pulse is extended for at least 200 ms. Thereby the reset condition is visible even if the reset pulse at RESIN# is very short.

3.3.3 Reset Configuration Word

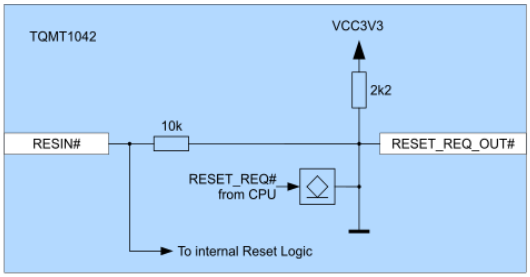
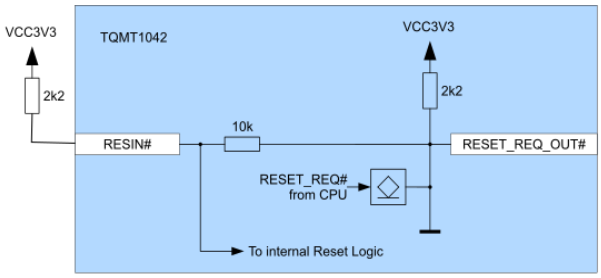
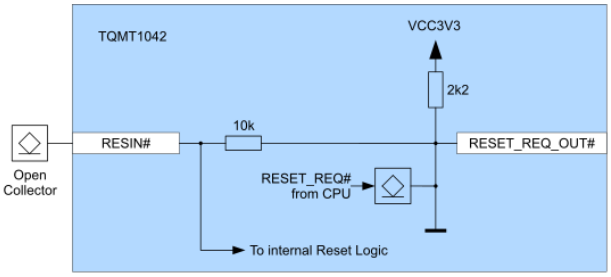
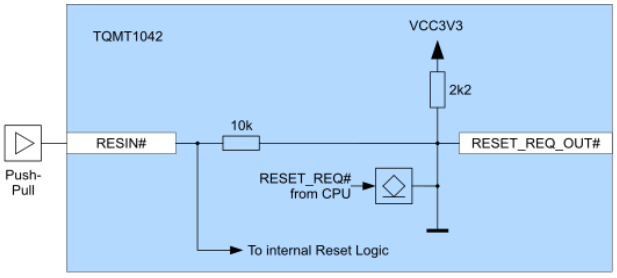
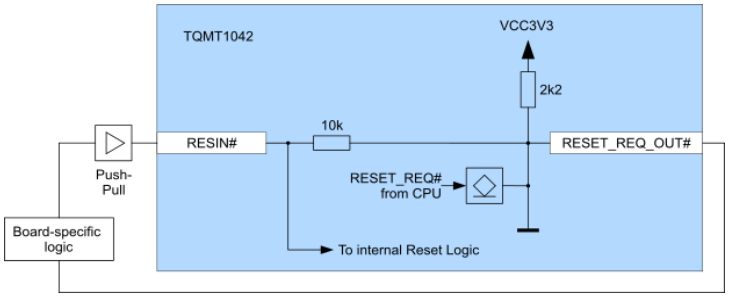
The Reset Configuration Word (RCW) is passed to the CPU as a memory structure.
The Reset Configuration Word contains 512 bits. If applicable the customer has to adapt it to match his application.
NXP provides the tool “QorIQ Configuration and validation Suite 4.2”, utilizing a graphical interface, free of charge (registration required).

5: Suitable modules are available on request.

3.3.4 Self-reset

The following RESIN# wirings show different possibilities to connect RESIN#.

Table 7: RESIN# connection

Self-Reset performed when RESET_REQ# asserted.	
No Self-Reset performed when RESET_REQ# asserted.	
Self-Reset performed when RESET_REQ# asserted, external reset signal connected to RESIN#.	
No Self-Reset performed when RESET_REQ# asserted, external reset signal connected to RESIN#.	
Self-Reset via external reset signal using additional logic.	

3.3.4 Self-reset (continued)

The following table shows the reset options, depending on the RESIN# signal wiring.

Table 8: Reset options

Wiring at RESIN#	Reset function
Open-Drain	Self-Reset possible Logic Low at RESIN# triggers RESET
Open, or Pull-up ≥47 kΩ to 3.3 V	Self-Reset possible RESET_REQ# can trigger RESIN# on TQMT104x
Pull-up <10 kΩ to 3.3 V	**No** Self-Reset possible RESET_REQ# cannot trigger RESIN# on TQMT104x
Push/Pull driver	**No** Self-Reset, but external RESET possible Logic High at RESIN# overrides RESET_REQ# on TQMT104x

3.3.5 Boot sources

The boot source can be selected by applying different voltage levels at pin RCW_SRC_SEL (X1-156).
By default a 10 kΩ PU to VCC3V3SBY is assembled on the TQMT104x.
The following table gives an overview over the different boot sources:

Table 9: Boot sources

Level	RCW_SRC_SEL	Reset Configuration Source	Remark
0 % to 25 %	Tied to GND	eMMC/SD card	Depending on signal SDHC_EXT_SEL#
25 % to 50 %	5.6 kΩ PD	(Reserved)	(Do not use)
50 % to 75 %	15 kΩ PD	I^2C EEPROM	Address `0x50 / 101 0000b`
75 % to 100 %	NC	Default: NOR flash on TQMT104x	10 kΩ PU to VCC3V3SBY on TQMT104x

3.3.6 Pre boot-loader PBL

The PBL provides an additional possibility to configure the CPU. It uses the same data structure as the RCW, or extends it.
For details see (3), Table 27-2. In contrast to the example shown there, an additional CRC should be added directly after the RCW if the PBL is used.

3.3.7 eMMC / SD card

The information provided in this User's Manual applies to both an eMMC [6], and an SD card, (which is not part of the TQMT104x, but provided on the Starterkit).
The data bus width of an SD card is limited to 4 bits; the option with 8 bits only applies to eMMC.
Maximum data rate with MTFC4GMDEA-1M WT:

- 8 Bit data bus width: 8 Bit × 2 × 52 MHz = 832 Mbit/s
- 4 Bit data bus width: 4 Bit × 2 × 52 MHz = 416 Mbit/s

6: The eMMC is an assembly option and not assembled by default.

3.3.8 I²C bus

The I²C bus on the TQMT104x operates at 3.3 V and is clocked with 400 kHz. All I²C bus devices on the TQMT104x are connected to I²C bus 1 of the CPU. The pull-ups available on the TQMT104x are sufficient for the bus loads on the TQMT104x. If more devices are connected to the bus on the carrier board, additional pull-ups must be assembled on the carrier board, to meet the I²C specification.

Table 10: I2C1 device addresses

Device	Function	7-bit address
M24256	EEPROM	0x57 / 101 0111b
SE97B	EEPROM (Normal Mode)	0x50 / 101 0000b
	EEPROM (Protection Mode)	0x30 / 011 0000b
	Temperature sensor	0x18 / 001 1000b
PCF85063A	RTC	0x51 / 101 0001b
SA560004EDP [7]	Temperature sensor [7]	0x4C / 100 1101b
ADM1068	Supervisor	0x44 / 100 0100b
MKL04Z16	System Controller	0x11 / 001 0001b

3.3.8.1 EEPROM M24256

An EEPROM M24256 is assembled on the TQMT104x. It is connected to I²C bus 1 of the CPU and clocked with 400 kHz.
The device address is 0x57 / 101 0111b, see Table 10. The EEPROM is empty at delivery.

3.3.8.2 Temperature sensor / EEPROM SE97B

A temperature sensor including a 256 byte EEPROM is connected to I²C bus 1. The I²C addresses are shown in Table 10.
The EEPROM contains TQMT104x-specific data at delivery, which is shown in Table 11.
The lower 128 bytes (00h to 7Fh) containing the TQMT104x-specific data, can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software. The upper 128 bytes (80h to FFh) are not write protected and can be used for general purpose data storage.

Table 11: TQMT104x-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
0x00	(Unused)		$32_{(10)}$	–	–
0x20	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	First MAC address
0x30	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
0x40	(Variable)	(Variable)	$32_{(10)}$	ASCII	Order code
0x60	(Unused)		$32_{(10)}$	–	(Unused)
0x80	(Unused)		$128_{(10)}$	–	–

The SE97B also provides a temperature sensor to monitor the temperature of the TQMT104x, it is assembled on the top side of the TQMT104x between the SDRAMs, see Illustration 5, (D13).
The following table shows details of the temperature sensor.

Table 12: Temperature sensor SE97B

Manufacturer	Part number	Resolution	Accuracy	Temperature range
NXP	SE97B	11 bits	Max. ±1 °C Max. ±2 °C Max. ±3 °C	+75 °C to +95 °C +40 °C to +125 °C –40 °C to +125 °C

7: Address is compatible to ADT7461, LM86, MAX6657/8 and ADM1032.

3.3.8.3 RTC PCF85063A

An RTC PCF85063A is assembled on the TQMT104x since the CPU has no bufferable internal RTC.

Characteristics of the RTC:

- Linux Kernel Driver is available: cateee.net/lkddb/
- I²C clock frequency 400 kHz
- Supplied by V_{IN}; battery buffering is possible (battery on carrier board, see Illustration 2)
- Alarm output INTA# routed to the connector and to the system controller for wake-up option
- Control via I2C1 controller, device address is `0x51 / 101 0001b`, see Table 10.
- Quartz FC-135, tolerance 20 ppm @ +25 °C
  ⇨ approx. 30 ppm @ –40 °C to +85 °C
  ⇨ 2.6 seconds / day, ≈ 16 min / year

Table 13: RTC, Quartz

Device	Type	Manufacturer	Ext. Temp.
PCF85063ATL/1,118	RTC, 400 kHz, I²C, calendar, Alarm, DFN2626-10	NXP	Yes
FC-135 32,768KHZ-20-12,5	Quartz 32.768 kHz, 20 ppm, 12.5 pF	Epson Toyocom	Yes

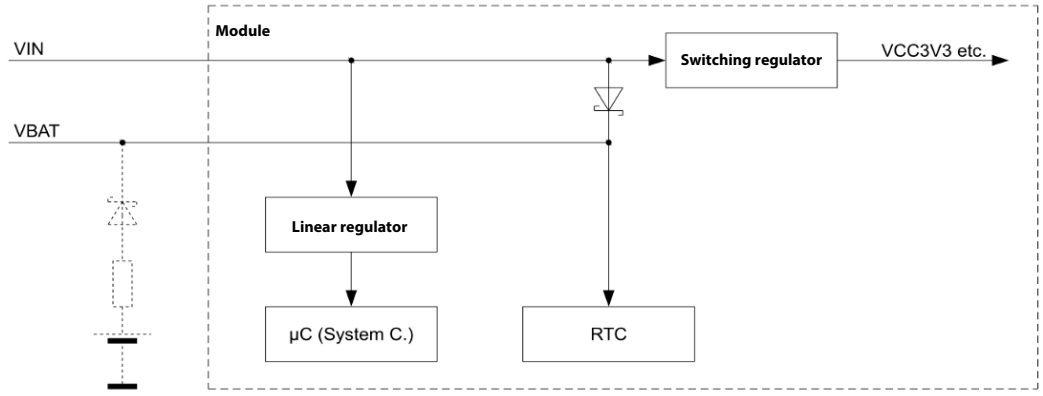


Illustration 2: RTC buffering

3.3.8.4 Temperature monitoring

It is mandatory to monitor the temperatures on account of the TQMT104x power consumption, to guarantee a reliable operation within the specified limits and that the specified operating conditions are met.

The temperature-critical components are the CPU and the DDR3-SDRAM on top and bottom side.

The CPU temperature is measured by the integrated measuring diode, which is connected to the external channel of the SA56004.

The DDR3L temperature on the bottom side of the TQMT104x is measured by the internal sensor of the SA56004.

The alarm outputs (Open Drain) are all connected together. They have a common Pull-Up, and are routed to signal TEMP_OS#.

The SA56004 is controlled by the I²C bus 1 of the CPU, device address is `0x4C / 100 1101b`, see Table 10.

The DDR3L temperature on the top side of the TQMT104x is measured by the combined temperature sensor / EEPROM SE97B (D13), see Illustration 5 and 3.3.8.2.

3.4 Supply

3.4.1 Power sequencing

The TQMT104x has to be supplied with 5 V ±5 %. All other voltages are generated on the TQMT104x.
The correct power sequencing is ensured by the TQMT104x.

3.4.2 Power outputs and inputs

Certain TQMT104x I/O voltages can be used. All I/O voltages that are supported by the T1042 can be selected.
I/O voltages may be Off in Deep Sleep (use switched I/O voltage) or always on (non-switched).
The voltages are selected by connecting one of the TQMT104x's I/O voltage outputs to the respective I/O voltage input.

- Power inputs CVDD, DVDD [8], and EVDD have to be connected to VCC3V3F, VCC3V3S, VCC1V8F, or VCC1V8S of the TQMT104x, depending on the I/O voltage required and whether the voltage is switched (…S) or not (…F).
- Power inputs LVDD, and L1VDD have to be connected to VCC3V3F, VCC3V3S, VCC2V5F, VCC2V5S, VCC1V8F, or VCC1V8S of the TQMT104x, depending on the I/O voltage required and whether the voltage is switched (…S) or not (…F)
- Power input USB_HVDD has to be connected to VCC3V3F, or VCC3V3S of the TQMT104x, depending on whether the voltage is switched (…S) or not (…F).
- Power input USB_OVDD has to be connected to VCC1V8F, or VCC1V8S of the TQMT104x, depending on whether the voltage is switched (…S) or not (…F).
- Power input USB_SVDD has to be connected to VDD, or VDDC of the TQMT104x, depending on whether the voltage is switched (VDD) or not (VDDC)

The following illustration shows a possible connection of TQMT104x power outputs and inputs.

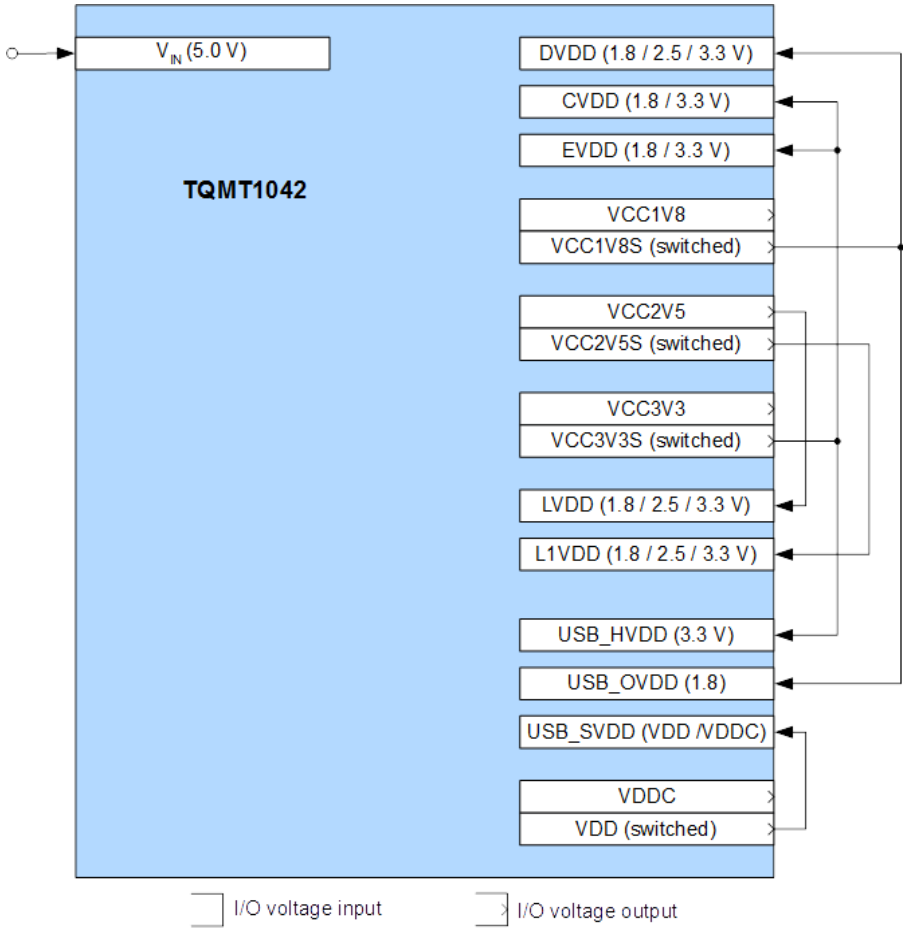


Illustration 3: TQMT104x power outputs and inputs

8: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (3), Table 4-11, DVDD_VSEL.

3.4.2 Power outputs and inputs (continued)

Above illustration shows the following configuration:

- DVDD uses 1.8 V, switched
- CVDD and EVDD use 3.3 V, switched
- LVDD uses 2.5 V, always on
- L1VDD uses 2.5 V, switched
- USB_HVDD, USB_OVDD, and OSB_SVDD use switched voltages

Note: DVDD I/O voltage level, output usage, RCW adaption	
	Only use TQMT104x's I/O voltage outputs to supply TQMT104x's I/O voltage inputs. The DVDD I/O voltage is set to 3.3 V by default. The RCW has to be adapted in case the DVDD I/O voltage is changed, i.e. to 1.8 V. See (3), Table 4-11, DVDD_VSEL.

3.4.3 Power consumption

The typical power consumption of a TQMT1042-AA (with 2GB SDRAM) is approximately 8 Watt.

3.5 Interfaces to other systems and devices

3.5.1 Serial interfaces

- UART1 to UART4, two UARTs (UART1 and UART2) with RTS/CTS signals
- Default assembly: RS-232 driver for UART1 and UART2
- Max. 115,200 Baud (limited by driver)
- All UART signals are also routed unbuffered to the TQMT104x connectors
- RS-232 driver for 2 × RxD and 2 × TxD are buffered, RTS and CTS (multiplexed with UART3, UART4) are not buffered.

3.5.2 COP/JTAG interface and AURORA

The AURORA interface is a high speed extension of the traditional ("Legacy") debug interface.
The full NXP COP/JTAG interface (debugging interface) is routed to the TQMT104x connectors.
They are routed to a shrouded header on the STKT104X:

- "Legacy": Double row, 16-pin, 2.54 mm header
- AURORA, e.g., ASP-137969-01 STC:
  Pinout includes all "Legacy" interface signals (22 pins), as well as the High-Speed-Lanes.

3.5.3 Display interface

If display colours are not mapped correctly, please contact TQ-Support.

3.5.4 IFC

Avoid stubs of more than 30 mm at the IFC signals. This compromises the IFC signal integrity on the TQMT104x.

3.5.5 General purpose I/O

Most I/O signals provided by the TQMT104x can be configured as GPIOs. There are no dedicated GPIOs.

3.5.6 Local bus, other interfaces

All signals are routed to three connectors with a total of 360 pins. (2 × 160 pins (X1, X2), 1 × 40 pins (X3)).
The Local Bus signals are mainly routed to X3. If the Local Bus is not used and if the space is required, X3 can be omitted.

3.6 Cooling

3.6.1 Power dissipation

Since the TQMT104x power consumption is significant, special care must be taken when designing the cooling method.
The TQMT104x power consumption details can be looked up in 3.4.

3.6.2 Heatsink

The heatsink required depends on the use case (CPU used, clock frequency, stack height, ambient temperature, and airflow) and can therefore not be determined universally. In the following is a theoretical calculation for the TQMT1042:

P_TDP_ TQMT1042 = 12 W, P_TDP_CPU = 9 W

R_th_max = (T_J_max – T_A_max) / P_TDP_CPU = (105 – 35) K / 9 W ≈ 8 K/W

In case the heat sink was removed from the TQMT104x and has to be mounted again, extreme care has to be taken to achieve optimal thermal connection between the CPU and the heat sink.
This can be achieved by using e.g. Phase-Change-Material Chomerics THERMFLOW® T725.

Attention: Destruction or malfunction, TQMT104x heat dissipation	
	The CPU on the TQMT104x belongs to a performance category in which cooling is essential. It is the user's sole responsibility to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). The CPU die on the TQMT104x is mechanically extremely sensitive! Under all circumstances avoid pressure at the edges of the die!

3.7 Notes of treatment

To avoid damage caused by mechanical stress, the TQMT104x may only be extracted from the carrier board by using the extraction tool MOZIP2020, which can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMT104x for the extraction tool MOZIP2020.

4. SOFTWARE

The TQMT104x comes with a preinstalled boot loader U-Boot and a TQ-BSP, which is tailored for the STKT104x.
The boot loader U-Boot provides TQMT104x-specific as well as STKT104x-specific settings, e.g.:

- Clocks
- CPU configuration
- Driver strengths
- eMMC configuration
- Multiplexing
- Pin configuration
- PMIC configuration
- RAM configuration and timing

More information can be found in the TQMT104x Support Wiki.

5. MECHANICS

5.1 TQMT104x connectors

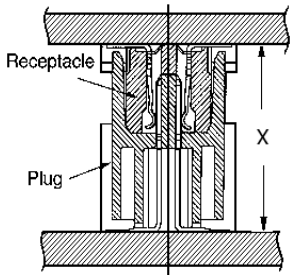
The TQMT104x is connected to the carrier board with 360 pins on three connectors.
The following table shows details of the connector used.

Table 14: Connectors on the TQMT104x

Manufacturer	Part number	Description	Package
TE connectivity	5177985-1	1 × 40-pin connector (receptacle)	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C
	5177985-8	2 × 160-pin connector (receptacle)	• 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMT104x is held in its mating connectors by the pins (a total of 360) with a retention force of approximately 36 N.
It is strongly recommended to use the extraction tool MOZIP2020 to remove the TQMT104x from the carrier board to avoid damaging the TQMT104x connectors as well as the carrier board connectors. See chapter 5.7 for further information.
The following table shows some suitable mating connectors for the carrier board.

Table 15: Carrier board mating connectors

Manufacturer	Part number	Remark	Stack height (X)	
TE connectivity	40-pin: 5177986-1 160-pin: 5177986-8	On STKT104x	5 mm	
	40-pin: 1-5177986-1 160-pin: 2-5179230-8	–	6 mm	
	40-pin: 2-5177986-1 160-pin: 5179030-8	–	7 mm	
	40-pin: 3-5177986-1 160-pin: 3-5177986-8	–	8 mm	

5.2 TQMT104x dimensions

The TQMT104x has dimensions of 74 × 54 mm².
The drawing shows the TQMT104x from the top **through** the PCB. This is equivalent to the footprint on the carrier board.

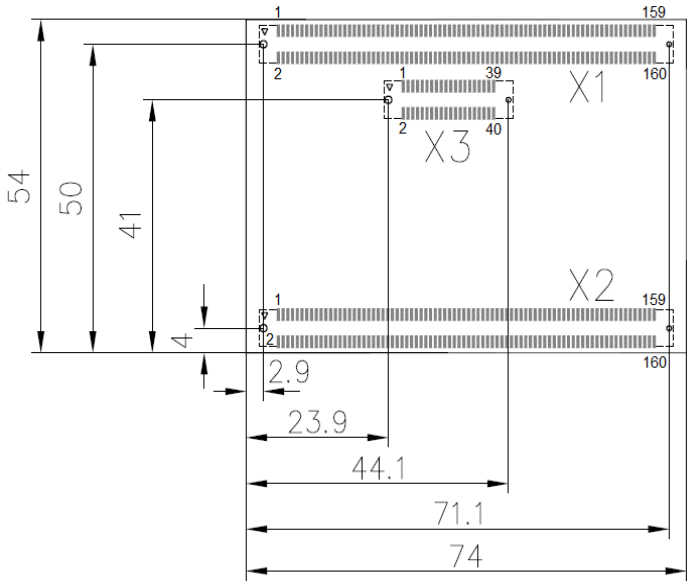


Illustration 4: TQMT104x dimensions, top view **through** TQMT104x

5.3 TQMT104x component placement

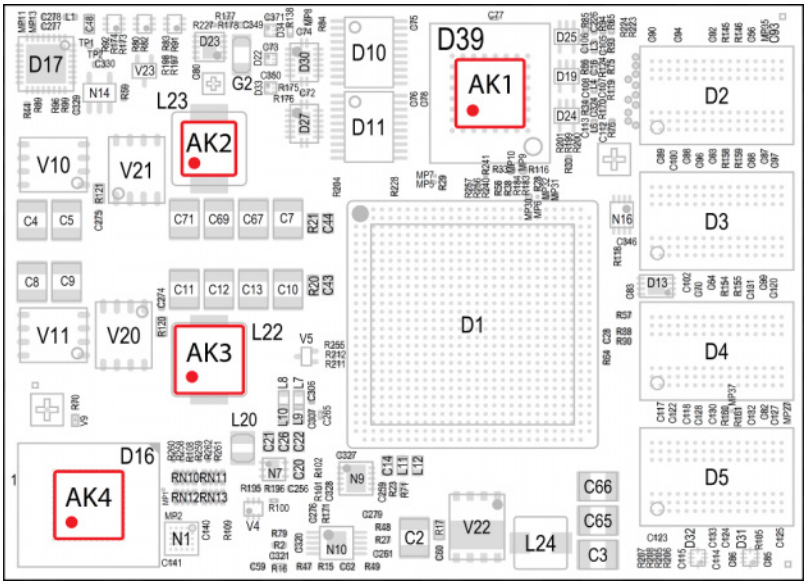


Illustration 5: TQMT104x, component placement top

The labels on the TQMT104x show the following information:

Table 16: Labels on TQMT104x

Label	Text
AK1	First MAC address (+ additional reserved MAC addresses)
AK2	Serial number
AK3	TQMT104x version and revision
AK4	Tests performed

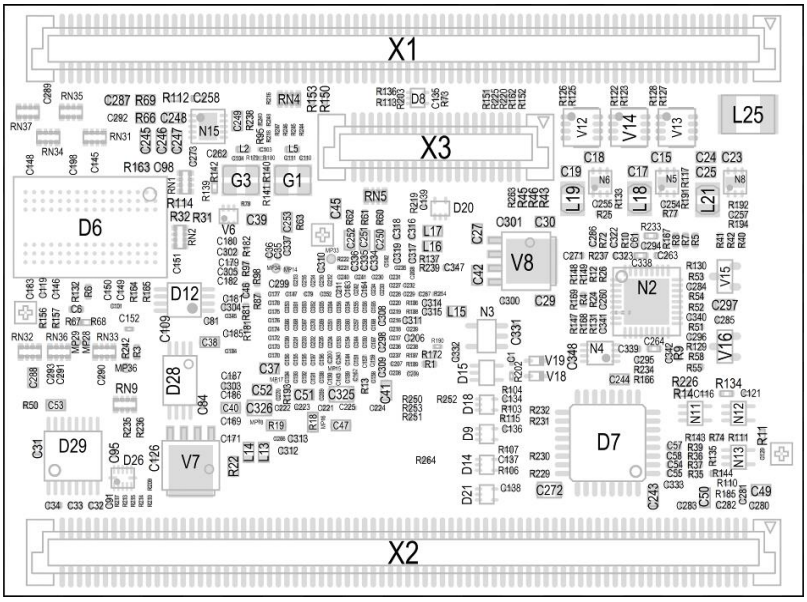


Illustration 6: TQMT104x, component placement bottom

5.4 Protection against external effects

As an embedded module the TQMT104x is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

To cool the TQMT104x, a theoretical maximum of approximately 12 W have to be dissipated, see also section 3.4.
The power dissipation originates primarily in the CPU, and the DDR3L SDRAM.
The power dissipation also depends on the software used and can vary according to the application.
See NXP and Intel Application Notes (8), (9), (10), and (12) for further information.

Attention: Destruction or malfunction, TQMT104x heat dissipation	
	The CPU on the TQMT104x belongs to a performance category in which cooling is essential. It is the user's sole responsibility to define a suitable cooling method depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). The CPU die on the TQMT104x is mechanically extremely sensitive! Under all circumstances avoid pressure at the edges of the die!

5.6 Structural requirements

The TQMT104x is held in its mating connectors by the pins (a total of 360) with a retention force of approximately 36 N.
For high requirements with respect to vibration and shock firmness an additional holder has to be provided in the final product to hold the TQMT104x in its position. For this purpose TQ-Systems GmbH can provide a suitable solution. As no heavy and big components are used, no further requirements are given.

5.7 Notes of treatment

To avoid damage caused by mechanical stress, the TQMT104x may only be extracted from the carrier board by using the extraction tool MOZIP2020 that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMT104x for the extraction tool MOZIP2020.

6. OPERATIONAL CONDITIONS

6.1 Climatic conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the whole assembly.

In general, a reliable operation is given when following conditions are met:

Table 17: Climate and operational conditions standard temperature range 0 °C to +70 °C

Parameter	Range	Remark
T_j temperature CPU T104x	0 °C to +105 °C	–
Case temperature DDR3L SDRAM	0 °C to +95 °C	–
Case temperature other ICs	0 °C to +70 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Table 18: Climate and operational conditions industrial temperature range –40 °C to +85 °C

Parameter	Range	Remark
T_j temperature CPU T104x	–40 °C to +105 °C	–
Case temperature DDR3L SDRAM	–40 °C to +95 °C	–
Case temperature other ICs	–40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the thermal characteristics of the CPU is to be taken from the NXP data sheets (3) and (4).

The TQMT104x is not protected against dust, external impact and contact (IP00). Adequate protection has to be guaranteed by the surrounding system.

6.2 Reliability and service life

No detailed MTBF calculation has been done for the TQMT104x.

The theoretical MTBF of the TQMT104x is approximately 1 / FIT = 1 / (800 × 10^{-9} / h) = 1,250,000 h at +40 °C, ground benign.

The TQMT104x is designed to be insensitive to vibration and impact.

High quality industrial grade connectors are assembled on the TQMT104x.

Detailed information concerning the service life of the CPU under different operational conditions is to be taken from the NXP Application Notes (11) and (14).

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

The TQMT104x was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board; connect all TQMT104x DGND pins.
- A good connection between PCB ground and housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short;
  avoid interference of other signals by distance and / or shielding, do not route tracks over separating trenches
- Filtering of all signals, which can be connected externally (also "slow signals" and DC can radiate RF indirectly)

7.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMT104x. According to the data sheets, the devices used already have some protection; however, this is generally not sufficient to meet the legal requirements without any further measures. The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signals: RC filtering, perhaps Zener diode(s)
- Fast signals: Integrated protective devices (e.g., suppressor diode arrays)

7.3 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

7.4 Environment protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimized by suitable measures. Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material. Due to the fact that at present there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material); such printed circuit boards are still used. No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications regarding this were not carried out.

7.5 RoHS

The TQMT104x is manufactured RoHS compliant.

- All components and assemblies used are RoHS compliant
- RoHS compliant soldering processes are used

7.6 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMT104x was designed to be recyclable and easy to repair.

7.7 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as TQ-Systems GmbH is informed by suppliers accordingly.

7.8 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMT104x must therefore always be seen in conjunction with the complete device.

7.9 Batteries

No batteries are used on the TQMT104x.

7.10 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMT104x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimized by suitable measures. The TQMT104x is delivered in reusable packaging.

7.11 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimized by suitable measures.

Printed PC-boards are delivered in reusable packaging.

Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 19: Acronyms

Acronym	Meaning
BIOS	Basic Input/Output System
BSP	Board Support Package
COP	Common On-Chip Processor
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DC	Direct Current
D-Cache	Data Cache
DDR3L	Double Data Rate 3 Low voltage
DIN	German industry standard (Deutsche Industrie Norm)
DIU	Display Interface Unit
DMA	Direct Memory Access
DMIPS	Dhrystone Million Instructions Per Second
DP	Double Precision
DUART	Debug Universal Asynchronous Receiver/Transmitter
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (Flash)
EN	European Standard (Europäische Norm)
ESD	Electrostatic Discharge
EuP	Energy using Products
FCBGA	Flip-Chip Ball Grid Array
FIT	Failure In Time
FPU	Floating-Point Unit
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
I-Cache	Instruction Cache
IEEE®	Institute of Electrical and Electronics Engineers
IFC	Integrated Flash-Controller
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JEDEC®	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPM	Low-Power Mode
LSB	Least Significant Bit
MIPS	Million Instructions Per Second
MMC	Multimedia Card

8.1 Acronyms and definitions (continued)

Table 19: Acronyms (continued)

Acronym	Meaning
MOZI	Modulzieher (module extractor)
MSB	Most Significant Bit
MTBF	Mean operating Time Between Failures
NC	Not Connected
NOR	Not-Or
O	Output
P	Power
P/I	Power In
P/O	Power Out
PBL	Pre Boot Loader
PCB	Printed Circuit Board
PCIe	PCI Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up
PWP	Permanent Write Protect
QUICC	Quad Integrated Communications Controller
R/W	Read/Write
RAM	Random Access Memory
RC	Resistor / Capacitor
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorization (and restriction of) Chemicals
RF	Radio Frequency
RISC	Reduced Instruction Set Computing
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
RWP	Reversible Write Protect
SATA	Serial ATA
SD card	Secure Digital Card
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SIMD	Single Instruction, Multiple Data
SM-bus	System Management Bus
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TDM	Time-Division Multiplexing
TSEC	Three-Speed Ethernet Controller
TSSOP	Thin-Shrink Small Outline Package
UART	Universal Asynchronous Receiver/Transmitter
U-Boot	Universal Bootloader
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment

8.2 References

Table 20: Further applicable documents

No.	Name	Rev., Date	Company
(1)	T1042, T1022 QorIQ Advanced Multicore Processor, Document Number T1042, T1022	Rev. 0, 01/2015	NXP
(2)	T1040, T1020 QorIQ Advanced Multicore Processor, Document Number T1042, T1022	Rev. 0, 01/2015	NXP
(3)	QorIQ T1040 Reference Manual, Document Number T1040RM	Rev. 0, 01/2015	NXP
(4)	T2081 QorIQ Integrated Multicore Communications Processor, Document Number T2081	Rev. 0, 01/2015	NXP
(5)	T2080 Integrated Multicore Communications Processor Family, Reference Manual Preliminary, NXP Confidential Proprietary, Document Number T2080RM	Rev. D, 07/2014	NXP
(6)	QorIQ T1024, T1014 Data Sheet, Product Preview / Preliminary, NXP Confidential Proprietary, Document Number T1024, T1014	Rev. D, 09/2014	NXP
(7)	QorIQ T1024 Reference Manual Preliminary, NXP Confidential Proprietary, Document Number T1024RM	Rev. A, 04/2014	NXP
(8)	Assembly Handling and Thermal Solutions for Leadless Flip Chip Ball Grid Array Packages Application Note, Document Number AN4871	Rev. 0, 02/2014	NXP
(9)	DDR4: The Right Memory for Your Next Server and High-End Desktop System IDF14	SPCS009, 09/2014	Intel
(10)	JEDEC® Standard DDR3 SDRAM Specification JESD79-3	F, 07/2012	JEDEC
(11)	JEDEC® Standard Addendum No. 1 to JESD79-3 - 1.35 V DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866	No.1, 07/2010	JEDEC
(12)	T1040 Family Design Checklist Application Note, Document Number AN4825	Rev. A, 01/2014	NXP
(13)	STKT104X User's Manual	– current –	TQ-Systems
(14)	Support-Wiki for the TQMT104x	– current –	TQ-Systems

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