For Technology
in Quality

User's Manual

TQM5200S

TQM5200S UM 301

12.10.2010

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Revision history

Rev.:	Date:	Name:	Pos.:	Modification:
001	04.09.2010	VJU		Created
002	07.09.2006	ROE		Review and Revision
200	05.10.2006	ROE		Revision update
201	16.02.2007	ROE	4.1.13	PSC2 replaced by PSC3
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1. About this manual

1.1 Tips on Safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.2 Terms and Conventions

Symbol / Tag	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed with the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages greater than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
Filename.ext	This specification is used to state the complete file name with its corresponding extension.
`Instructions / Examples`	Examples of an application. e.g., • specifying memory partitions • processing a script • .....
Reference	Cross-reference to another section, figure or table.

Table 1: Terms and conventions

1.3 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the system's power supply is switched off. Violation of this guideline may result in damage / destruction of the module and be dangerous to your health. Improper handling of your TQ-product renders the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing and use ESD-safe tools, packing materials etc. and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

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2. Product Idea

While designing the TQM5200S, particular importance has been given to the compact dimensions. With just 56 × 60 mm², the TQM5200S has a very compact form factor. Apart from requiring less space on the target hardware, it also has advantages with mechanical stress, e.g. shock or vibration. Robustness and industrial suitability were also important criteria according to which the connector system of the module was selected. Based on experience, a 0.8 mm mezzanine connector system is used.

3. Functionality and System Architecture

The TQM5200S is a Minimodule with MPC5200B PowerPC CPU (Freescale). As compared to the TQM5200, no graphic functionality is implemented.

Since the PCB of the TQM5200S is shorter than the TQM5200, the second SDRAM bank as well as the graphics controller and the plug connectors are not present. Therefore a maximum SDRAM size of 128 Mbyte is possible.

As a new system component, a temperature sensor is connected to the I²C bus.

3.1 System Architecture / Block Diagram

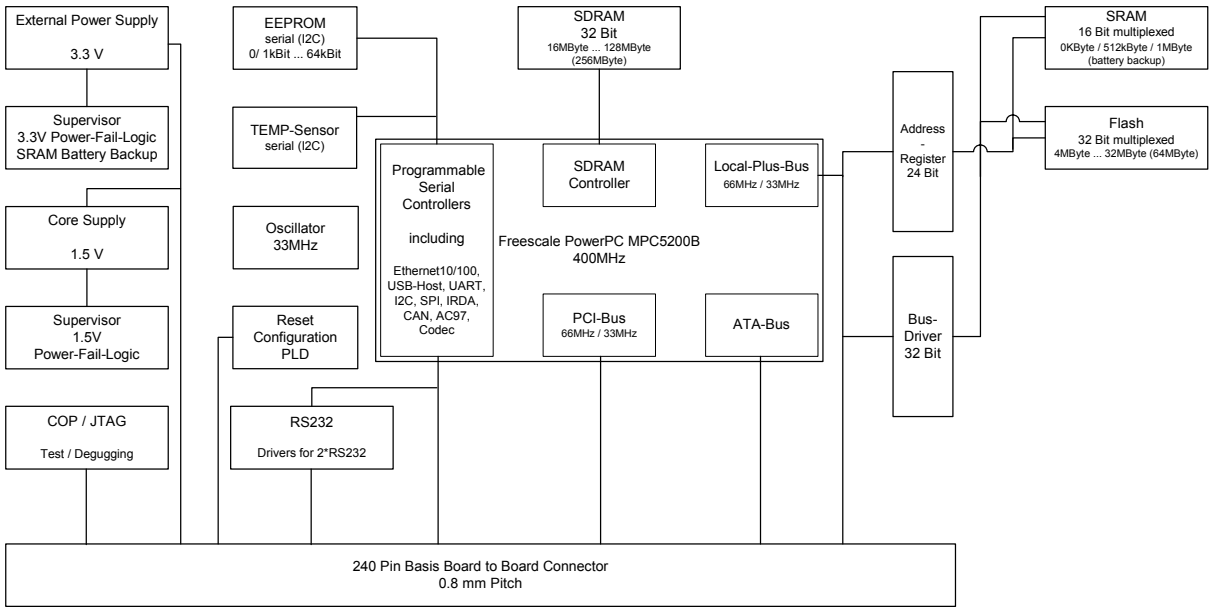

Illustration 1: TQM5200S Block Diagram

3.2 System Components

The board contains the following system components:

- Freescale PowerPC processor MPC5200B up to 400 MHz with MPC603e processor core
- 33 MHz oscillator for CPU clock
- SDRAM: 16 Mbyte to 128 Mbyte; 32 bit data bus width
- Flash: 4 Mbyte to 32 Mbyte[1], 32 bit data bus width
- SRAM: no SRAM, 512 Kbyte, or 1 Mbyte, 16 bit data bus width
  Possibility for battery back-up via battery supply from the target hardware
- Serial EEPROM: 0 Kbit or 64 Kbit, I²C bus
- CPLD for Reset-configuration and control of SRAM
- Driver for two serial interfaces (RxD, TxD)
- 32 bit bus driver and 24 bit address register for module components at the Local-Plus-Bus
- COP/JTAG interface
- Single power supply 3.3 V
- Switch-mode DC/DC converter on-board (3.3 V to 1.5 V)
- 1.5 V supervisor / power-fail logic
- 3.3 V supervisor / power-fail logic with SRAM battery backup
- 240 pin Board-to-Board plug system

All pins of the PowerPC processors are routed to the two 120 pin Board-to-Board connectors, except the SDRAM interface and the XTAL pins.

Transceivers for Ethernet, USB, CAN, etc… (except RS232 transceivers), are not assembled on the module. If necessary, drivers can be implemented on the target hardware.

4. Electronics Specification

The module is supplied with 3.3 V DC. The processor core voltage (1.5 V) is generated from the input voltage (3.3 V) on the module with a voltage regulator.

As a standard product, the TQM5200S is specified for a temperature range of 0 °C to +70 °C. Optionally it is also available for a temperature range of –40 °C to +85 °C.

[1] 32 Mbyte linear addressable; 64 and 128 Mbyte via bank select bits addressable

4.1 System Components

4.1.1 CPU

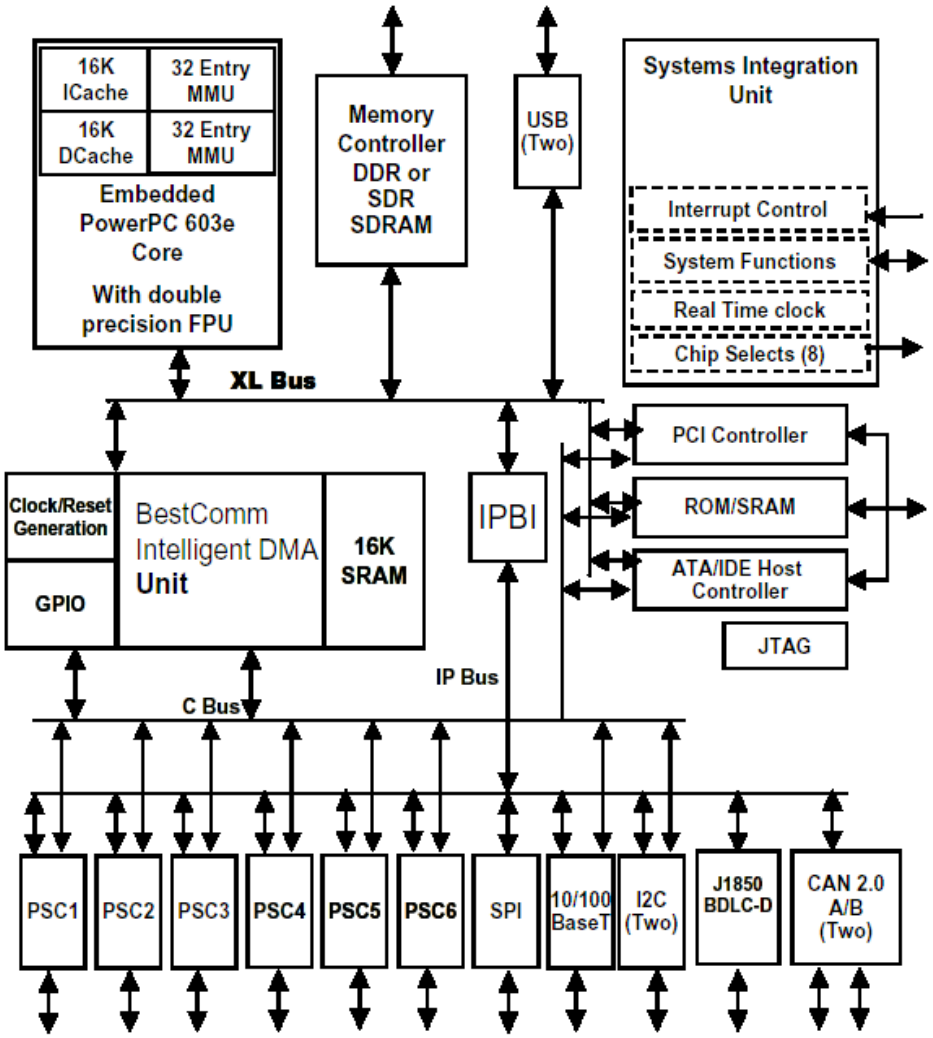

Illustration 2: Processor Block Diagram

The module offers the following features:

CPU Core

- MPC603e series G2_LE core
- Superscalar architecture
- 760 MIPS at 400 MHz (–40 °C to +85 °C)
- 450 MIPS at 264 MHz (–40 °C to +105 °C)
- 16 k Instruction cache, 16 k Data cache
- Double precision FPU
- Instruction and Data MMU
- Standard & Critical interrupt capability

SDRAM Memory Interface

- Up to 133 MHz operation
- 128 Mbyte addressing range
- 32 bit data bus
- Built-in initialization and refresh

External Bus Interface

- Supports interfacing to ROM/Flash/SRAM memories or other memory mapped devices
- 8 programmable Chip Selects
- Non multiplexed data access using 8/16/32 bit data bus with up to 26 bit address
- Short or Long Burst capable
- Multiplexed data access using 8/16/32 bit data bus with up to 25 bit address

Peripheral Component Interconnect (PCI) Controller

- Version 2.2 PCI compatibility
- PCI initiator and target operation
- 32 bit PCI address / data bus
- 33 and 66 MHz operation
- PCI arbitration function

ATA Controller

- Version 4 ATA compatible external interface
- ATA Software Reset via PSC1.4.
  If this feature is used, do not use PSC1.4 for other functions!

Six Programmable Serial Controllers (PSCs)

- UART or RS232 interface
- CODEC interface for Soft Modem, Master/Slave CODEC Mode, I2S and AC97
- Full duplex SPI mode
- IrDA mode from 2400 bps up to 4 Mbps

Fast Ethernet Controller (FEC)

- Supports 100 Mbps IEEE 802.3 MII, 10 Mbps IEEE 802.3 MII, 10 Mbps 7-wire interface

Universal Serial Bus Controller (USB)

- Version 1.1 Host only
- Support for two independent USB slave ports

Two Inter-Integrated Circuit Interfaces (I²C)

Serial Peripheral Interface (SPI)

Dual CAN 2.0 A/B Controller (MSCAN)

- Motorola Scalable Controller Area Network (MSCAN) architecture
- Implementation of version 2.0A/B CAN protocol
- Standard and extended data frames

J1850 Byte Data Link Controller (BDLC)

- J1850 Class B data communication network interface compatible and ISO compatible for low Speed (<125kbps) serial data communications in automotive applications.
- Supports 4× mode, 41,6 kbps
- In-frame response (IFR) types 0, 1, 2 and 3 supported

Component	Manufacturer	Type	Temperature Range
MPC5200CVR400B	Freescale	400 MHz PPC	–40 °C to +85 °C

Table 2: CPU

! note !	**The functions described here are not available simultaneously. The PSCs functions are multiplexed. More information about it can be found in section 2 of the MPC5200 User-Manual.**

4.1.2 CPU-Power-On Reset Configuration

In the table shown below, the described adjustments are made as per the rising edges of HRESET# and a Hold-Time of two clock cycles (SYS_XTAL) of CPU pins; and are stored in the CDM Reset Configuration register. The adjusted configuration cannot be changed when the CPU is running.

The Reset configuration is set by a CPLD. During the Reset phase, the configuration is set at the configuration pins of the CPU until the rising edge of the HRESET#. Afterwards the CPLD outputs are changed to high impedance. Wrong adjustment can render the system to be no longer bootable.

With the settings established, the PLL configuration is among the things that are of concern. This configuration determines the XL bus Frequency and the CPU core frequency. Settings for PCI and Local-Plus-Bus are derived from the XL bus frequency and can be changed at run-time. Further boot settings are made here, which apply only to data accesses over Boot-CS#. The access over Boot-CS0# to CS5# can be changed at runtime.

Warning! The default values specified in Table 3 are qualified for the module TQM5200S. The settings of the deviating values takes place at one's own risk and without guarantee on the part of TQ Components GmbH. Malfunctions as well as destruction of the module cannot be excluded with deviating configurations.

Reset Config Pin RST_CFGx	TQM5200S Start-up Config.	CDM Reset Config Register Bit PORCFG[x]	I/O Signal Name	Config Signal from CDM	Description
0	0	31	ATA_DACK#	ppc_pll_cfg_4	MPC5200 G2_LE PPC Core PLL Configuration
1	0	30	ATA_IOR#	ppc_pll_cfg_3	
2	0	29	ATA_IOW#	ppc_pll_cfg_2	
3	1	28	LP_RW	ppc_pll_cfg_1	
4	0	27	LP_ALE#	ppc_pll_cfg_0	
5	0	26	LP_TS#	xlb_clk_sel	Bit=0: XLB_CLK=SYS_PLL F_{VCO}/4 Bit=1: XLB_CLK=SYS_PLL F_{VCO}/8
6	0	25	USB1_1	sys_pll_cfg_0	Bit=0: SYS_PLL F_{VCO}=16 × SYS_PLL_FREF Bit=1: SYS_PLL F_{VCO}=12 × SYS_PLL_FREF
7	0	24	USB1_2	sys_pll_cfg_1	Bit=0: VCO = SYS_PLL_VCO Bit=1: VCO = 2xSYS_PLL_FVCO
8	0	23	ETH0	boot_rom_mg	Bit=0: No Boot in Most Graphics Mode Bit=1: Boot in Most Graphics Mode
	0	21	ETH2	ppc_msrip	Microprocessor Boot Address/Exception table location Bit=0: 0000_0100 (hex) Bit=1: FFF0_0100 (hex)
11	1	20	ETH3	boot_rom_wait	Bit=0: 4 PCI bus clocks of wait state Bit=1: 48 PCI bus clocks of wait state
12	0	19	ETH4	boot_rom_swap	Bit=0: No byte lane swap, same endian ROM image Bit=1: Byte lane swap, different endian ROM image
13	1	18	ETH5	boot_rom_size	For non-muxed boot ROMs: Bit=0: 8bit boot ROM data bus, 24bit max boot ROM address bus Bit=1: 16bit boot ROM data bus,16bit boot ROM address bus For muxed boot ROMs: 2,3 boot ROM address is max 25 significant bits during address tenure. Bit=0: 16bit ROM data bus Bit=1: 32bit ROM data bus
14	1	17	ETH6	boot_rom_type	Bit=0: non-muxed boot ROM bus, single tenure transfer. Bit=1: muxed boot ROM bus, with address and data tenures, ALE and TS active
15	0	16	ETH1	large_flash_sel	Bit=0: No Boot in Large Flash Mode Bit=1: Boot in Large Flash Mode

Table 3: Reset Configuration

4.1.3 CPU-Clock generation

On the module, one oscillator and one crystal oscillator are present:

- 33 MHz oscillator for the CPU
- 32.768 kHz crystal oscillator for the RTC of the MPC5200.
  To use this RTC, the 3.3 V supply voltage of the module must be available. In order to reduce the quiescent current input for a system, it is recommended to implement an external RTC on the target hardware. An external RTC can be connected e.g. via the I²C bus.

All clock frequencies required by the CPU are generated CPU-internal derived from the 33 MHz oscillator.

Component	Manufacturer	Type	Temperature Range
SX03-0507-E-50-W-33.000 MHz	THE	Oscillator 33 MHz	–40 °C to +85 °C
MC306	Epson / Seico	Crystal oscillator 32.768 kHz	–40 °C to +85 °C

Table 4: Crystal oscillators for MPC5200

The clock frequencies for the TQM5200S module are derived from the 33 MHz input clock and set by the Reset configuration register to generate the following frequencies:

- XLB-Clk: 132 MHz
- IPB-Clk: 132 MHz
- PCI-Bus-Clk: 66 MHz
- Core-Clk: 396 MHz

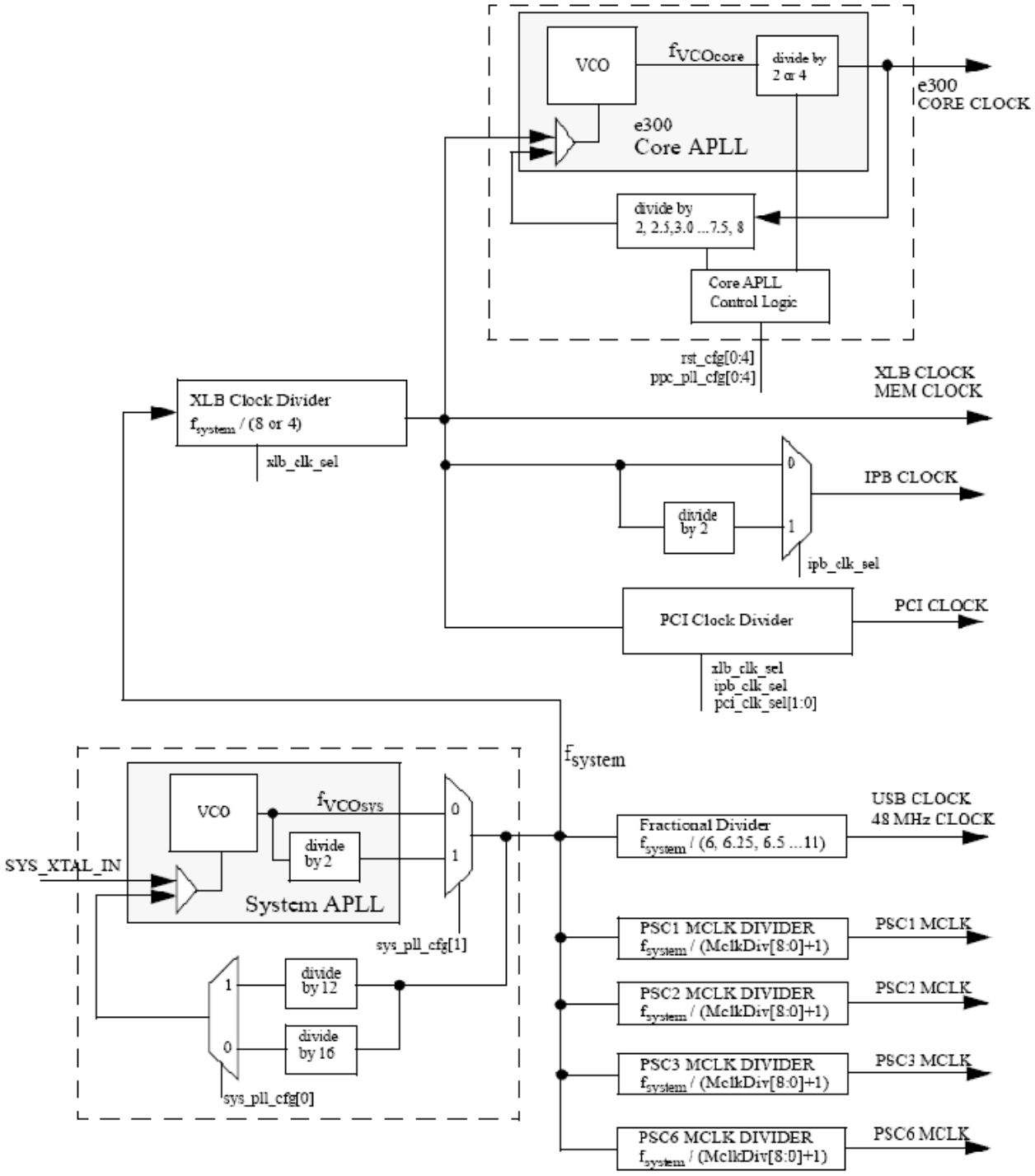

Illustration 3: MPC5200B Clock Relations

4.1.4 CPLD

A Lattice ispMach4064V 5T48I is used as CPLD in a 48 pin TQFP housing.

In addition to the CPU-Power-On Reset Configuration described above, the CPLD generates two Byte-Select signals for the SRAM.

Component	Manufacturer	Type	Temp. range
ispMach4064V 5T48I	Lattice	CPLD 64 macro cells	–40 °C to +85 °C

Table 5: CPLD

The JTAG pins of the CPLD are connected to the module pins of the TQM5200S described in the following table.

Signal	Module-Pin	Direction	Description
TCK_PLD	X3-118	I	CPLD-JTAG-Interface
TDI_PLD	X3-115	I	CPLD-JTAG-Interface
TDO_PLD	X3-116	O	CPLD-JTAG-Interface
TMS_PLD	X3-117	I	CPLD-JTAG-Interface
DVCC3V3	VCC3V3	–	Supply
DGNDG	GND	–	Ground

Table 6: TQM5200S CPLD-JTAG-Interface

4.1.5 Temperature Monitoring

- Monitors the CPU temperature indirectly, using a temperature sensor on the soldering side of the PCB near the CPU
- Sensor LM75
- The switching output of LM75 is routed to the Board-to-Board connectors

Control via I²C bus (I2C_2SCL / I2C_2SDA); address lines on 0b000; I²C bus is shared with the EEPROMs as the address parts are fixed and there is no address collision with EEPROMs.

Component	Manufacturer	Type	Temperature Range
LM75CIMM-3	National Semiconductor	I²C, 400 kHz, 3 Addr., MSOP8 (0.65 mm)	–40 °C to +85 °C

Table 7: Temperature Sensor

4.1.6 Address Register

All bus subscribers which are connected to the Local-Plus-Bus in multiplexed mode (SRAM, flash) require an address register with up to 25 bit width. The addresses are locked with the address register with the rising edge of the inverted LP_ALE# signal.
As a latch the positive edge triggered register 74LVC16374 is used.

Component	Manufacturer	Type	Temperature Range
SN74LVC16374 DGG	TI	16 bit D-Latch	–40 °C to +85 °C

Table 8: Address Register

4.1.7 Bus Driver

Bus drivers are installed, to prevent a bus overload. This bus is divided into Local-Plus, ATA and PCI bus. Two 16 bit bus drivers type 74ALVC16245A are used. The bus drivers are activated with the signals Boot-CS#, CS0# (flash) and CS2# (SRAM).
The change of direction is controlled by the LP_RW# signal.

Component	Manufacturer	Type	Temperature Range
74ALVC16245A	Philips	16 bit bus driver	–40 °C to +85 °C

Table 9: Bus Driver

4.1.8 Flash Memory

- 3.3 V Flashes, 16 bit
- 1 bank with two devices and a bus width of 32 bit
- Connected at the multiplexed Local-Plus-Bus. The address signals are connected via a 25 bit address register, the data signals via a 32 bit bus driver
- The ALE# signal is configured as “long”
- Eight wait states are used for accessing the flash memory
- Memory sizes of 4 Mbyte to 32 Mbyte, using the Bank-Select bits 64 / 128 Mbyte
- Access time 120 ns
- The signal Boot-CS# (physical CS0#) is used as chip select to boot from Flash. The configuration for CS0 is described in Table 10

The status signal RY/BY# of the Flash is not used, i.e. the write and delete cycles must be checked by polling the Flash status bits (DQ7#, Toggle bits etc.).

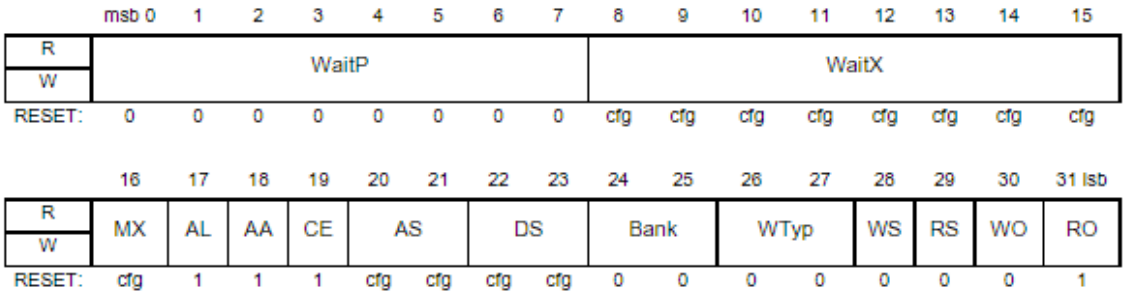

Illustration 4: Chip Select 0 / Boot Configuration Register—MBAR + 0x0300

Chip Select 0 / Boot Configuration Register

Bits	Name	Setting	Description
0:7	WaitP	0x00	Number of wait states to insert. Can be applied as a prescale to WaitX or used by itself, as specified by WTyp bits below. Wait states control how many PCI clocks the corresponding CS pin remains active.
8:15	WaitX	0x08	Base number of wait states to be inserted, or combined with WaitP as specified by WTyp bits below. cfg operation—If rstcfg[11] (on pad_eth_03) is zero then 4 wait states are in effect, else 48 wait states are in effect. Wait States equals the number of PCI clocks from CS assertion to when data must be valid from boot device.
16	MX	1	MX bit specifies whether a transaction operates as multiplexed or non-multiplexed. A multiplexed transaction presents address and data in different tenures. During the address tenure, ALE is asserted. At the end of ALE, AD bus is switched to data tenure and CSx pin is asserted. 0=Non-multiplexed 1=Multiplexed cfg operation—If rstcfg[14] on pad_eth_06 is low, boot operation is non-multiplexed (Single tenure), else boot operation is multiplexed (dual tenure).
17	AL	1	ALE length—multiplexed transactions only 0=ALE width is 1 internal IP bus clock 1=ALE width is 2 internal IP bus clocks At boot time, internal IP bus clock is twice the frequency of the PCI clock. Therefore, AL defaults to 1 (2 IP bus clocks) for boot device.
18	AA	0	ACK Active—multiplexed transactions only. This bit defines whether ALE input is active or not. If AA is 1, programmed wait states can be overridden when/if the external device drives the ACK input low. If AA is 0, the ACK input is ignored. Wait states are still in effect. If no ACK is received, cycle terminates at end of wait state period. cfg operation—If rstcfg[14] on pad_eth_06 is high, indicating multiplexed mode boot device, then AA is assumed high as well. This lets the boot device shorten the Wait State period by asserting the ACK input.
19	CE	1	An individual Enable bit—allows CS operation for the corresponding CS pin. CE must be high to allow operation. Register 6 master enable bit must also accept when CS [0] is used for boot ROM. 1 = Enable 0 = Disabled, register writes can occur but no external access is generated.
20:21	AS	11	Address Size field—defines size of peripheral address bus (in bytes) and must be consistent with physical connections. 00 = 8 bits 01 = 16 bits 10 = 24 bits 11 = 25 bits See documentation for Physical Connection requirements. The combination of address size, data size, and transaction type (MX) must be consistent with the peripheral physical connection. In case of a multiplexed transaction, the entire address is driven regardless of address size field. cfg operation—If rstcfg[13] on pad_eth_05 is low, then the address size for non-multiplexed boot device is set to 24 bits (AS=10), else the boot device is treated as a 16 bit address (AS=01) device. For multiplexed mode boot devices the maximum 25 bits of address is always driven. This rstcfg bit more particularly affects the DS field below, and can be thought of as the “small” or “big” data size config bit.
22:23	DS	11	Data Size field—represents the peripheral data bus size (in bytes): 00 = 1Byte 01 = 2Bytes 10 = 3Bytes (Not Supported) 11 = 4Bytes cfg operation—If rstcfg[13] on pad_eth_05 is low, then the data size for non-multiplexed boot device is set to 8 bits (DS=00), else the boot device is treated as a 16 bit (DS=01) device. For multiplexed mode boot device the selection is 16 bit data or 32 bit data respectively.
24:25	Bank	00	Bank bits—are reflected on external AD lines (AD[26:25]) during address tenure of a multiplexed transaction. Register bit 24 is the msb and appears on AD[26].
26:27	WTyp	11	Wait state Type bits—define the application of wait states contained in WaitP and WaitX fields, as follows: 00 = WaitX is applied to read and write cycles (WaitP is ignored). 01 = WaitX is applied to Read cycles; WaitP is applied to Write cycles. 10 = WaitX is applied to Reads; WaitP/WaitX (16-bit value) is applied to Writes. 11 = WaitP/Waitx (as a full 16-bit value) is applied to Reads and Writes.

Bits	Name	Setting	Description
28	WS	0	Write Swap bit—If high, Endian byte swapping occurs during writes to a peripheral. • For 8-bit peripherals, this bit has no effect. • For 16-bit peripherals, byte swapping can occur. • For 32-bit peripherals (possible in MUXed mode only) byte swap can occur. 1 = swap 0 = NO swap 2-byte swap is AB to BA; 4-byte swap is ABCD to DCBA. NOTE: Transactions at less than the defined port size (i.e. data size) apply swap rules as above, according to the current transaction size.
29	RS	0	Read Swap bit—Same as WS, but swapping is done when reading data from a peripheral. 1 = swap 0 = NO swap cfg operation—If rstcfg[12] on pad_eth_04 is low, data from the boot device is Endian swapped when read. This only has effect for boot devices configured as 16- or 32-bit data size.
30	WO	0	Write Only bit—If bit is high, the peripheral is treated as a write-only device. An attempted read access results in a bus error (as dictated by Chip Select Control Register EBEE bit) and/or an interrupt (as dictated by Chip Select Control Register IE bit). In any case, no transaction is presented to the peripheral. A bus error means the internal cycle is terminated with a transfer error acknowledge (ips_xfr_err assertion to IP bus, TEA assertion to XL bus).
31	RO	0	Read Only bit—If bit is high, the peripheral is treated as a read-only device. An attempted write access results in a bus error (as specified by Chip Select Control Register EBEE bit) and/or an interrupt (as specified by Chip Select Control Register IE bit). In any case, no transaction is presented to the peripheral. NOTE: This bit is high from Reset, indicating Boot Device is Read-Only.

Table 10: Chip Select 0 / Boot Configuration Register

Component	Manufacturer	Model	Temperature Range
K8P2815UQB-EI4B	Samsung	Flash MirrorBit, 16 M × 16	–40 °C to +85 °C

Table 11: Flash-Memory component

These devices have a 64-ball-Fortified-BGA housing with dimensions of 13 × 11 mm.

4.1.9 Diagnosis-LED

A red LED is provided to indicate CPU-Reset.

4.1.10 SRAM

- One memory bank with 16 bit bus width
- Memory capacity 512 kByte or optional 1 Mbyte
- Access time 70ns
- Battery buffering via module connector (Standby-Power consumption, max. 20 µA)
- The SRAM is connected via an address register and a bus driver to the multiplexed Local-Plus-Bus of the processor
- The ALE# signal is configured as “long”
- Four wait states are used for accessing the SRAM
- Signal CS2# is used for SRAM selection

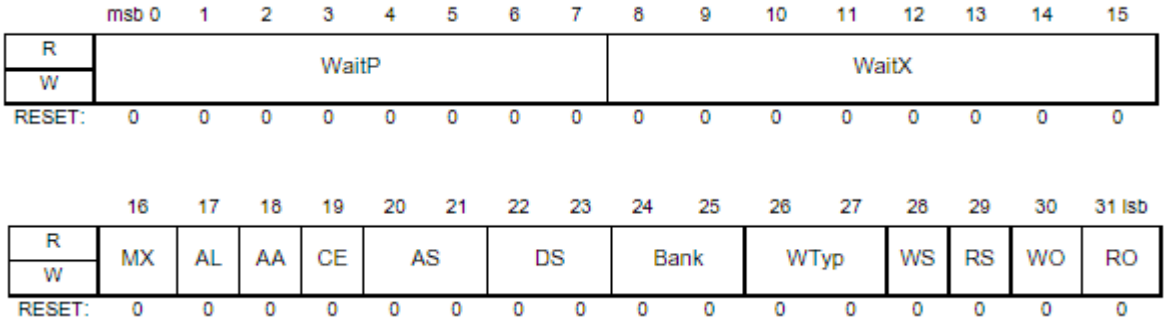

Illustration 5: Chip Select 2 Configuration Register—MBAR + 0x0308

Bits	Name	Setting	Description
0:7	WaitP	0x00	Number of Wait States
8:15	WaitX	0x04	The base number of wait states
16	MX	1	MX bit specifies whether transaction operates as multiplexed or non-multiplexed
17	AL	1	ALE Length
18	AA	0	ACK Active
19	CE	1	Chip Enable bit
20:21	AS	11	Address Size field
22:23	DS	01	Data Size field
24:25	Bank	00	Bank bits
26:27	Wtyp	11	Wait state Type bits
28	WS	0	Write Swap bit
29	RS	0	Read Swap bit
30	WO	0	Write Only bit
31	RO	0	Read Only bit

Table 12: Chip Select 2 Configuration Register

Component	Manufacturer	Type	Temperature Range
K6X4016T3F-TF70	Samsung	SRAM, 4 Mbit	–40 °C to +85 °C
K6X8016T3B-TF70	Samsung	SRAM, 8 Mbit	–40 °C to +85 °C
IS62WV25616BLL-55TLI	ISSI	SRAM, 4 Mbit	–40 °C to +85 °C
IS62WV51216BLL-55TLI	ISSI	SRAM, 8 Mbit	–40 °C to +85 °C

Table 13: SRAM Memory Component

4.1.11 EEPROM

The serial EEPROM can e.g. store the characteristics of the module and customer specific parameter data non-volatile. As against flash, individual memory cells can be deleted and overwritten in the EEPROM. At delivery the EEPROM is erased.

- Size 0 to 64 Kbit
- Control via I²C bus 2 of the CPU (I2C_2SCL / I2C_2SDA)
- 10 kΩ Pull-up resistors at I2C_2SCL and I2C_2SDA
- Address lines of EEPROM at 0b000

Component	Manufacturer	Model	Temperature Range
M24C01WDW6	ST Microelectronics	1-K EEPROM / TSSOP8	–40 °C to +85 °C
M24C02WDW6	ST Microelectronics	2-K EEPROM / TSSOP8	–40 °C to +85 °C
M24C04WDW6	ST Microelectronics	4-K EEPROM / TSSOP8	–40 °C to +85 °C
M24C08WDW6	ST Microelectronics	8-K EEPROM / TSSOP8	–40 °C to +85 °C
M24C16WDW6	ST Microelectronics	16-K EEPROM / TSSOP8	–40 °C to +85 °C
M24C32WDW6	ST Microelectronics	32-K EEPROM / TSSOP8	–40 °C to +85 °C
M24C64WDW6	ST Microelectronics	64-K EEPROM / TSSOP8	–40 °C to +85 °C

Table 14: Serial EEPROM

4.1.12 SDRAM

- Two memory devices with a bus width of 16 bit each
- Chip-Select through Mem_CS0
- 132 MHz clock
- 1 memory bank, 32 bit wide
- Memory sizes: 16 Mbyte to 128 Mbyte
- CAS Latency 3

When the mode-, control- and configuration register of the Micron 48LC16M16A2-75 SDRAM are programmed the following parameters must be taken into consideration:

4.1.12.1 Parameter for SDRAM-Controller Configuration

Description	Setting	Unit
Type of memory	SDR	–
XLB speed	132	MHz
CAS (Read) latency	3	Clock Cycles
THZ	5.4	ns
TDQSSmin	0	tCK
TWR	15	ns
TRCD	20	ns
TRFC	66	ns
TREF	64	ms
TREFI	7.8125	µs
#ROWs	8192	–
Mode Register Type	Normal	–
Generate a Mode Register Set command	Yes	–
Self Refresh Mode	No	–
Automatic Refresh	Yes	–
Extend Row and Column	Yes	–
Precharge Control	A10	–
Drive Rule for MDQ and MDQS	Drive except to read	–
MDQS OE Mask	0	–
Mode Register Locked	No	–
Soft Refresh	No	–
Soft Precharge All	No	–

Table 15: Parameter for SDRAM Controller Configuration

The following register settings result from the above described parameters:

- Mode Register (MBAR+0x0100) ⇨ 0x008D0000
- Control Register (MBAR+0x0104) ⇨ 0xD14F0000
- Configuration Register 1 (MBAR+0x0108) ⇨ 0xD2322800
- Configuration Register 2 (MBAR+0x010C) ⇨ 0x8AD70000

The description of the individual register bits can be found in section 8 SDRAM Memory Controller of the MP5200 User Manual [2].

The allocated SDRAM components are specified in the following table.

4.1.12.2 SDRAM components

Component	Manufacturer	Type	Temperature Range
MT48LC32M16A2TG 75 (K4S511632M-TC75)	Micron	SDRAM, 32 M × 16	0 °C to +70 °C
MT48LC16M16A2TG 75 (K4S561632E-TI75)	Micron	SDRAM, 16 M × 16	–40 °C to +85 °C
MT48LC8M16A2TG 75 (K4S281632E-TI75)	Micron	SDRAM, 8 M × 16	–40 °C to +85 °C
MT48LC4M16A2TG 75 (K4S641632E-TI75)	Micron	SDRAM, 4 M × 16	–40 °C to +85 °C

Table 16: SDRAM components (selection all released components)

4.1.13 Serial Interfaces

The internal UART PSC1 or optional the UART PSC6 of the MPC5200B is connected via an RS232-compatible transceiver (RxD / TxD channel) to the Board-to-Board connector.
It is configurable by placing 0 Ω resistors, irrespective of which of the two UARTs is used.

The internal UART PSC3 is connected via the RS232 transceiver to the Board-to-Board connector (RxD / TxD channel). Optionally the PSC3 UART can be detached by removing two 0 Ω resistors. The RS-232 interfaces offer a maximum speed of 115200 Baud.

RS232		UART		
Signal name	**Connector**	**Signal name**	**CPU-Port**	**Connector**
RS232_TxD_1	X3-72	UART1_TXD	PSC1_0	X3-65
RS232_RxD_1	X3-71	UART1_RXD	PSC1_1	X3-63
RS232_TxD_2	X3-76	UART3_TXD	PSC3_0	X3-53
RS232_RxD_2	X3-75	UART3_RXD	PSC3_1	X3-51

Table 17: RS232 / UART Signals

Component	Manufacturer	Type	Temperature Range
SP3222EEA	Sipex	Dual RS232 transceiver	–40 °C to +85 °C

Table 18: RS232 Transceiver

4.1.14 Module Interface

All pins of the MPC5200, except SDRAM interface, the PLL supply and the XTAL pins are routed to the Board-to-Board connectors. In addition, a Master Reset Input, an SRAM Backup Power Input as well as the RxD and TxD signals of the RS-232 interfaces are available at the module plug connectors.

The signals are arranged at the module plug in such a way that all processor signals, non-CPU and PLD signals as well as spare pins fit on the two 120 pin connectors.

4.1.14.1 Board-to-Board Connectors

Board-to-Board connection via two 120 pin plug connectors with 0.8 mm pitch.
The 0.8 mm pitch plug connectors are available in different heights.
On the TQM5200S the 5 mm high module plug connectors are used.

Board-to-Board Distance	Module Connector				Target Hardware Connector		
	No. of Pins	**Qty**	**Supplier**	**Order No.**	**No. of Pins**	**Supplier**	**Order No.**
5 mm	120	2	tyco	177983-5	120	tyco	177984-5
6 mm					120	tyco	179029-5
7 mm					120	tyco	179030-5
8 mm					120	tyco	179031-5

Table 19: Board-to-Board Connectors

The following lists describe the functionality and signal characteristics of the module pins:

4.1.14.2 Plug Connector X1

Pin	Function	I/O Type[1]	Description[2]
1	3V3	PWR	Module supply 3.3 V ±5 %
2	GND	PWR	Module supply
3	ETH_17	I/O3V3, 4/4 mA	CD / CRS
4	ETH_16	I/O3V3, 4/4 mA	USB_OVRCNT / CTS / RX_ER
5	ETH_15	I/O3V3, 4/4 mA	USB_RXN / RX / RXD[3]
6	ETH_14	I/O3V3, 4/4 mA	USB_RXP / UART_RX / RXD[2]
7	ETH_13	I/O3V3, 4/4 mA	USB_RXD / CTS / RXD[1] / I/O
8	ETH_12	I/O3V3, 4/4 mA	RXD[0] / I/O
9	ETH_11	I/O3V3, 4/4 mA	TX_CLK / I/O, 3.3 V Schmitt Trigger
10	GND	PWR	Module supply
11	ETH_9	I/O3V3, 4/4 mA	CD / RX_CLK, 3.3 V Schmitt Trigger
12	ETH_10	I/O3V3, 4/4 mA	CTS / COL / I/O
13	3V3	PWR	Module supply 3.3 V ±5 %
14	ETH_8	I/O3V3, 4/4 mA	RX_DV
15	ETH_7	I/O3V3, 4/4 mA	TXN / MDIO
16	ETH_6	I/O3V3, 4/4 mA	USB_OE / RTS / MDC, Reset configuration bit
17	ETH_5	I/O3V3, 4/4 mA	USB_SUPEND / TX_ER, Reset configuration bit
18	GND	PWR	Module supply
19	ETH_3	I/O3V3, 4/4 mA	USB_PRTPWR / TXD[2], Reset configuration bit
20	ETH_4	I/O3V3, 4/4 mA	USB_SPEED / TXD[3], Reset configuration bit
21	ETH_1	I/O3V3, 4/4 mA	RTS / TXD[0], Reset configuration bit
22	ETH_2	I/O3V3, 4/4 mA	USB_TXP / TX / TXD[1], Reset configuration bit
23	IRQ3	I/O 3V3, 4/4 mA, 100k PD	
24	ETH_0	I/O 3V3, 4/4 mA, 100k PU	TX / TX_EN, Reset configuration bit
25	3V3	PWR	Module supply 3.3 V ±5 %
26	GND	PWR	Module supply
27	IRQ1	I/O 3V3, 4/4 mA, 100k PU	
28	IRQ2	I/O 3V3, 4/4 mA, 100k PD	
29	PCI_STOP#	I/O 3V3, 16/16 mA, 5k6 PU	
30	IRQ0	I/O 3V3, 4/4 mA, 100k PU	
31	PCI_RESET#	I/O 3V3, 16/16 mA, 5k6 PU	
32	PCI_TRDY#	I/O 3V3, 16/16 mA, 5k6 PU	
33	PCI_PERR#	I/O 3V3, 16/16 mA, 5k6 PU	
34	GND	PWR	Module supply
35	PCI_IRDY#	I/O 3V3, 16/16 mA, 5k6 PU	
36	PCI_SERR#	I/O 3V3, 16/16 mA, 5k6 PU	
37	3V3	PWR	Module supply 3.3 V ±5 %
38	PCI_REQ#	I/O 3V3, 8/8 mA, 5k6 PU	
39	PCI_GNT#	I/O 3V3, 8/8 mA	
40	PCI_PAR	I/O 3V3, 16/16 mA	
41	PCI_DEVSEL#	I/O 3V3, 16/16 mA, 5k6 PU	
42	GND	PWR	Module supply
43	PCI_CBE_3#	I/O 3V3, 16/16 mA	
44	PCI_ID_SEL	I/O 3V3, 8/8 mA	
45	PCI_CBE_2#	I/O 3V3, 16/16 mA	
46	PCI_FRAME#	I/O 3V3, 16/16 mA, 5k6 PU	
47	PCI_CBE_1#	I/O 3V3, 16/16 mA	
48	PCI_CLOCK	O 3V3, 12/12 mA	
49	3V3	PWR	Module supply 3.3 V ±5 %
50	GND	PWR	Module supply
51	PCI_CBE_0#	I/O 3V3, 16/16 mA	
52	EXT_AD_30	I/O 3V3, 10/10 mA	
53	EXT_AD_31	I/O 3V3, 10/10 mA	
54	EXT_AD_28	I/O 3V3, 10/10 mA	
55	EXT_AD_29	I/O 3V3, 10/10 mA	
56	EXT_AD_26	I/O 3V3, 10/10 mA	
57	EXT_AD_27	I/O 3V3, 10/10 mA	
58	GND	PWR	Module supply
59	EXT_AD_25	I/O 3V3, 10/10 mA	
60	EXT_AD_24	I/O 3V3, 10/10 mA	
61	3.3 V	PWR	Module supply 3.3 V ±5 %
62	EXT_AD_22	I/O 3V3, 10/10 mA	
63	EXT_AD_23	I/O 3V3, 10/10 mA	

Pin	Function	I/O Type[1]	Description[2]
64	EXT_AD_20	I/O 3V3, 10/10 mA	
65	EXT_AD_21	I/O 3V3, 10/10 mA	
66	GND	PWR	Module supply
67	EXT_AD_19	I/O 3V3, 10/10 mA	
68	EXT_AD_18	I/O 3V3, 10/10 mA	
69	EXT_AD_17	I/O 3V3, 10/10 mA	
70	EXT_AD_16	I/O 3V3, 10/10 mA	
71	EXT_AD_15	I/O 3V3, 10/10 mA	
72	EXT_AD_14	I/O 3V3, 10/10 mA	
73	3.3 V	PWR	Module supply 3.3 V ±5 %
74	GND	PWR	Module supply
75	EXT_AD_13	I/O 3V3, 10/10 mA	
76	EXT_AD_12	I/O 3V3, 10/10 mA	
77	EXT_AD_11	I/O 3V3, 10/10 mA	
78	EXT_AD_10	I/O 3V3, 10/10 mA	
79	EXT_AD_9	I/O 3V3, 10/10 mA	
80	EXT_AD_8	I/O 3V3, 10/10 mA	
81	EXT_AD_7	I/O 3V3, 10/10 mA	
82	GND	PWR	Module supply
83	EXT_AD_5	I/O 3V3, 10/10 mA	
84	EXT_AD_6	I/O 3V3, 10/10 mA	
85	3.3 V	PWR	Module supply 3.3 V ±5 %
86	EXT_AD_4	I/O 3V3, 10/10 mA	
87	EXT_AD_3	I/O 3V3, 10/10 mA	
88	EXT_AD_2	I/O 3V3, 10/10 mA	
89	EXT_AD_1	I/O 3V3, 10/10 mA	
90	GND	PWR	Module supply
91	LP_RW	0 3V3, 4/4 mA	Reset configuration bit
92	EXT_AD_0	I/O 3V3, 10/10 mA	
93	LP_ALE#	0 3V3, 6/6 mA	Reset configuration bit
94	LP_TS#	0 3V3, 8/8 mA	Reset configuration bit
95	LP_ACK#	I 3V3, 4k7 PU	
96	LP_OE#	0 3V3, 6/6 mA	
97	3.3 V	PWR	Module supply 3.3 V ±5 %
98	GND	PWR	Module supply
99	ATA_ISOLATION	I/O 3V3, 8/8 mA	
100	ATA_IOR#	I/O 3V3, 8/8 mA	Reset configuration bit
101	ATA_IOW#	I/O 3V3, 8/8 mA	Reset configuration bit
102	ATA_INTRQ	I/O 3V3, 8/8 mA, 10k PD	
103	ATA_IOCHRDY	I/O 3V3, 8/8 mA, 10k PU	
104	ATA_DACK#	I/O 3V3, 8/8 mA	Reset configuration bit
105	ATA_DRQ	I/O 3V3, 8/8 mA, 10k PD	
106	GND	PWR	Module supply
107	ATA_Reset#	I/O 3V3, 8/8 mA, 10k PU	Driven from PSC1_4 (Software reset)
108	LP_CS5#	O 3V3, 8/8 mA, 100k PU	
109	3.3 V	PWR	Module supply 3.3 V ±5 %
110	LP_CS4#	O 3V3, 8/8 mA, 100k PU	
111	LP_CS3#	O 3V3, 8/8 mA, 100k PU	
112	LP_CS2#	O 3V3, 4/4 mA, 100k PU	Chip select for SRAM
113	LP_CS1#	O 3V3, 8/8 mA, 100k PU	
114	GND	PWR	Module supply
115	Reserve 19	–	Reserve, not connected
116	LP_CS0#	O 3V3, 4/4 mA, 100k PU	Chip select for Flash
117	Start_L_H	I 3V3, 3K3 PD	Changeover of Boot address, 0 – Low boot, 1 – High boot
118	LM75_Alarm#	O, –/6 mA, 10K PU	Alarm output of Temperature sensor, Open drain output
119	3.3 V	PWR	Module supply 3.3 V ±5 %
120	GND	PWR	Module supply

1. This value refers to Data Sheet MPC5200BDS Rev. 01, state 01/2006.
   Under certain circumstances changes in the Data Sheet can lead to the fact that the data in this table is no longer correct.
2. Further descriptions about the pins can be gathered from the Data Sheet MPC5200BDS Rev. 01 state 01/2006.

Table 20: Plug Connector X1

4.1.14.3 Pin Configuration X1

Group	Function	MPC5200 Ball	Pin No. X1		MPC5200 Ball	Function	Group
Power	GND	–	2	1	–	3.3 V	Power
Ethernet	ETH_16	L02	4	3	J04	ETH_17	Ethernet
	ETH_14	N04	6	5	N03	ETH_15	
	ETH_12	M02	8	7	M01	ETH_13	
Power	GND	–	10	9	L04	ETH_11	
Ethernet	ETH_10	J03	12	11	L01	ETH_9	
	ETH_8	M03	14	13	–	3.3 V	Power
	ETH_6	N02	16	15	N01	ETH_7	Ethernet
Power	GND	–	18	17	L03	ETH_5	
Ethernet	ETH_4	J02	20	19	J01	ETH_3	
	ETH_2	K03	22	21	K02	ETH_1	
	ETH_0	K01	24	23	R01	IRQ3	Interrupt
Power	GND	–	26	25	–	3.3 V	Power
Interrupt	IRQ2	P02	28	27	P01	IRQ1	Interrupt
	IRQ0	P03	30	29	V06	PCI_STOP#	PCI Control
PCI Control	PCI_TRDY#	W05	32	31	R02	PCI_RESET#	
Power	GND	–	34	33	Y07	PCI_PERR#	
PCI Control	PCI_SERR#	W08	36	35	Y06	PCI_IRDY#	
	PCI_REQ#	U01	38	37	–	3.3 V	Power
	PCI_PAR	V07	40	39	R04	PCI_GNT#	PCI Control
Power	GND	–	42	41	W07	PCI_DEVSEL#	
PCI	PCI_ID_SEL	U02	44	43	Y02	PCI_CBE_3#	
	PCI_FRAME#	V05	46	45	W06	PCI_CBE_2#	
	PCI_CLOCK	T01	48	47	Y08	PCI_CBE_1#	
Power	GND	–	50	49	–	3.3 V	Power
PCI/ATA/LP/AD-Bus	EXT_AD_30	R03	52	51	W10	PCI_CBE_0#	PCI Control
	EXT_AD_28	T03	54	53	V01	EXT_AD_31	PCI/ATA/LP/AD-Bus
	EXT_AD_26	T02	56	55	W01	EXT_AD_29	
Power	GND	–	58	57	Y01	EXT_AD_27	
PCI/ATA/LP/AD-Bus	EXT_AD_24	U03	60	59	W02	EXT_AD_25	
	EXT_AD_22	V03	62	61	–	3.3 V	Power
	EXT_AD_20	V02	64	63	W03	EXT_AD_23	PCI/ATA/LP/AD-Bus
Power	GND	–	66	65	Y03	EXT_AD_21	
PCI/ATA/LP/AD-Bus	EXT_AD_18	V04	68	67	Y04	EXT_AD_19	
	EXT_AD_16	W04	70	69	Y05	EXT_AD_17	
	EXT_AD_14	W09	72	71	U08	EXT_AD_15	
Power	GND	–	74	73	–	3.3 V	Power
PCI/ATA/LP/AD-Bus	EXT_AD_12	Y09	76	75	V08	EXT_AD_13	PCI/ATA/LP/AD-Bus
	EXT_AD_10	Y10	78	77	V09	EXT_AD_11	
	EXT_AD_8	W11	80	79	V10	EXT_AD_9	
Power	GND	–	82	81	Y11	EXT_AD_7	
PCI/ATA/LP/AD-Bus	EXT_AD_6	U11	84	83	W12	EXT_AD_5	
	EXT_AD_4	V11	86	85	–	3.3 V	Power
	EXT_AD_2	V12	88	87	Y12	EXT_AD_3	PCI/ATA/LP/AD-Bus
Power	GND	–	90	89	W13	EXT_AD_1	
PCI/ATA/LP/AD-Bus	EXT_AD_0	V13	92	91	W16	LP_RW	LP Control
LP Control	LP_TS#	Y13	94	93	V14	LP_ALE#	
ATA Control	LP_OE#	D08	96	95	U14	LP_ACK#	
Power	GND	–	98	97	–	3.3 V	Power
ATA Control	ATA_IOR#	Y17	100	99	Y16	ATA_ISOLATION	ATA Control
	ATA_INTRQ	Y19	102	101	W17	ATA_IOW#	
	ATA_DACK#	Y18	104	103	W18	ATA_IOCHRDY	
Power	GND	–	106	105	V17	ATA_DRQ	
CS#	LP_CS5#	V16	108	107	Non CPU	ATA_SW_Reset# (via PSC1.4)	
	LP_CS4#	Y15	110	109	–	3.3 V	Power
	LP_CS2#	V15	112	111	W15	LP_CS3#	CS#
Power	GND	–	114	113	Y14	LP_CS1#	
CS#	LP_CS0#	W14	116	115	–	Reserve 19	Reserve
LM75	LM75_Alarm#	Non CPU	118	117	PLD	Start_L_H	PLD-Input
Power	GND	–	120	119	–	3.3 V	Power

Table 21: Pin configuration plug connector X1 (base module connector 1)

4.1.14.4 Plug Connector X3

Pin	Function	I/O Type[1]	Description[2]
1	3.3 V	PWR	Module supply 3.3 V ±5 %
2	GND	PWR	Module supply
3	HRESET#	I/O 3V3, –/6 mA, 10k PU	MPC5200 HW Reset, Open drain output, 3.3 V Schmitt Trigger
4	RESIN#	I 3V3, 5k6 PU	TQM5200S RESET-IN
5	PO_RESET#	O 3V3, 6/6 mA	TQM5200S RESET-OUT
6	SRESET#	I/O 3V3, –/6 mA, 10k PU	MPC5200 SW-Reset, open drain output, 3.3 V Schmitt Trigger
7	CPU_JTAG_TMS	I 3V3, 10k PU	Processor debug port
8	CPU_JTAG_TDO	O 3V3, 8/8 mA	Processor debug port
9	CPU_JTAG_TDI	I 3V3, 10k PU	Processor debug port
10	GND	PWR	Module supply
11	CPU_JTAG_TRST#	I 3V3	Processor debug port
12	TEST_SEL_1	I/O 3V3, 8/8 mA, 10k PD	ENID Input in Test Mode (for processor production test)
13	3.3 V	PWR	Module supply 3.3 V ±5 %
14	CPU_JTAG_TCK	I 3V3, 10k PU	Processor debug port, 3.3 V Schmitt Trigger
15	Test_Mode1	I 3V3, 10k PD	Test Mode Select 1 (for processor production test)
16	TEST_SEL_0	I/O 3V3, 4/4 mA	Scan Enable (for processor production test), PLL_BYPASS input, CK_STOP – output
17	Test_Mode0	I 3V3, 10k PD	Test Mode Select 0 (for processor production test)
18	GND	PWR	Module supply
19	USB1_1	I/O 3V3, 4/4 mA	USB_TXN, Reset configuration bit
20	USB1_0	I/O 3V3, 4/4 mA	USB_OE
21	USB1_3	I/O 3V3, 4/4 mA	USB_RXD
22	USB1_2	I/O 3V3, 4/4 mA	USB_TXP, Reset configuration bit
23	USB1_5	I/O 3V3, 4/4 mA	USB_RXN
24	USB1_4	I/O 3V3, 4/4 mA	USB_RXP
25	3.3 V	PWR	Module supply 3.3 V ±5 %
26	GND	PWR	Module supply
27	USB1_7	I/O 3V3, 4/4 mA	USB_SPEED
28	USB1_6	I/O 3V3, 4/4 mA	USB_PORTPWR
29	USB1_9	I/O 3V3, 4/4 mA	USB_OVERCNT
30	USB1_8	I/O 3V3, 4/4 mA	USB_SUSPEND
31	TIMER_1	I/O 3V3, 4/4 mA	
32	TIMER_0	I/O 3V3, 4/4 mA	
33	TIMER_3	I/O 3V3, 4/4 mA	MISO
34	GND	PWR	Module supply
35	TIMER_5	I/O 3V3, 4/4 mA	SCK
36	TIMER_2	I/O 3V3, 4/4 mA	MOSI
37	3.3 V	PWR	Module supply 3.3 V ±5 %
38	TIMER_4	I/O 3V3, 4/4 mA	SS
39	TIMER_7	I/O 3V3, 4/4 mA	
40	TIMER_6	I/O 3V3, 4/4 mA	
41	PSC3_9	I/O 3V3, 4/4 mA	USB_OVRCNT / SCK
42	GND	PWR	Module supply
43	PSC3_7	I/O 3V3, 4/4 mA	USB_SPEED / MISO
44	PSC3_8	I/O 3V3, 4/4 mA	USB_SUSPEND / SS
45	PSC3_5	I/O 3V3, 4/4 mA	USB_RXN
46	PSC3_6	I/O 3V3, 4/4 mA	USB_PRTPWR / MCLK / MOSI
47	PSC3_3	I/O 3V3, 4/4 mA	USB_RXD / Frame / CTS
48	PSC3_4	I/O 3V3, 4/4 mA	USB_RXP / CD
49	3.3 V	PWR	Module supply 3.3 V ±5 %
50	GND	PWR	Module supply
51	PSC3_1	I/O 3V3, 3/3 mA	USB_TXN / RxD / RX, RS232 Driver2
52	PSC3_2	I/O 3V3, 4/4 mA	USB_TXP / RTS, 3.3 V Schmitt Trigger
53	PSC3_0	I/O 3V3, 3/3 mA	USB_OE / TxD / TX, RS232 Driver2
54	PSC2_4	I/O 3V3, 4/4 mA	Frame / SS / CD
55	PSC2_3	I/O 3V3, 4/4 mA	BitClk / CTS, 3.3 V Schmitt Trigger
56	PSC2_2	I/O 3V3, 4/4 mA	Mclk / Sync / RTS
57	PSC2_1	I/O 3V3, 4/4 mA	RxD / Sdata_in / RX
58	GND	PWR	Module supply
59	PSC1_3	I/O 3V3, 4/4 mA	BitClk / CTS, 3.3 V Schmitt Trigger
60	PSC2_0	I/O 3V3, 4/4 mA	TxD / Sdata_out / TX
61	3.3 V	PWR	Module supply 3.3 V ±5 %
62	PSC1_4	I/O 3V3, 4/4 mA	Frame / SS / CD, ATA Reset
63	PSC1_1	I/O 3V3, 3/3 mA	RxD / Sdata_in / RX, RS232 Driver1

Pin	Function	I/O Type[1]	Description[2]
64	PSC1_2	I/O 3V3, 4/4 mA	Mclk / Sync / RTS
65	PSC1_0	I/O 3V3, 3/3 mA	TxD / Sdata_out / TX, RS232 Driver1
66	GND	PWR	Module supply
67	PSC6_3	I/O 3V3, 4/4 mA	IR_USB_CLK / BitClk / RTS, 3.3 V Schmitt Trigger
68	PSC6_2	I/O 3V3, 4/4 mA	IrDA_TX / TxD
69	PSC6_1	I/O 3V3, 4/4 mA	CTS / FRAME
70	PSC6_0	I/O 3V3, 4/4 mA	IrDA_RX / RxD
71	RS232 RxD_1	I 15V	RS232 Port 1 Input, PSC1 RxD
72	RS232 TxD_1	O 15V (5V4), 35/35 mA	RS232 Port 1 Output, PSC1 TxD
73	3.3 V	PWR	Module supply 3.3 V ±5 %
74	GND	PWR	Module supply
75	RS232 RxD_2	I 15V	RS232 Port 2 Input, PSC3 RxD
76	RS232 TxD_2	O 15V (5V4), 35/35 mA	RS232 Port 2 Output, PSC3 TxD
77	SDA_2	I/O 3V3, 2/2 mA, 10k PU	I2C_3, 3.3 V Schmitt Trigger, EEPROM and temperature sensor (HW address 000)
78	SCL_2	I/O 3V3, 2/2 mA, 10k PU	I2C_2, 3.3 V Schmitt Trigger, EEPROM and temperature sensor (HW address 000)
79	SDA_1	I/O 3V3, 4/4 mA, PU, NA	I2C_1, CAN1_RX, 3.3 V Schmitt Trigger
80	SCL_1	I/O 3V3, 4/4 mA, PU, NA	I2C_0, CAN1_TX, 3.3 V Schmitt Trigger
81	WP# / ACC	I 3V3, 5k6 PU	Input accelerates Flash programming time (when high voltage is applied) for higher throughput during system production. Protects first or last sector regardless of sector protection settings
82	GND	PWR	Module supply
83	HRESETF#	I 3V3	External Flash reset (over 10k coupled with HRESET#)
84	GPIO_WKUP_7	I/O 3V3, 8/8 mA	
85	3.3 V	PWR	Module supply 3.3 V ±5 %
86	Vbatt 3V3		Battery supply for SRAM
87	SEL_B1#	I/O 3V3, 4/4 mA	Byte select (Byte 0) for 32 bit access
88	SEL_B0#	I/O 3V3, 4/4 mA	Byte select (Byte 1) for 32 bit access
89	SEL_B2#	I/O 3V3, 4/4 mA	Byte select (Byte 2) for 32 bit access
90	GND	PWR	Module supply
91	Reserve 1	–	Reserve, Not connected
92	SEL_B3#	I/O 3V3, 4/4 mA	Byte select (Byte 3) for 32 bit access
93	Reserve 3	–	Reserve, Not connected
94	Reserve 2	–	Reserve, Not connected
95	Reserve 5	–	Reserve, Not connected
96	Reserve 4	–	Reserve, Not connected
97	3.3 V	PWR	Module supply 3.3 V ±5 %
98	GND	PWR	Module supply
99	Reserve 7	–	Reserve, Not connected
100	Reserve 6	–	Reserve, Not connected
101	Reserve 9	–	Reserve, Not connected
102	Reserve 8	–	Reserve, Not connected
103	Reserve 11	–	Reserve, Not connected
104	Reserve 10	–	Reserve, Not connected
105	Reserve 12	–	Reserve, Not connected
106	GND	PWR	Module supply
107	Reserve 13	–	Reserve, Not connected
108	Reserve 14	–	Reserve, Not connected
109	3.3 V	PWR	Module supply 3.3 V ±5 %
110	Reserve 16	–	Reserve, Not connected
111	Reserve 15	–	Reserve, Not connected
112	Reserve 18	–	Reserve, Not connected
113	Reserve 17	–	Reserve, Not connected
114	GND	PWR	Module supply
115	JTAG_TDI	I 3V3, 10k PU	PLD-JTAG
116	JTAG_TDO	O 3V3, 8/8 mA	PLD-JTAG
117	JTAG_TMS	I 3V3, 10k PU	PLD-JTAG
118	JTAG_TCK	I 3V3, 10k PU	PLD-JTAG
119	3.3 V	PWR	Module supply 3.3 V ±5 %
120	GND	PWR	Module supply

1. This value refers to Data Sheet MPC5200BDS Rev. 01, state 01/2006.
Under certain circumstances changes in the Data Sheet can lead to the fact that the data in this table is no longer correct.
2. Further descriptions about the pins can be gathered from the Data Sheet MPC5200BDS Rev. 01 state 01/2006.

Table 22: Plug Connector X3

4.1.14.5 Pin Configuration X3

Group	Function	MPC5200 Ball	Pin No. X3		MPC5200 Ball	Function	Group
Power	GND	–	2	1	–	3.3 V	Power
Reset	RESIN#	Non CPU	4	3	B13	HRESET#	Reset
	SRESET#	A14	6	5	A13	PO_RESET#	
CPU JTAG	CPU_JTAG_TDO	A02	8	7	A04	CPU_JTAG_TMS	CPU JTAG
Power	GND	–	10	9	A03	CPU_JTAG_TDI	
CPU JTAG	TEST_SEL_1	C03	12	11	B03	CPU_JTAG_TRST#	
	CPU_JTAG_TCK	B04	14	13	–	3.3 V	Power
	TEST_SEL_0	B01	16	15	A01	Test_Mode1	CPU JTAG
Power	GND	–	18	17	B02	Test_Mode0	
USB1	USB1_0	H01	20	19	H02	USB1_1	USB1
	USB1_2	H03	22	21	G01	USB1_3	
	USB1_4	G02	24	23	G03	USB1_5	
Power	GND	–	26	25	–	3.3 V	Power
USB1	USB1_6	G04	28	27	F01	USB1_7	USB1
	USB1_8	F02	30	29	F03	USB1_9	
Timer	TIMER_0	Y20	32	31	V18	TIMER_1	Timer
Power	GND	–	34	33	D02	TIMER_3	
Timer	TIMER_2	D03	36	35	E03	TIMER_5	
	TIMER_4	D01	38	37	–	3.3 V	Power
	TIMER_6	E02	40	39	E01	TIMER_7	Timer
Power	GND	–	42	41	C04	PSC3_9	PSC 3
PSC 3	PSC3_8	A05	44	43	B05	PSC3_7	
	PSC3_6	C05	46	45	A06	PSC3_5	
	PSC3_4	B06	48	47	C06	PSC3_3	
Power	GND	–	50	49	–	3.3 V	Power
PSC 3	PSC3_2	A07	52	51	B07	PSC3_1	PSC 3
PSC 2	PSC2_4	A08	54	53	C07	PSC3_0	
	PSC2_2	A09	56	55	B08	PSC2_3	PSC 2
Power	GND	–	58	57	B09	PSC2_1	
PSC 2	PSC2_0	C09	60	59	B10	PSC1_3	PSC1
PSC 1	PSC1_4 / ATA-SW-Reset	A10	62	61	–	3.3 V	Power
	PSC1_2	C10	64	63	A11	PSC1_1	PSC1
Power	GND	–	66	65	B11	PSC1_0	
PSC 6	PSC6_2	A12	68	67	C13	PSC6_3	PSC 6
	PSC6_0	B12	70	69	C11	PSC6_1	
RS232	RS232 TxD_1	Non CPU	72	71	Non CPU	RS232 RxD_1	RS232
Power	GND	–	74	73	–	3.3 V	Power
RS232	RS232 TxD_2	Non CPU	76	75	Non CPU	RS232 RxD_2	RS232
I²C	SCL_2	V20	78	77	W20	SDA_2	I²C
	SCL_1	V19	80	79	W19	SDA_1	
Power	GND	–	82	81	Non CPU	WP#/ACC	Flash Reset
GPIO	GPIO_WKUP_7	C12	84	83	Non CPU	HRESETF#	
Battery	Vbatt 3V3	Non CPU	86	85	–	3.3 V	Power
LP_ByteSelect	SEL_B0#	Non CPU	88	87	Non CPU	SEL_B1	LP_ByteSelect
Power	GND	–	90	89	Non CPU	SEL_B2	
LP_ByteSelect	SEL_B3#	Non CPU	92	91	–	Reserve 1	Reserve
Reserve	*Reserve 2*	–	94	93	–	Reserve 3	
	Reserve 4	–	96	95	–	Reserve 5	
Power	GND	–	98	97	–	3.3 V	Power
Reserve	*Reserve 6*	–	100	99	–	Reserve 7	Reserve
	Reserve 8	–	102	101	–	Reserve 9	
	Reserve 10	–	104	103	–	Reserve 11	
Power	GND	–	106	105	–	Reserve 12	
Reserve	*Reserve 14*	–	108	107	–	Reserve 13	
	Reserve 16	–	110	109	–	3.3 V	Power
	Reserve 18	–	112	111	–	Reserve 15	Reserve
Power	GND	–	114	113	–	Reserve 17	
PLD-JTAG	JTAG_TDO	Non CPU	116	115	Non CPU	JTAG_TDI	PLD-JTAG
	JTAG_TCK	Non CPU	118	117	Non CPU	JTAG_TMS	
Power	GND	–	120	119	–	3.3 V	Power

Table 23: Pin configuration plug connector X3 (base module connector 2)

4.1.14.6 Electrical Characteristics of the Module Interfaces

In the following table the signal characteristics of the module pins are described.

Name	Alias	Type	Power Supply	Output Driver		Input Type	PU / PD
				IOH[mA]	IOL[mA]		
PCI / ATA / LP / AD-Bus							
EXT_AD[31:0]		I/O	VDD_IO (3.3 V)	12	12	PCI / LVTTL	–
PCI							
PCI_CBE_0		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_CBE_1		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_CBE_2		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_CBE_3		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_CLOCK		I/O	VDD_IO (3.3 V)	12	12	PCI	–
PCI_DEVSEL		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_FRAME		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_GNT		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
PCI_IDSEL		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
PCI_IRDY		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_PAR		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_PERR		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_REQ		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
PCI_RESET		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_SERR		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_STOP		I/O	VDD_IO (3.3 V)	16	16	PCI	–
PCI_TRDY		I/O	VDD_IO (3.3 V)	16	16	PCI	–
Local-Plus							
LP_ACK		I/O	VDD_IO (3.3 V)	6	6	LVTTL	Pullup
LP_ALE		I/O	VDD_IO (3.3 V)	7	7	LVTTL	–
LP_OE		I/O	VDD_IO (3.3 V)	6	6	LVTTL	–
LP_RW		I/O	VDD_IO (3.3 V)	6	6	LVTTL	–
LP_TS		I/O	VDD_IO (3.3 V)	6	6	LVTTL	–
LP_CS0		I/O	VDD_IO (3.3 V)	6	6	LVTTL	–
LP_CS1		I/O	VDD_IO (3.3 V)	6	6	LVTTL	–
LP_CS2		I/O	VDD_IO (3.3 V)	6	6	LVTTL	–
LP_CS3		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
LP_CS4		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
LP_CS5		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
ATA							
ATA_DACK		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
ATA_DRQ		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
ATA_INTRQ		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
ATA_IOCHRDY		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
ATA_IOR		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
ATA_IOW		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
ATA_ISOLATION		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–

Name	Alias	Type	Power Supply	Output Driver		Input Type	PU / PD
				IOH[mA]	IOL[mA]		
Ethernet							
ETH_0	TX / TX_EN	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_1	RTS / TXD[0]	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_2	USB_TXP / TX / TXD[1]	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_3	USB_PRTPWR / TXD[2]	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_4	USB_SPEED / TXD[3]	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_5	USB_SUPEND / TX_ER	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_6	USB_OE / RTS / MDC	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_7	TXN / MDIO	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_8	RX_DV	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_9	CD / RX_CLK	I/O	VDD_IO (3.3 V)	4	4	3.3 V Schmitt-Trigger	–
ETH_10	CTS / COL / I/O	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_11	TX_CLK / I/O	I/O	VDD_IO (3.3 V)	4	4	3.3 V Schmitt-Trigger	–
ETH_12	RXD[0] / I/O	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_13	USB_RXD / CTS / RXD[1] / I/O	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_14	USB_RXP / UART_RX / RXD[2]	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_15	USB_RXN / RX / RXD[3],	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_16	USB_OVRCNT / CTS / RX_ER	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
ETH_17	CD / CRS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
IrDA							
PSC6_0	IRDA_RX / TxD	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC6_1	RxD	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC6_2	Frame / CTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC6_3	IR_USB_CLK / BitClk / RTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB							
USB_0	USB_OE	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_1	USB_TXN	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_2	USB_TXP	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_3	USB_RXD	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_4	USB_RXP	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_5	USB_RXN	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_6	USB_PRTPWR	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_7	USB_SPEED	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_8	USB_SUPEND	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
USB_9	USB_OVRCNT	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
I²C							
I2C_0	SCL	I/O	VDD_IO (3.3 V)	4	4	3.3 V Schmitt-Trigger	–
I2C_1	SDA	I/O	VDD_IO (3.3 V)	4	4	3.3 V Schmitt-Trigger	–
I2C_2	SCL	I/O	VDD_IO (3.3 V)	3	3	3.3 V Schmitt-Trigger	–
I2C_3	SDA	I/O	VDD_IO (3.3 V)	3	3	3.3 V Schmitt-Trigger	–

Name	Alias	Type	Power Supply	Output Driver		Input Type	PU / PD
				IOH[mA]	IOL[mA]		
PSC							
PSC1_0	TxD / Sdata_out / MOSI / TX	I/O	VDD_IO (3.3 V)	3	3	LVTTL	–
PSC1_1	RxD / Sdata_in / MISO / TX	I/O	VDD_IO (3.3 V)	3	3	LVTTL	–
PSC1_2	Mclk / Sync / RTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC1_3	BitClk / SCK / CTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC1_4	Frame / SS / CD	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC2_0	TxD / Sdata_out / MOSI / TX	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC2_1	RxD / Sdata_in / MISO / TX	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC2_2	Mclk / Sync / RTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC2_3	BitClk / SCK / CTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC2_4	Frame / SS / CD	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_0	USB_OE / TxD / TX	I/O	VDD_IO (3.3 V)	3	3	LVTTL	–
PSC3_1	USB_TXN / RxD / RX	I/O	VDD_IO (3.3 V)	3	3	LVTTL	–
PSC3_2	USB_TXP / BitClk / RTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_3	USB_RXD / Frame / SS / CTS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_4	USB_RXP / CD	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_5	USB_RXN	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_6	USB_PRTPWR / Mclk / MOSI	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_7	USB_SPEED / MISO	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_8	USB_SUPEND / SS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
PSC3_9	USB_OVRCNT / SCK	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
GPIO/TIMER							
GPIO_WKUP_7		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
TIMER_0		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TIMER_1		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TIMER_2	MOSI	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TIMER_3	MISO	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TIMER_4	SS	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TIMER_5	SCK	I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TIMER_6		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TIMER_7		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
Misc							
PORRESET		Input	VDD_IO (3.3 V)	–	–	3.3 V Schmitt-Trigger	–
HRESET		I/O	VDD_IO (3.3 V)	–	8	3.3 V Schmitt-Trigger	–
SRESET		I/O	VDD_IO (3.3 V)	–	8	3.3 V Schmitt-Trigger	–
IRQ0		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
IRQ1		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
IRQ2		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
IRQ3		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–

Name	Alias	Type	Power Supply	Output Driver		Input Type	PU / PD
				IOH[mA]	IOL[mA]		
Test/Configuration							
SYS_PLL_TPA		I/O	VDD_IO (3.3 V)	4	4	LVTTL	–
TEST_MODE_0		Input	VDD_IO (3.3 V)	4	4	LVTTL	–
TEST_MODE_1		Input	VDD_IO (3.3 V)	4	4	LVTTL	–
TEST_SEL_0		I/O	VDD_IO (3.3 V)	4	4	LVTTL	Pullup
TEST_SEL_1		I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
JTAG_TCK	TCK	Input	VDD_IO (3.3 V)	–	–	LVTTL	Pullup
JTAG_TDI	TDI	Input	VDD_IO (3.3 V)	–	–	LVTTL	Pullup
JTAG_TDO	TDO	I/O	VDD_IO (3.3 V)	8	8	LVTTL	–
JTAG_TMS	TMS	Input	VDD_IO (3.3 V)	–	–	LVTTL	Pullup
JTAG_TRST	TRST	Input	VDD_IO (3.3 V)	–	–	LVTTL	Pullup
Serial Interfaces							
RS232 TxD_1		Output	VDD_IO (3.3 V)	60	60	LVTTL	–
RS232 RxD_1		Input	VDD_IO (3.3 V)	–	–	LVTTL	–
RS232 TxD_2		Output	VDD_IO (3.3 V)	60	60	LVTTL	–
RS232 RxD_2		Input	VDD_IO (3.3 V)	–	–	LVTTL	–

Table 24: Signal Characteristics

4.1.15 Chip-Selects und Interrupts

This table shows the chip selects and interrupts, which are available at the plug connectors.

Pin	Signal Name	Description	Status
X1-116	LP_CS0#	Chip Select 0	Used
X1-113	LP_CS1#	Chip Select 1	Used
X1-112	LP_CS2#	Chip Select 2	Used
X1-111	LP_CS3#	Chip Select 3	**Available**
X1-110	LP_CS4#	Chip Select 4	**Available**
X1-108	LP_CS5#	Chip Select 5	**Available**
X1-30	IRQ0	Interrupt 0	**Available**
X1-27	IRQ1	Interrupt 1	**Available**
X1-28	IRQ2	Interrupt 2	**Available**
X1-23	IRQ3	Interrupt 3	**Available**

Table 25: Available Chip Selects and Interrupts

4.1.16 Service-Interfaces

4.1.16.1 Download Interface

The serial interface at PSC1 is the default download-interface (only RxD and TxD).
For this purpose the serial interface at PSC1 is defined in the software (Universal-Boot) as the default download-interface.

As an alternative to PSC1-UART, the PSC6-UART by can be configured as the default interface by setting 0 Ω resistors. For this a modified Universal-Boot is required, which supports this interface as by default.

4.1.16.2 COP/JTAG Interface

All lines of the Freescale COP/JTAG interfaces (Debugging interface) are available.
The COP/JTAG interface is routed exclusively to the connectors.
It consists of the following signals:

Pin[2]	Signal name	Type	Function
1	TDO	O	Test Data Output
3	TDI	I/O	Test Data Input
12, 16	GND	–	Ground
5	NC	–	NC
7	TCK	O	Test Clock
9	TMS	I/O	Test Mode Select
11	SRESET#	I	Soft Reset
13	HRESET#		Hard Reset
15	CKSTP_OUT#		Check Stop Out *(Protective circuit on the target hardware)*
4	TRST#		Test Reset
6	3.3 V	O	Power

Table 26: COP/JTAG Interface

[2] Pin configuration on the Starterkit (STK52xx) / the module pins are listed in Table 20, connector assembly X3

4.1.17 Supply

The supply voltage of the module is specified as follows:

- **Module supply: 3.3 V ±5 %**
- Battery voltage: 3.0 V to 2.7 V; for example Lithium cell CR2032

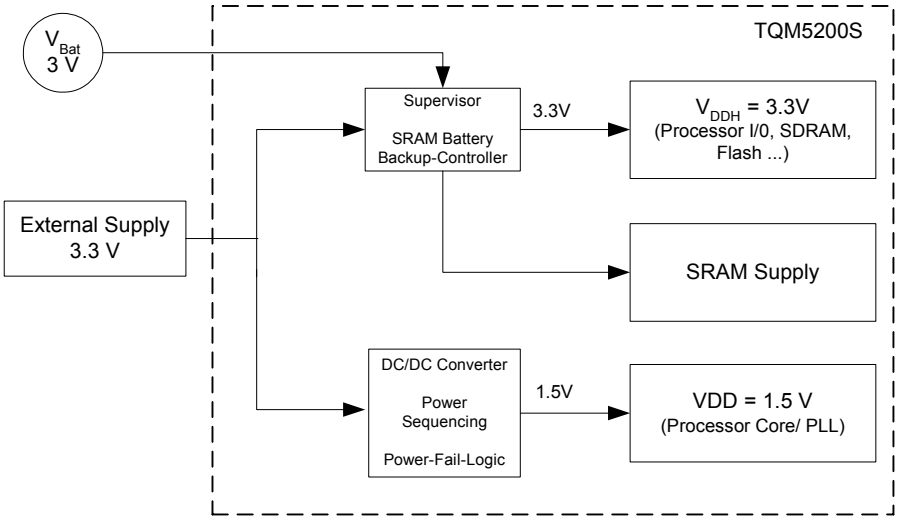

Illustration 6: Voltage Supply

4.1.17.1 Power Supply Tolerances

Tolerance of 3.3 V supply: VCC3V3 = 3.3 V ±5 % = 3.135 to 3.465 V

Reset is triggered when voltage drops below 3.06 V.

4.1.17.2 Internal Voltages

MPC5200 core voltage: 1.5 V ±5 %

4.1.17.3 Current Consumption, Maximum Values

Device	3.3 V	1.5 V
Processor Core	–	800 mA
Processor I/O	10 mA[3]	–
Processor PLL	–	1.5 mA
SDRAM	660 mA	–
SRAM	40 mA	–
Serial EEPROM	1 mA	–
Flash	120 mA	–
Supervisor 3.3 V	40 µA	–
Power Fail Logic 1.5 V	10 µA	–
RS232 Transceiver	1 mA	–
Bus driver	20 mA	–
Address register	20 mA	–
PLD	12 mA	–
Total	approx. 900 mA	approx. 800 mA
Total to be supplied	**Max. 1300 mA @ 3.3 V**	

Table 27: Maximum current consumption

4.1.17.4 Power Consumption, Typical Values

The typical current consumption of the TQM5200S-BD is approximately 600 mA @ 3.3V.

The TQM5200S-BD offers the following features:

- 32 Mbyte Flash
- 64 Mbyte SDRAM
- 0.5 Mbyte SRAM
- 4 Kbyte EEPROM
- Temperature Sensor
- 400 MHz Processor Clock

4.1.17.5 Reset Logic / Supervisor

The Reset Logic comprises of the following functions:

- Monitoring of all supply voltages used on the module (1.5 V, 3.3 V)
- External reset input
- Battery back-up function for SRAM (battery not on the module)
- Chip-Select gating for SRAM
- Reset-Status displayed by a red LED

[3] Without external protective circuit

5. Mechanics

5.1 General Information

- High pin count SMD plug connectors with 0.8 mm pitch
- The combination with different counterparts allows customisation of the stack height to the height of the parts mounted on the target hardware
- Double-sided SMD assembly

5.2 Dimensions

- Dimensions of the PCB: 56 mm × 60 mm
- Overall height: approx. 10 mm
- Free overall height under the module: approx. 2.9 mm

5.3 Mounting

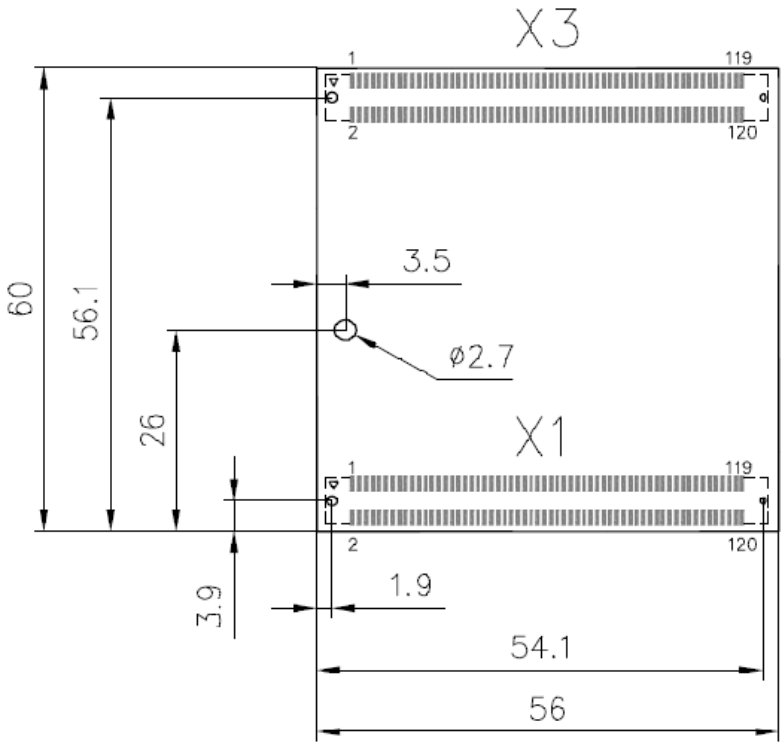

Illustration 7: Top view through the printed circuit board

5.4 Top View TQM5200S

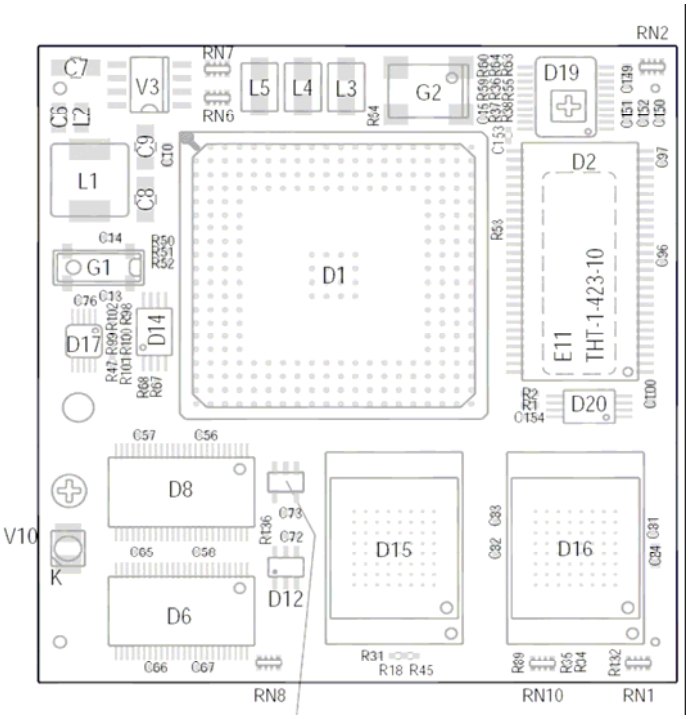

Illustration 8: Top View

5.5 Bottom View TQM5200S

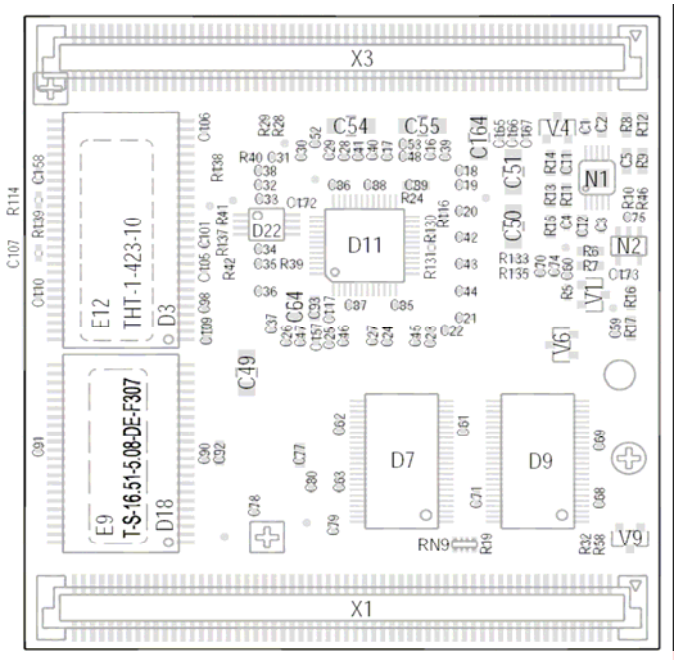

Illustration 9: Bottom View

5.6 Side View TQM5200S

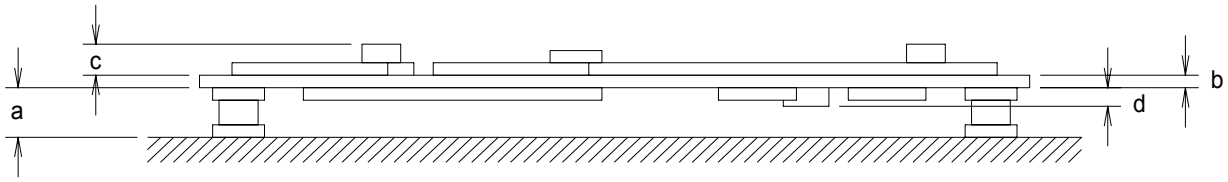

Illustration 10: Stack heights (not to scale)

Dim	Value [mm]	Remarks
a	5.0 ±0.2	Combination of module connector and standard mating connector. 6, 7 or 8 mm are possible with different connectors on the target hardware.
b	1.8 ±0.16	Printed circuit board
c	3.0 max.	Coils (maximum height on top)
d	1.6 max.	Ceramic capacitor

Table 28: Stack Heights

	To avoid damages caused by mechanical stress, it is recommended to extract the TQM5200S from the target hardware only by using the special extraction tool MOZI52xxS.
	2.5 mm should be kept free on the target hardware along the longitudinal edges on both sides of the module for the extraction tool MOZI52xxS.

One hole is provided for mounting the module on the target hardware and / or for mounting a CPU heat sink.

6. Software

On the module an adapted version of “U-Boot” is preinstalled as boot loader.
It is the basic software delivered with the TQM5200S.
For more information see separate specification.

7. Safety Requirements and Protective Regulations

7.1 EMC Requirements

The module was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the target hardware
- With metal casings, a good (at least according to RF) connection to the target hardware or to the potential of the housing
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanent clocked lines (e.g., clock) should be kept short; avoid interference of other signals by distance and/or shielding
- Filtering of all signals which can be connected externally (also "slow" signals and DC can radiate RF indirectly)

7.2 ESD Requirements

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the target hardware, no special preventive measures were planned on the module. According to the data sheets, the used devices already have some protection; however, this is generally not sufficient to fulfil the legal requirements without any further measures.

Following measures are recommended:

- Generally applicable: Shielding of the inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Protection by suppressor diode(s)
- Slow signal lines: RC filtering, perhaps Zener diode
- Fast signal lines: Integrated protective devices (suppressor diode arrays)

7.3 Reliability and Service Life

The module is designed for a service life of 10 years. It was also designed to be insensitive to vibration and impact.

7.4 Climate Conditions and Operational Conditions

- Protection class IP00
- Relative air humidity (operation / storing): 10 … 90 % (not condensing)

The possible temperature range strongly depends on the installation situation, (heat dissipation by conduction and convection). Hence, no fixed value can be given for the whole assembly. Reliable operation is generally achieved when the following conditions are met:

- Standard temperature range:
  - Chip temperature of the CPU: 0 °C to +70 °C
  - Package temperature of the remaining ICs: 0 °C to +70 °C
  - Storage temperature: –5 °C to +85 °C
- Extended temperature range:
  - Chip temperature of the CPU: –40 °C to +85 °C
  - Package temperature of the remaining ICs: –40 °C to +85 °C
  - Storage temperature: –55 °C to +100 °C

7.5 Environmental Protection

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.

To be able to reuse the product, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled.

The energy consumption of this subassembly is minimised by suitable measures.

Printed pc-boards are delivered in reusable packaging. Modules and devices are delivered in an outer packaging of paper, cardboard or other recyclable material.

Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (source of information: BGBl I 1996, 1382, (1997, 2860)
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (source of information: BGBl I 2001, 3379)

8. Appendix

8.1 Acronyms and Definitions

The following terminology and abbreviations are used:

Acronym	Meaning
AD	Address/Data
ATA	Advanced Technology Attachment
BDLC	Byte Data Link Controller
BGA	Ball Grid Array
CAN	Controller Area Network
CODEC	Code/Decode
COP	Common On-chip Processor
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CS	Chip Select
DC	Direct Current
DMA	Direct Memory Access
DS	Data Size
EEPROM	Electrically Erasable Programmable Read-Only Memory (Byte-wise re-writable)
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETH	Ethernet
FEC	Fast Ethernet Controller
Flash	Electrically Erasable Programmable Read-Only Memory (Block Erase)
FPU	Floating-Point Unit
FR-4	Flame Retardant-4
GND	Ground
GPIO	General Purpose Input/Output
HSYNC	Horizontal Synchronisation
HW	Hardware
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
IFR	In-Frame Response
IP	Internet Protocol
IrDA	Infrared Data Association
IRQ	Interrupt Request
ISO	International Organization for Standardization
I²C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
kbps	Kilobit Per Second
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LP	Local Plus (Bus)
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor

Acronym	Meaning
LVTTL	Low Voltage Transistor-Transistor Logic
Mbps	Megabit Per Second
MII	Media-Independent Interface
MIPS	Million Instructions Per Second
MMU	Memory Management Unit
MOZI	Module Extractor (Modulzieher)
msb	Most Significant Bit
MSCAN	Motorola Scalable Controller Area Network
MSOP	Micro Small Outline Package
NA	Not Assembled
NC	Not Connected
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PD	Pull-Down (Resistor)
PLD	Programmable Logic Device
PLL	Phase Locked Loop
PPC	PowerPC
PSC	Programmable Serial Controller
PU	Pull-Up (Resistor)
PWR	Power
RAM	Random Access Memory
RF	Radio Frequency
RO	Read-Only
ROM	Read-Only Memory
RTC	Real-Time Clock
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SMD	Surface Mounted Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SXGA	Super eXtended Graphics Array (1280x1024)
TQFP	Thin Quad Flat Package
TSSOP	Thin Shrink Small Outline Package
TTL	Transistor-Transistor Logic
U-Boot	Universal Bootloader
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VGA	Video Graphics Array
VSYNC	Vertical Synchronisation
WO	Write-Only
WP	Write-Protection

Table 29: Acronyms

8.2 References

	Document	Revision	Date	Supplied by
A	MPC5200BDS Data Sheet: Technical Data	Rev: 1	01/2006	Freescale Semiconductor
B	MPC5200BUG User Guide	Rev: 1.3	07/2006	Freescale Semiconductor
C	MPC5200BE Errata	Rev: 0	09 /2005	Freescale Semiconductor
	MPC5200B Spec Change Letter TCSA TCSN 26Jun2006.pdf	–	06/2006	Freescale Semiconductor
D	Application Note AN2458/D MPC5200 Local-Plus-Bus Interface	Rev. 2	08/2004	Freescale Semiconductor

Table 30: References