STKT104X
User's Manual

STKT104X UM 0106
03.11.2021

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FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	11.04.2017	Petz		Initial release
0101	29.08.2017	Petz	3.2.1 3.4.12 Table 22 3.6.2, 3.6.3, 3.6.5 8.2	Footnote (1) added Information added Values corrected Information added Updated
0102	25.04.2018	Petz	Table 3 3.6.1 Table 35	Table contents clarified removed X1-30: “VCC3V3” replaced with “VCC3V3F”, CPU ball assignment corrected
0103	26.10.2018	Petz	All	Links updated, formatting
0104	25.11.2020	Petz	Table 20 Table 23 3.5.2 Table 27 Table 35	Footnote 3 added Footnote 4 added Information updated and clarified, Note added Footnote 5 added Footnote 7 added
0105	11.10.2021	Kreuzer	Table 16 Figure 9	Table corrected and extended Figure corrected
0106	3.11.2021	Kreuzer	3.3.3	HRESET# corrected to RESET_OUT#

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the STKT104X and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- STKT104X circuit diagram
- TQMT104x User's Manual
- QorIQ T1040 Reference Manual (also supports T1040, T1042, T1020, T1022)
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- ELDK documentation: www.denx.de/wiki/DULG/ELDK
- TQ-Support Wiki: Support-Wiki TQMT104x

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the STKT104X **Rev. ≥02xx**, and refers to some software settings.
The STKT104X serves primarily as a baseboard for the Minimodule TQMT1042.
It can also be used as a development platform for low-level software development (BSP).
It also serves a reference platform to evaluate and test the functions of the TQMT1042.
The Minimodule TQMT1042 is based on the NXP QorIQ CPU T1042.
Modules with pin compatible CPUs (T1020, T1022, T1014, T1024, T1040 and T2081) are available on request.
The name TQMT104x in this User's Manual serves as a placeholder for all other supported CPUs mentioned above.
In case a certain CPU derivative provides different features it is especially mentioned.

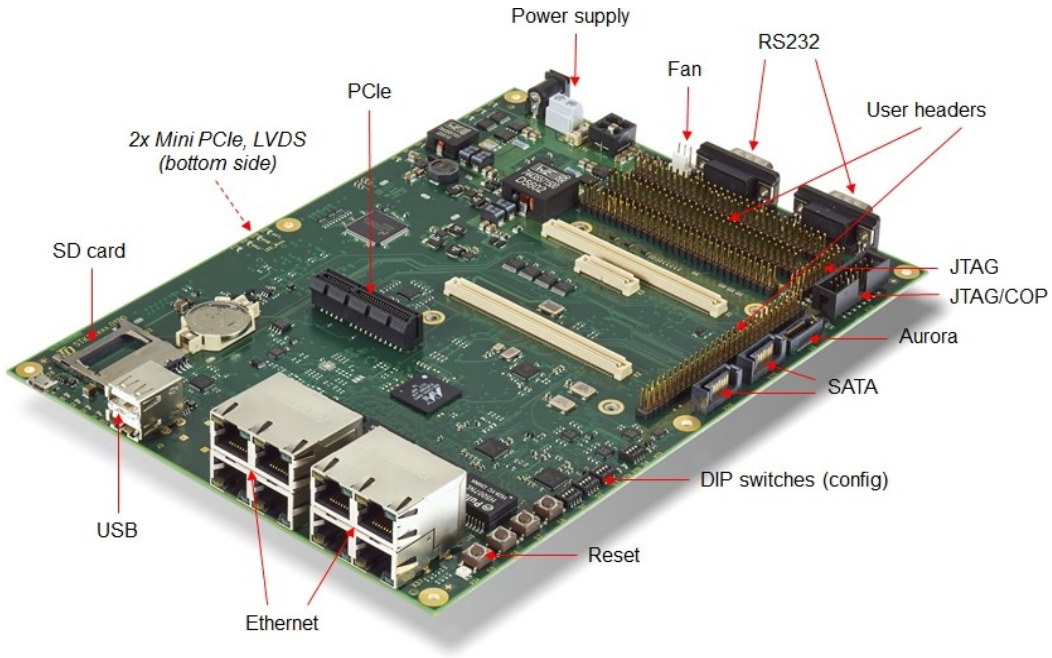

Figure 1: STKT104X interfaces

The following features mark the advantages of the Starterkit:

- Saving in time by early adaptation of software components on the target system.
- Users who design their own mainboard receive the Starterkit schematics from TQ-Systems GmbH.
  The user saves time, because frequently required parts of the circuitry can be copied from the schematics.
- Risk minimization by being able to evaluate single system requirements before completion of the whole system, e.g., test of response times, transfer speeds, CPU performance, thermal behaviour etc.
- Minimization of risk and time saving by being able to test customized functions, e.g., for PCI or PCIe or similar extension interfaces and to customize the software if necessary.
- Saving in time during start-up of the customized mainboard by reference measurements on the Starterkit.
- Time saving with troubleshooting on the customer's system by referencing to an examined, certified Starterkit platform.
- Comfortable start-up, because all necessary components like power supply, cable, module extractor, documentation, heat sink and software are already included in the delivery.

3. TECHNICAL DATA

3.1 Functionality and system architecture overview

The following block diagram shows the interfaces and STKT104X system components:
The interfaces marked green are supported with every CPU of the family.
The interfaces provided by the different CPU derivatives are marked in colour accordingly.

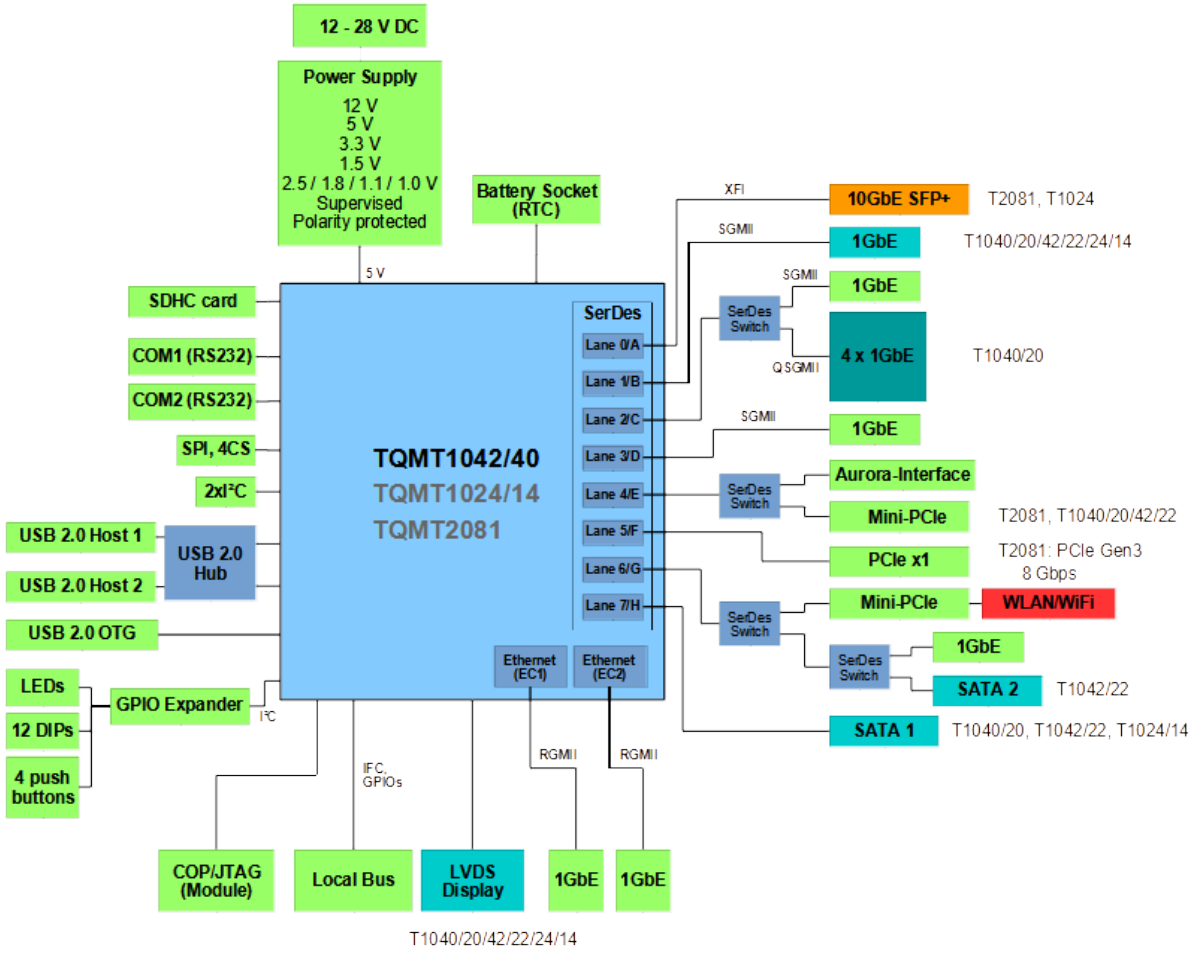

Figure 2: STKT104X block diagram

3.2 Technical data overview

3.2.1 Technical data electronics

The STKT104X supports the following interfaces, including PHYs and connectors:

- Max. 5 × Gigabit Ethernet
- 2 × UART
- Max. 3 × PCIe
- 1 × SDXC or eMMC
- Max. 2 × SATA [1]
- Max. 2 × USB 2.0 Host
- 1 × I²C (available for user)
- SPI
- COP/JTAG
- Aurora Interface through SerDes Lane 5 [2]
- MMC
- 2nd I²C
- 16 bit IFC (“Local Bus”)
- USB OTG
- GPIOs

The number of interfaces available also depends on the SerDes configuration.

3.2.2 Technical data mechanics

The STKT104X has overall dimensions of 230 mm × 170 mm.
Hexagonal bolts M3 × 12 are mounted on the STKT104X as spacers.

3.2.3 STKT104X component placement

The following STKT104X component placement top side view serves as orientation in order to search for interfaces and other components. With all following enlarged details this view serves as a reference.

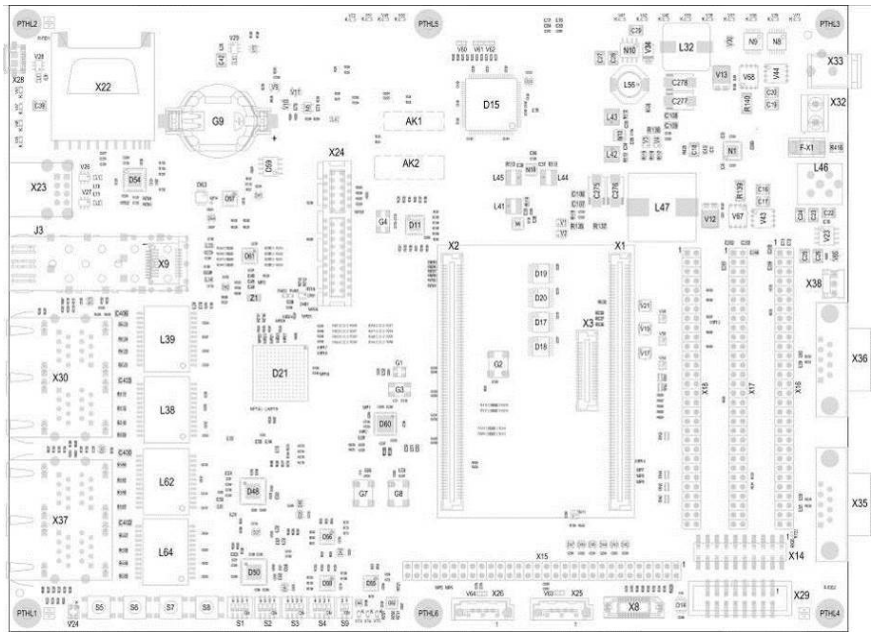

Figure 3: STKT104X, top view

1: Available with T1042/40/22/20, T1024/14, not with T2081.
2: According to NXP this interface is also qualified with T10xx CPUs and hence officially supported. Available with T1042/40/22/20, T1024/14, not with T2081.

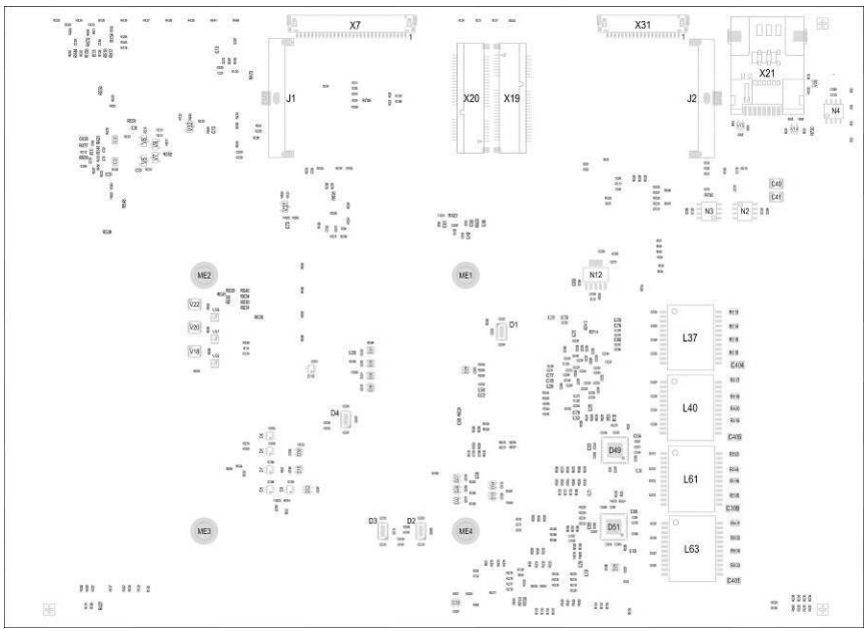

Figure 4: STKT104X, bottom view

Note: Orientation of illustrations	
	All detailed illustrations shown in this document have the same orientation as this top view. This illustration is also available as a separate pdf file.

3.3 System components

3.3.1 Clock generation

The following figure shows, which clocks on the STKT104X are required, and how they are generated.
The EC1 and EC2 interfaces are supplied with the 125 MHz outputs of the PHYs, or alternatively by a 125 MHz clock generator.

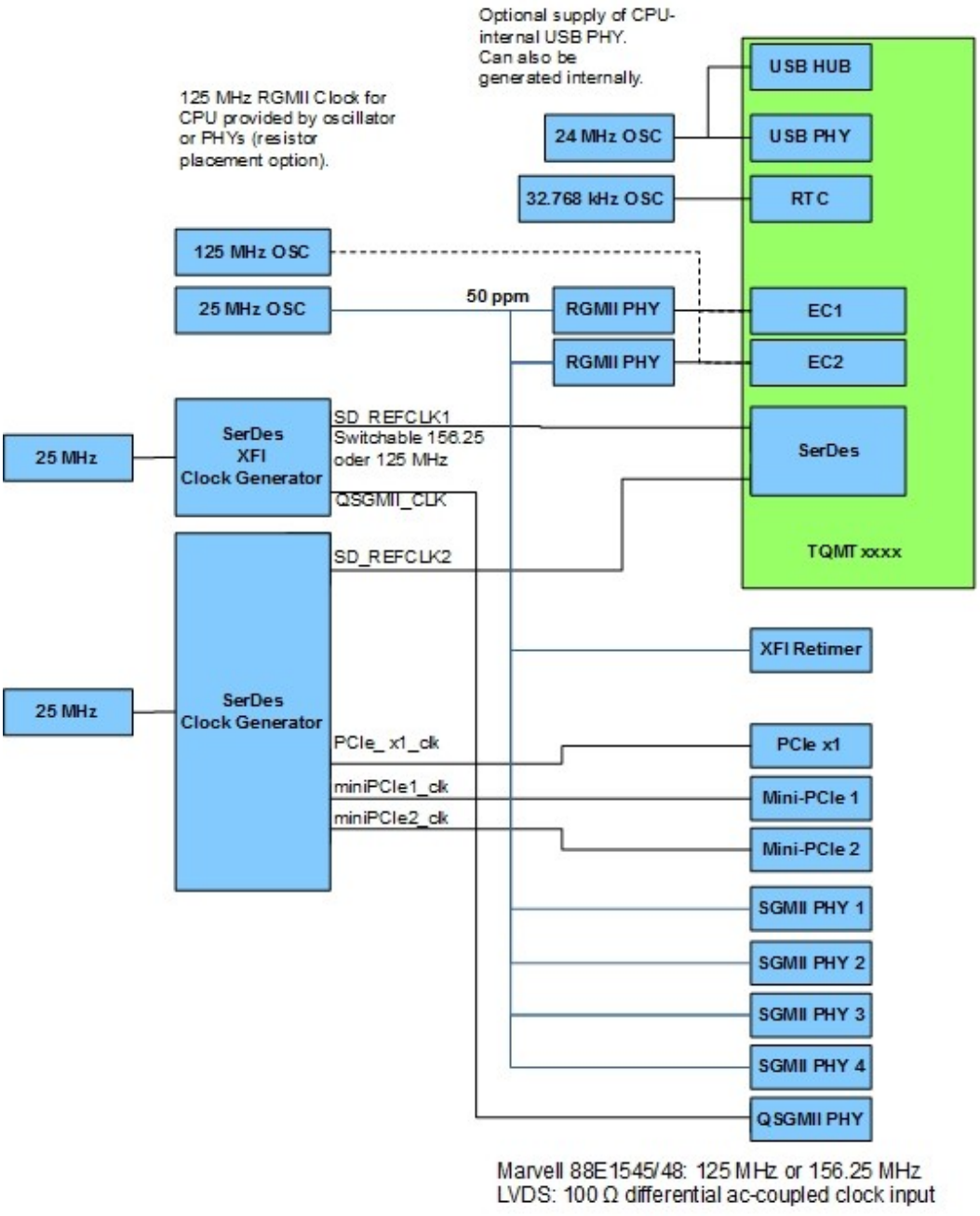

Figure 5: STKT104X clock generation

3.3.1.1 Ethernet RGMII

As an alternative to the CLK125 outputs of the PHYs, the 125 MHz for EC1 and EC2 can also be generated using a separate clock generator. The change-over is carried out with an analog switch, which is controlled by a GPIO (I/O expander). The STKT104X provides an assembly option (default: Clock generator).

- Clock generator: SXO25-03025-S-E-50-W-125.000MHZ-T
- Clock driver: NC7SV126
- Analog switch: TI TS5A23157DGSR

3.3.1.2 25 MHz Ethernet PHY clock

All RGMII and SGMII Ethernet PHYs require 25 MHz reference clocks.
A clock generator is provided to supply a maximum of five PHYs.
The Ethernet PHYs operate with an I/O voltage of 2.5 V.
Therefore, the clock buffers are also used as level shifters.

- SXO3-0507-E-50-W-25.000MHZ-T
- Quartz 25 MHz, 50 ppm
- Clock driver and level shifter: NC7SV126

3.3.1.3 24 MHz USB PHY clock

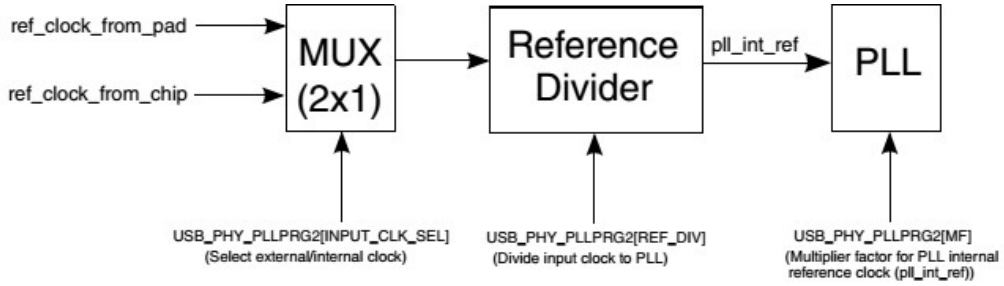

Figure 6: T2081 / T1040 / T1024 USB PHY clock

The PHY clock is derived from the 100 MHz system clock. An additional external supply is provided. The signal USBCLK is connected to the T1042 / T2081 / T1024 by default.
The T1024 can also be supplied with an external 24 MHz clock using a DIP switch and two Tristate buffers.

- Clock generator: SXO3-0507-E-50-W-24.000MHZ-T TJE, 50 ppm
- Clock driver: NC7SV126 ⇨ level shifting to 1.8 V (OVDD or O1VDD)

3.3.2 SerDes interfaces

The STKT104X generates the reference clocks for the TQMT104x SERDES interfaces. To use different protocols the TQMT104x SERDES interface has to be supplied with different clocks. Spread Spectrum Clocking is only possible with PCIe to improve EMC properties. The required clocks are 100 MHz, 125 MHz and 156.25 MHz. 100 MHz are required for the following components on the STKT104X:

- 2 × Mini PCIe slot
- 1 × PCIe slot
- 1 × CPU SerDes reference clock

Since the 2.5G SGMII is not used, all interfaces are supplied with 100 MHz, except for the 10 GbE (XFI).
Since XFI is only routed to Lanes A and B, the clock supply uses compulsory PLL1 and therefore SD_REF_CLK1.
SGMII mode of SerDes runs on Lanes A to D, likewise on PLL1, but with a different reference clock (100 MHz).
PLL1 can drive Lanes A to H, and PLL2 can drive Lanes C to H. PCIe, SGMII (1G) and QSGMII can work with a 5 GHz PLL, SATA with 3 GHz and Aurora with 2.5 / 5 GHz. This results in the following SerDes configuration:

- T2081: PLL1 is supplied with 156.25 MHz, PLL2 with 100 MHz
- T1040 / T1020 and T1042 / T1022: Both are supplied with 100 MHz
- T1024 / T1014: Depending on configuration PLL1 is supplied with 100 MHz or 156.25 MHz, PLL2 with 100 MHz

Switching is done by a DIP switch.
Spread Spectrum is only possible with the clock generator connected to PLL2.
This feature cannot be used with the T1042 and the preset SerDes configuration. It can be used after a software modification.
PCIe Lanes are supplied by PLL1, other configurations are also possible.

3.3.2.1 SerDes clock architecture

Two clock generators are present. Not shown in Figure 7 is the switch-over between 156.25 MHz and 125 MHz. This is done by a DIP switch (CLKSEL pin of the clock generator). For Spread Spectrum settings DIP switches exist likewise.

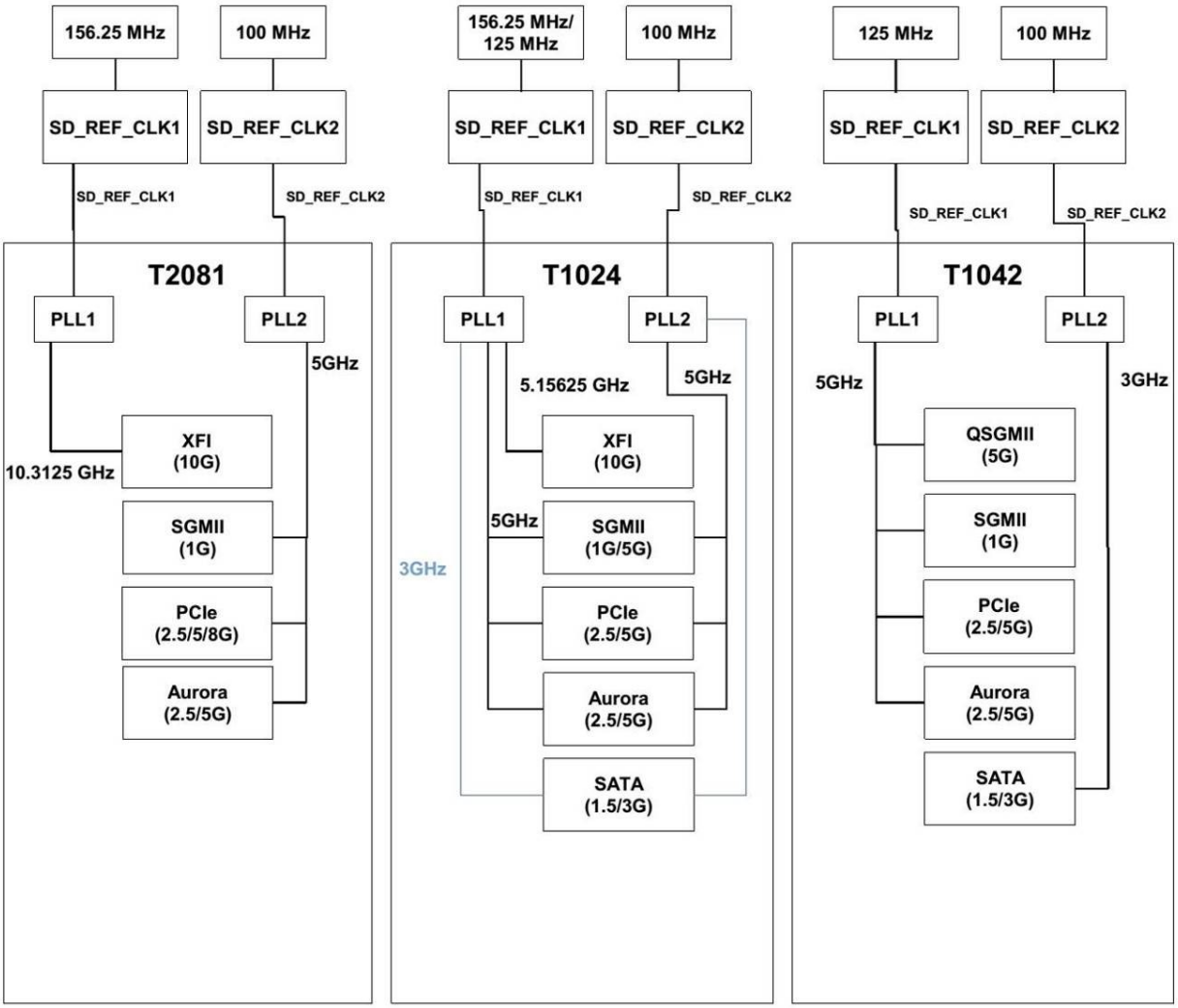

Figure 7: Clock architecture SerDes TQMT104x

Note: Spectrum Spreading	
	Spectrum Spreading is only permitted for PCIe with the CPUs used. If this feature is activated at the Clock Generator, all Lanes, which use different protocols, but are supplied by the same PLL, cannot be used anymore. By selecting the Clock Generators is defined, that Spectrum Spreading can only be activated at SD_REFCLK_2, and hence PLL2.

156.25 MHz are required as a reference clock for the 10 GbE interface. The following oscillator is used:

- ICS843002-01: 156.25 / 125 / 62.5 MHz, 3.3 V, LVPECL, RMS phase jitter 0.6 ps typ. @ 125 MHz

If no HCSL compatible clock (0.7 V logic) is used, the clock line must be AC coupled. To use SATA on the T1024 simultaneously with SGMII, PCIe or Aurora the 156.25 MHz oscillator can also generate 125 MHz or 100 MHz.

3.3.2.2 SerDes multiplexing

To make the best use of all CPU variations on the TQMT104x, the SerDes Lanes on the STKT104X are used several times by means of multiplexing. Beside the PCIe switches mentioned below, a 3-fold pad is used for Lane A (SD_0), since on this Lane the XFI interface (10 GbE, 10.625 GHz) is provided on the T2081. The SerDes Switches are controlled by DIP switches. Their state can be read and written by the CPU via I/O ports of an IIC GPIO expander (10 kΩ PD, 100 kΩ PU). The following interfaces are available on the STKT104X by default.

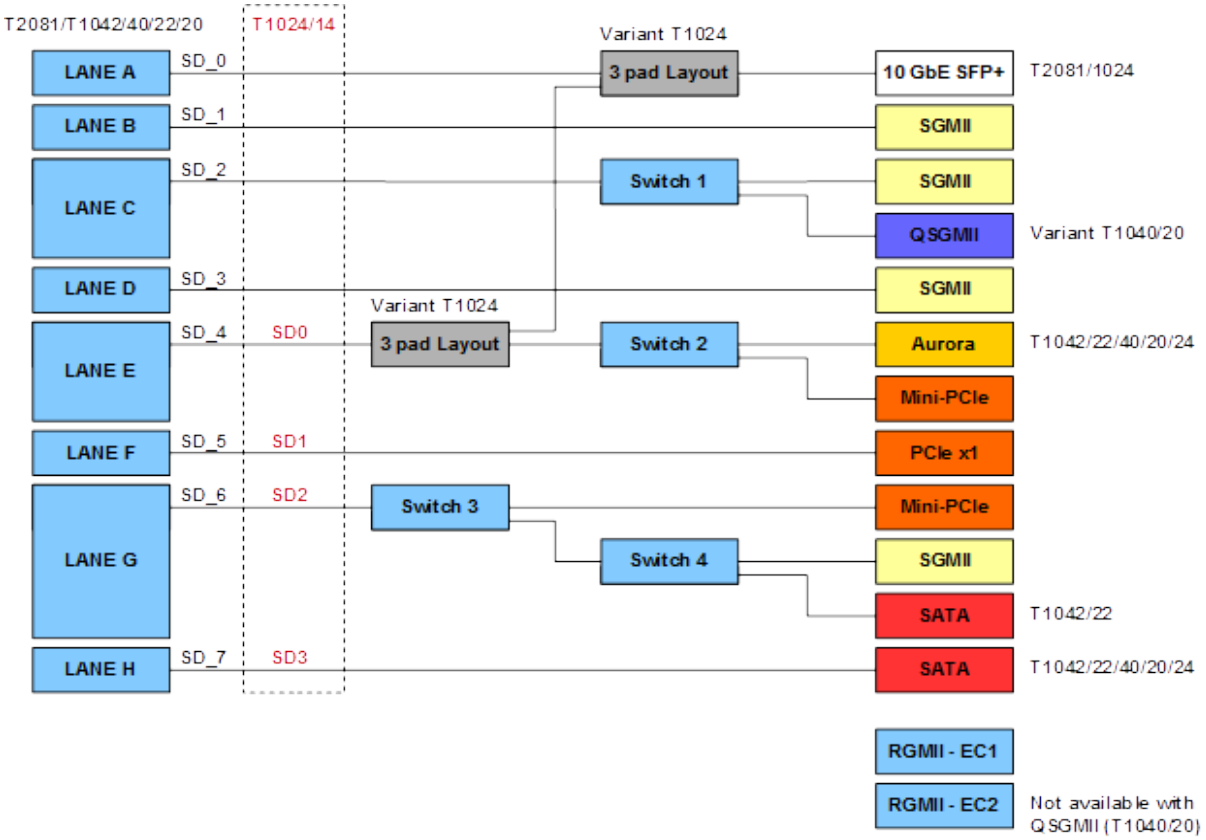

Figure 8: SerDes implementation

3.3.2.2 SerDes multiplexing (continued)

A 4-fold DIP switch is used to control the four PCIe lanes.

Table 2: Assignment PCIe lanes

DIP switch	Position	Function
S3-1	On	Lane C: SGMII
	Off	Lane C: QSGMII
S3-2	On	Lane E: Mini PCIe
	Off	Lane E: Aurora
S3-3	On	Lane G: Mini PCIe
	Off	Lane G: SGMII or SATA
S3-4	On	Lane G: SGMII
	Off	Lane G: SATA

Table 3: SerDes multiplexing: Available interfaces

CPU	[SRDS_PRTCL_S1_RCW]	10 GbE (SFP+)	SGMII	QSGMII	Aurora	PCIe	Mini PCIe	SATA	RGMII MACs
T2081	0x70	1	3	–	–	–	–	–	2
	0xF2	–	3	–	–	1	2	–	2
T1040 / T1020	0x66	–	1	1	–	1	2	1	1
	0x8E	–	3	–	1	1	–	1	2
T1042 / T1022	0x86	–	3	–	–	1	2	1	2
	0x88	–	3	–	–	1	1	2	2
	0x8E	–	3	–	1	1	–	1	2
T1024 / T1014	0x95	1	–	–	–	1	1	–	2
	0x119	–	–	–	1	1	–	–	2
	0x05A	–	1	–	–	1	–	1	2

The PCIe switches are supplied with 3.3 V. During power-up the power-down pin is pulled to 3.3 V with a PU. Depending on RESET_OUT# the switches are activated.

3.3.3 Reset generation and Power-Up

The following block diagram shows the reset generation:

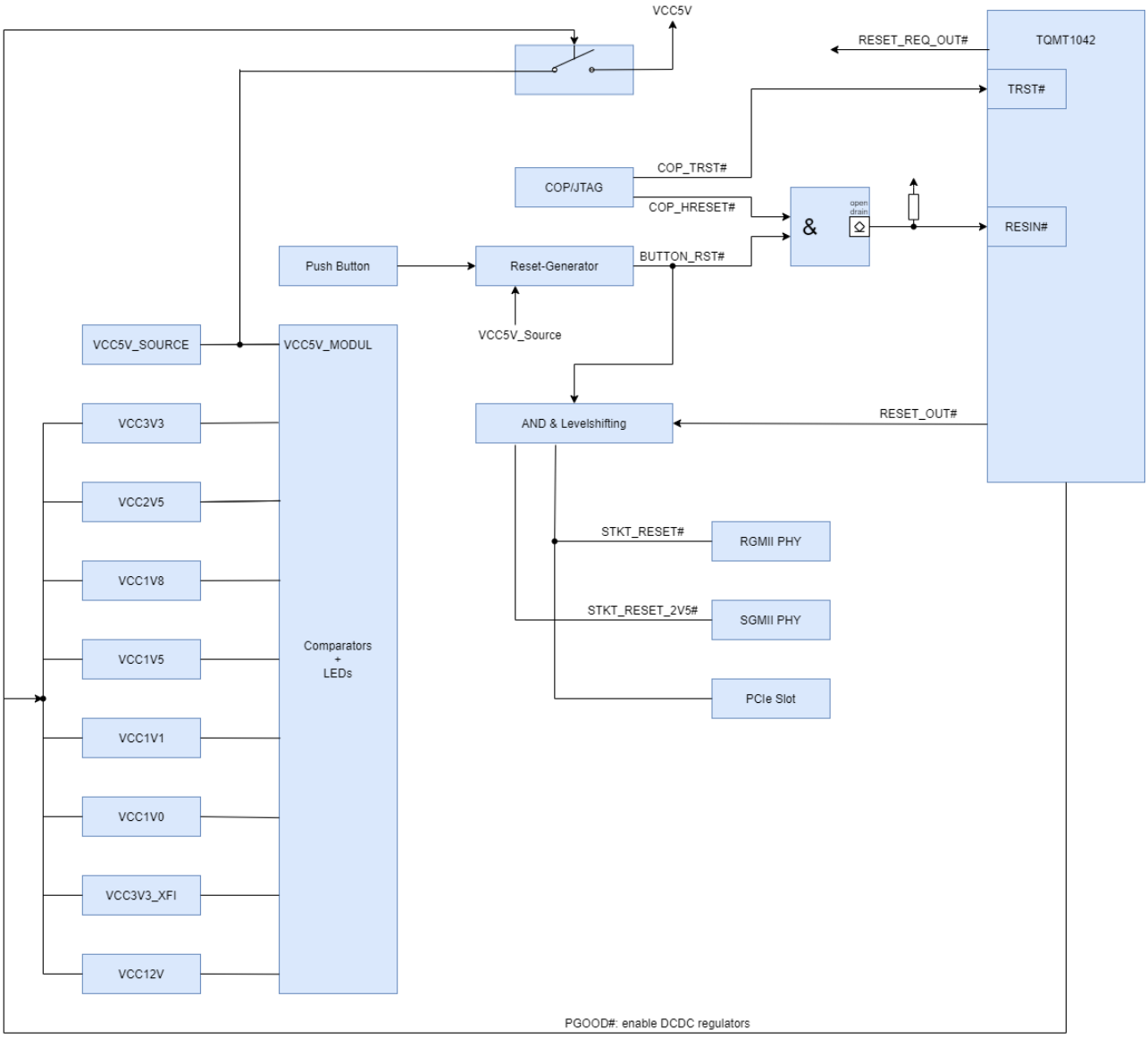

Figure 9: Block diagram Reset and Power-Up

Power-up:

1. The system is supplied with power / switched on and with it the VCC5V regulator is activated. VCC5V serves directly as module supply and the power sequencing begins, as soon as VCC5V has reached a certain threshold. RESIN# is pulled by the reset generator.
2. As soon as the power sequencing on the TQMT104x is completed and all voltages on the TQMT104x are OK, all other buck regulators on the carrier board are activated by the TQMT104x PGOOD# Signal.
3. As soon as all monitored voltages are within the permitted limits, the signal PGOOD_STKT goes high and the reset generator releases the TQMT104x and the STKT104X from reset.
4. When the CPU releases RESET_OUT# in the reset sequence, all reset signals on the TQMT104x are withdrawn.

Reset during operation:

During operation a reset can be triggered by the following devices:

- TQMT104x
- Voltage monitoring
- Reset button

- Debugger: JTAG or AURORA

On the STKT104X the Debugger Reset is triggered indirectly by the CPU signal RESET_OUT#.

Table 4: Devices on the STKT104X connected to reset

Device	Reset	I/O voltage
TI DP83867 1GbE PHYs	6 × RESET#	2.5 V
Marvell 88E1340S QSGMII	RESET#	2.5 V
USB Hub USB2514Bi	RESET#	3.3 V
PCIe Slot	RESET#	3.3 V
Mini PCIe Slot	RESET#	3.3 V
Mini PCIe Slot	RESET#	3.3 V
Display: (LVDS)	SHTDN#, RESET#	3.3 V
SerDes Switches	4 × PWRDN	3.3 V
Clock Generators	2 × RESET#: – 849N202I – 9GFV0441	3.3 V

3.3.4 Battery socket RTC

An RTC is present on the TQMT104x. It is supplied by a socketed lithium battery CR2032 on the STKT104X. The voltage can be measured at a pin header, or an external voltage can be fed alternatively.
A Schottky diode is provided to protect the battery (danger of explosion) against external voltage supply. A series resistor is provided to protect the battery against short circuit.
During storage the battery is protected against discharge with an insulation strip.

3.3.5 Diagnostic LEDs

(See 3.6.4.)

3.4 STKT104X interfaces

3.4.1 Gigabit Ethernet

To provide as many Gigabit Ethernet ports as possible, the following interfaces are used:

- SGMII: Max. four
- QSGMII: Only supported by T1040 / T1020
- RGMII: Two MACs are available for all selected SerDes configurations

For the PHY-internal generation of 125 MHz, a 125 MHz clock, or a 25 MHz Quartz can be used.

3.4.2 Ethernet clock (EC1, EC2)

The clock rate of Ethernet controller 1 and 2 (EC1, EC2), which permit 1Gbit Ethernet via RGMII, is 125 MHz.
Different sources can provide the CPU with this clock.

Note: Clock skew	
	The RGMII output clock skew is very different.

Table 5: Clock skew

Skew	T1042 / T1022	T1024 / T1014	T2081
Data to clock output skew	–620 ps to +520 ps (typ. 0 ps)	–500 ps to +500 ps (typ. 0 ps)	–750 ps to +1,000 ps (typ. 0 ps)
Data to clock input skew	2.0 to 3.0 ns	1.0 to 2.6 ns	1.0 to 2.6 ns

A double clock supply for the RGMII interface is provided on the STKT104X: The RGMII interface is supplied by either a clock generator (125 MHz) or the clock output of one the PHYs as a placement option.

3.4.3 QSGMII

A Marvell PHY 88E1340S-A0-BAM2I000 is assembled.
The outputs of the ICS849N202I can be adapted independently to LVDS via I^2C.
The factory configuration is LVPECL.

3.4.4 Magnetics and jacks

A total of 8 magnetics and RJ45 jacks for RGMII (2), SGMII (1, all other via ports of the QSGMII / SGMII PHY) and QSGMII (4) are provided on the STKT104X. Two 4-fold stacked RJ45 jacks are provided on the STKT104X.
The TI PHY DP83867 is used, since it also supports RGMII and SGMII, and enough PHY addresses can be set.

3.4.5 EMI - Ethernet Management Interface

The EMI is supplied, like the RGMII interface, by L1VDD (2.5 V).

Table 6: PHY addresses and I/O voltages

PHY	Device	PHY address	I/O voltage
RGMII PHY1	TI DP83867	01110b	2.5 V
RGMII PHY2	TI DP83867	00101b	2.5 V
SGMII PHY1	TI DP83867	00011b	2.5 V
SGMII PHY2	TI DP83867	00001b	2.5 V
QSGMII PHY	Marvell 88E1545 / 48 Marvell 88E1340S	11100b (Port 0) 11101b (Port 1) 11110b (Port 2) 11111b (Port 3)	2.5 V or 3.3 V

3.4.6 10 Gigabit Ethernet (only T1024 / T1014, T2081)

10 GbE interfaces via one Lane are supported by the CPUs T1024 / T1014 and T2081.

- Supply voltage: 3.3 V (SFP + connector)
- Connected to CPU via SerDes Lane 0 (A)

The reference clock of SerDes Lane 1 (XFI, 10GBit Ethernet) is 156.25 MHz.

3.4.7 DUART

The T-series CPUs provide DUART modules 1 and 2. Two UART interfaces are converted to RS232 level and routed to the TQMT104x connectors. The other two UART interfaces are routed directly to the TQMT104x connectors.
UART1 and UART2 provide Hand Shake signals RTS# and CTS#, UART3 and UART4 do not provide these Hand Shake signals.

Table 7: Possible UART configurations

[UART_BASE]=0b110	[UART_BASE]=0b111
UART1_SOUT	UART1_SOUT
UART1_SIN	UART1_SIN
UART1_RTS_B	UART3_SOUT
UART1_CTS_B	UART3_SIN
UART2_SOUT	UART2_SOUT
UART2_SIN	UART2_SIN
UART2_RTS_B	UART4_SOUT
UART2_CTS_B	UART4_SIN

On the STKT104X both RS232 interfaces are routed to two 9-pin D-SUB connectors.
An additional 10-pin header is provided on the STKT104X, which offers the DUART signals of both ports with CPU signal levels.

3.4.8 PCI-Express

A total of three PCIe slots result from the SerDes configuration. Two Mini PCIe ports and one PCIe ×1 port are provided.
The STKT104X provides a corresponding power supply (12 V and 3.3 V for PCIe, as well as 3.3 V and 1.5 V for Mini PCIe) and the PCIe slots. The power supply is described in a separate chapter.

3.4.9 SDXC / MMC

The CPUs provide an SDXC (SD 3.0) compatible memory controller.
An SD card slot, as well as protective circuitry is provided on the STKT104X. SD, SDHC and SDXC storage media can be connected. The interface is 4 bit wide. All SDIO modes provided by the CPU are supported, except for the MMCplus (8 bit).
Alternatively an eMMC can be connected to the SDXC controller. The eMMC flash is an assembly option on the TQMT104x.
For save operation of eMMC and SD card via the same controller, the interface signals are multiplexed on the TQMT104x.
On the CPU the interface is supplied by EVDD (or OVDD with the T2081), level shifter between 1.8 V and 3.3 V are provided.
Booting from SDHC is provided in case the main boot source is non-functional. A DIP switch signal forces boot from SDHC (I/O of system controller on TQMT104x). The RCW can either be read from SD card or the µC/EEPROM on the TQMT104x. The signal can also be read by the GPIO expander and overwrite the DIP switch state.
For the T1024 an erratum exists regarding "loading the RCW from SDHC". The affected signals / pins are used as SPI chip selects (SDHC_VS as USBCLK).
The following table lists the errata for the CPUs T1024 and T1040 regarding SDHC and RCW:

Table 8: Errata for T1024 and T1040 "Loading the RCW from SDHC"

No.	Description	Remark
A-007359	SDHC_VS signal is in high impedance while RCW is loaded from eSDHC interface	No fix planned
A-007396	SDHC_CMD_DIR, SDHC_DAT0_DIR and SDHC_DAT123_DIR signals are in high impedance while RCW is loaded from eSDHC interface	No fix planned

3.4.10 SATA

SATA is also implemented via the SerDes block. Both SATA ports are directly routed to SATA connectors using SerDes Lane H (or D with T1024 / T1014). Two cascaded 2:1 Mux SerDes Switches are provided for Lane G (PCIe, SGMII, and SATA). ESD protection is provided.

The differential SATA signals are AC coupled with 10 nF and routed to the connectors with 100 Ω impedance.

3.4.11 TDM, UC and DIU

The TDM bus, the UC and the DIU are available on all supported CPUs, except for the T2081.

Table 9: Signals TDM / GPIO / UC / DIU

Signal name	CPU ball
CLK09 / GPIO4_15 / BRGO2 / DIU_D10	P4
CLK10 / GPIO4_22 / BRGO3 / DIU_D11	P3
CLK11 / GPIO4_16 / BRGO4 / DIU_DE	N4
CLK12 / GPIO4_23 / BRGO1 / DIU_CLK_OUT	M4
TDMA_RQ / GPIO4_14 / UC1_CDB_RXER / DIU_D4	R2
TDMA_RSYNC / GPIO4_11 / UC1_CTSB_RXDV / DIU_D1	U1
TDMA_RXD / GPIO4_10 / UC1_RXD7 / DIU_D0	U2
TDMA_TSYNC / GPIO4_13 / UC1_RTSB_TXEN / DIU_D3	R1
TDMA_TXD / GPIO4_12 / UC1_TXD7 / DIU_D2	T1
TDMB_RQ / GPIO4_21 / UC3_CDB_RXER / DIU_D9	R4
TDMB_RSYNC / GPIO4_18 / UC3_CTSB_RXDV / DIU_D6	T3
TDMB_RXD / GPIO4_17 / UC3_RXD7 / DIU_D5	U4
TDMB_TSYNC / GPIO4_20 / UC3_RTSB_TXEN / DIU_D8	R3
TDMB_TXD / GPIO4_19 / UC3_TXD7 / DIU_D7	T4
IIC4_SCL / GPIO4_02 / EVT5_B / DIU_HSYNC	AA3
IIC4_SDA / GPIO4_03 / EVT6_B / DIU_VSYNC	AB3

3.4.12 Display interface unit DIU

The following diagrams and tables show the DIU timing and data mapping for the T1040:

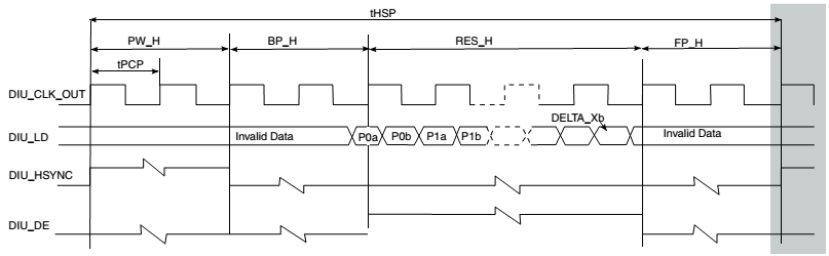

Figure 15-31. Horizontal sync signals

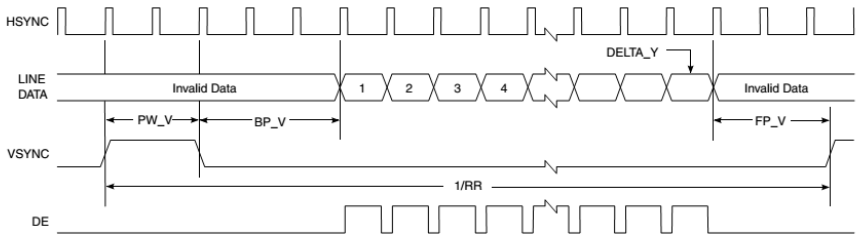

Figure 15-32. Vertical sync signals

The following table describes the pixel data mapping.

Table 15-64. Pixel data mapping

Data bus	P0a	P0b	P1a	P1b	Pxa	Pxb
D11	G0[3]	R0[7]	G1[3]	R1[7]	Gx[3]	Rx[7]
D10	G0[2]	R0[6]	G1[2]	R1[6]	Gx[2]	Rx[6]
D9	G0[1]	R0[5]	G1[1]	R1[5]	Gx[1]	Rx[5]
D8	G0[0]	R0[4]	G1[0]	R1[4]	Gx[0]	Rx[4]
D7	B0[7]	R0[3]	B1[7]	R1[3]	Bx[7]	Rx[3]
D6	B0[6]	R0[2]	B1[6]	R1[2]	Bx[6]	Rx[2]
D5	B0[5]	R0[1]	B1[5]	R1[1]	Bx[5]	Rx[1]
D4	B0[4]	R0[0]	B1[4]	R1[0]	Bx[4]	Rx[0]
D3	B0[3]	G0[7]	B1[3]	G1[7]	Bx[3]	Gx[7]
D2	B0[2]	G0[6]	B1[2]	G1[6]	Bx[2]	Gx[6]
D1	B0[1]	G0[5]	B1[1]	G1[5]	Bx[1]	Gx[5]
D0	B0[0]	G0[4]	B1[0]	G1[4]	Bx[0]	Gx[4]

On the STKT104X the 12-bit RGB display signals provided by the TQMT104x, are converted to LVDS by a TI DS90C387R.
An LVDS display has to support the following LVDS interface addressing scheme:

Table 10: LVDS interface

LVDS signal	Signal / Colour						
LVDS-A0	G2	R7	R6	R5	R4	R3	R2
LVDS-A1	B3	B2	G7	G6	G5	G4	G3
LVDS-A2	DE	VSYNC	HSYNC	B7	B6	B5	B4
LVDS-A3	RSV	B1	B0	G1	G0	R1	R0

3.4.12 Display interface unit DIU (continued)

Since the display data are output by the CPU with 12-bit (two data per clock), the selection of suitable displays is limited.
Displays with a 24-bit interface can only be connected via a suitable Deserializer, e.g. the TI DS90CF388.
To control an LVDS display, the LVDS CMD connector X31 is placed near the LVDS signal connector X7.
The FFC connector X31 provides a USB interface and control signals for display and backlight.
In addition to the data signals, 5 V and 12 V are available as supply voltages.

Table 11: Device LVDS CMD connector X31

Manufacturer	Part Number	Description	Package
Hirose	DF19G-20P-1H	Board-to-Cable FFC connector 20-pin, 1 mm pitch	SMT20

Table 12: Pinout LVDS CMD X31

Pin	Pin name	Signal	Dir.	Remark
1	VCC12V	VCC12V	P	I_{max} = 1 A
2	VCC12V	VCC12V	P	
3	VCC12V	VCC12V	P	
4	DGND	DGND	P	
5	DGND	DGND	P	
6	DGND	DGND	P	
7	VCC5V	VCC5V	P	I_{max} = 1 A
8	VCC5V	VCC5V	P	
9	DGND	DGND	P	
10	DGND	DGND	P	
11	VBUS	USB_H4_VBUS	P	EMI filter in series
12	DGND	DGND	P	
13	D+	USB_H4_D_N	I/O	Common mode choke in series
14	D–	USB_H4_D_P	I/O	Common mode choke in series
15	DGND	DGND	P	
16	STKT_RESET	STKT.RESET	O	
17	LCD_BLT_EN	LCD.BLT_EN	O	
18	LCD_PWR_EN	LCD.PWR_EN	O	10 kΩ PU to VCC3V3
19	PWM0	LCD.CONTRAST	O	10 kΩ PU to VCC3V3
20	DGND	DGND	P	
M1-2	DGND	DGND	P	

3.4.12 Display interface unit DIU (continued)

The LVDS interface is routed to 30-pin FFC (X7).
In addition to the LVDS signals 3.3 V and 5 V are provided at the connector.

Table 13: Device LVDS connector X7

Manufacturer	Part Number	Description	Package
Hirose	DF19G-30P-1H	Board-to-Cable FFC connector, 30-pin, 1 mm pitch	SMT30

Table 14: Pinout LVDS X7

Pin	Pin name	Signal	Dir.	Remark
1	0_TX0–	LVDS0_TX0_N	O	22 Ω in series
2	0_TX0+	LVDS0_TX0_P	O	22 Ω in series
3	0_TX1–	LVDS0_TX1_N	O	22 Ω in series
4	0_TX1+	LVDS0_TX1_P	O	22 Ω in series
5	0_TX2–	LVDS0_TX2_N	O	22 Ω in series
6	0_TX2+	LVDS0_TX2_P	O	22 Ω in series
7	DGND	DGND	P	
8	0_CLK–	LVDS0_CLK_N	O	22 Ω in series
9	0_CLK+	LVDS0_CLK_P	O	22 Ω in series
10	0_TX3–	LVDS0_TX3_N	O	22 Ω in series
11	0_TX3+	LVDS0_TX3_P	O	22 Ω in series
12	–	–	–	NC
13	–	–	–	NC
14	DGND	DGND	P	
15	–	–	–	NC
16	–	–	–	NC
17	DGND	DGND	P	
18	–	–	–	NC
19	–	–	–	NC
20	–	–	–	NC
21	–	–	–	NC
22	–	–	–	NC
23	–	–	–	NC
24	DGND	DGND	P	
25	VCC5V	VCC5V_LVDS	P	I_{max} = 1 A
26	VCC5V	VCC5V_LVDS	P	
27	VCC5V	VCC5V_LVDS	P	
28	VCC3V3	VCC3V3_LVDS	P	I_{max} = 1 A
29	VCC3V3	VCC3V3_LVDS	P	
30	VCC3V3	VCC3V3_LVDS	P	
M1-2	DGND	DGND	P	

3.4.13 USB 2.0 hosts

Two USB 2.0 host interfaces including PHY are provided by the TQMT104x.
The USB jacks (type A), the USB power supply (incl. current limitation), protective circuitry and a hub are implemented on the STKT104X.
A 4-port hub connected to USB1 is used. With it two USB 2.0 hosts via A-Type jacks are available permanently.
The 3rd host is routed to the Mini PCIe slot (WLAN card); the 4th host is routed to a header as an option.
USB2 is used as an OTG interface.

3.4.14 USB hub configuration

As an I²C master the hub can read its configuration from an EEPROM, be configured by SMBus or by bootstrapping.

Table 15: Configuration USB hub

Signal	PU / PD	Remark
SCL / SMBCLK / CFG_SEL0	100 kΩ PD (10 kΩ PU to VCC, NP)	- Strap options enabled - Self-powered operation enabled - Individual power switching and sensing
HS_IND / CFG_SEL1	100 kΩ PD (10 kΩ PU to VCC, NP)	
SDA / SMBDATA / NON_REM1	100 kΩ PD (10 kΩ PU to VCC, NP)	- All ports removable
SUSP_IND / LOCAL_PWR / NON_REM0	100 kΩ PD	Self / local power source not available ⇨ powered by host
USBDM_DN3 / PRT_IDS_M3	100 kΩ PU to VCC	Disable Port 4

3.4.15 USB 2.0 OTG

The internal PHYs support OTG. The PHY of USB2 is routed to a Micro AB USB jack and used as an OTG interface.
To use this interface as a host, as well, an adaptor (Micro USB plug to USB A-Type connector) is provided.
The CPU supports the modes "Host" and "Device" at both interfaces.
THE USB PHY ID Detect USB2_UID is supplied by USB_OVDD and with it 1.8 V.

3.4.16 WLAN / WiFi

A Mini PCIe slot with USB signals is provided.

3.4.17 I²C buses

The supported pin compatible T-series CPUs each provide four I²C buses. The I²C buses are routed to 3-pin headers.
Two I²C buses are available.

- IIC1: Used on the TQMT104x and routed to the connectors –available with all CPUs
- IIC2: Used on the STKT104X – available with all CPUs
- IIC3: Pins are configured as a GPIOs
- IIC4: Pins are configured for DIU

3.4.18 I²C devices

Table 16: IIC1

Device	Function	7-bit address
M24256	EEPROM	0x57 / 101 0111b
SE97B	EEPROM (Normal Mode)	0x50 / 101 0000b
	EEPROM (Protection Mode)	0x30 / 011 0000b
	Temperature sensor	0x18 / 001 1000b
PCF85063A	RTC	0x51 / 101 0001b
SA560004EDP	Temperature sensor	0x4C / 100 1101b
ADM1068	Supervisor	0x44 / 100 0100b
MKL04Z16	System Controller	0x11 / 001 0001b

Table 17: IIC2

Device	Address (hex)	Address (binary)	I/O voltage
CPU		Host	1.8 V
GPIO Expander 1	0x20	0010 0000b	3.3 V
GPIO Expander 2	0x21	0010 0001b	3.3 V
GPIO Expander 3	0x22	0010 0010b	3.3 V
10 GbE Retimer	SMBus: 0x30 write 0x31 read	 0011 0000b 0011 0001b	3.3 V (also 2.5 V possible)
LVDS	0x38	0011 1000b	3.3 V
GPIO Expander 4	0x42	0100 0010b	3.3 V
USB Hub	0x50 0x2C	0101 0000b (Master) 0010 1100b (Slave SMBus)	3.3 V
Clock Generator ICS849N202I	0x68	0110 1000b	
STMPE811	0x82	1000 0010b	3.3 V
PCIe mini Slot 1	(TBD)	(TBD)	3.3 V
PCIe mini Slot 2	(TBD)	(TBD)	3.3 V
PCIe x1 Slot	(TBD)	(TBD)	3.3 V
SFP+ Module	(TBD)	(TBD)	3.3 V

Depending on the track lengths, the number of I²C devices connected and their input capacitances, it may be necessary to add external pull-ups.

An I/O expander has a typical input capacitance of 5 to 10 pF. To prevent exceedance of maximum rise and fall times of 300 ns according to I²C specification, the maximum bus load can be calculated as follows:

- TXS0102: $C_{ges} < (300 * 10^{-9} / (10 * 10^{3} * 0.847298)) = 35.4$ pF

3.4.19 SPI

The eSPI interface of the CPU is provided at a pin header.

The four SPI chip selects are partly multiplexed with the SDHC interface [DATA4:7].

The I²C interface as well as the SPI interface is supplied with 1.8 V (CVDD) to remain compatible with the T2081.

3.4.20 COP/JTAG

The COP/JTAG interface of the CPU is routed with the Aurora interface to a 22-pin header.
Lauterbach provides a suitable debugger for the Aurora interface. Up to now this only supports the direction CPU ⇨ debugger.
The connector pin assignment deviates if the interface is used bidirectional.
The Freescale Gigabit TAP+ Trace is compatible, but an adaptor cable (provided by Samtec) must be used, however.
A header with JTAG signals only is also provided. Both headers are assembled by default. The CPU supply voltage is in all cases 1.8 V (OVDD). The Lauterbach debuggers detect the voltage level and behave accordingly.
The following boxed header is provided:

- JTAG: 093-3-016-0-F-BR1 MPG, SMD, 16 pin, RM 2.54, boxed header

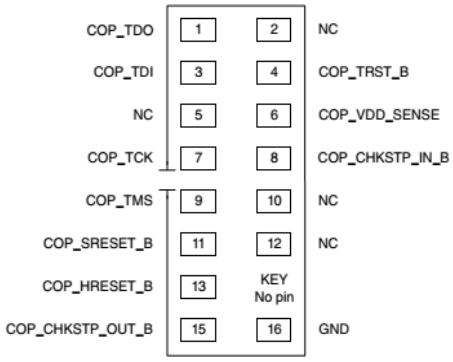

Figure 79. Legacy COP Connector Physical Pinout

Figure 10: COP/JTAG connector pinout

3.4.21 JTAG system controller

A header is provided on the STKT104X to program the system controller on the TQMT104x.
It is not recommended to alter the system controller since changes might damage the TQMT104x.

3.4.22 Aurora Interface via SerDes

The Aurora interface is supported by the CPUs T1042 / T1040, T1020 / T1022 and T1024 / T1014 at SerDes-Lane 5 (E). Debug headers see previous paragraph (3.4.20).
The cable to connect the Freescale Gigabit TAP and the 22-pin header has to be obtained from Samtec: HDR-141490-02.

3.4.23 IFC ("Local Bus")

The IFC is not used on the STKT104X, but it is routed to a header.
The IFC signals are also multiplexed with the Reset Configuration signals, which are controlled on the STKT104X by a pin to the TQMT104x system controller.

3.4.23 IFC ("Local Bus") (continued)

Table 18: IFC signals

IFC	Usage	CPU ball	Voltage
IFC_AD00 / CFG_GPINPUT0	IFC Address / Data / Reset Configuration	A4	OVDD
IFC_AD01 / CFG_GPINPUT1	IFC Address / Data / Reset Configuration	B5	OVDD
IFC_AD02 / CFG_GPINPUT2	IFC Address / Data / Reset Configuration	A5	OVDD
IFC_AD03 / CFG_GPINPUT3	IFC Address / Data / Reset Configuration	B6	OVDD
IFC_AD04 / CFG_GPINPUT4	IFC Address / Data / Reset Configuration	A6	OVDD
IFC_AD05 / CFG_GPINPUT5	IFC Address / Data / Reset Configuration	A7	OVDD
DGND			
IFC_AD06 / CFG_GPINPUT6	IFC Address / Data / Reset Configuration	B8	OVDD
IFC_AD07 / CFG_GPINPUT7	IFC Address / Data / Reset Configuration	A8	OVDD
IFC_AD08 / CFG_RCW_SRC0	IFC Address / Data / Reset Configuration	B9	OVDD
IFC_AD09 / CFG_RCW_SRC1	IFC Address / Data / Reset Configuration	A9	OVDD
IFC_AD10 / CFG_RCW_SRC2	IFC Address / Data / Reset Configuration	A10	OVDD
IFC_AD11 / CFG_RCW_SRC3	IFC Address / Data / Reset Configuration	B11	OVDD
DGND			
IFC_AD12 / CFG_RCW_SRC4	IFC Address / Data / Reset Configuration	A11	OVDD
IFC_AD13 / CFG_RCW_SRC5	IFC Address / Data / Reset Configuration	B12	OVDD
IFC_AD14 / CFG_RCW_SRC6	IFC Address / Data / Reset Configuration	A12	OVDD
IFC_AD15 / CFG_RCW_SRC7	IFC Address / Data / Reset Configuration	A13	OVDD
DGND			
IFC_A16	IFC Address	C5	OVDD
IFC_A17	IFC Address	C6	OVDD
IFC_A18	IFC Address	D7	OVDD
IFC_A19	IFC Address	C7	OVDD
IFC_A20	IFC Address	D8	OVDD
IFC_A21 / CFG_DRAM_TYPE	IFC Address	C8	OVDD
DGND			
IFC_A22	IFC Address	D9	OVDD
IFC_A23	IFC Address	C9	OVDD
IFC_A24	IFC Address	D10	OVDD
IFC_A25 / GPIO2_25 / IFC_WP1_B	IFC Address	C10	OVDD
IFC_A26 / GPIO2_26 / IFC_WP2_B	IFC Address	E11	OVDD
IFC_A27 / GPIO2_27 / IFC_WP3_B	IFC Address	C11	OVDD
DGND			
IFC_A28 / GPIO2_28	IFC Address	D11	OVDD
IFC_A29 / GPIO2_29 / IFC_RB2_B	IFC Address	C12	OVDD
IFC_A30 / GPIO2_30 / IFC_RB3_B	IFC Address	D12	OVDD
IFC_A31 / GPIO2_31 / IFC_RB4_B	IFC Address	E12	OVDD
IFC_CS_B0	IFC Chip Select	C13	OVDD
IFC_CS_B1 / GPIO2_10	IFC Chip Select	E15	OVDD
DGND			
IFC_CS_B2 / GPIO2_11	IFC Chip Select	D16	OVDD
IFC_CS_B3 / GPIO2_12	IFC Chip Select	C16	OVDD
IFC_CS_B4 / GPIO1_09	IFC Chip Select	E17	OVDD
IFC_CS_B5 / GPIO1_10	IFC Chip Select	C17	OVDD
IFC_CS_B6 / GPIO1_11	IFC Chip Select	D18	OVDD
IFC_CS_B7 / GPIO1_12	IFC Chip Select	C19	OVDD
DGND			
IFC_TE / CFG_IFC_TE	IFC External Transceiver Enable	B14	OVDD
IFC_WE0_B / CFG_ENG_USE0	IFC Write Enable	D13	OVDD
IFC_WP_B0 / CFG_ENG_USE2	IFC Write Protect	F17	OVDD
IFC_AVD	IFC Address Valid	D17	OVDD
IFC_BCTL	IFC Buffer control	A14	OVDD
IFC_CLE / CFG_RCW_SRC8	IFC Command Latch Enable / Write Enable	F16	OVDD
DGND			
IFC_RB_B0	IFC Ready / Busy CS0	B15	OVDD
IFC_RB_B1	IFC Ready / Busy CS1	A15	OVDD
IFC_CLK0	IFC Clock	A17	OVDD
IFC_CLK1	IFC Clock	A19	OVDD
DGND			
IFC_NDDDR_CLK	IFC NAND DDR Clock	D14	OVDD
IFC_NDDQS	IFC DQS Strobe	A16	OVDD
IFC_OE_B / CFG_ENG_USE1	IFC Output Enable	D15	OVDD
IFC_PAR0 / GPIO2_13	IFC Address & Data Parity	C15	OVDD
IFC_PAR1 / GPIO2_14	IFC Address & Data Parity	C14	OVDD
IFC_PERR_B / GPIO2_15	IFC Parity Error	E14	OVDD

3.4.24 GPIO

GPIOs are routed to a 2.54 mm header. An additional I²C controlled GPIO expander is available, which provides more GPIOs for DIP switches, push buttons and LEDs.

The following pins can be used as a GPIO on the supported CPUs.

Table 19: GPIO pins

Signal name	CPU ball	Description	Remark
IRQ			
IRQ00	F7	External Interrupt	
IRQ02	E9	External Interrupt	NC at the T1024 / 14
IRQ03 / GPIO1_23 / SDHC_VS	D1	External Interrupt	NC at the T1024 / 14
IRQ04 / GPIO1_24	D4	External Interrupt	NC at the T1024 / 14
IRQ05 / GPIO1_25	D5	External Interrupt	NC at the T1024 / 14
IRQ06 / GPIO1_26	AB4	External Interrupt	
IRQ07 / GPIO1_27	AD5	External Interrupt	NC at the T1024 / 14
IRQ08 / GPIO1_28 (used on STKT104X Rev. 02xx)	AB1	External Interrupt	NC at the T1024 / 14
IRQ09 / GPIO1_29	AC5	External Interrupt	
DMA			
DMA1_DREQ0_B / GPIO4_04 / TDM_TXD	P5	DMA1 channel 0 request	NC at the T1024 / 14
DMA1_DACK0_B / GPIO4_05 / TDM_TFS	U5	DMA1 channel 0 acknowledge	NC at the T1024 / 14
DMA1_DDONE0_B / GPIO4_06 / TDM_TCK	R5	DMA1 channel 0 done	NC at the T1024 / 14
DMA2_DREQ0_B / GPIO4_07 / TDM_RXD	V5	DMA2 channel 0 request	NC at the T1024 / 14
DMA2_DACK0_B / GPIO4_08 / EVT7_B / TDM_RFS	AA5	DMA2 channel 0 acknowledge	NC at the T1024 / 14
DMA2 DDONE0 B / GPIO4_09 / EVT8_B / TDM_RCK	Y5	DMA2 channel 0 done	NC at the T1024 / 14
TDM / DIU			
CLK09 / GPIO4_15 / BRGO2 / DIU_D10	P4	External Clock	NC at the T2081
CLK10 / GPIO4_22 / BRGO3 / DIU_D11	P3	External Clock	NC at the T2081
CLK11 / GPIO4_16 / BRGO4 / DIU_DE	N4	External Clock	NC at the T2081
CLK12 / GPIO4_23 / BRGO1 / DIU_CLK_OUT	M4	External Clock	NC at the T2081
TDMA_RQ / GPIO4_14 / UC1_CDB_RXER / DIU_D4	R2	Request	NC at the T2081
TDMA_RSYNC / GPIO4_11 / UC1_CTSB_RXDV / DIU_D1	U1	Receive Sync	NC at the T2081
TDMA RXD / GPIO4 10 / UC1_RXD7 / DIU_D0 / TDMA_TXD	U2	Receive Data	NC at the T2081
TDMA_TSYNC / GPIO4_13 / UC1_RTSB_TXEN / DIU_D3	R1	Transmit Sync	NC at the T2081
TDMA_TXD / GPIO4_12 / UC1_TXD7 / DIU_D2 / TDMA_RXD_EXC	T1	Transmit Data	NC at the T2081
TDMB_RQ / GPIO4_21 / UC3_CDB_RXER / DIU_D9	R4	Request	NC at the T2081
TDMB_RSYNC / GPIO4_18 / UC3_CTSB_RXDV / DIU_D6	T3	Receive Sync	NC at the T2081
TDMB_RXD / GPIO4_17 / UC3_RXD7 / DIU_D5 / TDMB_TXD	U4	Receive Data	NC at the T2081
TDMB TSYNC / GPIO4 20 / UC3_RTSB_TXEN / DIU_D8	R3	Transmit Sync	NC at the T2081
TDMB_TXD / GPIO4_19 / UC3_TXD7 / DIU_D7 / TDMB_RXD_EXC	T4	Transmit Data	NC at the T2081

To provide the user's interfaces, more GPIOs are required. 32 additional GPIOs are provided via four GPIO expanders.

Table 20: Required GPIOs

Function	Qty.	Remark
Disable/Enable Buck regulator	3	VCC12V, VCC3V3_PCIE, VCC1V5
SFP+ Module: XFI_TX_DISABLE	1	–
SFP+ Module: XFI_TX_FAULT	1	–
SFP+ Module: XFI_RX_LOS	1	–
SFP+ Module: XFI_MOD_DEF	1	–
SerDes Lane Mux	5	–
Selected DVDD [3]	1	–
PCIe PWR / DISABLE / WAKE#	3	–
LCD_BLT/PWR	2	–

3: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (4), Table 4-11, DVDD_VSEL.

3.4.25 JTAG Chain

The following components can be included in the JTAG chain by a placement option:

Table 21: JTAG chain

Interface	Device	I/O voltage
CPU	T1042 / 40 / 24 / 14	1.8 V
RGMII PHY1	TI DP83867	2.5 V
RGMII PHY2	TI DP83867	2.5 V
SGMII PHY1	TI DP83867	2.5 V
SGMII PHY2	TI DP83867	2.5 V
QSGMII PHY	Marvell 88E1545 / 48	2.5 V
PCIe x1 Slot	–	3.3 V

By default the JTAG connector is only connected to the CPU and uncoupled via resistor placement option.

3.5 Supply

3.5.1 Power requirements

The STKT104X can be supplied with 18 to 28 V DC. An 18 V DC power supply comes with the STKT104X.
For demanding applications, which make full usage of PCIe slots, a stronger power supply has to be used.

The following table shows the power consumption of STKT104X with a TQMT104x.

Table 22: Estimated full load power consumption

Voltage rail	Voltage	Current	Power
VCC5V	5.0 V	9.400 A	47 W
VCC5V_USB			
VCC3V3	3.3 V	7.629 A	25.176 W
VCC3V3_PCI			
VCC12V_PCI	12.0 V	0.5 A	6 W
VCC2V5	2.5 V	0.83 A	2.075 W
VCC1V8	1.8 V	0.837 A	1.507 W
VCC1V5_mPCI	1.5 V	0.75 A	1.125 W
VCC1V0	1.0 V	0.364 A	0.364 W
VCC1V1	1.1 V	0.413 A	0.454 W
Total I/O	–	–	5.525 W
I/O supply VCC3V3	3.3 V	2.093 A	6.907 W
Supply	24.0 V	3.939 A	94.536 W

Table 23: CPU I/O voltages

Voltage rail	Function	Possible voltages	Voltage set
OVDD	I/O voltage for MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply und JTAG, (+ eSDHC with T2081, Note: If used as an SDHC signal, pull up 10 kΩ to 100 kΩ to the respective I/O supply)	1.8 V, 3.3 V	1.8 V
O1VDD (T2081=OVDD)	I/O voltage for IRQ00 ~ IRQ05, Reset Signals, Debug, EVT0_B-EVT4_B, USBCLK	1.8 V, 3.3 V	1.8 V
DVDD	I/O voltage for DUART, I²C, DMA, TDM, QE, MPIC, DIU	1.8 V, 2.5 V, 3.3 V T2081: 1.8 V; 2.5 V T1042: DIU only 3.3 V T1042: TDM only 3.3 V T1024: DIU only 3.3 V T1024: TDM 2.5 V;3.3 V	3.3 V or 1.8 V Switchable + level shifting on TQMT104x and / or carrier board [4]
CVDD	I/O voltage for eSPI, SDHC_WP, SDHC_CD, SDHC_DAT[4:7]	1.8 V, 3.3 V T2081: 1.8 V; 2.5 V	SDHC_DAT[4:7] are used as SPI chip selects All SDHC modes with 1.8 V are not supported
EVDD (T2081=OVDD)	I/O voltage for eSDHC: SDHC_CLK SDHC_CMD SDHC_DAT[0:3]	1.8 V, 3.3 V T2081:OVDD=1.8 V	All SDHC modes with 1.8 V are not supported
LVDD	I/O voltage for Ethernet interface 2, 1588, GPIO	1.8 V, 2.5 V, 3.3 V (protocol dependent) (1.8 V or 2.5 V with T2081, T1024)	2.5 V
L1VDD (T2081=LVDD)	I/O voltage for Ethernet interface 1, Ethernet management interface 1 (EMI1), GPIO	1.8 V, 2.5 V, 3.3 V (protocol dependent) (1.8 V or 2.5 V with T1024)	2.5 V
USB_HVDD	All USB signals except: see USB_OVDD	3.3 V	3.3 V
USB_OVDD	USB1_UID, USB2_UID	1.8 V	1.8 V

4: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (4), Table 4-11, DVDD_VSEL.

3.5.2 Change of I/O voltages

On all TQMT104x the I/O voltages 1.8 V, 2.5 V and 3.3 V are routed switched and unswitched to the TQMT104x connectors.
Which voltage is switched to which bank, can be set according to the interface / functionality used on the carrier board.
DVDD has to be 1.8 V for the T2081 and 3.3 V for the T1042 or T1024, if the DIU is used.
The voltage can be set by a DIP switch. Changing the voltage may only be performed in the power-off state.
The DIP switch controls a MOSFET, which controls two anti-serial switched FETs.
The maximum current consumption on the DVDD rail is 56 mA.

- Voltage drop @ 4.5 V: $\Delta U = 14.5\ m\Omega * 56\ mA = 0.8\ mV \approx 0.02\ \%$
- Voltage drop @ 1.8 V: $\Delta U = 60\ m\Omega * 56\ mA = 3.36\ mV \approx 0.2\ \%$
- Voltage drop @ 3.3 V: $\Delta U = 90\ m\Omega * 56\ mA = 5.04\ mV \approx 0.15\ \%$
- Additional 0 Ω bridge:
  - With 50 mΩ: 2.8 mV ≈ 0.08 %
  - With 20 mΩ: 1.1 mV ≈ 0.03 %

Note: DVDD I/O voltage	
	The DVDD I/O voltage is set to 3.3 V by default. The RCW has to be adapted in case the DVDD I/O voltage is changed, i.e. to 1.8 V. See (4), Table 4-11, DVDD_VSEL.

3.5.3 Power supply concept

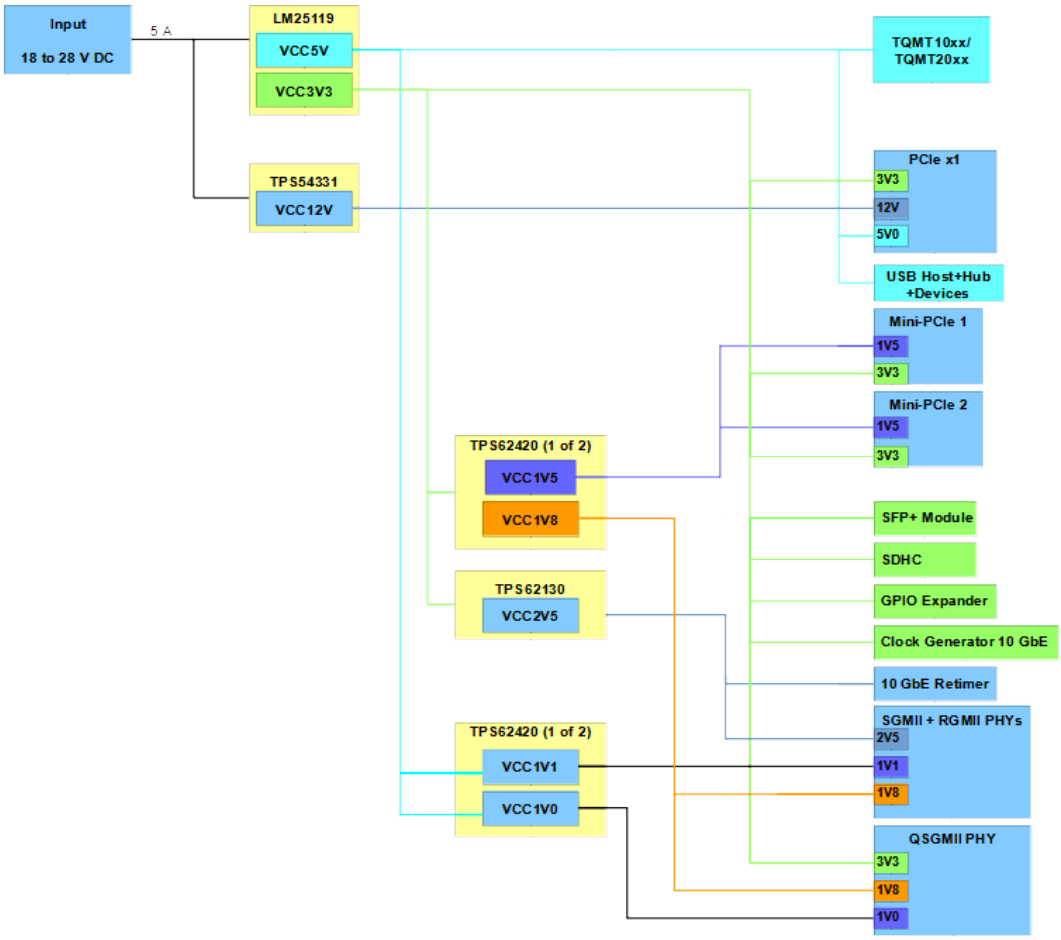

Figure 11: Block diagram power supply

A 1.0 V supply is only required with QSGMII.
The screw terminal connector X32 provided is insensitive to mechanical stress.
Alternatively the STKT104X can be supplied via the DC power jack X33.
A reverse polarity protection is provided on the STKT104X.
All voltage rails provide shunts for current measurement.
These shunts have a sufficiently low resistance to meet the voltage tolerances of the TQMT104x and other components.

- 5 V
  - CSNL1206FT3L00 SLE: 3 mΩ, 1 W, 1 %, 1206
  - 27 mV voltage drop with 9 A (0.243 W)

- 3.3 V
  - CSNL1206FT3L00 SLE: 3 mΩ, 1 W, 1 %, 1206
  - 27 mV voltage drop with 9 A (0.243 W)

- 2.5 V, 1.8 V, 1.5 V, 1.1 V, 1.0 V
  - PF0805FRM7W0R01L YAG: 10 mΩ, 0.25 W, 1 %, 0805

3.5.3.1 VCC5V

5 V and 3.3 V are generated with voltage regulators type LM25119.

3.5.3.2 VCC3V3

Dual regulator of VCC5V is used.

3.5.3.3 VCC12V

12 V are generated with a voltage regulator type TPS54331.

3.5.3.4 VCC2V5

2.5 V is generated with a voltage regulator type TPS62130.

3.5.3.5 VCC1V1, VCC1V5, VCC1V8

VCC1V1, VCC1V5, VCC1V8 are generated with voltages regulators type TPS62420-Q1.

3.5.3.6 VCC1V0

The TQMT2081 additionally requires 1.0 V.
This voltage is generated with a voltage regulator type NCP585HSN10T1G.

3.5.3.7 Shutdown of single voltages

All PCIe voltages (12 V, 3V3_PCIE, 1V5) can be switched off by the CPU via GPIOs. With VCC12V and VCC1V5 the shutdown is carried out by controlling the Enable pin of the respective buck regulator by a GPIO. 3V3_PCIE is separated from VCC3V3 via FETs. The GPIOs are provided by a GPIO expander.

3.5.4 Monitoring supply and reset generation

The voltages on the STKT104X are monitored by comparators, which compare the voltage to be monitored to a reference voltage. The comparators are supplied with VCC5V. If one monitored voltages drops below a defined threshold, this is signalled with an LED. If the threshold of VCC5V drops below the permitted value, #RESIN of the TQMT104x is pulled low and the TQMT104x is reset by that. The state of certain voltages is displayed via status LEDs (see 1.2.3.1).

Table 24: Voltage supervision

Nominal [V]	Permitted [V]	DC/DC [V]	Set threshold [V]	R1 (0.1 %)	R2 (0.1 %)	Actual threshold [V]
12.0	11.4 – 12.6	11.64 – 12.36	11.6	43 kΩ	2.4 kΩ	11.454 – 11.720
5.0	4.45 – 5.25	4.90 – 5.10	4.8	10 kΩ	1.5 kΩ	4.643 – 4.749
3.3	3.14 – 3.47	3.20 – 3.40	3.15	7.5 kΩ 11.5 kΩ	1.8 kΩ 2.74 kΩ	3.129 – 3.200 3.148 – 3.219
2.5	2.38 – 2.63	2.45 – 2.55	2.40	24 kΩ	8.2 kΩ	2.379 – 2.432
1.8	1.70 – 1.90	1.764 – 1.836	1.74	20 kΩ	11 kΩ	1.707 –1.745
1.5	1.425 – 1.575	1.470 – 1.530	1.45	15 kΩ	11 kΩ	1.436 – 1.460
1.2	1.14 – 1.26	1.176 – 1.224	1.16	13 kΩ	15 kΩ	1.143 – 1.165
1.1	1.045 – 1.155	1.078 – 1.122	1.06	11 kΩ	15 kΩ	1.051 – 1.073
1.0	0.95 – 1.05	0.98 – 1.02	0.96	6.8 kΩ	12 kΩ	0.950 – 0.969

Other reset sources are a debounced reset button, as well as another optional signal.

3.5.5 Status LEDs

Several LEDs are provided on the STKT104X to display the power supply status.

Table 25: Power supply status LEDs

Led	Voltage
V71	24 V
V40	12 V
V42	5 V
V39	3.3 V
V37	2.5 V
V35	1.8 V
V41	1.5 V
V36	1.1 V
V38	1.0 V

3.5.6 Power Sequencing

At first VCC5V is ramped up. The PHYs I/Os (3.3 V, 2.5 V, etc.) may only be powered when all supply voltages on the TQMT104x are successfully ramped up.

⇨ Enable signal "PGOOD" comes from the TQMT104x.

3.6 User's interfaces

3.6.1 Reset push button

A reset push button (S5) is provided on the STKT104X to bring back the STKT104X to a defined state at any time.
Further information can be found in 3.6.2.

3.6.2 Other push buttons

The STKT104X provides three more push buttons (S6, S7, and S8). The state of three of them can be read by an I²C I/O expander.

Figure 12: Other push buttons

Table 26: Other push buttons

Push button	I²C address	Remark
S5	–	Master Reset
S6	0x40 / 0100 0000b	D56, IO0
S7	0x40 / 0100 0000b	D56, IO1
S8	0x40 / 0100 0000b	D56, IO2

3.6.3 DIP switches

The STKT104X provides a DIP switch for user's inputs. Their state can be read by the I²C I/O Expander, like the user's buttons state. The DIP switches may only be operated when the STKT104X is switched off.

Table 27: DIP switches

Function	Qty.	Connected to
SerDes Switches	4	SerDes Switches und I/O Expander
DVDD (3.3 V or 1.8 V) [5]	1	FETs und I/O Expander
SerDes Clock PLL1 (125 MHz or 156.25 MHz)	1	Clock Generator
SerDes Clock PLL2 Spectrum Spreading	1	Clock Generator
Change-over DIU / TDM Bus	1	Bus switch und I/O Expander
RCW Source: SDHC	1	µC on TQMT104x
USB_CLK T1024 / T1042	1	Tristate Buffer
GPIOs	4	I/O Expander

Table 28: DIP switches assignment

DIP switch	Position	Function
S1-1	On	GPIO DIP 0 low
	Off	GPIO DIP 0 high
S1-2	On	GPIO DIP 1 low
	Off	GPIO DIP 1 high
S1-3	On	GPIO DIP 2 low
	Off	GPIO DIP 2 high
S1-4	On	XFI_ENSMB# low
	Off	XFI_ENSMB# high
S2-1	On	DIU – Display Interface
	Off	TDM Interface
S2-2	On	TBD – depends on system controller software on TQMT104x
	Off	TBD – depends on system controller software on TQMT104x
S2-3	On	T1024 USB Clock
	Off	T1042 USB Clock
S2-4	On	SerDes PLL1 clock = 156.25 MHz
	Off	SerDes PLL1 clock = 100 MHz
S3-1	On	Lane C: SGMII
	Off	Lane C: QSGMII
S3-2	On	Lane E: Mini PCIe
	Off	Lane E: Aurora
S3-3	On	Lane G: Mini PCIe
	Off	Lane G: SGMII or SATA
S3-4	On	Lane G: SGMII
	Off	Lane G: SATA
S4-1	On	DVDD=3.3 V (default)
	Off	DVDD=1.8 V [5]
S4-2	On	EVDD=3.3 V
	Off	EVDD=1.8 V
S4-3	On	CVDD=3.3 V
	Off	CVDD=1.8 V
S4-4	On	SDHC Boot
	Off	Other boot source

5: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (4), Table 4-11, DVDD_VSEL.

3.6.4 LEDs

Four red / green bicolour LEDs indicate the TQMT104x operating conditions. They are controlled by an I²C I/O expander. The states of RESIN#, PGOOD_STKT, PGOOD (TQMT104x) and from configurable GPIO expander I/Os are indicated.

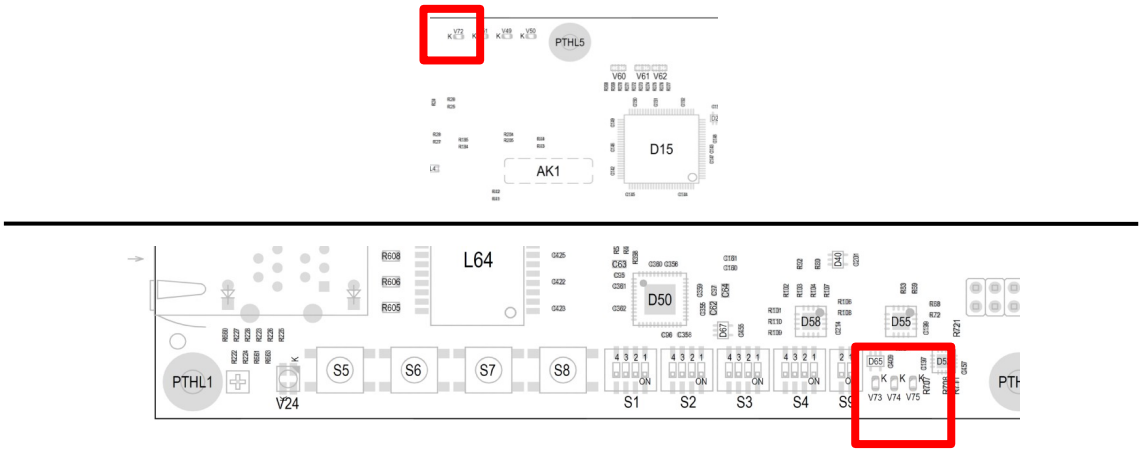

Figure 13: LEDs V72, V73, V74, V75

Table 29: LEDs V72, V73, V74, V75

Led	I²C address	Remark
V72	0x60 / 110 0000b	D59, LED1
V73	0x21 / 010 0001b	D55, IO7
V74	0x22 / 010 0010b	D58, IO6
V75	0x22 / 010 0010b	D58, IO7

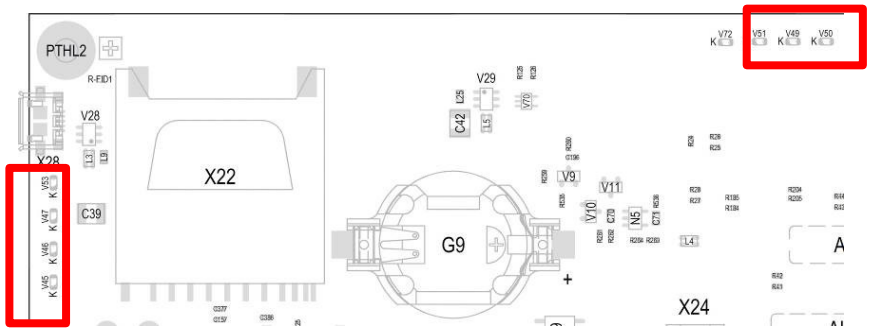

Figure 14: LEDs V45, V46, V47, V53 + V49, V50, V51

Table 30: LEDs V45, V46, V47, V53 + V49, V50, V51

LED	Function
V45	USB_H1
V46	USB_H2
V47	USB_H3
V53	USB_H4
V49	WWAN
V50	WLAN
V51	WPAN
V72	User
V73	User
V74	User
V75	User

3.6.5 Headers

The UART, I²C, SPI, TDM, UC, DIU interfaces and GPIOs are arranged in groups on 2.54 mm headers. The voltages VCC12V, VCC5V and VCC3V3 are also routed to these headers on the STKT104X.

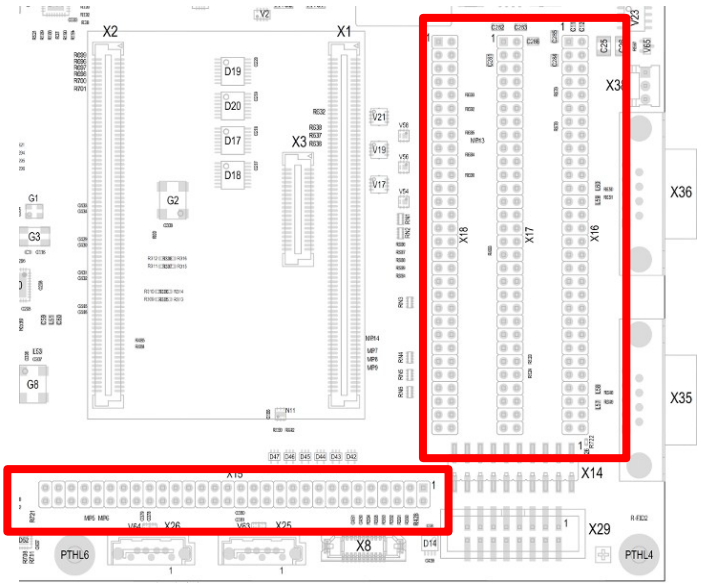

Figure 15: Header X15, X16, X17, X18

3.6.5 Headers (continued)

Table 31: Pinout X15

Signal	Pin		Signal
NC	1	2	NC
NC	3	4	NC
DGND	5	6	PWM_1
CLK09 / GPIO4_15 / BRGO2	7	8	DGND
DGND	9	10	GPIO_ADC_I2C1_1
CLK10 / GPIO4_22 / BRGO3	11	12	GPIO_ADC_I2C1_3
DGND	13	14	GPIO_ADC_I2C1_2
CLK11 / GPIO4_16 / BRGO4	15	16	NC
DGND	17	18	DGND
CLK12 / GPIO4_23 / BRGO1	19	20	EVT0#
DGND	21	22	EVT1#
TDMA_RQ / GPIO4_14 / UC1_CDB_RXER	23	24	EVT2#
TDMA_RSYNC / GPIO4_11 / UC1_CTSB_RXDV	25	26	EVT3#
TDMA_RXD / GPIO4_10 / UC1_RXD7	27	28	EVT4#
TDMA_TSYNC / GPIO4_13 / UC1_RTSB_TXEN	29	30	IRQ05#
TDMA_TXD / GPIO4_12 / UC1_TXD7	31	32	IRQ08# / GPIO1_28
DGND	33	34	DGND
TDMB_RQ / GPIO4_21 / UC3_CDB_RXER	35	36	NC
TDMB_RSYNC / GPIO4_18 / UC3_CTSB_RXDV	37	38	NC
TDMB_RXD / GPIO4_17 / UC3_RXD7	39	40	IRQ01#
TDMB_TSYNC / GPIO4_20 / UC3_RTSB_TXEN	41	42	NC
TDMB_TXD / GPIO4_19 / UC3_TXD7	43	44	DGND
DGND	45	46	SGMII_PHY_GPIO1
EC1_RX_ER	47	48	SGMII_PHY_GPIO2
EC1_TX_ER	49	50	DGND
EC1_COL	51	52	SGMII_PHY2_GPIO1
NC	53	54	SGMII_PHY2_GPIO2
NC	55	56	EC2_PHY_GPIO1
NC	57	58	EC2_PHY_GPIO2
DGND	59	60	DGND

3.6.5 Headers (continued)

Table 32: Pinout X16

Signal	Pin		Signal
VCC12V	1	2	DGND
VCC5V	3	4	DGND
DGND	5	6	NC
TEMP_CRIT_MOD#	7	8	NC
RTC	9	10	NC
RES / LP_TMP_DETECT#	11	12	TMP_DETECT#
RTC_INT_MOD#	13	14	DGND
SCAN_MODE#	15	16	RTC_CLKOUT
DGND	17	18	NC
NC	19	20	NC
CLKOE	21	22	NC
DGND	23	24	DGND
TEST_SEL#	25	26	UART2_SIN#
ASLEEP	27	28	UART2_SOUT#
STAT1	29	30	UART3_SOUT# / UART1_RTS#
STAT0 / PGOOD	31	32	UART3_SIN# / UART1_CTS#
DGND	33	34	UART4_SOUT# / UART2_RTS#
DMA1_DREQ#	35	36	UART4_SIN# / UART2_CTS#
DMA1_DACK#	37	38	UART1_SIN#
DMA1_DDONE#	39	40	UART1_SOUT#
DMA2_DREQ0#	41	42	DGND
DMA2_DACK0#	43	44	HRESET#
DMA2_DDONE0#	45	46	PROG_SFP
TSEC_1588_ALARM_OUT1	47	48	PORESET#
TSEC_1588_ALARM_OUT2	49	50	RESIN#
IRQ_OUT#	51	52	RESET_REQ_OUT#
TSEC_1588_CLK_IN	53	54	NC
NC	55	56	USB1_DRVVBUS
NC	57	58	USB1_PWRFAULT [6]
DGND	59	60	DGND

6: 10 kΩ PU to VCC3V3.

3.6.5 Headers (continued)

Table 33: Pinout X17

Signal	Pin		Pin	Signal
VCC12V	1		2	VCC3V3_PCIE
VCC5V	3		4	VCC3V3_PCIE
DGND	5		6	DGND
NC	7		8	NC
NC	9		10	NC
NC	11		12	NC
NC	13		14	NC
NC	15		16	SPI_MISO
NC	17		18	SPI_MOSI
NC	19		20	SPI_CS0# / SDHC_DAT4
IIC4_SCL / GPIO4_02 / EVT5_B	21		22	SPI_CS1# / SDHC_DAT5
IIC4_SDA / GPIO4_03 / EVT6_B	23		24	SPI_CS2# / SDHC_DAT6
NC	25		26	SPI_CS3# / SDHC_DAT7
NC	27		28	DGND
IIC3_SCL	29		30	SPI_CLK
IIC3_SDA	31		32	DGND
IIC2_SCL	33		34	NC
IIC2_SDA	35		36	NC
DGND	37		38	NC
IIC1_SCL_SPV	39		40	DGND
IIC1_SDA_SPV	41		42	NC
NC	43		44	NC
NC	45		46	NC
EXT_TOUCH_INT#	47		48	DGND
LCD_PWR_EN	49		50	LCD_BLT_EN
STKT_RST#	51		52	PWM_0
DGND	53		54	DGND
TOUCH_Y+	55		56	TOUCH_X+
TOUCH_Y–	57		58	TOUCH_X–
DGND	59		60	DGND

3.6.5 Headers (continued)

Table 34: Pinout X18

Signal	Pin		Pin	Signal
IFC_AD00	1		2	IFC_AVD
IFC_AD01	3		4	IFC_BCTL
IFC_AD02	5		6	IFC_TE
IFC_AD03	7		8	DGND
IFC_AD04	9		10	IFC_CS0# / CS_NOR#
IFC_AD05	11		12	IFC_WP0#
IFC_AD06	13		14	IFC_RB0#
IFC_AD07	15		16	IFC_WE0#
IFC_AD08	17		18	IFC_OE#
IFC_PERR#	19		20	IFC_CLE
IFC_AD14	21		22	IFC_CLK0
IFC_AD15	23		24	IFC_RB1#
IFC_NDDDR_CLK	25		26	IFC_CLK1
DGND	27		28	IFC_NDDQS
IFC_AD09	29		30	DGND
IFC_AD10	31		32	IFC_CS3#
IFC_AD11	33		34	IFC_AD12
IFC_CS2#	35		36	IFC_RB1#
IFC_CS1#	37		38	IFC_AD13
IFC_CS4#	39		40	IFC_A16
IFC_CS5#	41		42	IFC_A17
IFC_CS6#	43		44	IFC_A18
IFC_CS7#	45		46	IFC_A19
IFC_PAR0	47		48	IFC_A20
IFC_PAR1	49		50	IFC_A21
IFC_A23	51		52	IFC_A22
IFC_A25	53		54	IFC_A24
IFC_A27	55		56	IFC_A26
IFC_A29	57		58	IFC_A28
IFC_A31	59		60	IFC_A30

3.6.6 Ethernet LEDs

LEDs for the Ethernet interfaces are integrated in the RJ45 jacks.

3.6.7 Pin assignment TQMT104x connectors

The following tables show the interface to the TQMT104x.

Table 35: Pinout connector X1 (X1 on TQMT104X)

CPU ball	Dir.	Signal	Pin		Signal	Dir.	CPU ball
	P/I	VIN	1	2	VIN	P/I	
	P/I	VIN	3	4	VIN	P/I	
	P/I	VIN	5	6	VIN	P/I	
	P/I	VIN	7	8	VIN	P/I	
	P/I	VIN	9	10	VIN	P/I	
	P/I	VIN	11	12	VIN	P/I	
	P/I	VIN	13	14	VIN	P/I	
	P/I	VIN	15	16	VBAT	P/I	
	P/O	VDD	17	18	VDDC	P/O	
	P/O	VDD	19	20	VDDC	P/O	
	P/I	USB_SVDD_IN	21	22	USB_SVDD_IN	P/I	
	P/O	VCC1V8	23	24	VCC1V8	P/O	
	P/O	VCC1V8	25	26	USB_OVDD_IN	P/I	
	P/O	VCC1V8S	27	28	USB_HVDD_IN	P/I	
	P/O	VCC1V8S	29	30	VCC3V3F	P/O	
	P/O	VCC1V8S	31	32	EVDD	P/I	
	P/O	VCC1V8S	33	34	CVDD	P/I	
	P/O	VCC3V3S	35	36	DVDD [7]	P/I	
	P/I	LVDD	37	38	LVDD	P/I	
	P/I	L1VDD	39	40	L1VDD	P/I	
	P/O	VCC2V5S	41	42	VCC2V5	P/O	
	P/O	VCC2V5S	43	44	VCC2V5	P/O	
	P / I/O	TVDD	45	46	CLK09	I	P4
	P	DGND	47	48	CLK10	I	P3
F8	I	USBCLK	49	50	CLK11	I	N4
F1	I/O	USB1_UDP	51	52	CLK12	I	M4
F2	I/O	USB1_UDM	53	54	TDMB_RQ	O	R4
F4	I	USB1_UID	55	56	TDMB_TSYNC	I	R3
F5	I	USB1_PWRFAULT	57	58	TDMB_RSYNC	I	T3
E4	I	USB1_VBUSCLMP	59	60	TDMB_RXD	I	U4
F6	O	USB1_DRVVBUS	61	62	TDMB_TXD	O	T4
	P	DGND	63	64	TDMA_RQ	O	R2
H1	I/O	USB2_UDP	65	66	TDMA_TSYNC	I	R1
H2	I/O	USB2_UDM	67	68	TDMA_RSYNC	I	U1
H4	I	USB2_UID	69	70	DGND	P	
H5	I	USB2_PWRFAULT	71	72	TDMA_RXD	I	U2
J4	I	USB2_VBUSCLMP	73	74	TDMA_TXD	O	T1
J5	O	USB2_DRVVBUS	75	76	SWD_DIO	I/O	
A4	I/O	IFC_AD0	77	78	SWD_CLK	I	
A5	I/O	IFC_AD2	79	80	IFC_AD1	I/O	B5

7: DVDD I/O voltage is set to 3.3 V by default. RCW has to be adapted if DVDD I/O voltage is set to 1.8 V. See (4), Table 4-11, DVDD_VSEL.

3.6.7 Pin assignment TQMT104x connectors (continued)

Table 35: Pinout connector X1 (X1 on TQMT104X) (continued)

CPU ball	Dir.	Signal	Pin		Signal	Dir.	CPU ball
A6	I/O	IFC_AD4	81	82	IFC_AD3	I/O	B6
B8	I/O	IFC_AD6	83	84	IFC_AD5	I/O	A7
	P	DGND	85	86	IFC_AD7	I/O	A8
C6	O	IFC_A17	87	88	IFC_A16	O	C5
C7	O	IFC_A19	89	90	IFC_A18	O	D7
C8	O	IFC_A21	91	92	IFC_A20	O	D8
D9	O	IFC_A22	93	94	DGND	P	
D10	O	IFC_A24	95	96	IFC_A23	O	C9
E11	O	IFC_A26	97	98	IFC_A25	O	C10
D11	O	IFC_A28	99	100	IFC_A27	O	C11
D12	O	IFC_A30	101	102	IFC_A29	O	C12
	P	DGND	103	104	IFC_A31	O	E12
D17	O	IFC_AVD	105	106	IFC_CS1#	O	E15
B14	O	IFC_TE	107	108	IFC_CS2#	O	D16
D13	O	IFC_WE0#	109	110	IFC_CS3#	O	C16
D15	O	IFC_OE#	111	112	DGND	P	
A14	O	IFC_BCTL	113	114	IFC_CLE	O	F16
G8	I	TEST_SEL#	115	116	TCK	I	E18
B2	O	ASLEEP	117	118	TMS	I	B18
	O	STAT1	119	120	TDO	O	C18
	O	STAT0/PGOOD	121	122	TDI	I	A18
P5	I	DMA1_DREQ0#	123	124	TRST#	I	D19
U5	O	DMA1_DACK0#	125	126	IRQ00#	I	F7
R5	O	DMA1_DDONE0#	127	128	IRQ01#	I	D3
V5	I	DMA2_DREQ0#	129	130	IRQ02#	I	E9
AA5	O	DMA2_DACK0#	131	132	IRQ03#	I	D1
Y5	O	DMA2_DDONE0#	133	134	IRQ04#	I	D4
	P	DGND	135	136	CLK_OUT	O	E6
D5	I	IRQ05#	137	138	DGND	P	
AB4	I	IRQ06#	139	140	SYSCLK	O	
AD5	I	IRQ07#	141	142	DDRCLK	O	
AB1	I	IRQ08#	143	144	DGND	P	
AC5	I	IRQ09#	145	146	RTC	I	B17
L4	I	IRQ10#	147	148	VDD_LP	I	P6
U3	I	IRQ11#	149	150	NC	–	
A3	O	IRQ_OUT# / EVT9#	151	152	DGND	P	
E8	O	HRESET#	153	154	SDHC_EXT_SEL#	I	
F12	O	PROG_SFP	155	156	RCW_SRC_SEL	I	
F13	O	PORESET#	157	158	RESET_REQ_OUT#	I/O	
	I	RESIN#	159	160	RESET_OUT#	O	

3.6.7 Pin assignment TQMT104x connectors (continued)

Table 36: Pinout connector X2 (X2 on TQMT104X)

CPU ball	Dir.	Signal	Pin		Signal	Dir.	CPU ball
P1	I	SPI_MISO	1	2	SDHC_DAT0_MOD	I/O	
P2	O	SPI_MOSI	3	4	SDHC_DAT1_MOD	I/O	
N1	O	SPI_CLK	5	6	DGND	P	
M1	O	SPI_CS0# / SDHC_DAT4	7	8	SDHC_DAT2_MOD	I/O	
M2	O	SPI_CS1# / SDHC_DAT5	9	10	SDHC_DAT3_MOD	I/O	
M3	O	SPI_CS2# / SDHC_DAT6	11	12	SDHC_CMD_MOD	I/O	
N3	O	SPI_CS3# / SDHC_DAT7	13	14	DGND	P	
L5	I	SDHC_CD#	15	16	SDHC_CLK_MOD	I/O	
M5	I	SDHC_WP	17	18	EMI1_MDC	O	AH3
AB6	I	TSEC_1588_TRIG_IN1	19	20	EMI1_MDIO	I/O	AH4
AE6	O	TSEC_1588_PULSE_OUT1	21	22	TSEC_1588_CLK_IN	I	AC8
AF5	O	TSEC_1588_ALARM_OUT1	23	24	TSEC_1588_CLK_OUT	O	AD7
	P	DGND	25	26	TSEC_1588_TRIG_IN2	I	AE5
AF2	I	EC1_RXD0	27	28	TSEC_1588_PULSE_OUT2	O	AD8
AF1	I	EC1_RXD1	29	30	TSEC_1588_ALARM_OUT2	O	AC7
AE1	I	EC1_RXD2	31	32	EC2_RXD0	I	AH8
AD2	I	EC1_RXD3	33	34	EC2_RXD1	I	AG7
AC2	I/O	EC1_RX_ER	35	36	EC2_RXD2	I	AH7
AG2	I	EC1_RX_CTL	37	38	DGND	P	
AD1	I	EC1_RX_CLK	39	40	EC2_RXD3	I	AH6
	P	DGND	41	42	EC2_RX_CTL	I	AG8
AE3	O	EC1_TXD0	43	44	EC2_RX_CLK	I	AH5
AE4	O	EC1_TXD1	45	46	EC2_TXD0	O	AE7
AD3	O	EC1_TXD2	47	48	EC2_TXD1	O	AF7
AC3	O	EC1_TXD3	49	50	EC2_TXD2	O	AF6
AC4	I/O	EC1_TX_ER	51	52	EC2_TXD3	O	AG5
AF4	O	EC1_TX_CTL	53	54	DGND	P	
	P	DGND	55	56	EC2_TX_CTL	O	AF8
AC1	I/O	EC1_COL	57	58	EC2_GTX_CLK	O	AE8
AF3	O	EC1_GTX_CLK	59	60	EC2_GTX_CLK125	I	AC6
AG3	I	EC1_GTX_CLK125	61	62	DGND	P	
	P	DGND	63	64	SD1_TX0_P	O	AD10
	P	DGND	65	66	SD1_TX0_N	O	AE10
AH10	I	SD1_RX0_P	67	68	DGND	P	
AG10	I	SD1_RX0_N	69	70	DGND	P	
	P	DGND	71	72	SD1_TX1_P	O	AD11
	P	DGND	73	74	SD1_TX1_N	O	AE11
AH11	I	SD1_RX1_P	75	76	DGND	P	
AG11	I	SD1_RX1_N	77	78	DGND	P	
	P	DGND	79	80	SD1_TX2_P	O	AD13

3.6.7 Pin assignment TQMT104x connectors (continued)

Table 36: Pinout connector X2 (X2 on TQMT104X) (continued)

CPU ball	Dir.	Signal	Pin		Signal	Dir.	CPU ball
	P	DGND	81	82	SD1_TX2_N	O	AE13
AH13	I	SD1_RX2_P	83	84	DGND	P	
AG13	I	SD1_RX2_N	85	86	DGND	P	
	P	DGND	87	88	SD1_TX3_P	O	AD14
	P	DGND	89	90	SD1_TX3_N	O	AE14
AH14	I	SD1_RX3_P	91	92	DGND	P	
AG14	I	SD1_RX3_N	93	94	DGND	P	
	P	DGND	95	96	SD1_TX4_P	O	AD16
	P	DGND	97	98	SD1_TX4_N	O	AE16
AH16	I	SD1_RX4_P	99	100	DGND	P	
AG16	I	SD1_RX4_N	101	102	DGND	P	
	P	DGND	103	104	SD1_TX5_P	O	AD17
	P	DGND	105	106	SD1_TX5_N	O	AE17
AH17	I	SD1_RX5_P	107	108	DGND	P	
AG17	I	SD1_RX5_N	109	110	DGND	P	
	P	DGND	111	112	SD1_TX6_P	O	AD19
	P	DGND	113	114	SD1_TX6_N	O	AE19
AH19	I	SD1_RX6_P	115	116	DGND	P	
AG19	I	SD1_RX6_N	117	118	DGND	P	
	P	DGND	119	120	SD1_TX7_P	O	AD20
	P	DGND	121	122	SD1_TX7_N	O	AE20
AH20	I	SD1_RX7_P	123	124	DGND	P	
AG20	I	SD1_RX7_N	125	126	DGND	P	
	P	DGND	127	128	SD1_REF_CLK1_P	I	AB14
	P	DGND	129	130	SD1_REF_CLK1_N	I	AA14
AB18	I	SD1_REF_CLK2_P	131	132	DGND	P	
AA18	I	SD1_REF_CLK2_N	133	134	DGND	P	
	P	DGND	135	136	IIC1_SCL_SPV	I/O	
V2	I/O	IIC3_SCL	137	138	IIC1_SDA_SPV	I/O	
W3	I/O	IIC3_SDA	139	140	IIC2_SCL	I/O	V3
AA3	I/O	IIC4_SCL	141	142	IIC2_SDA	I/O	Y3
AB3	I/O	IIC4_SDA	143	144	RES / EMI2_MDC	O	
	P	DGND	145	146	RES / EMI2_MDIO	I/O	
	I	CLKOE	147	148	UART1_SIN#	I	AA1
W4	I	UART2_SIN#	149	150	UART1_SOUT#	O	AA2
AA4	O	UART2_SOUT#	151	152	DGND	P	
Y1	O	UART3_SOUT# / UART1_RTS#	153	154	SOUT1	O	
Y2	I	UART3_SIN# / UART1_CTS#	155	156	SOUT2	O	
V4	O	UART4_SOUT# / UART2_RTS#	157	158	SIN1	I	
Y4	I	UART4_SIN# / UART2_CTS#	159	160	SIN2	I	

3.6.7 Pin assignment TQMT104x connectors (continued)

Table 37: Pinout connector X3 (X3 on TQMT104X)

CPU ball	Dir.	Signal	Pin		Signal	Dir.	CPU ball
F9	I	SCAN_MODE#	1	2	EVT4#	I/O	C3
F18	O	CKSTP_OUT#	3	4	EVT3#	I/O	C2
F19	I	TMP_DETECT#	5	6	EVT2#	I/O	C1
R6	I	RES / LP_TMP_DETECT#	7	8	EVT1#	I/O	C4
	O	RTC_CLKOUT	9	10	EVT0#	I/O	D6
	I/O	RTC_INT_OUT#	11	12	DGND	P	
	I/O	TEMP_CRIT_MOD#	13	14	IFC_AD15	I/O	A13
C14	I/O	IFC_PAR1	15	16	IFC_AD14	I/O	A12
C15	I/O	IFC_PAR0	17	18	IFC_AD13	I/O	B12
	P	DGND	19	20	IFC_AD12	I/O	A11
E14	I	IFC_PERR#	21	22	IFC_AD11	I/O	B11
F17	O	IFC_WP0#	23	24	IFC_AD10	I/O	A10
A15	I	IFC_RB1#	25	26	IFC_AD9	I/O	A9
B15	I	IFC_RB0#	27	28	IFC_AD8	I/O	B9
A16	I/O	IFC_NDDQS	29	30	DGND	P	
D14	O	IFC_NDDDR_CLK	31	32	IFC_CS7#	O	C19
	P	DGND	33	34	IFC_CS6#	O	D18
A19	O	IFC_CLK1	35	36	IFC_CS5#	O	C17
A17	O	IFC_CLK0	37	38	IFC_CS4#	O	E17
	P	DGND	39	40	IFC_CS0# / CS_NOR#	O	C13

4. MECHANICS

4.1 Design

The STKT104X is designed for laboratory usage.

To avoid damage caused by mechanical stress, the TQMT104x may only be extracted from the carrier board by using the extraction tool MOZIP2020 that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMT104x for the extraction tool MOZIP2020.

A free stack height must be kept under the TQMT104x.

The overall dimensions of the STKT104X are 230 mm × 170 mm.

Hexagonal bolts M3 × 12 are mounted at the STKT104X PCB as spacers.

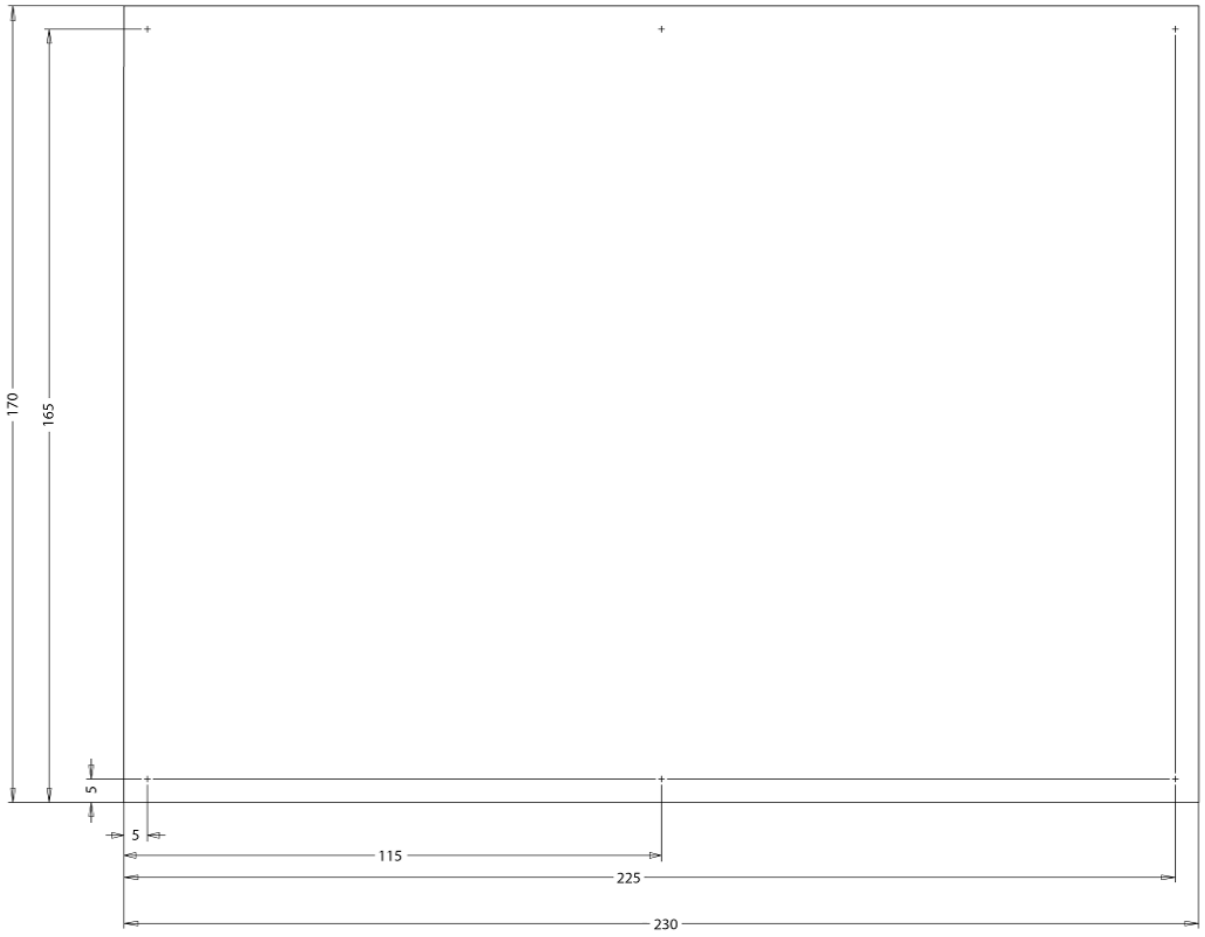

Figure 16: Dimensions of STKT104X

4.2 Thermal management

The cooling solution for the TQMT104x has following characteristics:

- Under laboratory conditions quietly, in particular with low power dissipation / use with TQMT1042
- Sufficient cooling in the climate chamber with TQMT2081 with +85 °C
- Excellent mechanical stability
- Flexibility / possibility to adapt to other installation situations

Attention: Destruction or malfunction, TQMT104x heat dissipation	
	The TQMT104x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the T104x must be taken into consideration when connecting the heat sink. The T104x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMT104x and thus malfunction, deterioration or destruction.

In case the heat sink was removed from the TQMT104x and has to be mounted again, extreme care has to be taken to achieve optimal thermal connection between the CPU and the heat sink.

This can be achieved by using e.g. Phase Change Material Chomerics THERMFLOW® T725.

4.3 Power supply

The STKT104X supply voltage range is 18 V to 28 V DC.
A suitable table top power supply (TR70A18-01A03 IPC, 18 V; 3.9 A) is included in the delivery of the STKT104X.
This, or a comparable CE certified, protective isolated DC power supply can be connected at the 2-pin Phoenix connector X32.

The following illustration shows the position of the power supply connectors X32 and X33 on the STKT104X:

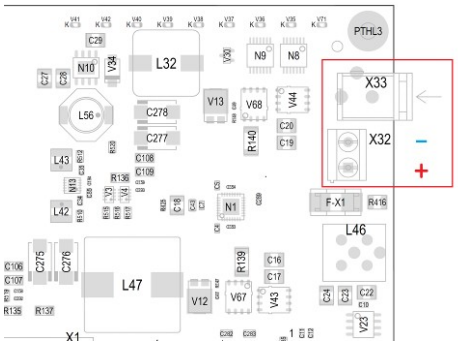

Figure 17: Position of power supply connectors

Table 38: Pinout of power supply connector X32

Pin	Signal name	Remark
1	VIN	18 V to 28 V DC
2	GND	Ground

Alternatively a power supply can also be connected at X33.

Table 39: Pinout of DC power jack X33

Pin	Signal name	Remark
1	VIN	18 V to 28 V DC
2	GND	Ground
3	NC	Not connected

An external power supply (laboratory power supply, alternative table top power supply) should be able to supply at least 3.9 A, like the provided table top power supply TR70A18.
Details about the current consumption can be taken from Table 22.

The following protection circuits exist at the supply input:

- Input filter
- Protection against reverse polarity

5. SOFTWARE

Information can be found in the Support Wiki for the TQMT1042.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC characteristics

The STKT104X is operated as a development platform with TQMT104x without housing.
The EMC behaviour is not taken into consideration.

6.2 Operational safety and personal security

Due to the occurring voltages (≤28 V DC), and its use as a development platform, tests with respect to the operational and personal safety have not been carried out.

7. CLIMATIC AND OPERATIONAL CONDITIONS

Table 40: Climate and operational conditions

Parameter	Range	Remark
Storage temperature	–40 °C to +85 °C	Or according to the specification of the respective component
Operating temperature	–40 °C to +85 °C	Not designed for permanent usage @ +85 °C
Case temperature	0 °C to +70 °C	Or according to the specification of the respective component
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

7.1 Reliability and service life

The STKT104X serves as a development platform. It is designed to be insensitive to vibration and impact.
The components used were in principle selected for the commercial temperature range.
Further considerations with regard to climate and operating conditions were not made.
High quality industrial grade connectors are assembled on the STKT104X.

7.2 Protection against external effects

The STKT104X is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

8. ENVIRONMENT PROTECTION

8.1 RoHS

The STKT104X is manufactured RoHS compliant.

- All components used and assemblies are RoHS compliant
- RoHS compliant soldering processes are used

8.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of technical possibilities, the STKT104X was designed to be recyclable and easy to repair.

8.3 REACH®

The EU chemicals regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, authorization and restriction of SVHC substances (substances of very high concern, e.g. carcinogenic, mutagenic and/or persistent, bioaccumulative and toxic). It applies to all SVHC substances placed on the market in quantities of more than 1 t per year per manufacturer or importer.
No control over REACH beyond the RoHS test was conducted.

8.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The STKT104X must therefore always be seen in conjunction with the complete device.

8.5 Packaging

The STKT104X is delivered in reusable packaging.

8.6 Batteries

8.6.1 General notes

Due to technical reasons a battery is necessary for the STKT104X. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used. If this is unavoidable for technical reasons, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

8.6.2 Lithium batteries

The requirements concerning special provision 188 of ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams
  (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.
- During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

8.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the STKT104X, it is produced in such a way, that it can be easily repaired and disassembled.
The energy consumption of the STKT104X is minimized by suitable measures.
Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as information. Tests or certifications were not carried out with respect to this.

9. APPENDIX

9.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 41: Acronyms

Acronym	Meaning
COP	Common On-chip Processor
DIU	Display Interface Unit
eMMC	embedded Multimedia Card
eSPI	enhanced Serial Peripheral Interface
EuP	Energy using Products
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
IFC	Integrated Flash-Controller
JTAG®	Joint Test Action Group
LDI	LVDS Display Interface
LDO	Low Drop-Out
LVDS	Low-Voltage Differential Signalling
MMC	Multimedia Card
NC	Not Connected
NP	Not Placed
OTG	On-The-Go
PCIe	PCI Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (interface)
REACH®	Registration, Evaluation, Authorization (and restriction of) Chemicals
RoHS	Restriction of (the use of certain) Hazardous Substances
SATA	Serial Advanced Technology Attachment
SDXC	Secure Digital eXtended Capacity
SPI	Serial Peripheral Interface
TBD	To Be Determined
TDM	Time-Division Multiplexing
UART	Universal Asynchronous Receiver/Transmitter
UC	Universal Controller
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment

9.2 References

Table 42: Further applicable documents

No.	Name	Rev., Date	Company
(1)	QorIQ® T Series T1020 / 22 and T1040 / 42 Processors - Fact Sheet	Rev. 1, 04/2014	NXP
(2)	QorIQ® T1040, T1020 Data Sheet	Rev. 2, 06/2015	NXP
(3)	QUICC Engine® Block Reference Manual with Protocol Interworking	Rev. 8, 05/2016	NXP
(4)	QorIQ® T1040 Reference Manual	Rev. 1, 08/2015	NXP
(5)	e5500RM, e5500 Core Reference Manual	Rev. 4, 07/2015	NXP
(6)	TQMT104x User's Manual	– current –	TQ-Systems
(7)	TQMT1040 / TQMT1042 Support-Wiki	– current –	TQ-Systems

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Technology in Quality