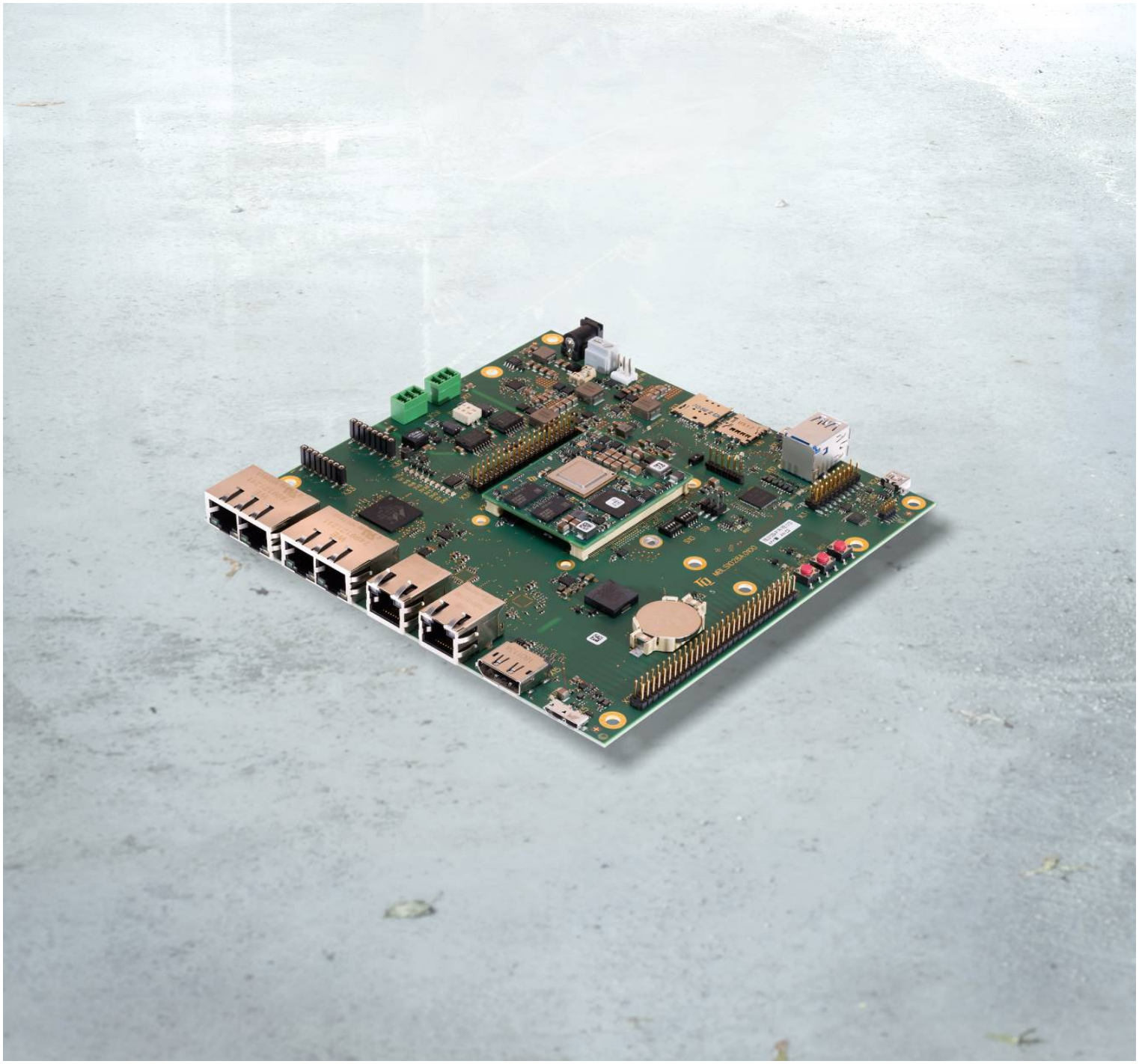
MBLS1028A
User's Manual

MBLS1028A UM 0100
03.11.2020



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REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	03.11.2020	Petz		First edition

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is: do not touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the MBLS1028A and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation. These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBLS1028A circuit diagram
- TQMLS1028A User's Manual
- LS1028A Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMLS1028A

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the MBLS1028A revision 0100.

The MBLS1028A is designed as a carrier board for the TQMLS1028A.

All TQMLS1028A interfaces, which can be used, are available on the MBLS1028A, thus the features of the CPU LS1028A can be evaluated and software development for a TQMLS1028A-based project can be started directly.

The MBLS1028A supports TQMLS1028A modules with an LS1017A, LS1027A, LS1018A or LS1028A CPU.

3. TECHNICAL DATA

3.1 System architecture and functionality

3.1.1 Block diagram MBLS1028A

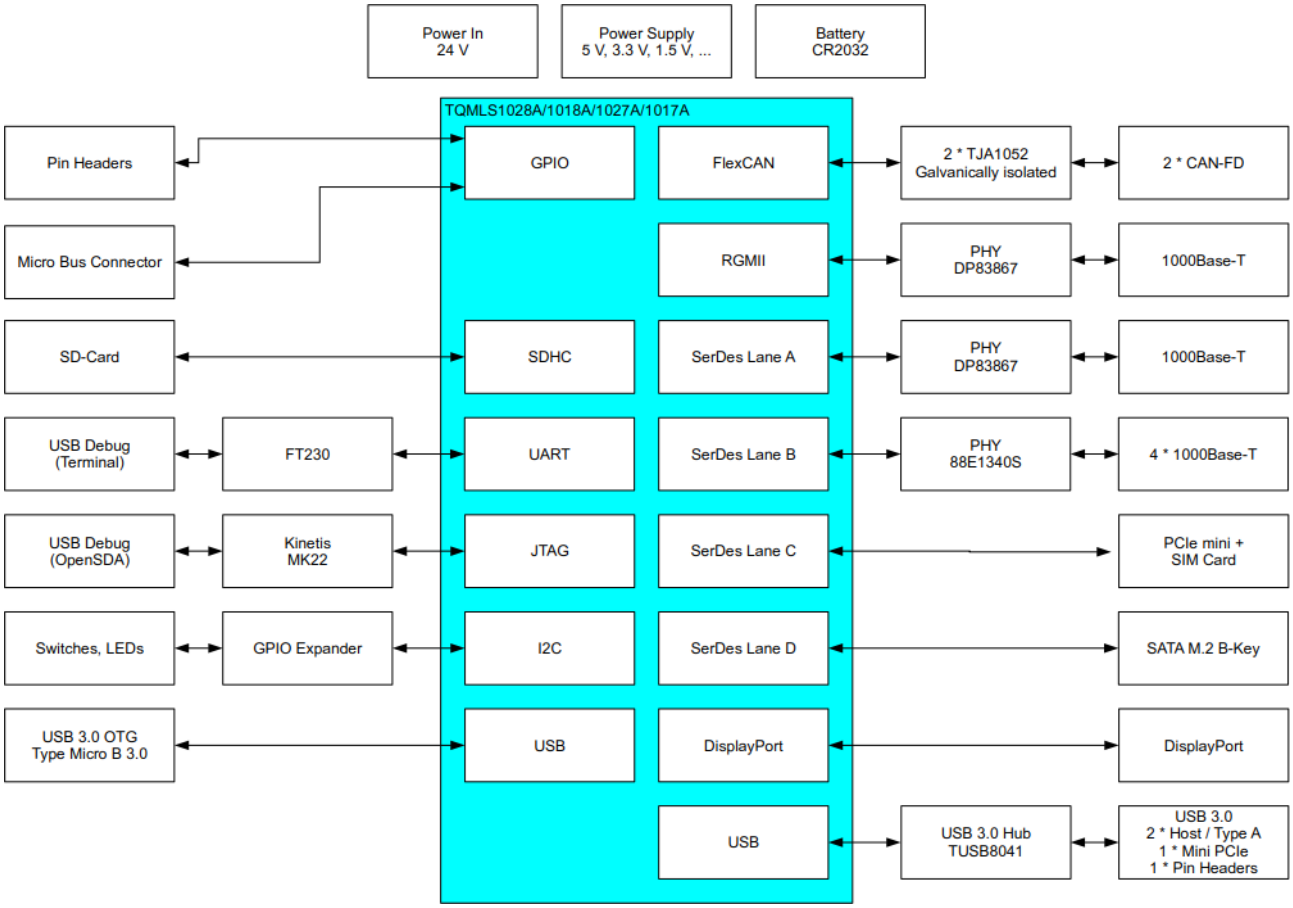

Figure 1: Block diagram MBLS1028A

4. ELECTRONICS

The TQMLS1028A with its LS1028A CPU is the central system component. It provides DDR4 SDRAM, eMMC, NOR flash and EEPROM memory. All voltages required by the TQMLS1028A are derived from the supply voltage of 5 V.

The boot behaviour of the TQMLS1028A can be customised. The required boot-mode configuration can be set with DIP switches on the MBLS1028A, see chapter 4.1.1.3.

4.1 System components

4.1.1 TQMLS1028A

The TQMLS1028A with its LS1028A CPU is the central system component. It provides DDR4 SDRAM, eMMC, NOR flash and an EEPROM. All TQMLS1028A internal voltages are derived from the 5 V supply voltage. Further information can be found in the TQMLS1028A User's Manual. The available signals are routed to the MBLS1028A via two connectors. On the MBLS1028A the interfaces provided by the TQMLS1028A are routed to industry standard connectors. Furthermore the MBLS1028A provides all power supplies and configurations required for the operation of the TQMLS1028A. The MBLS1028A supports TQMLS1028A modules with an LS1017A, LS1027A, LS1018A or LS1028A CPU.

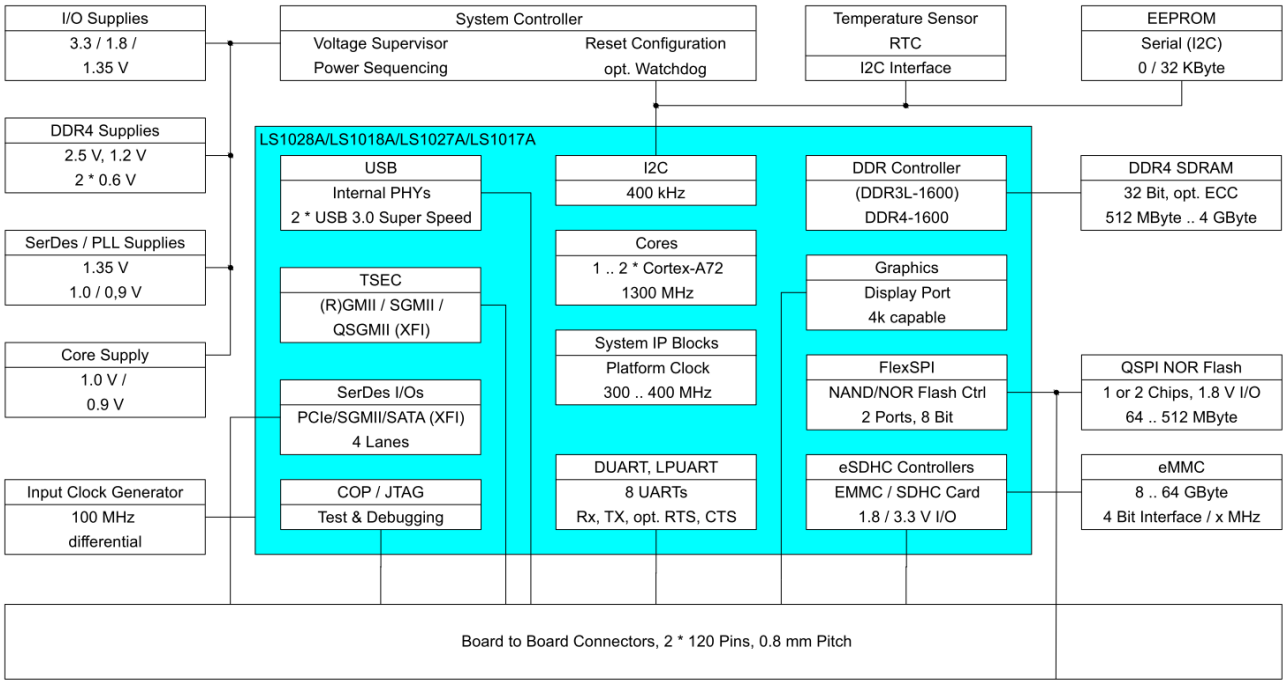

Figure 2: Block diagram TQMLS1028A

4.1.1.1 TQMLS1028A pinout

All available TQMLS1028A signals are routed to two connectors on the MBLS1028A.
More detailed information is to be taken from the TQMLS1028A User's Manual (4).

Note: Available interfaces	
	Depending on the TQMLS1028A derivative not all interfaces are available. Refer to the TQMLS1028A User's Manual and the TQMLS1028A pinout table to see which interfaces are available.

4.1.1.2 TQMLS1028A connectors

The MBLS1028A is connected to the carrier board with 240 pins on two connectors.
The following table shows details of the connectors assembled on the MBLS1028A:

Table 2: Connectors assembled on MBLS1028A

Manufacturer	Part number	Remark
TE connectivity	5177986-5	• 120 pin, 0.8 mm pitch • Plating: Gold 0.2 µm • –40 °C to +125 °C

The TQMLS1028A is held in the mating connectors on the TQMLS1028A by 240 pins with a retention force of approximately 24 N.
To avoid damaging the connectors of the MBLS1028A or the TQMLS1028A while removing the TQMLS1028A, the use of the extraction tool MOZI8XX is strongly recommended.

4.1.1.3 Boot configuration

The boot mode of the TQMLS1028A is determined by the level of the analogue 3.3 V signal RCW_SRC_SEL.
The boot mode defines the boot device and specific configurations. The boot mode is set with DIP switches.
The following table shows the permitted Boot Mode settings:

Table 3: Boot Mode configuration, DIP switch S9

Boot Mode	S9-1~2	S9-3~4	S9-5~6	S9-7~8	RCW_SRC_SEL (3.3 V)
SD card, on MBLS1028A	OFF	OFF	OFF	OFF	3.3 V (80 % to 100 %)
eMMC, on TQMLS1028A	ON	OFF	OFF	OFF	2.33 V (60 % to 80 %)
NOR flash, on TQMLS1028A	OFF	ON	OFF	OFF	1.65 V (40 % to 60 %)
Hard Coded RCW, on TQMLS1028A	OFF	OFF	ON	OFF	1.05 V (20 % to 40 %)
I^2C EEPROM, on TQMLS1028A	OFF	OFF	OFF	ON	0 V (0 % to 20 %)

4.1.2 Clock generation

The following figure shows, which clocks are required on the TQMLS1028A and how they are generated.

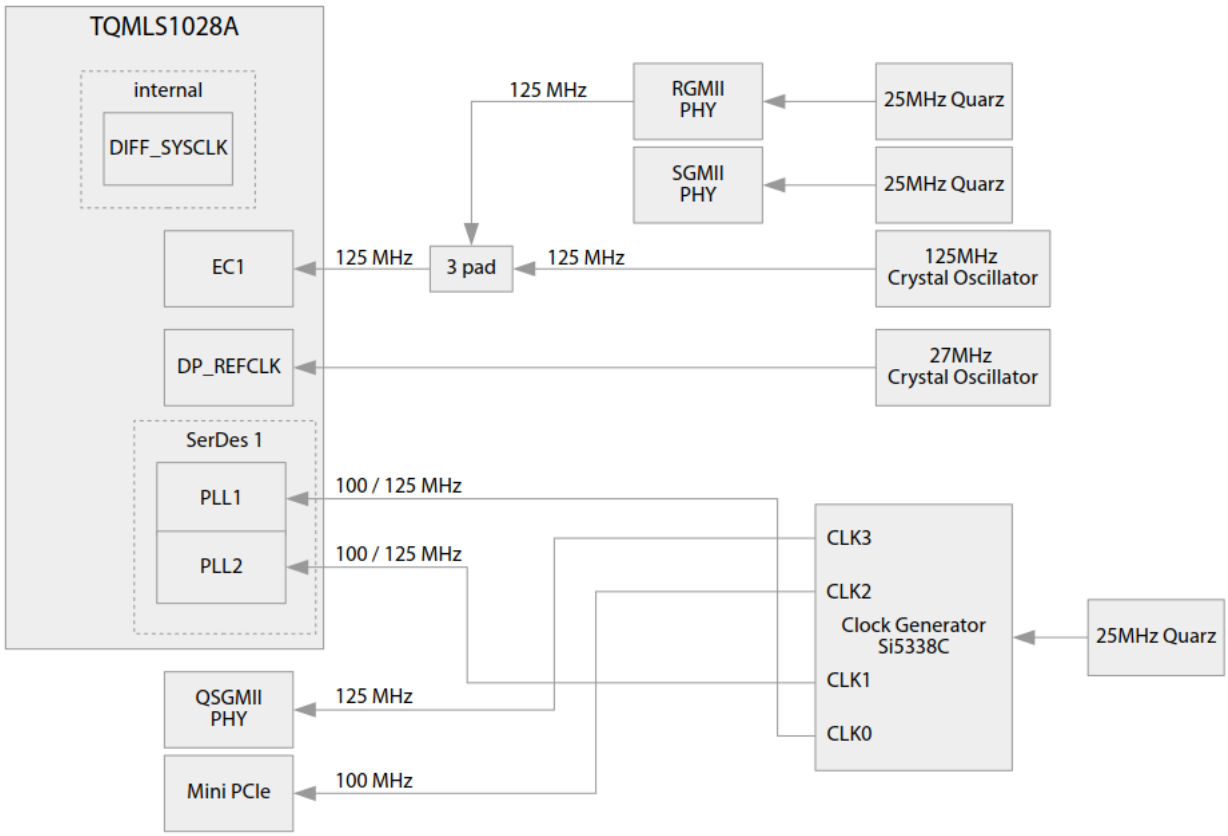

Figure 3: Block diagram clock generation on MBLS1028A

4.1.3 Reset structure

The reset structure is designed in such a way that the TQMLS1028A and the Reset button on the MBLS1028A are the control center. This ensures that the Reset is enabled at the right time during power-up. Corresponding reset delays are handled by the TQMLS1028A. The remaining PHYs, hub and other reset-capable components on the module are controlled by the I²C expander.

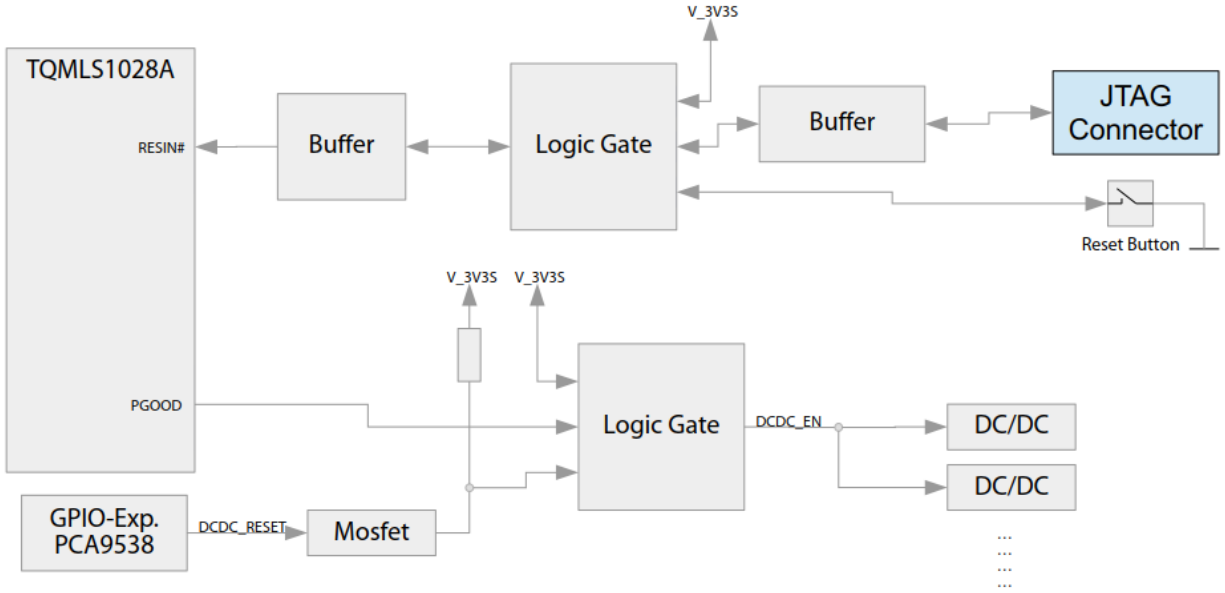

Figure 4: Block diagram Reset structure

4.1.4 I²C devices

The TQMLS1028A provides various I²C buses, of which only IIC5 and IIC6 are used on the MBLS1028A.
The following block diagram shows the I²C bus structure.

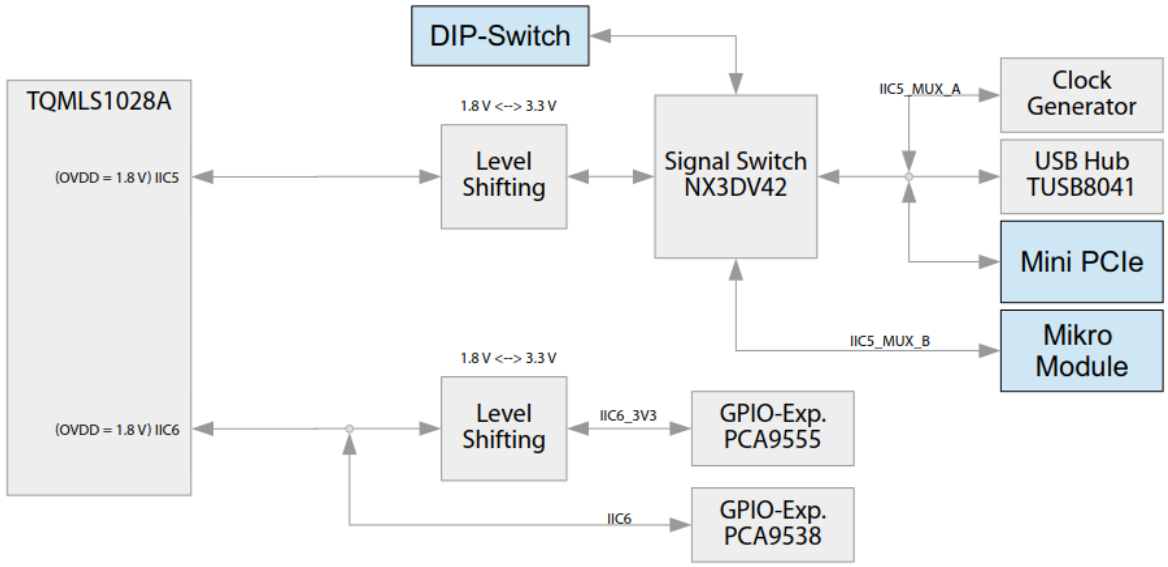

Figure 5: Block diagram I²C bus

On the TQMLS1028A further I²C devices are used, therefore the already assigned I²C addresses were taken into account.
The voltage (OVDD at IIC6) is fixed at 1.8 V and therefore requires a level shifter to 3.3 V.
The following table shows the I²C address mapping on TQMLS1028A and MBLS1028A.

Table 4: I²C devices, address mapping on TQMLS1028A and MBLS1028A

Location	I²C bus	Device	Function	7-bit address	Remark
MBLS1028A	IIC5	SI5338C	Clock Generator	0x70 / 111 0000b	Optional, not connected
		TUSB8041	USB 3.0 Hub	0x44 / 100 0100b	Optional, not connected
		–	mPCIe	–	Defined by customer, X12
		–	mikroBUS™	–	Defined by customer, X32
	IIC6	PCA9555	Port expander	0x25 / 010 0101b	Device D43, 3.3 V
		PCA9538	Port expander	0x70 / 111 0000b	Device D46, 1.8 V
TQMLS1028A	IIC1	MKL04Z16	System Controller	0x11 / 001 0001b	Should not be altered
		SE97B	Temp. Sensor	0x18 / 001 1000b	Access to temperature registers
			EEPROM	0x50 / 101 0000b	R/W access in Normal Mode
			EEPROM	0x30 / 011 0000b	R/W access in Protected Mode
		24LC256T	EEPROM	0x57 / 101 0111b	–
		SA56004EDP	Temp. Sensor	0x4C / 100 1100b	–
		PCF85063	RTC	0x51 / 101 0001b	–

4.1.4.1 Temperature sensor

There is no temperature sensor on the MBLS1028A, but a temperature sensor SE97BTP is provided on the TQMLS1028A.

4.1.4.2 GPIO port expander

To control several components on the MBLS1028A, a port expander PCA9538 with 8 ports and a port expander PCA9555 with 16 ports are assembled. Both port expanders are controlled via IIC6. The addresses of the port expanders can be changed by reassembling resistors. When changing the address, care must be taken to avoid address conflicts with existing I²C devices. The assembly options are documented in the circuit diagram.

In the initial state, after power-up, all ports are set as input and the connected component is thus deactivated.

The following table shows the signals controlled by the port expanders.

Table 5: Function of Port Expanders

Port	Signal	Dir.	Remark
8-port Expander PCA9538, D68, I²C address 0x25 / 010 0101b			
IO_0	EC1_INT#	I	–
IO_1	EC1_RESET#	O	–
IO_2	SGMII_INT#	I	–
IO_3	SGMII_RESET#	O	–
IO_4	QSGMII_INT#	I	–
IO_5	QSGMII_RESET#	O	–
IO_6	DCDC_RESET	O	–
IO_7	–	–	(not used)
16-port Expander, PCA9538, D69, I²C address 0x70 / 111 0000b			
IO0_0	CLK_INT#	I	–
IO0_1	USB_RST#	O	–
IO0_2	MPCIE_WAKE#	O	–
IO0_3	MPCIE_DIS#	O	–
IO0_4	MPCIE_RST#	O	–
IO0_5	SIM_CARD_DETECT	I	–
IO0_6	SATA_PERST#	O	–
IO0_7	RESET_SDA_3V3#	O	–
IO1_0	Mikro_Module_RST#	O	–
IO1_1	Mikro_Module_PWM	O	–
IO1_2	Mikro_Module_INT	I	–
IO1_3	USER_BUTTON_1	I	–
IO1_4	USER_BUTTON_2	I	–
IO1_5	USER_LED_1	O	–
IO1_6	USER_LED_2	O	–
IO1_7	BUZZER	O	–

4.2 Power supply

The MBLS1028A has to be supplied with 18 V to 28 V at X3 or X27. The typical supply voltage is 24 V.

The following figure shows all voltages present on the MBLS1028A, which are structured into three main paths consisting of an LM25119, an LTC3851 and a TPS54335. These supply the biggest loads (TQMLS1028A, USB supply, SATA supply with up to 2500 mA). The power supply structure is designed in such a way that the 5 V voltage is always activated.

Furthermore the design allows power sequencing of all voltage levels used. All voltages are powered up after the boot process of the TQMLS1028A.

At the two headers X25 and X38 on the MBLS1028A 1.8 V, 3.3 V, 5 V and 12 V are available. Both connectors share the available total power of the individual voltage rails.

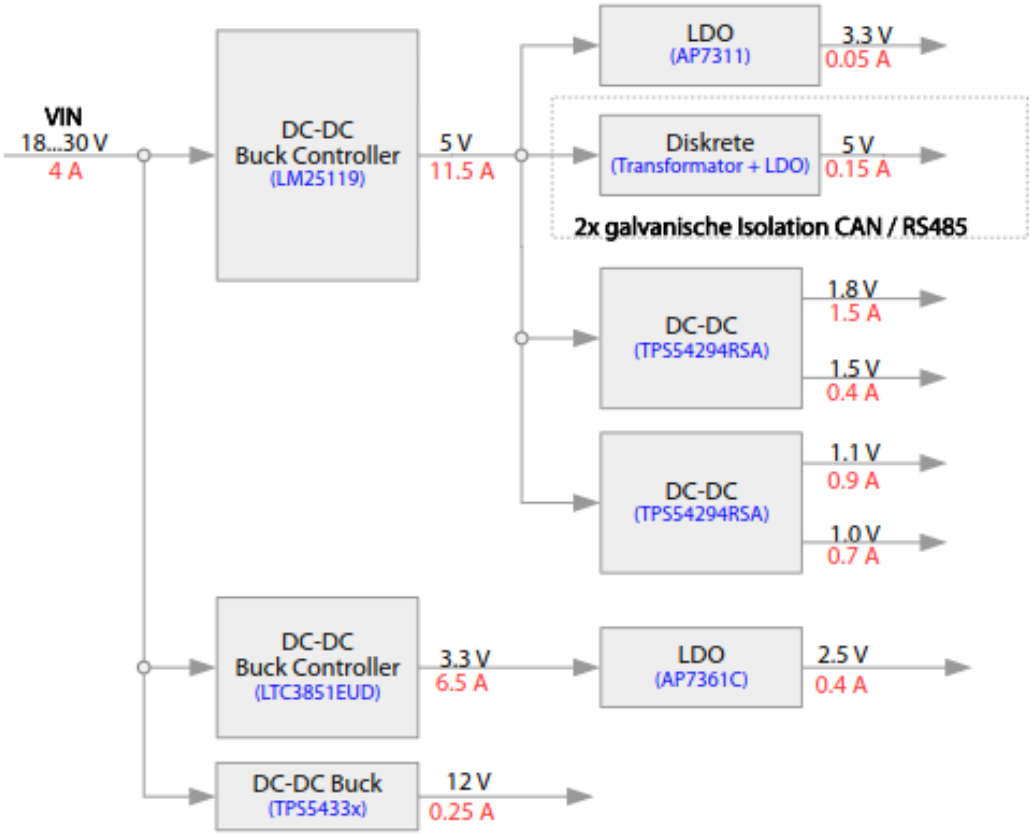

Figure 6: Block diagram power supply

4.2.1 Protective circuitry

The protection circuit (see Figure 7) features the following characteristics:

- Overcurrent protection by fuse 5 A, slow blow
- Overvoltage protection diode
- PI filter
- Reverse polarity protection by MOSFET

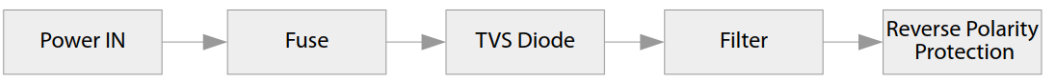

Figure 7: Block diagram protective circuit

4.2.2 Battery

In case of power failure a lithium battery type CR2032 on the MBLS1028A supplies the RTC on the TQMLS1028A.

4.3 Communication interfaces

4.3.1 Ethernet

4.3.1.1 RGMII

The LS1028A provides an RGMII Ethernet controller (EC1 – port 1). On the MBLS1028A the interface provides a Gigabit Ethernet port. The PHY supports IEEE® 802.3 10BASE-T, 100BASE-T, and 1000BASE-T.

The 125 MHz reference clock for the MAC of the CPU is generated by a quartz oscillator.

The RGMII interface contains PHY reset and interrupt signals. The PHY signals are routed to RJ-45 connector X6.

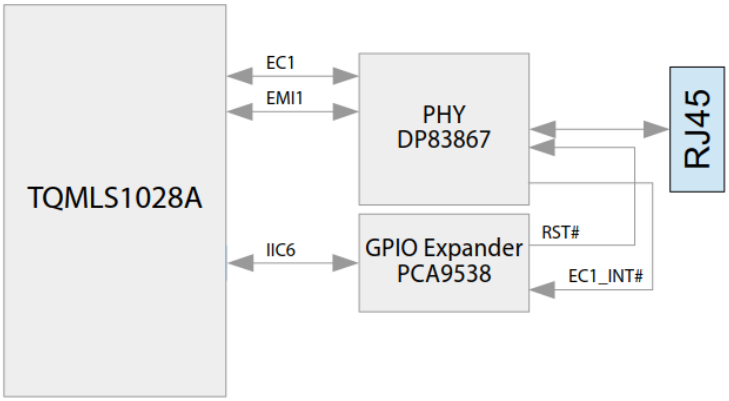

Figure 8: Block diagram Ethernet RGMII

4.3.1.2 SGMII

The LS1028A provides an Ethernet controller (SGMII – port 0), which is used as SGMII interface via SerDes Lane 0.

On the MBLS1028A the interface provides a Gigabit Ethernet port.

The SGMII interface contains PHY reset and interrupt signals. The PHY signals are routed to RJ-45 connector X7.

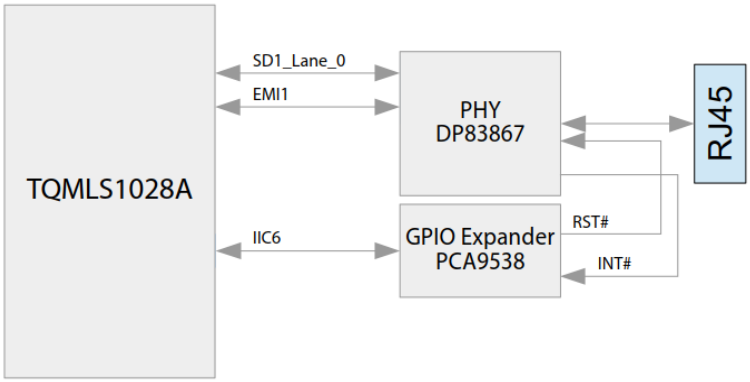

Figure 9: Block diagram Ethernet SGMII

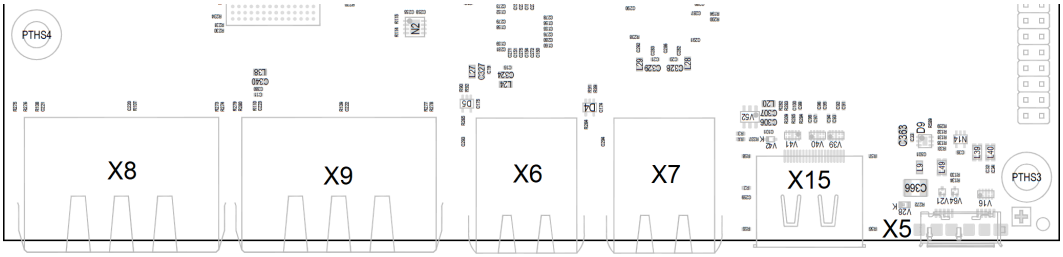

Figure 10: Gbit ETH connectors X6, X7

4.3.1.3 QSGMII

In addition to the Ethernet Controller (ENETC), the LS1028A CPU provides a TSN switch (Time-Sensitive Networking Switch) that operates four external ports via SerDes.

The TSN switch is not routed via the Ethernet controller but via SerDes and is implemented as QSGMII.

The QSGMII interface includes PHY reset and interrupt signals.

When looking at the MBLS1028A from outside, X8 is on the left, X9 is on the right.

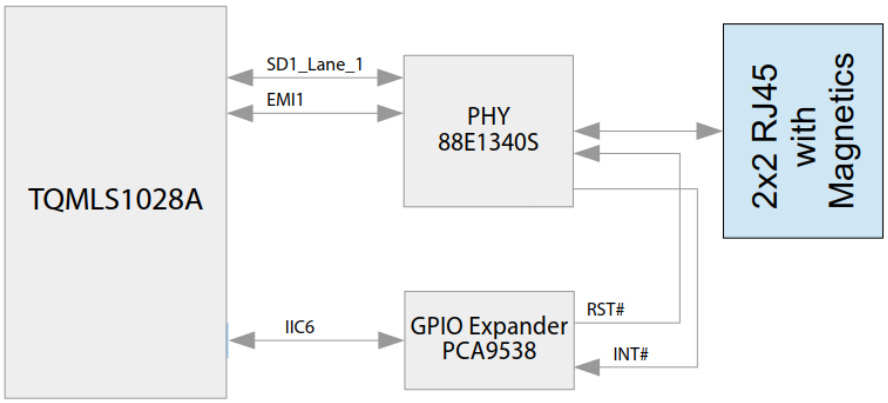

Figure 11: Block diagram Ethernet QSGMII

The following table shows the pinout of the Ethernet connectors X8, and X9.

Table 6: Pinout Ethernet QSGMII, RJ-45 connectors X8, X9

RJ-45	X8		X9	
	Left	Right	Left	Right
Interface	P0_MDI	P1_MDI	P2_MDI	P3_MDI

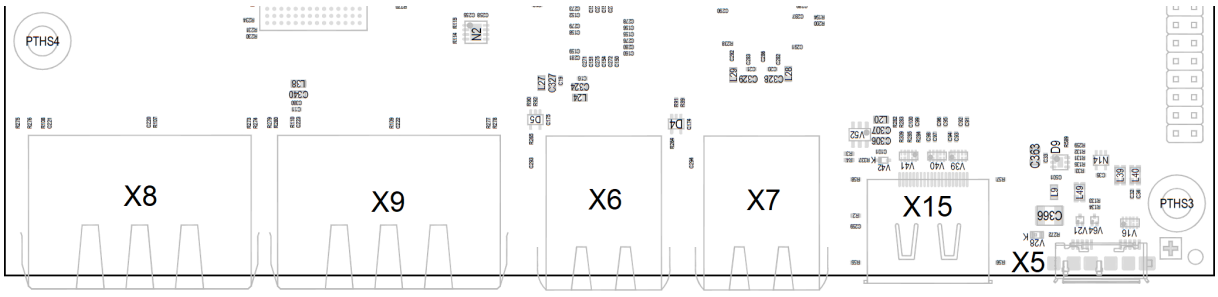

Figure 12: Gbit ETH connectors X8, X9

4.3.2 USB 3.0 Hub

The TI USB 3.0 Hub TUSB8041 connected to the USB 3.0 OTG port (USB2) of the TQMLS1028A provides four USB HOST ports.
Two ports (USB Host1&2) are routed as USB 3.0 interfaces to a stacked connector (X10), the third port is routed as USB 2.0 interface to the mPCIe connector X12, the fourth port is routed as USB 2.0 interface to header X38.
The USB 3.0 Hub TUSB8041 can be programmed via I²C, the address is 0x44 / 100 0100b, see also Table 4.
A power distribution switch provides 5 V for the USB connectors. The current is monitored and can be switched off in case of an overload and/or overheating.

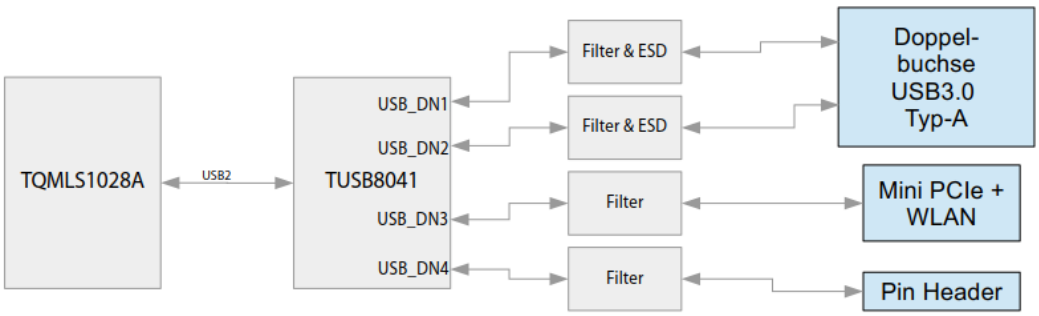

Figure 13: Block diagram USB 3.0 Hub

The USB host port of the TQMLS1028A provides a theoretical data rate of 5 Gbit/s. This is divided among the connected ports. Depending on the software and hardware used, the effective read and write rates of the ports may vary.
The following table shows the pinout of the stacked connector X10.

Table 7: Pinout USB Host1&2, USB Type A, X10

Pin	Pin name	Signal	Remark
1	VBUS_2	V_VBUS_DN2	100 µF to DGND + EMI filter
2	D–_2	USB_DN2_D–	Common Mode Choke in series
3	D+_2	USB_DN2_D+	Common Mode Choke in series
4	GND_2	DGND	–
5	SSRX–_2	USB_DN2_RX–	Common Mode Choke in series
6	SSRX+_2	USB_DN2_RX+	Common Mode Choke in series
7	GND-DRAIN_2	DGND	–
8	SSTX–_2	USB_DN2_TX–	Common Mode Choke in series + 100 nF AC coupling capacitor
9	SSTX+_2	USB_DN2_TX+	Common Mode Choke in series + 100 nF AC coupling capacitor
10	VBUS_1	V_VBUS_DN1	100 µF to DGND + EMI filter
11	D–_1	USB_DN1_D–	Common Mode Choke in series
12	D+_1	USB_DN1_D+	Common Mode Choke in series
13	GND_1	DGND	–
14	SSRX–_1	USB_DN1_RX–	Common Mode Choke in series
15	SSRX+_1	USB_DN1_RX+	Common Mode Choke in series
16	GND-DRAIN_1	DGND	–
17	SSTX–_1	USB_DN1_TX–	Common Mode Choke in series + 100 nF AC coupling capacitor
18	SSTX+_1	USB_DN1_TX+	Common Mode Choke in series + 100 nF AC coupling capacitor
M1 … M4	Shield	DGND	–

Table 8: Pinout USB Host3, mPCIe connector, X12

Pin	Pin name	Signal	Remark
36	D–	USB_DN3_D–	Common Mode Choke in series
38	D+	USB_DN3_D+	Common Mode Choke in series

Table 9: Pinout USB Host4, 40-pin header, X38

Pin	Pin name	Signal	Remark
31	D+	USB_DN4_D+	Common Mode Choke in series
35	D–	USB_DN4_D–	Common Mode Choke in series

4.3.3 USB 3.0 OTG

The LS1028A has two USB3.0 controllers with integrated PHY. USB1 is used as OTG interface.
A USB 3.0 Micro B connector is assembled on the MBLS1028A.
In order to use the interface as Host/Device, a suitable adapter comes with the MBLS1028A.

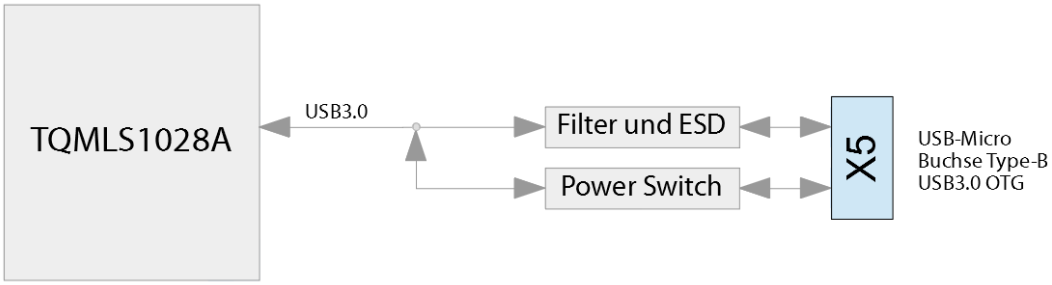

Figure 14: Block diagram USB

The USB1 port of the TQMLS1028A provides a theoretical data rate of 5 Gbit/s.
Depending on the software and hardware used, the effective read and write rates of the ports may vary.
The following table shows the pinout of USB OTG connector X5.

Table 10: Pinout USB OTG, X5

Pin	Pin name	Signal	I/O	Remark
1	VBUS	V_VBUS_USB1	P	100 µF to DGND + EMI filter
2	D–	USB1_D_M	I/O	Common Mode Choke in series
3	D+	USB1_D_P	I/O	Common Mode Choke in series
4	ID	USB1_ID	I	–
5	GND	DGND	P	–
6	SSTX–	USB1_TX_M	I/O	Common Mode Choke in series
7	SSTX+	USB1_TX_P	I/O	Common Mode Choke in series
8	GND_DRAIN	DGND	P	–
9	SSRX–	USB1_RX_M	I/O	Common Mode Choke in series + 100 nF AC coupling capacitor
10	SSRX+	USB1_RX_P	I/O	Common Mode Choke in series + 100 nF AC coupling capacitor
M1 … M6	Shield	DGND	P	–

4.3.4 CAN

Two ISO-11898 compliant CAN interfaces are provided on the MBLS1028A.
The signals are each connected to a 3-pin connector.
The interfaces are galvanically isolated, but not among each other.
The High-Speed Mode supports data rates of up to 5 Mbit/s.

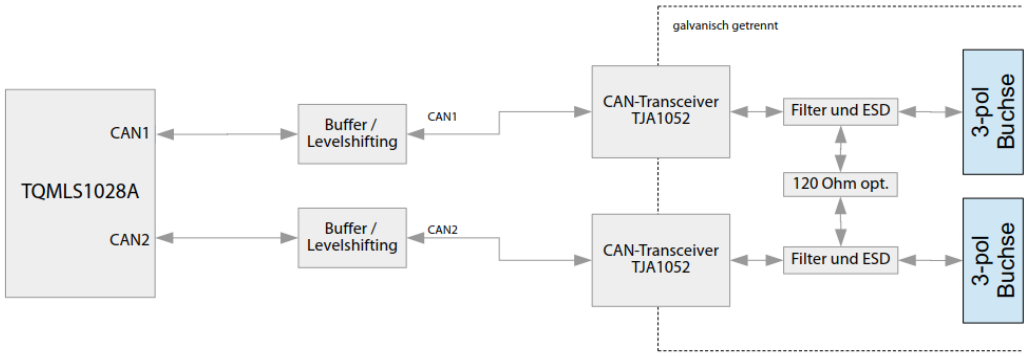

Figure 15: Block diagram CAN

The following table shows the pinout of the CAN connectors.

Table 11: Pinout CAN, X17, X29

CAN bus / connector	Pin	Signal	Direction	Remark
CAN1 / X17 CAN2 / X29	1	CAN_H	I/O	Galvanically separated
	2	CAN_L	I/O	
	3	GND_CAN	P	

The CAN signals can be terminated with 120 Ω using the DIP switches S1-1 & S1-2

Table 12: CAN termination, DIP switch S1

DIP switch	Interface	ON	OFF
S1-1	CAN1	CAN1 terminated with 120 Ω	CAN1 not terminated
S1-2	CAN2	CAN2 terminated with 120 Ω	CAN2 not terminated

All other combinations of S11 (e.g., S11-1 ON & S11-2 OFF) are not permitted.

4.3.5 Mini PCIe plus SIM card socket

The MBLS1028A provides a Mini PCIe slot with one PCIE lane (×1) for full-size cards (50.95 mm × 30 mm). Any standard compliant Mini PCIe card can be used. A SIM card holder is also provided.

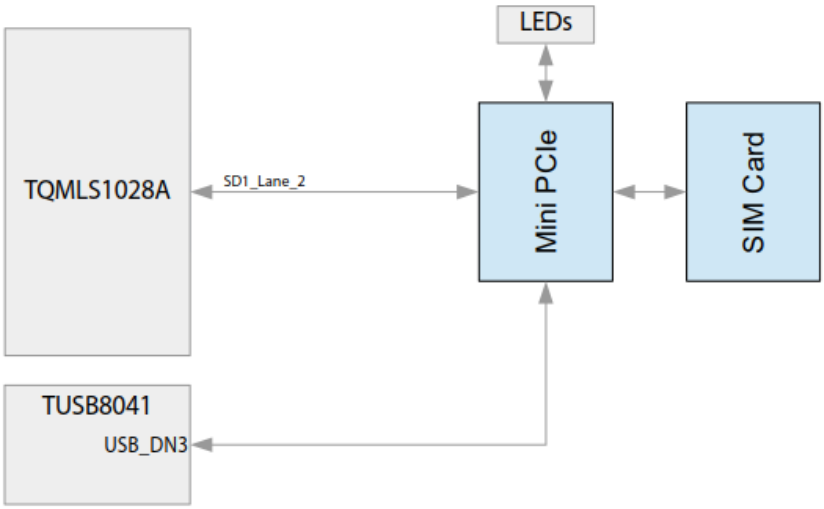

Figure 16: Block diagram Mini PCIe, SIM card

The voltages provided for the Mini PCIe card must not exceed the currents specified in the following table.

Table 13: Maximum permitted currents Mini PCIe, X12

Voltage	Nominal value	I_{max}
V_3V3_PCIE	3.3 V	1.1 A
V_1V5_PCIE	1.5 V	0.375 A

4.3.5 Mini PCIe plus SIM card socket (continued)

Table 14: Pinout Mini PCIe, X12

Remark	Signal	Pin		Signal	Remark
–	PCIE_WAKE#	1	2	V_3V3_MPCIE	–
–	NC	3	4	DGND	–
–	NC	5	6	V_1V5_MPCIE	–
–	NC	7	8	SIM_VCC	–
–	DGND	9	10	SIM_DATA	–
Signal from Clock Generator	MPCIE_CLK_N	11	12	SIM_CLK	–
Signal from Clock Generator	MPCIE_CLK_P	13	14	SIM_RST	–
–	DGND	15	16	SIM_VPP	–
Key notch					
–	NC	17	18	DGND	–
–	NC	19	20	MPCIE_DIS#	10 kΩ PU/PD, default: 10 kΩ PU
–	DGND	21	22	MPCIE_RST#	Global Reset
0 Ω serial termination	SD1_RX2_N	23	24	V_3V3_MPCIE	–
0 Ω serial termination	SD1_RX2_P	25	26	DGND	–
–	DGND	27	28	V_1V5_MPCIE	–
–	DGND	29	30	IIC5_SCL_MUX_A	–
100 nF in series	SD1_TX2_N	31	32	IIC5_SDA_MUX_A	I^2C address, see Table 4
100 nF in series	SD1_TX2_P	33	34	DGND	–
–	DGND	35	36	USB_DN3_D–	–
–	DGND	37	38	USB_DN3_D+	–
–	V_3V3_MPCIE	39	40	DGND	–
–	V_3V3_MPCIE	41	42	WWAN-LED	–
–	DGND	43	44	WLAN-LED	–
–	NC	45	46	WPAN-LED	–
–	NC	47	48	V_1V5_MPCIE	–
–	NC	49	50	DGND	–
–	NC	51	52	V_3V3_MPCIE	–

Table 15: Pinout SIM card connector, X13

Pin	Signal
C1	SIM_VCC
C2	UIM_RST
C3	UIM_CLK
C4	(NA)
C5	DGND
C6	SIM_VPP
C7	SIM_DATA
DL	SIM_CARD_DETECT
DS	DGND

4.3.6 M.2 B-Key (SSD SATA)

The LS1028A provides a SATA 3.0 AHCI interface via SerDes, which is routed from the TQMLS1028A to an M.2 connector on the MBLS1028A to provide an interface for mass storage.

Transfer rates of 1.5 Gb/s (Gen I), 3 Gb/s (Gen II) and 6Gb/s (Gen III) are possible.

An M.2 slot with B-coding is used on the MBLS1028A. The MBLS1028A supports M.2 sizes 2242, 2260 and 2280.

The standard mounting is for type 2280.

The SATA interface of the LS1028A and a 3.3 V power supply are connected to X35.

According to the M.2 specification, the power budget of the MBLS1028A includes 2.5 A for a SATA SSD.

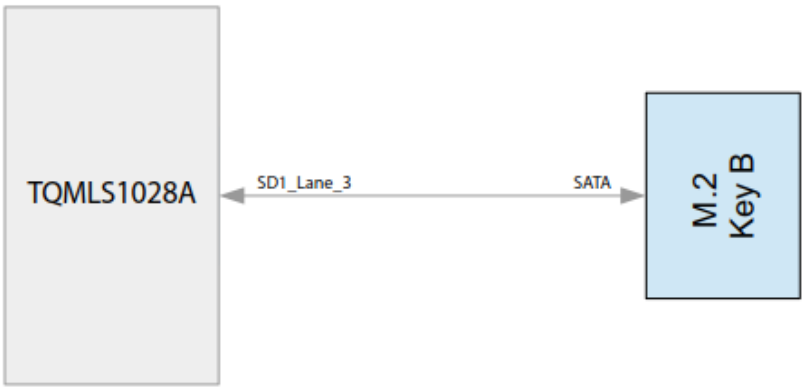

Figure 17: Block diagram M.2 (SSD SATA)

4.3.6 M.2 B-Key (SSD SATA) (continued)

Table 16: Pinout M.2 B-Key, X35

Remark	Signal	Pin		Signal	Remark
Assembly option: 10 kΩ Pull-Up	M2_CONFIG3	1			
–	DGND	3	2	V_3V3	–
–	DGND	5	4	V_3V3	–
–	NC	7	6	NC	–
–	NC	9	8	NC	–
–	DGND	11	10	LED	Activity LED at 3.3 V
Key notch (B-Key)					
Assembly option: 10 kΩ Pull-Up	M2_CONFIG0	21	20	NC	–
–	NC	23	22	NC	–
–	NC	25	24	NC	–
–	DGND	27	26	NC	–
–	NC	29	28	NC	–
–	NC	31	30	NC	–
–	DGND	33	32	NC	–
–	NC	35	34	NC	–
–	NC	37	36	NC	–
–	DGND	39	38	NC	–
10 nF AC from TQMLS1028A	SD1_RX3_P	41	40	NC	–
10 nF AC from TQMLS1028A	SD1_RX3_N	43	42	NC	–
–	DGND	45	44	NC	–
–	SD1_TX3_N	47	46	NC	–
–	SD1_TX3_P	49	48	NC	–
–	DGND	51	50	PERST#	100 kΩ PU or 0 Ω PD; default: NP
–	NC	53	52	NC	–
–	NC	55	54	NC	–
–	DGND	57	56	NC	–
–	NC	59	58	NC	–
–	NC	61	60	NC	–
–	NC	63	62	NC	–
–	NC	65	64	NC	–
–	NC	67	66	NC	–
Assembly option: 10 kΩ Pull-Up	M2_CONFIG1	69	68	NC	–
–	DGND	71	70	V_3V3	–
–	DGND	73	72	V_3V3	–
Assembly option: 10 kΩ Pull-Up	M2_CONFIG2	75	74	V_3V3	–

4.3.7 mikroBUS™

The MBLS1028A provides a mikroBUS™ for system extensions. The I2C5 bus is used at the mikroBUS™.
mikroBUS™ modules require 3.3 V and 5 V, which are provided by the MBLS1028A. PTC fuses limit the current load at 750 mA.
SPI and UART interfaces are connected via a switch in order to use them on headers or to be able to disconnect the mikroBUS™.
No maximum values are specified for the power consumption. Since these are low-power modules, the current consumption is limited to 500 mA per supply rail.
The following table shows the signals of mikroBUS™ connectors X32 and X33.

Table 17: Pinout mikroBUS™ connectors X32, X33

X33			
Remark	Signal	Name	Pin
10 kΩ to DGND optional 10 kΩ to 3.3 V	0 V	AN	1
–	Mikro_Module_RST#	RST	2
–	SPI3_PCS0_MUX_B	CS	3
–	SPI3_SCK_MUX_B	SCK	4
–	SPI3_SIN_MUX_B	MISO	5
–	SPI3_SOUT_MUX_B	MOSI	6
750 mA PTC fuse	V_3V3	+3.3V	7
–	DGND	GND	8

X32			
Pin	Name	Signal	Remark
1	PWM	Mikro_Module_PWM	–
2	INT	Mikro_Module_INT	–
3	RX	UART2_SOUT_MUX_B	–
4	TX	UART2_SIN_MUX_B	–
5	SCL	IIC5_SCL_MUX_B	–
6	SDA	IIC5_SDA_MUX_B	–
7	+5V	V_5V0_SW	750 mA PTC fuse
8	GND	DGND	–

4.3.8 SD card

The SD card socket is directly connected via a 4-bit data interface to the uSDHC controller of the TQMLS1028A.
The uSDHC controller in the TQMLS1028A supports UHS-I mode.
The USDHC1 signals are supplied by EVDD (10 kΩ PU to 1.8 V or 3.3 V).
The I/O voltage is switched by the TQMLS1028A signal SDHC1_VSEL.
The SD card supply is fixed at 3.3V. The signal lines have PUs to 3.3 V. This ensures that the pull-up voltage is at the correct level after automatic switching to UHS-I mode. All data lines are ESD protected.
It is possible to boot from SD card.

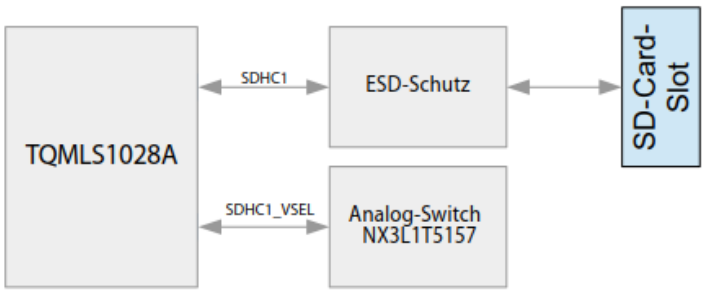

Figure 18: Block diagram SD card

Table 18: Pinout SD card, X16

Pin	Signal	Remark
1	SDHC1_DATA2_R	10 kΩ PU to 3.3 V + ESD protection
2	SDHC1_DATA3_R	10 kΩ PU to 3.3 V + ESD protection
3	SDHC1_CMD_R	10 kΩ PU to 3.3 V + ESD protection
4	VCC3V3	Optional: 1.8 V or 3.3 V
5	SDHC1_CLK	ESD protection
6	DGND	–
7	SDHC1_DATA0_R	10 kΩ PU to 3.3 V + ESD protection
8	SDHC1_DATA1_R	10 kΩ PU to 3.3 V + ESD protection
SW1	SDHC1_CD#	10 kΩ PU to 1.8 V + ESD protection
SW2	DGND	–
M1 … M4	SHIELD	Shield

Note: SD card supply voltage	
	SD cards always start with 3.3 V I/O voltage after power-up. For the modes with 1.8 V I/O voltage they are switched by software. When rebooting or resetting the MBLS1028A, the SD card remains at the last used I/O voltage because it does not have a separate reset signal. The SDHC controller, on the other hand, returns to 3.3 V I/O voltage. Therefore, the supplied BSP is limited to the 3.3 V modes.

4.3.9 Headers

The MBLS1028A features a 40-pin and a 60-pin 100 mil header, which provide all unused signals and those which should be easy to access. 1.8 V, 3.3 V, 5 V, and 12 V are available at both headers. The maximum current load of all four voltage rails is 3 A each. Both headers share the total available power of the four respective voltage rails.

Table 19: Pinout Header 1, X25

Level	Group	Signal	Pin		Signal	Group	Level
12 V	Power	V_12V	1	2	V_3V3	Power	3.3 V
5 V	Power	V_5V0_SW	3	4	V_3V3	Power	3.3 V
5 V	Power	V_5V0_SW	5	6	V_1V8	Power	1.8 V
0 V	Power	DGND	7	8	V_1V8	Power	1.8 V
3.3 V	PGOOD	PGOOD	9	10	DGND	Power	0 V
3.3 V	I²C	IIC1_SDA_3V3	11	12	IIC1_SCL_3V3	I²C	3.3 V
0 V	Power	DGND	13	14	PROG_MTR	Factory Test	–
5 V (OC)	System	RTC_INT_OUT#	15	16	FA_VL	Factory Test	–
VBAT	System	RTC_CLKOUT	17	18	TA_PROG_SFP	Factory Test	–
0 V	Power	DGND	19	20	TA_BB_VDD	Power	(VDD)
1.8 V	XSPI	XSPI1_A_SCK	21	22	DGND	Power	0 V
0 V	Power	DGND	23	24	XSPI1_A_DATA4	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DQS	25	26	XSPI1_A_DATA5	XSPI	1.8 V
0 V	Power	DGND	27	28	XSPI1_A_DATA6	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA0	29	30	XSPI1_A_DATA7	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA1	31	32	XSPI1_A_CS0#	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA2	33	34	XSPI1_A_CS1#	XSPI	1.8 V
1.8 V	XSPI	XSPI1_A_DATA3	35	36	DGND	Power	0 V
0 V	Power	DGND	37	38	SPI3_PCS0_MUX_A	SPI	1.8 V
1.8 V	SDHC	SDHC2_CLK	39	40	SPI3_SIN_MUX_A	SPI	1.8 V
0 V	Power	DGND	41	42	SPI3_SOUT_MUX_A	SPI	1.8 V
1.8 V	SDHC	SDHC2_CMD	43	44	SPI3_SCK_MUX_A	SPI	1.8 V
0 V	Power	DGND	45	46	DGND	Power	0 V
1.8 V	SDHC	SDHC2_DS	47	48	DGND	Power	0 V
0 V	Power	DGND	49	50	SDHC2_DAT4	SDHC	1.8 V
1.8 V	SDHC	SDHC2_DAT0	51	52	SDHC2_DAT5	SDHC	1.8 V
1.8 V	SDHC	SDHC2_DAT1	53	54	SDHC2_DAT6	SDHC	1.8 V
1.8 V	SDHC	SDHC2_DAT2	55	56	SDHC2_DAT7	SDHC	1.8 V
1.8 V	SDHC	SDHC2_DAT3	57	58	DGND	Power	0 V
0 V	Power	DGND	59	60	DGND	Power	0 V

4.3.9 Headers (continued)

Table 20: Pinout Header 2, X38

Level	Group	Signal	Pin		Signal	Group	Level
12 V	Power	V_12V	1	2	V_3V3	Power	3.3 V
5 V	Power	V_5V0_SW	3	4	V_3V3	Power	3.3 V
5 V	Power	V_5V0_SW	5	6	V_1V8	Power	1.8 V
0 V	Power	DGND	7	8	V_1V8	Power	1.8 V
1.8 V	UART	UART_RX_SDA_3V3	9	10	DGND	Power	0 V
1.8 V	UART	UART_TX_SDA_3V3	11	12	IIC1_SCL	I^2C	1.8 V
0 V	Power	DGND	13	14	IIC1_SDA	I^2C	1.8 V
1.8 V	UART	UART2_SIN_MUX_A	15	16	DGND	Power	0 V
1.8 V	UART	UART2_SOUT_MUX_A	17	18	TEMP_ALERT#	System	3.3 V
0 V	Power	DGND	19	20	TEMP_CRIT_MOD#	System	3.3 V
1.8 V	Reset	PORESET#	21	22	DGND	Power	0 V
1.8 V	Reset	HRESET#	23	24	CLK_OUT	System	VBAT
1.8 V	Reset	RESET_REQ#	25	26	DGND	Power	0 V
0 V	Power	DGND	27	28	ASLEEP	Debug	1.8 V
0 V	Power	DGND	29	30	TA_TMP_DETECT#	Trust	1.8 V
–	USB 3.0	USB_DN4_D+	31	32	TA_BB_TMP_DETECT#	Trust	1.8 V
0 V	Power	DGND	33	34	SCAN_MODE#	Factory Test	1.8 V
–	USB 3.0	USB_DN4_D-	35	36	TEST_SEL#	Factory Test	1.8 V
0 V	Power	DGND	37	38	TBSCAN_EN#	JTAG	1.8 V
0 V	Power	DGND	39	40	DGND	Power	0 V

4.4 User interfaces

4.4.1 Display port

The LS1028A provides a GPU with an integrated LCD controller that supports DisplayPort 1.3 and eDP 1.4.
DisplayPort is implemented on the MBLS1028A.
The DisplayPort connector X15 provides 3.3 V, which may be loaded with max. 500 mA. All signals provide ESD protection.

➢ Due to different electrical specifications of DisplayPort and eDP,
it may be necessary to correct the voltage swing or pre-emphasis level via software.

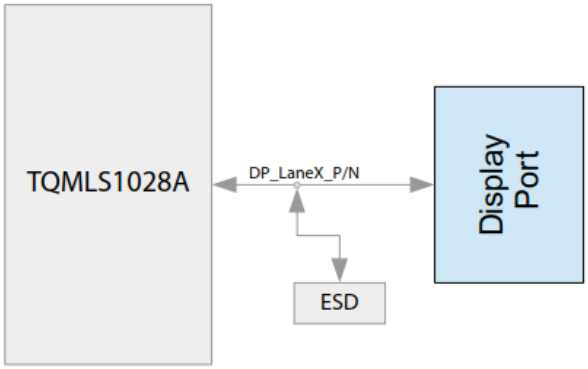

Figure 19: Block diagram display port

Table 21: Pinout display port, X15

Pin	Signal	Remark
1	DP_ML0+	ESD protection + 100 nF in series
2	DGND	–
3	DP_ML0–	ESD protection + 100 nF in series
4	DP_ML1+	ESD protection + 100 nF in series
5	DGND	–
6	DP_ML1–	ESD protection + 100 nF in series
7	DP_ML2+	ESD protection + 100 nF in series
8	DGND	–
9	DP_ML2–	ESD protection + 100 nF in series
10	DP_ML3+	ESD protection + 100 nF in series
11	DGND	–
12	DP_ML3–	ESD protection + 100 nF in series
13	DP_CFG1	1MΩ to DGND
14	DP_CFG2	1MΩ to DGND
15	DP_AUX_CH+	ESD protection + 100 nF in series
16	DGND	–
17	DP_AUX_CH–	ESD protection + 100 nF in series
18	DP_HPD_R	51 kΩ in series
19	DGND	–
20	V_3V3_DP	V_3V3
M1 … M4	DGND	–

4.4.2 Status LEDs

Two green LEDs (V55, V56) are provided on the MBLS1028A for tests. They are controlled by IO1_5 and IO1_6 of the 16-port I²C expander PCA9538, D69, see Table 5.

The presence of all important supply voltages is indicated by green LEDs. They light up when the corresponding voltage is active and simplify developing with the MBLS1028A. The following supply voltages are indicated by green LEDs:

Table 22: Supply voltages LEDs

Voltage	LED
V_24V	V72
V_12V	V71
V_5V0	V73
V_3V3	V74
V_3V3S	V70
V_2V5	V84
V_1V8	V75
V_1V5	V76
V_1V1	V77
V_1V0	V78

4.4.3 Buzzer

For acoustic signalling of events, a signal generator is provided on the MBLS1028A.

It is controlled by IO1_7 of the 16-port I²C expander PCA9538, D69, see Table 5.

4.4.4 Reset Push button

A reset button (S7) is provided on the MBLS1028A.

4.4.5 User push button

Two push buttons (S4, S5) are provided on the MBLS1028A.

The push button status can be read at the 16-port I²C expander PCA9538, D69, see Table 5.

4.4.6 DIP switches

Two 4-fold DIP switches (S9, S10) are provided on the MBLS1028A. The function of DIP switch S9 is described in Table 3.

With DIP switch S10 the SPI, IIC5, UART2, and VCC_FAN signals on the MBLS1028A can be toggled between two destinations.

The four individual switches switch to Ground and have 4.7 kΩ PU to 3.3 V.

The following table shows the functions of DIP switch S10.

Table 23: Function DIP switch, S10

Switch	Position	Function	Remark
1~2	Open	I2C5 switched to MikroBUS™	4.7 kΩ PU to 3.3 V
	Closed	I2C5 switched to I2C5_MUX_A or I2C5_MUX_B on MBLS1028A	
3~4	Open	UART2 switched to MikroBUS™	4.7 kΩ PU to 3.3 V
	Closed	UART2 switched to UART2_MUX_A or UART2_MUX_B on MBLS1028A	
5~6	Open	SPI3 switched to MikroBUS™	4.7 kΩ PU to 3.3 V
	Closed	SPI3 switched to header X25	
7~8	Open	Fan on	4.7 kΩ PU to 3.3 V
	Closed	Fan off	

4.5 Diagnostic interfaces

4.5.1 JTAG®

The JTAG® port of the LS1028A on the TQMLS1028A is routed to a standard ARM® 20-pin JTAG® connector.
The JTAG® signals of the TQMLS1028A are routed to an OpenSDA microcontroller via level shifters.
Between level shifter and MBLS1028A are tri-state buffers, which are switched by the firmware of the OpenSDA.
The JTAG® port of the microcontroller for the OpenSDA interface is routed to a 10-pin JTAG® connector with standard ARM pinout. For the OpenSDA circuitry see chapter 4.5.2.
A Lauterbach debugger is intended for programming the TQMLS1028A. The JTAG® interface has no ESD protection.

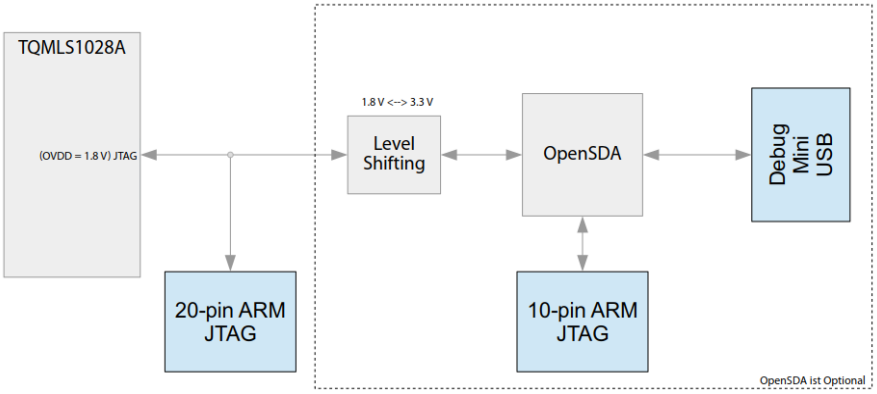

Figure 20: Block diagram JTAG®

The following table shows the pin assignment of the JTAG® connector.

Table 24: Pinout JTAG® header, X34

Pin	Signal	Remark
1	JTAG_VREF	100 Ω in series to 1.8 V, use only as reference
2	1.8 V	0 Ω in series to 1.8 V
3	JTAG_TRST#	10 kΩ PU to 1.8 V
4	DGND	–
5	JTAG_TDI	10 kΩ PU to 1.8 V
6	DGND	–
7	JTAG_TMS	10 kΩ PU to 1.8 V
8	GND_DETECT	10 kΩ PU to 1.8 V – OpenSDA interface
9	JTAG_TCK	–
10	DGND	–
11	NC	10 kΩ to DGND
12	DGND	–
13	JTAG_TDO	–
14	DGND	–
15	JTAG_SRST#	10 kΩ PU to 1.8 V, Open-Drain-Buffer at JTAG_SRST#_3V3
16	DGND	–
17	1.8 V	10 kΩ to 1.8 V
18	DGND	–
19	DGND	10 kΩ to DGND
20	DGND	–

4.5.2 OpenSDA / DAPLink

Currently the implementation of OpenSDA for the LS1028A is not available. However, a circuit for an OpenSDA programmer is prepared on the MBLS1028A, but it is currently not supported. A USB Mini-B connector (X24) to connect to a PC is available.
The following table shows the pin assignment of the JTAG connector for the Kinetis µC (D23).

Table 25: Pinout OpenSDA, 100 mil header, X22

Pin	Signal	Remark
1	V_SDA_3V3	–
2	SDA_JTAG_TMS	10 kΩ PU to V_SDA_3V3 ⇨ OpenSDA interface
3	DGND	–
4	SDA_JTAG_TCLK	–
5	DGND	–
6	SDA_JTAG_TDO	–
7	NC	–
8	SDA_JTAG_TDI	–
9	DGND	–
10	SDA_RESET#	–

Table 26: Pinout OpenSDA, USB Mini-B, X24

Pin	Signal	Remark
1	V_SDA_VBUS	–
2	USB0_DM	33 Ω in series
3	USB0_DP	33 Ω in series
4	NC	–
5	DGND	–
M1	Shield	–
M2	NC	–

4.5.3 USB Debug

A debug interface is available via UART1 of the TQMLS1028A.
The UART signals are routed to header X36 as well as to a UART to USB converter and routed to USB Micro AB connector X19.
To use the UART a DIP switch (S8) is provided to switch off the USB path.

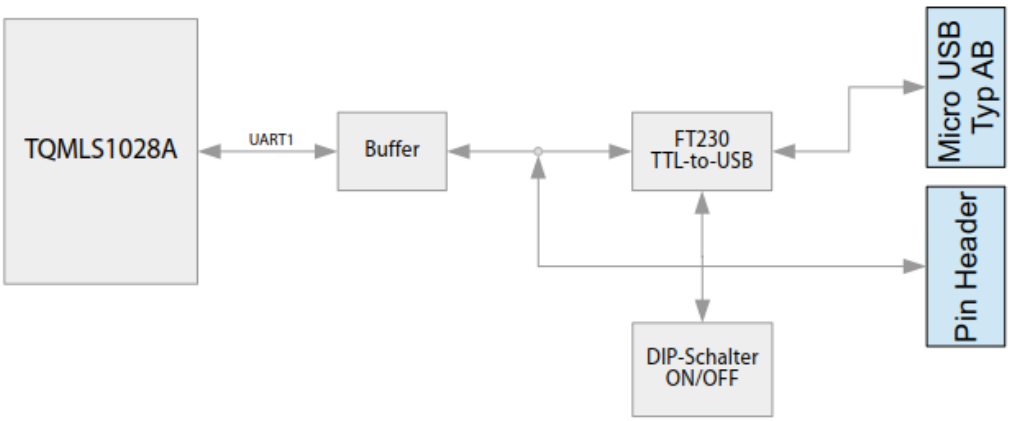

Figure 21: Block diagram Debug / RS-232

Table 27: Pinout Debug USB, X19

Pin	Signal
1	V_USB_DBG_VBUS
2	USB_DBG_D–
3	USB_DBG_D+
4	NC
5	DGND
M1 … M6	DGND

5. SOFTWARE

No software is required for the MBLS1028A.
Suitable software is only required on the TQMLS1028A and is not a part of this specification.
More information can be found in the Support Wiki for the TQMLS1028A.

6. MECHANICS

6.1 TQMLS1028A and MBLS1028A dimensions

The MBLS1028A has overall dimensions (length × width) of 170 × 170 mm².
The MBLS1028A has a maximum height of approximately 26.4 mm.
The MBLS1028A has six 4.3 mm mounting holes for the housing, and four 3.2 mm mounting holes for a heat sink.
The MBLS1028A weighs approximately 200 grams without TQMLS1028A.

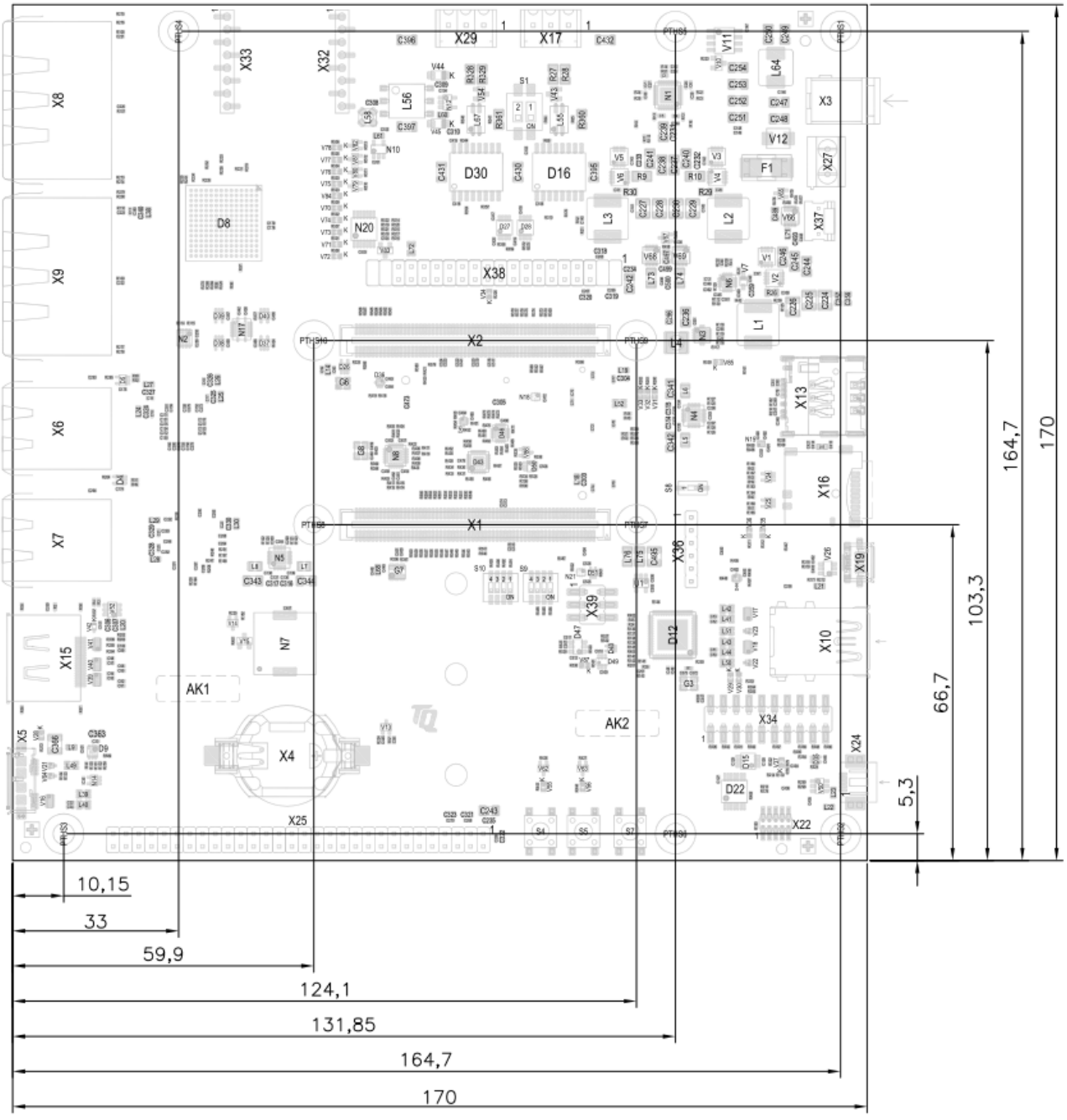

Figure 22: MBLS1028A dimensions

6.2 Notes of treatment

The TQMLS1028A is held in its mating connectors with a retention force of approximately 24 N.

To avoid damage caused by mechanical stress, the TQMLS1028A may only be extracted from the MBLS1028A by using the extraction tool MOZI8XX that can be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the MBLS1028A for the extraction tool MOZI8XX.

6.3 Embedding in the overall system

The MBLS1028A serves as a design base for customer products, as well as a platform to support during development.

6.4 Housing

The form factor and the mounting holes of the MBLS1028A are designed for installation in a standard EURO housing.

6.5 Thermal management

The MBLS1028A has a maximum peak power consumption of approximately 3 watts. Further power loss occurs mainly at externally connected devices.

Attention: TQMLS1028A heat dissipation	
	The LS1028A CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMLS1028A must be taken into consideration when connecting the heat sink. The TQMLS1028A is not the highest component. Inadequate cooling connections can lead to overheating of the TQMLS1028A or the MBLS1028A and thus malfunction, deterioration or destruction.

6.6 Assembly

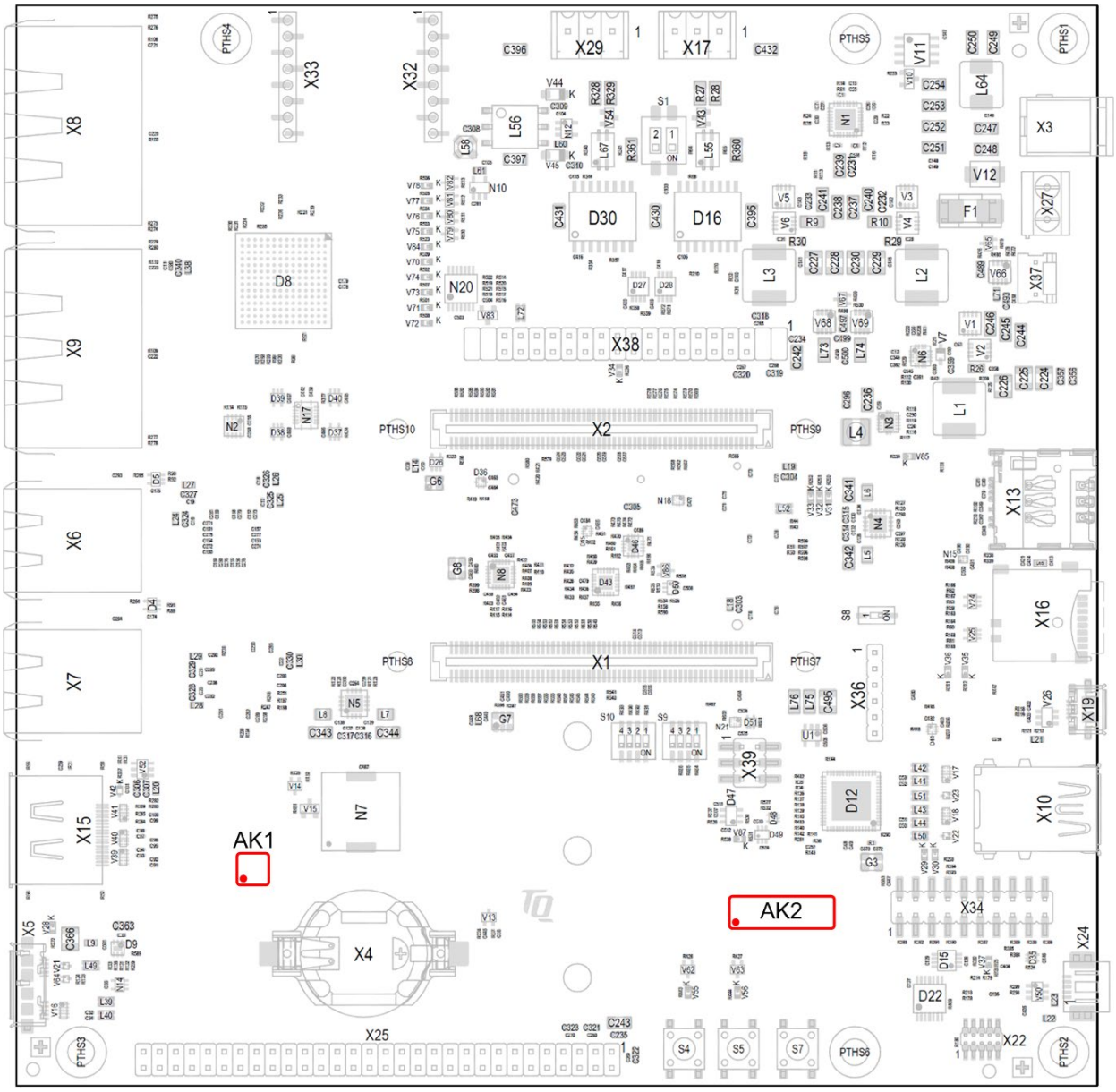

Figure 23: MBLS1028A component placement top

The labels on the MBLS1028A revision 0100 show the following information:

Table 28: Labels on MBLS1028A

Label	Text
AK1	Serial number
AK2	MBLS1028A version and revision + tests performed

6.6 Assembly (continued)

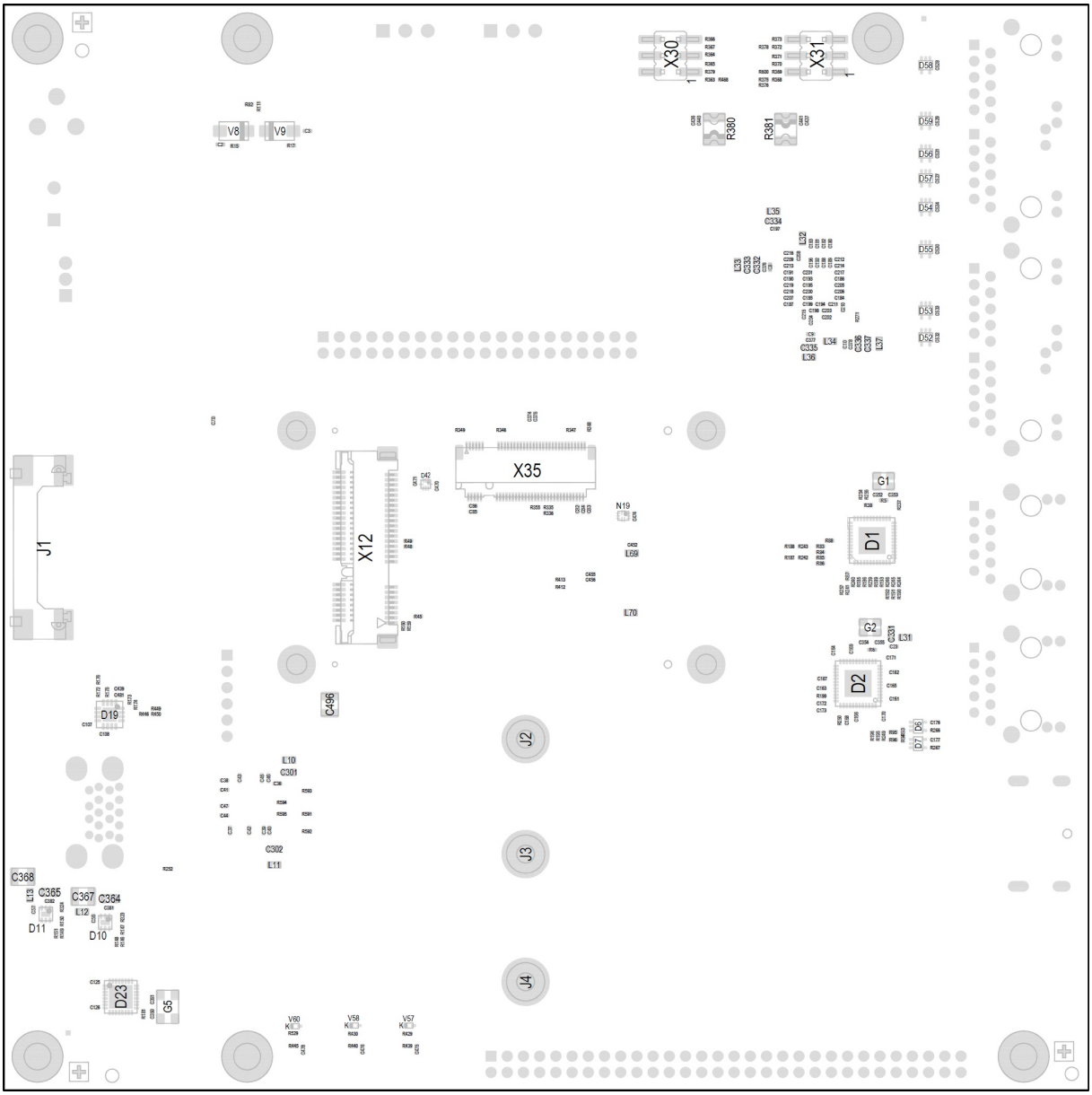

Figure 24: MBLS1028A component placement bottom

7. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

7.1 EMC

Since the MBLS1028A is a development platform, no EMC tests have been performed.

7.2 ESD

ESD protection is provided on most interfaces of the MBLS1028A.
The circuit diagram shows which interfaces provide ESD protection.

7.3 Operational safety and personal security

Tests for operational safety and personal protection were not carried out due to the voltages ≤30 V DC.

8. CLIMATIC AND OPERATIONAL CONDITIONS

In general reliable operation is given when the following conditions are met:

Table 29: Climatic and operational conditions MBLS1028A

Parameter	Range	Remark
Ambient temperature	0 °C to +60 °C	With Lithium battery
Ambient temperature	0 °C to +70 °C	Without Lithium battery
Storage temperature	–10 °C to +60 °C	With Lithium battery
Relative humidity (operation / storing)	10 % to 90 %	Not condensing

Attention: TQMLS1028A heat dissipation	
	The LS1028A CPU belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the TQMLS1028A must be taken into consideration when connecting the heat sink. The TQMLS1028A is not the highest component. Inadequate cooling connections can lead to overheating of the TQMLS1028A and thus malfunction, deterioration or destruction.

8.1 Protection against external effects

Protection class IP00 was defined for the MBLS1028A. There is no protection against foreign objects, touch or humidity.

8.2 Reliability and service life

No detailed MTBF calculation has been done for the MBLS1028A.
The MBLS1028A is designed to be insensitive to vibration and impact.

9. ENVIRONMENT PROTECTION

9.1 RoHS

The MBLS1028A is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

9.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the MBLS1028A was designed to be recyclable and easy to repair.

9.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

9.4 EuP

The Ecodesign Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The MBLS1028A must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the MBLS1028A enable compliance with EuP requirements for the MBLS1028A.

9.5 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the MBLS1028A, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. The MBLS1028A is delivered in reusable packaging.

9.6 Batteries

9.6.1 General notes

Due to technical reasons a battery is necessary for the MBLS1028A. Batteries containing mercury (Hg), cadmium (Cd) or lead (Pb) are not used. If this is for technical reasons unavoidable, the device is marked with the corresponding hazard note.
To allow a separate disposal, batteries are generally only mounted in sockets.

9.6.2 Lithium batteries

The requirements concerning special provision 188 of the ADR (section 3.3) are complied with for Lithium batteries.
There is therefore no classification as dangerous goods:

- Basic lithium content per cell not more than 1 grams (except for lithium ion and lithium polymer cells for which a lithium content of not more than 1.5 g per cell applies (equals 5 Ah)).
- Basic lithium content per battery not more than 2grams
  (except for lithium ion batteries for which a lithium content of not more than 8 grams per cell applies (equals 26 Ah)).
- Lithium cells and batteries are examined according to UN document ST/SG/AC.10-1.

During transport a short circuit or discharging of the socketed lithium battery is prevented by extricable insulating foils or by other suitable insulating measures.

9.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment.
To be able to reuse the MBLS1028A, it is produced in such a way, that it can be easily repaired and disassembled. The energy consumption of this subassembly is minimised by suitable measures. Due to the fact that at the moment there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls). These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally
  acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

10. APPENDIX

10.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 30: Acronyms

Acronym	Meaning
AC	Alternating Current
AHCI	Advanced Host Controller Interface
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DC	Direct Current
DDR4	Double Data Rate 4
DIP	Dual In-line Package
eDP	Embedded Display Port
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
eMMC	embedded Multimedia Card (flash)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
GPIO	General Purpose Input/Output
GPU	Graphics Processing Unit
I	Input
I/O	Input/Output
I2C	Inter-Integrated Circuit
IEEE®	Institute of Electrical and Electronics Engineers
IIC	Inter-Integrated Circuit
IP00	Ingress Protection 00
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Controller
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOZI	Modulzieher (module extractor)
mPCIe	Mini Peripheral Component Interconnect Express
MTBF	Mean operating Time Between Failures
NA	Not Available
NC	Not Connected
NOR	Not-Or
NP	Not Placed
O	Output
OC	Open Collector
OpenSDA	Serial and Debug Adapter (NXP)
OTG	On-The-Go

10.1 Acronyms and definitions (continued)

Table 30: Acronyms (continued)

Acronym	Meaning
P	Power
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PD	Pull-Down
PHY	Physical (layer of the OSI model)
PTC	Positive Temperature Coefficient
PU	Pull-Up
PWM	Pulse-Width Modulation
QSGMII	Quad Serial Gigabit Media-Independent Interface
R/W	Read/Write
RCW	Reset Configuration Word
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RGMII	Reduced Gigabit Media Independent Interface
RJ-45	Registered Jack 45
RoHS	Restriction of (the use of certain) Hazardous Substances
RS-232	Recommended Standard (serial interface)
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SerDes	Serializer/Deserializer
SGMII	Serial Gigabit Media Independent Interface
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SSD	Solid-State Disk
SVHC	Substances of Very High Concern
TSN	Time Sensitive Networking
UART	Universal Asynchronous Receiver/Transmitter
UHS-I	Ultra High-Speed (Speed Grade I)
UM	User's Manual
UN	United Nations
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network
WWAN	Wireless Wide Area Network
XSPI	Expanded Serial Peripheral Interface

10.2 References

Table 31: Further applicable documents

No.	Name	Rev., Date	Company
(1)	QorIQ® LS1028A Data Sheet	Rev. 0, 12/2019	NXP
(2)	QorIQ® LS1028A Reference Manual	Rev. 0, 12/2019	NXP
(3)	QorIQ® LS1028A Design Checklist, AN12028	Rev. 0, 12/2019	NXP
(4)	TQMLS1028A User's Manual	– current –	TQ-Systems
(5)	TQMLS1028A Support Wiki	– current –	TQ-Systems

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