TQMaRZG2x
User's Manual

TQMaRZG2x UM 0103
12.05.2023

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TABLE DIRECTORY

ILLUSTRATION DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0100	29.03.2021	Petz		First edition
0101	03.01.2022	Kreuzer	Table 7	Correction: MD15 has to be set to 1 (high) for booting.
0102	11.01.2022	Kreuzer	Table 7	Colour scheme adjusted
0103	12.05.2023	Kreuzer	Table 4 Table 17	3.3 V tolerance added (HDMI0_SCL/SDA)

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and Conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage / destruction of the component.
	This symbol indicates a possible source of danger. Acting against the procedure described can lead to possible damage to your health and / or cause damage / destruction of the material used.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is, not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMaRZG2x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.

Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.

Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.

The identification of the individual functions follows the above conventions.

Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBaRZG2x circuit diagram
- MBaRZG2x User's Manual
- RZ/G2x Data Sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: TQMaRZG2x Support Wiki

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMaRZG2x as of revision 0100, and refers to some software settings.
A certain TQMaRZG2x derivative does not necessarily provide all features described in this User's Manual.
This User's Manual does also not replace the Renesas CPU Reference Manuals. The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMaRZG2x, and the BSP provided by TQ-Systems; see also chapter 5.
The TQMaRZG2x is a universal Minimodule based on the Renesas CPUs RZ/G2H, RZ/G2M, or RZ/G2N. These CPUs feature up to four Cortex®-A53 cores, up to four Cortex®-A57 cores and one Cortex®-R7 core.
The TQMaRZG2x extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
All components required for the correct function of the CPU, like LPDDR4 SDRAM, eMMC, power supply and power management are integrated on the TQMaRZG2x. All essential CPU pins are routed to the TQMaRZG2x connectors.
There are therefore no restrictions for customers using the TQMaRZG2x with respect to an integrated customised design.
The functionality of the different TQMaRZG2x is mainly determined by the features provided by the respective RZ/G2x derivative.

2.1 Block diagram

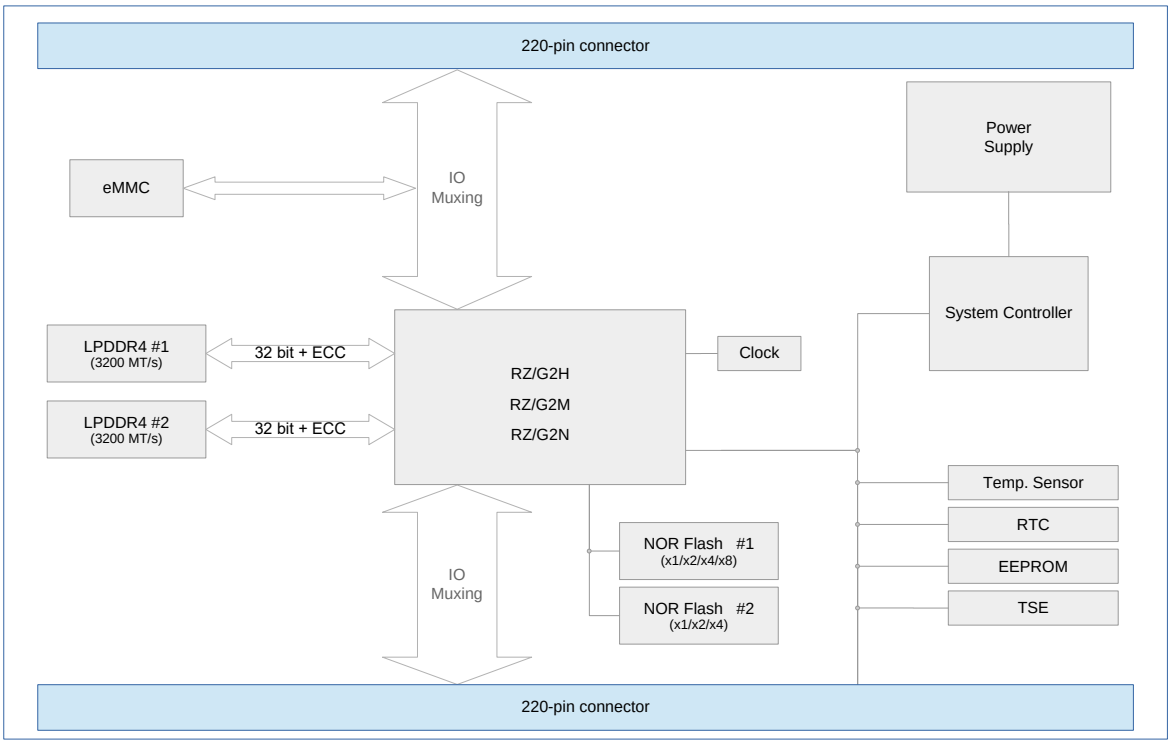

Figure 1: Block diagram TQMaRZG2x (simplified)

2.2 Functions and characteristics

The TQMaRZG2x provides the following key functions and characteristics:

- CPU derivatives RZ/G2H, RZ/G2M, RZ/G2N
- Up to 8 Gbyte of LPDDR4 SDRAM, optional with In-Line ECC
- Up to 64 Gbyte of eMMC NAND flash (assembly option)
- Up to 512 Mbyte of QSPI NOR flash (assembly option)
- RTC (assembly option)
- 64 Kbit EEPROM (assembly option)
- Secure Element SE050 (assembly option)
- Temperature sensor including EEPROM
- System Controller for reset control, power sequencing and power management, voltage supervision
- Voltage regulators and oscillators for all voltages and clocks used on the TQMaRZG2x
- All essential RZ/G2x signals routed to board-to-board connectors
- 5 V single supply
- Dimensions of 77 mm × 50 mm

3. ELECTRONICS

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

When using the processor signals the multiple pin configurations by different processor-internal function units must be taken note of. The pin assignment in Table 4 and Table 5 refers to the BSP provided by TQ-Systems in combination with the MBaRZG2x.

Attention: Destruction or malfunction	
	Depending on the configuration many RZ/G2x pins can provide several different functions. Please take note of the information concerning the configuration of these pins in (1), before integration or start-up of your carrier board / Starterkit. RFU: Reserved pins without function. To support future module revisions, these pins must not be connected.

3.1.2 Impedances

By default, all signals have a single-ended impedance of nominal 50 Ω ±10 %. Depending on the interface, other impedances are also used on the TQMaRZG2x. The following table shows the affected interfaces:

Table 2: Impedances

Interface	Signal type	Impedance TQMaRZG2x	Recommendation for carrier board
CSI	Clock + data	100 Ω differential	100 Ω ±10 % differential
HDMI	Clock + data	100 Ω differential	100 Ω ±10 % differential
LVDS	Clock + data	100 Ω differential	100 Ω ±10 % differential
PCIe	Clock	100 Ω differential	100 Ω ±10 % differential
PCIe / SATA	Data	90 Ω differential	90 Ω ±10 % differential
USB 2.0	Data	90 Ω differential	90 Ω ±10 % differential
USB 3.0	Clock	100 Ω differential	100 Ω ±10 % differential
	Data	90 Ω differential	90 Ω ±10 % differential

3.1.3 Track length

The following table shows the track lengths of critical TQMaRZG2x interfaces:

Table 3: Track lengths

Interface	**Signal**	**RZ/G2x ball to TQMaRZG2x connector [mm]**
USB 3.0	RX	22.7
	TX	23.2
	CLK	19.8
PCIe0	RX	24.0
	TX	24.9
	CLK	28.6
PCIe1	RX	34.8
	TX	36.4
	CLK	42.4
LVDS	CH[3:0]	26.0
	CLK	26.0
HDMI	DATA[2:0]	35.0
	CLK	35.0
CSI0	DATA[3:0]	17.5
	CLK	17.5
CSI1	DATA[3:0]	14.0
	CLK	14.0

3.1.4 Pinout TQMaRZG2x

Table 4: Pinout connector X1

Dir.	Level	Group	Signal	X1		Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	–
I	5 V	Power	V_5V_IN	A2	B2	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A3	B3	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A4	B4	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A5	B5	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A6	B6	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A7	B7	V_5V_IN	Power	5 V	I
I	5 V	Power	V_5V_IN	A8	B8	V_5V_IN	Power	5 V	I
–	0 V	Ground	DGND	A9	B9	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A10	B10	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A12	B12	DGND	Ground	0 V	–
O	1.8 V	Power	V_1V8	A13	B13	V_3V3	Power	3.3 V	O
O	1.8 V	Power	V_1V8	A14	B14	V_3V3	Power	3.3 V	O
–	0 V	Ground	DGND	A15	B15	DGND	Ground	0 V	–
O	1.8 V	HDMI	HDMI0_TMDS_DATA2_P	A16	B16	HDMI0_TMDS_DATA1_P	HDMI	1.8 V	O
O	1.8 V	HDMI	HDMI0_TMDS_DATA2_N	A17	B17	HDMI0_TMDS_DATA1_N	HDMI	1.8 V	O
–	0 V	Ground	DGND	A18	B18	DGND	Ground	0 V	–
O	1.8 V	HDMI	HDMI0_TMDS_CLK_P	A19	B19	HDMI0_TMDS_DATA0_P	HDMI	1.8 V	O
O	1.8 V	HDMI	HDMI0_TMDS_CLK_N	A20	B20	HDMI0_TMDS_DATA0_N	HDMI	1.8 V	O
–	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	–
I	5 V	HDMI	HDMI0_HPD	A22	B22	HDMI0_SCL	HDMI	1.8 / 3.3 V	O
IO	3.3 V	GPIO	GP7_02	A23	B23	HDMI0_SDA	HDMI	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A24	B24	DGND	Ground	0 V	–
O	1.8 V	LVDS	LVDS0_CH2_P	A25	B25	LVDS0_CH0_P	LVDS	1.8 V	O
O	1.8 V	LVDS	LVDS0_CH2_N	A26	B26	LVDS0_CH0_N	LVDS	1.8 V	O
–	0 V	Ground	DGND	A27	B27	DGND	Ground	0 V	–
O	1.8 V	LVDS	LVDS0_CH3_P	A28	B28	LVDS0_CH1_P	LVDS	1.8 V	O
O	1.8 V	LVDS	LVDS0_CH3_N	A29	B29	LVDS0_CH1_N	LVDS	1.8 V	O
–	0 V	Ground	DGND	A30	B30	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI0_DATA0_P	A32	B32	LVDS0_CLK_P	LVDS	1.8 V	O
I	1.8 V	CSI	CSI0_DATA0_N	A33	B33	LVDS0_CLK_N	LVDS	1.8 V	O
–	0 V	Ground	DGND	A34	B34	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI0_DATA2_P	A35	B35	CSI0_DATA1_P	CSI	1.8 V	I
I	1.8 V	CSI	CSI0_DATA2_N	A36	B36	CSI0_DATA1_N	CSI	1.8 V	I
–	0 V	Ground	DGND	A37	B37	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI0_CLK_P	A38	B38	CSI0_DATA3_P	CSI	1.8 V	I
I	1.8 V	CSI	CSI0_CLK_N	A39	B39	CSI0_DATA3_N	CSI	1.8 V	I
–	0 V	Ground	DGND	A40	B40	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	–
I	1.8 V	CSI	CSI1_CLK_P	A42	B42	CSI1_DATA0_P	CSI	1.8 V	I
I	1.8 V	CSI	CSI1_CLK_N	A43	B43	CSI1_DATA0_N	CSI	1.8 V	I
–	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	–
I	1.8 V	DU	DU_DOT_CLK2_IN	A45	B45	CSI1_DATA1_P	CSI	1.8 V	I
–	0 V	Ground	DGND	A46	B46	CSI1_DATA1_N	CSI	1.8 V	I
I	1.8 V	DU	DU_DOT_CLK1_IN	A47	B47	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A48	B48	SDA4	I2C	1.8 V	IO
I	1.8 V	DU	DU_DOT_CLK0_IN	A49	B49	SCL4	I2C	1.8 V	O
–	0 V	Ground	DGND	A50	B50	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–
O	3.3 V	LBSC	CLKOUT	A52	B52	RD_WR#	LBSC	3.3 V	O
–	0 V	Ground	DGND	A53	B53	BS#	LBSC	3.3 V	O
IO	3.3 V	IIC_DVFS	IIC_DVFS_SDA	A54	B54	WE0#	LBSC	3.3 V	O
O	3.3 V	IIC_DVFS	IIC_DVFS_SCL	A55	B55	WE1#	LBSC	3.3 V	O

3.1.4 Pinout TQMaRZG2x (continued)

Table 4: Pinout connector X1 (continued)

Dir.	Level	Group	Signal	X1		Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A56	B56	RD#	LBSC	3.3 V	O
O	3.3 V	GPIO	AVS1	A57	B57	CS1#	LBSC	3.3 V	O
O	3.3 V	GPIO	AVS2	A58	B58	CS0#	LBSC	3.3 V	O
IO	3.3 V	GPIO	GP7_03	A59	B59	EX_WAIT0_A	LBSC	3.3 V	I
–	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	–
O	3.3 V	LBSC	A0	A61	B61	D0	LBSC	3.3 V	IO
O	3.3 V	LBSC	A1	A62	B62	D1	LBSC	3.3 V	IO
O	3.3 V	LBSC	A2	A63	B63	D2	LBSC	3.3 V	IO
O	3.3 V	LBSC	A3	A64	B64	D3	LBSC	3.3 V	IO
O	3.3 V	LBSC	A4	A65	B65	D4	LBSC	3.3 V	IO
O	3.3 V	LBSC	A5	A66	B66	D5	LBSC	3.3 V	IO
O	3.3 V	LBSC	A6	A67	B67	D6	LBSC	3.3 V	IO
O	3.3 V	LBSC	A7	A68	B68	D7	LBSC	3.3 V	IO
O	3.3 V	LBSC	A8	A69	B69	D8	LBSC	3.3 V	IO
–	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	–
O	3.3 V	LBSC	A9	A71	B71	D9	LBSC	3.3 V	IO
O	3.3 V	LBSC	A10	A72	B72	D10	LBSC	3.3 V	IO
O	3.3 V	LBSC	A11	A73	B73	D11	LBSC	3.3 V	IO
O	3.3 V	LBSC	A12	A74	B74	D12	LBSC	3.3 V	IO
O	3.3 V	LBSC	A13	A75	B75	D13	LBSC	3.3 V	IO
O	3.3 V	LBSC	A14	A76	B76	D14	LBSC	3.3 V	IO
O	3.3 V	LBSC	A15	A77	B77	D15	LBSC	3.3 V	IO
O	3.3 V	LBSC	A16	A78	B78	DGND	Ground	0 V	–
O	3.3 V	LBSC	A17	A79	B79	IRQ0	INTC	3.3 V	I
–	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	–
O	3.3 V	LBSC	A18	A81	B81	IRQ1	INTC	3.3 V	I
O	3.3 V	LBSC	A19	A82	B82	IRQ2	INTC	3.3 V	I
–	0 V	Ground	DGND	A83	B83	IRQ3	INTC	3.3 V	I
I	3.3 V	INTC	IRQ5	A84	B84	IRQ4	INTC	3.3 V	I
O	3.3 V	PWM	PWM	A85	B85	DGND	Ground	0 V	–
O	3.3 V	PWM	PWM1_A	A86	B86	AVB_TXCREFCLK	EtherAVB	3.3 V	I
O	3.3 V	PWM	PWM2_A	A87	B87	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A88	B88	AVB_TX_CTL	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RXC	A89	B89	AVB_TXC	EtherAVB	2.5 V	O
–	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	–
I	2.5 V	EtherAVB	AVB_RX_CTL	A91	B91	AVB_TD0	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD0	A92	B92	AVB_TD1	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD1	A93	B93	AVB_TD2	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD2	A94	B94	AVB_TD3	EtherAVB	2.5 V	O
I	2.5 V	EtherAVB	AVB_RD3	A95	B95	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A96	B96	AVB_MDIO	EtherAVB	3.3 V	IO
O	3.3 V	EtherAVB	AVB_MAGIC	A97	B97	AVB_MDC	EtherAVB	3.3 V	O
I	3.3 V	EtherAVB	AVB_PHY_INT	A98	B98	DGND	Ground	0 V	–
I	3.3 V	EtherAVB	AVB_LINK	A99	B99	RPC_INT#	RPC	1.8 V	I
–	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	–
O	3.3 V	EtherAVB	AVB_AVTP_MATCH_A	A101	B101	RPC_WP#	RPC	1.8 V	O
I	3.3 V	EtherAVB	AVB_AVTP_CAPTURE_A	A102	B102	RPC_RESET#	RPC	1.8 V	O
–	0 V	Ground	DGND	A103	B103	DGND	Ground	0 V	–
O	1.8 V	QSPI	QSPI1_CLK_CON	A104	B104	QSPI0_CLK_CON	QSPI	1.8 V	O
IO	1.8 V	QSPI	QSPI1_IO0_CON	A105	B105	QSPI0_IO0_CON	QSPI	1.8 V	IO
IO	1.8 V	QSPI	QSPI1_IO1_CON	A106	B106	QSPI0_IO1_CON	QSPI	1.8 V	IO
IO	1.8 V	QSPI	QSPI1_IO2_CON	A107	B107	QSPI0_IO2_CON	QSPI	1.8 V	IO
IO	1.8 V	QSPI	QSPI1_IO3_CON	A108	B108	QSPI0_IO3_CON	QSPI	1.8 V	IO
O	1.8 V	QSPI	QSPI1_SS#_CON	A109	B109	QSPI0_SS#_CON	QSPI	1.8 V	O
–	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	–

3.1.4 Pinout TQMaRZG2x (continued)

Table 5: Pinout connector X2

Dir.	Level	Group	Signal	X2		Signal	Group	Level	Dir.
–	0 V	Ground	DGND	A1	B1	DGND	Ground	0 V	–
I	0.8 V	PCIE	PCIE1_CLK_P	A2	B2	PCIE0_CLK_P	PCIE	0.8 V	I
I	0.8 V	PCIE	PCIE1_CLK_M	A3	B3	PCIE0_CLK_M	PCIE	0.8 V	I
–	0 V	Ground	DGND	A4	B4	DGND	Ground	0 V	–
O	0.8 V	PCIE	PCIE1_TX_P	A5	B5	PCIE0_TX_P	PCIE	0.8 V	O
O	0.8 V	PCIE	PCIE1_TX_M	A6	B6	PCIE0_TX_M	PCIE	0.8 V	O
–	0 V	Ground	DGND	A7	B7	DGND	Ground	0 V	–
I	0.8 V	PCIE	PCIE1_RX_P	A8	B8	PCIE0_RX_P	PCIE	0.8 V	I
I	0.8 V	PCIE	PCIE1_RX_M	A9	B9	PCIE0_RX_M	PCIE	0.8 V	I
–	0 V	Ground	DGND	A10	B10	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A11	B11	DGND	Ground	0 V	–
O	0.8 V	USB 3.0	USB3S0_TX_P	A12	B12	USB3HS0_DP	USB 3.0	3.3 V	IO
O	0.8 V	USB 3.0	USB3S0_TX_M	A13	B13	USB3HS0_DM	USB 3.0	3.3 V	IO
–	0 V	Ground	DGND	A14	B14	DGND	Ground	0 V	–
I	0.8 V	USB 3.0	USB3S0_RX_P	A15	B15	USB3S0_CLK_P	USB 3.0	0.8 V	I
I	0.8 V	USB 3.0	USB3S0_RX_M	A16	B16	USB3S0_CLK_M	USB 3.0	0.8 V	I
–	0 V	Ground	DGND	A17	B17	DGND	Ground	0 V	–
IO	3.3 V	USB 2.0	DP1	A18	B18	DP0	USB 2.0	3.3 V	IO
IO	3.3 V	USB 2.0	DM1	A19	B19	DM0	USB 2.0	3.3 V	IO
–	0 V	Ground	DGND	A20	B20	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A21	B21	DGND	Ground	0 V	–
I	3.3 V	USB 2.0	ID1	A22	B22	VBUS0	USB 2.0	5 V	I
O	3.3 V	USB 2.0	USB1_PWEN	A23	B23	ID0	USB 2.0	3.3 V	I
I	3.3 V	USB 2.0	USB1_OVC	A24	B24	USB0_PWREN	USB 2.0	3.3 V	O
I	5 V	USB 3.0	USB3HS0_VBUS	A25	B25	USB0_OVC	USB 2.0	3.3 V	I
I	3.3 V	USB 3.0	USB3HS0_ID	A26	B26	DGND	Ground	0 V	–
O	3.3 V	USB 3.0	USB30_PWEN	A27	B27	SD3_DAT3_CON	SD	1.8 / 3.3 V	IO
I	3.3 V	USB 3.0	USB30_OVC	A28	B28	SD3_DAT2_CON	SD	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A29	B29	SD3_DAT1_CON	SD	1.8 / 3.3 V	IO
O	1.8 / 3.3 V	SD	SD3_CLK_CON	A30	B30	SD3_DAT0_CON	SD	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A31	B31	DGND	Ground	0 V	–
IO	1.8 / 3.3 V	SD	SD3_DAT7_CON	A32	B32	SD3_DS_CON	SD	1.8 / 3.3 V	I
IO	1.8 / 3.3 V	SD	SD3_DAT6_CON	A33	B33	SD3_CMD_CON	SD	1.8 / 3.3 V	IO
IO	1.8 / 3.3 V	SD	SD3_DAT5_CON	A34	B34	RTC_INT_OUT#	RTC	3.3 V	O
IO	1.8 / 3.3 V	SD	SD3_DAT4_CON	A35	B35	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A36	B36	TRST#	DBG	1.8 V	I
I	3.3 V	RTC	V_BAT	A37	B37	TDI	DBG	1.8 V	I
–	0 V	Ground	DGND	A38	B38	TMS	DBG	1.8 V	I
I	3.3 V	SYSC	SWD_CLK	A39	B39	ASEBRK	DBG	1.8 V	IO
IO	3.3 V	SYSC	SWD_DIO	A40	B40	TDO	DBG	1.8 V	O
–	0 V	Ground	DGND	A41	B41	DGND	Ground	0 V	–
O	3.3 V	RESET	TQMARZG_RST_OUT#	A42	B42	TCK	DBG	1.8 V	I
I	3.3 V	RESET	TQMARZG_RST_IN#	A43	B43	JTAG_SRST#	SYSC	3.3 V	I
–	0 V	Ground	DGND	A44	B44	DGND	Ground	0 V	–
O	3.3 V	SYSC	PGOOD	A45	B45	USB_EXTAL_CON	USB	1.8 V	I
O	3.3 V	SYSC	BOOT_CFG#	A46	B46	DGND	Ground	0 V	–
–	–	RESERVED	RFU0	A47	B47	SYSC_UART0_TX	SYSC	3.3 V	O
–	–	RESERVED	RFU1	A48	B48	SYSC_UART0_RX	SYSC	3.3 V	I
–	–	RESERVED	RFU2	A49	B49	DGND	Ground	0 V	–
I	1.8 V	INTC	NMI	A50	B50	EXTALR_CON	CPG	1.8 V	I
–	0 V	Ground	DGND	A51	B51	DGND	Ground	0 V	–
IO	3.3 V	GPIO	GP6_30	A52	B52	FSCLKST#	CPG	1.8 V	O
IO	3.3 V	GPIO	GP6_31	A53	B53	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A54	B54	AUDIO_CLKB_B	ADG	3.3 V	I
IO	3.3 V	SSI	SSI_SDATA9_A	A55	B55	DGND	Ground	0 V	–

3.1.4 Pinout TQMaRZG2x (continued)

Table 5: Pinout connector X2 (continued)

Dir.	Level	Group	Signal	X2		Signal	Group	Level	Dir.
IO	3.3 V	SSI	SSI_SDATA8	A56	B56	AUDIO_CLKA_A	ADG	3.3 V	I
IO	3.3 V	SSI	SSI_SDATA7	A57	B57	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA6	A58	B58	SSI_SCK5	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_SDATA5	A59	B59	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A60	B60	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA4	A61	B61	SSI_SCK6	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_SDATA3	A62	B62	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA2_A	A63	B63	SSI_SCK78	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_SDATA1_A	A64	B64	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_SDATA0	A65	B65	SSI_SCK4	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_WS78	A66	B66	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_WS5	A67	B67	SSI_SCK349	SSI	3.3 V	IO
IO	3.3 V	SSI	SSI_WS6	A68	B68	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_WS4	A69	B69	SSI_SCK01239	SSI	3.3 V	IO
–	0 V	Ground	DGND	A70	B70	DGND	Ground	0 V	–
IO	3.3 V	SSI	SSI_WS349	A71	B71	VDDQVA_SD0	SD	1.8 / 3.3 V	I
IO	3.3 V	SSI	SSI_WS01239	A72	B72	VDDQVA_SD1	SD	1.8 / 3.3 V	I
O	3.3 V	TEMP	EVENT_TEMPSENSOR#	A73	B73	VDDQVA_SD2	SD	1.8 / 3.3 V	I
I	3.3 V	EEPROM	EEPROM_WP	A74	B74	VDDQVA_SD3	SD	1.8 / 3.3 V	I
O	3.3 V	SCIF	TX0	A75	B75	DGND	Ground	0 V	–
I	3.3 V	SCIF	RX0	A76	B76	SCK2	SCIF	3.3 V	O
IO	3.3 V	SCIF	CTS0#	A77	B77	DGND	Ground	0 V	–
IO	3.3 V	SCIF	RTS0#	A78	B78	TX2_A	SCIF	3.3 V	O
O	3.3 V	SCIF	SCK0	A79	B79	RX2_A	SCIF	3.3 V	I
–	0 V	Ground	DGND	A80	B80	DGND	Ground	0 V	–
O	3.3 V	SCIF	TX1_A	A81	B81	MLB_CLK	MLB	3.3 V	I
I	3.3 V	SCIF	RX1_A	A82	B82	MLB_DAT	MLB	3.3 V	IO
IO	3.3 V	SCIF	CTS1#	A83	B83	MLB_SIG	MLB	3.3 V	IO
IO	3.3 V	SCIF	RTS1#	A84	B84	HRTS0#	HSCIF	3.3 V	IO
IO	3.3 V	MSIOF	MSIOF0_SYNC	A85	B85	HCTS0#	HSCIF	3.3 V	IO
O	3.3 V	MSIOF	MSIOF0_TXD	A86	B86	HRX0	HSCIF	3.3 V	I
I	3.3 V	MSIOF	MSIOF0_RXD	A87	B87	HTX0	HSCIF	3.3 V	O
O	3.3 V	MSIOF	MSIOF0_SS1	A88	B88	DGND	Ground	0 V	–
O	3.3 V	MSIOF	MSIOF0_SS2	A89	B89	HSCK0	HSCIF	3.3 V	I
–	0 V	Ground	DGND	A90	B90	DGND	Ground	0 V	–
O	3.3 V	MSIOF	MSIOF0_SCK	A91	B91	SD1_DAT0	SD	1.8 / 3.3 V	IO
–	0 V	Ground	DGND	A92	B92	SD1_DAT1	SD	1.8 / 3.3 V	IO
I	3.3 V	SD	SD0_WP	A93	B93	SD1_DAT2	SD	1.8 / 3.3 V	IO
I	3.3 V	SD	SD0_CD	A94	B94	SD1_DAT3	SD	1.8 / 3.3 V	IO
IO	1.8 / 3.3 V	SD	SD0_CMD	A95	B95	SD1_CD	SD	3.3 V	I
IO	1.8 / 3.3 V	SD	SD0_DAT0	A96	B96	SD1_WP	SD	3.3 V	I
IO	1.8 / 3.3 V	SD	SD0_DAT1	A97	B97	SD1_CMD	SD	1.8 / 3.3 V	IO
IO	1.8 / 3.3 V	SD	SD0_DAT2	A98	B98	DGND	Ground	0 V	–
IO	1.8 / 3.3 V	SD	SD0_DAT3	A99	B99	SD1_CLK	SD	1.8 / 3.3 V	O
–	0 V	Ground	DGND	A100	B100	DGND	Ground	0 V	–
O	1.8 / 3.3 V	SD	SD0_CLK	A101	B101	DGND	Ground	0 V	–
–	0 V	Ground	DGND	A102	B102	SD2_DAT0	SD	1.8 / 3.3 V	IO
I	3.3 V	SECURE	SE_ENABLE	A103	B103	SD2_DAT1	SD	1.8 / 3.3 V	IO
IO	3.3 V	SECURE	SE_7816_IO1	A104	B104	SD2_DAT2	SD	1.8 / 3.3 V	IO
IO	3.3 V	SECURE	SE_7816_IO2	A105	B105	SD2_DAT3	SD	1.8 / 3.3 V	IO
I	3.3 V	SECURE	SE_7816_RST#	A106	B106	SD2_CMD	SD	1.8 / 3.3 V	IO
IO	3.3 V	SECURE	SE_14443_LA	A107	B107	SD2_DS	SD	1.8 / 3.3 V	I
IO	3.3 V	SECURE	SE_14443_LB	A108	B108	DGND	Ground	0 V	–
O	3.3 V	SECURE	SE_7816_CLK	A109	B109	SD2_CLK	SD	1.8 / 3.3 V	O
–	0 V	Ground	DGND	A110	B110	DGND	Ground	0 V	–

3.2 Boot source

The boot source is selected via the boot strapping pins of the RZ/G2x. All signals are routed to the TQMaRZG2x connectors.

After the release of PRESET# the configuration is read in. Depending on the boot device the RZ/G2x may read the data directly from the boot device or the RZ/G2x boots from its on-chip boot ROM and loads the IPL into the internal RAM.

It is recommended to switch the boot strap pins to high impedance after read-in.

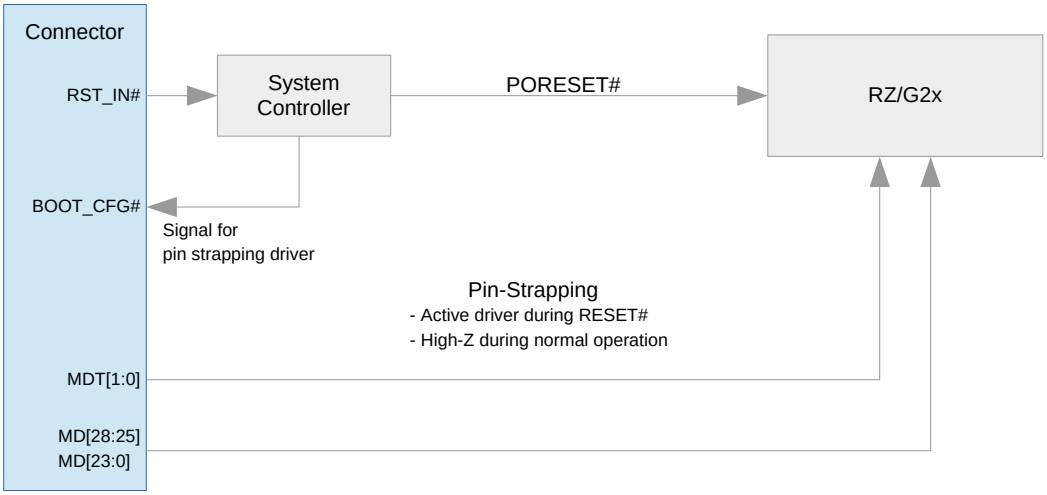

Figure 2: Block diagram boot strapping

Table 6: Boot source selection

X1-B67	X1-B66	X1-B64	X1-B63	Boot source	Boot interface
MD4	MD3	MD2	MD1		
0	1	0	0	NOR flash	QSPI
1	1	0	1	eMMC	SDHI3
1	1	1	0	USB download	USB2_CH0
1	1	1	1	SCIF download	SCIF2

Note: Field software updates	
	When designing a carrier board, it is recommended to include an interface for software updates in the field.

3.2 Boot source (continued)

Table 7: General boot settings

Boot config pin	TQMaRZG2x	Setting	Remark
MDT1	X1-B56	JTAG section. More information in (1) and (2).	Don't care
MDT0	X1-B53		
MD28	X1-A61	0 – RCLK from inside 1 – RCLK from EXTALR	1
MD27	X1-A62	00 – LPDDR4 Other settings are prohibited	00
MD22	X1-A68		
MD26	X1-A64	Reserved, fixed to 0	0
MD25	X1-A65	Reserved, fixed to 0	0
MD23	X1-A67	Reserved, fixed to 0	0
MD21	X1-A74	JTAG section. More information in (1) and (2).	Don't care
MD20	X1-A72		
MD11	X1-B65		
MD10	X1-B75		
MD19	X1-A75	00 – DDR3200 01 – DDR2800 10 – Setting prohibited 11 – DDR1600	00
MD17	X1-A77		
MD18	X1-A76	0 – PLL1 division ratio: 1/24 1 – PLL1 division ratio: 1/36	0
MD16	X1-A78	Reserved, fixed to 1	1
MD15	X1-A79	0 – AArch32 1 – AArch64	1
MD14	X1-A81	EXTAL Select: 00 – 16.66 MHz 01 – 20.00 MHz 10 – 25.00 MHz 11 – 33.33 MHz	10
MD13	X1-A82		
MD12	X1-B69	0 – PCIe 1 – SATA	RZ/G2M – 0 (fixed) RZ/G2H or N – don't care
MD9	X1-B74	0 – Input of an external clock at EXTAL pin 1 – Connects the crystal to the EXTAL and XTAL pins	1
MD8	X1-B73	EXBUS Data Bus Width 0 – 8-bit 1 – 16-bit	Don't care
MD7	X1-B72	00 – Cortex-A57 boot 01 – Cortex-A53 boot 10 – Setting prohibited 11 – Setting prohibited	00
MD6	X1-B71		
MD5	X1-B68	0 – Setting prohibited 1 – Normal boot	1
MD0	X1-B62	Reserved, fixed to 0	0

3.3 System components

3.3.1 RZ/G2x

3.3.1.1 RZ/G2x variants, block diagrams

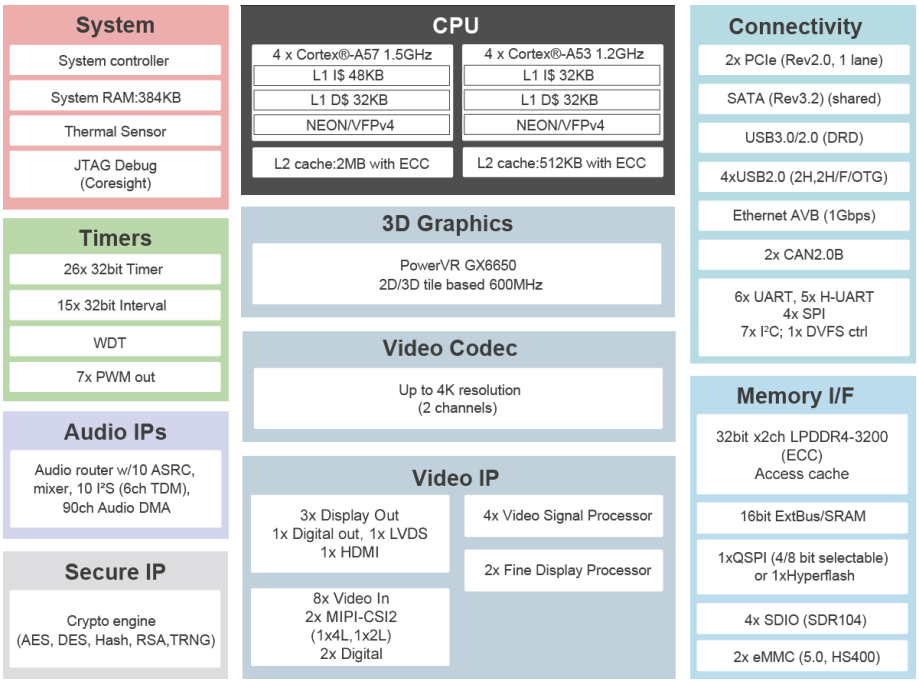

Figure 3: Block diagram RZ/G2H
(Source: Renesas)

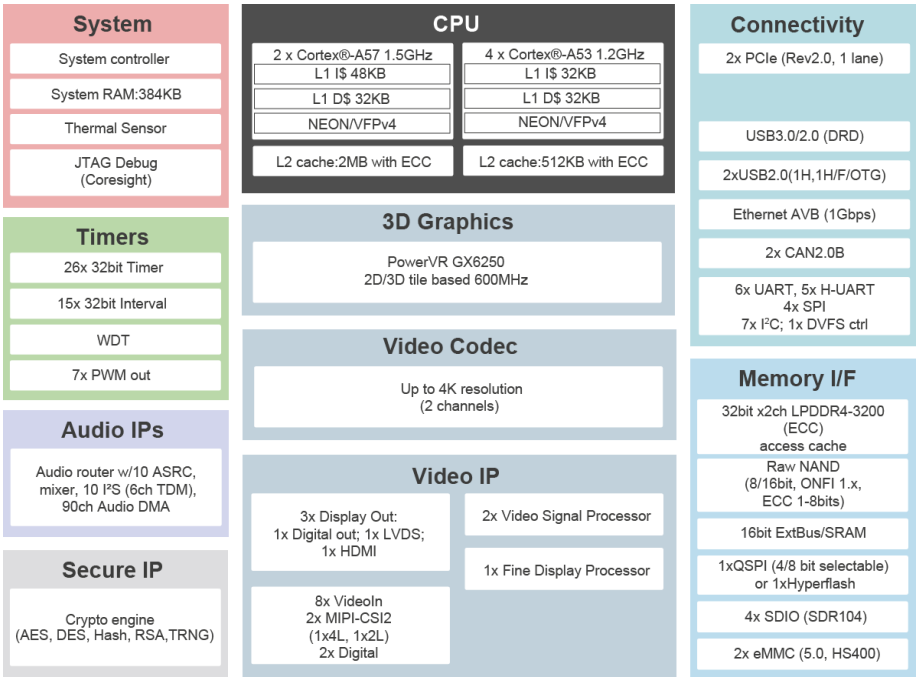

Figure 4: Block diagram RZ/G2M
(Source: Renesas)

3.3.1.1 RZ/G2x variants, block diagrams (continued)

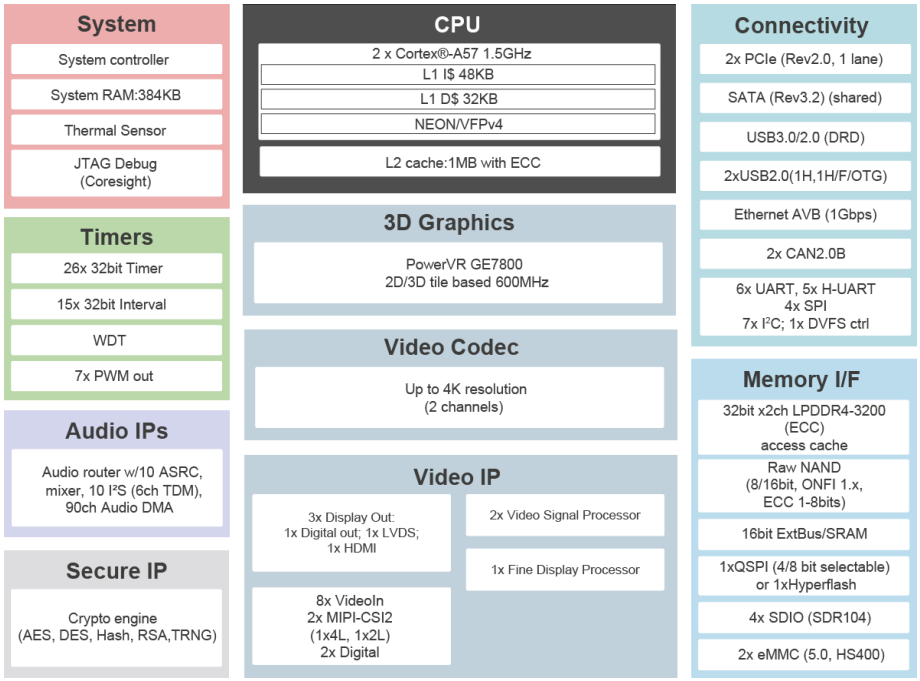

Figure 5: Block diagram RZ/G2N
(Source: Renesas)

3.3.1.2 RZ/G2x variants, details

The following table shows the features provided by the different RZ/G2x variants.
Fields with a red background indicate differences, fields with a green background indicate identical features.

Table 8: RZ/G2x variants

Feature	RZ/G2H	RZ/G2M	RZ/G2N
ARM® Cortex®-A	4× Cortex®-A57@1.5 GHz 4× Cortex®-A53@1.2 GHz L1, L2 Parity/ECC	2× Cortex®-A57@1.5 GHz 4× Cortex®-A53@1.2 GHz L1, L2 Parity/ECC	2× Cortex®-A57@1.5 GHz – L1, L2 Parity/ECC
ARM® Cortex®-R	1× Cortex®-R7@800 MHz L1, TCM w/ECC	1× Cortex®-R7@800 MHz L1, TCM w/ECC	1× Cortex®-R7@800 MHz L1, TCM w/ECC
SDRAM I/F	32-bit × 2 ch LPDDR4(3200) w/ECC	32-bit × 2 ch LPDDR4(3200) w/ECC	32-bit × 1 ch LPDDR4(3200) w/ECC
Video in	2× MIPI CSI2, 2× Digital (RGB/YCbCr), up to 8 input image can be captured	2× MIPI CSI2, 2× Digital (RGB/YCbCr), up to 8 input image can be captured	2× MIPI CSI2, 2× Digital (RGB/YCbCr), up to 8 input image can be captured
Video Codec	Support up to 4k resolutions Decoding: H.265 Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265 Encoding and Decoding: H.264	Support up to 4k resolutions Decoding: H.265 Encoding and Decoding: H.264
3D GFX	PowerVR GX6650@600 MHz	PowerVR GX6250@600 MHz	PowerVR GE7800@600 MHz
Display out	1× HDMI, 1× LVDS, 1× Digital RGB	1× HDMI, 1× LVDS, 1× Digital RGB	1× HDMI, 1× LVDS, 1× Digital RGB
USB	USB 2.0, 2 ch (1H, 1H/F/OTG) USB 3.0/2.0, 1 ch (DRD)	USB 2.0, 2 ch (1H, 1H/F/OTG) USB 3.0/2.0, 1 ch (DRD)	USB 2.0, 2 ch (1H, 1H/F/OTG) USB 3.0/2.0, 1 ch (DRD)
Gbit Ethernet	1 ch	1 ch	1 ch
CAN	2 ch (support CAN FD)	2 ch (support CAN FD)	2 ch (support CAN FD)
PCIe	2 ch (Rev2.0, 1 Lane), one of the 2 ch is shared with SATA	2 ch (Rev2.0, 1 Lane)	2 ch (Rev2.0, 1 Lane), one of the 2 ch is shared with SATA
SATA	1 ch (pins shared)	–	1 ch (pins shared)

3.3.2 Memory

3.3.2.1 SDRAM

Up to 8 Gbyte of LPDDR4-3200 SDRAM can be assembled on the TQMaRZG2x, optional with In-Line ECC:

- TQMaRZG2H, TQMaRZG2M: 8 Gbyte
- TQMaRZG2N: 4 Gbyte

3.3.2.2 eMMC

The RZ/G2x provides an SDHC interface, which is connected to SDHI3.
The eMMC on the TQMaRZG2x is configured as MLC by default, but it can be configured as SLC (higher reliability, half capacity).
Please contact TQ-Support for details.
In case the eMMC is not populated on the TQMaRZG2x, a 1.8 V eMMC can be connected on the carrier board.

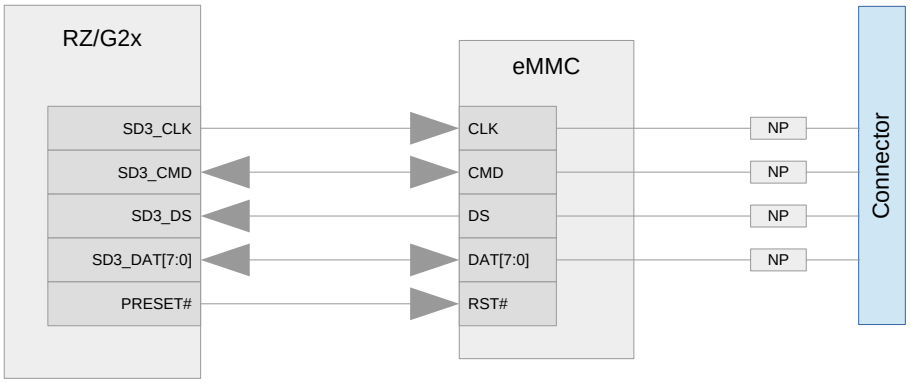

Figure 6: Block diagram eMMC interface

The TQMaRZG2x supports the following transfer modes:

Table 9: eMMC transfer modes

Mode	1-bit	4-bit	8-bit	Remark
Default Speed	–	–	–	–
High Speed	–	–	Yes	Boot process
HS200	–	–	Yes	U-Boot
HS400	–	–	Yes	Linux

3.3.2.3 QSPI NOR

The TQMaRZG2x provides two QSPI interfaces, QSPI0 and QSPI1, which operate at 1.8 V.
The TQMaRZG2x supports three different configurations.

1. No NOR flash assembled on the TQMaRZG2x, both QSPI interfaces are available at the TQMaRZG2x connectors
2. 1 × QSPI NOR flash assembled on the TQMaRZG2x
3. 2 × QSPI NOR flash assembled on the TQMaRZG2x

3.3.2.4 EEPROM

Two EEPROMs can be assembled on the TQMaRZG2x. Both EEPROMs are controlled by the IIC_DVFS bus.

- 24LC64T, 64 Kbit EEPROM (assembly option)
- SE97BTP, combined temperature sensor and 2 Kbit EEPROM

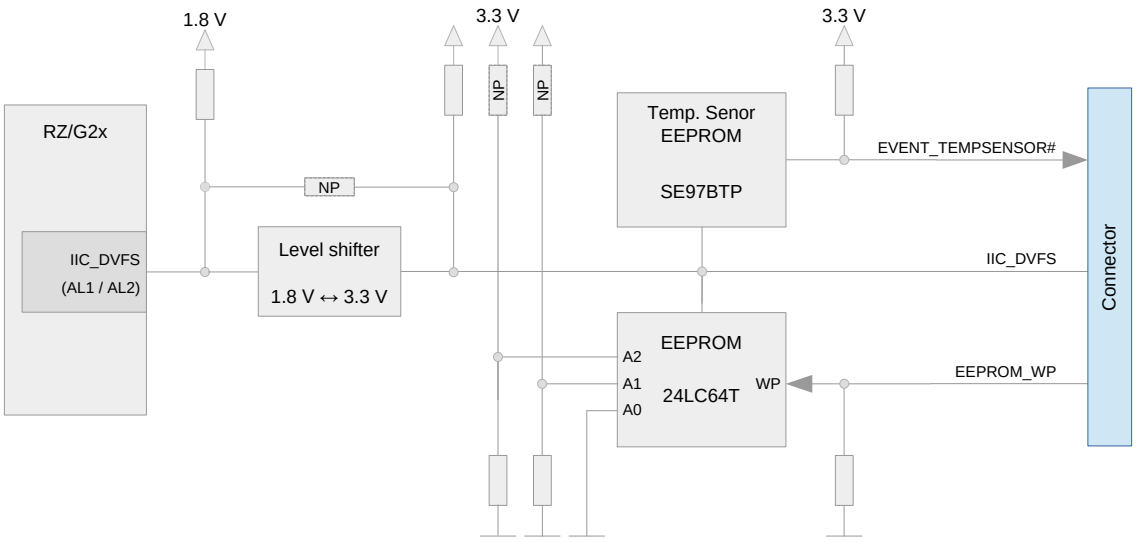

Figure 7: Block diagram EEPROMs

3.3.2.5 EEPROM 24LC64T

The EEPROM is empty on delivery. The Write Protection signal is available at the TQMaRZG2x connectors.
Read/Write is enabled by default (100 kΩ pull-down on TQMaRZG2x).

➢ The EEPROM has I²C address `0x50 / 101 0000b`

3.3.2.6 EEPROM SE97BTP

The temperature sensor SE97BTP contains a 2 Kbit (256 × 8 Bit) EEPROM. For details about the temperature sensor; see 3.3.4.
The SE97BTP is controlled by the RZ/G2x I²C bus IIC_DVFS, device addresses see Table 22. The EEPROM is divided into two parts:
The lower 128 bytes (00h to 7Fh) can be Permanent Write Protected (PWP) or Reversible Write Protected (RWP) by software.
The upper 128 bytes (80h to FFh) are not write protected and can be used for general purpose.

➢ The EEPROM in the SE97BTP has two I²C addresses:
- o EEPROM (Normal Mode): `0x57 / 101 0111b`
- o EEPROM (Protected Mode): `0x37 / 011 0111b`

The following table lists the parameters stored in the configuration EEPROM.

Table 10: EEPROM, TQMaRZG2x-specific data

Offset	Payload (byte)	Padding (byte)	Size (byte)	Type	Remark
`0x00`	–	$32_{(10)}$	$32_{(10)}$	Binary	(Not used)
`0x20`	$6_{(10)}$	$10_{(10)}$	$16_{(10)}$	Binary	MAC address
`0x30`	$8_{(10)}$	$8_{(10)}$	$16_{(10)}$	ASCII	Serial number
`0x40`	Variable	Variable	$64_{(10)}$	ASCII	Order code

3.3.3 RTC

The RTC PCF85063A (assembly option) can be supplied via V_BAT (0.9 V to 3.6 V) by a battery on the carrier board.
Signal RTC_INT is routed to the TQMaRZG2x connectors. CLKOUT is only activated if the TQMaRZG2x is supplied with 5 V.
The RTC is controlled by the I²C controller IIC_DVFS. The RTC has I²C address `0x51 / 101 0001b`.
The quartz used for the RTC on the TQMaRZG2x has a tolerance of ±20 ppm at +25 °C.
This results in an accuracy of approximately 2.6 seconds / day = 16 minutes / year.

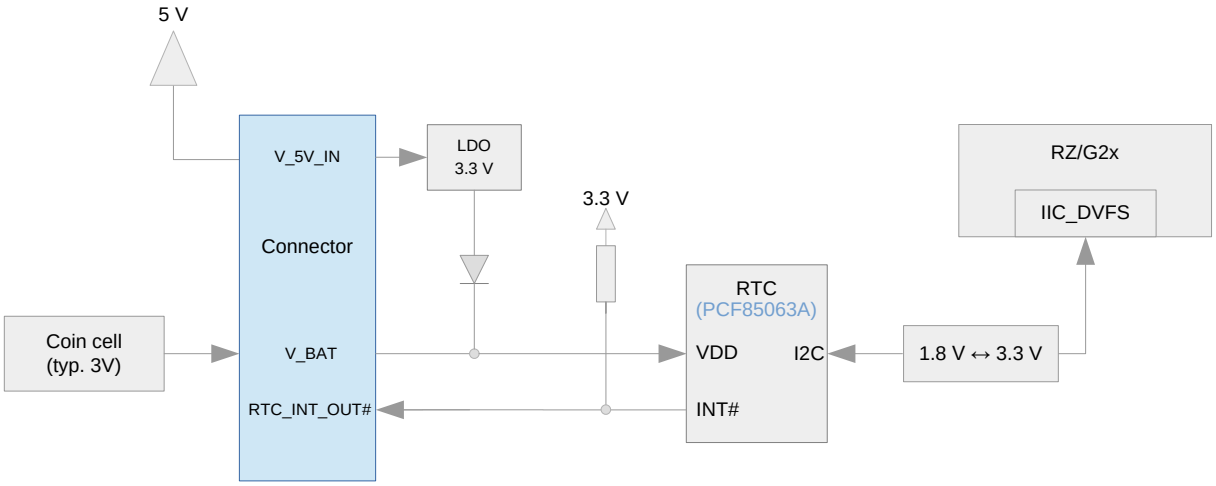

Figure 8: Block diagram RTC buffering

Attention: Destruction or malfunction, prohibited charging of coin cells	
	If the TQMaRZG2x is supplied with 5 V (V_5V_IN), V_BAT is supplied from 3.3 V generated on the TQMaRZG2x. V_BAT can be used to charge GoldCaps®. If coin cells or similar non-rechargeable sources are used, protection measures against unauthorized charging must be provided by the carrier board.

3.3.4 Temperature sensor SE97BTP

A temperature sensor SE97BTP is provided on the TQMaRZG2x. For details about the EEPROM; see 3.3.2.6.
The open-drain Alarm Output EVENT_EVENT_TEMPSENSOR# is pulled-up to 3.3 V and routed to the TQMaRZG2x connectors.
The SE97BTP is controlled by the RZ/G2x I²C bus IIC_DVFS. The following table shows details of the temperature sensor.

Table 11: Temperature sensor SE97BTP

Manufacturer	Device	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±1 °C	+75 °C to +95 °C
			Max. ±2 °C	+40 °C to +125 °C
			Max. ±3 °C	–40 °C to +125 °C

➢ The temperature sensor has I²C address `0x1F / 001 1111b`

3.3.5 Secure Element SE050

A Secure Element SE050 is available as assembly option. The SE050 is controlled by IIC_DVFS.
All six SE050 ISO_14443 (NFC Antenna) and ISO_7816 (Sensor Interface) signals are routed to the TQMaRZG2x connectors.

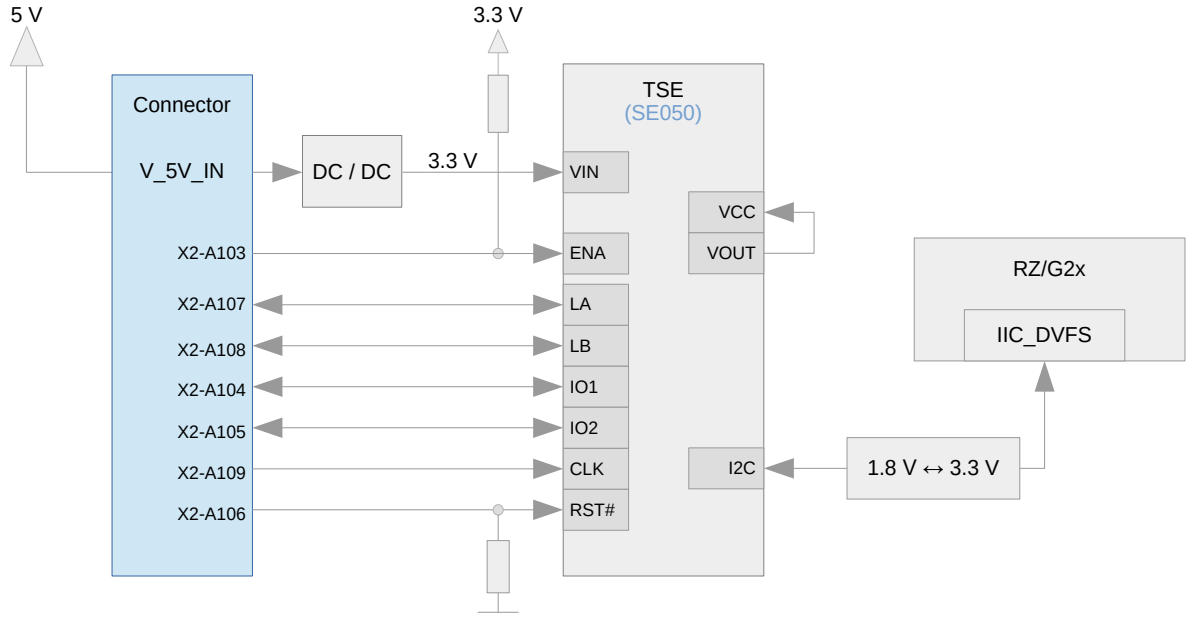

Figure 9: Block diagram SE050

➢ The Secure Element has I²C address `0x48 / 100 1000b`.

Table 12: TQMaRZG2x Reset- and Status signals

Signal	TQMaRZG2x	SE050	Remark
ENA	X2-A103	11	SE_ENABLE
LA	X2-A107	17	ISO_14443_LA
LB	X2-A108	1	ISO_14443_LB
IO1	X2-A104	3	ISO_7816_IO1
IO2	X2-A105	16	ISO_7816_IO2
CLK	X2-A109	13	ISO_7816_CLK
RST#	X2-A106	14	ISO_7816_RST#
I2C_SDA	X1-A54	9	IIC_DVFS_SDA
I2C_SCL	X1-A55	10	IIC_DVFS_SCL

3.4 Data interfaces

In general all RZ/G2x IO pins, partly also the memory interface, are provided at the TQMaRZG2x connectors.
The following chapters describe the RZ/G2x interfaces that are provided by the TQMaRZG2x in connection with the MBaRZG2x.
The interfaces are set as default in the described function and are directly routed to the TQMaRZG2x connectors.
Depending on multiplexing further, or other interfaces are possible.

3.4.1 Audio

The RZ/G2x provides up to ten audio interfaces (SSI modules).
Depending on the multiplexing, the following signals are primarily available.

Table 13: Audio signals

Signal	TQMaRZG2x	Power group
SSI_SDATA1_A	X2-A64	3.3 V
SSI_SDATA0	X2-A65	
SSI_SCK_0	X2-B69	
SSI_WS_0	X2-A72	
AUDIO_CLKOUT3	X2-A88	

3.4.2 CAN

The RZ/G2x provides two CAN controllers that support CAN-FD.
Depending on the multiplexing, the following signals are primarily available.

Table 14: CAN signals

Signal	TQMaRZG2x	Power group
CAN0_TX	X1-B79	3.3 V
CAN0_RX	X1-B81	
CAN1_TX	X1-B53	
CAN1_RX	X1-B55	

3.4.3 Clock

The RZ/G2x provides several clock inputs as well as outputs for different functions.
Depending on the multiplexing the following signals are primarily available.

Table 15: Clock signals

Signal	TQMaRZG2x	Power group	Remark
DU_DOTCLK_IN2	X1-A45	1.8 V	External clock input for DU clocks (PLL)
DU_DOTCLK_IN1	X1-A47	1.8 V	External clock input for DU clocks (PLL)
DU_DOTCLK_IN0	X1-A49	1.8 V	External clock input for DU clocks (PLL)
USB_EXTAL_CON	X2-B45	1.8 V	External clock input for USB PLL
EXTALR_CON	X2-B50	1.8 V	External clock input for RCLK
FSCLKST#	X2-B52	1.8 V	Clock output RZ/G2x
AUDIO_CLKB_A	X2-B89	3.3 V	External clock input for Audio PLL
AUDIO_CLKC_B	X2-A79	3.3 V	External clock input for Audio PLL

3.4.4 Display interfaces

The RZ/G2x offers a display unit module that can output data via an LVDS, HDMI or digital RGB interface.

3.4.4.1 24-bit RGB

Depending on the multiplexing, the following signals are primarily available.

Table 16: 24-bit RGB signals

Signal	TQMaRZG2x	Power group
DU_DB7	X1-A68	3.3 V
DU_DB6	X1-A67	
DU_DB5	X1-A66	
DU_DB4	X1-A65	
DU_DB3	X1-A64	
DU_DB2	X1-A63	
DU_DB1	X1-A62	
DU_DB0	X1-A61	
DU_DG7	X1-A77	
DU_DG6	X1-A76	
DU_DG5	X1-A75	
DU_DG4	X1-A74	
DU_DG3	X1-A82	
DU_DG2	X1-A81	
DU_DG1	X1-A79	
DU_DG0	X1-A78	
DU_DR7	X1-B77	
DU_DR6	X1-B76	
DU_DR5	X1-B75	
DU_DR4	X1-B74	
DU_DR3	X1-B73	
DU_DR2	X1-B72	
DU_DR1	X1-B71	
DU_DR0	X1-B69	
DU_DOTCLKOUT1	X1-B83	
DU_EXVSYNC	X1-A84	
DU_EXHSYNC	X1-B84	
DU_EXODDF	X1-B82	

3.4.4.2 HDMI

The RZ/G2x provides a dedicated HDMI output interface. The following signals are primarily available.

Table 17: HDMI signals

Signal	TQMaRZG2x	Power group
HDMI0_TX2_M	X1-A17	1.8 V
HDMI0_TX2_P	X1-A16	
HDMI0_TX1_M	X1-B17	
HDMI0_TX1_P	X1-B16	
HDMI0_TX0_M	X1-B20	
HDMI0_TX0_P	X1-B19	
HDMI0_CLK_M	X1-A20	
HDMI0_CLK_P	X1-A19	
HDMI0_SCL	X1-B22	1.8 V (3.3 V tolerant)
HDMI0_SDA	X1-B23	
HDMI0_HPD	X1-A22	5 V
HDMI0_CEC	X1-A23	3.3 V

3.4.4.3 LVDS

The RZ/G2x provides a dedicated LVDS interface. The following signals are primarily available.

Table 18: LVDS signals

Signal	TQMaRZG2x	Power group
LVDS0_CH3_TX_M	X1-A29	1.8 V
LVDS0_CH3_TX_P	X1-A28	
LVDS0_CH2_TX_M	X1-A26	
LVDS0_CH2_TX_P	X1-A25	
LVDS0_CH1_TX_M	X1-B29	
LVDS0_CH1_TX_P	X1-B28	
LVDS0_CH0_TX_M	X1-B26	
LVDS0_CH0_TX_P	X1-B25	
LVDS0_CLK_M	X1-B33	
LVDS0_CLK_P	X1-B32	

3.4.5 CSI

The RZ/G2x offers two CSI2 modules supporting MIPI CSI-2 V1.1 as well as MIPI D-PHY V1.1.
The following signals are primarily available.

Table 19: CSI signals

Signal	TQMaRZG2x	Power group
CSI0_DATA3_M	X1-B39	1.8 V
CSI0_DATA3_P	X1-B38	
CSI0_DATA2_M	X1-A36	
CSI0_DATA2_P	X1-A35	
CSI0_DATA1_M	X1-B36	
CSI0_DATA1_P	X1-B35	
CSI0_DATA0_M	X1-A33	
CSI0_DATA0_P	X1-A32	
CSI0_CLK_M	X1-A39	
CSI0_CLK_P	X1-A38	
CSI1_DATA1_M	X1-B46	
CSI1_DATA1_P	X1-B45	
CSI1_DATA0_M	X1-B43	
CSI1_DATA0_P	X1-B42	
CSI1_CLK_M	X1-A43	
CSI1_CLK_P	X1-A42	

3.4.6 Ethernet

The RZ/G2x offers an EthernetAVB interface which has an Ethernet controller with a MAC layer according to IEEE802.3 standard.
The following signals are primarily available.

Table 20: Ethernet signals

Signal	TQMaRZG2x	Power group
AVB_RX_CTL	X1-A91	2.5 V
AVB_RD3	X1-A95	
AVB_RD2	X1-A94	
AVB_RD1	X1-A93	
AVB_RD0	X1-A92	
AVB_RXC	X1-A89	
AVB_PHY_INT	X1-A98	
AVB_TX_CTL	X1-B88	
AVB_TXC	X1-B89	
AVB_TD3	X1-B94	
AVB_TD2	X1-B93	
AVB_TD1	X1-B92	
AVB_TD0	X1-B91	
AVB_TXCREFCLK	X1-B86	3.3 V
AVB_MDC_3V3	X1-B97	
AVB_MDIO_3V3	X1-B96	
AVB_PHY_RST#	X1-B54	

3.4.7 GPIO

The RZ/G2x offers various GPIOs, which are partially occupied by multiplexing.
The following signals are primarily available as GPIO.

Table 21: GPIOs

Signal	TQMaRZG2x	Power group
PCIE1_CLK_EN	X1-A52	3.3 V
MIKRO_BUS_INT	X1-B52	
AVS1	X1-A57	
MSIOF2_MUX_CTRL	X1-B57	
AVS2	X1-A58	
TOUCH_CTRL_INT#	X1-B58	
UART_MUX_CTRL	X1-A59	
MIKRO_BUS_RST#	X1-B59	
SEL_V_FAN	X1-B61	
PCIE0_RST#	X1-B62	
PCIE0_DISABLE#	X1-B63	
PCIE0_WAKE#	X1-B64	
LVDS0_RST#	X1-B66	
LCD_PWR_EN	X1-B67	
LCD_BLT_EN	X1-B68	
PCIE1_SATA_SEL	X1-A71	
PCIE1_RST#	X2-A23	
PCIE1_WAKE#	X2-A24	
AUDIO_CODEC_RST#	X2-A27	
PCIE1_CLK_REQ#	X2-A28	
CSI0_MCLK_OUT	X2-A52	
CSI1_MCLK_OUT	X2-A53	
M2_PEDET	X2-B54	
USER_BUTTON_1	X2-A55	
CSI0_PWR#	X2-A56	
USB30_HUB_RST#	X2-B56	
USER_LED_1	X2-A57	
USER_BUTTON_2	X2-A58	
USER_LED_2	X2-B58	
CSI1_PWR#	X2-A59	
SEL_VDDQVA_SD1	X2-A61	
USER_LED_3	X2-B61	
SEL_VDDQVA_SD0	X2-A62	
SEL_VDDQVA_SD3	X2-A63	
CSI0_RST#	X2-B63	
CSI1_TRIGGER	X2-B65	
USER_BUTTON_3	X2-A66	
CSI0_TRIGGER	X2-A67	
CSI1_SYNC	X2-B67	
CSI1_RST#	X2-A68	
SEL_VDDQVA_SD2	X2-A69	
CSI0_SYNC	X2-A71	
RGB_24BIT_18BIT_SEL	X2-B76	
LVDS0_BLT_EN	X2-A77	
LVDS0_PWR_EN	X2-A78	
SIM_CARD_DETECT	X2-A83	
DISPLAY_RST#	X2-A84	

3.4.8 I²C

The RZ/G2x offers up to seven I²C interfaces. The IIC_DVFS is used on the TQMaRZG2x. There are 2.2 kΩ pull-ups on the IIC_DVFS interface. If further I²C devices are connected to the I²C bus on the carrier board, the maximum capacitive bus load according to the I²C standard must be observed. If necessary, additional pull-ups must be provided on the carrier board.
The following figure shows the I²C bus structure on the TQMaRZG2x.

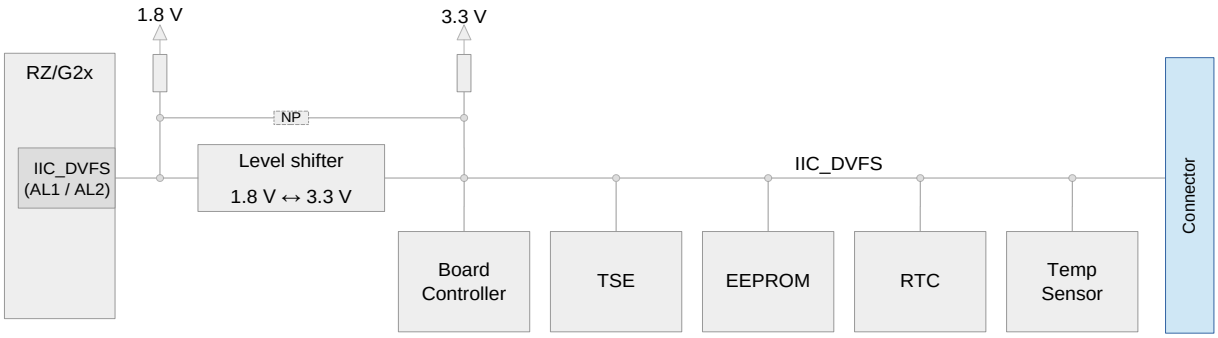

Figure 10: Block diagram I²C bus

The following table shows the addresses of all I²C devices:

Table 22: I2C1 device addresses

Device	Function	7-bit address	Remark
24LC64T	EEPROM	0x50 / 101 0000b	For general usage
MKL04Z16	System Controller	0x11 / 001 0001b	Should not be altered
PCF85063A	RTC	0x51 / 101 0001b	Assembly option
SE97BTP	Temperature sensor	0x1F / 001 1111b	Temperature
	EEPROM	0x57 / 101 0111b	Normal Mode
	EEPROM	0x37 / 011 0111b	Protected Mode
SE050	Secure Element	0x48 / 100 1000b	Assembly option

Depending on the multiplexing, the following signals are primarily available.

Table 23: I²C signals

Signal	TQMaRZG2x	Power group	Remark
IIC_DVFS_SDA	X1-A54	3.3 V	2.2 kΩ pull-up on TQMaRZG2x
IIC_DVFS_SCL	X1-A55		2.2 kΩ pull-up on TQMaRZG2x
I2C4_SDA	X1-B48	1.8 V	–
I2C4_SCL	X1-B49		–
I2C6_SDA	X1-A69	3.3 V	–
I2C6_SCL	X1-A73		–

3.4.9 Interrupt Controller

The RZ/G2x provides an interrupt controller with six IRQ, as well as an NMI interrupt.
The NMI (INTC) works at 1.8 V and is routed to X2-A50.

3.4.10 JTAG®

The RZ/G2x provides three 5-pin JTAG and SWD interfaces. JTAG2 and JTAG3 are additional debug ports that can be used by multiplexing. Depending on the multiplexing and MD pins, a different TAP controller can be selected. The primary JTAG interface JTAG1 is available directly on the TQMaRZG2x connector.

A default pull-up configuration is available on the TQMaRZG2x. Accordingly, the connector with wiring must be provided on the carrier board. The following figure shows the JTAG interface on the module.

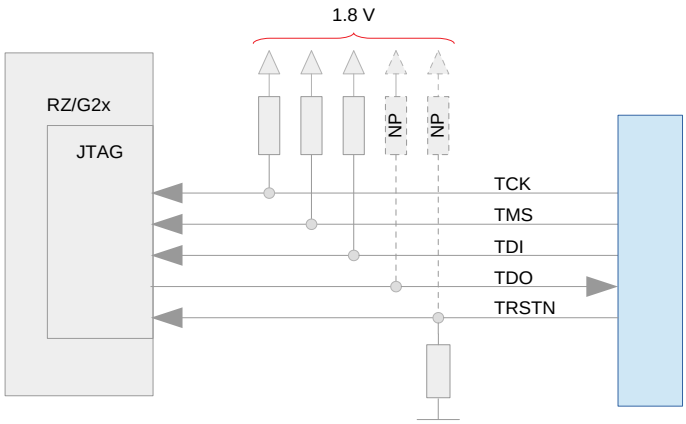

Figure 11: Block diagram JTAG

The following signals are primarily available.

Table 24: JTAG signals

Signal	TQMaRZG2x	Power group	Remark
JTAG_TCK	X2-B42	VDDQ18 (1.8 V)	10 kΩ pull-up on TQMaRZG2x
JTAG_TDI	X2-B37		10 kΩ pull-up on TQMaRZG2x
JTAG_TDO	X2-B40		–
JTAG_TMS	X2-B38		10 kΩ pull-up on TQMaRZG2x
JTAG_TRST#	X2-B36		10 kΩ pull-down on TQMaRZG2x
ASEBRK	X2-B39		Optional: not required for JTAG

3.4.11 MLB

The RZ/G2x offers an MLB interface that is primarily available.

Table 25: MLB signals

Signal	TQMaRZG2x	Power group
MLB_CLK	X2-B81	3.3 V
MLB_DAT	X2-B82	
MLB_SIG	X2-B83	

3.4.12 PCIe / SATA

The RZ/G2x offers 2 PCIe lanes. With the derivatives RZ/G2H and RZ/G2N one of the two PCIe lanes can be used as SATA. The following signals are primarily available.

Table 26: PCIe / SATA signals

Signal	TQMaRZG2x	Signal level	Remark
PCIE0_CPU_CLK_M	X2-B3	0.8 V	–
PCIE0_CPU_CLK_P	X2-B2	0.8 V	–
PCIE0_TX_M	X2-B6	0.8 V	–
PCIE0_TX_P	X2-B5	0.8 V	–
PCIE0_RX_M	X2-B9	0.8 V	–
PCIE0_RX_P	X2-B8	0.8 V	–
PCIE1_CPU_CLK_M	X2-A3	0.8 V	Can be muxed as SATA
PCIE1_CPU_CLK_P	X2-A2	0.8 V	
PCIE1_TX_M	X2-A6	0.8 V	
PCIE1_TX_P	X2-A5	0.8 V	
PCIE1_RX_M	X2-A9	0.8 V	
PCIE1_RX_P	X2-A8	0.8 V	

3.4.13 PWM

The RZ/G2x offers seven PWM outputs. The following signals are primarily available.

Table 27: PWM signals

Signal	TQMaRZG2x	Power group
MIKRO_BUS_PWM0	X1-A85	3.3 V
LVDS0_PWM1_A	X1-A86	
LCD_CONTRAST_PWM2_A	X1-A87	

3.4.14 SD / MMC Interface

The RZ/G2x offers four SDHI interfaces, which support SD/SDHC/SDXC and MMC (eMMC).
The following signals are primarily available.

Table 28: SDHI signals

Signal	TQMaRZG2x	Power group	Remark
SD0_WP	X2-A93	V_VDDQVA_SD0	Power rail must be supplied by external source. The TQMaRZG2x provides suitable voltages at the connectors. (V_1V8 or V_3V3)
SD0_CD#	X2-A94		
SD0_CMD	X2-A95		
SD0_DATA3	X2-A99		
SD0_DATA2	X2-A98		
SD0_DATA1	X2-A97		
SD0_DATA0	X2-A96		
SD0_CLK	X2-A101		
SD1_CD	X2-B95	V_VDDQVA_SD1	Power rail must be supplied by external source. The TQMaRZG2x provides suitable voltages at the connectors. (V_1V8 or V_3V3)
SD1_WP	X2-B96		
SD1_CMD	X2-B97		
SD1_DAT3	X2-B94		
SD1_DAT2	X2-B93		
SD1_DAT1	X2-B92		
SD1_DAT0	X2-B91		
SD1_CLK	X2-B99		
SD2_DS	X2-B107	V_VDDQVA_SD2	Power rail must be supplied by external source. The TQMaRZG2x provides suitable voltages at the connectors. (V_1V8 or V_3V3)
SD2_CMD	X2-B106		
SD2_DAT3	X2-B105		
SD2_DAT2	X2-B104		
SD2_DAT1	X2-B103		
SD2_DAT0	X2-B102		
SD2_CLK	X2-B109		

3.4.15 SPI (MSIOF)

The RZ/G2x provides four clock-synchronized serial I/O modules. The following signals are primarily available.

Table 29: SPI signals

Signal	TQMaRZG2x	Power group
MSIOF0_SCK	X2-A91	3.3 V
MSIOF0_SS2	X2-A89	
MSIOF0_RXD	X2-A87	
MSIOF0_TXD	X2-A86	
MSIOF0_SYNC	X2-A85	
MSIOF2_SCK	X1-A99	
MSIOF2_SS1	X1-A97	
MSIOF2_RXD	X1-A101	
MSIOF2_TXD	X1-A102	

3.4.16 UART (SCIF / HSCIF)

The RZ/G2x offers five HSCIF and six SCIF interfaces. One of the UARTs can be configured by software to output kernel debug messages. The following signals are primarily available.

Table 30: UART signals

Signal	TQMaRZG2x	Power group
RX0	X2-A76	3.3 V
TX0	X2-A75	
RX1	X2-A82	
TX1	X2-A81	
RX2	X2-B79	
TX2	X2-B78	
HRTS0#	X2-B84	
HCTS0#	X2-B85	
HRX0	X2-B86	
HTX0	X2-B87	

3.4.17 USB

The RZ/G2x offers one USB3.0 and two USB2.0 controllers with internal PHY. All controllers are OTG resp. DRD capable.
The following signals are primarily available.

Table 31: USB signals

Signal	TQMaRZG2x	Power group	Remark
USB30_DM	X2-B13	3.3 V	
USB30_DP	X2-B12	3.3 V	
USB30_CPU_CLK_M	X2-B16	0.8 V	
USB30_CPU_CLK_P	X2-B17	0.8 V	
USB30_TX_M	X2-A13	0.8 V	100 nF AC coupling on TQMaRZG2x
USB30_TX_P	X2-A12	0.8 V	100 nF AC coupling on TQMaRZG2x
USB30_RX_M	X2-A16	0.8 V	
USB30_RX_P	X2-A15	0.8 V	
USB30_ID	X2-A26	3.3 V	
USB30_VBUS	X2-A25	5 V	30 kΩ in series must be provided on carrier board
DM0	X2-B19	3.3 V	
DP0	X2-B18	3.3 V	
VBUS0	X2-B22	5 V	30 kΩ in series must be provided on carrier board
ID0	X2-B23	3.3 V	
USB0_PWREN	X2-B24	3.3 V	
USB0_OVC	X2-B25	3.3 V	
DM1	X2-A19	3.3 V	
DP1	X2-A18	3.3 V	
ID1	X2-A22	3.3 V	

3.5 Power

3.5.1 TQMaRZG2x supply

The TQMaRZG2x only requires a single supply voltage of 5 V ±5 % (4.75 V to 5.25 V).
All other voltages required for the correct operation of the TQMaRZG2x are generated on the TQMaRZG2x.
Supply rails that require an input voltage of 1.8 V or 3.3 V can be powered from an external source, or by a voltage provided by the TQMaRZG2x ; see Table 35. The following table shows all supply voltages for the TQMaRZG2x.

Table 32: TQMaRZG2x supply inputs

Voltage	Level	I_{max}	Usage
V_5V_IN	5 V	See 3.5.2	TQMaRZG2x supply
VDDQVA_SD0	1.8 V or 3.3 V	35 mA	Supply for IO rail SD0
VDDQVA_SD1	1.8 V or 3.3 V	35 mA	Supply for IO rail SD1
VDDQVA_SD2	1.8 V or 3.3 V	35 mA	Supply for IO rail SD2
VDDQVA_SD3	1.8 V or 3.3 V	35 mA	Supply for IO rail SD3
V_BAT	0.9 V to 3.6 V	See 3.3.3	Supply for TQMaRZG2x RTC
VBUS0	Typ. 5 V	<1 mA	Serves to detect the USB VBUS voltage. Supplied by VBUS switched by the USB host. VBUS must be connected to 30 kΩ in series on carrier board.
USB3HS0_VBUS	Typ. 5 V	<1 mA	

3.5.2 Power consumption TQMaRZG2x

The power consumption of the TQMaRZG2x strongly depends on the application, the mode of operation and the operating system. For this reason the given values have to be seen as approximate values.
The following table shows the current consumption of the three TQMaRZG2x variants at a supply voltage of 5 V and an ambient temperature of +25 °C.

Table 33: TQMaRZG2x current consumption

Mode of operation	TQMaRZG2H	TQMaRZG2M	TQMaRZG2N	Remark
STOP-Mode	16 mA	21 mA	22 mA	STOP-Mode by Board Controller
Reset	23 mA	29 mA	29 mA	TQMARZG_RST_IN# = LOW
U-Boot idle	622 mA	591 mA	339 mA	–
Linux idle	552 mA	497 mA	340 mA	–
Linux 100 % load	1260 mA	953 mA	555 mA	Stress test [1]

1: stressapptest -W -s 60 -M 1024 -m 4 -C 4 -i 4 | stress-ng --cpu-load 100 --cpu 4 --timeout 31536000

3.5.3 Power consumption RTC

Table 34: RTC power consumption

Mode of operation	Min.	Typ.	Max.
V_{BAT}, RTC active	1.8 V	3 V	4.5 V
I_{BAT}, RTC active	–	18 µA	50 µA
V_{BAT}, RTC inactive	0.9 V	3 V	4.5 V
I_{BAT}, RTC inactive	–	220 nA	600 nA

3.5.4 Power supply outputs

Depending on the function, some IO rails of the RZ/G2x have different voltages. These IO rails are routed to the TQMaRZG2x connectors and can be supplied externally. No additional switching regulators are required on the carrier board. The 1.8 V and 3.3 V generated on the TQMaRZG2x are available at the connectors for this purpose.
The following table shows the supply outputs provided by the TQMaRZG2x that can be used on the carrier board.

Table 35: TQMaRZG2x supply outputs

Voltage	Level	I_{max}	Usage
V_3V3	3.3 V	200 mA	For Boot Configuration and IO rail VDDQVA_SD[3:0]
V_1V8	1.8 V	200 mA	For IO rail VDDQVA_SD[3:0]
V_BAT	3 V	–	Via low-leakage diode at internal 3.3 V supply

Attention: Destruction or malfunction, overload	
	The voltages mentioned are outputs and must not be supplied externally under any circumstances. The outputs are not short-circuit proof. If the voltages are exceeded, there is a risk of malfunction and damage to components. An overload at one of the voltage outputs may reset the TQMaRZG2x.

3.5.5 Power modes

The TQMaRZG2x provides the following Power Modes:

Table 36: RZ/G2x Power Modes

Power Mode	CPU#n Clock	CPU#n Power	CPU Peripheral (SCU and L2 Cache Controller) Power
Run mode	ON	ON	ON
Sleep mode	OFF	OFF	ON
CoreStandby mode	OFF	OFF [2]	ON
L2 shutdown mode	OFF	OFF [2]	OFF [2]

Table 37: TQMaRZG2x Power Modes details

Power Mode	Condition
Run mode	– TQMaRZG2x is supplied and active.
Sleep mode	– TQMaRZG2x is supplied, all supplies except RZ/G2x clocks are active.
Self-Refresh Mode (Suspend to RAM)	– The LPDDR4 can be switched to Self-Refresh mode with an SRE command. – IDD6 is specified in Self-Refresh, typical current consumption at +25 °C ambient temperature is approx. 0.4 mA … 2.7 mA
Stop Mode	– The TQMaRZG2x must still be supplied with V_5V_IN. – All power supplies on the TQMaRZG2x are switched off, only the board controller and the RTC remain active. – Wake-up e.g. via programmed RTC interrupt or dedicated WAKE-UP pin. – The current consumption is only determined by the board controller and the RTC.
RTC Mode	– The TQMaRZG2x is not supplied with V_5V_IN. – Only the RTC remains supplied and active via V_BAT. – Wake-up only possible via VIN and reset control. – The current consumption is only determined by the current consumption of the RTC and is in the range of 0.2 µA … 0.6 µA.

2: [RZ/G2D] ON (Pseudo Power Shut OFF)

3.6 Reset

The reset logic contains the following functions:

- Voltage monitoring on the TQMaRZG2x
- External reset input
- PGOOD output for power-up of circuits on the carrier board, e.g., PHYs
- Reset LED (Function: PORESET# low: LED lights up)

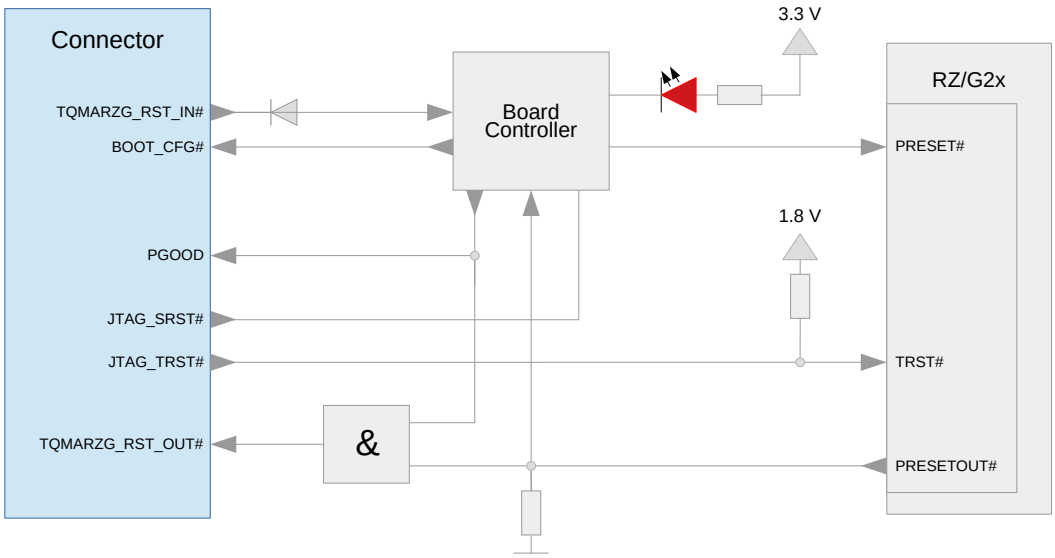

Figure 12: Block diagram Reset structure

➢ **TQMARZG_RST_IN#**

The reset signal controls the complete TQMaRZG2x. As soon as the signal has high level, the TQMaRZG2x starts. The TQMaRZG2x starts as soon as the 5V input voltage is applied. By a diode on the TQMaRZG2x the signal TQ_RST_IN# on the carrier board can be combined with other voltages. A LOW holds the TQMaRZG2x in reset.

➢ **BOOT_CFG#**

BOOT_CFG# controls the boot strapping pins, respectively its driver. The signal is LOW during the reset phase and goes, after PRESETOUT# became HIGH, delayed also on HIGH. This signals the carrier board that the boot strap signals can be switched to high impedance.

➢ **PGOOD**

PGOOD signals that the voltages on the carrier board can be switched on. PGOOD only becomes active when the power sequencing on the TQMaRZG2x has successfully completed.

➢ **JTAG_SRST#**

Depending on the debugger it is necessary to separate PRESET# and TRST# for JTAG access. For this reason the JTAG debugger signal JTAG_SRST# is not connected to the RZ/G2x but to the board controller (3.3V). This causes a PRESET# to be triggered. For the boundary scan test, TRST# must be able to be controlled independently of PRESET#.

➢ **JTAG_TRST#**

TRST# of the debugger is directly connected to TRST# of the RZ/G2x. TRST# has a pull-up to 1.8V.

➢ **TQMARZG_RST_OUT#**

TQMARZG_RST_OUT# is the status signal for the carrier board that the RZ/G2x is still held in reset. TQMARZG_RST_OUT# is connected with PRESETOUT# of the RZ/G2x via an AND. This allows the board controller to hold the periphery in reset in case of an error on the TQMaRZG2x.

3.7 Housekeeping

The TQMaRZG2x uses a system controller for housekeeping and initialization functions. The system controller is also responsible for power sequencing and voltage monitoring.

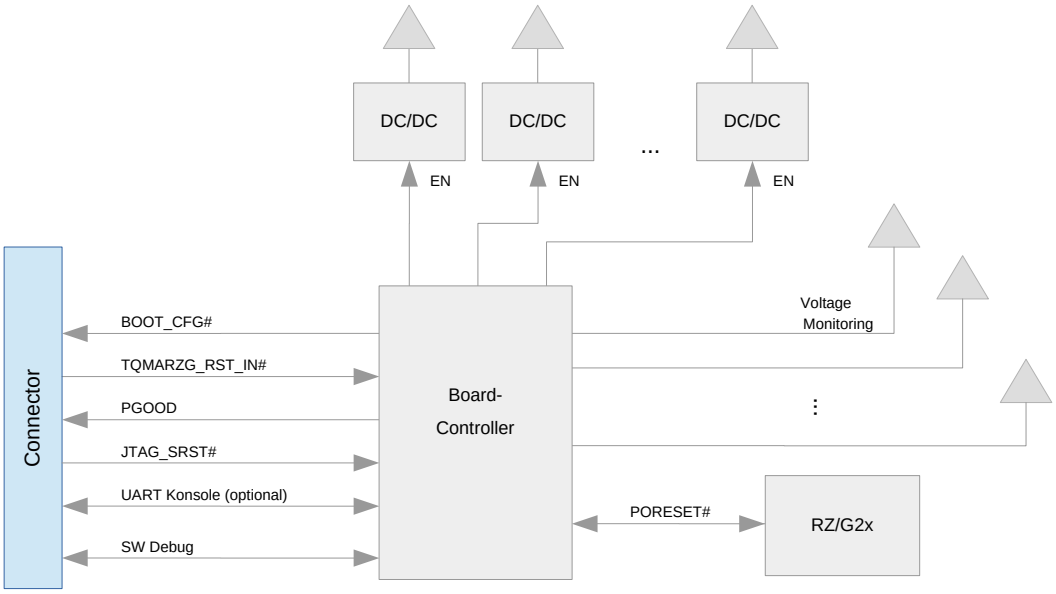

Figure 13: Block diagram Housekeeping

3.7.1 Power sequencing

After activating the TQMaRZG2x 5 V supply and TQMARZG_RST_IN# to “High” the power-up sequence of the TQMaRZG2x starts. After the successful completion of the power-up sequence PGOOD signals by a high level that circuit parts on the carrier board can be supplied.

Attention: Destruction or malfunction, Power-Up sequence	
	To avoid cross-supplies and errors in the power-up sequence of the TQMaRZG2x, no I/O pins may be externally supplied or driven until the power-up sequence of the I/O voltages on the TQMaRZG2x is completed. At the same time, the carrier board component supply voltages must be stable. A high level of PGOOD indicates the successful completion of the power-up sequence.

3.7.2 Voltage monitoring

On the TQMaRZG2x, all voltages are monitored for overvoltage and undervoltage.

4. MECHANICS

4.1 Assembly

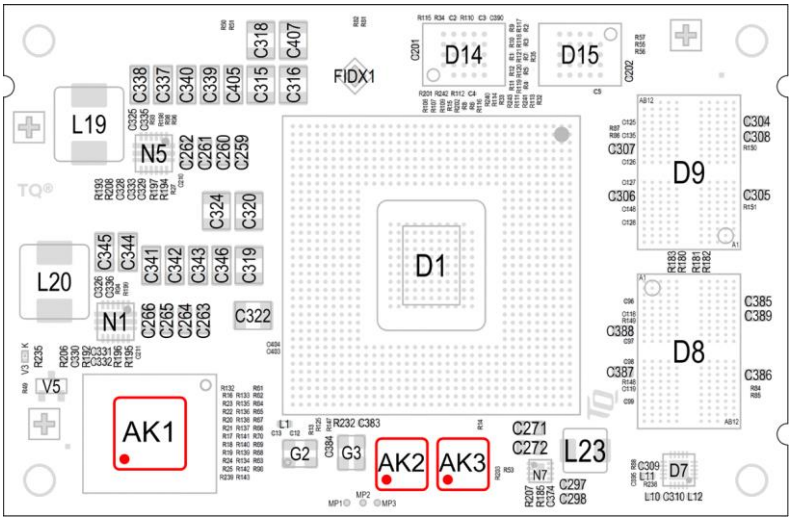

Figure 14: TQMaRZG2x assembly, top

The labels on the TQMaRZG2x show the following information:

Table 38: Labels on TQMaRZG2x

Label	Content
AK1	MAC address, tests performed
AK2	TQMaRZG2x version and revision
AK3	Serial number

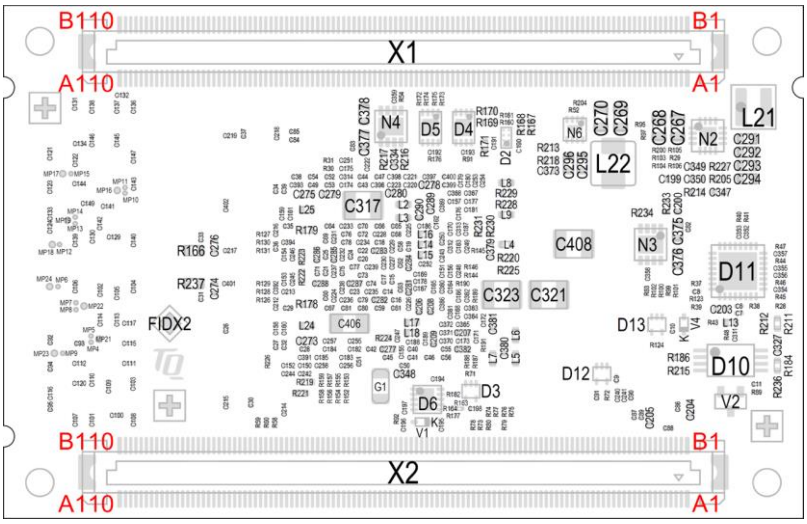

Figure 15: TQMaRZG2x assembly, bottom

4.2 Dimensions

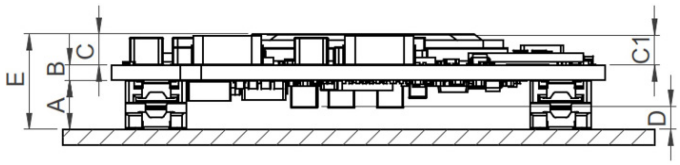

Figure 16: TQMaRZG2x dimensions, side view

The following dimensions result with the EPT mating connector number 401-51101-51 (5 mm board-to-board; see Table 40):

Table 39: TQMaRZG2x heights

Dim.	Value	Tolerance	Remark
A	5.10 mm	±0.07 mm	Board-to-board distance
B	1.48 mm	±0.15 mm	PCB thickness
C	2.85 mm	±0.20 mm	CPU RZ/G2H
C	2.20 mm	±0.15 mm	CPUs RZ/G2M, RZ/G2N
C1	3.00 mm	±0.05 mm	Inductors
D	2.60 mm	±0.31 mm	Free space under TQMaRZG2x
E	9.43 mm	±0.26 mm	Height to top of CPU above carrier board with RZ/G2H
E	8.78 mm	±0.22 mm	Height to top of CPU above carrier board with RZ/G2M, RZ/G2N

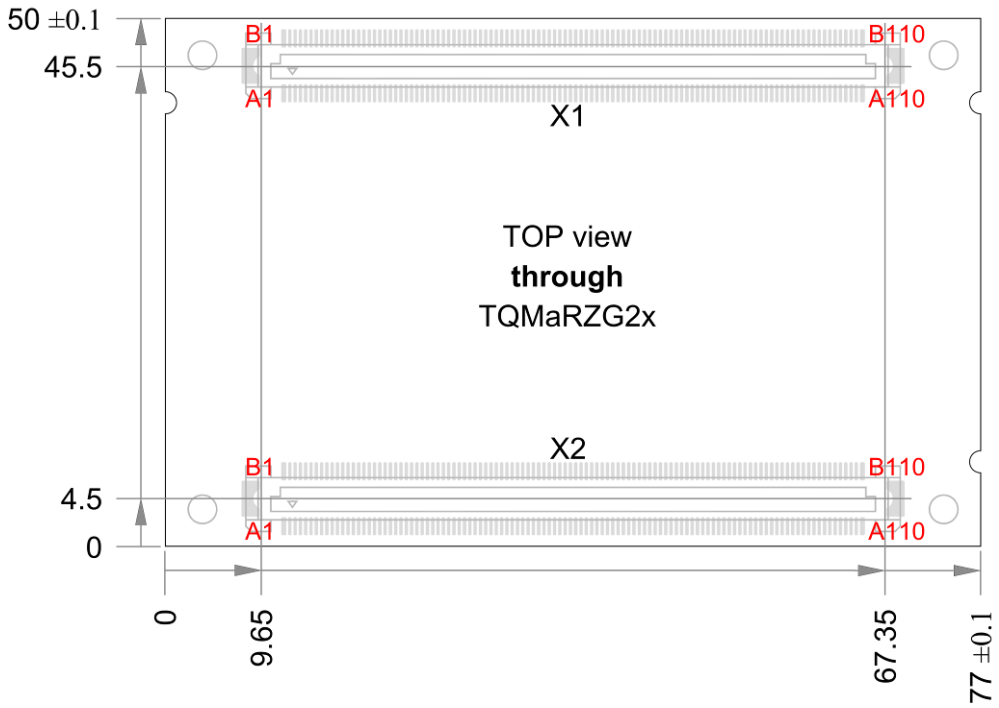

Figure 17: TQMaRZG2x, dimensions, top through view

4.2 Dimensions (continued)

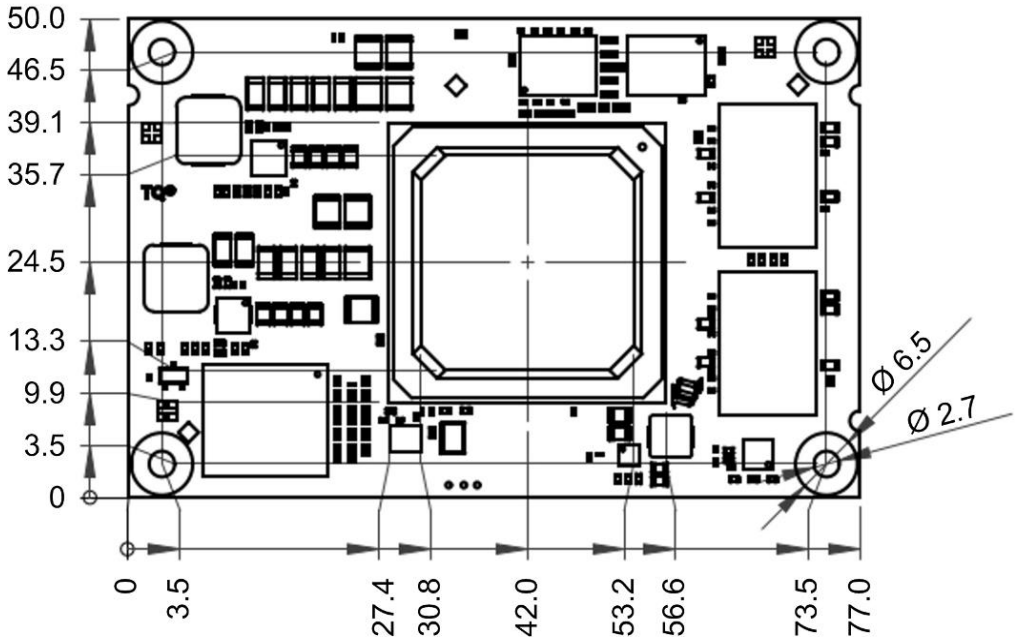

Figure 18: Dimensions TQMaRZG2H

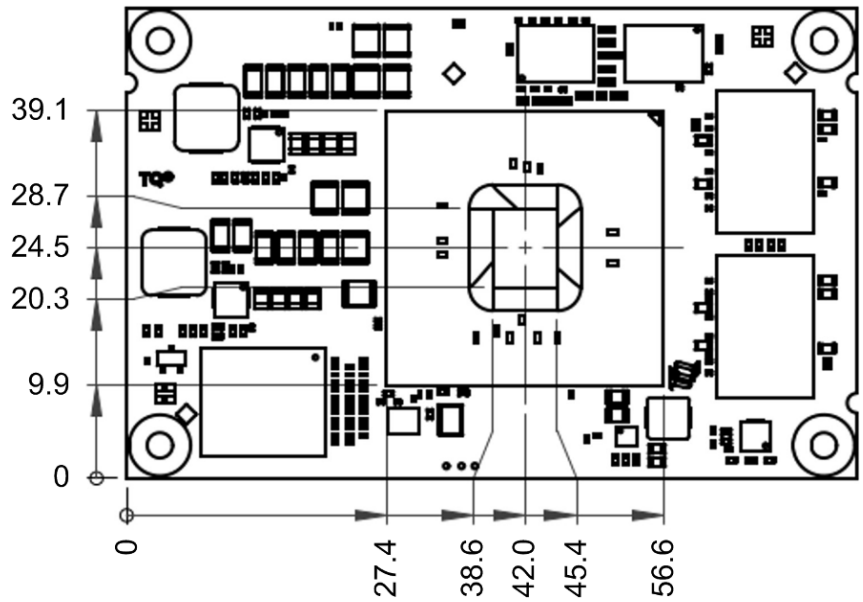

Figure 19: Dimensions TQMaRZG2M, TQMaRZG2N

3D (STEP) models are available on request. Please contact TQ-Support.

4.3 Weight

The three different TQMaRZG2x versions have the following approximate weights:

- TQMaRZG2**H**: 33 ±2 grams
- TQMaRZG2**M**: 28 ±2 grams
- TQMaRZG2**N**: 26 ±2 grams

4.4 Connectors

The TQMaRZG2x is connected to the carrier board with two 220-pin connectors, EPT part number 402-51101-51.
To avoid damaging the connectors of the TQMaRZG2x as well as the connectors on the carrier board while removing the TQMaRZG2x the use of the extraction tool MOZIaRZG2x is strongly recommended.

Attention: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMaRZG2x for the extraction tool MOZIaRZG2x.

The following table shows suitable carrier board mating connectors.

Table 40: Carrier board mating connectors

Manufacturer	Stack height	Part number	Remark
EPT	5 mm	401-51101-51	On MBaRZG2x
	8 mm	401-55101-51	–

The pins assignment in Table 4 and Table 5 refers to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in Table 4 and Table 5, refer to the RZ/G2x documentation (1), (2).

4.5 Protection against external effects

As an embedded module, the TQMaRZG2x is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMaRZG2x, approximately 6 watts must be dissipated; see Table 33 for typical power consumption.
The power dissipation originates primarily in the RZ/G2x, the LPDDR4 SDRAM and the buck regulators.
The power dissipation also depends on the software used and can vary according to the application.

Attention: Destruction or malfunction, TQMaRZG2x heat dissipation	
	The TQMaRZG2x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the RZ/G2x must be taken into consideration when connecting the heat sink. The RZ/G2x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMaRZG2x and thus malfunction, deterioration or destruction.

TQ-Systems offers a heat spreader for the TQMaRZG2H (TQMaRZG2H_HSP) and for the TQMaRZG2M / TQMaRZG2N (TQMaRZG2M_HSP). Please contact your local sales representative.

4.7 Structural requirements

The TQMaRZG2x is held in the mating connectors by the retention force of the pins (440). For high requirements with respect to vibration and shock firmness, an additional retainer has to be provided in the final product to hold the TQMaRZG2x in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

4.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMaRZG2x may only be extracted from the carrier board by using the extraction tool MOZIaRZG2x that can also be obtained separately.

Note: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMaRZG2x for the extraction tool MOZIaRZG2x.

5. SOFTWARE

The TQMaRZG2x is delivered with a preinstalled boot loader and a BSP provided by TQ-Systems, which is configured for the combination of TQMaRZG2x and MBaRZG2x.
The boot loader provides TQMaRZG2x-specific as well as board-specific settings, e.g.:

- RZ/G2x configuration
- LPDDR4 SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

If a different boot loader is used, these settings have to be adapted accordingly.
More information can be found in the TQMaRZG2x Support Wiki.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMaRZG2x was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

The following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board.
- A sufficient number of blocking capacitors in all supply voltages.
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times.
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly).
- Direct signal routing without stubs

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMaRZG2x.

The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Shock and Vibration

Table 41: Shock resistance

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Duration	10 msec
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 42: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 ~ 9 Hz, 9 ~ 200 Hz, 200 ~ 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Acceleration	2 Hz to 9 Hz: 3.5 m/s^2 9 Hz to 200 Hz: 10 m/s^2 200 Hz to 500 Hz: 15 m/s^2

6.4 Climatic and operational conditions

The possible temperature range strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMaRZG2x.
In general, a reliable operation is given when following conditions are met:

Table 43: Climate and operational conditions

Parameter	Range	Remark
Ambient temperature TQMaRZG2x	–40 °C to +85 °C	–
T_J temperature RZ/G2x	–40 °C to +115 °C	–
Case temperature LPDDR4	–40 °C to +95 °C	–
Storage temperature TQMaRZG2x	–40 °C to +100 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Detailed information concerning the CPUs' thermal characteristics is to be taken from the Renesas Reference Manuals (1).

Attention: Destruction or malfunction, TQMaRZG2x heat dissipation	
	The TQMaRZG2x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the RZ/G2x must be taken into consideration when connecting the heat sink. The RZ/G2x is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMaRZG2x and thus malfunction, deterioration or destruction.

6.5 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.6 Reliability and service life

For the three derivatives of the TQMaRZG2x, MTBFs were calculated with a constant error rate @ +40 °C, Ground Benign:

- TQMaRZG2**H**: 567,716 hours
- TQMaRZG2**M**: 588,726 hours
- TQMaRZG2**N**: 627,066 hours

The TQMaRZG2x is designed to be insensitive to vibration and impact.
High quality industrial grade connectors are assembled on the TQMaRZG2x.

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMaRZG2x is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.
Within the scope of the technical possibilities, the TQMaRZG2x was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMaRZG2x always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMaRZG2x on account of available Standby or Sleep-Modes of the components on the TQMaRZG2x.

7.5 Battery

No batteries are assembled on the TQMaRZG2x.

7.6 Packaging

The TQMaRZG2x is delivered in reusable packaging.

7.7 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMaRZG2x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMaRZG2x is minimised by suitable measures.
Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.
No use of PCB containing capacitors and transformers (polychlorinated biphenyls).
These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 44: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
ASCII	American Standard Code for Information Interchange
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN-FD	Controller Area Network Flexible Data-Rate
CPU	Central Processing Unit
CSI	Camera Serial Interface
DDR4	Double Data Rate 4
DIN	Deutsche Industrienorm (German industry standard)
DU	Display Unit
ECC	Error Checking and Correction
EEPROM	Electrically Erasable Programmable Read-only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multi-Media Card
EN	Europäische Norm (European standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FD	Flexible Data-Rate
FR-4	Flame Retardant 4
GPIO	General-Purpose Input/Output
HDMI	High-Definition Multimedia Interface
HSCIF	High-speed Serial Communication Interface
I^2C	Inter-Integrated Circuit
IIC	Inter-Integrated Circuit
IO	Input/Output
IP00	Ingress Protection 00
IPL	Initial Program Loader
JTAG®	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPDDR4	Low-Power Double Data Rate 4
LVDS	Low Voltage Differential Signal
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
MLC	Multi-Level Cell
MMC	Multimedia Card
MOZI	Modulzieher (module extractor)
MTBF	Mean (operating) Time Between Failures

8.1 Acronyms and definitions (continued)

Table 44: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NFC	Near Field Communication
NMI	Non-Maskable Interrupt
NOR	Not-Or
OTG	On-The-Go
PBL	Pre-Boot Loader
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (device)
PLL	Phase-Locked Loop
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Use
RGB	Red Green Blue
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
SATA	Serial Advanced Technology Attachment
SCIF	Serial Communication Interface
SCU	System Control Unit
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDHI	Secure Digital Host Interface
SDRAM	Synchronous Dynamic Random Access Memory
SDXC	Secure Digital eXtended Capacity
SLC	Single-Level Cell (memory technology)
SPI	Serial Peripheral Interface
STEP	Standard for the Exchange of Product (model data)
SVHC	Substances of Very High Concern
SWD	Software Debug
TAP	Test Access Port
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
WEEE®	Waste Electrical and Electronic Equipment

8.2 References

Table 45: Further applicable documents

No.:	Name	Rev., Date	Company
(1)	RZ/G2x Data Sheet		Renesas
(2)	RZ/G Series, 2nd Generation User's Manual	Rev. 1.00, Mar. 2020	Renesas
(3)	MBaRZG2x User's Manual	– current –	TQ-Systems
(4)	TQMaRZG2x Support-Wiki	– current –	TQ-Systems

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Technology in Quality