TQMa93xxCA
Preliminary User's Manual

TQMa93xxCA UM 0003
05.12.2023

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TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	13.4.2023	Kreuzer		First issue
0002	3.8.2023	Kreuzer	Table 2, Table 3 3.2.6.18	Renaming of signals for harmonization with MBa93xxCA Chapter added
0003	5.12.2023	Kreuzer	Table 4 6.3 6.4 6.5 7.5	Table mating connectors added Chapter added Chapter added Chapter added Chapter added

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1.4 Imprint

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa93xxCA and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa93xxCA circuit diagram
- MBa93xxCA User's Manual
- i.MX 93 Data Sheet
- i.MX 93 Reference Manual
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- PTXdist documentation: www.ptxdist.de
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa93xxCA (in progress)

2. BRIEF DESCRIPTION

This User's Manual describes the hardware of the TQMa93xxCA as of revision 01xx, in combination with the MBa93xxCA as of revision 02xx and refers to some software settings. A certain TQMa93xxCA derivative does not necessarily provide all features described in this User's Manual.

This User's Manual does neither replace the i.MX 93 Reference Manual (1), nor the i.MX 93 Data Sheet (2), nor any other documents from NXP.

The TQMa93xxCA is a universal Minimodule based on the NXP ARM® Cortex®-A55 based i.MX 93 CPU family, see also Table 5.

2.1 Key functions and characteristics

The TQMa93xxCA extends the TQ-Systems GmbH product range and offers an outstanding computing performance.

All essential i.MX 93 signals are routed to the TQMa93xxCA connectors. There are therefore no restrictions for customers using the TQMa93xxCA with respect to an integrated customised design. All essential components like CPU, LPDDR4, eMMC, and PMIC are already integrated on the TQMa93xxCA.

The main features of the TQMa93xxCA are:

- 64 bit NXP i.MX 93 CPU, up to 2 × ARM Cortex®-A55 and 1 × Cortex®-M33
- Up to 2 Gbyte of LPDDR4- or LPDDR4X RAM
- Up to 256 Gbyte of eMMC NAND Flash, eMMC standard 5.1
- Up to 256 Mbyte QSPI NOR Flash (optional)
- 64 Kbit EEPROM (optional)
- Temperature sensor + EEPROM
- NXP Power Management Integrated Circuit PCA9451
- RTC (optional)
- Trust Secure Element (optional)
- Gyroscope (optional)
- All essential i.MX 93 signals are routed to the TQMa93xxCA connectors
- Single supply voltage 5 V

2.2 CPU block diagram

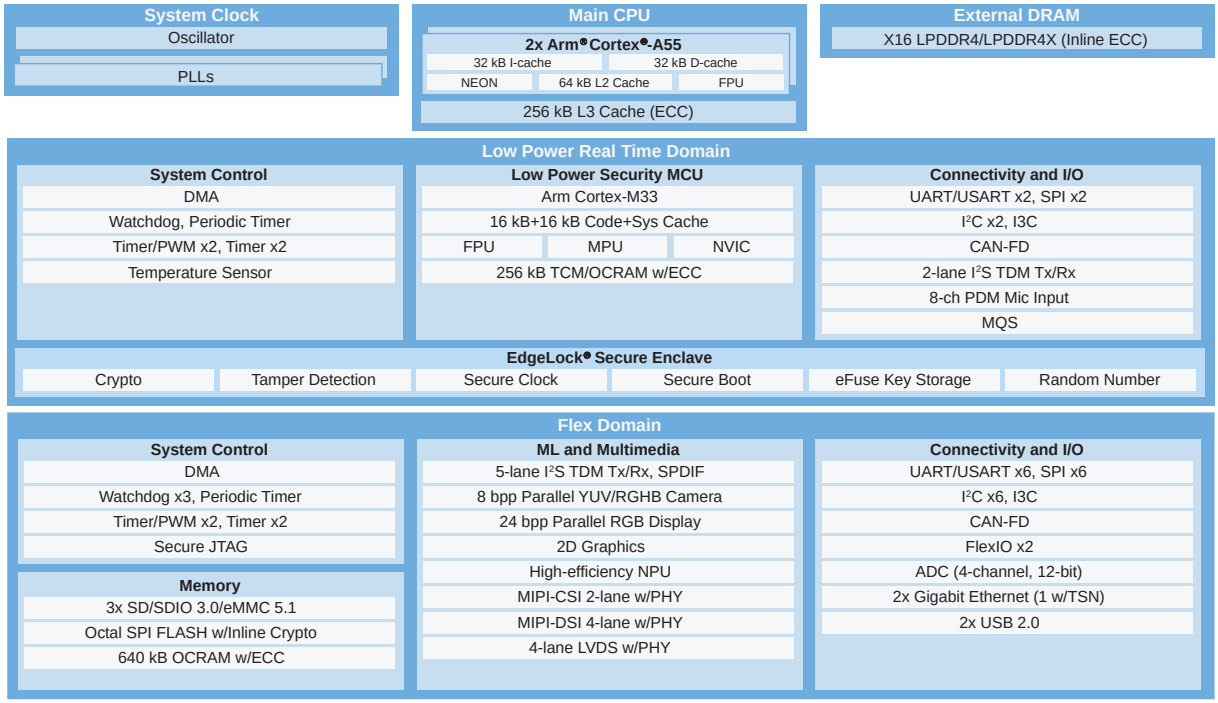

Figure 1: Block diagram i.MX 93
(Source: NXP)

3. ELECTRONICS

The information provided in this User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa93xxCA, and the BSP provided by TQ-Systems GmbH, see also chapter 4.

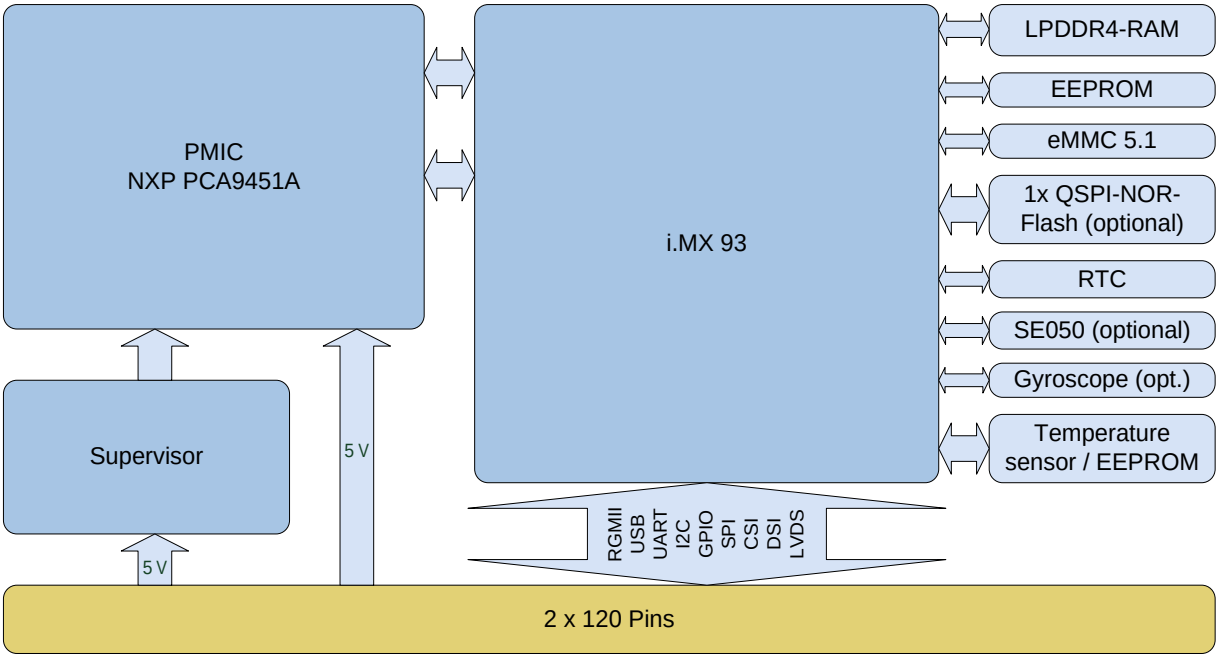

Figure 2: Block diagram TQMa93xxCA (simplified)

3.1 Interfaces to other systems and devices

3.1.1 Pin multiplexing

The multiple pin configurations by different i.MX 93 internal function units must be taken note of.
The pin assignment in Table 3 refers to a TQMa93xxCA with i.MX 93 CPU in combination with the carrier board MBa93xxCA.
NXP provides a tool showing the multiplexing and simplifies the selection and configuration (i.MX Pins Tool – NXP Tool).
The electrical and pin characteristics are to be taken from the i.MX 93 and PMIC documentation, see Table 39.

Attention: Destruction or malfunction, pin multiplexing	
	Depending on the configuration, many i.MX 93 pins can provide several different functions. Please take note of the information concerning the configuration of these pins in the i.MX 93 Reference Manual (1), before integration or start-up of your carrier board / Starterkit. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa93xxCA. The descriptions given in the following tables should be taken note of: – DNC: These pins must never be connected and have to be left open. Please contact TQ-Support for details.

3.1.2 Pinout TQMa93xxCA

The TQMa93xxCA has a total of 240 connector pins (2 x 120). The following tables show the TQMa93xxCA pin-out.

Table 2: Pinout TQMa93xxCA, X1

Cpu ball	Dir.	Level	TQ Multiplexing	Pin		TQ Multiplexing	Level	Dir.	CPU ball
-	P	5 V	V_5V_IN	X1-A1	X1-B1	V_5V_IN	5 V	P	-
-	P		V_5V_IN	X1-A2	X1-B2	V_5V_IN		P	-
-	P		V_5V_IN	X1-A3	X1-B3	V_5V_IN		P	-
-	-	0 V	GND	X1-A4	X1-B4	GND	0 V	-	-
AA2	O	1.8 V	GPIO3_IO26	X1-A5	X1-B5	ENET1_TXC	1.8 V	O	U10
-	-	0 V	GND	X1-A6	X1-B6	GND	0 V	-	-
Y3	O	1.8 V	GPIO3_IO27	X1-A7	X1-B7	ENET1_TX_CTL	1.8 V	O	V10
U4	O		CLK3_OUT	X1-A8	X1-B8	ENET1_TXD0		O	W11
V4	O		GPIO4_IO29	X1-A9	X1-B9	ENET1_TXD1		O	T12
-	-	0 V	GND	X1-A10	X1-B10	ENET1_TXD2		O	U12
-	I/O	3.3 V	PMIC_SCLH	X1-A11	X1-B11	ENET1_TXD3		O	V12
-	I/O		PMIC_SDAH	X1-A12	X1-B12	GND	0 V	-	-
-	-	0 V	GND	X1-A13	X1-B13	ENET1_RXC	1.8 V	I	AA7
-	I/O	1.8 V	PMIC_SDAL	X1-A14	X1-B14	GND	0 V	-	-
-	I/O		PMIC_SCLL	X1-A15	X1-B15	ENET1_RX_CTL	1.8 V	I	Y8
-	-	0 V	GND	X1-A16	X1-B16	GND	0 V	-	-
AA19	O	V_SD2	SD2_CLK	X1-A17	X1-B17	ENET1_RXD0	1.8 V	I	AA8
-	-	0 V	GND	X1-A18	X1-B18	ENET1_RXD1		I	Y9
Y19	I/O	V_SD2	SD2_CMD	X1-A19	X1-B19	ENET1_RXD2		I	AA9
Y17	I		SD2_CD#	X1-A20	X1-B20	ENET1_RXD3		I	Y10
-	-	0 V	GND	X1-A21	X1-B21	GND	0 V	-	-
Y18	I/O	V_SD2	SD2_DATA0	X1-A22	X1-B22	ENET1_MDC	1.8 V	O	AA11
AA18	I/O		SD2_DATA1	X1-A23	X1-B23	ENET1_MDIO		I/O	AA10
Y20	I/O		SD2_DATA2	X1-A24	X1-B24	GND	0 V	-	-
AA20	I/O		SD2_DATA3	X1-A25	X1-B25	QSPI_SCLK[1]	1.8 V	O	V16
-	-	0 V	GND	X1-A26	X1-B26	GND	0 V	-	-
AA17	O	V_SD2	SD2_RST#	X1-A27	X1-B27	QSPI_SS0#[1]	1.8 V	O	U16
-	-	0 V	GND	X1-A28	X1-B28	QSPI_DATA0[1]		I/O	T16
-	P	1.8 V / 3.3V	V_SD2	X1-A29	X1-B29	QSPI_DATA1[1]		I/O	V14
-	-	0 V	GND	X1-A30	X1-B30	QSPI_DATA2[1]		I/O	U14
-	P	3.3 V	V_3V3_SD[2]	X1-A31	X1-B31	QSPI_DATA3[1]		I/O	T14
-	-	0 V	GND	X1-A32	X1-B32	GND	0 V	-	-
-	P	3.3 V	V_3V3[3]	X1-A33	X1-B33	RFU	-	-	-
-	P	1.8 V	V_1V8[3]	X1-A34	X1-B34	RFU	-	-	-
-	-	0 V	GND	X1-A35	X1-B35	GND	0 V	-	-
R20	I/O	V_GPIO	SAI3_MCLK	X1-A36	X1-B36	PMIC_RST#	1.8 V	I	-
-	-	0 V	GND	X1-A37	X1-B37	RESET_OUT#	open drain, needs external pull-up		
T21	I/O	V_GPIO	SAI3_TXD0	X1-A38	X1-B38	GPIO1_IO02	3.3 V	I/O	D20
V20	I/O		SAI3_TXFS	X1-A39	X1-B39	GND	0 V	-	-
R21	I/O		SAI3_TXC	X1-A40	X1-B40	UART6_RXD	V_GPIO	I/O	L18
-	-	O V	GND	X1-A41	X1-B41	UART6_TXD		I/O	L17
T20	I/O	V_GPIO	SAI3_RXD0	X1-A42	X1-B42	GND	0 V	-	-
R17	I/O		SAI3_RXFS	X1-A43	X1-B43	TPM5_CH0	V_GPIO	I/O	L20
R18	I/O		SAI3_RXC	X1-A44	X1-B44	GPIO2_IO07		I/O	L21
-	-	0 V	GND	X1-A45	X1-B45	GND	0 V	-	-
N20	I/O	V_GPIO	UART8_TXD	X1-A46	X1-B46	SPI6_PCS0#	V_GPIO	I/O	J21
N21	I/O		UART8_RXD	X1-A47	X1-B47	SPI6_SIN		I/O	J20
-	-	0 V	GND	X1-A48	X1-B48	SPI6_SOUT		I/O	K20
P20	I/O	V_GPIO	UART3_TXD	X1-A49	X1-B49	SPI6_SCK		I/O	K21
P21	I/O		UART3_RXD	X1-A50	X1-B50	GND	0 V	-	-
-	-	0 V	GND	X1-A51	X1-B51	GPIO2_IO10	V_GPIO	I/O	N17
U21	I/O	V_GPIO	GPIO2_IO24	X1-A52	X1-B52	TPM3_EXTCLK		I/O	M21
U20	I/O		I2C5_SCL	X1-A53	X1-B53	TPM6_CH0		I/O	M20
U18	I/O		I2C5_SDA	X1-A54	X1-B54	GPIO2_IO11		I/O	N18
-	-	0 V	GND	X1-A55	X1-B55	GND	0 V	-	-
W21	I/O	V_GPIO	CAN2_RX	X1-A56	X1-B56	GPIO1_IO14	3.3 V	O	H20
V21	I/O		CAN2_TX	X1-A57	X1-B57	GPIO1_IO12		I	G20
-	-	0 V	GND	X1-A58	X1-B58	GPIO1_IO11		O	G21
Y21	I/O	V_GPIO	I2C3_SCL	X1-A59	X1-B59	UART2_RTS#		O	H21
W20	I/O		I2C3_SDA	X1-A60	X1-B60	GND	0 V	-	-

[1] NC if NOR-Flash is placed

[2] Power-Output (max. 400 mA)

[3] Power-Output (max. 500 mA)

Table 3: Pinout TQMa93xxCA, X2

CPU ball	Dir.	Level	TQ Multiplexing	Pin		TQ Multiplexing	Level	Dir.	CPU ball
-	I/O	3.3 V	ISO_14443_LA	X2-A1	X2-B1	LVDS_D3_P	1.8 V	O	C1
-	I/O		ISO_14443_LB	X2-A2	X2-B2	LVDS_D3_N		O	B1
-	-	0 V	GND	X2-A3	X2-B3	GND	0 V	-	-
-	I	3.3 V	ISO_7816_CLK	X2-A4	X2-B4	LVDS_CLK_P	1.8 V	O	B3
-	I/O		ISO_7816_IO1	X2-A5	X2-B5	LVDS_CLK_N		O	A3
-	-	0 V	GND	X2-A6	X2-B6	GND	0 V	-	-
-	I/O	3.3 V	ISO_7816_IO2	X2-A7	X2-B7	LVDS_D2_P	1.8 V	O	B2
-	I	3.3 V	ISO_7816_RST	X2-A8	X2-B8	LVDS_D2_N		O	A2
-	-	0 V	GND	X2-A9	X2-B9	GND	0 V	-	-
W1	I	1.8 V	JTAG_TDI	X2-A10	X2-B10	LVDS_D1_P	1.8 V	O	B4
Y2	O		JTAG_TDO	X2-A11	X2-B11	LVDS_D1_N		O	A4
Y1	O		JTAG_TCK	X2-A12	X2-B12	GND	0 V	-	-
W2	I/O		JTAG_TMS	X2-A13	X2-B13	LVDS_D0_P	1.8 V	O	B5
-	-	0 V	GND	X2-A14	X2-B14	LVDS_D0_N		O	A5
-	P	0.9…5.5 V	V_LICELL	X2-A15	X2-B15	RTC_EVENT#	open drain, needs external pull-up		
-	-	0 V	GND	X2-A16	X2-B16	GND	0 V	-	-
U6	O	1.8 V	ENET2_TXC	X2-A17	X2-B17	TEMP_EVENT#	open drain, needs external pull-up		
-	-	0 V	GND	X2-A18	X2-B18	DSI1_D0_N	1.8 V	O	A6
V6	O	1.8 V	ENET2_TX_CTL	X2-A19	X2-B19	DSI1_D0_P		O	B6
T8	O		ENET2_TXD0	X2-A20	X2-B20	GND	0 V	-	-
U8	O		ENET2_TXD1	X2-A21	X2-B21	DSI1_D1_N	1.8 V	O	A7
V8	O		ENET2_TXD2	X2-A22	X2-B22	DSI1_D1_P		O	B7
T10	O		ENET2_TXD3	X2-A23	X2-B23	GND	0 V	-	-
-	-	0 V	GND	X2-A24	X2-B24	DSI1_CLK_N	1.8 V	O	D6
AA3	I	1.8 V	ENET2_RXC	X2-A25	X2-B25	DSI1_CLK_P		O	E6
-	-	0 V	GND	X2-A26	X2-B26	GND	0 V	-	-
Y4	I	1.8 V	ENET2_RX_CTL	X2-A27	X2-B27	DSI1_D2_N	1.8 V	O	A8
AA4	I		ENET2_RXD0	X2-A28	X2-B28	DSI1_D2_P		O	B8
Y5	I		ENET2_RXD1	X2-A29	X2-B29	GND	0 V	-	-
AA5	I		ENET2_RXD2	X2-A30	X2-B30	DSI1_D3_N	1.8 V	O	A9
Y6	I		ENET2_RXD3	X2-A31	X2-B31	DSI1_D3_P		O	B9
-	-	0 V	GND	X2-A32	X2-B32	GND	0 V	-	-
AA6	I/O	1.8 V	ENET2_MDIO	X2-A33	X2-B33	CSI1_D0_N	1.8 V	I	A11
Y7	O		ENET2_MDC	X2-A34	X2-B34	CSI1_D0_P		I	B11
-	-	0 V	GND	X2-A35	X2-B35	GND	0 V	-	-
C20	O	3.3 V	I2C1_SCL	X2-A36	X2-B36	CSI1_CLK_N	1.8 V	I	D10
C21	I/O		I2C1_SDA	X2-A37	X2-B37	CSI1_CLK_P		I	E10
-	-	0 V	GND	X2-A38	X2-B38	GND	0 V	-	-
J17	I	3.3 V	CAN1_RX	X2-A39	X2-B39	CSI1_D1_N	1.8 V	I	A10
G17	O		CAN1_TX	X2-A40	X2-B40	CSI1_D1_P		I	B10
-	-	0 V	GND	X2-A41	X2-B41	GND	0 V	-	-
G18	I	3.3 V	M33_NMI	X2-A42	X2-B42	ONOFF	1.8 V	I	A19
B16	I/O	1.8 V	TAMPER0	X2-A43	X2-B43	USB1_ID	1.8 V	I	C11
F14	I/O		TAMPER1	X2-A44	X2-B44	USB2_ID		I	E12
-	-	0 V	GND	X2-A45	X2-B45	GND	0 V	-	-
B17	I	1.8 V	CLK1_IN	X2-A46	X2-B46	V_GPIO[4]	1.8 V / 3.3 V	P	N15
A18	I		CLK2_IN	X2-A47	X2-B47	USB1_VBUS	3.3 V	P	F12
J18	O	3.3 V	WDOG_ANY	X2-A48	X2-B48	USB2_VBUS	(5 V tolerant)	P	E14
-	I	3.3 V	PMIC_WDOG_IN#	X2-A49	X2-B49	GND	0 V	-	-
-	-	0 V	GND	X2-A50	X2-B50	DNC	-	-	B12
B19	I	1.8 V	ADC_IN0	X2-A51	X2-B51	DNC		-	A12
A20	I		ADC_IN1	X2-A52	X2-B52	GND	0 V	-	-
B20	I		ADC_IN2	X2-A53	X2-B53	DNC	-	-	B13
B21	I		ADC_IN3	X2-A54	X2-B54	DNC		-	A13
-	-	0 V	GND	X2-A55	X2-B55	GND	0 V	-	-
E20	I	3.3 V	UART1_RXD	X2-A56	X2-B56	USB1_DP	3.3 V	I/O	B14
E21	O	3.3 V	UART1_TXD	X2-A57	X2-B57	USB1_DN		I/O	A14
F20	I	3.3 V	UART2_RXD	X2-A58	X2-B58	GND	0 V	-	-
F21	O	3.3 V	UART2_TXD	X2-A59	X2-B59	USB2_DP	3.3 V	I/O	B15
-	-	0 V	GND	X2-A60	X2-B60	USB2_DN		I/O	A15

Details about the electrical characteristics of single pins and interfaces are to be taken from the i.MX 93 documentation (1), (2), (3), as well as the PMIC Data Sheet (4).

[4] Power-Input for NVCC_GPIO

The mating connectors for X1 and X2 are available from ept GmbH in two heights:

Table 4: Mating connectors

Name	Part number	Height
Colibri Plug 120, 5mm	401-51401-51	5 mm
Colibri Plug 120, 8mm	401-55401-51	8 mm

3.2 System components

3.2.1 i.MX 93

3.2.1.1 i.MX 93 derivatives

Depending on the TQMa93xxCA version, one of the following i.MX 93 derivatives is assembled.

Table 5: i.MX 93 derivatives

TQMa93xxCA version	i.MX 93 derivative	i.MX 93 clocks	Temperature range
TQMa9352CA	i.MX 9352	2 x A55: 1.5 GHz, M33: 250 MHz, NPU	–40 °C … +105 °C
TQMa9351CA	i.MX 9351	1 x A55: 1.5 GHz, M33: 250 MHz, NPU	–40 °C … +105 °C
TQMa9332CA	i.MX 9332	2 x A55: 1.5 GHz, M33: 250 MHz	–40 °C … +105 °C
TQMa9331CA	i.MX 9331	1 x A55: 1.5 GHz, M33: 250 MHz	–40 °C … +105 °C

3.2.1.2 i.MX 93 errata

Attention: Destruction or malfunction, i.MX 93 errata	
	Please take note of the current i.MX 93 errata (5).

3.2.1.3 Boot modes

The i.MX 93 has a ROM with integrated boot loader. After the release of PMIC_POR# the System Controller (SCU) boots from the internal ROM and then loads the program image from the selected boot device. For example, the integrated eMMC or the optional QSPI NOR Flash can be selected as the default boot device. The following boot sources are supported by TQMa93xxCA:

- eMMC (SD1)
- QSPI/FlexSPI NOR Flash (SD1 + SD3)
- SD card (SD2)
- Serial Download (USB1)

Alternatively, an image can be loaded into the internal RAM using the serial downloader.
More information about the boot flow can be found in the Reference Manual (1), and the Data Sheet (2) of i.MX 93.

3.2.1.4 Boot configuration

This section provides information on boot mode configuration pins allocation and boot device interface allocation. The i.MX 93 uses four BOOT_MODE signals provided on the TQMa93xxCA's connector pins. These require pull-up/pull-down (4.7 kΩ/ 100 kΩ) wiring to 3.3 V and Ground. However, the BOOT_MODE signals are not dedicated to this function, but have other functionalities in normal operation. The boot mode is initialized by sampling the BOOT_MODE[3:0] inputs when the reset is deactivated and are to be set high or low according to the desired boot source at the time of readout. After these inputs are sampled, their subsequent state does not affect the contents of the BOOT_MODE internal register.

The exact boot source configuration can be seen in the following table:

Table 6: Boot configuration i.MX 93

Boot source	Boot Core	BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0
Boot from eFuse	A55	0	0	0	0
Serial Downloader (USB1)		0	0	0	1
Boot from eMMC 5.1 (USDHC1, 8-bit))		0	0	1	0
Boot from SD 3.0 card (USDHC2, 4-bit)		0	0	1	1
Boot from FlexSPI Serial NOR		0	1	0	0
Boot from FlexSPI NAND 2K (not supported)		0	1	0	1
Boot from eFuse	M33	1	0	0	0
Serial Downloader (USB1)		1	0	0	1
Boot from eMMC 5.1 (USDHC1, 8-bit)		1	0	1	0
Boot from SD 3.0 card (USDHC2, 4-bit)		1	0	1	1
Boot from FlexSPI Serial NOR		1	1	0	0
Boot from FlexSPI Serial NAND 2K (not supported)		1	1	0	1

BOOT_MODE3 is used to distinguish between Low Power Boot (LPB - start of the M33 core) and Single Boot (start of the A55 core).

In LPB, only the M33 ROM is running after Power-On Reset (POR); the A55 core is expected to be kicked off by M33 firmware in some use cases.

In Single Boot, the Cortex-A55 ROM loads both the Cortex-A55 firmware image and the Cortex-M33 firmware image (if exists). If the container set has the Cortex-M33 firmware image, the Cortex-A55 ROM will read and place it in the Shared RAM (Cortex-M33 TCM). The Cortex-M33 BootROM is not involved in the Single Boot Flow. Once the Cortex-A55 loads the Cortex-M33 firmware image to the Cortex-M33 TCM, the Cortex-A55 ROM will issue a message that kick off the Cortex-M33 core, and continues the Cortex-A55 boot process, with Cortex-M33 & Cortex-A55 boot running in parallel.

3.2.2 Memory

3.2.2.1 LPDDR4 SDRAM

The memory interface of the i.MX 93 supports LPDDR4 and LPDDR4X memory (16 bit bus) with a maximum clock rate of 1866 MHz, which meets JEDEC LPDDR4-3733 standard. 1 GByte is the standard configuration, a maximum of 2 Gbyte of LPDDR4 SDRAM is supported.

3.2.2.2 eMMC

An eMMC is provided on the TQMa93xxCA for boot loader, operating system and application software. It is connected to the i.MX 93 via SD1-interface. A maximum transfer rate of 400 MB/s is supported (HS400 mode). Resets have to be done via software.

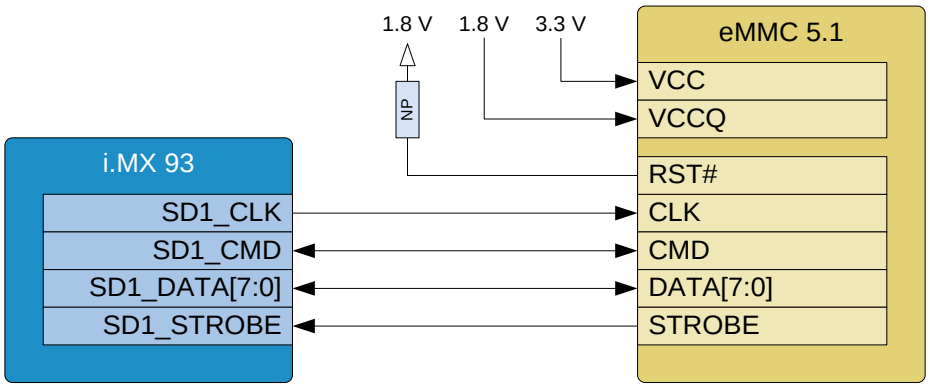

Figure 3: Block diagram eMMC

The boot configuration is described in chapter 3.2.1.3

3.2.2.3 QSPI NOR Flash / NAND Flash

QSPI NOR flash can optionally be assembled on the TQMa93xxCA. Because a separation of the signal paths is not possible, these connector pins must not be wired when equipped with NOR Flash. With unpopulated NOR Flash the signals of the SD3 interface can be used outside the module.

The NOR flash signals use a part of the NAND pins of the i.MX 93. All other NAND pins of the i.MX 93 are used from the TQMa93xxCA for the eMMC as SD1 boot source and for the SD-Card (SD2).

Table 7: QSPI signals

Signal	i.MX 93	TQMa93xxCA	Power group
QSPI_DATA0	T16	X1-B28	1,8 V
QSPI_DATA1	V14	X1-B29	
QSPI_DATA2	U14	X1-B30	
QSPI_DATA3	T14	X1-B31	
QSPI_SCLK	V16	X1-B25	
QSPI_SS0#	U16	X1-B27	

3.2.2.4 EEPROM M24C64-D

A 64 Kbit EEPROM is assembled by default on the TQMa93xxCA. The serial EEPROM is controlled by the I2C1 bus. The M24C64-D offers an additional page, named the Identification Page (32 Byte). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

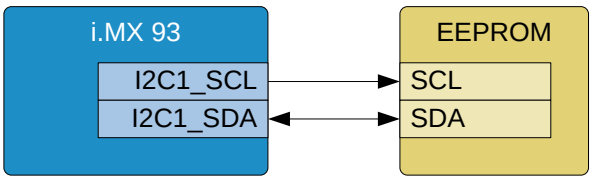

Figure 4: Block diagram EEPROM

- The EEPROM has I²C address `0x57 / 101 0111b`
- Identification Page (32 Byte) `0x5F / 101 1111b`

3.2.2.5 EEPROM with temperature sensor SE97BTP

A serial EEPROM including temperature sensor type SE97BTP, controlled by the I2C1 bus, is assembled on the TQMa93xxCA.
The lower 128 bytes (address 00h to 7Fh) can be set to Permanent Write-Protected mode (PWP) by software. The upper 128 bytes (address 80h to FFh) cannot be write-protected and are available for general data storage.
The overtemperature output of the SE97BTP is connected as open drain to TQMa93xxCA pin X2-B17 (TEMP_EVENT#). The device is assembled on the top side of the TQMa93xxCA (component D6).

- The device provides the following I2C addresses:
  - EEPROM (Normal Mode): `0x53 / 101 0011b`
  - EEPROM (Protection Mode): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

3.2.3 Trust Secure Element SE050

An NXP Trust Secure Element SE050 is available on the TQMa93xxCA as an assembly option.

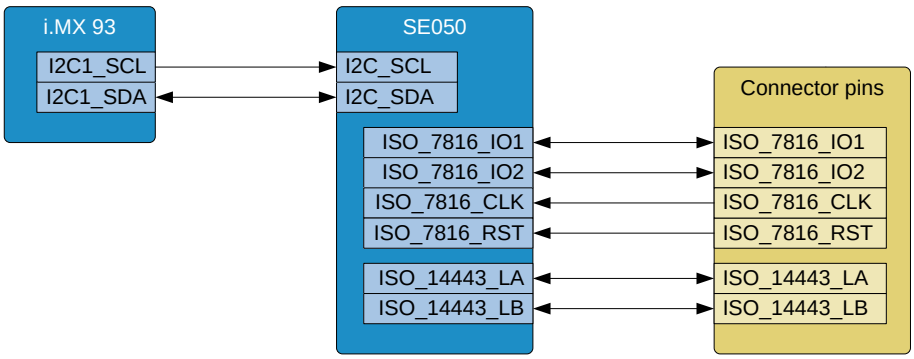

Figure 5: Block diagram SE050

When equipped, the chip provides two interfaces according to ISO 7816 and ISO 14443. Among other things, antennas can be connected to these.

Table 8: ISO_7816 and ISO_14443 signals

Signal	Direction	TQMa93xxCA	Remark
ISO_7816_CLK	I	X2-A4	Only with populated Trust Secure Element
ISO_7816_RST	I	X2-A8	
ISO_7816_IO1	I/O	X2-A5	
ISO_7816_IO2	I/O	X2-A7	
ISO_14443_LA	I/O	X2-A1	
ISO_14443_LB	I/O	X2-A2	

The SE050 is controlled by the I2C1 bus. More details can be found in (8).

- The Trust Secure Element has I²C address `0x48 / 100 1000b`

3.2.4 Accelerometer/Gyroscope

As an optional extension a 3D Digital Accelerometer / 3D Digital Gyroscope (ISM330DHCX from STMicroelectronics) is provided on theTQMa93xxCA, which has an I²C interface. It allows to determine the position of the module and provides two interrupts. However, these are not routed to the outside.

- The Accelerometer/Gyroscope has I²C address `0x6A / 110 1010b`

3.2.5 RTC

The TQMa93xxCA can use the internal Real Time Clock of the i.MX 93 or can be provided with an optional discrete RTC PCF85063A.

3.2.5.1 i.MX 93 internal RTC

The i.MX 93 provides an internal RTC, which has its own power domain, supplied by the PMIC. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

Note: RTC power supply	
	The CPU internal RTC can be used in regular operation. If the TQMa93xxCA supply (5 V) fails, it is no longer available, since the i.MX 93 power rail is no longer supplied.

3.2.5.2 Discrete RTC PCF85063A

In addition to the i.MX 93 internal RTC the TQMa93xxCA provides a discrete RTC PCF85063A as an assembly option, which is controlled by the I2C1 bus. The quartz used to clock the RTC has a standard frequency tolerance of ±20 ppm @ +25 °C.

The discrete RTC has an interrupt output which provides the open-drain signal RTC_EVENT# at pin X2-B15. This pin requires a pull-up to 3.3 V (maximum 3.6 V) on the carrier board.

The RTC PCF85063A is only directly supplied by V_LICELL when the PMIC or the TQMa93xxCA supply is switched off.

During normal operation of the TQMa93xxCA, the PMIC supplies 3.3 V. To prevent charging a non-rechargeable backup supply, a diode on the baseboard is needed for V_LICELL.

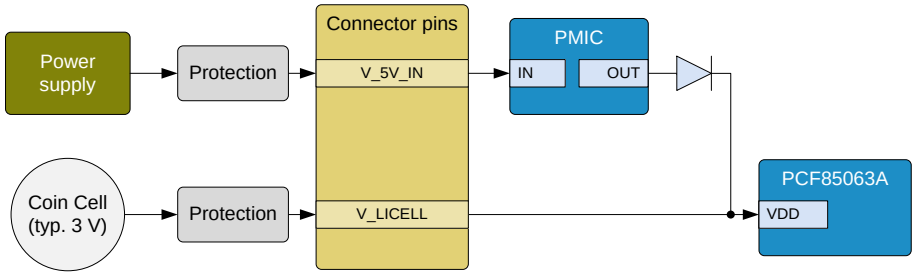

Figure 6: Block diagram RTC supply (TQMa93xxCA with discrete RTC)

- The discrete RTC has I2C address `0x51 / 101 0001b`

Note: RTC power supply	
	The BBSM functions of the i.MX 93 can only be used if the TQMa93xxCA is supplied with 5 V. Because the BBSM rail is not supplied when the TQMa93xxCA is not powered-up, we recommend using the optional RTC PCF85063A.

3.2.6 Interfaces

3.2.6.1 Overview

Except for the internal interfaces, all functional pins of the i.MX 93 are routed to TQMa93xxCA connector pins. Each customer must check the suitability of the multiplexing in the respective project and adapt it if necessary. The following table shows one exemplary multiplexing with the TQMa93xxCA to utilize the most primary interfaces simultaneously:

Table 9: TQMa93xxCA interfaces

i.MX 93 Interface	Quantity	Remark
Internal interfaces		
LPDDR4	1	LPDDR4(X), x16
SD3 (QSPI)	1	
SD1 (eMMC)	1	8 bit (HS400)
External interfaces		
ADC	1	4 x inputs
CAN	2	
GPIO	6	
I2C	3	1 x for internal components, 2x for other peripherals
JTAG	1	
LVDS	1	4 x diff. DATA, 1x diff. CLK
MIPI CSI	1	2 x diff. DATA, 1x diff. CLK
MIPI DSI	1	4 x diff. DATA, 1x diff. CLK
RGMII	2	
SAI (Audio)	1	
SPI	2	1 x CS each (2x CS possible with omission of GPIOs)
SmartCard ISO14443 / ISO7816	1	optionally provided by TSE
TAMPER	2	
UART	5	1 x incl. RTS/CTS
USB 2.0	2	
SD2 (SD-Card)	1	4 bit

3.2.6.2 ADC

The i.MX 93 has a 12-bit analog-digital converter with a reference voltage of 1.8 V and max. 4 channels.

Figure 7: Block diagram ADC

The reference voltage is provided on the module by the PMIC and is additionally filtered. The supply of an external reference voltage is not provided.

Table 10: Pin assignment ADC

Signal	i.MX 93	TQMa93xxCA	Power group
ADC_IN0	B19	X2-A51	VDD_ANA_1P8 (1.8 V)
ADC_IN1	A20	X2-A52	
ADC_IN2	B20	X2-A53	
ADC_IN3	B21	X2-A54	

3.2.6.3 CAN FD

The i.MX 93 provides two CAN FD interfaces. Both are specified according to the CAN 2.0B protocol but have different electrical properties due to their multiplexing. CAN1 has a 3.3 V level. The levels of CAN2 are dependent on the voltage V_GPIO which is set via connector pin X2-B46.

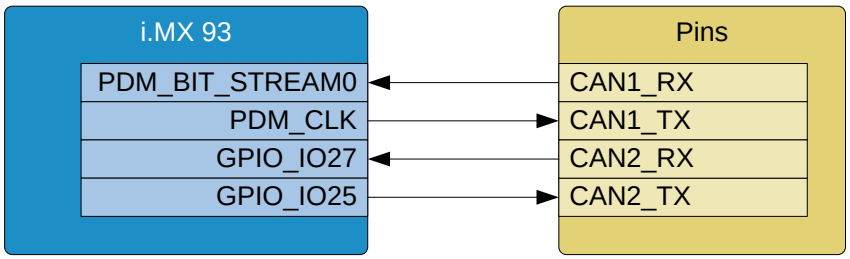

Figure 8: Block diagram CAN

Table 11: CAN FD signals

Signal	i.MX 93	TQMa93xxCAA	Power group
CAN1_TX	G17	X2-A40	NVCC_AON (3.3 V)
CAN1_RX	J17	X2-A39	
CAN2_TX	V21	X1-A57	NVCC_GPIO (1.8 V / 3.3 V)
CAN2_RX	W21	X1-A56	

3.2.6.4 Ethernet / RGMII

The i.MX 93 has two Ethernet MACs, each operating in maximum Gigabit full-duplex mode. MII, RMII or RGMII can be used as interfaces, the latter being used for standard multiplexing. Each MAC unit has its own MDIO/SMI interface. ENET1 supports both QOS (Quality-of-Service) and TSN (Time-sensitive Network).

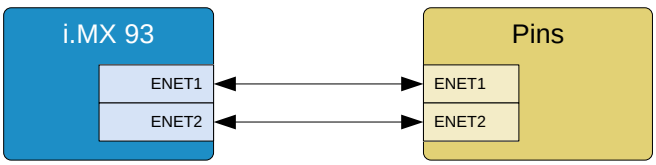

Figure 9: Block diagram RGMII

For RGMII an IO voltage of 1.8 V and for RMII an IO voltage of either 1.8 V or 3.3 V is specified. Due to an operation of both modes with 1.8 V the rail NVCC_WAKEUP is set to 1.8 V. The signals are length matched on the TQMa93xxCA and routed with a differential impedance of 100 Ω. On the carrier board they have to be connected according to RGMII specifications.

The following table shows the signals used in RGMII mode:

Table 12: ENET signals in RGMII mode

Signal	i.MX 93	TQMa93xxCA	Power group
ENET1_RX_CTL	Y8	X1-B15	NVCC_WAKEUP (1.8 V)
ENET1_RXC	AA7	X1-B13	
ENET1_RXD0	AA8	X1-B17	
ENET1_RXD1	Y9	X1-B18	
ENET1_RXD2	AA9	X1-B19	
ENET1_RXD3	Y10	X1-B20	
ENET1_TX_CTL	V10	X1-B7	
ENET1_TXC	U10	X1-B5	
ENET1_TXD0	W11	X1-B8	
ENET1_TXD1	T12	X1-B9	
ENET1_TXD2	U12	X1-B10	
ENET1_TXD3	V12	X1-B11	
ENET1_MDC	AA11	X1-B22	
ENET1_MDIO	AA10	X1-B23	
ENET2_RX_CTL	Y4	X2-A27	
ENET2_RXC	AA3	X2-A25	
ENET2_RXD0	AA4	X2-A28	
ENET2_RXD1	Y5	X2-A29	
ENET2_RXD2	AA5	X2-A30	
ENET2_RXD3	Y6	X2-A31	
ENET2_TX_CTL	V6	X2-A19	
ENET2_TXC	U6	X2-A17	
ENET2_TXD0	T8	X2-A20	
ENET2_TXD1	U8	X2-A21	
ENET2_TXD2	V8	X2-A22	
ENET2_TXD3	T10	X2-A23	
ENET2_MDC	Y7	X2-A34	
ENET2_MDIO	AA6	X2-A33	

3.2.6.5 I²C

The i.MX 93 provides up to eight I²C interfaces. I2C1 serves as system bus for internal components (RTC, EEPROM, temperature sensor, TSE, gyroscope and PMIC), has pull-ups on the module and is additionally available at connector pins.

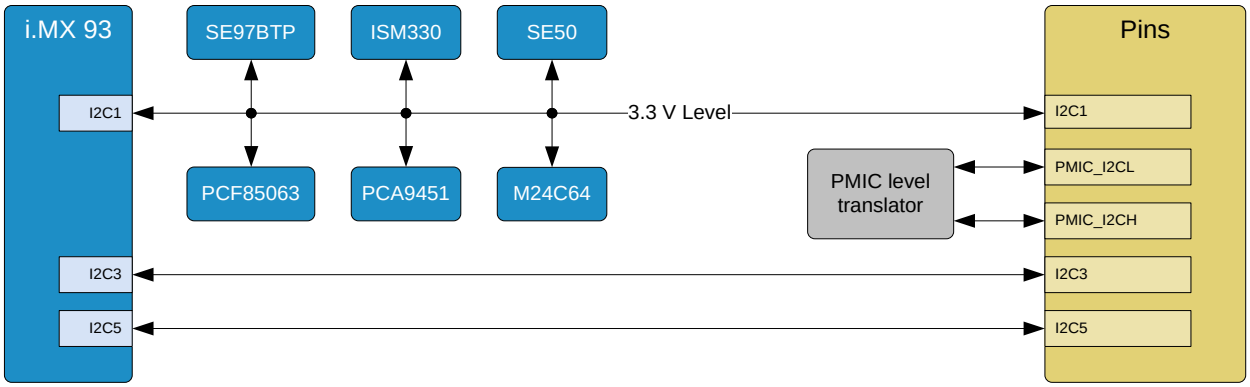

Figure 10: Block diagram I²C

I2C3 and I2C5 are provided as further buses, but without wiring on the TQMa93xxCA. Voltage levels and pull-up resistors are to be defined or placed outside the module.

The PMIC PCA9451 additionally provides an integrated I2C level translator. It is connected to four connector pins and can thus be used in customer designs. The corresponding wiring by means of pull-ups is to be provided outside TQMa93xxCA.

The TQMa93xxCA internal components with their associated addresses are listed in the following table.

Table 13: Address assignment I2C1 bus

Component	Function		7-bit address
PCA9451	PMIC		0x25 / 010 0101b
M24C64	EEPROM	Memory array	0x57 / 101 0111b
		Identification page (32 Byte)	0x5F / 101 1111b
PCF85063A	RTC		0x51 / 101 0001b
SE97BTP	EEPROM	Read / Write	0x53 / 101 0011b
		Protection command	0x33 / 011 0011b
	Temperature sensor in EEPROM		0x1B / 001 1011b
SE050 (optional)	Trust Secure Element		0x48 / 100 1000b
ISM330 (optional)	Gyroscope		0x6A / 110 1010b

The following table shows the I²C pin assignment on the TQMa93xxCA.

Table 14: Pin assignment I²C

Signal	i.MX 93	TQMa93xxCA	Power group
I2C1_SCL	C20	X2-A36	NVCC_AON (3.3 V)
I2C1_SDA	C21	X2-A37	
I2C3_SCL	Y21	X1-A59	NVCC_GPIO (1.8 V / 3.3 V)
I2C3_SDA	W20	X1-A60	
I2C5_SCL	U20	X1-A53	
I2C5_SDA	U18	X1-A54	
PMIC_SCLL	-	X1-A15	V_1V8
PMIC_SDAL	-	X1-A14	
PMIC_SCLH	-	X1-A11	V_3V3
PMIC_SDAH	-	X1-A12	

If more devices are connected to the I2C1 bus on the carrier board, the maximum capacitive bus load according to the I²C standard has to be taken note of. Additional pull-ups should be provided at the I²C bus on the carrier board, if required.

3.2.6.6 JTAG

The processor provides a JTAG interface that can be used to debug the programs executed on the processor. A corresponding hardware tool is required for this. The JTAG signals are routed directly to the connector pins. Pull resistors must be provided on the mainboard.

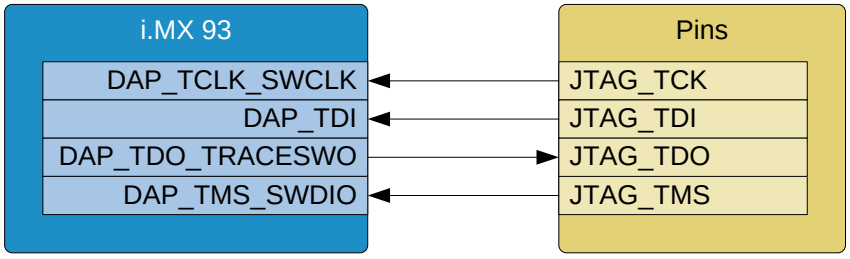

Figure 11: Block diagram JTAG interface

The following table shows the signals used by the JTAG interface. An external circuit on the mainboard has not to be provided.

Table 15: JTAG signals

Signal	i.MX 93	TQMa93xxCA	Power group
JTAG_TCK	Y1	X2-A12	NVCC_WAKEUP (1.8 V)
JTAG_TDI	W1	X2-A10	
JTAG_TDO	Y2	X2-A11	
JTAG_TMS	W2	X2-A13	

3.2.6.7 GPIO

Except for dedicated differential signals, e.g., MIPI DSI/CSI, and USB, most CPU signals routed to the TQMa93xxCAA connector pins can be configured as GPIO. GPIO1_IO03 is not routed to the outside and is used internally in the module to connect the open drain signal PMIC_IRQ_B. The electrical characteristics of the GPIOs are to be taken from the i.MX 93 Data Sheet (2).
The following table shows the GPIO signals primarily configured as GPIO:

Table 16: GPIO signals

Signal	i.MX 93	TQMa93xxCA	Power group
GPIO1_IO02	D20	X1-B38	NVCC_AON (3.3 V)
GPIO1_IO11	G21	X1-B58	
GPIO1_IO12	G20	X1-B57	
GPIO1_IO14	H20	X1-B56	
GPIO2_IO07	L21	X1-B44	NVCC_GPIO (1.8 V / 3.3 V)
GPIO2_IO10	N17	X1-B51	
GPIO2_IO11	N18	X1-B54	
GPIO2_IO24	U21	X1-A52	
GPIO3_IO26	AA2	X1-A5	NVCC_WAKEUP
GPIO3_IO27	Y3	X1-A7	
GPIO4_IO29	V4	X1-A9	

3.2.6.8 MIPI CSI

MIPI-CSI represents a differential camera interface. Up to 1.5 Gbps are transmitted on two data pairs. A resolution of up to 2K is possible as image format. The differential signals are length matched on the TQMa93xxCA and routed with a differential impedance of 100 Ω.

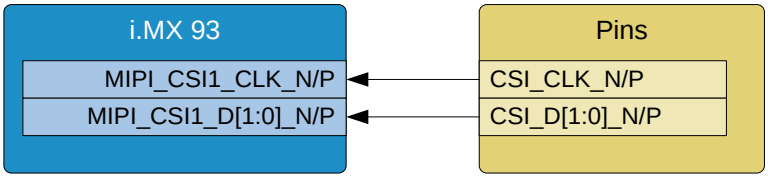

Figure 12: Block diagram MIPI CSI

The following table shows the signals used by the MIPI CSI interface.

Table 17: MIPI CSI signals

Signal	i.MX 93	TQMa93xxCA	Power group
CSI1_D0_N	A11	X2-B33	MIPI_CSI1_VPH (1.8 V)
CSI1_D0_P	B11	X2-B34	
CSI1_D1_N	A10	X2-B39	
CSI1_D1_P	B10	X2-B40	
CSI1_CLK_N	D10	X2-B36	
CSI1_CLK_P	E10	X2-B37	

3.2.6.9 MIPI DSI

The i.MX 93 provides a DSI interface with four data pairs to output serial display data at up to 1.5 Gbps.
The MIPI-DSI PHY supports resolutions up to 1920x1200 @ 60 fps.
The differential signals are length matched on the TQMa93xxCA and routed with a differential impedance of 100 Ω.

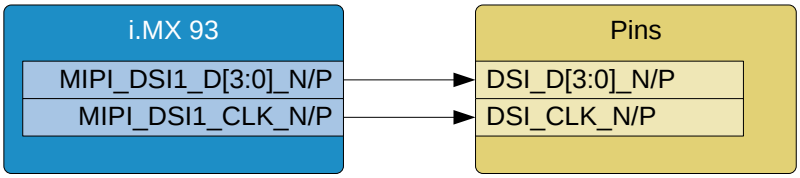

Figure 13: Block diagram MIPI DSI

The following table shows the signals used by the MIPI DSI interface.

Table 18: MIPI DSI signals

Signal	i.MX 93	TQMa93xxCA	Power group
DSI1_CLK_N	D6	X2-B24	MIPI_DSI1_VPH (1.8 V)
DSI1_CLK_P	E6	X2-B25	
DSI1_D0_N	A6	X2-B18	
DSI1_D0_P	B6	X2-B19	
DSI1_D1_N	A7	X2-B21	
DSI1_D1_P	B7	X2-B22	
DSI1_D2_N	A8	X2-B27	
DSI1_D2_P	B8	X2-B28	
DSI1_D3_N	A9	X2-B30	
DSI1_D3_P	B9	X2-B31	

3.2.6.10 LVDS

The i.MX 93 has an LVDS controller with four differential lanes for data transmission. The LVDS PHY supports outputs up to 1366 x 768 pixels at 60 FPS. The differential signals are length matched on the TQMa93xxCA and routed with a differential impedance of 100 Ω.

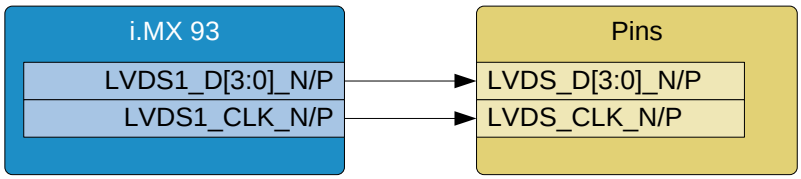

Figure 14: Block diagram LVDS

Table 19: LVDS signals

Signal	i.MX 93	TQMa93xxCA	Power group
LVDS0_D0_N	A5	X2-B14	VDD_LVDS_1P8 (1.8 V)
LVDS0_D0_P	B5	X2-B13	
LVDS0_D1_N	A4	X2-B11	
LVDS0_D1_P	B4	X2-B10	
LVDS0_D2_N	A2	X2-B8	
LVDS0_D2_P	B2	X2-B7	
LVDS0_D3_N	B1	X2-B2	
LVDS0_D3_P	C1	X2-B1	
LVDS0_CLK_N	A3	X2-B5	
LVDS0_CLK_P	B3	X2-B4	

3.2.6.11 SAI

The i.MX 93 has several SAI interfaces with different data bus widths. Due to limited multiplexing options, only the SAI3 interface is provided at the connector pins. SAI2 as the most extensive SAI interface (4-bit) can only be used if the second Ethernet interface is omitted.

The SAI interface is full-duplex capable and supports I2S, AC97, TDM and other codec interfaces.

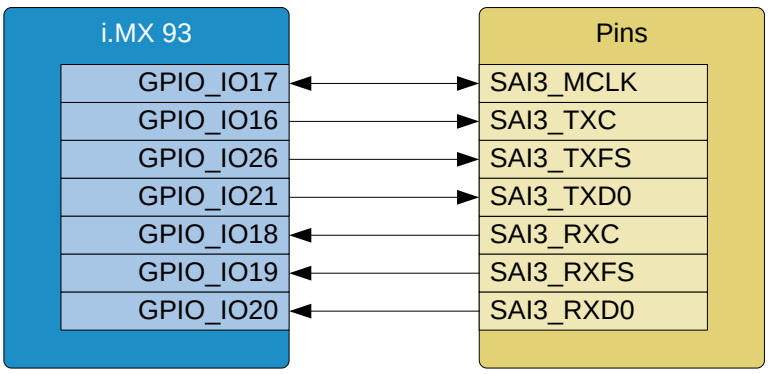

Figure 15: Block diagram SAI3

The following table lists all SAI signals provided by the TQMa93xxCA:

Table 20: SAI signals

Signal	i.MX 93	TQMa93xxCA	Power group
SAI3_MLCK	R20	X1-A36	NVCC_GPIO (1.8 V / 3.3 V)
SAI3_TXC	R21	X1-A40	
SAI3_TXFS	V20	X1-A39	
SAI3_TXD0	T21	X1-A38	
SAI3_RXD0	T20	X1-A42	
SAI3_RXFS	R17	X1-A43	
SAI3_RXC	R18	X1-A44	

3.2.6.12 SPI

The TQMa93xxCA provides in the TQ standard multiplexing a SPI interface, which can be operated in both master and slave mode.

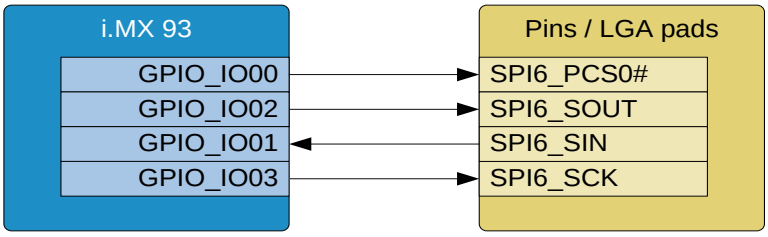

Figure 16: Block diagram SPI

Table 21: Pinning SPI

Signal	i.MX 93	TQMa93xxCA	Power group
SPI6_PCS0#	J21	X1-B46	NVCC_GPIO (1.8 V / 3.3 V)
SPI6_SIN	J20	X1-B47	
SPI6_SOUT	K20	X1-B48	
SPI6_SCK	K21	X1-B49	

3.2.6.13 Tamper

As one of the safety functions of the BBSM unit of the i.MX 93, a total of two tamper signals are provided - one active and one passive. These are routed to the outside without any further circuitry.

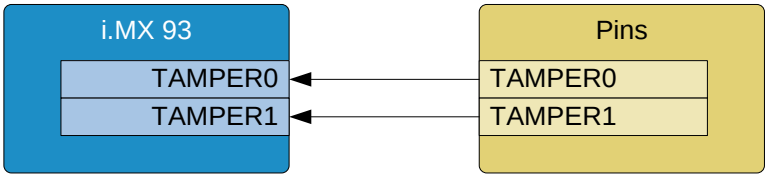

Figure 17: Block diagram Tamper

Table 22: Pinning Tamper

Signal	i.MX 93	TQMa93xxCA	Power group
TAMPER0	B16	X2-A43	NVCC_BBSM (1.8 V)
TAMPER1	F14	X2-A44	

3.2.6.14 UART

In standard multiplexing five of eight possible UART interfaces are provided.
If less UARTs are required in customer applications, further interfaces, e.g. SPI or I2C, can be multiplexed at the same CPU pins.

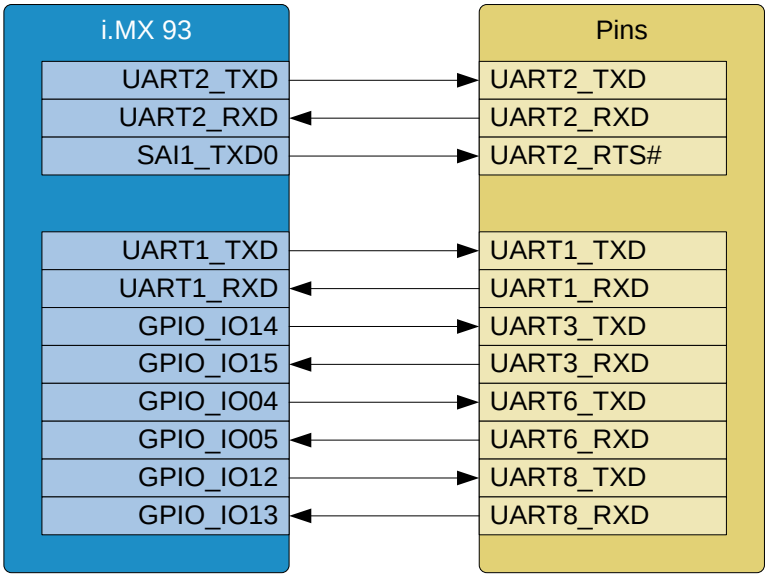

Figure 18: Block diagram UART interfaces

The following table shows the signals used by the UART interfaces.

Table 23: UART signals

Signal	i.MX 93	TQMa93xxCA	Power group
UART1_RXD	E20	X2-A56	NVCC_AON (3.3 V)
UART1_TXD	E21	X2-A57	
UART2_RXD	F20	X2-A58	
UART2_TXD	F21	X2-A59	
UART3_RXD	P21	X1-A50	NVCC_GPIO (1.8 V / 3.3 V)
UART3_TXD	P20	X1-A49	
UART6_RXD	L18	X1-B40	
UART6_TXD	L17	X1-B41	
UART8_RXD	N21	X1-A47	
UART8_TXD	N20	X1-A46	

3.2.6.15 USB

The i.MX 93 has two USB 2.0 OTG controllers, each providing device, host or OTG ports at high speed (480 Mbps). The OTG signals are not available by default because their multiplexing overlaps with the ENET1 interface.

Up to 5 V can be applied to the VBUS pins. The 30 kΩ resistors required by NXP are already provided on the module. The differential signals are length matched on the TQMa93xxCA and routed with a differential impedance of 90 Ω.

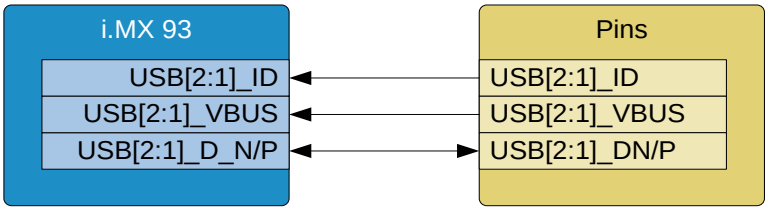

Figure 19: Block diagram USB interfaces

Table 24: USB signals

Signal	i.MX 93	TQMa93xxCA	Power group
USB1_ID	C11	X2-B43	VDD_USB_1P8 (1.8 V)
USB2_ID	E12	X2-B44	
USB1_DN	A14	X2-B57	VDD_USB_3P3 (3.3 V)
USB1_DP	B14	X2-B56	
USB1_VBUS	F12	X2-B47	
USB2_DN	A15	X2-B60	
USB2_DP	B15	X2-B59	
USB2_VBUS	E14	X2-B48	

3.2.6.16 SD2 (SD-Card)

The i.MX 93 supports SD cards up to UHS-I in SDR104/DDR50 mode. This corresponds to SD card specification v3.0 and a maximum data width of 4 bit.

To enable booting from SD cards, the SD2 interface is routed to connector pins with the exception of SD2_VSELECT. SD2_RESET_B is available at a connector pin, but can remain unconnected because the actual reset function of this signal is already implemented on TQMa93xxCA.

The signals of the SD2 interface are supplied by a separate PMIC LDO whose IO voltage can be set to a 1.8 V or 3.3 V range by the signal SD2_VSELECT. SD2_VSELECT is automatically switched by the driver so that the fastest possible mode is used depending on the SD card used. The default setting at boot is 3.3 V.

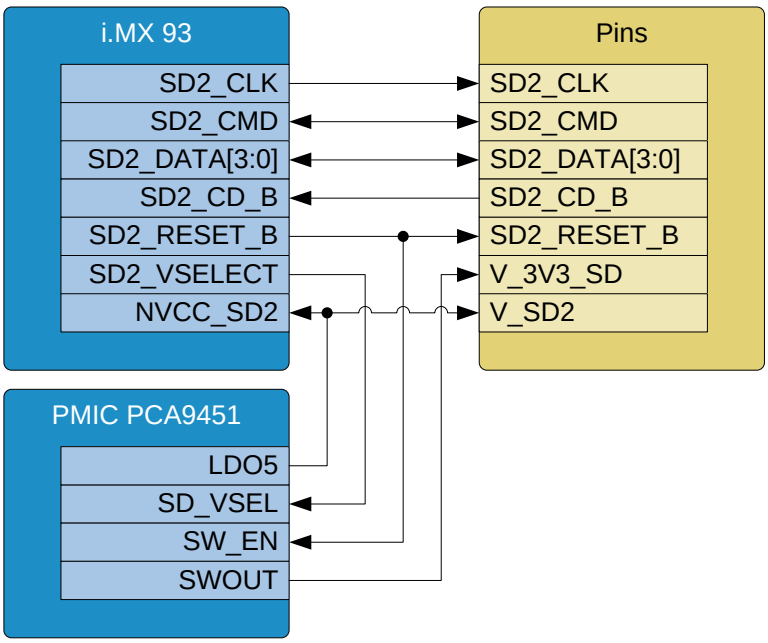

Figure 20: Block diagram SD card interface

Additionally the supply voltage V_SD2 is provided externally by the TQMa93xxCA. In customer designs this voltage can be used to connect the pull-up resistors of the SD card interface. Alternatively the use of CPU internal pull-up resistors is possible.

The voltage V_3V3_SD serves as main supply for SD cards. The TQMa93xxCA-internal wiring allows to interrupt the SD card supply at a module reset and thus to enable a reset of the SD card.

Table 25: SD2 signals

Signal	i.MX 93	TQMa93xxCA	Power group
SD2_CD#	Y17	X1-A20	NVCC_SD2 (1.8 V / 3.3 V)
SD2_CLK	AA19	X1-A17	
SD2_CMD	Y19	X1-A19	
SD2_DATA0	Y18	X1-A22	
SD2_DATA1	AA18	X1-A23	
SD2_DATA2	Y20	X1-A24	
SD2_DATA3	AA20	X1-A25	
SD2_RST#	AA17	X1-A27	

3.2.6.17 External clock sources

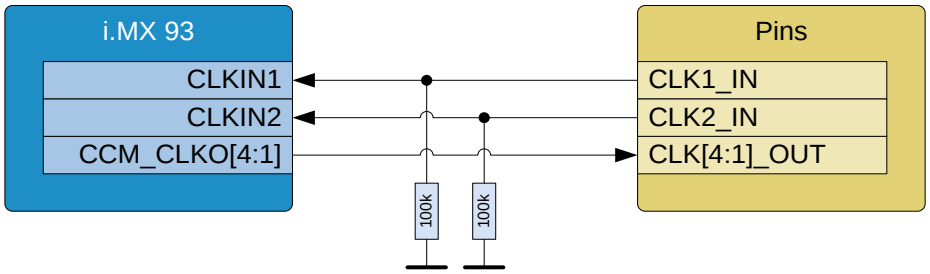

Figure 21: Block diagram external clocks

The i.MX 93 has the option to use two external oscillators as clock sources. Depending on the configuration of the internal clock tree, further reference clocks can be created.
All six i.MX 93 signals provided for this purpose are routed to TQMa93xxCA pins. The following table shows these clock signals.

Table 26: CLK signals

Signal	i.MX 93	TQMa93xxCA	Power group
CLK1_IN[5]	B17	X2-A46	VDD_ANA_1P8 (1.8 V)
CLK2_IN[5]	A18	X2-A47	
CLK1_OUT	AA2	X1-A5	NVCC_WAKEUP (1.8 V)
CLK2_OUT	Y3	X1-A7	
CLK3_OUT[5]	U4	X1-A8	
CLK4_OUT	V4	X1-A9	

[5] Default multiplexing

3.2.6.18 TPM / PWM

The TPM (Timer/PWM Module) of the i.MX 93 is a multi-channel timer that supports input capture, output compare, and the generation of PWM signals to control electrical motor and power management applications. The counter, compare, and capture registers are clocked by an asynchronous clock that can remain enabled in low power modes.

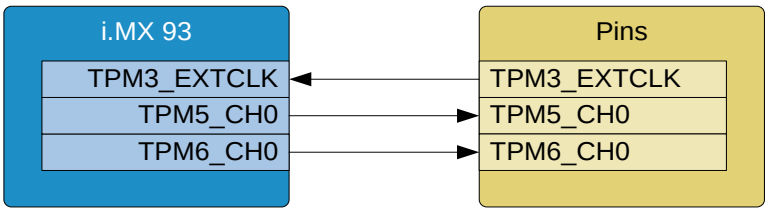

Figure 22: Block diagram TPM

Table 27: TPM Signals

Signal	i.MX 93	TQMa93xxCA	Power group
TPM3_EXTCLK	M21	X1-B52	V_GPIO (1.8 V / 3.3 V)
TPM5_CH0	L20	X1-B43	
TPM6_CH0	M20	X1-B53	

3.2.7 Reset and unspecific signals

Two reset options are provided by the TQMa93xxCA. A reset is triggered by the signal PMIC_RST#. This signal is fed to the PMIC from outside, is low-active and has an internal pull-up. By default, the PMIC is configured so that activation triggers a cold reset. The cold reset is a power cycle, with the exception of the LDO1 controller. The BBSM voltage is thus retained.

A second reset possibility is given by the signal PMIC_WDOG_IN#. This is a 3.3 V signal which has a pull-up on the module. The corresponding PMIC behavior can be set via I2C. By default, a response to this signal is disabled.

The ONOFF pin of the CPU offers two reaction possibilities. It has an internal pull-up and is low-active. If this signal is held low for more than 5 s, the CPU enters OFF mode. If the signal is briefly pulled low in OFF mode, the CPU switches back to ON mode. A short low impuls in ON mode triggers an interrupt.

In addition, a reset is triggered by a module-internal supervisor when the module supply voltage drops.

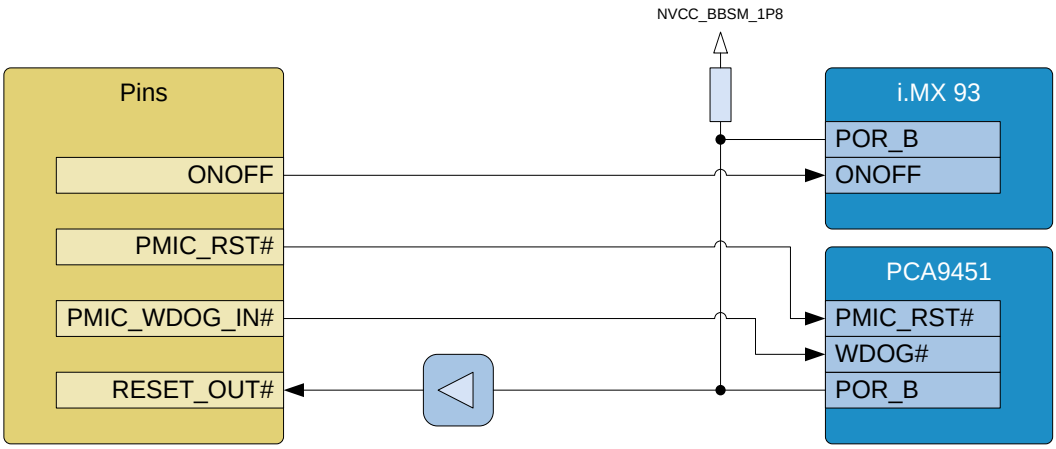

Figure 23: Block diagram Reset

RESET_OUT# is an open-drain output and is routed to a connector pin. In customer applications, this ensures feedback on a reset of the module to external components. In customer designs a pull-up is required at this output.

Table 28: Reset and unspecific signals

Signal	i.MX 93	Power group	Remark
PMIC_RST#	-	NVCC_BBSM (1.8 V)	• No pull-up on carrier board required; low-active. • Programmable PMIC response (warm / cold reset).
ONOFF	[A19] ONOFF		• ON/OFF function of the i.MX 93. • No pull-up on carrier board required; low-active. • Pull to GND for 5 s to activate.
RESET_OUT#	[A16] POR_B		• Open drain output; low-active. • Activates RESET of carrier board components. • External pull-up required.
M33_NMI	[G18] PDM_BIT_STREAM1	NVCC_AON (3.3 V)	
WDOG_ANY	[J18] WDOG_ANY		
PMIC_WDOG_IN#	-	BUCK4 (3.3 V)	
RTC_EVENT#	-	Open Drain	
TEMP_EVENT#	-		

3.2.8 Power

3.2.8.1 Power supply

The TQMa93xxCA requires a main supply voltage of 5 V ±5 %. All power supply and ground pins should be connected.

Through V_LICELL the TQMa93xxCA has an input for the backup voltage supply of the optional discrete RTC PCF85063A. Please refer to chapter 3.2.5.2

The characteristics and functions of a certain pin or signal is to be taken from the PMIC Data Sheet (4), and the i.MX 93 Data Sheet (2).

3.2.8.2 Configurable voltages

V_GPIO must be powered by the baseboard to supply the CPU rail NVCC_GPIO. The required voltage is either 1.8 V (1.65…1.95 V) or 3.3 V (3.00…3.60 V).

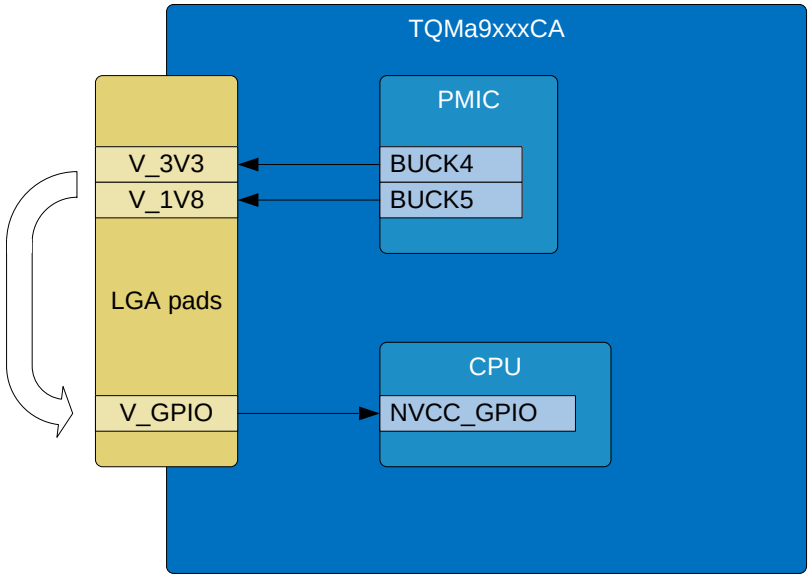

Figure 24: Possible power supply of the CPU-rail NVCC_GPIO

Attention: Destruction or malfunction	
	If V_GPIO is not connected to a power supply the corresponding CPU-Rail is not powered. This can cause malfunction or damage the CPU.

3.2.8.3 Power consumption

The given power consumption has to be seen as an approximate value.
The TQMa93xxCA power consumption strongly depends on the application, the mode of operation and the operating system.

The following table shows TQMa93xxCA power supply and power consumption parameters:

Table 29: Power consumption

Mode of operation	Current @ 5 V	Power consumption @ 5 V
Theoretical calculated peak (worst case)	2.5 A	12.5 W
U-Boot prompt	208 mA	1040 mW
Linux prompt	154 mA	770 mW
Linux stress test	265 mA	1325 mW
Reset	118 µA	590 µW

3.2.8.4 Voltage monitoring

The TQMa93xxCA features a supervisor which monitors the input voltage (V_{IN}).
If the input voltage drops below 4.38 V, a Reset (PMIC_ON_REQ) is triggered and the TQMa93xxCA is held in reset until the input voltage is in the permitted range again.

Attention: Destruction or malfunction, supply voltage exceedance	
	The voltage monitoring does not detect an exceedance of the permitted input voltage. An exceedance of the permitted input voltage may cause malfunction, destruction or accelerated ageing of the TQMa93xxCA.

3.2.8.5 Supply outputs

The TQMa93xxCA provides three voltages that can be used on the carrier board.

Table 30: Voltages provided by TQMa93xxCA

Voltage	TQMa93xxCA	Usage	Max. load
V_1V8	X1-A34	General usage on carrier board	500 mA
V_3V3	X1-A33	General usage on carrier board	500 mA
V_3V3_SD	X1-A31	SD card supply	400 mA

The voltage V_3V3 can be used as Power-Good signal for the supply of circuitry on the carrier board.

Attention: Destruction or malfunction, current exceedance	
	A load of up to 500 mA at V_1V8 or V_3V3, as well as up to 400 mA at V_3V3_SD causes an increased power consumption of the TQMa93xxCA and thus a higher self-heating. These three voltages are outputs and must never be supplied from external sources! Furthermore the outputs are not short-circuit proof. Overloading the voltage outputs can damage the TQMa93xxCA.

3.2.8.6 Power-Up sequence TQMa93xxCA / carrier board

As the TQMa93xxCA operates with 5 V and the I/O voltages of the CPU signals are generated on the TQMa93xxCA, there are timing requirements for the carrier board design with respect to the voltages generated on the carrier board:
After power up of the 5V supply for the TQMa93xxCA, the PMIC power-up sequence starts. External TQMa93xxCA inputs driven by the carrier board may only be switched on after the power-up of V_3V3. Connector pin X1-A33 (V_3V3) can be used as feedback.

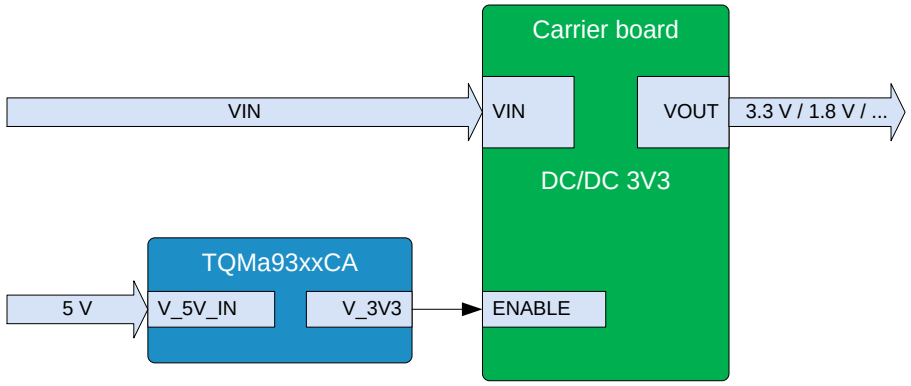

Figure 25: Block diagram power supply carrier board

Attention: Destruction or malfunction, Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the power-up sequence is indicated by a high level of signal V_3V3, connector pin X1-A33.

3.2.8.7 Standby and BBSM

In standby mode, several voltage controllers on the TQMa93xxCA are switched off.
The rail V_1V8_BBSM remain active, which ensures the correct function of the BBSM.

3.2.8.8 PMIC

The characteristics and functions of all pins and signals have to be taken from the i.MX 93 Reference Manual (1) and the PMIC Data Sheet (4). The PMIC is controlled by the I2C1 bus.

- The PMIC has I²C address `0x25 / 010 0101b`

The following PMIC and power management signals are available on the TQMa93xxCA connector pins

Table 31: PMIC signals

Signal	Direction	TQMa93xxCA	Power group	Remark
PMIC_WDOG_IN#	I	X2-A49	3.3 V	• Low-active input
PMIC_RST#	I	X1-B36	1.8 V	• Low-active input
RESET_OUT#	O	X1-B37	1.8 V	• Low-active output • Connected to PMIC POR# • Can signal a TQMa93xxCA reset
SD_VSEL	–	–	–	• See chapter 3.2.6.16

Attention: Destruction or malfunction, PMIC programming	
	Improper programming of the PMIC may result in the i.MX 93 or periphery being operated outside its specification. This may lead to malfunctions, accelerated aging or destruction of the TQMa93xxCA.

3.2.9 Impedances

By default, all single-ended signals have a nominal impedance of 50 Ω ±10 %.
However, some interfaces on the TQMa93xxCA are routed with different impedances, depending on the signal requirements.

The following table is taken from the Hardware Developer's Guide (3) and shows the respective interfaces:

Table 32: Trace impedance recommendations

Signal / Interface	Impedance on TQMa93xxCA	Recommendation for carrier board
DDR DQS/CLK	85 Ω, differential	85 Ω ±10 %, differential
Differential USB signals	90 Ω, differential	90 Ω ±10 %, differential
Differential signals, including Ethernet, MIPI (CSI and DSI), LVDS	100 Ω, differential	100 Ω ±10 %, differential

4. SOFTWARE

The TQMa93xxCA is delivered with a preinstalled boot loader U-Boot.
The BSP provided by TQ-Systems GmbH is configured for the combination of TQMa93xxCA and MBa93xxCA.
The boot loader U-Boot provides TQMa93xxCA-specific as well as board-specific settings, e.g.:

- i.MX 93 configuration
- PMIC configuration
- SDRAM configuration
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

Further information can be found in the https://support.tq-group.com/TQMa93xxCA.

If another bootloader is used, this data must be adapted. Contact TQ-Support for detailed information.

5. MECHANICS

5.1 Dimensions

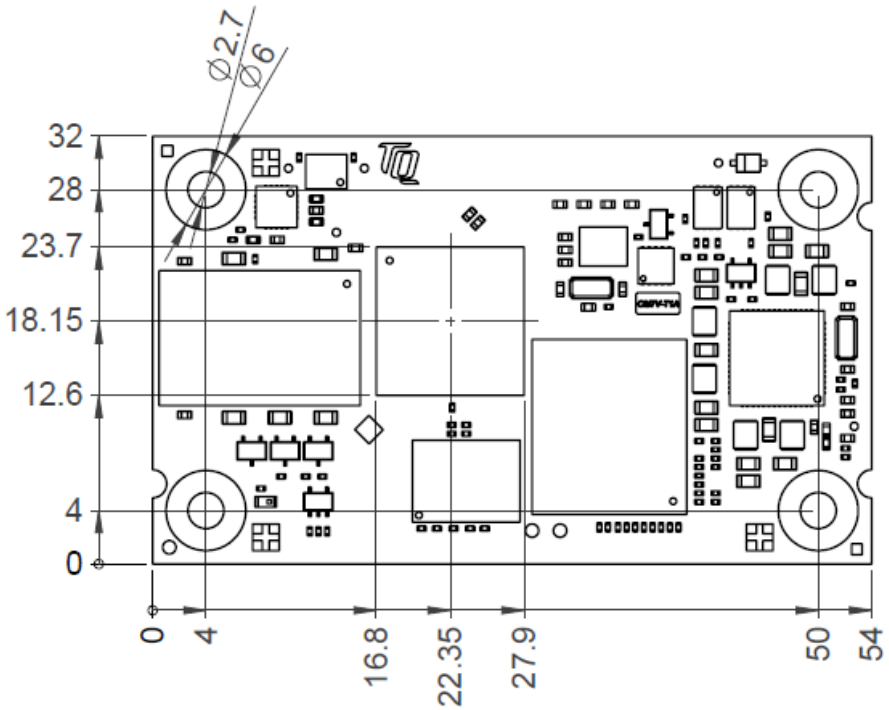

Figure 26: TQMa93xxCA dimensions, top view (dimensions in mm)

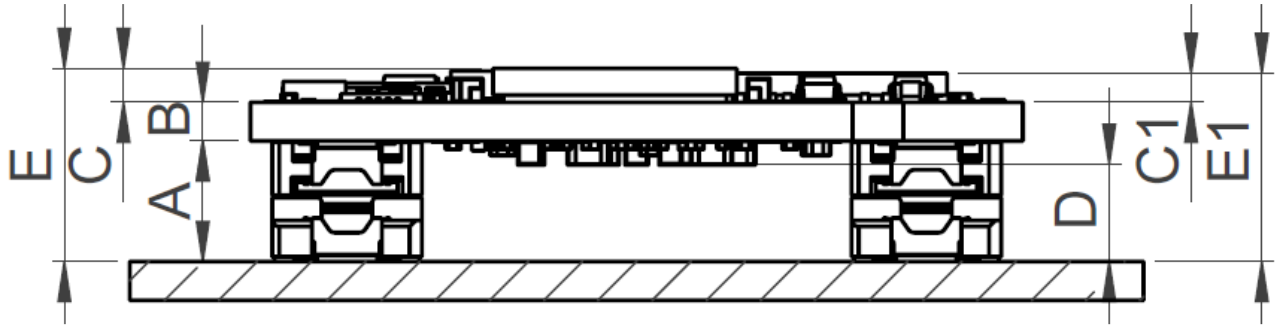

Figure 27: TQMa93xxCA dimensions, side view

Table 33: TQMa93xxCA heights

Dim.	Value	Tolerance	Remark
A	5.10 mm	+0.07 mm	Board to board distance
B	1.60 mm	±0.16 mm	PCB without solder resist
C	1.05 mm	±0.10 mm	Height of CPU
C1	1.08 mm	±0.06 mm	Height of NOR Flash
D	4.25 mm	±0.21 mm	Space below module
E	7.75 mm	±0.20 mm	Overall height to CPU surface
E1	7.78 mm	±0.18 mm	Overall height to NOR Flash

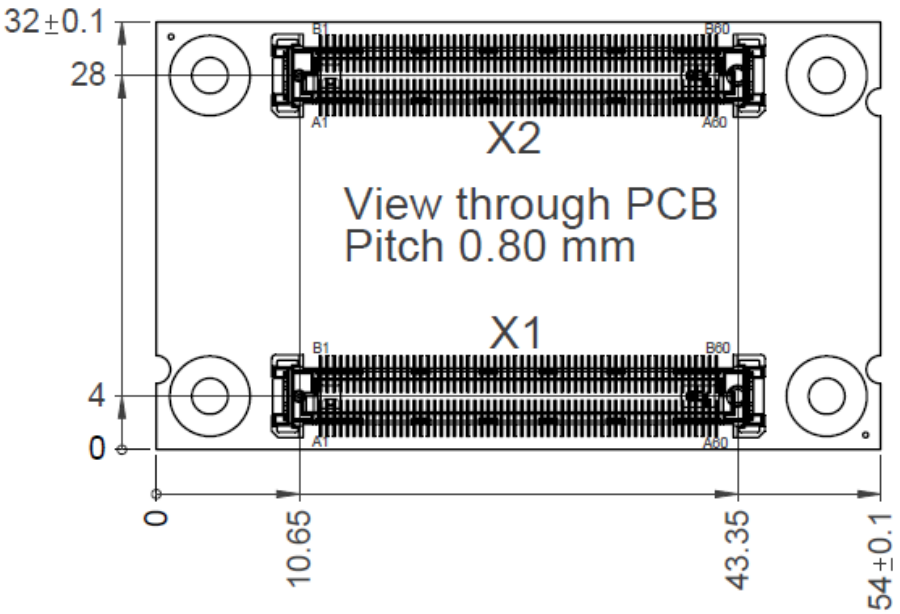

Figure 28: TQMa93xxCA dimensions (in mm), view through PCB

5.2 Component placement and labeling

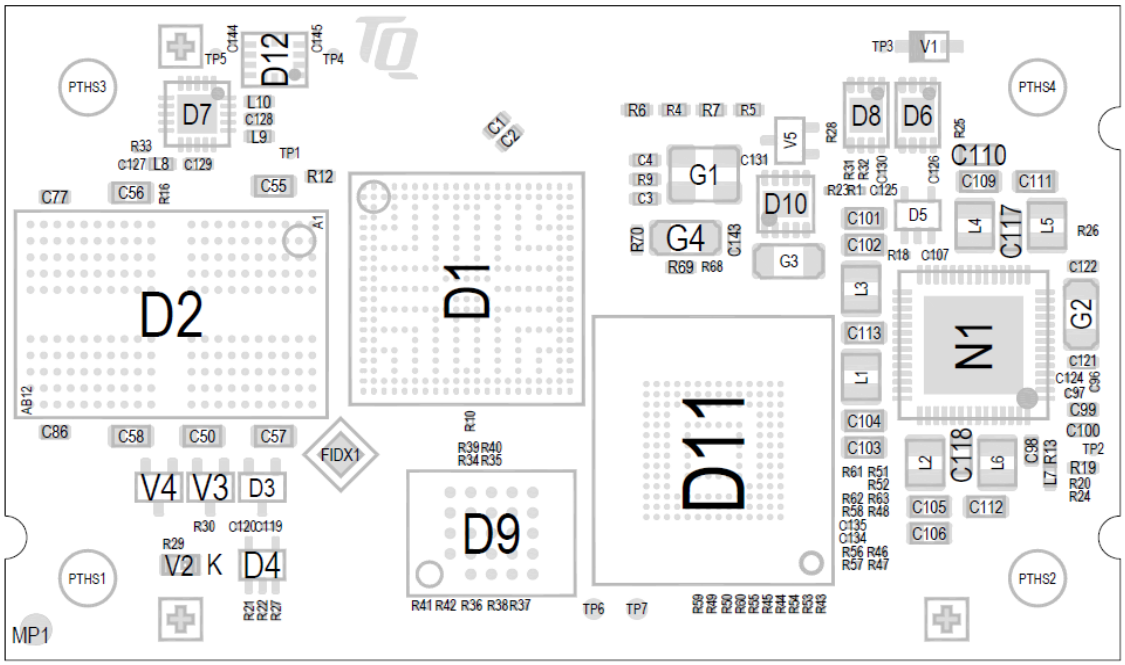

Figure 29: TQMa93xxCA, component placement top

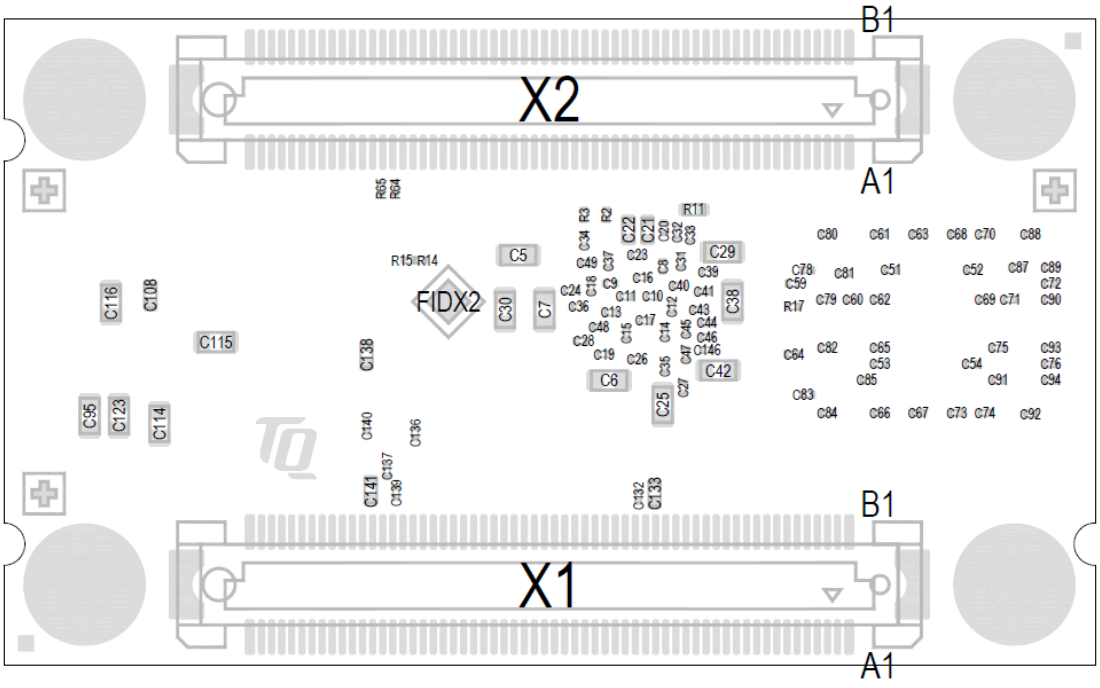

Figure 30: TQMa93xxCA, bottom view

The labels on the TQMa93xxCA show the following information:

Table 34: Labels on TQMa93xxCA

Label	Content
AK1	Serial number
AK2	MAC address
AK3	TQMa93xxCA version and revision

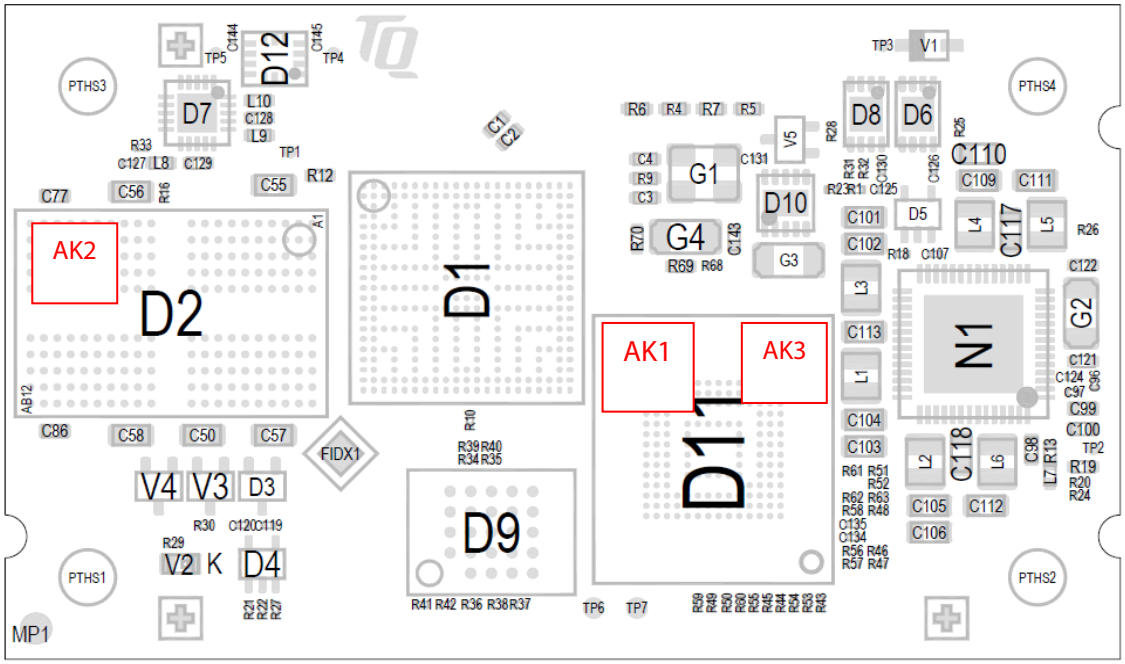

Figure 31: Labels on TQMa93xxCA

5.3 Adaptation to the environment

The TQMa93xxCA has overall dimensions (length × width) of 32 mm × 54.0 mm (± 0.1 mm).
The TQMa93xxCA has a maximum height above the carrier board of approximately 7.78 mm (± 0.18 mm).
The TQMa93xxCA has two 120-pin connectors (240 pins in total) with a pitch of 0.50 mm.
The TQMa93xxCA weighs approximately 11 g.

5.4 Protection against external effects

The TQMa93xxCA does not provide protection against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

5.5 Thermal management

To cool the TQMa93xxCA, note Table 29. The power dissipation originates primarily in the i.MX 93, the LPDDR4 SDRAM and the PMIC.
The power dissipation also depends on the software used and can vary according to the application.
See NXP documents (6) and (7) for further information.

Attention: Destruction or malfunction, TQMa93xxCA cooling	
	The i.MX 93 belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 93 must be taken into consideration when connecting the heat sink, see (6). The i.MX 93 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa93xxCA and thus malfunction, deterioration or destruction.

5.6 Structural requirements

The TQMa93xxCA is held in the mating connectors by the retention force of the pins (240). For high requirements with respect to vibration and shock firmness, an additional retainer has to be provided in the final product to hold the TQMa93xxCA in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa93xxCA was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.
Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be arranged directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special preventive measures were planned on the TQMa93xxCA.
Following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diode(s)
- Slow signals: RC filtering, Zener diode(s)
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Intended Use

TQ DEVICES, PRODUCTS AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION IN NUCLEAR FACILITIES, AIRCRAFT OR OTHER TRANSPORTATION NAVIGATION OR COMMUNICATION SYSTEMS, AIR TRAFFIC CONTROL SYSTEMS, LIFE SUPPORT MACHINES, WEAPONS SYSTEMS, OR ANY OTHER EQUIPMENT OR APPLICATION REQUIRING FAIL-SAFE PERFORMANCE OR IN WHICH THE FAILURE OF TQ PRODUCTS COULD LEAD TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE. (COLLECTIVELY, "HIGH RISK APPLICATIONS")

You understand and agree that your use of TQ products or devices as a component in your applications are solely at your own risk. To minimize the risks associated with your products, devices and applications, you should take appropriate operational and design related protective measures.

You are solely responsible for complying with all legal, regulatory, safety and security requirements relating to your products. You are responsible for ensuring that your systems (and any TQ hardware or software components incorporated into your systems or products) comply with all applicable requirements. Unless otherwise explicitly stated in our product related documentation, TQ devices are not designed with fault tolerance capabilities or features and therefore cannot be considered as being designed, manufactured or otherwise set up to be compliant for any implementation or resale as a device in high risk applications. All application and safety information in this document (including application descriptions, suggested safety precautions, recommended TQ products or any other materials) is for reference only. Only trained personnel in a suitable work area are permitted to handle and operate TQ products and devices. Please follow the general IT security guidelines applicable to the country or location in which you intend to use the equipment.

6.4 Export Control and Sanctions Compliance

The customer is responsible for ensuring that the product purchased from TQ is not subject to any national or international export/import restrictions. If any part of the purchased product or the product itself is subject to said restrictions, the customer must procure the required export/import licenses at its own expense. In the case of breaches of export or import limitations, the customer indemnifies TQ against all liability and accountability in the external relationship,irrespective of the legal grounds. If there is a transgression or violation, the customer will also be held accountable for any losses, damages or fines sustained by TQ. TQ is not liable for any delivery delays due to national or international export restrictions or for the inability to make a delivery as a result of those restrictions. Any compensation or damages will not be provided by TQ in such instances.

The classification according to the European Foreign Trade Regulations (export list number of Reg. No. 2021/821 for dual-use-goods) as well as the classification according to the U.S. Export Administration Regulations in case of US products (ECCN according to the U.S. Commerce Control List) are stated on TQ´s invoices or can be requested at any time. Also listed is the Commodity code (HS) in accordance with the current commodity classification for foreign trade statistics as well as the country of origin of the goods requested/ordered.

6.5 Warranty

TQ-Systems GmbH warrants that the product, when used in accordance with the contract, fulfills the respective contractually agreed specifications and functionalities and corresponds to the recognized state of the art.

The warranty is limited to material, manufacturing and processing defects. The manufacturer's liability is void in the following cases:

- Original parts have been replaced by non-original parts.
- Improper installation, commissioning or repairs.
- Improper installation, commissioning or repair due to lack of special equipment.
- Incorrect operation
- Improper handling
- Use of force
- Normal wear and tear

6.6 Shock and Vibration

Table 35: Shock resistance

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 ms
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 36: Vibration resistance

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 ~ 9 Hz, 9 ~ 200 Hz, 200 ~ 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Acceleration	2 Hz to 9 Hz: 3.5 m/s^2 9 Hz to 200 Hz: 10 m/s^2 200 Hz to 500 Hz: 15 m/s^2

6.7 Climate and operational conditions

The TQMa93xxCA is available in different variants with different ambient temperature ranges. The operating temperature range for the TQMa93xxCA strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa93xxCA.

In general, a reliable operation is given when following conditions are met:

Table 37: Climate and operational conditions

Parameter		Range	Remark
Ambient temperature TQMa93xxCA	Standard	–25 °C to +85 °C	–
	Extended	–40 °C to +85 °C	–
T_J temperature i.MX 93		–40 °C to +105 °C	–
T_J temperature PMIC		–40 °C to +125 °C	–
Case temperature LPDDR4		–40 °C to +95 °C	–
Case temperature other ICs	Standard	–25 °C to +85 °C	–
	Extended	–40 °C to +85 °C	–
Storage temperature TQMa93xxCA		–40 °C to +100 °C	–
Relative humidity (operating / storage)		10 % to 90 %	Not condensing

Detailed information concerning the i.MX 93 thermal characteristics is to be taken from NXP documents (6) and (7).

Attention: Destruction or malfunction, TQMa93xxCA cooling	
	The i.MX 93 belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 93 must be taken into consideration when connecting the heat sink, see (6). The i.MX 93 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa93xxCA and thus malfunction, deterioration or destruction.

6.8 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.9 Reliability and service life

The MTBF calculated for the TQMa93xxCA is 1,107,304 hours with a constant error rate @ +40 °C, Ground Benign. The TQMa93xxCA is designed to be insensitive to shock and vibration.

The TQMa93xxCA must be assembled in accordance with the processing instructions provided by TQ-Systems GmbH.

Detailed information concerning the i.MX 93 service life under different operational conditions is to be taken from the NXP Application Note (7).

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa93xxCA is manufactured RoHS compliant. All components, assemblies and soldering processes are RoHS compliant.

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa93xxCA was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Energy using Products (EuP) is applicable for end user products with an annual quantity of >200,000. Thus the TQMa93xxCA always has to be considered in combination with the complete system. The compliance regarding EuP directive is basically possible for the TQMa93xxCA on account of available Standby or Sleep-Modes of the components on the TQMa93xxCA.

7.5 Statement on California Proposition 65

California Proposition 65, formerly known as the Safe Drinking Water and Toxic Enforcement Act of 1986, was enacted as a ballot initiative in November 1986. The proposition helps protect the state's drinking water sources from contamination by approximately 1,000 chemicals known to cause cancer, birth defects, or other reproductive harm ("Proposition 65 Substances") and requires businesses to inform Californians about exposure to Proposition 65 Substances.

The TQ device or product is not designed or manufactured or distributed as consumer product or for any contact with end-consumers. Consumer products are defined as products intended for a consumer's personal use, consumption, or enjoyment. Therefore, our products or devices are not subject to this regulation and no warning label is required on the assembly.

Individual components of the assembly may contain substances that may require a warning under California Proposition 65. However, it should be noted that the Intended Use of our products will not result in the release of these substances or direct human contact with these substances. Therefore you must take care through your product design that consumers cannot touch the product at all and specify that issue in your own product related documentation.

TQ reserves the right to update and modify this notice as it deems necessary or appropriate.

7.6 Battery

No batteries are assembled on the TQMa93xxCA.

7.7 Packaging

The TQMa93xxCA is delivered in reusable packaging.

7.8 Other entries

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa93xxCA, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa93xxCA is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 38: Acronyms

Acronym	Meaning
ARM®	Advanced RISC Machine
BBSM	Battery Backed Secure Module
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CAN-FD	CAN with Flexible Data-Rate
CPU	Central Processing Unit
CSI	CMOS Sensor Interface
DDR	Double Data Rate
DIN	Deutsche Industrienorm (German industry standard)
DNC	Do Not Connect
DSI	Display Serial Interface
EARC	Enhanced Audio Return Channel
ECSPI	Enhanced Configurable SPI
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card (Flash)
EN	Europäische Norm (European standard)
ESD	Electrostatic Discharge
EuP	Energy using Products
FR-4	Flame Retardant 4
Gbps	Gigabit per second
GPIO	General Purpose Input/Output
GPT	General-Purpose Timer
HDMI	High-Definition Multimedia Interface
I	Input
I/O	Input/Output
I^2C	Inter-Integrated Circuit
IP00	Ingress Protection 00
IPU	Input with Pull-Up
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LGA	Land Grid Array
LPDDR4	Low Power DDR4
LVDS	Low-Voltage Differential Signaling
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
ML/AI	Machine Learning / Artificial Intelligence
MMC	Multimedia Card
MTBF	Mean operating Time Between Failures

8.1 Acronyms and definitions (continued)

Table 38: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NOR	Not-Or
O	Output
OD	Open Drain
OOD	Output with Open Drain
OTG	On-The-Go
P	Power
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PD	Pull-Down (resistor)
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PU	Pull-Up (resistor)
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RC	Resistor-Capacitor
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protection
SAI	Serial Audio Interface
SCU	System Control Unit
SD	Secure Digital
SDRAM	Synchronous Dynamic Random Access Memory
SNVS	Secure Non-Volatile Storage
SPDIF	Sony-Philips Digital Interface Format
SPI	Serial Peripheral Interface
SVHC	Substances of Very High Concern
TBD	To Be Determined
TSE	Trust Secure Element
UART	Universal Asynchronous Receiver/Transmitter
UM	User's Manual
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment
WP	Write-Protection

8.2 References

Table 39: Further applicable documents

No.	Name	Rev., Date	Company
(1)	i.MX 93 Applications Processor Reference Manual	Rev. 1, Oct 2022	NXP
(2)	i.MX 93 Industrial Application Processors Data Sheet	Rev F, Sep 2022	NXP
(3)	i.MX 93 Hardware Developer's Guide	Rev 0, Jun 2022	NXP
(4)	Power management IC for i.MX 93 application processor	Rev 1, Dec 2022	NXP
(5)	i.MX 93 Mask Set Errata	Rev 0, Sep 2022	NXP
(6)	i.MX 93 Power Consumption Measurement	Rev 1, Sep 2023	NXP
(7)	i.MX 93 Product Lifetime Usage	TBD	NXP
(8)	SE050 Trust Secure Element Data Sheet	Rev. 3.1, Dec 2020	NXP
(9)	MBa93xxCA User's Manual	– current –	TQ-Systems
(10)	TQMa93xxCA Support-Wiki	– current –	TQ-Systems
(11)	TQMa93xxCA Processing instructions	– current –	TQ-Systems

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