TQMa8x
User's Manual

TQMa8x UM 0100
25.11.2021

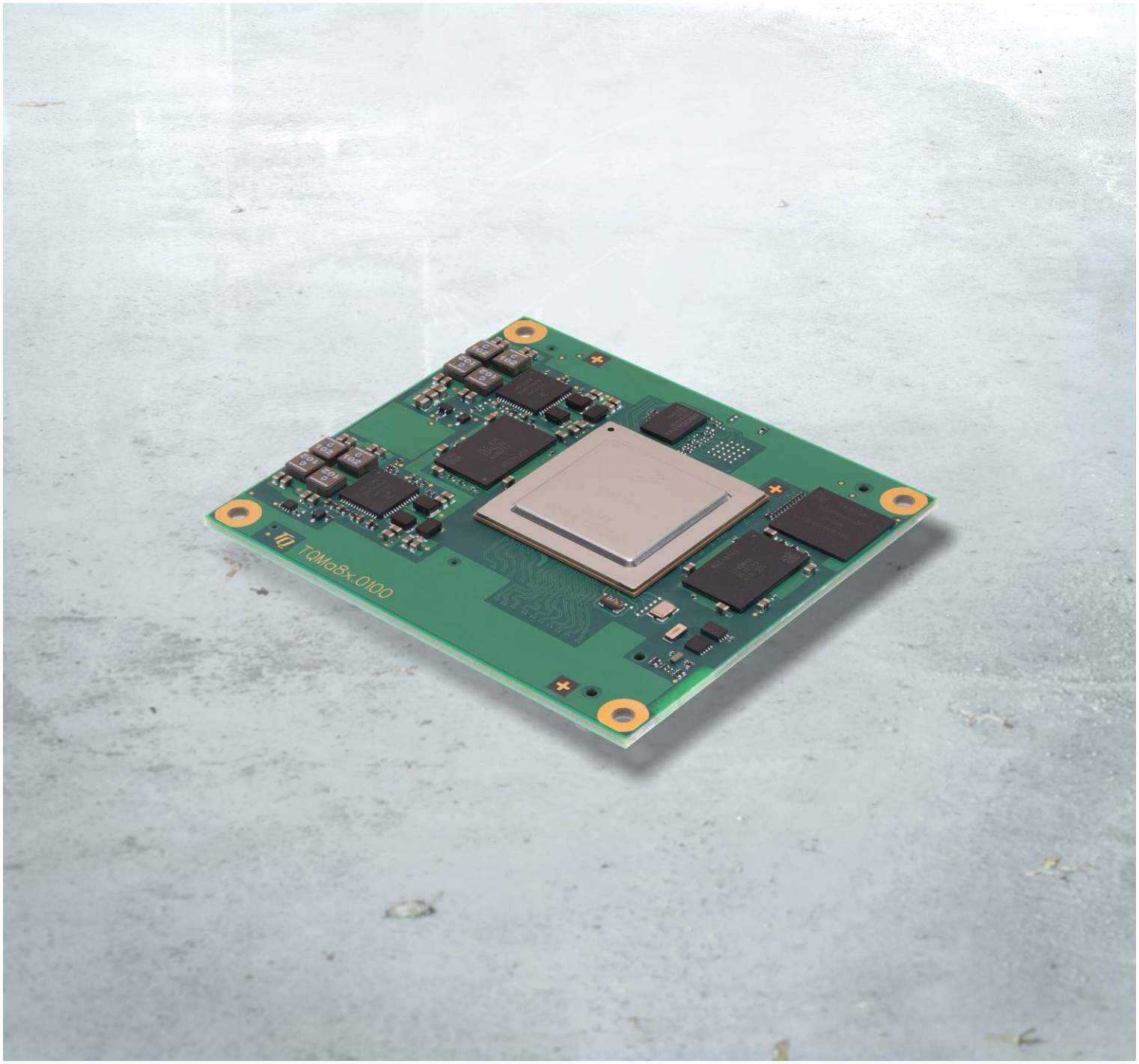

TABLE OF CONTENTS

TABLE DIRECTORY

FIGURE DIRECTORY

REVISION HISTORY

Rev.	Date	Name	Pos.	Modification
0001	07.08.2019	Petz		Initial release
0002	14.08.2019	Petz	Cover image, Figure 23, Figure 24, Figure 25, Table 46	Added
0003	30.10.2020	Petz	All 1.9, 8.2 3.1.1, 3.1.2 3.1.3 Table 11, Table 40 3.2.1.3, 3.2.1.4, 3.2.4.1 3.2.2.1 3.2.5 Table 46 4.6	Assignment of PCF85063, PMIC, V_LICELL, V_VBAT, B37 and B109 corrected Link to PTXdist documentation removed, Link to Yocto documentation added, links updated Swapped Chapters 3.1.3 to 3.1.5 merged Max. current consumption PCF85063 corrected Added Bus width and max SDRAM size corrected Note added Default stack height changed from 8 mm to 5 mm Statements rephrased
0100	25.11.2021	Kreuzer	All 2.1 3.2.3 3.2.4 3.2.6 Figure 2 Figure 5 Table 22	Update for hardware revision 02xx CPU derivatives and memory sizes adjusted Chapter enhanced TSE description added Figure 20, Table 38 and description adapted and extended for selecting the pull-up voltage adapted to RESET_OUT# updated Enhanced Default voltage of VDD_USDHC2_1P8_3P3 corrected to 1.8V

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1.5 Tips on safety

Improper or incorrect handling of the product can substantially reduce its life span.

1.6 Symbols and typographic conventions

Table 1: Terms and conventions

Symbol	Meaning
	This symbol represents the handling of electrostatic-sensitive modules and / or components. These components are often damaged / destroyed by the transmission of a voltage higher than about 50 V. A human body usually only experiences electrostatic discharges above approximately 3,000 V.
	This symbol indicates the possible use of voltages higher than 24 V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and may damage or destroy the component.
	This symbol indicates a possible source of danger. Ignoring the instructions described can cause health damage, or damage the hardware.
	This symbol represents important details or aspects for working with TQ-products.
`Command`	A font with fixed-width is used to denote commands, contents, file names, or menu items.

1.7 Handling and ESD tips

General handling of your TQ-products

	The TQ-product may only be used and serviced by certified personnel who have taken note of the information, the safety regulations in this document and all related rules and regulations. A general rule is not to touch the TQ-product during operation. This is especially important when switching on, changing jumper settings or connecting other devices without ensuring beforehand that the power supply of the system has been switched off. Violation of this guideline may result in damage / destruction of the TQMa8x and be dangerous to your health. Improper handling of your TQ-product would render the guarantee invalid.

Proper ESD handling

	The electronic components of your TQ-product are sensitive to electrostatic discharge (ESD). Always wear antistatic clothing, use ESD-safe tools, packing materials etc., and operate your TQ-product in an ESD-safe environment. Especially when you switch modules on, change jumper settings, or connect other devices.

1.8 Naming of signals

A hash mark (#) at the end of the signal name indicates a low-active signal.
Example: RESET#

If a signal can switch between two functions and if this is noted in the name of the signal, the low-active function is marked with a hash mark and shown at the end.
Example: C / D#

If a signal has multiple functions, the individual functions are separated by slashes when they are important for the wiring.
The identification of the individual functions follows the above conventions.
Example: WE2# / OE#

1.9 Further applicable documents / presumed knowledge

- **Specifications and manual of the modules used:**
  These documents describe the service, functionality and special characteristics of the module used (incl. BIOS).
- **Specifications of the components used:**
  The manufacturer's specifications of the components used, for example CompactFlash cards, are to be taken note of. They contain, if applicable, additional information that must be taken note of for safe and reliable operation.
  These documents are stored at TQ-Systems GmbH.
- **Chip errata:**
  It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of. The manufacturer's advice should be followed.
- **Software behaviour:**
  No warranty can be given, nor responsibility taken for any unexpected software behaviour due to deficient components.
- **General expertise:**
  Expertise in electrical engineering / computer engineering is required for the installation and the use of the device.

The following documents are required to fully comprehend the following contents:

- MBa8x circuit diagram
- MBa8x User's Manual
- i.MX 8 data sheet
- U-Boot documentation: www.denx.de/wiki/U-Boot/Documentation
- Yocto documentation: www.yoctoproject.org/docs/
- TQ-Support Wiki: Support-Wiki TQMa8x

2. BRIEF DESCRIPTION

This Preliminary User's Manual describes the hardware of TQMa8x revision 02xx. The MBa8x serves as an evaluation board for the TQMa8x. A certain TQMa8x version does not necessarily provide all features described in this Preliminary User's Manual.
This Preliminary User's Manual does also not replace the NXP i.MX 8 data sheets (2), (3).
The CPU derivatives provide ARM® Cortex®-A53 and Cortex®-A72 cores, and up to two Dual ARM® Cortex®-M4 coprocessors.
An i.MX 8 Cortex®-A53 core typically operates at 1.2 GHz, a Cortex®-A72 core typically operates at 1.6 GHz.

2.1 i.MX 8 CPU

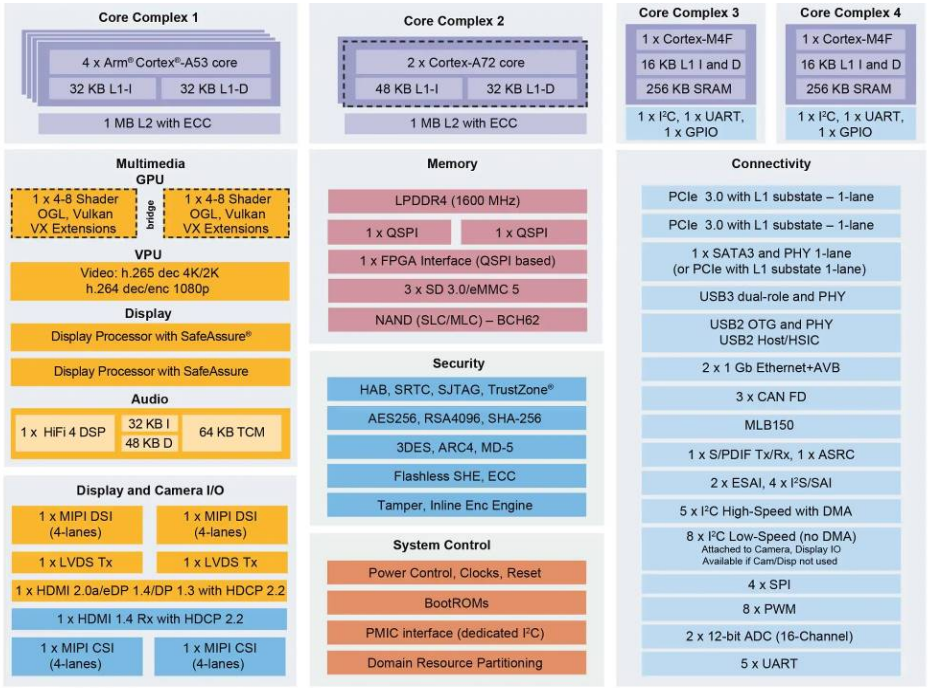

Figure 1: Block diagram i.MX 8 CPU
(Source: NXP)

The TQMa8x extends the TQ-Systems GmbH product range and offers an outstanding computing performance.
A suitable i.MX 8 derivative (i.MX 8 QuadPlus, i.MX 8 QuadMax) can be selected for each requirement.
All essential CPU signals are routed to the connectors. There are therefore no restrictions for customers using the TQMa8x with respect to an integrated customised design. All essential components like CPU, LPDDR4 SDRAM, eMMC, and power management are already integrated on the TQMa8x. The main features of the TQMa8x are:

- 64-bit NXP i.MX 8 CPU with up to 4 × ARM® Cortex®-A53, 2 × ARM® Cortex®-A72, and 2 × ARM® Cortex®-M4
- Derivatives: i.MX 8 QuadMax and i.MX 8 QuadPlus
- Up to 8 Gbyte LPDDR4 SDRAM with 32-bit data bus interface
- Up to 64 Gbyte eMMC NAND flash (optional)
- Up to 512 Mbyte QSPI NOR flash (optional)
- 64 Kbit EEPROM (optional)
- EEPROM + temperature sensor
- 2 x Power-Management-Controller PF8100
- All essential CPU signals are routed to the TQMa8x connectors
- Extended temperature range
- Boot mode selection on TQMa8x
- 5 V single supply voltage

2.2 Integration into the superior system

The TQMa8x operates as an embedded module on a customer-specific carrier board. This carrier board has to provide all interfaces to external systems. The implementation of protective devices as well as normative or regulatory requirements is largely the responsibility of the carrier board. All components required to operate the i.MX 8 are implemented on the TQMa8x.

3. ELECTRONICS

The information provided in this Preliminary User's Manual is only valid in connection with the tailored boot loader, which is preinstalled on the TQMa8x, and the BSP provided by TQ-Systems GmbH, see also chapter 5.

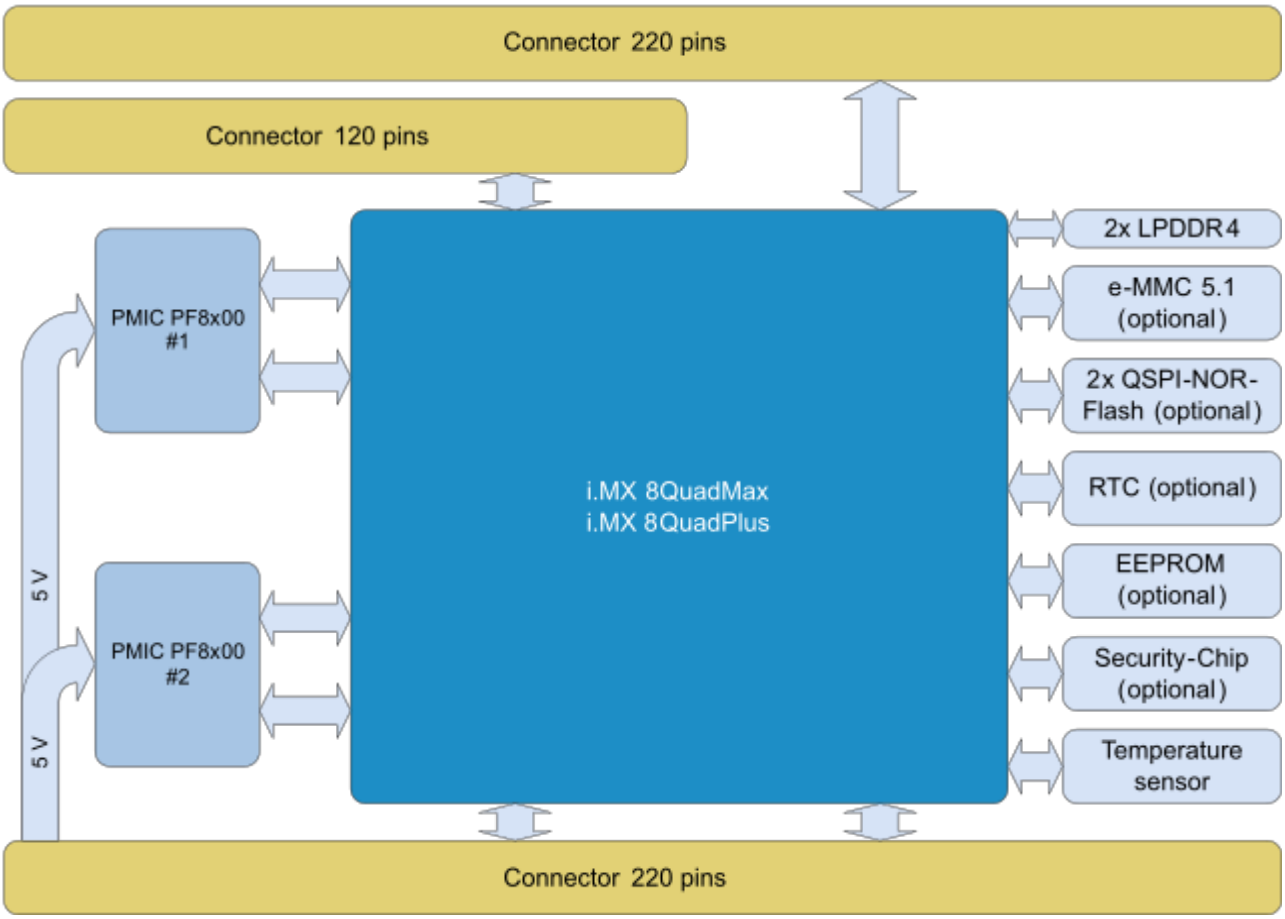

Figure 2: Block diagram TQMa8x

3.1 Interfaces to other systems and devices

3.1.1 Interface impedances

Depending on the signal requirement, the following impedances are used on the TQMa8x.

Table 2: TQMa8x interface impedances

Interface	Impedance TQMa8x	Recommendation for carrier board
HDMI Rx/Tx LVDS MIPI CSI MIPI DSI MLB PCIe Refclk	100 Ω, differential	100 Ω ±10 %, differential
PCIe	85 Ω, differential	85 Ω ±15 %, differential
SATA	85 Ω, differential [1]	Usage as PCIe: differential 85 Ω Usage as SATA: Redriver with 100 Ω
USB HSIC	50 Ω, single ended	50 Ω, single ended
USB OTG1 / OTG2	90 Ω, differential	90 Ω ±15 %, differential [2]
USB SS 3.0	90 Ω, differential	90 Ω ±7 Ω, differential [3]

The layout guidelines of the respective standards are to be taken note of for the carrier board design.

3.1.2 Pin multiplexing

When using the CPU signals, the multiple pin configurations by different CPU-internal function units must be taken note of.
NXP provides a tool showing the multiplexing and simplifies the selection and configuration (NXP Pin Mux Tool):
The TQMa8DM with i.MX 8 DualMax CPU does not provide some signals or they have different functions.
The pin assignment in Table 3 to Table 5 refers to the corresponding BSP provided by TQ-Systems GmbH in combination with the MBa8x.
The electrical and pin characteristics are to be taken from the i.MX 8 data sheets (2), (3) and the PMIC data sheet (4).

Attention: Destruction or malfunction	
	Depending on the configuration, many i.MX 8 balls can provide several different functions. Please take note of the information in the data sheets (2), (3), and the i.MX 8 Errata (1) concerning the configuration of these pins before integration or start-up of your carrier board. Improper programming by operating software can cause malfunctions, deterioration or destruction of the TQMa8x. The meanings given in the following tables must be observed: RFU: Reserved pins without function. To support future TQMa8x versions, these pins must not be connected. DNC: These pins must never be wired and must be left open.

1: Impedance in i.MX 8 is 85 Ω.
2: See Universal Serial Bus Specification, Revision 2.0.
3: See Universal Serial Bus 3.0 Specification, Revision 1.0.

3.1.3 Pinout TQMa8x connectors

Table 3: Pinout connector X1

i.MX 8 ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	i.MX 8 ball
–	–	–	Ground	GND	A1	B1	GND	Ground	–	–	–
–	P	5 V	Power	V_5V_IN	A2	B2	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A3	B3	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A4	B4	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A5	B5	V_5V_IN	Power	5 V	P	–
–	P	5 V	Power	V_5V_IN	A6	B6	V_5V_IN	Power	5 V	P	–
–	–	–	Ground	GND	A7	B7	GND	Ground	–	–	–
–	P	VAR	Power	V_ENET_IN	A8	B8	V_SIM_IN	Power	VAR	P	AK42
–	P	1.8 V	Power	V_1V8_OUT	A9	B9	V_ADC_IN	Power	1.8 V	P	–
–	P	1.8 V	Power	V_1V8_OUT	A10	B10	V_3V3_OUT	Power	3.3 V	P	–
–	–	–	Ground	GND	A11	B11	GND	Ground	–	–	–
BC3	I	1.8 V	MCLK	MCLK_IN	A12	B12	PWM3_OUT	PWM	1.8 V	O	AW53
–	–	–	Ground	GND	A13	B13	PWM2_OUT	PWM	1.8 V	O	BA51
–	OD	VAR	SYSTEM	RESET_OUT#	A14	B14	PMIC_I2C_SCL	I2C	1.8 V	O	AY46
–	I	1.8 V	SYSTEM	RESET_IN#	A15	B15	PMIC_I2C_SDA	I2C	1.8 V	I/O	BG51
J11	O	1.8 V	QSPI	QSPI1A_SS0#	A16	B16	FTM_CH0	FTM	1.8 V	I/O	BF2
G11	O	1.8 V	QSPI	QSPI1A_SS1#	A17	B17	FTM_CH1	FTM	1.8 V	I/O	BE5
H12	I	1.8 V	QSPI	QSPI1A_DQS	A18	B18	FTM_CH2	FTM	1.8 V	I/O	BG5
–	–	–	Ground	GND	A19	B19	GPIO2_IO17	GPIO	1.8 V	I/O	BF6
F10	O	1.8 V	QSPI	QSPI1A_SCLK	A20	B20	GPIO2_IO21	GPIO	1.8 V	I/O	BD8
–	–	–	Ground	GND	A21	B21	GND	Ground	–	–	–
E11	I/O	1.8 V	QSPI	QSPI1A_DATA3	A22	B22	CAN2_RX	CAN	1.8 V	I	C3
E13	I/O	1.8 V	QSPI	QSPI1A_DATA2	A23	B23	CAN2_TX	CAN	1.8 V	O	E7
D14	I/O	1.8 V	QSPI	QSPI1A_DATA1	A24	B24	CAN1_RX	CAN	1.8 V	I	E5
D12	I/O	1.8 V	QSPI	QSPI1A_DATA0	A25	B25	CAN1_TX	CAN	1.8 V	O	G7
–	–	–	Ground	GND	A26	B26	CAN0_RX	CAN	1.8 V	I	C5
D2	O	1.8 V	MLB	MLB_CLK	A27	B27	CAN0_TX	CAN	1.8 V	O	H6
–	–	–	Ground	GND	A28	B28	GND	Ground	–	–	–
E1	O	1.8 V	MLB	MLB_SIG	A29	B29	PCIE0_REFCLK100M_P	PCIE	1.8 V	I/O	F26
E3	O	1.8 V	MLB	MLB_DATA	A30	B30	PCIE0_REFCLK100M_N	PCIE	1.8 V	I/O	E25
–	–	–	Ground	GND	A31	B31	GND	Ground	–	–	–
A9	O	1.8 V	ENET	ENET0_MDC	A32	B32	USB_HSIC_DATA	HSIC	1.8 V	I/O	H26
D10	I/O	1.8 V	ENET	ENET0_MDIO	A33	B33	GND	Ground	–	–	–
–	–	–	Ground	GND	A34	B34	USB_HSIC_STROBE	HSIC	1.8 V	I/O	F28
B10	O	1.8 V	ENET	ENET0_REFCLK_125M_25M	A35	B35	GND	Ground	–	–	–
–	–	–	Ground	GND	A36	B36	PCIE1_RX_P	PCIE	1.8 V	I	A21
A11	O	1.8 V	ENET	ENET1_REFCLK_125M_25M	A37	B37	PCIE1_RX_N	PCIE	1.8 V	I	B22
–	–	–	Ground	GND	A38	B38	GND	Ground	–	–	–
A13	O	VAR	ENET	ENET1_MDC	A39	B39	PCIE1_TX_P	PCIE	1.8 V	O	B24
C13	I/O	VAR	ENET	ENET1_MDIO	A40	B40	PCIE1_TX_N	PCIE	1.8 V	O	C25
–	–	–	Ground	GND	A41	B41	GND	Ground	–	–	–
D20	O	3.3 V	PCIE	PCIE0_PERST#	A42	B42	PCIE1_PERST#	PCIE	3.3 V	O	G25
A15	I	3.3 V	PCIE	PCIE0_WAKE#	A43	B43	PCIE1_WAKE#	PCIE	3.3 V	I	A27
A17	I	3.3 V	PCIE	PCIE0_CLKREQ#	A44	B44	PCIE1_CLKREQ#	PCIE	3.3 V	I	A25
–	P	VAR	Power	V_PMIC2_LDO1	A45	B45	GND	Ground	–	–	–
H22	I	1.8 V	QSPI	QSPI0B_DQS	A46	B46	PCIE0_TX_P	PCIE	1.8 V	O	B26
F16	O	1.8 V	QSPI	QSPI0A_SS1#	A47	B47	PCIE0_TX_N	PCIE	1.8 V	O	C27
H24	O	1.8 V	QSPI	QSPI0B_SS1#	A48	B48	GND	Ground	–	–	–
A5	I/O	1.8 V	GPIO	GPIO4_IO07	A49	B49	PCIE0_RX_P	PCIE	1.8 V	I	A29
J43	I/O	VAR	GPIO	GPIO5_IO23	A50	B50	PCIE0_RX_N	PCIE	1.8 V	I	B30
–	–	–	Ground	GND	A51	B51	GND	Ground	–	–	–
J39	I/O	VAR	SD	USDHC1_CLK	A52	B52	USB_SS_TX_N	USB	1.8 V	O	B32
–	–	–	Ground	GND	A53	B53	USB_SS_TX_P	USB	1.8 V	O	A33
G41	I/O	VAR	SD	USDHC1_CMD	A54	B54	GND	Ground	–	–	–
H42	I/O	VAR	SD	USDHC1_CD#	A55	B55	USB_SS_RX_N	USB	1.8 V	I	B34

3.1.3 Pinout TQMa8x connectors (continued)

Table 3: Pinout connector X1 (continued)

i.MX 8 ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	i.MX 8 ball
E37	I/O	VAR	SD	USDHC1_DATA0	A56	B56	USB_SS_RX_P	USB	1.8 V	I	C35
F38	I/O	VAR	SD	USDHC1_DATA1	A57	B57	GND	Ground	–	–	–
E39	I/O	VAR	SD	USDHC1_DATA2	A58	B58	NC	DNC	–	–	–
F40	I/O	VAR	SD	USDHC1_DATA3	A59	B59	USB_OTG2_OC	OTG	3.3 V	I	H10
–	–	–	Ground	GND	A60	B60	GND	Ground	–	–	–
H40	I/O	VAR	GPIO	GPIO5_IO19	A61	B61	USB_OTG2_PWR	OTG	3.3 V	O	L9
G43	I/O	VAR	GPIO	GPIO5_IO20	A62	B62	USB_OTG2_ID	OTG	3.3 V	I	F30
F42	I/O	VAR	SD	USDHC1_WP	A63	B63	USB_OTG2_VBUS	OTG	3.3 V	P	A35
–	–	–	Ground	GND	A64	B64	GND	Ground	–	–	–
D30	O	1.8 V	MLB	MLB_SIG_P	A65	B65	USB_OTG2_DN	OTG	3.3 V	I/O	C37
E31	O	1.8 V	MLB	MLB_SIG_N	A66	B66	USB_OTG2_DP	OTG	3.3 V	I/O	B38
–	–	–	Ground	GND	A67	B67	GND	Ground	–	–	–
D32	O	1.8 V	MLB	MLB_CLK_P	A68	B68	USB_OTG1_DN	OTG	3.3 V	I/O	C39
E33	O	1.8 V	MLB	MLB_CLK_N	A69	B69	USB_OTG1_DP	OTG	3.3 V	I/O	B40
–	–	–	Ground	GND	A70	B70	GND	Ground	–	–	–
F34	O	1.8 V	MLB	MLB_DATA_P	A71	B71	USB_OTG1_OC	OTG	3.3 V	I	F8
E35	O	1.8 V	MLB	MLB_DATA_N	A72	B72	USB_OTG1_PWR	OTG	3.3 V	O	J9
–	–	–	Ground	GND	A73	B73	USB_OTG1_ID	OTG	1.8 V	I	A37
–	–	–	DNC	NC	A74	B74	USB_OTG1_VBUS	OTG	5 V	P	A39
–	–	–	Ground	GND	A75	B75	GND	Ground	–	–	–
A41	O	1.8 V	ENET	ENET0_TXC	A76	B76	ENET1_TXC	ENET	1.8 V	O	D46
–	–	–	Ground	GND	A77	B77	GND	Ground	–	–	–
E41	O	1.8 V	ENET	ENET0_TX_CTL	A78	B78	ENET1_TX_CTL	ENET	1.8 V	O	B48
A43	O	1.8 V	ENET	ENET0_TXD0	A79	B79	ENET1_TXD0	ENET	1.8 V	O	A49
–	–	–	Ground	GND	A80	B80	GND	Ground	–	–	–
B42	O	1.8 V	ENET	ENET0_TXD1	A81	B81	ENET1_TXD1	ENET	1.8 V	O	C47
A45	O	1.8 V	ENET	ENET0_TXD2	A82	B82	ENET1_TXD2	ENET	1.8 V	O	G47
D42	O	1.8 V	ENET	ENET0_TXD3	A83	B83	ENET1_TXD3	ENET	1.8 V	O	D48
–	–	–	Ground	GND	A84	B84	GND	Ground	–	–	–
B44	I	1.8 V	ENET	ENET0_RXC	A85	B85	ENET1_RXC	ENET	1.8 V	I	B50
–	–	–	Ground	GND	A86	B86	GND	Ground	–	–	–
E43	I	1.8 V	ENET	ENET0_RX_CTL	A87	B87	ENET1_RX_CTL	ENET	1.8 V	I	E49
A47	I	1.8 V	ENET	ENET0_RXD0	A88	B88	ENET1_RXD0	ENET	1.8 V	I	E51
D44	I	1.8 V	ENET	ENET0_RXD1	A89	B89	ENET1_RXD1	ENET	1.8 V	I	C51
–	–	–	Ground	GND	A90	B90	GND	Ground	–	–	–
C45	I	1.8 V	ENET	ENET0_RXD2	A91	B91	ENET1_RXD2	ENET	1.8 V	I	D52
E45	I	1.8 V	ENET	ENET0_RXD3	A92	B92	ENET1_RXD3	ENET	1.8 V	I	E53
–	–	–	Ground	GND	A93	B93	GND	Ground	–	–	–
AL45	O	VAR	SIM	SIM_CLK	A94	B94	M41_GPIO0_00	M4 GPIO	1.8 V	I/O	AP44
AL43	I	VAR	SIM	SIM_PD	A95	B95	M41_GPIO0_01	M4 GPIO	1.8 V	I/O	AU47
AN45	I/O	VAR	SIM	SIM_IO	A96	B96	M41_UART_TX	M4 UART	1.8 V	O	AU49
AP46	I/O	VAR	SIM	GPIO0_IO05	A97	B97	M41_UART_RX	M4 UART	1.8 V	I	AR45
AP48	O	VAR	SIM	SIM_RST	A98	B98	M40_UART_RX	M4 UART	1.8 V	I	AM44
AT48	O	VAR	SIM	SIM_PWR_EN	A99	B99	M40_UART_TX	M4 UART	1.8 V	O	AU51
–	–	–	Ground	GND	A100	B100	GND	Ground	–	–	–
BC51	O	1.8 V	JTAG	JTAG_TCK	A101	B101	UART0_RX	UART	1.8 V	I	AV50
BA49	I	1.8 V	JTAG	JTAG_TMS	A102	B102	UART0_TX	UART	1.8 V	O	AV48
BD52	O	1.8 V	JTAG	JTAG_TDO	A103	B103	UART0_CTS#	UART	1.8 V	I	AV46
BE53	I	1.8 V	JTAG	JTAG_TRST#	A104	B104	UART0_RTS#	UART	1.8 V	O	AU45
BE51	I	1.8 V	JTAG	JTAG_TDI	A105	B105	GND	Ground	–	–	–
–	–	–	Ground	GND	A106	B106	UART1_RX	UART	1.8 V	I	AT44
–	P	VAR	Power	V_PMIC2_LDO3	A107	B107	UART1_TX	UART	1.8 V	O	AY48
–	OD	VAR	SYSTEM	RTC_EVENT#	A108	B108	UART1_CTS#	UART	1.8 V	I	AV46
BE47	I	1.8 V	SYSTEM	IMX_ONOFF	A109	B109	UART1_RTS#	UART	1.8 V	O	AR43
–	–	–	Ground	GND	A110	B110	GND	Ground	–	–	–

3.1.3 Pinout TQMa8x connectors (continued)

Table 4: Pinout connector X2

i.MX 8 ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	i.MX 8 ball
–	–	–	Ground	GND	A1	B1	GND	Ground	–	–	–
BC1	O	1.8 V	SPI	SPI0_CS0	A2	B2	ADC_IN0	ADC	1.8 V	A	AP10
BA3	O	1.8 V	SPI	SPI0_CS1	A3	B3	ADC_IN1	ADC	1.8 V	A	AN11
BA5	I	1.8 V	SPI	SPI0_SDI	A4	B4	ADC_IN2	ADC	1.8 V	A	AP8
AY6	O	1.8 V	SPI	SPI0_SDO	A5	B5	GND	Ground	–	–	–
BB4	O	1.8 V	SPI	SPI0_SCK	A6	B6	IMX_MEMC_ON	SYSTEM	1.8 V	O	BC53
AL9	O	1.8 V	SPI	SPI1_CS0	A7	B7	PMIC_PWR_ON	SYSTEM	1.8 V	I	–
AP6	O	1.8 V	SPI	SPI1_CS1	A8	B8	GND	Ground	–	–	–
AR7	I	1.8 V	SPI	SPI1_SDI	A9	B9	HDMI_TX_AUX_N	HDMI	1.8 V	O	BG3
AN9	O	1.8 V	SPI	SPI1_SDO	A10	B10	HDMI_TX_AUX_P	HDMI	1.8 V	O	BH2
–	–	–	Ground	GND	A11	B11	GND	Ground	–	–	–
AR9	O	1.8 V	SPI	SPI1_SCK	A12	B12	GND	Ground	–	–	–
AW1	O	1.8 V	SPI	SPI2_CS0	A13	B13	HDMI_TX_CLK_N	HDMI	1.8 V	O	BK2
AY2	O	1.8 V	SPI	SPI2_CS1	A14	B14	HDMI_TX_CLK_P	HDMI	1.8 V	O	BL3
AY4	I	1.8 V	SPI	SPI2_SDI	A15	B15	GND	Ground	–	–	–
BA1	O	1.8 V	SPI	SPI2_SDO	A16	B16	HDMI_TX_DATA0_N	HDMI	1.8 V	O	BM4
AW5	O	1.8 V	SPI	SPI2_SCK	A17	B17	HDMI_TX_DATA0_P	HDMI	1.8 V	O	BL5
AU1	O	1.8 V	SAI	SAI1_TXD	A18	B18	GND	Ground	–	–	–
AV2	O	1.8 V	SAI	SAI1_TXFS	A19	B19	HDMI_TX_DATA1_N	HDMI	1.8 V	O	BM6
AU5	O	1.8 V	SAI	SAI1_TXC	A20	B20	HDMI_TX_DATA1_P	HDMI	1.8 V	O	BL7
–	–	–	Ground	GND	A21	B21	GND	Ground	–	–	–
AU3	I	1.8 V	SAI	SAI1_RXFS	A22	B22	HDMI_TX_DATA2_N	HDMI	1.8 V	O	BM8
AV6	I	1.8 V	SAI	SAI1_RXC	A23	B23	HDMI_TX_DATA2_P	HDMI	1.8 V	O	BL9
AV4	I	1.8 V	SAI	SAI1_RXD	A24	B24	GND	Ground	–	–	–
BN35	I/O	1.8 V	GPIO	GPIO1_IO15	A25	B25	HDMI_TX_DDC_SCL	HDMI	1.8 V	O	BG1
–	–	–	Ground	GND	A26	B26	HDMI_TX_DDC_SDA	HDMI	1.8 V	I/O	BN5
AT10	I/O	1.8 V	ESAI	ESAI1_TX5_RX0	A27	B27	HDMI_TX_CEC	HDMI	1.8 V	O	BJ1
AY12	I/O	1.8 V	ESAI	ESAI1_TX4_RX1	A28	B28	HDMI_TX_HPD	HDMI	1.8 V	O	BH8
AV10	I/O	1.8 V	ESAI	ESAI1_TX3_RX2	A29	B29	GPIO2_IO02	GPIO	3.3 V	I/O	BN9
AU11	I/O	1.8 V	ESAI	ESAI1_TX2_RX3	A30	B30	GPIO2_IO03	GPIO	3.3 V	I/O	BN7
–	–	–	Ground	GND	A31	B31	GND	Ground	–	–	–
BA11	O	1.8 V	ESAI	ESAI1_TX1	A32	B32	MCLK_OUT	MCLK	1.8 V	O	BD4
BF10	O	1.8 V	ESAI	ESAI1_TX0	A33	B33	GND	Ground	–	–	–
BD12	O	1.8 V	ESAI	ESAI1_SCKR	A34	B34	GPIO1_IO14	GPIO	1.8 V	I/O	BD32
BE11	O	1.8 V	ESAI	ESAI1_FSR	A35	B35	PMIC2_FSOB	SYSTEM	1.8 V	O	–
AY10	O	1.8 V	ESAI	ESAI1_SCKT	A36	B36	PMIC2_PGOOD	SYSTEM	1.8 V	OD	–
BF12	O	1.8 V	ESAI	ESAI1_FST	A37	B37	V_LICELL	Power	3.3 V	P	–
–	–	–	Ground	GND	A38	B38	GND	Ground	–	–	–
AR47	I/O	1.8 V	M4 GPIO	M40_GPIO0_00	A39	B39	MIPI_CSI0_SDA	CSI	1.8 V	I/O	BN19
AU53	I/O	1.8 V	M4 GPIO	M40_GPIO0_01	A40	B40	MIPI_CSI0_SCL	CSI	1.8 V	O	BH24
–	–	–	Ground	GND	A41	B41	GND	Ground	–	–	–
–	P	1.8 V	Power	V_1V8_ANA	A42	B42	NC	DNC	–	–	–
–	–	–	Ground	GND	A43	B43	GND	Ground	–	–	–
BN15	I/O	1.8 V	CSI	MIPI_CSI1_RST#	A44	B44	MIPI_CSI0_MCLK_OUT	CSI	1.8 V	O	BJ23
BN13	O	1.8 V	CSI	MIPI_CSI1_EN	A45	B45	GND	Ground	–	–	–
BM22	O	1.8 V	CSI	MIPI_CSI0_EN	A46	B46	MIPI_CSI0_DATA3_N	CSI	1.8 V	I	BE17
BL23	I/O	1.8 V	CSI	MIPI_CSI0_RST#	A47	B47	MIPI_CSI0_DATA3_P	CSI	1.8 V	I	BF16
–	OD	VAR	SYSTEM	TEMP_EVENT#	A48	B48	GND	Ground	–	–	–
–	–	–	Ground	GND	A49	B49	MIPI_CSI0_DATA2_N	CSI	1.8 V	I	BE25
BN23	O	1.8 V	CSI	MIPI_CSI1_MCLK_OUT	A50	B50	MIPI_CSI0_DATA2_P	CSI	1.8 V	I	BF24
–	–	–	Ground	GND	A51	B51	GND	Ground	–	–	–
–	O	1.8 V	SYSTEM	PMIC1_FSOB	A52	B52	MIPI_CSI0_CLK_N	CSI	1.8 V	I	BE21
–	OD	1.8 V	SYSTEM	PMIC1_PGOOD	A53	B53	MIPI_CSI0_CLK_P	CSI	1.8 V	I	BF20
–	–	–	Ground	GND	A54	B54	GND	Ground	–	–	–
BH12	I	1.8 V	CSI	MIPI_CSI1_DATA3_N	A55	B55	MIPI_CSI0_DATA1_N	CSI	1.8 V	I	BE19

3.1.3 Pinout TQMa8x connectors (continued)

Table 4: Pinout connector X2 (continued)

i.MX 8 ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	i.MX 8 ball
BJ13	I	1.8 V	CSI	MIPI_CSI1_DATA3_P	A56	B56	MIPI_CSI0_DATA1_P	CSI	1.8 V	I	BF18
–	–	–	Ground	GND	A57	B57	GND	Ground	–	–	–
BH20	I	1.8 V	CSI	MIPI_CSI1_DATA2_N	A58	B58	MIPI_CSI0_DATA0_N	CSI	1.8 V	I	BE23
BJ21	I	1.8 V	CSI	MIPI_CSI1_DATA2_P	A59	B59	MIPI_CSI0_DATA0_P	CSI	1.8 V	I	BF22
–	–	–	Ground	GND	A60	B60	GND	Ground	–	–	–
BH16	I	1.8 V	CSI	MIPI_CSI1_CLK_N	A61	B61	I2C2_SCL	I2C	1.8 V	O	BA53
BJ17	I	1.8 V	CSI	MIPI_CSI1_CLK_P	A62	B62	I2C2_SDA	I2C	1.8 V	I/O	AY50
–	–	–	Ground	GND	A63	B63	MIPI_DSI0_GPIO0_01	DSI	1.8 V	I/O	BD28
BH14	I	1.8 V	CSI	MIPI_CSI1_DATA1_N	A64	B64	MIPI_DSI0_PWM	DSI	1.8 V	O	BD30
BJ15	I	1.8 V	CSI	MIPI_CSI1_DATA1_P	A65	B65	MIPI_DSI0_SCL	DSI	1.8 V	O	BE29
–	–	–	Ground	GND	A66	B66	MIPI_DSI0_SDA	DSI	1.8 V	I/O	BE31
BH18	I	1.8 V	CSI	MIPI_CSI1_DATA0_N	A67	B67	GND	Ground	–	–	–
BJ19	I	1.8 V	CSI	MIPI_CSI1_DATA0_P	A68	B68	MIPI_DSI0_DATA3_N	DSI	1.8 V	O	BN25
–	–	–	Ground	GND	A69	B69	MIPI_DSI0_DATA3_P	DSI	1.8 V	O	BL25
–	–	–	Ground	GND	A70	B70	GND	Ground	–	–	–
BE15	I/O	1.8 V	CSI	MIPI_CSI1_SDA	A71	B71	GND	Ground	–	–	–
BN17	O	1.8 V	CSI	MIPI_CSI1_SCL	A72	B72	MIPI_DSI0_DATA2_N	DSI	1.8 V	O	BN29
BE39	O	1.8 V	LVDS	LVDS0_PWM	A73	B73	MIPI_DSI0_DATA2_P	DSI	1.8 V	O	BL29
BD40	I/O	1.8 V	LVDS	LVDS0_GPIO01	A74	B74	GND	Ground	–	–	–
BD36	I/O	1.8 V	LVDS	LVDS0_I2C0_SDA	A75	B75	MIPI_DSI0_CLK_N	DSI	1.8 V	O	BN27
BD38	O	1.8 V	LVDS	LVDS0_I2C0_SCL	A76	B76	MIPI_DSI0_CLK_P	DSI	1.8 V	O	BL27
–	–	–	Ground	GND	A77	B77	GND	Ground	–	–	–
BG37	O	1.8 V	LVDS	LVDS0_CH1_TX3_N	A78	B78	MIPI_DSI0_DATA1_N	DSI	1.8 V	O	BM26
BH38	O	1.8 V	LVDS	LVDS0_CH1_TX3_P	A79	B79	MIPI_DSI0_DATA1_P	DSI	1.8 V	O	BK26
–	–	–	Ground	GND	A80	B80	GND	Ground	–	–	–
–	–	–	Ground	GND	A81	B81	GND	Ground	–	–	–
BG39	O	1.8 V	LVDS	LVDS0_CH1_TX2_N	A82	B82	MIPI_DSI0_DATA0_N	DSI	1.8 V	O	BM28
BH40	O	1.8 V	LVDS	LVDS0_CH1_TX2_P	A83	B83	MIPI_DSI0_DATA0_P	DSI	1.8 V	O	BK28
–	–	–	Ground	GND	A84	B84	GND	Ground	–	–	–
BG41	O	1.8 V	LVDS	LVDS0_CH1_TX1_N	A85	B85	SCU_UART_RX	SCU	1.8 V	I	AU43
BH42	O	1.8 V	LVDS	LVDS0_CH1_TX1_P	A86	B86	SCU_UART_TX	SCU	1.8 V	O	AV44
–	–	–	Ground	GND	A87	B87	SCU_GPIO0_02	SCU	1.8 V	I/O	AW45
BG43	O	1.8 V	LVDS	LVDS0_CH1_TX0_N	A88	B88	SCU_GPIO0_03	SCU	1.8 V	I/O	BB46
BH44	O	1.8 V	LVDS	LVDS0_CH1_TX0_P	A89	B89	SCU_GPIO0_04	SCU	1.8 V	I/O	BC47
–	–	–	Ground	GND	A90	B90	GND	Ground	–	–	–
BG45	O	1.8 V	LVDS	LVDS0_CH1_CLK_N	A91	B91	SCU_GPIO0_05	SCU	1.8 V	I/O	AY44
BH46	O	1.8 V	LVDS	LVDS0_CH1_CLK_P	A92	B92	SCU_GPIO0_06	SCU	1.8 V	I/O	BG49
–	–	–	Ground	GND	A93	B93	SCU_GPIO0_07	SCU	1.8 V	I/O	BF48
BL41	O	1.8 V	LVDS	LVDS0_CH0_CLK_N	A94	B94	BOOT_MODE0	BOOT	1.8 V	I	BB44
BN41	O	1.8 V	LVDS	LVDS0_CH0_CLK_P	A95	B95	BOOT_MODE1	BOOT	1.8 V	I	BC45
–	–	–	Ground	GND	A96	B96	BOOT_MODE2	BOOT	1.8 V	I	BJ53
BK42	O	1.8 V	LVDS	LVDS0_CH0_TX0_N	A97	B97	BOOT_MODE3	BOOT	1.8 V	I	BA43
BM42	O	1.8 V	LVDS	LVDS0_CH0_TX0_P	A98	B98	BOOT_MODE4	BOOT	1.8 V	I	AY42
–	–	–	Ground	GND	A99	B99	BOOT_MODE5	BOOT	1.8 V	I	BK52
–	–	–	Ground	GND	A100	B100	GND	Ground	–	–	–
BL43	O	1.8 V	LVDS	LVDS0_CH0_TX1_N	A101	B101	I2C1_SDA	I2C	1.8 V	I/O	AV52
BN43	O	1.8 V	LVDS	LVDS0_CH0_TX1_P	A102	B102	I2C1_SCL	I2C	1.8 V	O	AY52
–	–	–	Ground	GND	A103	B103	TAMPER_IN0	SNVS	1.8 V	I	BE41
BK44	O	1.8 V	LVDS	LVDS0_CH0_TX2_N	A104	B104	TAMPER_IN1	SNVS	1.8 V	I	BE43
BM44	O	1.8 V	LVDS	LVDS0_CH0_TX2_P	A105	B105	TAMPER_OUT0	SNVS	1.8 V	O	BD46
–	–	–	Ground	GND	A106	B106	TAMPER_OUT1	SNVS	1.8 V	O	BD42
BL45	O	1.8 V	LVDS	LVDS0_CH0_TX3_N	A107	B107	UART2_TX	UART	1.8 V	O	BE37
BN45	O	1.8 V	LVDS	LVDS0_CH0_TX3_P	A108	B108	UART2_RX	UART	1.8 V	I	BE35
–	–	–	Ground	GND	A109	B109	V_VBAT	Power	3.3 V	P	–
–	–	–	Ground	GND	A110	B110	GND	Ground	–	–	–

3.1.3 Pinout TQMa8x connectors (continued)

Table 5: Pinout connector X3

i.MX 8 ball	I/O	Level	Group	Signal	Pin		Signal	Group	Level	I/O	i.MX 8 ball
–	–	–	Ground	GND	A1	B1	GND	Ground	–	–	–
C17	O	1.8 V	SATA	SATA_TX_N	A2	B2	SATA_RX_N	SATA	1.8 V	I	B20
B16	O	1.8 V	SATA	SATA_TX_P	A3	B3	SATA_RX_P	SATA	1.8 V	I	A19
–	–	–	Ground	GND	A4	B4	GND	Ground	–	–	–
BD6	O	1.8 V	S/PDIF	SPDIF_EXT_CLK	A5	B5	GPIO4_IO10	SD / GPIO	1.8 V	I/O	A7
–	–	–	Ground	GND	A6	B6	GND	Ground	–	–	–
BC7	I	1.8 V	S/PDIF	SPDIF_RX	A7	B7	HDMI_RX_CLK_N	HDMI	1.8 V	I	BL11
BC9	O	1.8 V	S/PDIF	SPDIF_TX	A8	B8	HDMI_RX_CLK_P	HDMI	1.8 V	I	BM12
BH10	O	1.8 V	HDMI	HDMI_RX_DDC_SCL	A9	B9	GND	Ground	–	–	–
BE13	I/O	1.8 V	HDMI	HDMI_RX_DDC_SDA	A10	B10	HDMI_RX_ARC_N	HDMI	1.8 V	I	BL13
BN11	I	1.8 V	HDMI	HDMI_RX_MON_5V	A11	B11	HDMI_RX_ARC_P	HDMI	1.8 V	I	BM14
BE33	I/O	1.8 V	LVDS	LVDS1_I2C0_SDA	A12	B12	GND	Ground	–	–	–
BL35	O	1.8 V	LVDS	LVDS1_I2C0_SCL	A13	B13	HDMI_RX_DATA0_N	HDMI	1.8 V	I	BL15
BH36	I/O	1.8 V	LVDS	LVDS1_GPIO01	A14	B14	HDMI_RX_DATA0_P	HDMI	1.8 V	I	BM16
BD34	O	1.8 V	LVDS	LVDS1_PWM	A15	B15	GND	Ground	–	–	–
–	–	–	Ground	GND	A16	B16	GND	Ground	–	–	–
BK30	O	1.8 V	LVDS	LVDS1_CH1_TX3_N	A17	B17	HDMI_RX_DATA1_N	HDMI	1.8 V	I	BL17
BM30	O	1.8 V	LVDS	LVDS1_CH1_TX3_P	A18	B18	HDMI_RX_DATA1_P	HDMI	1.8 V	I	BM18
–	–	–	Ground	GND	A19	B19	GND	Ground	–	–	–
BL31	O	1.8 V	LVDS	LVDS1_CH1_TX2_N	A20	B20	HDMI_RX_DATA2_N	HDMI	1.8 V	I	BL19
BN31	O	1.8 V	LVDS	LVDS1_CH1_TX2_P	A21	B21	HDMI_RX_DATA2_P	HDMI	1.8 V	I	BM20
–	–	–	Ground	GND	A22	B22	GND	Ground	–	–	–
BK32	O	1.8 V	LVDS	LVDS1_CH1_TX1_N	A23	B23	HDMI_RX_CEC	HDMI	1.8 V	I	BJ9
BM32	O	1.8 V	LVDS	LVDS1_CH1_TX1_P	A24	B24	HDMI_RX_HPD	HDMI	1.8 V	I	BF14
–	–	–	Ground	GND	A25	B25	GND	Ground	–	–	–
–	–	–	Ground	GND	A26	B26	GND	Ground	–	–	–
BL33	O	1.8 V	LVDS	LVDS1_CH1_TX0_N	A27	B27	ESAI0_TX5_RX0	ESAI	1.8 V	I/O	AU7
BN33	O	1.8 V	LVDS	LVDS1_CH1_TX0_P	A28	B28	ESAI0_TX4_RX1	ESAI	1.8 V	I/O	AV8
–	–	–	Ground	GND	A29	B29	ESAI0_TX3_RX2	ESAI	1.8 V	I/O	BC5
BK34	O	1.8 V	LVDS	LVDS1_CH1_CLK_N	A30	B30	ESAI0_TX2_RX3	ESAI	1.8 V	I/O	AU9
BM34	O	1.8 V	LVDS	LVDS1_CH1_CLK_P	A31	B31	GND	Ground	–	–	–
–	–	–	Ground	GND	A32	B32	ESAI0_TX1	ESAI	1.8 V	O	BA7
BK36	O	1.8 V	LVDS	LVDS1_CH0_CLK_N	A33	B33	ESAI0_TX0	ESAI	1.8 V	O	BA9
BM36	O	1.8 V	LVDS	LVDS1_CH0_CLK_P	A34	B34	ESAI0_SCKR	ESAI	1.8 V	O	BB8
–	–	–	Ground	GND	A35	B35	GND	Ground	–	–	–
BL37	O	1.8 V	LVDS	LVDS1_CH0_TX0_N	A36	B36	ESAI0_FSR	ESAI	1.8 V	O	AW9
BN37	O	1.8 V	LVDS	LVDS1_CH0_TX0_P	A37	B37	ESAI0_SCKT	ESAI	1.8 V	O	AY8
–	–	–	Ground	GND	A38	B38	ESAI0_FST	ESAI	1.8 V	O	BG9
BK38	O	1.8 V	LVDS	LVDS1_CH0_TX1_N	A39	B39	NC	DNC	–	–	–
BM38	O	1.8 V	LVDS	LVDS1_CH0_TX1_P	A40	B40	GND	Ground	–	–	–
–	–	–	Ground	GND	A41	B41	MIPI_DSI1_SCL	DSI	1.8 V	O	BE27
BL39	O	1.8 V	LVDS	LVDS1_CH0_TX2_N	A42	B42	MIPI_DSI1_SDA	DSI	1.8 V	I/O	BG25
BN39	O	1.8 V	LVDS	LVDS1_CH0_TX2_P	A43	B43	MIPI_DSI1_PWM	DSI	1.8 V	O	BM24
–	–	–	Ground	GND	A44	B44	MIPI_DSI1_GPIO0_01	DSI	1.8 V	I/O	BK24
–	–	–	Ground	GND	A45	B45	GND	Ground	–	–	–
BK40	O	1.8 V	LVDS	LVDS1_CH0_TX3_N	A46	B46	MIPI_DSI1_DATA3_N	DSI	1.8 V	O	BH26
BM40	O	1.8 V	LVDS	LVDS1_CH0_TX3_P	A47	B47	MIPI_DSI1_DATA3_P	DSI	1.8 V	O	BG27
–	–	–	Ground	GND	A48	B48	GND	Ground	–	–	–
F46	I/O	VAR	SD / GPIO	GPIO5_IO24	A49	B49	MIPI_DSI1_DATA2_N	DSI	1.8 V	O	BH34
–	–	–	Ground	GND	A50	B50	MIPI_DSI1_DATA2_P	DSI	1.8 V	O	BG35
B8	I/O	1.8 V	SD / GPIO	GPIO4_IO12	A51	B51	GND	Ground	–	–	–
C7	I/O	1.8 V	SD / GPIO	GPIO4_IO09	A52	B52	MIPI_DSI1_CLK_N	DSI	1.8 V	O	BH30
D8	I/O	1.8 V	SD / GPIO	GPIO4_IO11	A53	B53	MIPI_DSI1_CLK_P	DSI	1.8 V	O	BG31
H44	I/O	VAR	SD / GPIO	GPIO5_IO25	A54	B54	GND	Ground	–	–	–
–	–	–	Ground	GND	A55	B55	GND	Ground	–	–	–
H48	I/O	VAR	SD / GPIO	GPIO5_IO26	A56	B56	MIPI_DSI1_DATA1_N	DSI	1.8 V	O	BH28
G45	I/O	VAR	SD / GPIO	GPIO5_IO27	A57	B57	MIPI_DSI1_DATA1_P	DSI	1.8 V	O	BG29
L45	I/O	VAR	SD / GPIO	GPIO5_IO28	A58	B58	GND	Ground	–	–	–
J45	I/O	VAR	SD / GPIO	GPIO5_IO29	A59	B59	MIPI_DSI1_DATA0_N	DSI	1.8 V	O	BH32
–	–	–	Ground	GND	A60	B60	MIPI_DSI1_DATA0_P	DSI	1.8 V	O	BG33

3.2 System components

3.2.1 i.MX 8 CPU

3.2.1.1 i.MX 8 derivatives

Depending on the TQMa8x version, one of the following i.MX 8 derivatives is assembled.

Table 6: i.MX 8 derivatives

TQMa8x variant	CPU derivative	Cortex®-A53 clock	Cortex®-A72 clock	Cortex®-M4 clock	T_J, temperature range
TQMa8QM-xx	i.MX 8QuadMax	1.2 GHz (4×)	1.6 GHz (2×)	264 MHz (2×)	–40 °C … +105 °C
TQMa8QP-xx	i.MX 8QuadPlus	1.2 GHz (4×)	1.6 GHz (1×)	264 MHz (2×)	–40 °C … +105 °C
TQMa8DM-xx	i.MX 8DualMax	–	1.6 GHz (TBD)	264 MHz (TBD)	–40 °C … +105 °C

3.2.1.2 i.MX 8 errata

Attention: Malfunction or destruction	
	Please take note of the current i.MX 8 errata (1).

3.2.1.3 Boot modes

After release of PMIC_POR#, the System Controller (SCU) starts from the internal ROM. Depending on the OTP fuses (eFuse) and the boot mode settings of the system controller, the TQMa8x boots from the specified boot source:

- eMMC
- QSPI NOR flash
- SD card

More information about boot interfaces and its configuration is to be taken from the i.MX 8 data sheets (2), (3).

Alternatively, an image can be loaded into the internal RAM via serial downloader.

The i.MX 8's six BOOT_MODE signals, which are required for boot device configurations, are all available on the module header X2. In the following chapters, the configurations for the following possible boot devices are described exemplarily:

Table 7: Boot Mode / BT_FUSE_SEL

BOOT_MODE[5] 5 4 3 2 1 0	Boot source
0 0 0 0 0 0	Internal Fuse
0 0 0 1 0 0	USB Serial Downloader
0 0 1 0 0 0	eMMC
0 0 1 1 0 0	SD card (USDHC1)
0 1 1 0 0 0	Flash / 3-Byte Read
0 1 1 0 1 0	Hyperflash 1.8 V
0 1 1 1 1 0	Flash / 4-Byte Read

Note: Field software updates	
	When designing a carrier board, it is recommended to have a redundant update concept for field software updates.

3.2.2 Memory

3.2.2.1 LPDDR4 SDRAM

Two 32-bit LPDDR4 memory chips are assembled on the TQMa8x, each connected to a dedicated controller in the i.MX 8. Due to the selected memory architecture, the topology consists of direct connections of the signals between controller and SDRAM.

There are no differences in the memory interface between the i.MX 8 variants QuadMax and QuadPlus.

The IO voltage of the LPDDR4 is 1.1 V. The timing of the resulting 64-bit bus meets JEDEC standard LPDDR4-3200, with a maximum clock rate of 1600 MHz. The maximum SDRAM size is currently 8 Gbyte.

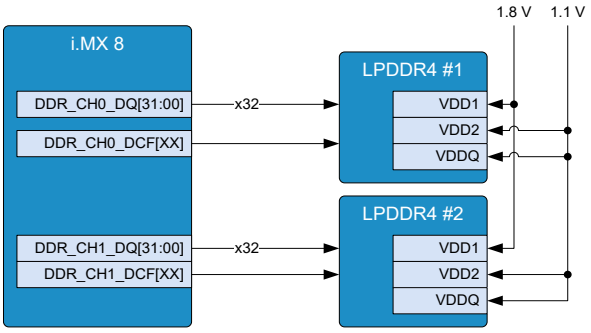

Figure 3: Block diagram LPDDR4

Attention: Malfunction	
	The TQMa8x uses a specially developed RAM timing. Each memory expansion stage required its own LPDDR4 configuration.

3.2.2.2 eMMC NAND flash

An eMMC is available on the TQMa8x as non-volatile memory for programs and data (e.g. bootloader, operating system, or application). The i.MX 8 supports MMC card data rates up to the current eMMC standard v5.1, or SD card standard 3.0. In DDR mode (HS400) a data rate of up to 400 Mbyte/s can be achieved.

The eMMC can be used as boot medium. The boot configuration is described in 3.2.1.5.

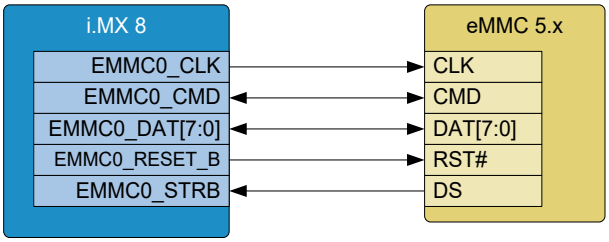

Figure 4: Block diagram eMMC

Additional series resistors are inserted in the data and clock signals in order to be able to influence the driver strength starting from the e-MMC.

3.2.2.3 QSPI NOR flash

The i.MX 8 provides three QSPI interfaces. The interface QSPI1A with four data lines and two chip selects is completely available at the module header X1. The unused signals QSPI0B_DQS, QSPI0B_SS1 and QSPI0A_SS1 are also connected to module header X1.

The first SPI-NOR flash is connected with QSPI0A and QSPI0B including the QSPI0A_DQS clock signal as well as two chip select

signals and thus allows the use of QSPI-NOR, octal, twin-quad as well as Hyperflash or Xccela flash devices.

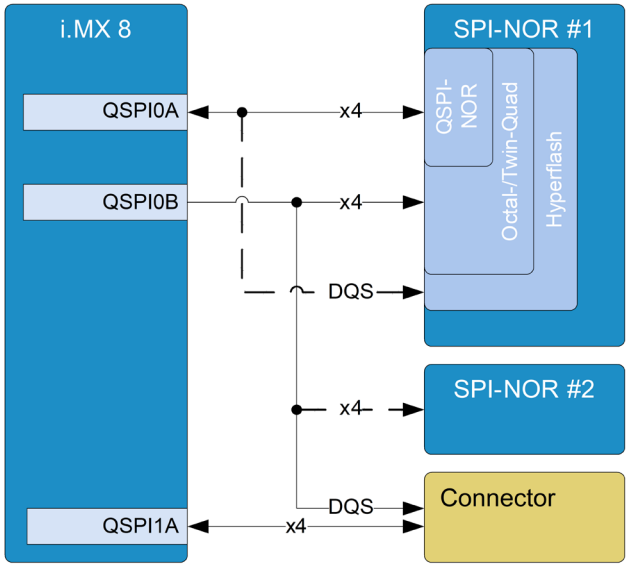

Figure 5: Block diagram QSPI

As the memory size is limited with octal or twin-quad devices, the second SPI-NOR flash can be used to realize a higher memory capacity. If two SPI-NOR Flashes are to be equipped, only two QSPI types can be used in each case due to the connection:

- QSPI Flash - Simple NOR-Flashes only use the QSPI0A interface. The signal lines of the second interface (QSPI0B), which are only routed internally in the module, are not connected in this case and can therefore not be used.
- Octal-SPI / Twin-Quad-SPI - These NOR-Flashes represent a Dual-Die-Flash which uses additional pins for the second QSPI interface (QSPI0B) compared to the simple NOR-Flash.
- Hyperflash / Xccela Flash - The most modern serial Flash devices are connected similar to an Octal-SPI / Twin-Quad-SPI, but have a DQS signal (RX clock) to increase the transfer rate. Thus up to 400 MB/s can be achieved.

3.2.2.4 EEPROM

A serial EEPROM, controlled by the I2C1 bus, is assembled. Write-Protect (WP#) is not supported.
To store data “read-only”, the EEPROM with temperature sensor must be used, see chapter 3.2.2.5.

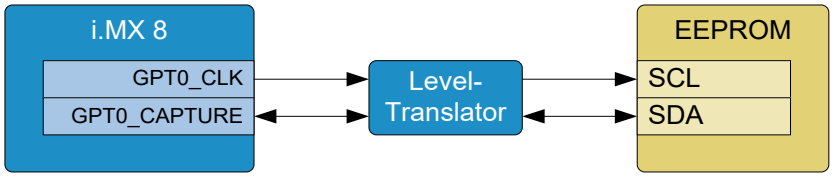

Figure 6: Block diagram EEPROM

The following table shows details of the EEPROM:

Table 8: EEPROM

Manufacturer	Part number	Size	Temperature range
Microchip	24LC64T-I/MC MCH	64 Kbit	–45 °C … +85 °C

➢ The EEPROM has the I²C address `0x57 / 101 0111b`

3.2.2.5 EEPROM with temperature sensor

A serial EEPROM including temperature sensor, controlled by the I2C1 bus, is assembled on the TQMa8x.
The lower 128 bytes (addresses 00h to 7Fh) can be set to Permanent Write Protected (PWP) mode or Reversible Write Protected (RWP) mode by software. The upper 128 bytes (addresses 80h to FFh) cannot be write-protected and can be used for general data storage. The EEPROM also provides a temperature sensor to monitor the temperature of the TQMa8x.
The following table shows details of the Manufacturer EEPROM.

Table 9: Manufacturer EEPROM with temperature sensor

Manufacturer	Part number	Size	Temperature range
NXP	SE97BTP,547	2 × 128 bytes	–40 °C … +85 °C

- The device has the following I²C addresses:
  - EEPROM (normal): `0x53 / 101 0011b`
  - EEPROM (Protection mode): `0x33 / 011 0011b`
  - Temperature sensor: `0x1B / 001 1011b`

The following figure shows the interface of the temperature sensor to the i.MX 8.

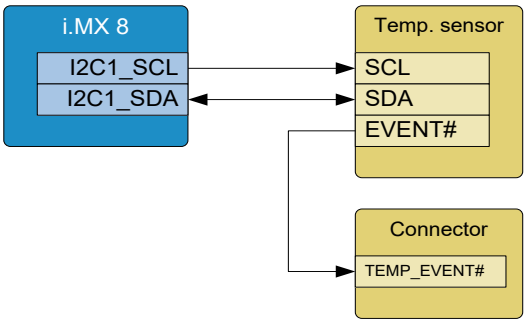

Figure 7: Block diagram temperature sensor

The EEPROM with temperature sensor (D7) is assembled on the bottom side of the TQMa8x, see Figure 28.
The overtemperature output of the sensor is connected as open drain to connector X2-A48 (TEMP_EVENT#).
A pull-up to a maximum voltage of 3.6 V must be provided on the carrier board.
The following table shows details of the temperature sensor.

Table 10: Temperature sensor

Manufacturer	Part number	Resolution	Accuracy	Temperature range
NXP	SE97BTP	11 bits	Max. ±3 °C	–40 °C … +125 °C

3.2.3 RTC & SNVS

In addition to the i.MX 8-internal RTC, the TQMa8x provides a discrete RTC PCF85063 as an assembly option.
The accuracy of the RTC is essentially determined by the characteristics of the quartz used.
The quartz used on the TQMa8x has a standard frequency tolerance of ±20 ppm at +25 °C.
The RTC is connected to the I2C1 bus.

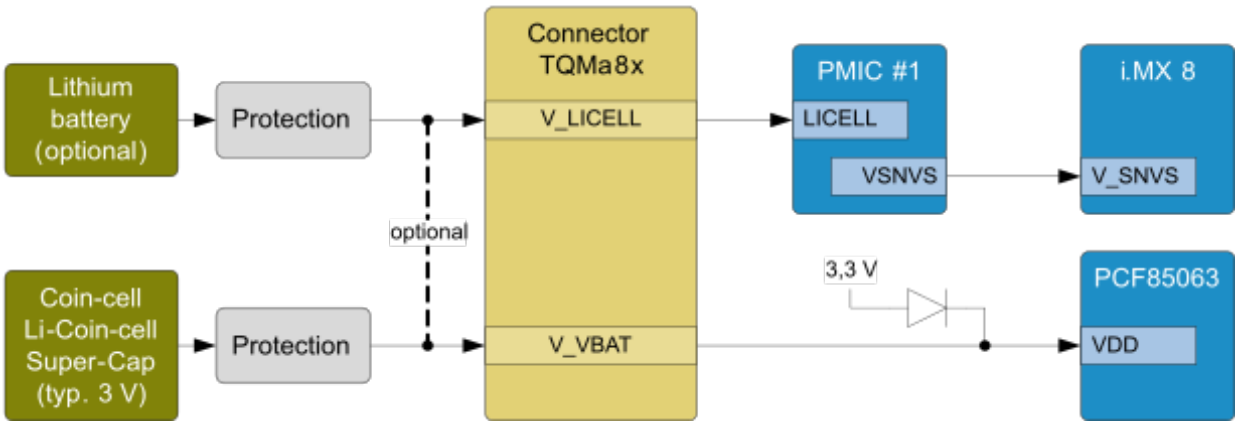

Figure 8: Block diagram RTC

Both RTCs are supplied via dedicated pins at the TQMa8x connectors. This permits different functions and an adapted backup concept (battery design) depending on the application:

- V_VBAT supplies the PCF85063 for applications with Coin Cell or GoldCaps®.
- V_LICELL supplies the SNVS domain of the i.MX 8 via the LICELL input of PMIC1.

The PCF85063 is supplied from V_VBAT as long as the V_3V3 of the PMIC is not yet switched on. The SNVS domain of the i.MX 8 is supplied from V_LICELL as long as the module supply voltage of 5 V is not yet present.

V_VBAT and V_LICELL can also be supplied from a common backup supply.

The realization makes it possible to use the TAMPER and SNVS functions of the i.MX 8 without having to waive the additional extremely power-saving RTC, as these are available independently of the assembly of the PCF85063.

➢ The RTC has the I²C address `0x51 / 101 0001b`

Table 11: Current consumption V_LICELL, V_VBAT

Voltage	Voltage	Current	Remark
V_LICELL (RTC in PMIC)	3.2 V	Typ. 7.1 µA, max. 10 µA	VCC5V = 0 V T_{amb} = +25 °C
	3.0 V	Typ. 7.1 µA, max. 10 µA	
	2.1 V	Typ. 6.1 µA, max. 10 µA	
V_VBAT (RTC PCF85063)	3.2 V	Typ. 0.44 µA, max. 0.7 µA [4]	
	3.0 V	Typ. 0.44 µA, max. 0.7 µA [4]	
	2.1 V	Typ. 0.4 µA, max. 0.7 µA [4]	

Attention: Malfunction or destruction	
	V_VBAT is supplied from internal 3.3 V, fed by the TQMa8x supply (V_5V_IN). V_VBAT can thus be used, for example, to load GoldCaps®. When Coin Cells (CR2032) and other non-rechargeable sources are used, external protective measures must be provided. This also applies if V_VBAT and V_LICELL are combined and supplied from a common source!

4: See data sheet PCF85063 (7).

3.2.3.1 CPU internal RTC

The i.MX 8 has an internal real-time clock, which is supplied via the power domain V_SNVS. The accuracy of the RTC is mainly determined by the characteristics of the crystal used. The type FC-135 used on the TQMa8x has a standard frequency tolerance of ±20 ppm at 25 °C (parabolic coefficient: max. -0.04 x 10-6 / °C^2).

The CPU internal RTC can always be used in ON mode. In OFF mode, it can only be used when the power supply is applied to module pin V_LICELL.

Note: Current consumption	
	The use of the CPU-internal RTC is not recommended for a long-term bridging, because the current consumption is too high to supply it e.g. with a coin cell for a longer time. Therefore, no further information about the current consumption of the CPU-internal RTC is given in this document.

3.2.3.2 External RTC

In addition to the CPU-internal RTC, module variants with optional RTC of the type PCF85063ATL are available. This is connected to the I2C1 bus of the i.MX 8 via a level translator.

The accuracy of the RTC is mainly determined by the characteristics of the crystal used. The type CM7V used on the TQMa8x has a standard frequency tolerance of ±20 ppm at 25 °C (parabolic coefficient: max. -0.04 x 10-6 / °C^2).

The RTC PCF85063ATL is supplied directly by V_VBAT only when the PMIC is switched off or the module supply is switched off. During runtime the PMIC takes over the supply via the internal module supply voltage V_3V3.

The interrupt output of the RTC is connected as open-drain signal (RTC_EVENT#) to a module pin header. This requires a pull-up to a voltage of up to 3.3 V on the mainboard.

3.2.4 Trust Secure Element

Depending on the module variant, a Trust Secure Element (TSE) is available on the TQMa8x. This is connected to the I2C1 bus of the i.MX 8 via a level translator.

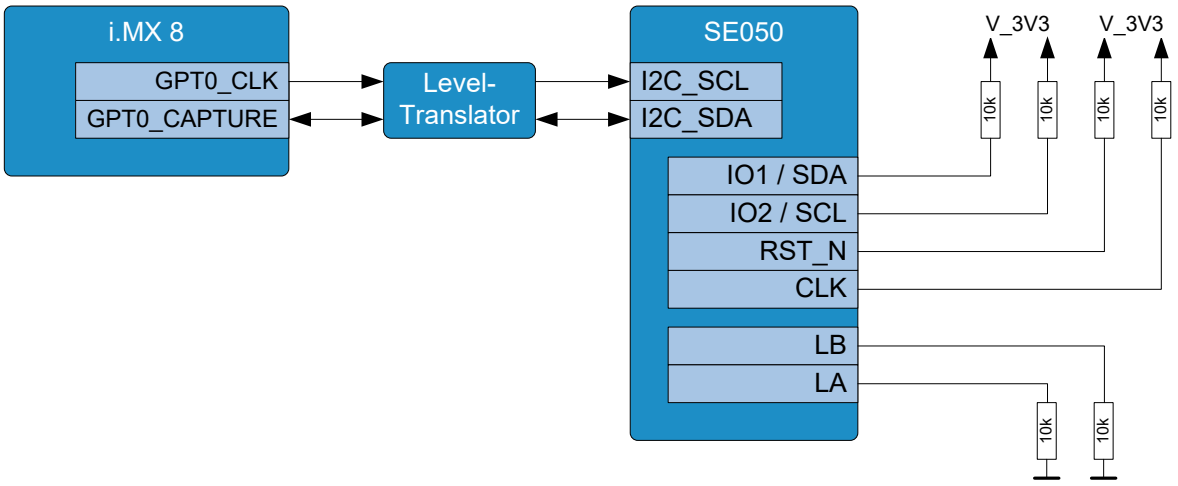

Figure 9: Block diagram Trust Secure Element

The selected SE050 chip from NXP provides additional smart card interfaces according to ISO14443 and ISO7816 in addition to the I^{2}C interface. If the SE050 is equipped as an option, the signals are wired as shown in the figure above.

3.2.5 Interfaces

3.2.5.1 TQMa8x internal interfaces

The following table shows the different i.MX 8 interfaces. The mentioned pins are set as standard multiplexing in the described function and directly routed to the TQMa8x connectors. Depending on the multiplexing, additional or a different number of interfaces are possible.

Table 12: TQMa8x internal interfaces

i.MX 8 interface	Remark
LPDDR4	2 × controller for LPDDR4-3200 2 × 32 bits per controller
QSPI	1 × QSPI (×4 or ×8) including optional DQS 1 × QSPI (×4)
eMMC	1 × HS400 (×8)
I²C	1 × PMIC-I²C on TQMa8x, routed to TQMa8x connectors 1 × I²C on TQMa8x, routed to TQMa8x connectors

3.2.5.2 Communication interfaces overview

The following table shows the different i.MX 8 interfaces. The mentioned pins are set as standard multiplexing in the described function and directly routed to the TQMa8x connectors. Depending on the multiplexing, additional or a different number of interfaces are possible.

Table 13: Communication interfaces overview

i.MX 8 interface	Remark
ADC	3 × Input
Boot Mode	–
CAN	–
ENET	2 × MDIO RGMII (1.8 V) or RMII (3.3 V) supported IO voltage defined by V_ENET_IN
ESAI	2 × TX and RX Data
GPIO [5]	18 × GPIO (2 × 3.3 V) 4 × MIPI DSI / 4 × MIPI CSI 6 × SCU / 4 × M4 2 × LVDS 1 × SIM
HDMI Rx	1 × including dedicated DDC channel
HDMI Tx	1 × including dedicated DDC channel
I²C	1 × for PMIC 2 × for other periphery 1 × HDMI I²C 2 × LVDS I²C 2 × MIPI CSI 2 × MIPI DSI
JTAG	–
LVDS	2 controllers each with 2 channels of 4 differential pairs each
MIPI CSI	2 × GPIO and 1 × I²C each
MIPI DSI	2 × GPIO and 1 × I²C each
MLB (differential)	–
MLB (Single Ended)	–
PCIe	1 × In/Output for REFCLK, CLKREQ#, PERST# and WAKE# respectively

5: Number of GPIOs available for DualMax is very limited.

i.MX 8 interface	Remark
PWM	2 × PWM controller 2 × MIPI DSI 2 × LVDS
QSPI	1 × QSPI (x4) incl. optional DQS
SAI (I2S)	TX and RX Data
S/PDIF	Incl. Clock Input
TAMPER	2 × IN / 2 × OUT
UART	2 × incl. RTS/CTS 1 × without RTS/CTS 2 × M4 (without RTS/CTS) 1 × SCU (without RTS/CTS)
USB 2.0 HSIC	1 ×
USB 2.0 OTG	2 ×
USB 3.0	Can only be used with OTG2
uSDHC2 (SD card)	1 × USDHC (×4) with WP and CD#
SATA	Optional: PCIe
SIM	1 × GPIO
SPI	3 × with two CS each
TAMPER	2 × IN, 2 × OUT

3.2.5.3 Unused Pins

To ensure flexible use of all i.MX 8 functions, all pins or interfaces of the i.MX 8 are routed to the module headers where possible and are thus available on the base board. Apart from some pins that are not available due to internal module functions such as LPDDR4 and for technical reasons, there are minor restrictions in the availability of i.MX 8 pins, which are shown in the following table.

Table 14: Module internal interfaces that are not available at the module connectors

Interface i.MX 8	Quantity	Chapter	Note
EMMC0	1	eMMC NAND flash	Use for optional eMMC, 8 bit
QSPI0A / QSPI0B	1	QSPI NOR flash	Use for optional SPI-NOR-Flash
DDR_CH0 / DDR_CH1	1	LPDDR4 SDRAM	Use for 2x LPDDR4, 2x 32 bit

3.2.5.4 ADC

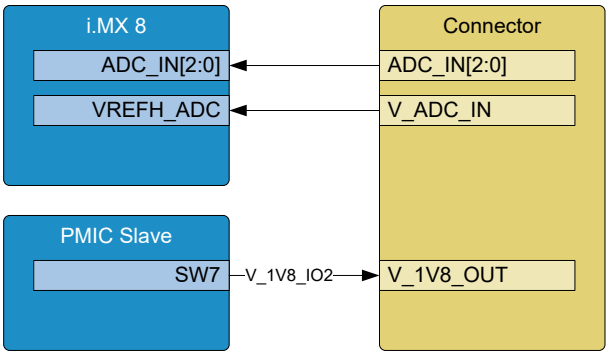

Figure 10: Block diagram ADC

The i.MX 8 has two 12 bit ADC interfaces with four channels each, of which ADC_IN[2:0] are three ADC inputs for analog voltages up to 1.8V. The ADC parameters can be found in the respective data sheets (2), (3).

The ADC inputs require a 1.8 V reference voltage at TQMa8x pin V_ADC_IN (X1-B9). The TQMa8x provides an internal reference voltage of 1.8 V at V_1V8_OUT, which can be directly used for applications without high requirements for accuracy.

A separate voltage reference must be connected to V_ADC_IN for high-precision measurements. Its specification depends on the requirements of the measurement task, but must have at least the following parameters:

- V_ADC_IN voltage: 1.0 V to 2.1 V (typ. 1.8 V)
- V_ADC_IN current load: Peak 20 mA (estimated)
- Compliance with i.MX 8 Power Sequencing: Switch on with V_1V8_IO2

The voltage input at pin V_ADC_IN is additionally filtered on the TQMa8x. See also chapter 3.2.6.

Table 15: ADC

Signal	Power Domain	Remark
ADC_IN[2:0]	VDD_ADC_1P8 (1.8 V)	–
V_1V8_IN	–	See chapter 3.2.6

3.2.5.5 CAN0 / CAN1

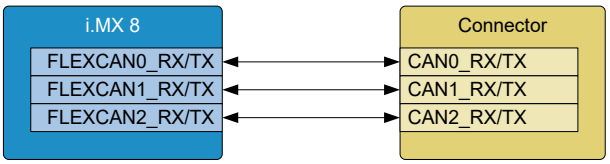

Figure 11: Block diagram CAN

The i.MX 8 provides three CAN interfaces, which support CAN FD (Flexible Data Rate) as well as the CAN protocol 2.0B. All three are available on module headers. The necessary driver modules are to be rea-lized on the mainboard.

Table 16: CAN signals

Signal	Power Domain
CAN[2:0]_RX	VDD_FLEXCAN_1P8_3P3 (1.8 V)
CAN[2:0]_TX	

3.2.5.6 Ethernet

The i.MX 8 provides two Gigabit Ethernet MACs, which support the 10/100/1000 Mbit/s modes. External PHYs can be connected via RMII or RGMII. Due to the internal TQMa8x power supply and CPU Errata ERR010913, the following design criteria apply:

- ENET0 and ENET1 can only be configured together for either RGMII or RMII.
- An IO voltage of 2.5 V for the ENET0 and ENET1 interfaces is not supported.
- Only an IO voltage of 1.8 V can be used for RGMII and only 3.3 V for RMII.

Since the IO voltage for ENET0, ENET1 and MDIO depends on the selected interface, these are connected to the supply input V_ENET_IN of the TQMa8x and thus allow the IO voltage to be determined by the user (see chapter 3.2.6).

The signal names chosen on the TQMa8x refer to the usage as RGMII. The relevant signal names for RMII are defined in the i.MX 8 data sheets (2), (3). Both interfaces have a dedicated MDIO interface for PHY configuration.

Table 17: ENET0 signals

Signal	i.MX 8 ball	Power Group
ENET0_TXD[3:0]	ENET0_RGMII_TXD[3:0]	VDD_ENET0_1P8_3P3
ENET0_TXC	ENET0_RGMII_TXC	
ENET0_TX_CTL	ENET0_RGMII_TX_CTL	
ENET0_RXD[3:0]	ENET0_RGMII_RXD[3:0]	
ENET0_RXC	ENET0_RGMII_RXC	
ENET0_RX_CTL	ENET0_RGMII_RX_CTL	
ENET0_MDIO	ENET0_MDIO	VDD_ENET_MDIO_1P8_3P3
ENET0_MDC	ENET0_MDC	
ENET0_REFCLK_125M_25M	ENET0_REFCLK_125M_25M	

Table 18: ENET1 signals

Signal	i.MX 8 ball	Power Group
ENET1_TXD[3:0]	ENET1_RGMII_TXD[3:0]	VDD_ENET1_1P8_2P5_3P3
ENET1_TXC	ENET1_RGMII_TXC	
ENET1_TX_CTL	ENET1_RGMII_TX_CTL	
ENET1_RXD[3:0]	ENET1_RGMII_RXD[3:0]	
ENET1_RXC	ENET1_RGMII_RXC	
ENET1_RX_CTL	ENET1_RGMII_RX_CTL	
ENET1_MDIO	ENET1_MDIO	VDD_ENET_MDIO_1P8_3P3
ENET1_MDC	ENET1_MDC	
ENET1_REFCLK_125M_25M	ENET1_REFCLK_125M_25M	

3.2.5.7 ESAI

The i.MX 8 has two independent ESAI interfaces. Among others, I2S, AC97 and TDM are supported. Both are available on module headers.

The following table shows the used signals of the ESAI interface:

Table 19: ESAI signals

Signal	I/O	Power Domain
ESAI0_FSR	I	VDD_ESAI0_MCLK_1P8_3P3 (1.8 V)
ESAI0_FST	O	
ESAI0_SCKR	I	
ESAI0_SCKT	O	
ESAI0_TX0	O	
ESAI0_TX1	O	
ESAI0_TX2_RX3	I/O	
ESAI0_TX3_RX2	I/O	
ESAI0_TX4_RX1	I/O	
ESAI0_TX5_RX0	I/O	
ESAI1_FSR	I	VDD_ESAI_SPDIF_1P8_2P5_3P3 (1.8 V)
ESAI1_FST	O	
ESAI1_SCKR	I	
ESAI1_SCKT	O	
ESAI1_TX0	O	
ESAI1_TX1	O	
ESAI1_TX2_RX3	I/O	
ESAI1_TX3_RX2	I/O	
ESAI1_TX4_RX1	I/O	
ESAI1_TX5_RX0	I/O	

3.2.5.8 SAI

In addition to the Enhanced Serial Audio Interfaces (ESAI), the CPU also offers Synchronous Audio Interfaces (SAI). These also support I2S, AC97 and TDM, as well as various other codecs.

Table 20: SAI signals

Signal	I/O	Power-domain
SAI1_TXC	O	VDD_SPI_SAI_1P8_3P3
SAI1_TXFS	O	
SAI1_TXD	O	
SAI1_RXC	I	
SAI1_RXFS	I	
SAI1_RXD	I	

3.2.5.9 SPDIF

Furthermore, the CPU supports the Sony/Philips Digital Interface (SPDIF). This is fully available at the module header X3.

Table 21: SPDIF signals

Signal	I/O	Power-domain
SPDIF_EXT_CLK	O	VDD_ESAI1_SPDIF_SPI_1P8_3P3
SPDIF_RX	I	
SPDIF_TX	O	

3.2.5.10 GPIOs

Except for dedicated differential signals (e.g. MIPI DSI/CSI, USB), all CPU signals can be configured as GPIO signals.
The signals GPIO5_IO[20:19] and GPIO5_IO[23] are switched by the SD card driver with USDHC1_VSELECT.
When used on the customer specific carrier board, compatibility with 1.8 V / 3.3 V should be ensured.
The following signals are multiplexed as GPIO as their primary function:

Table 22: GPIOs

Signal	Power Domain	Remark
GPIO0_IO05	VDD_SIM_1P8_3P3 (1.8 V / 3.3 V)	IO voltage defined by V_SIM_IN (see chapter 3.2.6)
GPIO1_IO[15:14]	VDD_LVDS_DIG_1P8_3P3 (1.8 V)	
GPIO2_IO[03:02]	VDD_HDMI_TX0_DIG_3P3 (3.3 V)	
GPIO2_IO17	VDD_ESAI1_SPDIF_SPI_1P8_3P3 (1.8 V)	
GPIO2_IO21		
GPIO4_IO07	VDD_USDHC_VSELECT_1P8_3P3 (1.8 V)	
GPIO4_IO09		
GPIO4_IO11		
GPIO4_IO[12:09]		
GPIO5_IO[20:19]	VDD_USDHC1_1P8_3P3 (1.8 V / 3.3 V)	IO voltage determined by SD card driver (see chapter 3.2.4.23)
GPIO5_IO23		
GPIO5_IO[29:24]	VDD_USDHC2_1P8_3P3 (1.8 V / 3.3 V)	IO voltage by default 1.8 V Can be set by USDHC2_VSELECT through placement option
M41_GPIO0_[01:00]	VDD_M4_GPT_UART_1P8_3P3 (1.8 V)	
M40_GPIO0_[01:00]		
SCU_GPIO0_[07:02]	VDD_SCU_1P8 (1.7 V)	TQMa8x in series production: 1.7 V

Note: SCU GPIO	
	Due to changes in the i.MX 8 specification, the IO voltage of the SCU GPIO (VDD_SCU_1P8) is reduced from 1.8 V to 1.7 V for the TQMa8x in series production.

3.2.5.11 HDMI-In

The i.MX 8 provides an HDMI input. The HDMI RX supports resolutions of up to 4K at 60 fps. However this function is not supported in the current chip version. The current data sheets must therefore always be observed.

Table 23: HDMI RX signals

Signal	I/O	Power Domain
HDMI_RX_ARC_N/P	I/O	VDD_HDMI_RX0_1P8 (1.8 V)
HDMI_RX_CEC	O	
HDMI_RX_CLK_N/P	I	
HDMI_RX_DATA0_N/P	I	
HDMI_RX_DATA1_N/P	I	
HDMI_RX_DATA2_N/P	I	
HDMI_RX_DDC_SCL	O	
HDMI_RX_DDC_SDA	I/O	
HDMI_RX_HPD	I	
HDMI_RX_MON_5V	I	

3.2.5.12 HDMI-Out

In addition to the LVDS and DSI ports, a multifunctional HDMI interface is also available.
The following display specifications are supported:

- HDMI 2.0a
- Display-Port 1.3
- Embedded Display-Port 1.4

For HDMI and DisplayPort different conversions on the carrier board are required. The HDMI signals are therefore available without further wiring from the i.MX 8 to the TQMa8x connectors. The recommended wiring can be found in the Developers Guide (6).
When using the display port, the names of the differential signal pairs change in relation to the TQMa8x signal name (HDMI_TX). Please refer to the multiplexing table (8) or directly to the NXP Config Tool.

Table 24: HDMI TX Signals

Signal	I/O	Power Domain	Remark
HDMI_TX_ARC_N/P	I/O	VDD_HDMI_TX0_1P8 (1.8 V)	–
HDMI_TX_CEC	O		–
HDMI_TX_CLK_N/P	I		Display-Port: DATA3_N/P
HDMI_TX_DATA0_N/P	I		Display-Port: DATA2_N/P
HDMI_TX_DATA1_N/P	I		Display-Port: DATA1_N/P
HDMI_TX_DATA2_N/P	I		Display-Port: DATA0_N/P
HDMI_TX_DDC_SCL	O		–
HDMI_TX_DDC_SDA	I/O		–
HDMI_TX_HPD	I		–
HDMI_TX_MON_5V	I		–

3.2.5.13 I²C

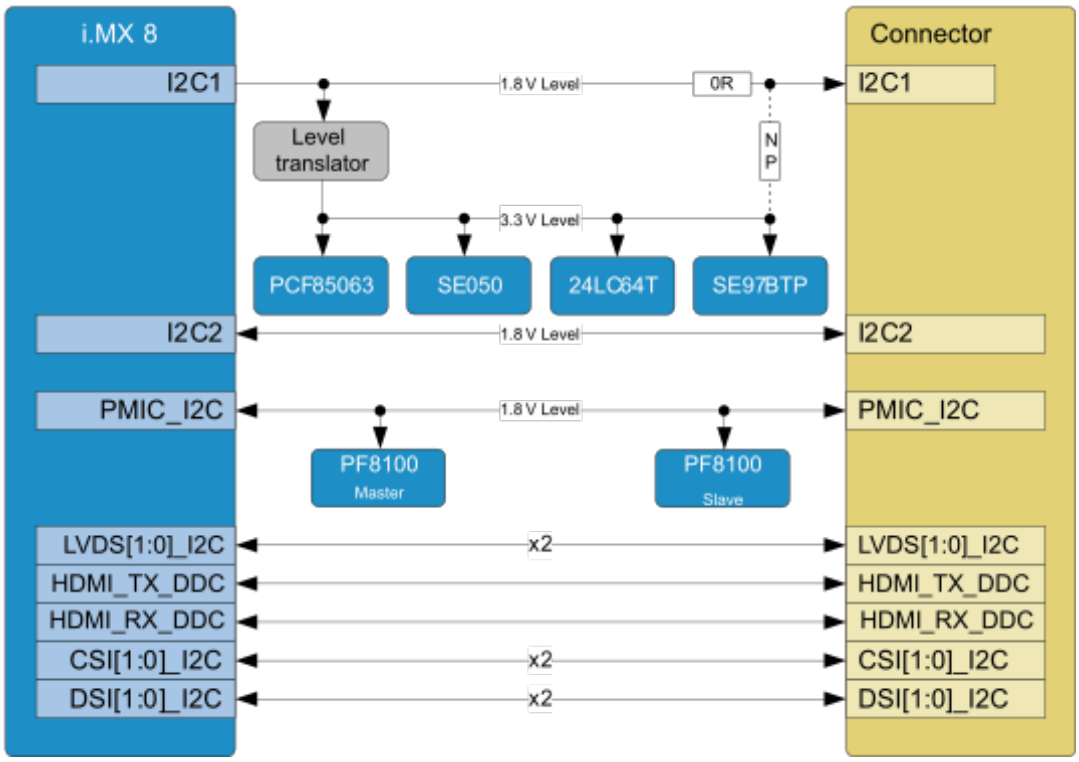

Figure 12: Block diagram I²C

The TQMa8x provides several I²C interfaces. Some of them are reserved for the display interfaces.

I2C1 is used for internal components, therefore also the necessary pull-up resistors are already equipped on the TQ module. A level shifter on the module raises the bus voltage to 3.3 V. I2C1 with 1.8 V or 3.3 V level can be provided on module connectors via assembly option. The standard bus voltage is 1.8 V. 3.3 V types are used for the RTC, the temperature sensor and the EEPROM.

The PMIC_I2C interface is a special I²C bus of the SCU interface, which can be used to configure the PMIC by the SCU firmware. Unlike the reference design from NXP, configuration of the PMIC during runtime is not required, since all necessary configurations are predefined via OTP.

An I²C bus is also available for the LVDS, CSI and DSI interfaces, each of which is available twice. A DDC interface is available for HDMI TX and HDMI RX.

The following table shows the I²C addresses used on the TQMa8x:

Table 25: I²C addresses

Bus	Device	Address	Pull-Ups	Remark
I2C1	Temp. sensor SE97BTP	0x1B / 001 1011b	2.2 kΩ on TQMa8x	Temperature sensor
		0x53 / 101 0011b		EEPROM Read/Write
		0x33 / 011 0011b		EEPROM Protection Command
	EEPROM 24LC64T	0x57 / 101 0111b		Assembly option
	RTC PCF85063	0x51 / 101 0001b		Assembly option
	TSE SE050	0x48 / 100 1000b		Assembly option
I2C2	–	–	Optional Pull-Ups on TQMa8x	–
PMIC_I2C	PMIC PF8100 #1	0x08 / 000 1000b	2.2 kΩ on TQMa8x	–
PMIC_I2C	PMIC PF8100 #2	0x09 / 000 1001b		–
LVDS[1:0] HDMI TX HDMI RX MIPI DSI[1:0] MIPI CSI[1:0]	–	–	Placement on carrier board	–

The following table shows the signals used for the I²C interfaces:

Table 26: I²C signals

Signal	I/O	Power Domain	Note
I2C[2:1]_SCL	O	VDD_M4_GPT_UART_1P8_3P3 (1.8V)	
I2C[2:1]_SDA	I/O		
PMIC_I2C_SCL	O	VDD_SCU_1P8 (1.8V)	1,7 V
PMIC_I2C_SDA	I/O		1,7 V
MIPI_CSI[1:0]_SCL	O	VDD_MIPI_CSI[1:0]_DIG (1.8V)	
MIPI_CSI[1:0]_SDA	I/O		
MIPI_DSI[1:0]_SCL	O	VDD_MIPI_DSI_DIG_1P8_3P3 (1.8V)	
MIPI_DSI[1:0]_SDA	I/O		
HDMI_TX_DDC_SCL	O	VDD_HDMI_TX0_1P8 (1.8V)	
HDMI_TX_DDC_SDA	I/O		
HDMI_RX_DDC_SCL	O	VDD_HDMI_RX0_1P8 (1.8V)	
HDMI_RX_DDC_SDA	I/O		
LVDS[1:0]_I2C0_SCL	O	VDD_LVDS_DIG_1P8_3P3 (1.8V)	
LVDS[1:0]_I2C0_SDA	I/O		

3.2.5.14 JTAG

The JTAG signals of the CPU are directly connected to module connectors. The pull-up wiring must be done on the mainboard according to the i.MX8 QM/i.MX8 QXP Hardware Developers Guide.

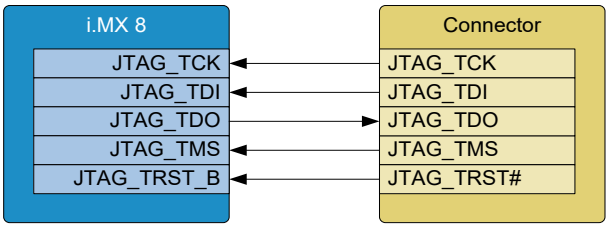

Figure 13: Block diagram JTAG

Table 27: JTAG signals

Signal	I/O	Power-Domain
JTAG_TCK	I	VDD_SCU_1P8
JTAG_TDI	I	
JTAG_TDO	O	
JTAG_TMS	I	
JTAG_TRST#	I	

3.2.5.15 LVDS

The i.MX 8 provides two LVDS controllers, each with dual LVDS or two channels. Each channel uses four differential lanes for transmission.

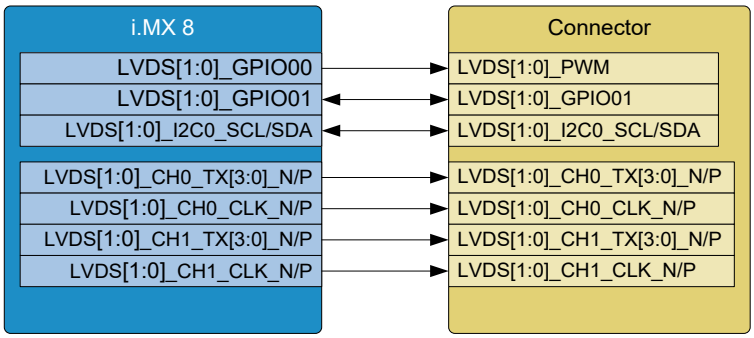

Figure 14: Block diagram LVDS

For each LVDS interface, one I2C bus as well as one GPIO and one PWM signal are provided.

Table 28: LVDS signals

Signal	I/O	Power Domain
LVDS0_PWM	O	VDD_LVDS_DIG_1P8_3P3 (1.8 V)
LVDS0_GPIO01	I/O	
LVDS0_I2C0_SCL	O	
LVDS0_I2C0_SDA	I/O	
LVDS0_CH0_TX[3:0]_N/P	O	VDD_LVDS0_1P8 (1.8 V)
LVDS0_CH0_CLK_N/P	O	
LVDS0_CH1_TX[3:0]_N/P	O	
LVDS0_CH1_CLK_N/P	O	
LVDS1_PWM	O	VDD_LVDS_DIG_1P8_3P3 (1.8 V)
LVDS1_GPIO01	I/O	
LVDS1_I2C0_SCL	O	
LVDS1_I2C0_SDA	I/O	
LVDS1_CH0_TX[3:0]_N/P	O	VDD_LVDS1_1P8 (1.8 V)
LVDS1_CH0_CLK_N/P	O	
LVDS1_CH1_TX[3:0]_N/P	O	
LVDS1_CH1_CLK_N/P	O	

3.2.5.16 MIPI CSI

Two MIPI CSI interfaces with four lanes each are available as differential camera input. Up to 1.5 Gbps can be transmitted and a maximum image format of 4K with 30 fps can be processed.

Both CSI interfaces are assigned an I2C bus, two GPIO signals (reset, power enable) and a master clock output as standard.

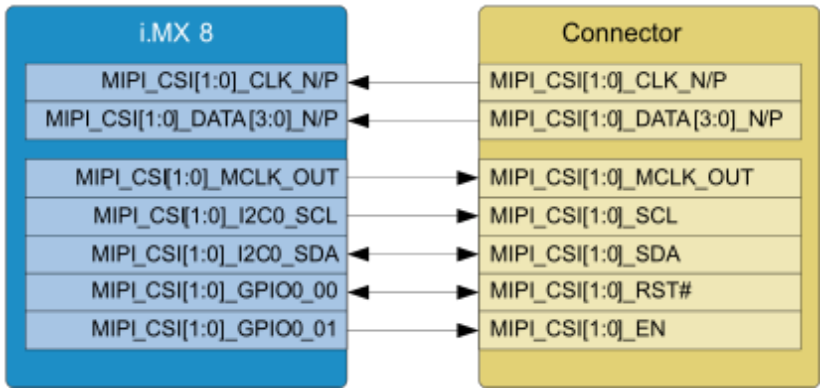

Figure 15: Block diagram MIPI CSI

Table 29: MIPI CSI signals

Signal	I/O	Power-Group
MIPI_CSI[1:0]_CLK_N/P	I	VDD_MIPI_CSI[1:0]_1P8 (1.8V)
MIPI_CSI[1:0]_DATA0_N/P	I	
MIPI_CSI[1:0]_DATA1_N/P	I	
MIPI_CSI[1:0]_DATA2_N/P	I	
MIPI_CSI[1:0]_DATA3_N/P	I	
MIPI_CSI[1:0]_I2C_SCL	O	VDD_MIPI_CSI_DIG_1P8 (1.8V)
MIPI_CSI[1:0]_I2C_SDA	I/O	
MIPI_CSI[1:0]_MCLK_OUT	O	
MIPI_CSI[1:0]_RST#	I/O	
MIPI_CSI[1:0]_EN	O	

3.2.5.17 MIPI DSI

Two DSI interfaces are available for the output of serial display data. Each lane can transmit from 80 Mbps to 1.5 Gbps. The supported image/video formats can be found in the i.MX 8 specification.

In addition, the interfaces offer an I2C master for each of the two DSI ports as well as dedicated GPIOs.

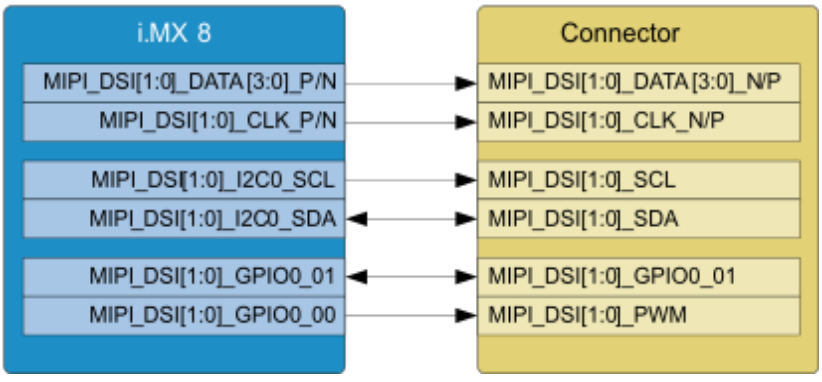

Figure 16: Block diagram MIPI DSI

Table 30: MIPI DSI Signals

Signal	I/O	Power-Group
MIPI_DSI[1:0]_CLK_N/P	O	VDD_MIPI_DSI[1:0]_1P8
MIPI_DSI[1:0]_DATA0_N/P	O	
MIPI_DSI[1:0]_DATA1_N/P	O	
MIPI_DSI[1:0]_DATA2_N/P	O	
MIPI_DSI[1:0]_DATA3_N/P	O	
MIPI_DSI[1:0]_I2C_SCL	O	VDD_MIPI_DSI_DIG_1P8_3P3
MIPI_DSI[1:0]_I2C_SDA	I/O	
MIPI_DSI[1:0]_GPIO0_01	I/O	
MIPI_DSI[1:0]_PWM	O	

3.2.5.18 MLB

The i.MX 8 has an MLB interface according to the MediaLB protocol, which is completely available at a module connector. However, according to the current data sheet (Rev. 2 / 05/2021), this interface is not supported and can therefore be used for muxing other signals. Further information can be found in the latest data sheet.

Table 31: MLB signals

Signal	I/O	Power-Group
MLB_CLK	O	VDD_MLB_DIG_1P8_3P3
MLB_DATA	O	
MLB_SIG	O	
MLB_CLK_N/P	O	VDD_MLB_1P8
MLB_DATA_N/P	O	
MLB_SIG_N/P	O	

3.2.5.19 PCIe

The i.MX 8 provides a PCIe 3.0 controller with two lanes or two PCIe 3.0 controllers with one lane each.
In addition to the two lanes, the SATA interface (see chapter 3.1.3.18) can be used as a PCIe lane.

Due to the experience regarding jitter requirements with previous i.MX processors, a reference clock of 100 MHz should be applied to the module as an external clock source. All series components (capacitors and resistors) to be placed according to the PCIe standard must be placed on the mainboard by the customer.

The following table shows the used signals of the PCIe interfaces:

Table 32: PCIe signals

Signal	I/O	Power-Group
PCIE[1:0]_TX_N	O	VDD_PCIE[1:0]_1P0
PCIE[1:0]_TX_P		
PCIE[1:0]_RX_N	I	
PCIE[1:0]_RX_P		
PCIE0_REFCLK100M_N	I/O	VDD_PCIE0_1P0
PCIE0_REFCLK100M_P		
PCIE[1:0]_CLKREQ#	O	VDD_PCIE_DIG_1P8_3P3
PCIE[1:0]_WAKE#	I	
PCIE[1:0]_PERST#	I	

3.2.5.20 PWM

The i.MX 8 has four PWM channels, two of them are routed out.
Separate PWM signals are available for the LVDS and DSI interfaces.

Table 33: PWM signals

Signal	I/O	Power Domain
PWM2_OUT	O	VDD_M4_GPT_UART_1P8_3P3 (1.8 V)
PWM3_OUT	O	

3.2.5.21 MCLK

The MCLK signals are available as clock input and clock output for other interfaces (e.g. PCIe reference clock). For more information, refer to the i.MX 8 Reference Manual (8).

Table 34: MCLK signals

Signal	I/O	Connector	Power Domain
MCLK_IN	I	X1	VDD_ESAI0_MCLK_1P8_3P3
MCLK_OUT	O	X2	

3.2.5.22 FTM

The i.MX 8 offers a FlexTimer module (FTM), which can be used to control motors or power management applications by generating PWM signals. More detailed information can be found in the i.MX 8 Reference Manual (8).

Table 35: FTM

Signal	I/O	Connector	Power Domain
FTM_CH[2:0]	I/O	X1	VDD_ESAI1_SPDIF_SPI_1P8_3P3

3.2.5.23 SPI

The SPI interfaces of the i.MX 8 are full-duplex capable and support master and slave modes..

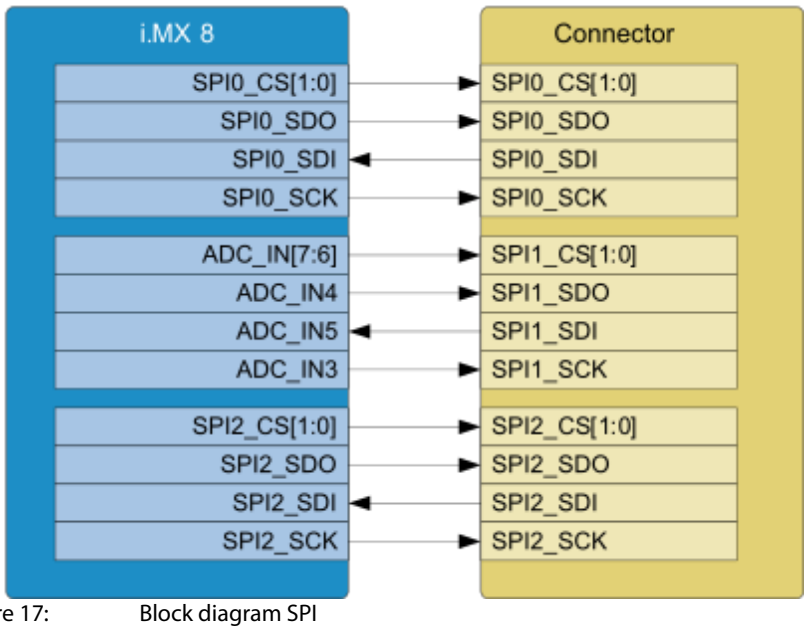

Figure 17: Block diagram SPI

All three SPI interfaces are led out with two chip select signals each:

Table 36: SPI signals

Signal	I/O	Power-Domain
SPI[2;0]_CS0	O	VDD_SPI_SAI_1P8_3P3
SPI[2;0]_CS1	O	
SPI[2;0]_SCK	O	
SPI[2;0]_SDI	I	
SPI[2;0]_SDO	O	
SPI1_CS0	O	VDD_ADC_1P8
SPI1_CS1	O	
SPI1_SCK	O	
SPI1_SDI	I	
SPI1_SDO	O	

3.2.5.24 TAMPER

The i.MX 8 has two tamper inputs and two tamper outputs, which are completely routed out to a module pin header.

Note: Tamper pins	
	Due to a change in the i.MX 8 specification, the IO voltage of the TAMPER signals (VDD_SCU_1P8) is reduced from 1.8 V to 1.7 V for the TQMa8x in series production.

Table 37: TAMPER signals

Signal	I/O	Power Domain	Remark
TAMPER_IN[1:0]	I	VDD_SNVS_1P8 (1.8 V)	TQMa8x in series production: 1.7 V
TAMPER_OUT[1:0]	O		

3.2.5.25 UART (Debug)

The i.MX 8 provides several UART interfaces. UART[2:0] interfaces are available for general usage. Only UART[1:0] provide RTS# and CTS# signals. One of the UARTs can be configured by software to output kernel debug messages.
The SCU has its own UART for debug output. This should be implemented on the carrier board separately from the debug UART.

Note: SCU UART	
	Due to changes in the i.MX 8 specification, the IO voltage of the SCU UART (VDD_SCU_1P8) is reduced from 1.8 V to 1.7 V for the TQMa8x in series production.

Table 38: UART (Debug) signals

Signal	I/O	Power Domain
UART[1:0]_RTS#	O	VDD_M4_GPT_UART_1P8_3P3 (1.8 V)
UART[1:0]_CTS#	I	
UART[1:0]_TX	O	
UART[1:0]_RX	I	
UART2_RX	I	VDD_LVDS_DIG_1P8_3P3 (1.8 V)
UART2_TX	O	

Table 39: SCU UART signals

Signal	I/O	Power Domain	Remark
SCU_UART_RX	I	VDD_SCU_1P8 (1.8 V)	TQMa8x in series production: 1.7 V
SCU_UART_TX	O		

3.2.5.26 UART (M4)

More UARTs are available exclusively for both Cortex®-M4 controllers.

Table 40: UART (M4) signals

Signal	I/O	Power Domain
M40_UART_RX	I	VDD_M4_GPT_UART_1P8_3P3 (1.8 V)
M40_UART_TX	O	
M41_UART_RX	I	
M41_UART_TX	O	

3.2.5.27 USB 2.0 HSIC

The i.MX 8 has a USB host as HSIC interface for connection to an external USB HSIC PHY. All other signals (e.g. OC# or VBUS) must be managed by the PHY. The interface transmits data at 480 MHz and can only be used as a direct connection from the controller to the HSIC chip. HSIC is not available with the TQMa8DM.

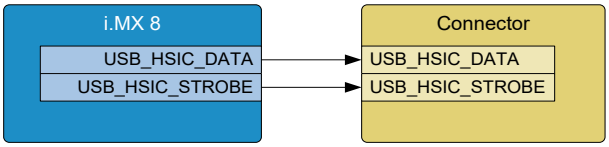

Figure 18: Block diagram USB 2.0 HSIC

Table 41: USB HSIC

Signal	Power Domain	Remark
USB_HSIC_DATA	VDD_USB_HSIC0_1P2 (1.2 V)	NC on TQMa8DM
USB_HSIC_STROBE		NC on TQMa8DM

Note: USB 2.0 HSIC	
	The length of the routed HSIC signals on the carrier board must not exceed 60 mm (2.36 inches) starting from the TQMa8x mating connectors on the carrier board. HSIC is not available with the TQMa8DM.

3.2.5.28 USB 3.0 SS and 2.0 OTG

The i.MX 8 provides a USB 3.0 controller (incl. USB 2.0 OTG) and a separate controller for another USB 2.0 OTG.
The OTG controller can also be configured as a dedicated Host or Client.
When using the Super-Speed signals (SS) for a USB 3.0 interface, the USB 2.0 signals of the OTG2 must be used, as only these can act together as an interface.

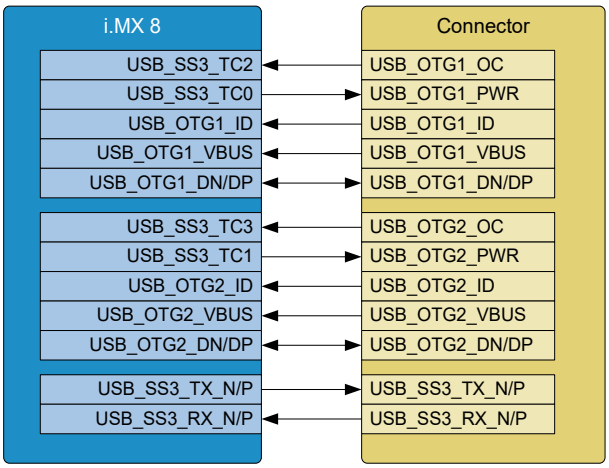

Figure 19: Block diagram USB / USB OTG

Table 42: USB 3.0 SS and 2.0 OTG

Signal	I/O	Power Domain	Remark
USB_SS_TX_N/P	O	VDD_USB_SS3_1P8 (1.8 V)	Use for USB 3.0 interface
USB_SS_RX_N/P	I		
USB_OTG2_OC	I	VDD_USB_SS3_3P3 (3.3 V)	
USB_OTG2_PWR	O		
USB_OTG2_ID	I	VDD_USB_OTG2_3P3 (3.3 V)	
USB_OTG2_VBUS	Power		
USB_OTG2_DN/DP	I/O		
USB_OTG1_OC	I	VDD_USB_SS3_3P3 (3.3 V)	–
USB_OTG1_PWR	O		–
USB_OTG1_ID	I	VDD_USB_OTG1_3P3 (3.3 V)	–
USB_OTG1_VBUS	Power		–
USB_OTG1_DN/DP	I/O		–

3.2.5.29 USDHC (SD card)

In addition to the eMMC interface, the i.MX 8 has two further USDHC interfaces:

- USDHC1: 8 bit SD card / eMMC interface
- USDHC2: 4 bit SD card interface

The USDHC1 interface is intended for use with SD cards, USDHC2 is muxed as GPIO. Both VSELECT signals are connected to one of the two PMICs each, USDHC2_VSELECT however only optionally, in order to be able to use the driver-side voltage switching of the slave PMIC. Thus up to two SD card interfaces can be realized. By default the CPU pin USDHC2_VSELECT is available as GPIO4_IO10 at the module header.

USDHC2 is not available for the i.MX 8 DualMax, therefore the 8-bit interface USDHC1 is multiplexed for the use of SD cards.
For the optional use of USDHC2, USDHC2_VSELECT can also be connected to the Slave-PMIC by an assembly option in order to use the driver-side voltage switching.

The IO voltage of USDHC1 and USDHC2 is supplied by the LDO2 of both PMICs, whose IO voltage can be set to 1.8 V or 3.3 V with signal USDHC[2:1]_VSELECT. The VSELECT signal is automatically switched by the driver in order to use the fastest possible mode depending on the SD card used. In addition to the dedicated SD card signals, there are other GPIOs whose IO voltage is also determined by VSELECT. See chapter 3.2.4.8.

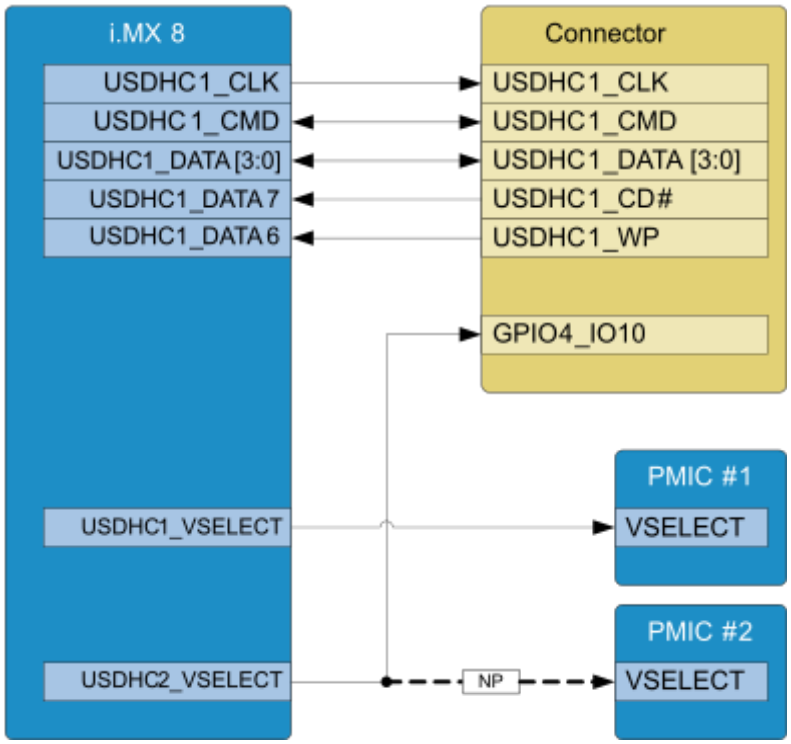

Figure 20: Block diagram USDHC2

Table 43: USDHC

Signal	I/O	Power Domain	Remark
USDHC2_VSELECT	O	VDD_USDHC_VSELECT_1P8_3P3 (1.8 V)	GPIO_IO10
USDHC1_VSELECT	O		Used on the TQMa8x internally
USDHC1_WP	I	VDD_USDHC1_1P8_3P3 (1.8 V / 3.3 V)	–
USDHC1_CD#	I		–
USDHC1_CLK	O		–
USDHC1_CMD	I/O		–
USDHC1_DATA0	I/O		–
USDHC1_DATA1	I/O		–
USDHC1_DATA2	I/O		–
USDHC1_DATA3	I/O		–

Note: USDHC	
	Due to the internal wiring of USDHC1_WP and USDHC1_CD# no pull circuitry has to be provided on the carrier board for these signals. These are already present on the TQMa8x. Both voltages V_SD1 and V_SD2 supplying the USDHC interfaces are not routed down from the module, therefore no connection of external pull-ups to the data lines is possible. It is therefore recommended to use the CPU internal pull-ups.

3.2.5.30 SIM

The i.MX 8 has a SIM interface according to standard ISO7816. Except SIM0_GPIO0_00 all signals are available at the module pin header X1.

The following table shows the used signals of the SIM interface:

Table 44: SIM signals

Signal	I/O	Power-Domain
SIM_CLK	O	VDD_SIM0_1P8_3P3
SIM_IO	I/O	
SIM_PD	I	
SIM_PWR_EN	O	
SIM_RST	O	

The power group for SIM is routed to the supply input V_SIM_IN of the module and thus allow the definition of the IO voltage depending on the customer application.

3.2.5.31 SATA

The i.MX 8 provides a SATA 3.0 controller. A PCI 3.0 lane can also be output via the PHY.

Irrespective of the selected function of the signals, the impedance of the i.MX 8 is internally set to 85 Ω and also adopted for the TQMa8x. The interface is therefore optimized for PCI.

When using the SATA controller, it is recommended to use a SATA Redriver on the carrier board, especially when using SATA cable connectors. Thus, the impedance is optimally designed for the standardized cables. NXP recommends a differential impedance of 100 Ω in this case.

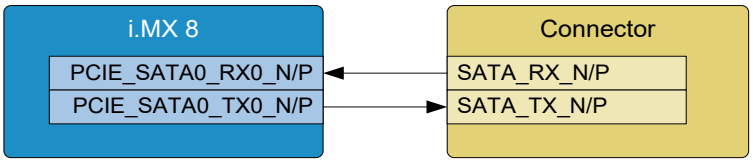

Figure 21: Block diagram SATA

Table 45: SATA

Signal	I/O	Power Domain	Remark
SATA_RX_N/P	I	VDD_PCIE_SATA0_PLL_1P8 (1.8 V)	Can be multiplexed as PCIe
SATA_TX_N/P	O		

3.2.6 Reset

Reset inputs and outputs are available on the TQMa8x connectors.
The following table describes the reset and config signals available on the TQMa8x connector.

Table 46: Reset signals

Signal	I/O	Power domain	Function	TQMa8x	Remark
RESET_IN#	I	V_ANA_1P8 (1.8 V)	i.MX 8 and NOR-Flash reset input	X1-A15	Low Active signal Deactivate: float or connect to 1.8 V
RESET_OUT#	O	Externally defined with Pull-up (max. 6.5 V)	Reset output of the module for mainboard components	X1-A14	Activated by PMIC or RESET_IN# Open-Drain; low active
IMX_ONOFF	I	V_SNVS_CAP	ON / OFF signal of i.MX 8	X1-A109	Low active signal Deactivate: float

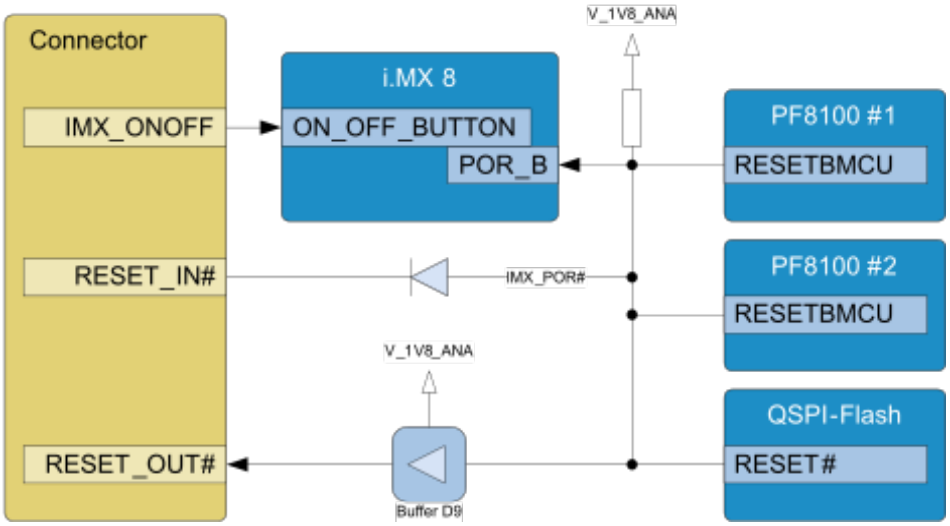

Figure 22: Block diagram Reset

Note: Pull-Up voltage for RESET_OUT#	
	Switching off the TQMa8x power supply V_5V_IN or deactivating PMIC_PWR_ON results in a shutdown of the circuit on the TQMa8x responsible for RESET_OUT#. From this point RESET_OUT# can no longer be kept low by the TQMa8x. Depending on the external pull-up voltage used, RESET_OUT# can be recognized as high. RESET_OUT# is actively driven for at least 2 ms [6] after PMIC_PWR_ON is deactivated. V_1V8_ANA is recommended as the pull-up voltage, since this ensures a permanent low level at RESET_OUT#.

6: It is assumed that V_1V8_ANA is connected as on the MBa8x. Additional loads on V_1V8_ANA reduce this time.

3.2.7 Power

3.2.7.1 Power supply

The TQMa8x only requires a single power supply of 5 V ±5 %. Most of the internal voltages for module components or the i.MX 8 are provided by two PF8100 PMICs.

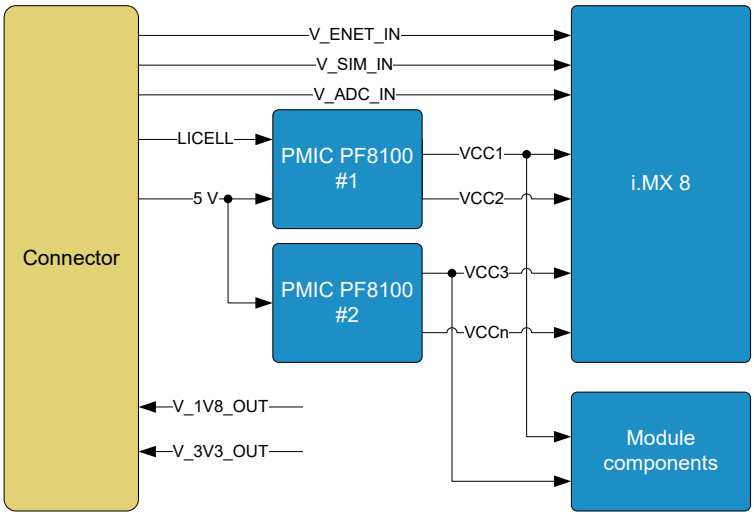

Figure 23: Block diagram power supply

1.8 V and 3.3 V are provided by the TQMa8x to supply circuitry on the carrier board.

The TQMa8x requires a supply voltage of typically 5 V ±5 %. Some of the i.MX 8 IO-Rails have different voltage ranges depending on the application. For a flexible use of the TQMa8x, these IO-Rails are connected to the TQMa8x connectors and must be supplied by the carrier board. No additional voltage regulators are required on the carrier board, since the voltage outputs V_1V8_OUT or V_3V3_OUT (see chapter 3.2.6.6) can be used for this.

Table 47: Supply voltages

Signal	TQMa8x	Voltage	Max. range	Current	Usage
V_5V_IN	X1-A2:B6	4.75 … 5.25 V	–0.3 … +6.0 V	See 3.2.6.8	– TQMa8x supply
V_ADC_IN	X1-B9	1 … 1.98 V	–0.5 … +2.1 V	20 mA (estimated)	– Supplies i.MX 8 Rail VREFH_ADC – Supply with V_1V8_OUT or other voltage on carrier board
V_SIM_IN	X1-B8	1.65 … 1.95 V or 3.0 … 3.6 V	–0.3 … +3.8 V	15 mA	– Supplies i.MX 8 Rail VDD_SIM0_1P8_3P3 – Connect to V_1V8_OUT or V_3V3_OUT on carrier board
V_ENET_IN	X1-A8	1.65 … 1.95 V or 3.0 … 3.6 V	–0.3 … +3.8 V	65 mA [7]	– Supplies i.MX 8 Rails VDD_ENET0_1P8_3P3, VDD_ENET1_1P8_2P5_3P3, and VDD_ENET_MDIO_1P8_3P3 – Connect to V_1V8_OUT or V_3V3_OUT on carrier board
V_LICELL	X2-B37	1.8 … 5.5 V	–0.5 … +6.5 V	See 3.2.3	– Supplies PMIC LICELL / SNVS domain
V_VBAT	X2-B109	2.6 … 4.2 V	–0.3 … +5.5 V	See 3.2.3	– Supplies RTC PCF85063

7: Sum of VDD_ENET0_1P8_3P3, VDD_ENET1_1P8_2P5_3P3, and VDD_ENET_MDIO_1P8_3P3.

Attention: Malfunction or destruction	
	If the absolute maximum voltages are exceeded, malfunctions may occur and components on the TQMa8x may be damaged.

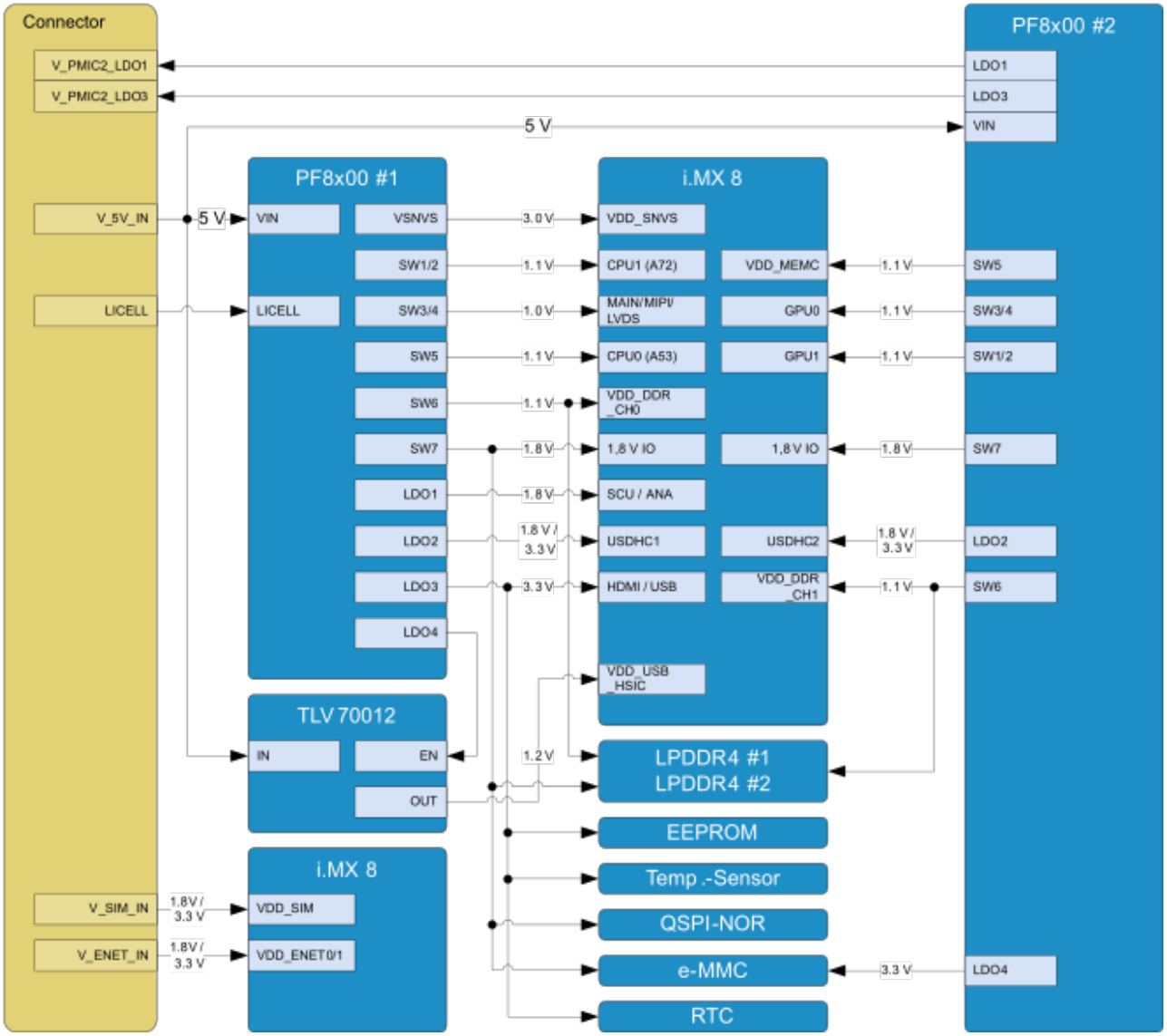

Figure 24: Block diagram PMIC Power rail of TQMa8x

3.2.7.2 V_V5_IN

The operating voltage of the TQMa8x is applied to the V_5V_IN pins. The following table lists the technical parameters of the module supply. The specified current consumptions are determined on the basis of example applications and should be regarded as a guide value, since the current consumption of the TQMa8x can differ greatly depending on the application, modes and operating system.

Table 48: Technical Data V_5V_IN

Parameter	Min.	Typ.	Max.	Unit of measurement	Note
Input voltage $V_{V\_5V\_IN}$	4,75	5,0	5,25	V	
Current consumption $I_{V\_5V\_IN}$					
Off mode		0,3		mA	PMIC_PWRON = low
Reset		161		mA	RESET_IN# = low
U-Boot-Idle		484		mA	Console prompt
Linux-Idle		435		mA	Console prompt
Linux 100 % CPU load		1470		mA	With parallel use of further interfaces, higher current consumption is to be expected
Full load		5440		mA	Theoretical worst case used as a design basis for the module supply

3.2.7.3 V_LICELL

The voltage input V_LICELL at the the TQMa8x connector (X2-B37) is used for the supply of a backup voltage (e.g. via coin cell) by one of the PMICs. Depending on the TQMa8x variant, the SNVS domain of the i.MX 8 or the external RTC PCF85063 is thus supplied.

Note: Charging	
	In addition to the pure voltage supply, voltage sources with low capacity (e.g. super-caps) connected via V_LICELL can also be charged. For this purpose the PMIC offers a constant current charging function. Further information can be found in the PMIC PF8100 data sheet.

Note: Functional scope of RTC	
	Depending on the TQMa8x variant, the range of functions is reduced in battery mode (only V_LICELL supplied), since no SNVS function of the i.MX 8 is available when using the PCF85063.

3.2.7.4 ADC

The voltage input V_ADC_IN at TQMa8x connector X1-B9 serves as voltage reference for the ADC of the i.MX 8.
This voltage is filtered and connected to the VREFH_ADC pin of the i.MX 8.
V_ADC_IN must typically be supplied with 1.8 V in order to use the ADC function of the i.MX 8.
Depending on the accuracy requirements, V_1V8_OUT can be used for this.
Further information about the ADC can be found in the i.MX 8 data sheets (2), (3).

3.2.7.5 USB_OTG[2:1]_VBUS

The voltage inputs USB_OTG1_VBUS and USB_OTG2_VBUS are used to detect the voltage of USB VBUS. They are usually connected to the VBUS voltage switched by the USB host.
Due to the different implementations of the OTG PHYs in the i.MX 8, different voltages must be used for this.

Table 49: USB VBUS

Signal	TQMa8x	Voltage	Usage
USB_OTG1_VBUS	X1-B74	typ. 5 V	Input for VBUS comparator OTG1
USB_OTG2_VBUS	X1-B63	typ. 3.3 V	Input for VBUS comparator OTG2

3.2.7.6 Voltage monitoring

The 5 V input voltage is monitored on the TQMa8x: The internal voltage monitoring of the PMIC is used, since no switching regulator for an intermediate voltage is used.
If the input voltage is too low, a reset is triggered until the input voltage is within the defined range again.

Attention: Malfunction or destruction	
	The voltage monitoring does not detect an exceedance of the maximum permitted input voltage. An excessively high supply voltage can lead to malfunctions, untimely aging or destruction of the TQMa8x.

3.2.7.7 TQMa8x voltage outputs

In addition to the TQMa8x supply input, the TQMa8x provides voltages at the TQMa8x connectors.
The following table shows these voltages:

Table 50: TQMa8x voltage outputs

Voltage	I/O	TQMa8x	Voltage	I_{max}	Usage
V_1V8_OUT	O	X1-A9:A10	1.764 … 1.836 V	700 mA	Supply for carrier board or TQMa8x feedback
V_3V3_OUT	O	X1-B10	3.201 … 3.399 V	240 mA	
V_1V8_ANA_OUT	O	X2-A42	1.649 … 1.751 V	20 mA	For Boot Configuration
V_PMIC2_LDO1	O	X1-A45	1,5 … 5 V	400 mA	Available for user; switched off by default
V_PMIC2_LDO3	O	X1-A107	1,5 … 5 V	400 mA	Available for user; switched off by default
V_LICELL	I/O	X2-B37	–	–	See Coin Cell Charger of PMIC PF8100 (4)
V_VBAT	I	X2-B109	typ. 3.3 V	–	Low-Leakage diodes to internal 3.3 V

The supply inputs for Ethernet, SIM or the ADC can be directly supplied from the voltage outputs V_1V8_OUT or V_3V3_OUT.
The required power sequencing is ensured by the voltage outputs.

Attention: Malfunction or destruction, supply outputs	
	The additional power taken from the voltage outputs results in a higher power consumption of the TQMa8x and an increased temperature of both PMICs. An efficiency of 90 % should be assumed as the base for calculating the additional power. The BOOT_MODE signals should be pulled-up to V_1V8_ANA_OUT or a voltage switched by V_1V8_ANA_OUT. This is the only way to ensure that the boot mode pins are read correctly and that no cross supply occurs. The mentioned voltages are outputs and must under no circumstances be supplied externally. The outputs are not short-circuit proof, an overload of the voltage outputs leads to a reset or restart of the power management controllers. When using the supply outputs on the mainboard, it must therefore be ensured that the specified maximum current is not exceeded.

3.2.7.8 Power-Up sequence TQMa8x / carrier board

After switching on the module supply V_5V_IN the power-up sequence of the two PMICs starts.
With a rising edge at PMIC2_PGOOD, external power supplies can be activated on the carrier board. It is recommended to logically AND PMIC1_PGOOD and PMIC2_PGOOD signals and to use the output as switching signal.

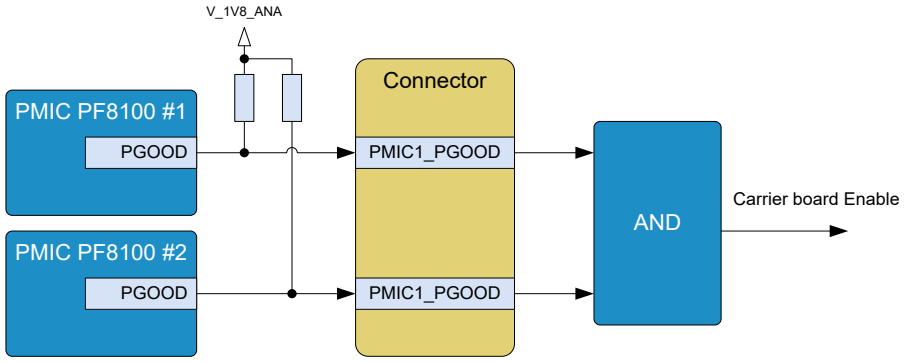

Figure 25: Block diagram PMIC PGOOD

Attention: Malfunction or destruction, Power-Up sequence	
	To avoid cross-supply and errors in the power-up sequence, no I/O pins may be driven by external components until the power-up sequence has been completed. The end of the sequence is indicated by the latest high level of signals PMIC1_PGOOD or PMIC2_PGOOD. After switching on the TQMa8x supply V_5V_IN, the power-up sequence of the two PMICs starts. The TQMa8x pins may only be supplied by external carrier board components (e.g. via low-impedance pull-ups) after the TQMa8x power-up has been completed.

Note: Configuration not as Power Good signal	
	PMIC1_PGOOD or PMIC2_PGOOD are not configured as power good signal but as GPO, because only this way an integration into the sequence of the PMIC with time offset to the last controller is possible. See section PGOOD in the PMIC PF8100 Datasheet.

3.2.7.9 PMIC

On the TQMa8x two PMICs NXP PF8100 are assembled. Both PMICs are connected to a dedicated I²C bus of the i.MX 8 (PMIC_I2C) intended for power management. Regarding the communication to the i.MX 8 a PMIC acts as master. Interrupts in the slave PMIC are transferred to the master via the INTB and XFAILB pins. The master signals interrupts directly to the i.MX 8.

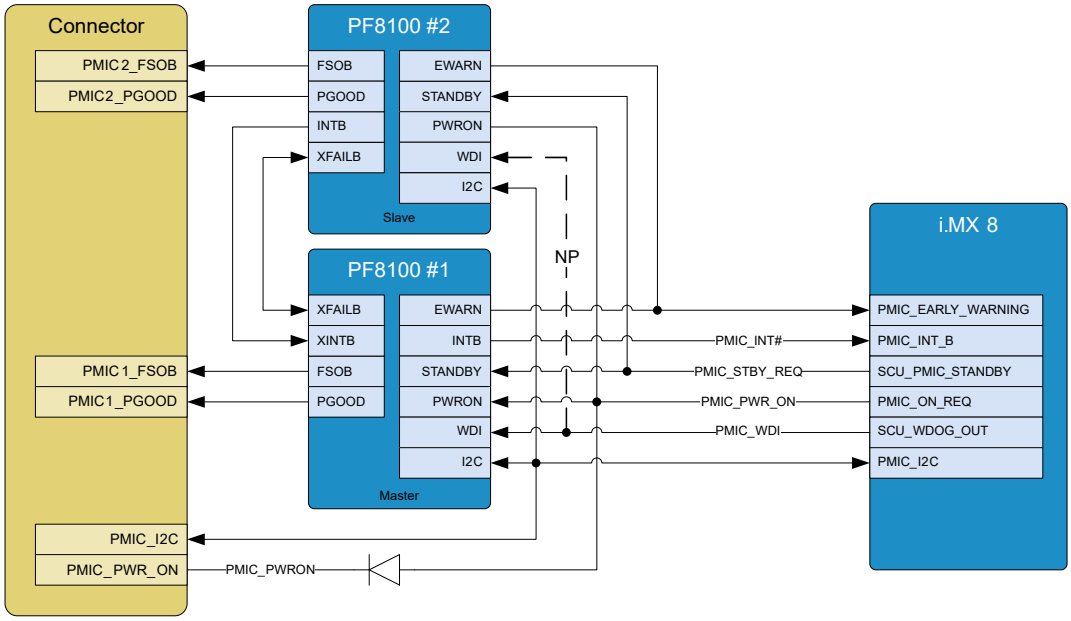

Figure 26: Block diagram PMIC signals

The following PMIC and power management signals are available on the TQMa8x connectors.

Table 51: PMIC signals

Signal	TQMa8x	I/O	Power domain	Remark
PMIC1_FSOB	X2-A52	O	V_1V8_ANA	• Output of PMIC FSOB signals • Open drain with TQMa8x-internal pull-up
PMIC2_FSOB	X2-B35			
PMIC_I2C_SCL	X1-B14	O		• Dedicated PMIC interface • Can be used for further power management on carrier board • Open drain with TQMa8x-internal pull-ups
PMIC_I2C_SDA	X1-B15	I/O		
PMIC_PWR_ON	X2-B7	I	V_SNVS_CAP	• Enable signal for PMIC (high active) • Is activated by default when V_5V_IN is switched on • To activate: Float • To deactivate: Connect to GND
PMIC1_PGOOD	X2-A53	O	V_1V8_ANA	• Low level when a power rail of the respective PMIC signals undervoltage or overvoltage • Open drain with TQMa8x-internal pull-up
PMIC2_PGOOD	X2-B36	O		

For both PMICs a module specific OTP programming is necessary. The program data was created with the tool "OTP-Request-Form" from NXP. According to the specification the PMIC can be configured via the PMIC_I2C interface after the system start.

Attention: Malfunction or destruction, PMIC programming	
	The PMICs can be controlled via the dedicated i.MX 8 I²C bus (PMIC_I2C). Improper PMIC programming may cause the i.MX 8 or other peripherals on the TQMa8x to operate outside their specification. This can lead to malfunction, deterioration or destruction of the TQMa8x.

4. MECHANICS

4.1 Connectors

The TQMa8x is connected to the carrier board with 560 pins on three connectors.
The following table shows details of the connectors used:

Table 52: TQMa8x connectors

Manufacturer	Part number	Remark
EPT	220-pin: 402-51101-51 120-pin: 402-51401-51	0.5 mm pitch

To avoid damaging the connectors of the TQMa8x as well as the connectors on the carrier board while removing the TQMa8x the use of the extraction tool MOZIa8 is strongly recommended.

Attention: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa8x for the extraction tool MOZIa8.

The following table shows some suitable mating connectors for the carrier board.

Table 53: Carrier board mating connectors

Manufacturer	Part number	Remark	Stack height
EPT	220-pin: 401-51101-51 120-pin: 401-51401-51	On MBa8x	5 mm
	220-pin: 401-55101-51 120-pin: 401-55401-51	–	8 mm

The pins assignment in Table 3 to Table 5 refers to the corresponding BSP provided by TQ-Systems.
For information regarding I/O pins in Table 3 to Table 5, refer to the i.MX 8 data sheets (2), (3).

4.2 Dimensions

Figure 27: TQMa8x dimensions, side view

The following table provides the height dimensions of the TQMa8x.

Table 54: TQMa8x height dimensions

Dimension	Value (mm)	Tolerance (mm)	Remark
A	5.10	±0.07	Board-to-Board distance
B	1.72	±0.17	PCB thickness
C	2.27	±0.15	i.MX 8 height
C1	2.05	±0.11	Inductors
D	3.98	±0.10	Space below TQMa8x
E	9.09	±0.25	Overall height to top of CPU

4.2 Dimensions (continued)

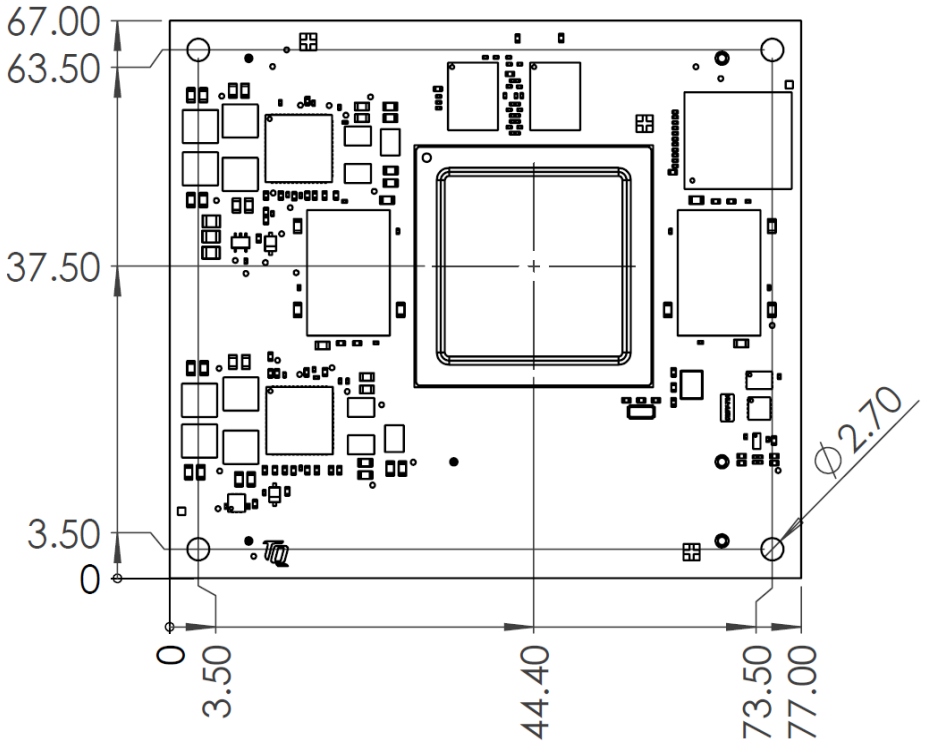

Figure 28: TQMa8x dimensions, top view

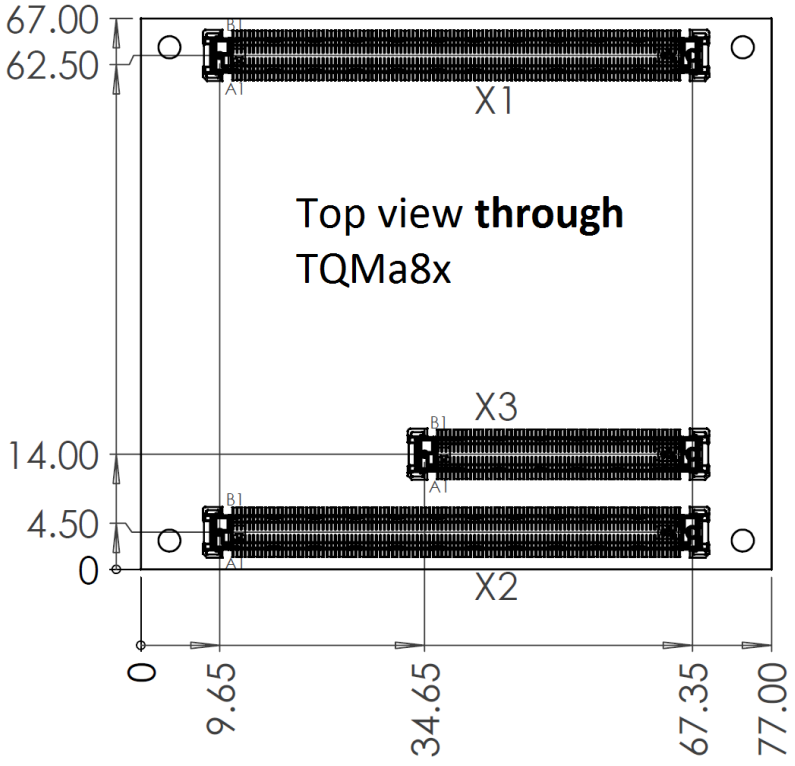

Figure 29: TQMa8x dimensions, top view **through** TQMa8x

4.3 Component placement

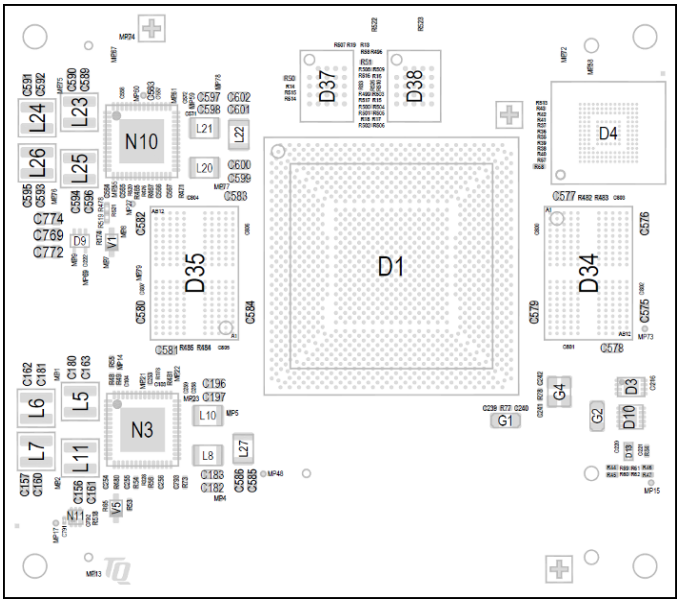

Figure 30: TQMa8x, component placement top

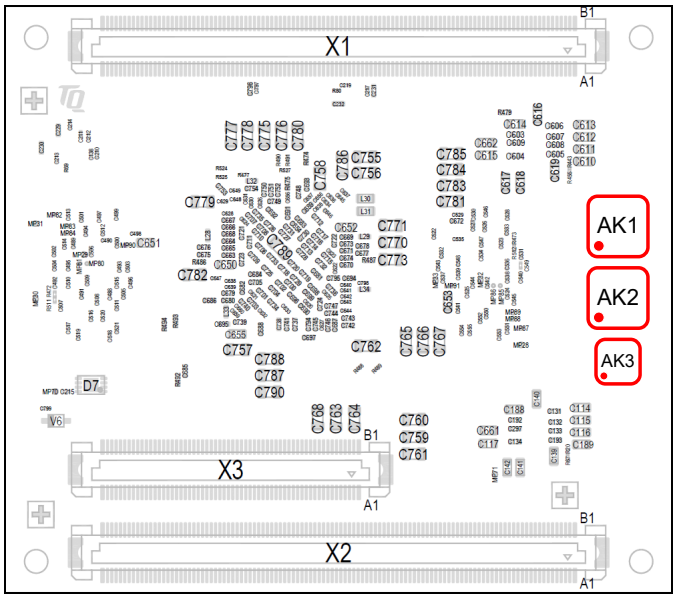

Figure 31: TQMa8x, component placement bottom

Table 55: TQMa8x labels

Label	Text
AK1	TQMa8x version, revision
AK2	MAC address (+ additional reserved MAC addresses), tests performed
AK3	Serial number

4.4 Adaptation to the environment

The TQMa8x has overall dimensions (length × width) of 77 mm × 67 mm.
The TQMa8x weighs approximately 39 g.
The TQMa8x provides four metalized mounting holes with a diameter of 2.7 mm.

4.5 Protection against external effects

As an embedded module, the TQMa8x is not protected against dust, external impact and contact (IP00).
Adequate protection has to be guaranteed by the surrounding system.

4.6 Thermal management

To cool the TQMa8x, a maximum of approximately 27,2 W must be dissipated, see Table 43 for peak currents. The cooling solution must be able to dissipate this power peak; it will never occur permanently in normal operation.
The power dissipation originates primarily in the i.MX 8, the LPDDR4 SDRAM and the PMICs.
The power dissipation also depends on the software used and can vary according to the application.
See i.MX 8 data sheets (2), (3) for further information.

Attention: Destruction or malfunction, cooling the TQMa8x	
	The TQMa8x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8 must be taken into consideration when connecting the heat sink. The i.MX 8 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8x and thus malfunction, deterioration or destruction.

4.7 Structural requirements

The TQMa8x is held in the mating connectors by the retention force of the pins (560). For high requirements with respect to vibration and shock firmness, an additional retainer has to be provided in the final product to hold the TQMa8x in its position. This can be achieved with the combination of heat sink and mounting method. Since no heavy and large components are used, there are no further requirements.

4.8 Notes of treatment

To avoid damage caused by mechanical stress, the TQMa8x may only be extracted from the carrier board by using the extraction tool MOZIa8 that can also be obtained separately.

Attention: Component placement on carrier board	
	2.5 mm should be kept free on the carrier board, on both long sides of the TQMa8x for the extraction tool MOZIa8.

5. SOFTWARE

The TQMa8x is delivered with a preinstalled boot loader U-Boot and a TQ-BSP, which is tailored for the MBa8x.
The boot loader U-Boot provides TQMa8x-specific as well as MBa8x-specific settings, e.g.:

- i.MX 8 configuration
- PMIC configuration
- SDRAM configuration and timing
- eMMC configuration
- Multiplexing
- Clocks
- Pin configuration
- Driver strengths

These settings have to be adapted, in case another bootloader, BSPs or mainboard is used. More information can be found in the Support Wiki for the TQMa8x.

6. SAFETY REQUIREMENTS AND PROTECTIVE REGULATIONS

6.1 EMC

The TQMa8x was developed according to the requirements of electromagnetic compatibility (EMC). Depending on the target system, anti-interference measures may still be necessary to guarantee the adherence to the limits for the overall system.

Following measures are recommended:

- Robust ground planes (adequate ground planes) on the printed circuit board
- A sufficient number of blocking capacitors in all supply voltages
- Fast or permanently clocked lines (e.g., clock signals) should be kept short;
  avoid interference of other signals by distance and/or shielding,
  also pay attention to frequencies and signal rise times
- Filtering of all signals, which can be connected externally
  (also "slow signals" and DC can radiate RF indirectly)
- Direct signal routing without stubs for multi-pole interfaces (e.g. LC display)

6.2 ESD

In order to avoid interspersion on the signal path from the input to the protection circuit in the system, the protection against electrostatic discharge should be provided directly at the inputs of a system. As these measures always have to be implemented on the carrier board, no special protective measures were provided on the TQMa8x.

The following measures are recommended for a carrier board:

- Generally applicable: Shielding of inputs (shielding connected well to ground / housing on both ends)
- Supply voltages: Suppressor diodes
- Slow signals: RC filtering, Zener diodes
- Fast signals: Protection components, e.g., suppressor diode arrays

6.3 Climate and operational conditions

The TQMa8x is available in three different variants with different ambient temperature ranges. The operating temperature range for the TQMa8x strongly depends on the installation situation (heat dissipation by heat conduction and convection); hence, no fixed value can be given for the TQMa8x.

Detailed information concerning the thermal characteristics is to be taken from the i.MX 8 NXP data sheets (2), (3).

In general, a reliable operation is given when the following conditions are met:

Table 56: Climate and operational conditions industrial temperature range

Parameter	Range	Remark
Ambient temperature	-25 °C to +60 °C	–
T_J i.MX 8	-40 °C to +125 °C	Industrial
T_J PMIC	(TBD)	–
Case temperature SDRAM	-40 °C to +95 °C	–
Case temperature other ICs	0 °C to +85 °C -25 °C to +85 °C -40 °C to +85 °C	Consumer Extended (Standard) Industrial
Storage temperature TQMa8x	-40 °C to +85 °C	–
Relative humidity (operating / storage)	10 % to 90 %	Not condensing

Attention: Destruction or malfunction, cooling the TQMa8x	
	The TQMa8x belongs to a performance category in which a cooling system is essential. It is the user's sole responsibility to define a suitable heat sink (weight and mounting position) depending on the specific mode of operation (e.g., dependence on clock frequency, stack height, airflow, and software). Particularly the tolerance chain (PCB thickness, board warpage, BGA balls, BGA package, thermal pad, heatsink) as well as the maximum pressure on the i.MX 8 must be taken into consideration when connecting the heat sink. The i.MX 8 is not necessarily the highest component. Inadequate cooling connections can lead to overheating of the TQMa8x and thus malfunction, deterioration or destruction.

6.4 Shock and Vibration

Table 57: Shock

Parameter	Details
Shock	According to DIN EN 60068-2-27
Shock form	Half sine
Acceleration	30 g
Residence time	10 msec
Number of shocks	3 shocks per direction
Excitation axes	6X, 6Y, 6Z

Table 58: Vibration

Parameter	Details
Oscillation, sinusoidal	According to DIN EN 60068-2-6
Frequency ranges	2 – 9 Hz, 9 – 200 Hz, 200 – 500 Hz
Wobble rate	1.0 octaves / min
Excitation axes	X– Y – Z axis
Amplitude	2 Hz … 9 Hz: 3.5 ms^{-2} 9 Hz … 200 Hz: 10 ms^{-2} 200 Hz … 500 Hz: 15 ms^{-2}

6.5 Operational safety and personal security

Due to the occurring voltages (≤5 V DC), tests with respect to the operational and personal safety have not been carried out.

6.6 Reliability and service life

The calculated MTBF of the TQMa8x is 589,555 hours @ +40 °C ambient temperature, Ground, Benign.
The TQMa8x is designed to be insensitive to shock and vibration.
High quality industrial grade connectors are assembled on the TQMa8x.

7. ENVIRONMENT PROTECTION

7.1 RoHS

The TQMa8x is manufactured RoHS compliant.

- All components and assemblies are RoHS compliant
- The soldering processes are RoHS compliant

7.2 WEEE®

The final distributor is responsible for compliance with the WEEE® regulation.

Within the scope of the technical possibilities, the TQMa8x was designed to be recyclable and easy to repair.

7.3 REACH®

The EU-chemical regulation 1907/2006 (REACH® regulation) stands for registration, evaluation, certification and restriction of substances SVHC (Substances of very high concern, e.g., carcinogen, mutagen and/or persistent, bio accumulative and toxic). Within the scope of this juridical liability, TQ-Systems GmbH meets the information duty within the supply chain with regard to the SVHC substances, insofar as suppliers inform TQ-Systems GmbH accordingly.

7.4 EuP

The Eco Design Directive, also Energy using Products (EuP), is applicable to products for the end user with an annual quantity >200,000. The TQMa8x must therefore always be seen in conjunction with the complete device. The available standby and sleep modes of the components on the TQMa8x enable compliance with EuP requirements for the TQMa8x.

7.5 Battery

No batteries are assembled on the TQMa8x.

7.6 Packaging

By environmentally friendly processes, production equipment and products, we contribute to the protection of our environment. To be able to reuse the TQMa8x, it is produced in such a way (a modular construction) that it can be easily repaired and disassembled. The energy consumption of the TQMa8x is minimised by suitable measures. The TQMa8x is delivered in reusable packaging.

7.7 Other entries

The energy consumption of the TQMa8x is minimised by suitable measures.

Because currently there is still no technical equivalent alternative for printed circuit boards with bromine-containing flame protection (FR-4 material), such printed circuit boards are still used.

No use of PCB containing capacitors and transformers (polychlorinated biphenyls).

These points are an essential part of the following laws:

- The law to encourage the circular flow economy and assurance of the environmentally acceptable removal of waste as at 27.9.94
  (Source of information: BGBl I 1994, 2705)
- Regulation with respect to the utilization and proof of removal as at 1.9.96
  (Source of information: BGBl I 1996, 1382, (1997, 2860))
- Regulation with respect to the avoidance and utilization of packaging waste as at 21.8.98
  (Source of information: BGBl I 1998, 2379)
- Regulation with respect to the European Waste Directory as at 1.12.01
  (Source of information: BGBl I 2001, 3379)

This information is to be seen as notes. Tests or certifications were not carried out in this respect.

8. APPENDIX

8.1 Acronyms and definitions

The following acronyms and abbreviations are used in this document:

Table 59: Acronyms

Acronym	Meaning
ADC	Analog/Digital Converter
ARM®	Advanced RISC Machine
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
CSI	Camera Serial Interface (MIPI)
DDC	Display Data Channel
DDR	Double Data Rate
DNC	Do Not Connect
DSI	Display Serial Interface
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
eMMC	embedded Multimedia Card
EN	Europäische Norm
ESAI	Enhanced Serial Audio Interface
ESD	Electrostatic Discharge
EU	European Union
EuP	Energy using Products
FD	Flexible Data Rate
fps	frames per second
FR-4	Flame Retardant 4
GPIO	General-Purpose Input/Output
HDMI	High Definition Multimedia Interface
HSIC	High-Speed Inter-Chip
I/O	Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IO	Input/Output
IP00	Ingress Protection 00
JEDEC	Joint Electronic Device Engineering Council
JTAG®	Joint Test Action Group
LDO	Low Drop-Out regulator
LPDDR4	Low Power DDR4
LVDS	Low-Voltage Differential Signalling
MAC	Media Access Control
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
MMC	Multimedia Card
MOZI	Module extractor (Modulzieher)
MTBF	Mean (operating) Time Between Failures

8.1 Acronyms and definitions (continued)

Table 52: Acronyms (continued)

Acronym	Meaning
NAND	Not-And
NC	Not Connected
NOR	Not-Or
OBFF	Optimized Buffer Flush/Fill
OTG	On-The-Go
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PCMCIA	People Can't Memorize Computer Industry Acronyms
PHY	Physical (layer of the OSI model)
PMIC	Power Management Integrated Circuit
PWM	Pulse-Width Modulation
PWP	Permanent Write Protected
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
REACH®	Registration, Evaluation, Authorisation (and restriction of) Chemicals
RF	Radio Frequency
RFU	Reserved for Future Usage
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
RoHS	Restriction of (the use of certain) Hazardous Substances
ROM	Read-Only Memory
RTC	Real-Time Clock
RWP	Reversible Write Protected
S/PDIF	Sony-Philips Digital Interface Format
SAI	Serial Audio Interface / Synchronous Audio Interface
SATA	Serial ATA
SCU	System Control Unit
SD	Secure Digital
SDIO	Secure Digital Input/Output
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
SS	Super-Speed
SVHC	Substances of Very High Concern
TBD	To Be Determined
UART	Universal Asynchronous Receiver / Transmitter
UM	User's Manual
USB	Universal Serial Bus
uSDHC	Ultra-Secured Digital Host Controller
WEEE®	Waste Electrical and Electronic Equipment

8.2 References

Table 60: Further applicable documents

No.	Name	Revision / Date	Company
(1)	Mask Set Errata for Mask 1N94W, IMX8_1N94W_Rev2.pdf	Rev. 2 / 05/2021	NXP
(2)	i.MX 8QuadMax Automotive and Infotainment Applications Processors, IMX8QMAEC_Rev2.pdf	Rev. 2 / 05/2021	NXP
(3)	i.MX 8QuadPlus Automotive and Infotainment Applications Processors, IMX8QPAEC_Rev2.pdf	Rev. 2 / 05/2021	NXP
(4)	PMIC PF8100 data sheet, PF8100_PF8200 v11.pdf	Rev. 11 / 24.02.2021	NXP
(5)	i.MX 8 MEK Platform MCIMX8QM CPU (EVK), SPF-29420_C2.pdf	Rev. C / 17 Sept 2018	NXP
(6)	i.MX 8 QM/i.MX 8 QXP Hardware Developers Guide, IMX8_Hardware_Developers_Guide_v2.4.pdf	Rev. 2.4p / 6 Jun 2021	NXP
(7)	RTC PCF85063 data sheet, PCF85063A.pdf	Rev. 7 / 23 Jan 2018	NXP
(8)	i.MX 8QuadMax Applications Processor Reference Manual, IMX8QMRM_Rev0.pdf	Rev. 0 / 09/2021	NXP
(9)	MBa8x User's Manual	– current –	TQ-Systems
(10)	TQMa8x Support-Wiki	– current –	TQ-Systems

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